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S1R72U06
SPI
Interface Manual

SEIKO EPSON CORPORATION

Rev. 1.01

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Scope

This document applies to the S1R72U06 serial (UART/SPI) - USB Host/Device bridge LSI, which supports USB 2.0 FS/LS.

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1. Overview

This is the SPI Interface Manual for the S1R72U06 serial (UART/SPI) - USB Host/Device bridge LSI (hereinafter referred to as the "LSI"), which supports USB 2.0 FS/LS.

This document explains the various commands and protocols supporting SPI.

For details of hardware control and operating procedures for the LSI, refer to the *S1R72U06 Application Note*.

This document uses the terms defined in the section on "Terminology" in the *S1R72U06 Technical Manual*.

2. Command Specifications

The LSI has two command systems, depending on the SIO (UART/SPI).

SPI controls using registers and EI requests (hereinafter referred to as “EIreq”).

For information on UART, refer to the *S1R72U06 UART Interface Manual*.

There are three EIreq types with differing functions, as follows.

- Control EI request:·····Common
- HID Class EI request: ·····For USB (Host/Device) HID Class only
- MSC EI request: ·····For USB Host MSC only

EIreq is a command consisting of three bytes for “Block size”, “Control code”, and “EIreq code”, and “Information data” (not included in some EIreq).

Data and notification information (status information, event information, error information) read from the LSI has the EIreq value (refer to the relevant EIreq for details) written by the Main CPU added at the start as an EI header (hereinafter referred to as “EIhead”). The Main CPU should check the EIhead to determine if the data is in response to an EIreq.

The XIRQ_STATUS and XIRQ_EVENT pins may change depending on the register or EIreq protocol.

The explanations in the following sections use the abbreviations shown in Table 2.1.

Table 2.1 Abbreviations

Abbreviation	Full description
Tx	MOSI pin
Rx	MISO pin
xSTATUS	XIRQ_STATUS pin
xEVENT	XIRQ_EVENT pin
Stat	Status information
Event	Event information
Error	Error information

Abbreviation	Full description
reg	Register
size	Block size
code	Control code
cmd	EIreq code
Info	Information data*
D	Data*

* Multiple Information data and multiple data are described as shown below in examples 1 and 2, respectively.

Example 1 When Information data exist from Block 3 to Block 5

Block 3: Info0, Block 4: Info1, Block 5: Info2

Example 2 When multiple data exist

D0 to Dn, D00 to D0n, D10 to D1n, Dm0 to Dmn

2.1 Terminology

The terminology used in this manual is defined as shown below.

THROUGH command ..... Generic term for the MSC "STORAGE COMMAND THROUGH (6) to (16)".

Ended ..... "Command Through Ended event" that can be specified by the MSC THROUGH command.

Ended notification ..... Notification of Ended event information using the Ended "permitted" setting.

Ended non-notification ..... Non-notification of Ended event information using the Ended "prohibited" setting.

2.2 Usage conditions

(1) "reserved" for each of the command settings should be set to "0".

(2) The Main CPU must be accessed while checking the status information included in each subsequent protocol. For details of status information, refer to the description for each protocol.

(3) The Main CPU must process events occurring first. Unforeseen states (data errors or malfunction) may occur if other processes (e.g. writing EIreq unrelated to events) are performed after events have occurred.

(4) "EIRequest" (01h) must first be accessed in order to transmit an EIreq.

(5) Other EIreqs cannot be received while an EIreq is being processed. Therefore, if an error occurs during EIreq processing, the LSI transfers error information after the processing has ended.

(6) EIreqs can be written when the status is "Idle". Writing in states other than "Idle" will be ignored as invalid access.

(7) Data should be written after the status information has changed to "TranRdy". Writing in states other than "TranRdy" will be ignored as invalid access.

(8) When reading data, check for the presence of following data using the status information. "TranRdy" indicates that data will follow. "Idle" indicates that data transfer is complete.

(9) "RcvShort" in the status information indicates the data to follow is shorter than the Burst size.

(10) Data for reading or writing is transferred in Burst size units.
Once Burst transfer starts ("SendData" (04h) or "ReceiveData" (85h)), other registers cannot be accessed until the transfer is complete.

(11) "SRST" (47h) can be used with HID Class. It cannot be used with MSC.

(12) The status information changes to "Idle" when the EIreq processing is completed. After that, a waiting time of 100 μsec or more is necessary before writing of the following EIreq.
For example, in "RECV REPORT" (23h), it is necessary to wait after "Stat" is acquired in the period when "Internal State" is "Idle" in protocol procedure (4) or (5).

2.3 Precautions

(1) Errors or malfunction may occur if commands other than the registers or EIreqs stipulated below are written in error. If an EIreq error occurs, check that the values have been set correctly and re-write.

(2) The same event may occur in event management for the LSI depending on the baud rate and read timing from the Main CPU.

(3) Check that the status is “TranRdy” before reading or writing data. Data cannot be read or written correctly unless the status is “TranRdy”.

(4) The LSI asserts the XIRQ_EVENT pin when an event occurs, even during command processing.

(5) Error information should be checked when the status is “Idle”. Information cannot be checked correctly in other states.

(6) Accessing a register for which the data transfer direction differs (“SendData” (04h) for reading and “ReceiveData” (85h) for writing) will be ignored as invalid access.

3. Sequences

This section describes sequences of steps for various procedures between the Main CPU and the LSI.

3.1 Register access

Figure 3.1 illustrates register access for writing from the Main CPU to the LSI.

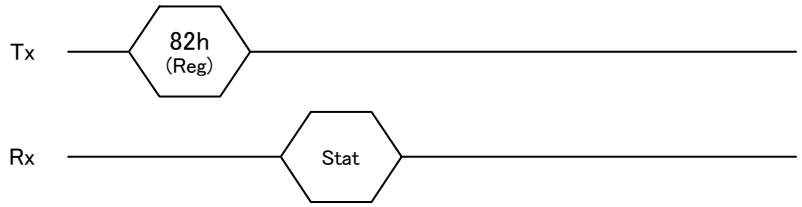


Figure 3.1 Register access

3.2 EI request

Figure 3.2 illustrates the EIreq for writing from the Main CPU to the LSI.

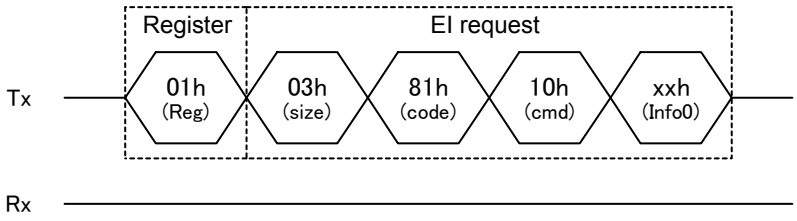


Figure 3.2 EIreq

3.3 Data writing

Figure 3.3 illustrates the sequence of steps for writing data from the Main CPU to the LSI.

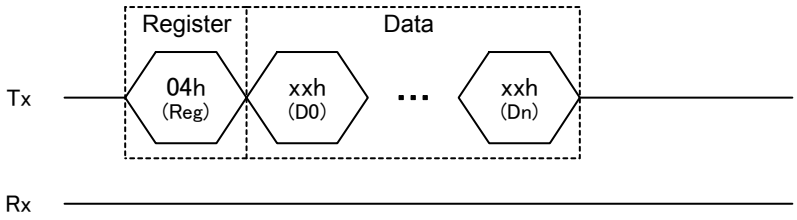


Figure 3.3 Data writing

3.4 Data reading

Figure 3.4 illustrates the sequence of steps for reading data from the LSI by the Main CPU.

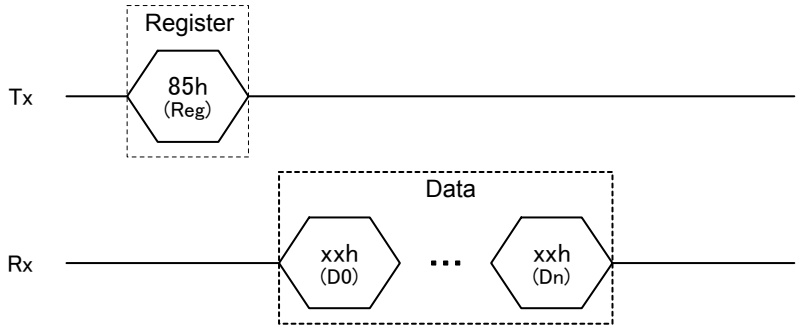


Figure 3.4 Data reading

4. Registers

The Main CPU should access registers by writing the addresses listed in Table 4.1. Any EIreq used should be written after the “EIRequest” (01h) register.

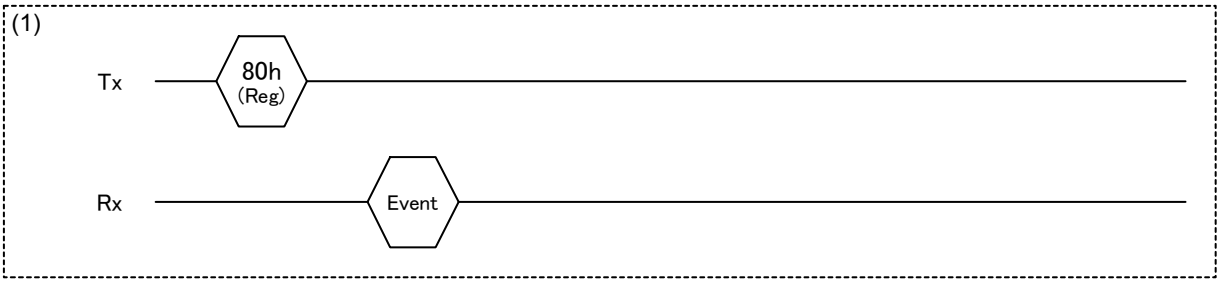
Table 4.1 Registers

Address	Register	Access	Description
80h	Event	Read	Event information acquisition register
01h	EIRequest	Write	EI request write register
82h	Status	Read	Status information acquisition register
83h	ErrorInfo	Read	Error information acquisition register
04h	SendData	Write	Data write register
85h	ReceiveData	Read	Data read register
86h	ReceiveDataSize	Read	Short data size acquisition register
47h	SRST	Write	Soft reset register

4.1 80h_Event

This register is used to obtain event information from the LSI. For more information on event information, refer to the *S1R72U06 Technical Manual*.

Access using protocol procedure (1).



4.2 01h_EIRequest

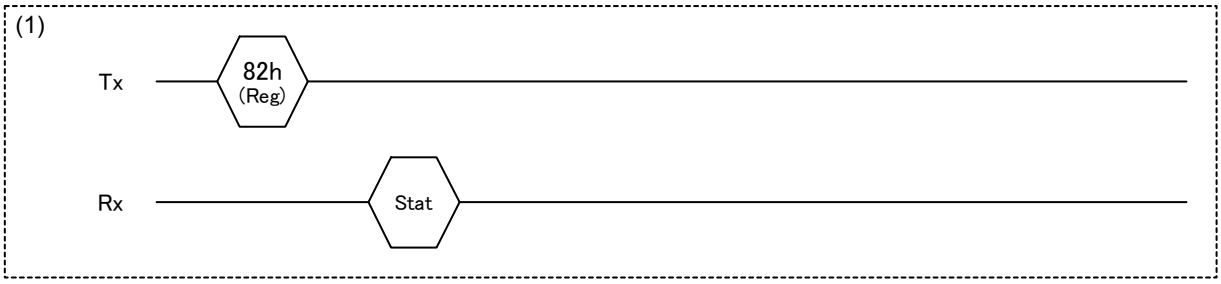
This register is used for EI requests by the Main CPU.

For detailed information on protocol procedures, refer to the discussion of the EI request in question.

4.3 82h_Status

This register is used to obtain status information from the LSI. For more information on status information, refer to the *S1R72U06 Technical Manual*.

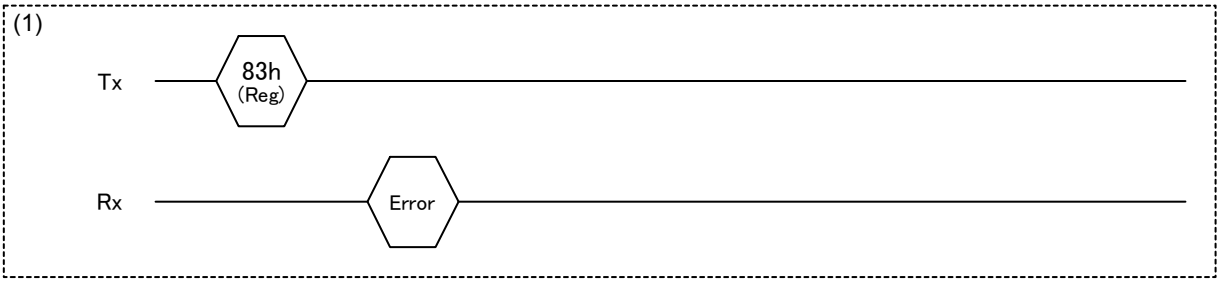
Access using protocol procedure (1).



4.4 83h_ErrorInfo

This register is used to obtain error information from the LSI. For more information on error information, refer to the *S1R72U06 Technical Manual*.

Access using protocol procedure (1).



4.5 04h_SendData

This register is used to write data to the LSI.

For detailed information on protocol procedures, refer to the discussion of the EI request in question.

4.6 85h_ReceiveData

This register is used to read data from the LSI.

For detailed information on protocol procedures, refer to the discussion of the EI request in question.

4.7 86h_ReceiveDataSize

Used when the size of the last data is less than the Burst size.

This register is used to check the valid data size.

For detailed information on protocol procedures, refer to the discussion of the EI request in question.

4.8 47h_SRST

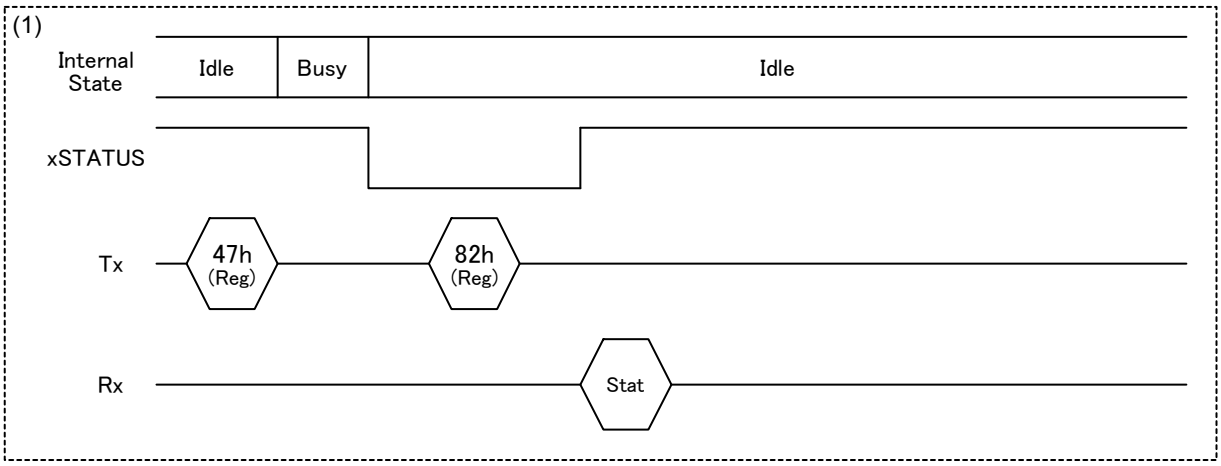
Used for soft resets, it can also be used with HID Class.

4.8.1 Device Idle State

Shown below is the protocol for the Device from the **Idle** state. Access using protocol procedure (1).

xSTATUS in (1) is asserted when abort processing has ended for the LSI. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.

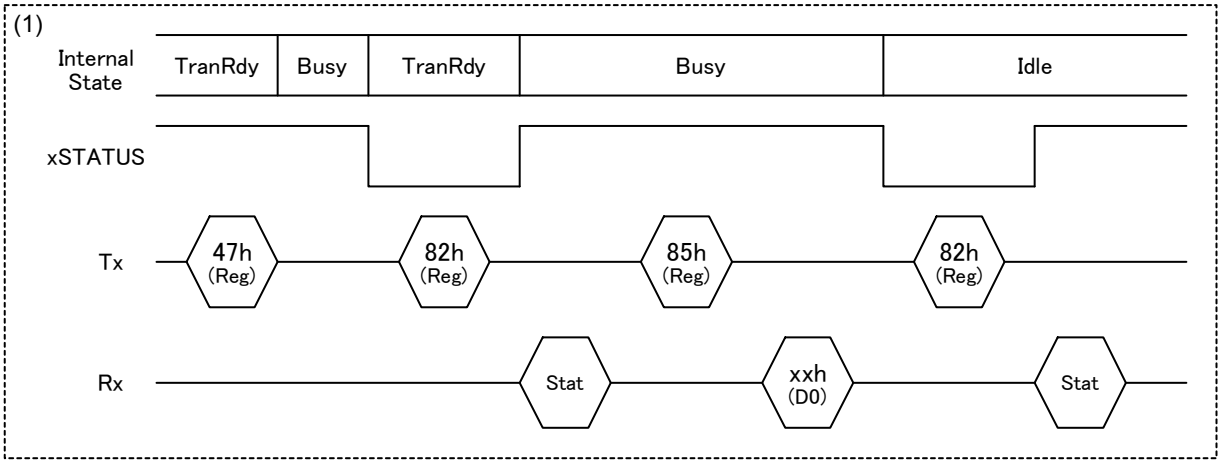


4.8.2 Device TranRdy State

Shown below is the protocol from the **TranRdy** state for the Device when reading. Access using protocol procedure (1). For detailed information on the negate timing, refer to (1).

The first xSTATUS in (1) is asserted. If the status information is **TranRdy**, read 1 byte of dummy data using "ReceiveData" (85h). Once abort processing has ended for the LSI, the second xSTATUS is asserted.

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.

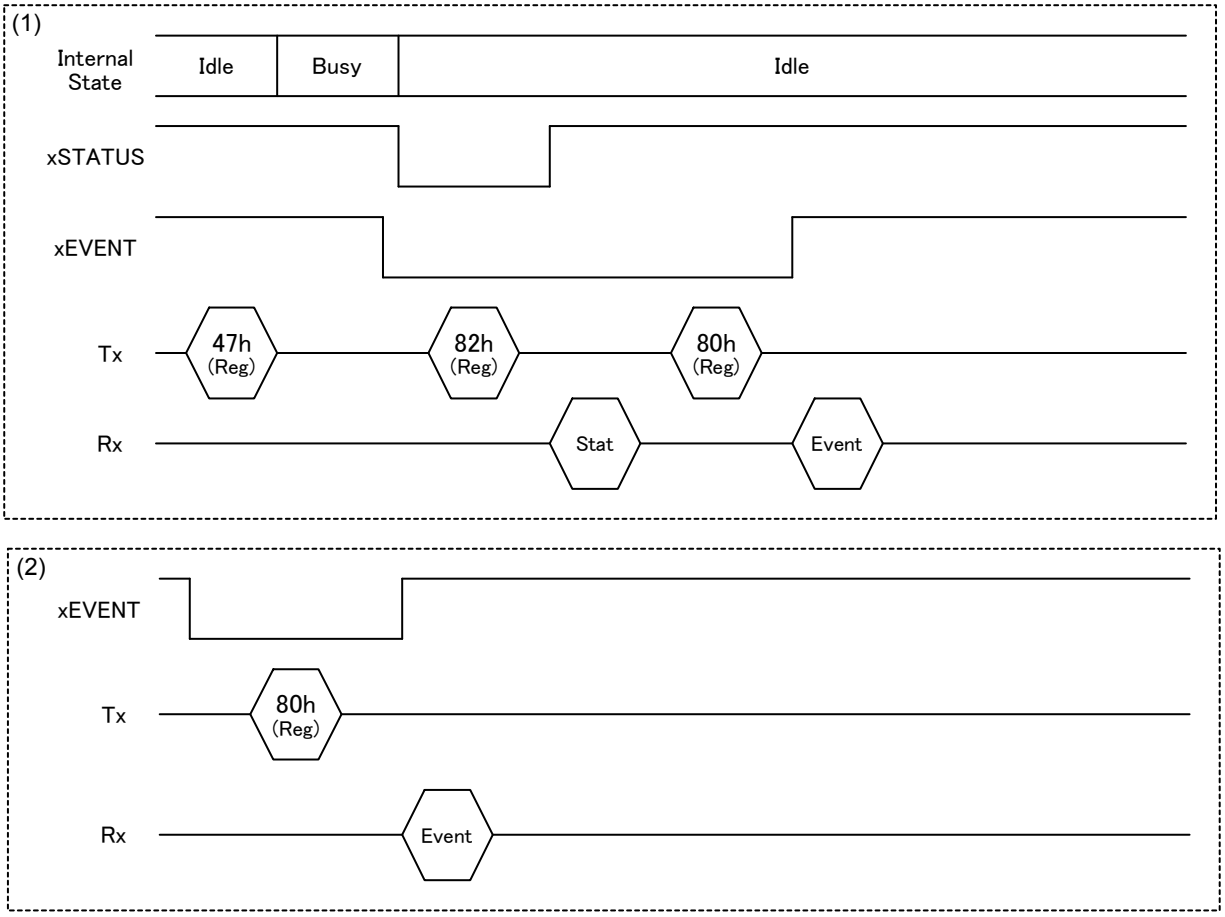


4.8.3 Host Idle State

Shown below is the protocol for the Host from the **Idle** state. Access using protocol procedures (1) and (2). For detailed information on pin negate timing, refer to (1) and (2).

xEVENT and xSTATUS in (1) are asserted when abort processing has ended for the LSI (xEVENT comes first). The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state, then acquire event information.

When the Device is reconnected, xEVENT in (2) is asserted. The Main CPU should acquire event information.



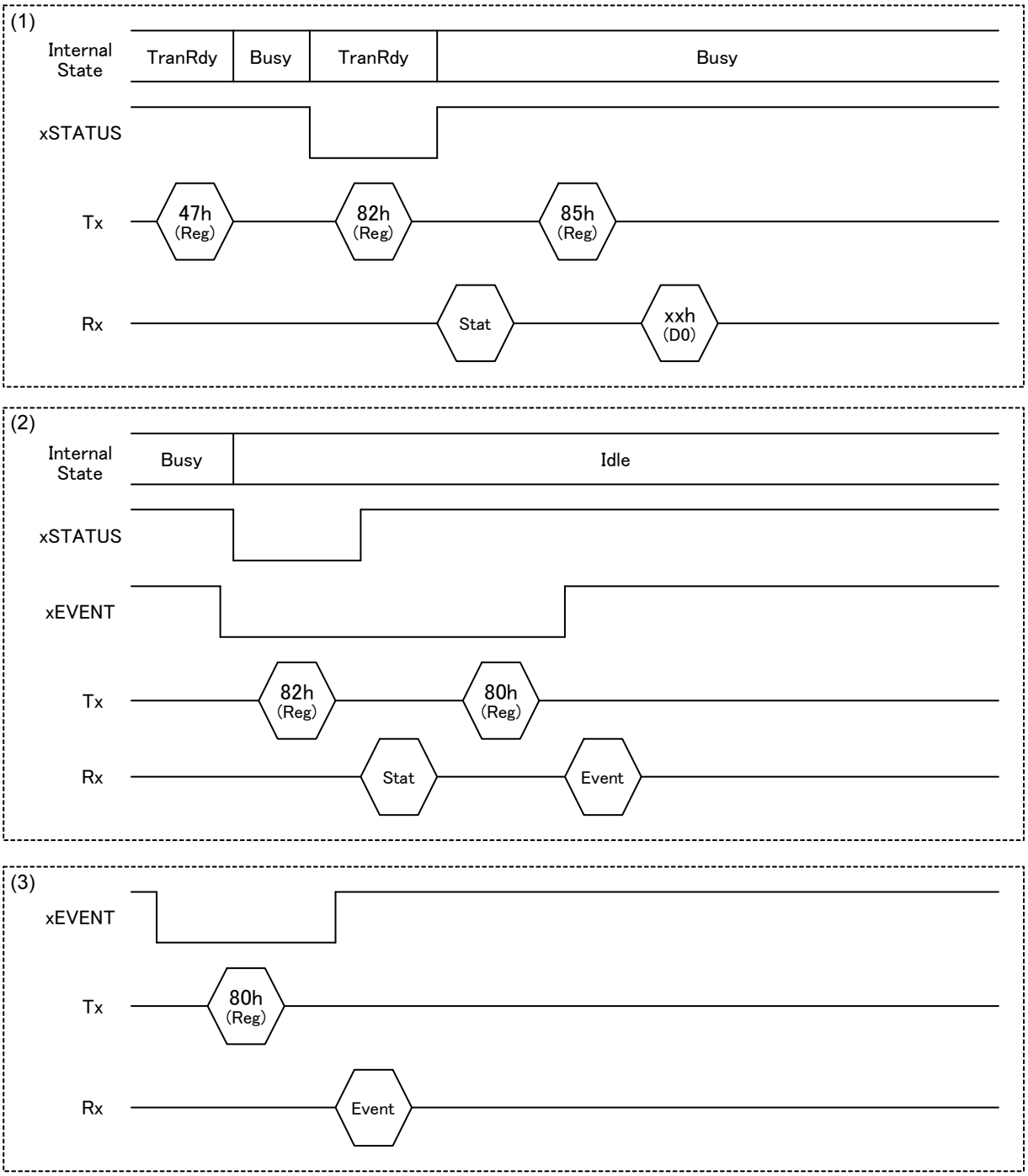
4.8.4 Host TranRdy State

Shown below is the protocol from the **TranRdy** state for the Host when reading. Access using protocol procedures (1) to (3). For detailed information on pin negate timing, refer to (1) to (3).

If the status information in (1) is **TranRdy**, read 1 byte of dummy data using "ReceiveData" (85h).

xEVENT and xSTATUS in (2) are asserted when abort processing has ended for the LSI (xEVENT comes first). The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state, then acquire event information.

When the Device is reconnected, xEVENT in (3) is asserted. The Main CPU should acquire event information.



5. Control EI Requests

Table 5.1 lists the control EI requests. These EIreqs are used for both HID Class and MSC.

The following sections describe the command parameters and protocols.

Table 5.1 Control EI requests

Control code	EIreq code	EIreq name	Description
00h	00h	BURST SIZE	Burst size setting
	01h	SLEEP	Sleep setting
	02h	DOWNLOAD	Download execution
	03h	LSI SETTING	LSI-specific setting

5.1 Usage conditions

(1) The LSI switches to Sleep state when the Main CPU acquires status information using the “SLEEP” (01h) protocol.

5.2 Precautions

(1) The read Burst size must be set to a size that can be correctly read by the Main CPU.

5.3 00h_BURST SIZE

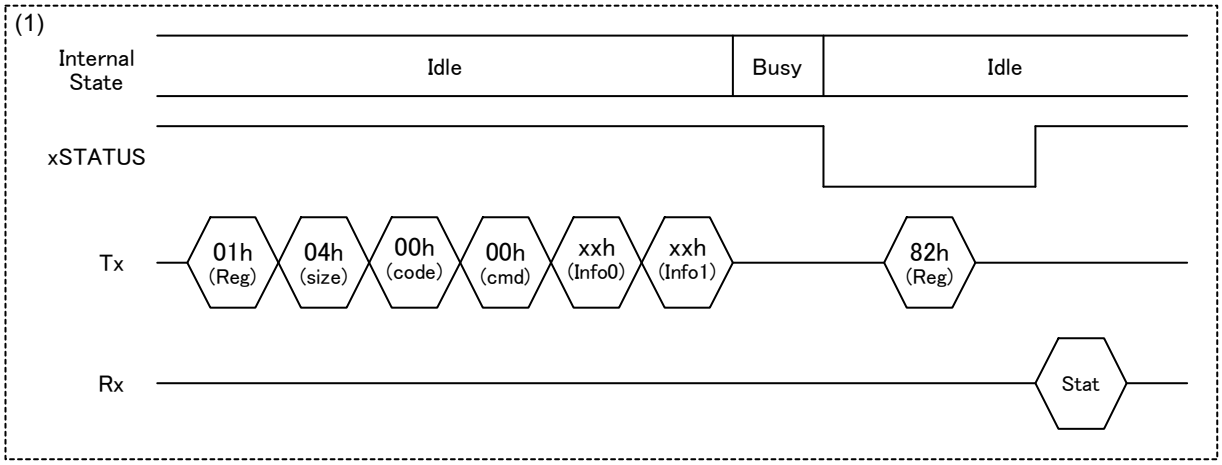
This sets the Burst size. Independent Burst sizes can be set for reading and writing. A maximum Burst size can be set for writing, but choose carefully when setting the Burst size for reading. Refer to "5.2 Precautions" for more information.

Table 5.2 BURST SIZE

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	00h	Fixed value
	EIreq code	2	00h	Fixed value
	Information data	3	xxh	Burst size for reading 01h to 80h (default = 01h)
		4	xxh	Burst size for writing 01h to 80h (default = 80h)

Access using protocol procedure (1).

The LSI asserts xSTATUS in (1) when command processing has ended. For detailed information on negate timing, refer to (1). The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.



5.4 01h_SLEEP

This switches the LSI to the Sleep state. For detailed information on how to reset from the Sleep state, refer to "Power management" in the *S1R72U06 Application Note*.

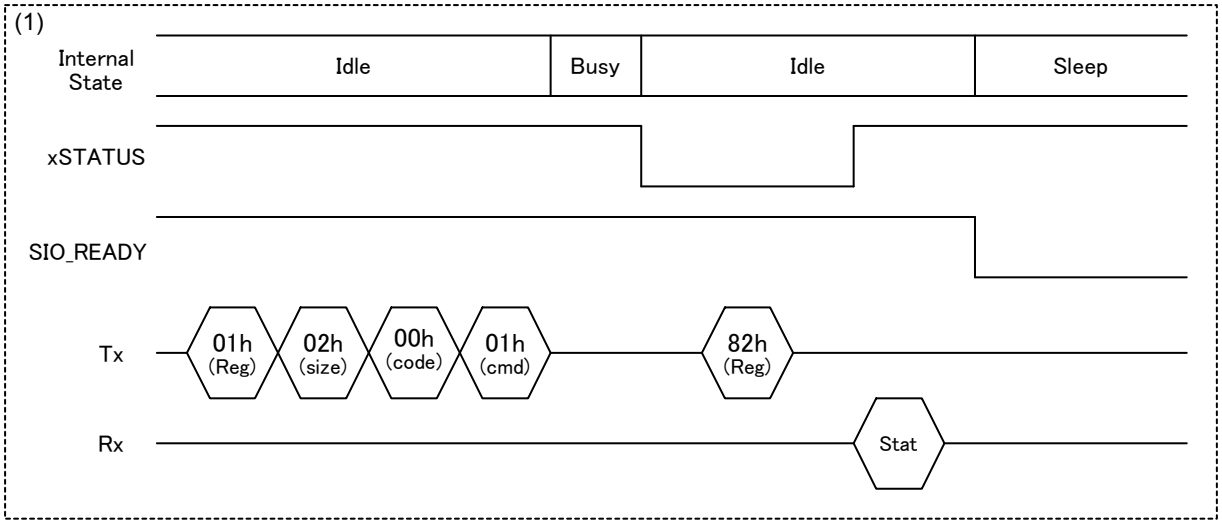
Table 5.3 SLEEP

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	02h	Total for Control code + EIreq code
	Control code	1	00h	Fixed value
	EIreq code	2	01h	Fixed value

Access using protocol procedure (1).

The LSI asserts xSTATUS in (1) when command processing has ended. For detailed information on negate timing, refer to (1). The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.

The LSI is switched to the Sleep state after status information is transferred. The SIO_READY pin is switched to "Low" at the same time.



5.5 02h_DOWNLOAD

This downloads TPL and descriptors to the LSI. For information on how to create download data, refer to the *S1R72U06 Development Support Manual*. For detailed information on TPL and the descriptors, refer to the *S1R72U06 Technical Manual*.

This EIreq can be executed when "HID START" (10h) or "MSC START" (30h) are set to "Stop".

Table 5.4 DOWNLOAD

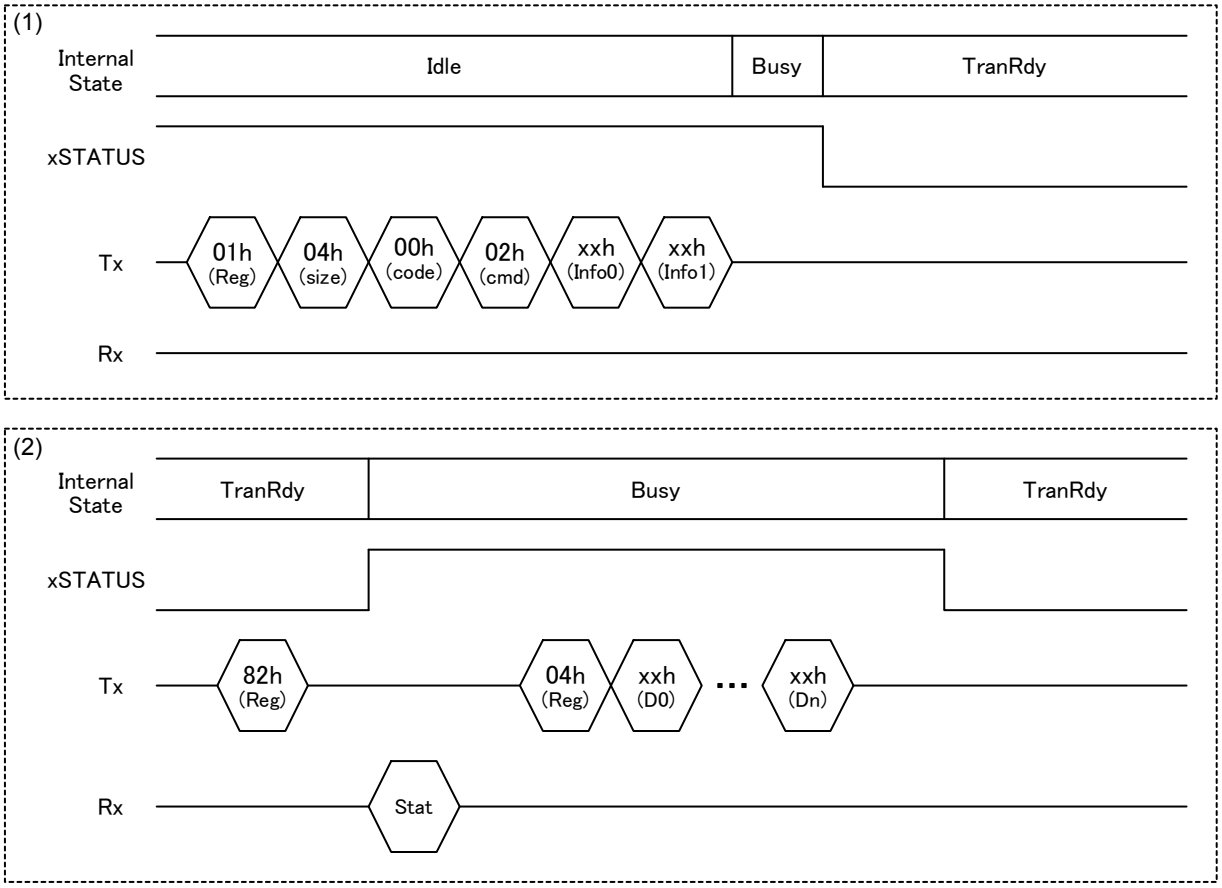
Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	00h	Fixed value
	EIreq code	2	02h	Fixed value
	Information data	3	xxxxh	Download data size 0001h to FFFFh (Block4: MSB, Block3: LSB)
		4		
Data		-	xxh	Download data

Access using protocol procedures (1) to (3). For detailed information on pin negate timing, refer to (1) to (3).

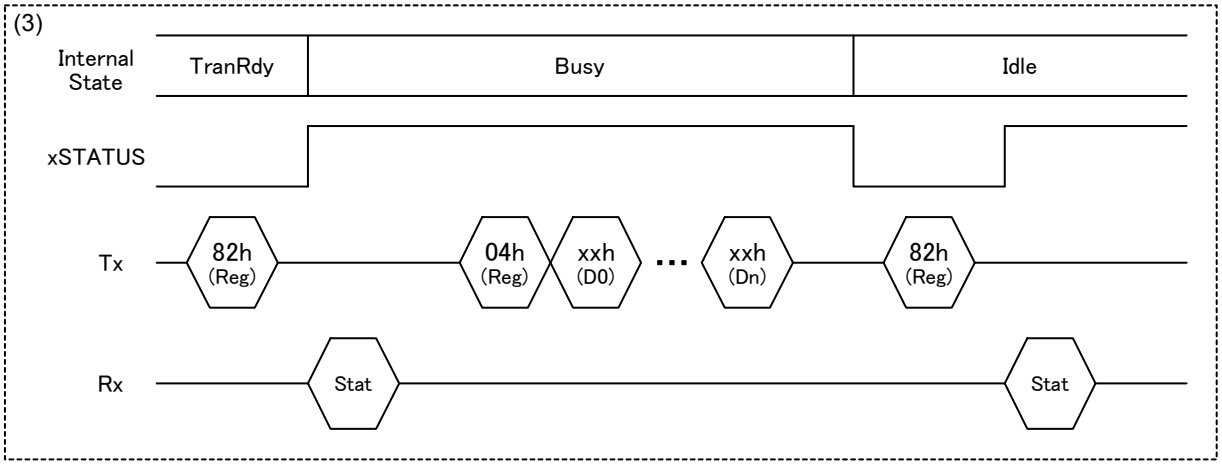
If the LSI is in the **TranRdy** state, xSTATUS in (1) is asserted.

The Main CPU should acquire status information in (2) and write the data after confirming that the status information is in the **TranRdy** state. "SendData" (04h) is used to write data. To continue writing (in Burst units), repeat the protocol in (2).

The final protocol for writing data is as shown in (3).



Confirm that the status information in (3) is in the **TranRdy** state and write using "SendData" (04h). After writing, acquire status information to confirm that the LSI is in the **Idle** state.



5.6 03h_LSI SETTING

This sets the LSI CLKOUT pin and VBUS detection for Host operation. Refer to the *S1R72U06 Data Sheet* for more information on the CLKOUT pin. For more information on VBUS detection, refer to the *S1R72U06 Technical Manual*.

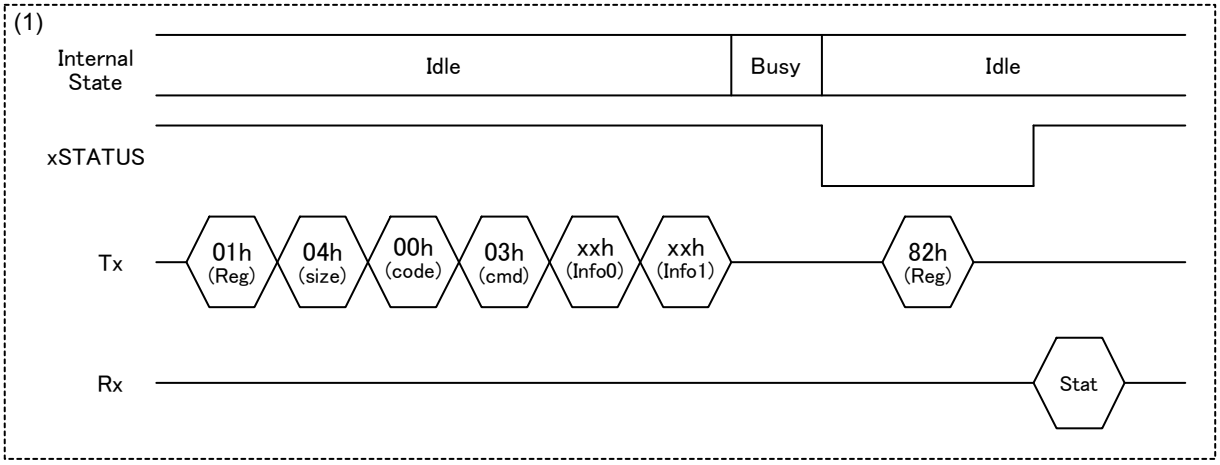
Table 5.5 LSI SETTING

Content		Block	Value	Description			
Register		-	01h	EIRequest			
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data			
	Control code	1	00h	Fixed value			
	EIreq code	2	03h	Fixed value			
	Information data	3	xxh	Clock output setting			
					Bit	Content	Setting value
					7	Output setting	0b: Output prohibited 1b: Output permitted (default)
					6-4	reserved	
					3-0	Frequency setting (valid when Bit 7 = 1b)	0000b: 48 MHz (default) 0001b: 24 MHz 0010b: 12 MHz 0100b: 6 MHz 1000b: 3 MHz
		4	xxh	VBUS setting			
					Bit	Content	Setting value
					7	Over Current detection setting	0b: Detection prohibited 1b: Detection permitted (default)
					6-0	reserved	

Access using protocol procedure (1).

The LSI asserts xSTATUS in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.



6. HID Class EI Requests

Table 6.1 lists the HID Class EI requests. These EIreqs are used for HID Class only.

The command parameters and protocols are described in the following sections.

Table 6.1 HID Class EI requests

DEVICE		HOST		EIreq name	Description
Control code	EIreq code	Control code	EIreq code		
81h	10h	C1h	10h	HID START	HID Class control
	-		11h	REPORT ID REGISTRATION	Report ID registration information setting
	-		12h	DEVICE POWER MANAGEMENT	Power management
	-		13h	DEVICE RESET	USB BUS reset
	20h		20h	SEND FEATURE REPORT	Feature Report write
	21h		21h	RECV FEATURE REPORT	Feature Report read
	22h		22h	SEND REPORT	Report write
	23h		23h	RECV REPORT	Report read
	24h		-	INITIAL FEATURE REPORT	Feature Report initialization setting
	25h		-	GET PROTOCOL MODE	Protocol mode read
	-		24h	GET DESCRIPTOR	Descriptor read

6.1 Usage conditions

(1) HID Class EI requests are assumed to be used after “HID START” (10h) has been set to “Start”. The only HID Class EI request that can be used with “HID START” (10h) set to “Stop” is “INITIAL FEATURE REPORT” (24h). For more details, refer to “HID Class Device initialization flow” in the *S1R72U06 Application Note*.

(2) EIreqs cannot contain data with differing Report IDs.

(3) It is not possible to divide into multiple EIreqs when writing Report data.

(4) For details of Report settings, refer to the *S1R72U06 Technical Manual*.

6.2 Precautions

(1) The corresponding code should be used, as the “Control code” will vary depending on the USB function (Host/Device).

(2) The LSI will issue an error notification if the Main CPU issues a read command (such as “GET DATA” (F5h) or “RECV REPORT” (23h)) when there is no data to be transferred from the LSI.

(3) The Host “HID START” (10h) should use “Report Protocol HID Class Start” if it is expected that a standard HID Class Device will be connected. “Boot Protocol HID Class Start” should be used when it is necessary to restrict to Boot Protocol dedicated Device.

6.3 10h_HID START

This sets HID Class control for the USB. Device settings are shown in Table 6.2; the Host settings are shown in Table 6.3.

Table 6.2 Device HID START

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	03h	Total for Control code + EIreq code + Information data
	Control code	1	81h	Fixed value
	EIreq code	2	10h	Fixed value
	Information data	3	xxh	Mode setting 00h: HID Class Stop (default) 01h: Low Speed HID Class Start 02h: Full Speed HID Class Start 03h to FFh: reserved

Table 6.3 Host HID START

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	C1h	Fixed value
	EIreq code	2	10h	Fixed value
	Information data	3	xxh	Protocol mode setting 00h: HID Class Stop (default) 01h: Report Protocol HID Class Start 02h: Boot Protocol HID Class Start 03h to FFh: reserved
		4	xxh	Interrupt cycle setting 00h: Response only when change occurs 01h to FFh: Responds at specified frequency of between 4 and 1,020 ms

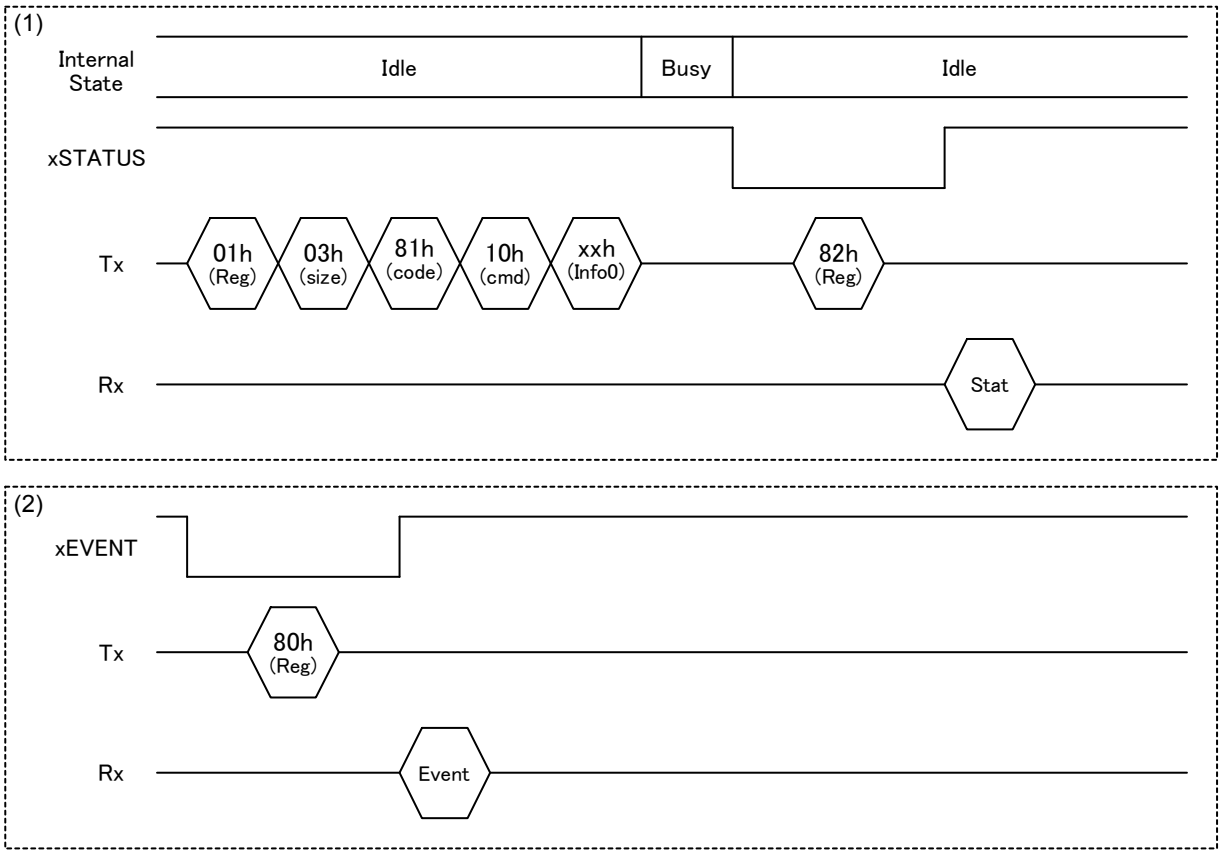
6.3.1 Device

The Device protocol is shown below.

Access using protocol procedures (1) and (2). For detailed information on pin negate timing, refer to (1) and (2).

The LSI asserts xSTATUS in (1) when command processing has ended. The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.

When connected to the Host, xEVENT in (2) is asserted. The Main CPU should acquire event information.



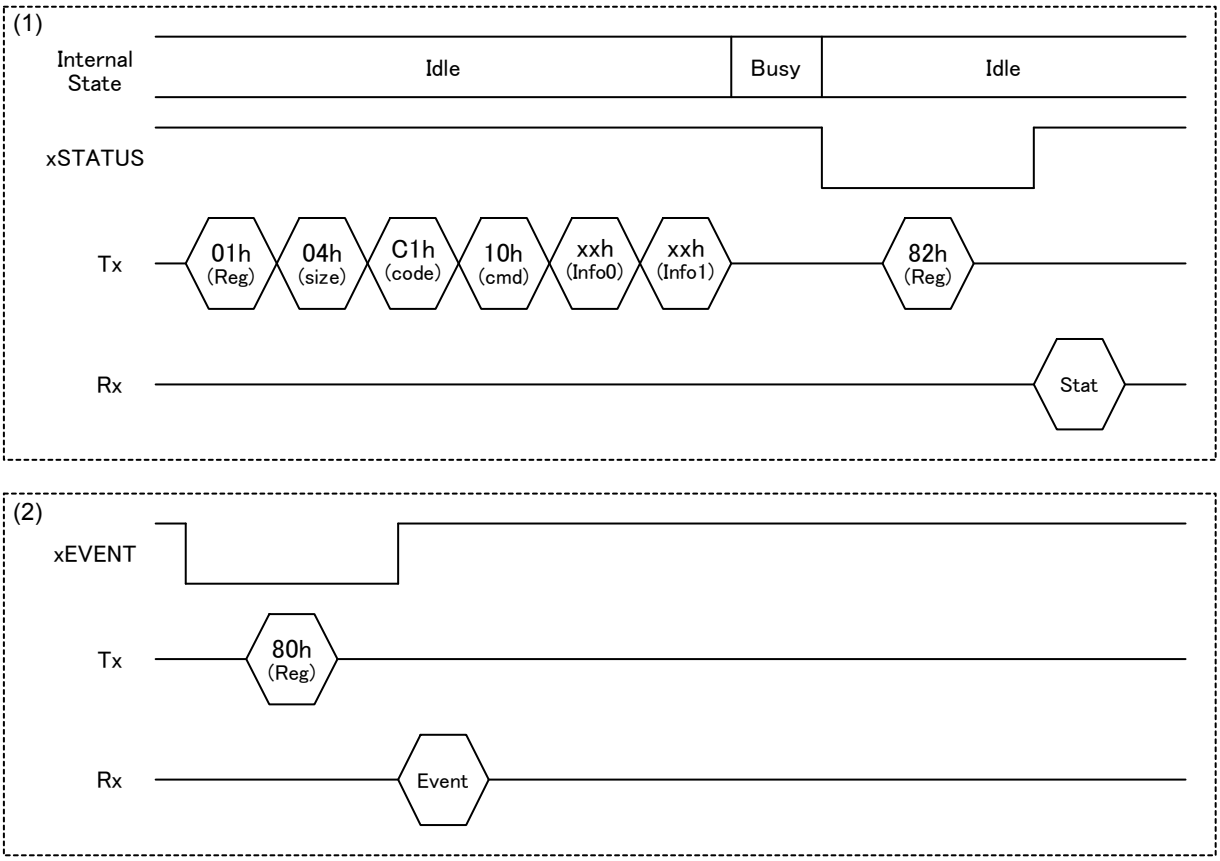
6.3.2 Host

The Host protocol is shown below.

Access using protocol procedures (1) and (2). For detailed information on pin negate timing, refer to (1) and (2).

The LSI asserts xSTATUS in (1) when command processing has ended. The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.

When the Device is connected, xEVENT in (2) is asserted. The Main CPU should acquire event information.



6.4 11h_REPORT ID REGISTRATION

This sets the Report ID registration information acquired from the Device descriptor to the LSI.

For more information on Report ID registration information, refer to the *S1R72U06 Technical Manual*.

Table 6.4 Host REPORT ID REGISTRATION

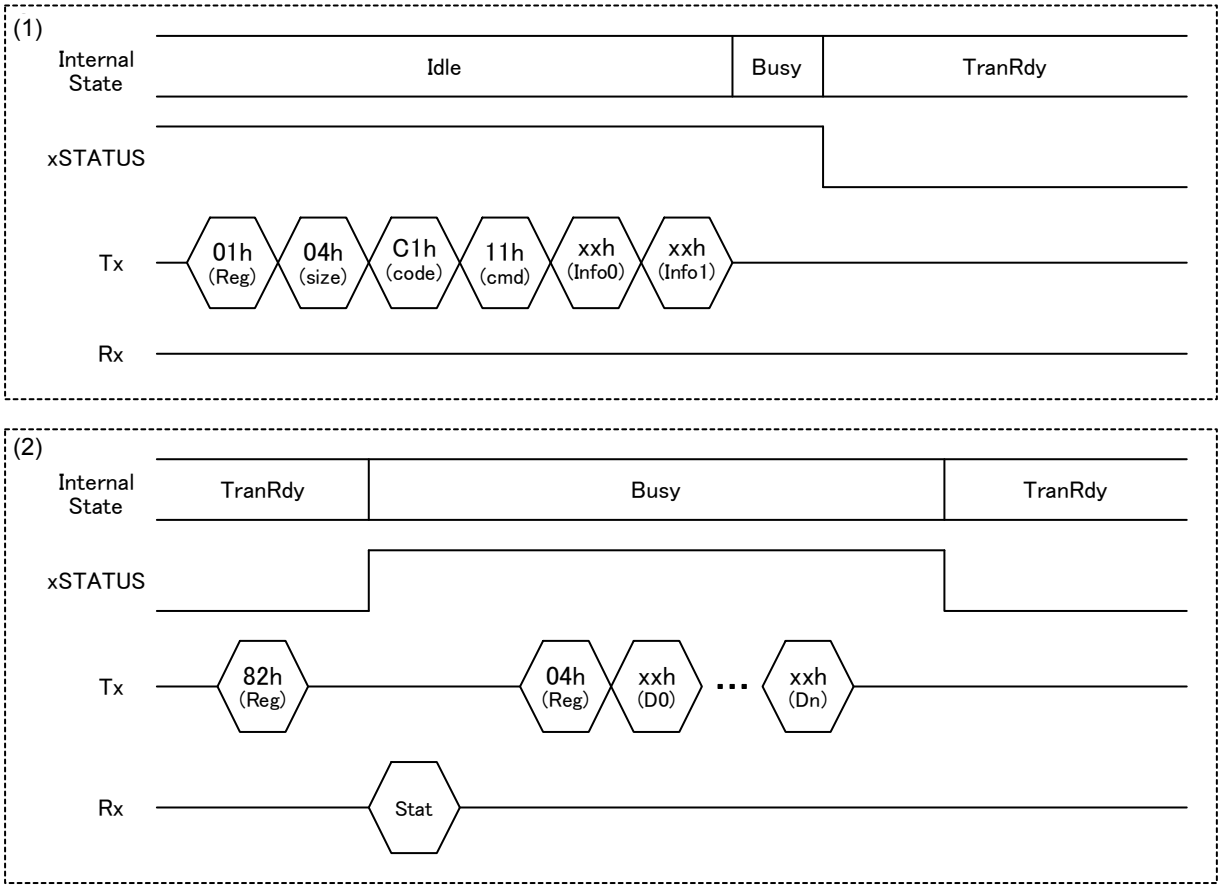
Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	C1h	Fixed value
	EIreq code	2	11h	Fixed value
	Information data	3	xxxxh	Report ID registration information data size 0008h to 0084h (Block4: MSB, Block3: LSB)
		4		
Data		-	xxh	Report ID registration information data

Access using protocol procedures (1) to (3). For detailed information on pin negate timing, refer to (1) to (3).

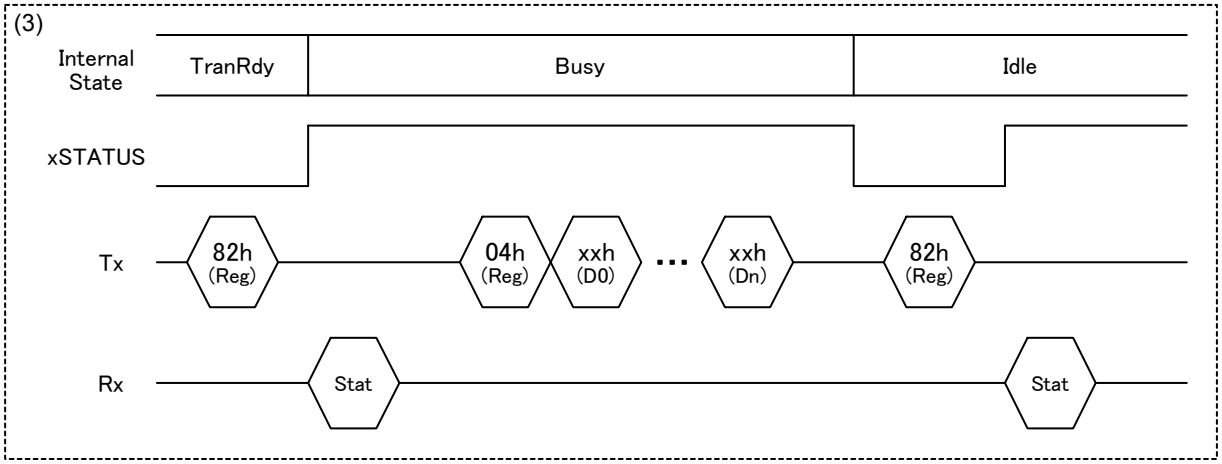
If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

The Main CPU should acquire status information in (2) and write the data after confirming that the status information is in the **TranRdy** state. “SendData” (04h) is used to write data. To continue writing (in Burst units), repeat the protocol in (2).

The final protocol for writing data is as shown in (3).



Confirm that the status information in (3) is in the **TranRdy** state and write using “SendData” (04h). After writing, acquire status information to confirm that the LSI is in the **Idle** state. Data writing ends with this protocol.



6.5 12h_DEVICE POWER MANAGEMENT

This controls Device Suspend and Resume operations. For more information on control methods, refer to “Power management” in the *S1R72U06 Application Note*.

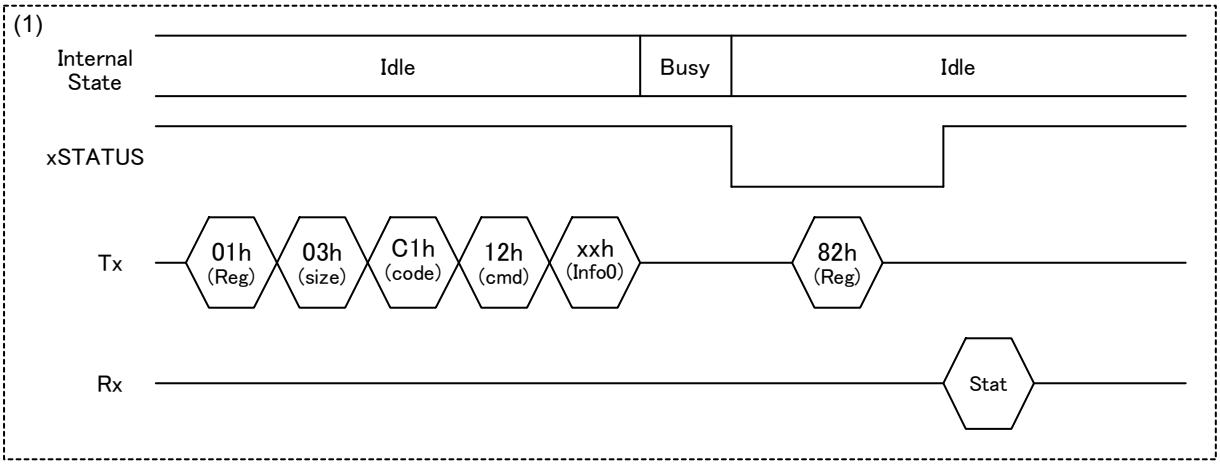
Table 6.5 Host DEVICE POWER MANAGEMENT

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	03h	Total for Control code + EIreq code + Information data
	Control code	1	C1h	Fixed value
	EIreq code	2	12h	Fixed value
	Information data	3	xxh	Operation setting 01h: Suspend & Remote Wakeup prohibited 02h: Suspend & Remote Wakeup permitted 03h to FFh: reserved

Access using protocol procedure (1).

The LSI asserts xSTATUS in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.



6.6 13h_DEVICE RESET

This performs a BUS reset for Devices in accordance with the USB standard.

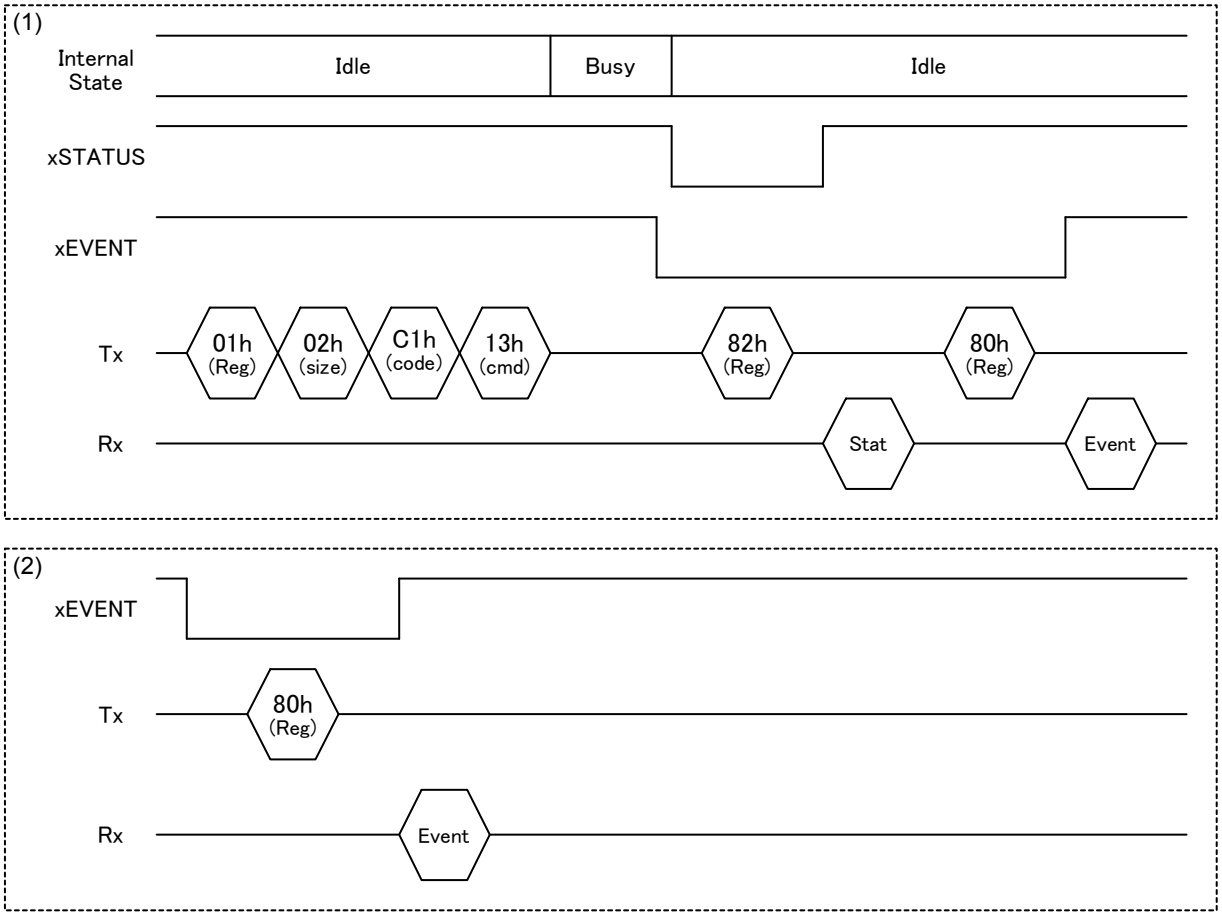
Table 6.6 Host DEVICE POWER MANAGEMENT

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	02h	Total for Control code + EIreq code
	Control code	1	C1h	Fixed value
	EIreq code	2	13h	Fixed value

Access using protocol procedures (1) and (2). For detailed information on pin negate timing, refer to (1) and (2).

xEVENT and xSTATUS in (1) are asserted when the Device has been disconnected by the BUS reset (xEVENT changes first). The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state, then acquire event information.

When the Device is reconnected, xEVENT in (2) is asserted. The Main CPU should acquire event information.



6.7 20h_SEND FEATURE REPORT

This writes Feature Report data to the LSI. The Device settings are shown in Table 6.7; the Host settings are shown in Table 6.8.

"Write data size" should be set to the Feature Report data size. For more information on data size, refer to the *S1R72U06 Technical Manual*.

Table 6.7 Device SEND FEATURE REPORT

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	81h	Fixed value
	EIreq code	2	20h	Fixed value
	Information data	3	xxxxh	Write data size 0001h to 0101h (Block4: MSB, Block3: LSB)
		4		
Data		-	xxh	Feature Report data

Table 6.8 Host SEND FEATURE REPORT

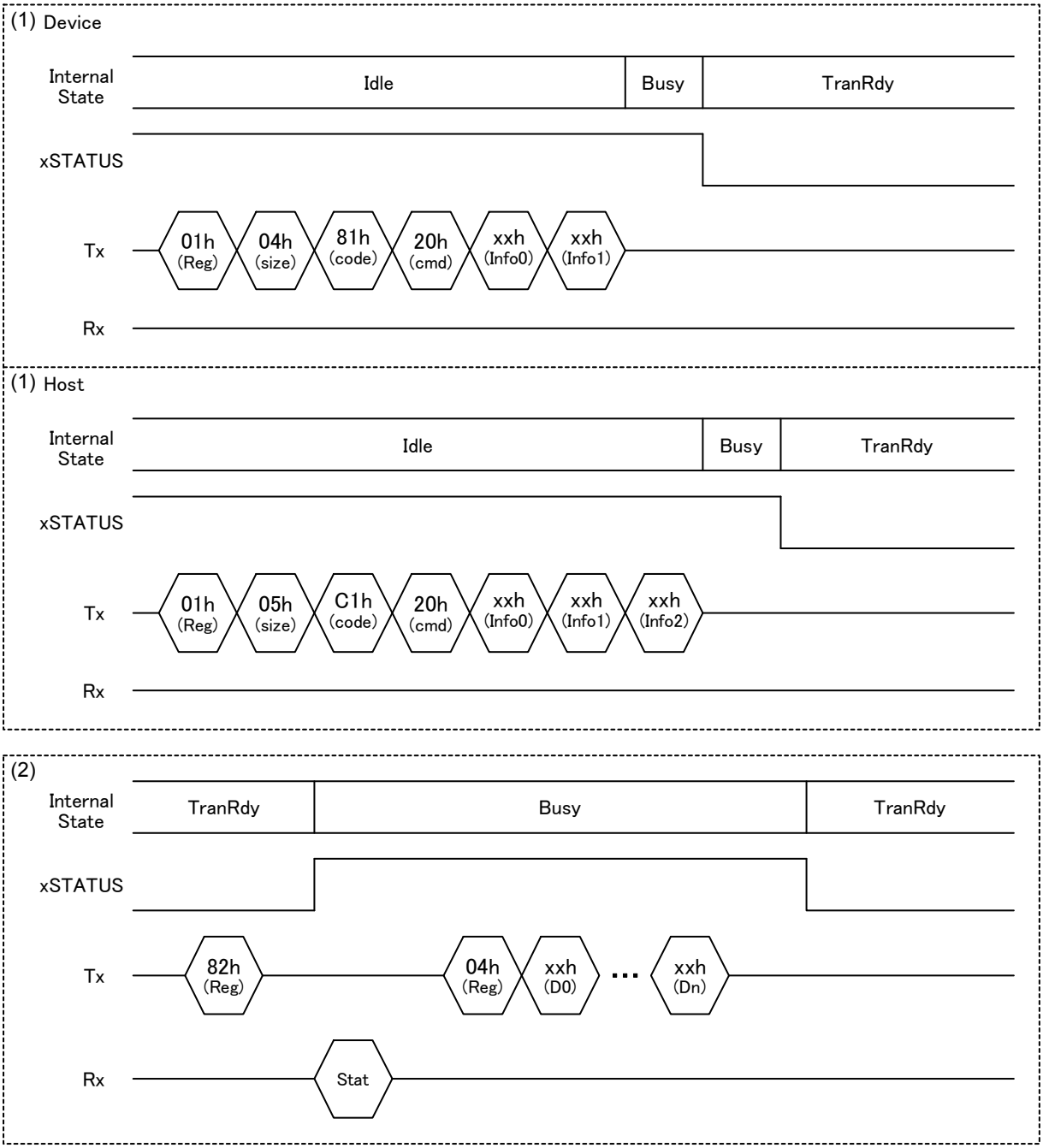
Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	05h	Total for Control code + EIreq code + Information data
	Control code	1	C1h	Fixed value
	EIreq code	2	20h	Fixed value
	Information data	3	00h	Fixed value
		4	xxxxh	Write data size 0001h to 0101h (Block5: MSB, Block4: LSB)
		5		
Data		-	xxh	Feature Report data

Access using protocol procedures (1) to (3). For detailed information on pin negate timing, refer to (1) to (3).

If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

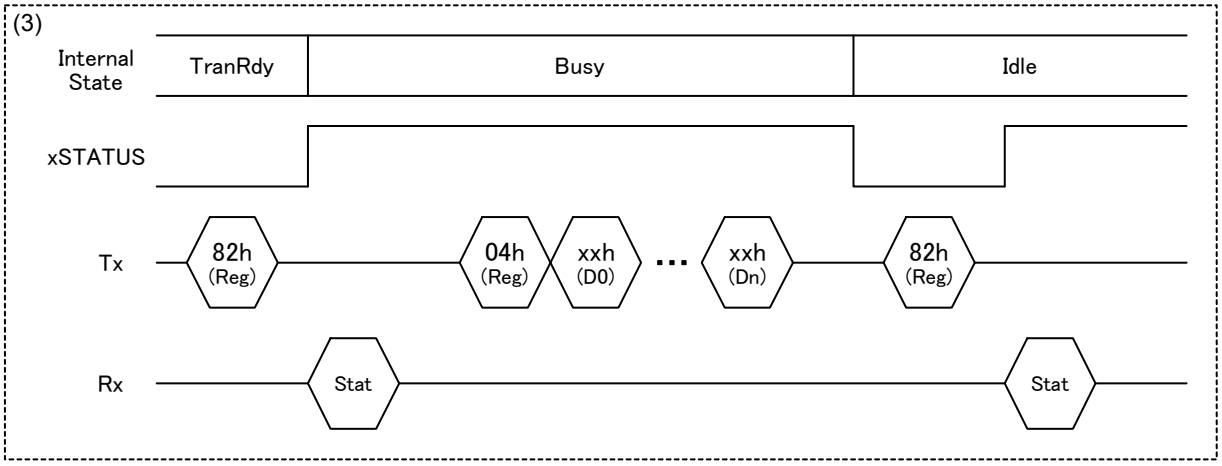
The Main CPU should acquire status information in (2) and write the data after confirming that the status information is in the **TranRdy** state. “SendData” (04h) is used to write data. To continue writing (in Burst units), repeat the protocol in (2).

The final protocol for writing data is as shown in (3).



Confirm that the status information in (3) is in the **TranRdy** state and write using “SendData” (04h). After writing, acquire status information to confirm that the LSI is in the **Idle** state. Data writing ends with this protocol.

When the LSI is operated as a Device, the data is retained until a request is issued by the Host. The transmission timing depends on requests from the Host.



6.8 21h_RECV FEATURE REPORT

This reads Feature Report data from the LSI. The Device settings are shown in Table 6.9; the Host settings are shown in Table 6.10.

The LSI should set the EIhead "Information data" to the read data size. For more information on data size, refer to the *S1R72U06 Technical Manual*.

Table 6.9 Device RECV FEATURE REPORT

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	81h	Fixed value
	EIreq code	2	21h	Fixed value
	Information data	3	0000h	Fixed value (Block4: MSB, Block3: LSB) *Indicates read data size for EIhead.
		4		
Data		-	xxh	Feature Report data

Table 6.10 Host RECV FEATURE REPORT

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	05h	Total for Control code + EIreq code + Information data
	Control code	1	C1h	Fixed value
	EIreq code	2	21h	Fixed value
	Information data	3	xxh	Report ID [00h: Not used]
		4	0000h	Fixed value (Block5: MSB, Block4: LSB) *Indicates read data size for EIhead.
		5		
Data		-	xxh	Feature Report data

6.8.1 Device

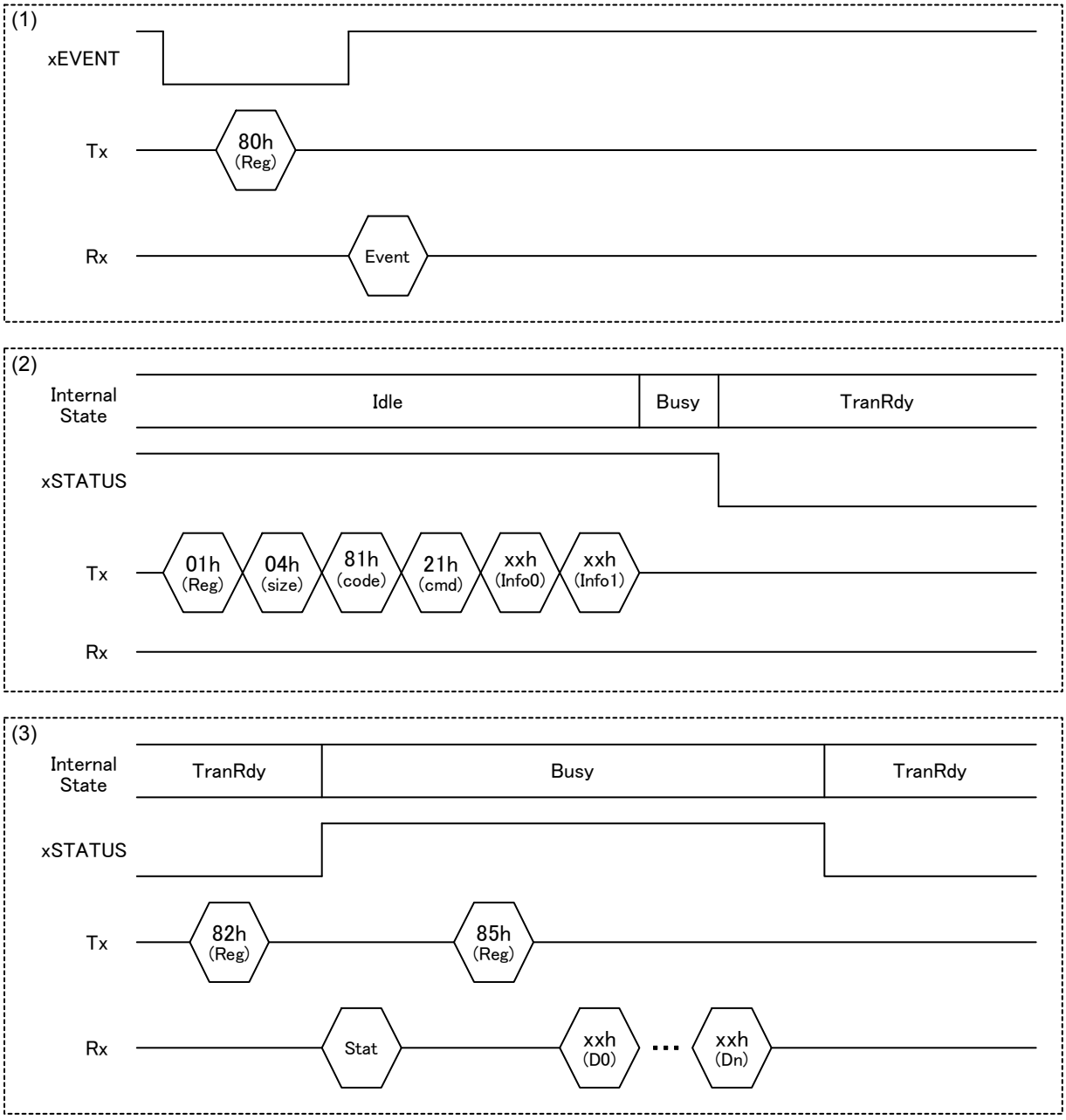
The Device protocol is shown below. Access using protocol procedures (1) to (5). For detailed information on pin negate timing, refer to (1) to (5).

If Feature Report is received from the Host, xEVENT in (1) is asserted.

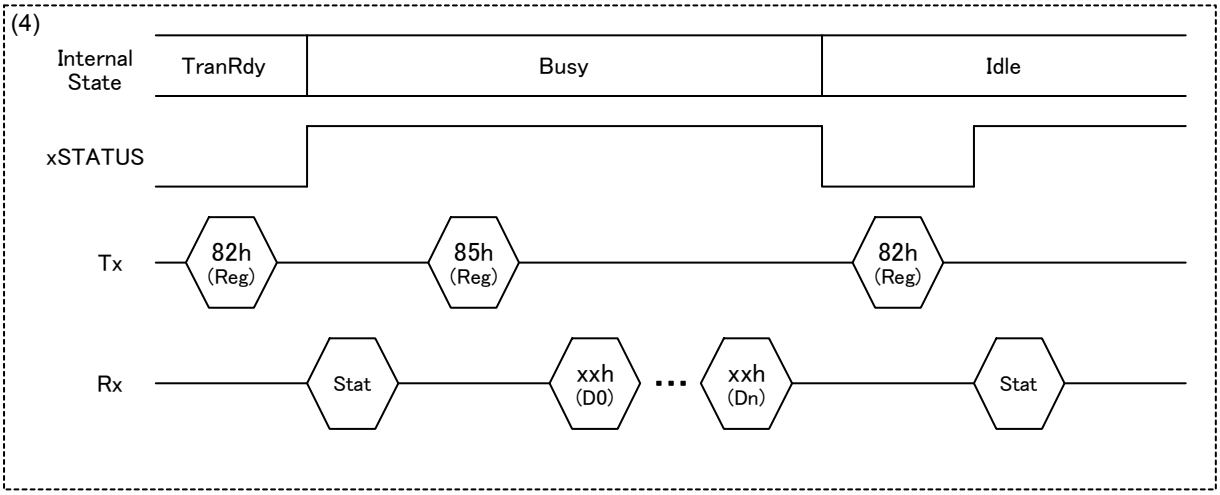
If the LSI switches to the **TranRdy** state, xSTATUS in (2) is asserted.

The Main CPU should acquire status information in (3) and read data after confirming that the status information is in the **TranRdy** state. "ReceiveData" (85h) is used for data reading. To continue reading (in Burst units), repeat the protocol in (3).

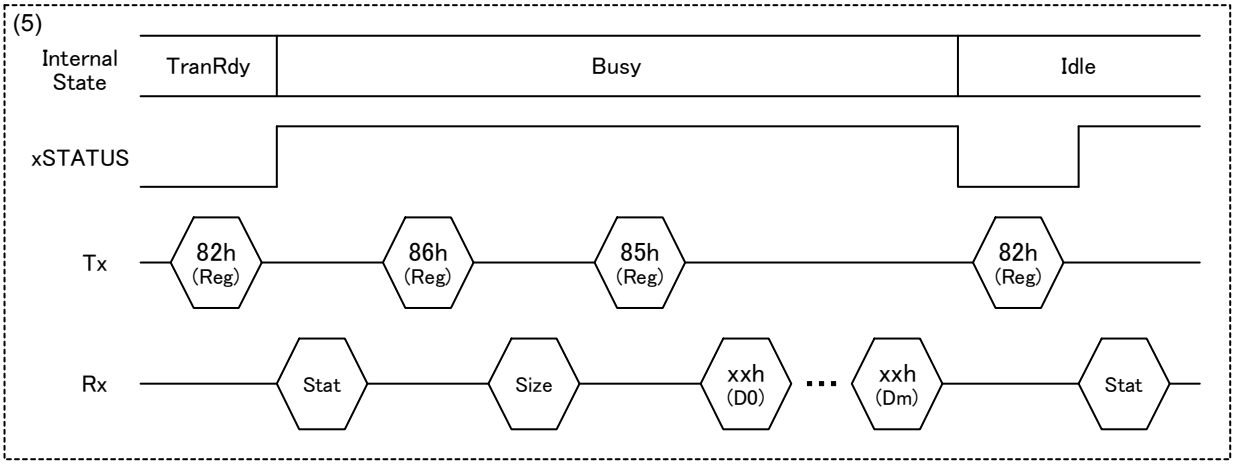
The final protocol for data reading will be one of two types, (4) or (5).



If the status information in (4) is in the **TranRdy** state, read using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. Data reading ends with this protocol.



If the status information in (5) is in the **RcvShort** + **TranRdy** state, check the valid data size using "ReceiveDataSize" (86h). Read the valid data using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. Data reading ends with this protocol.



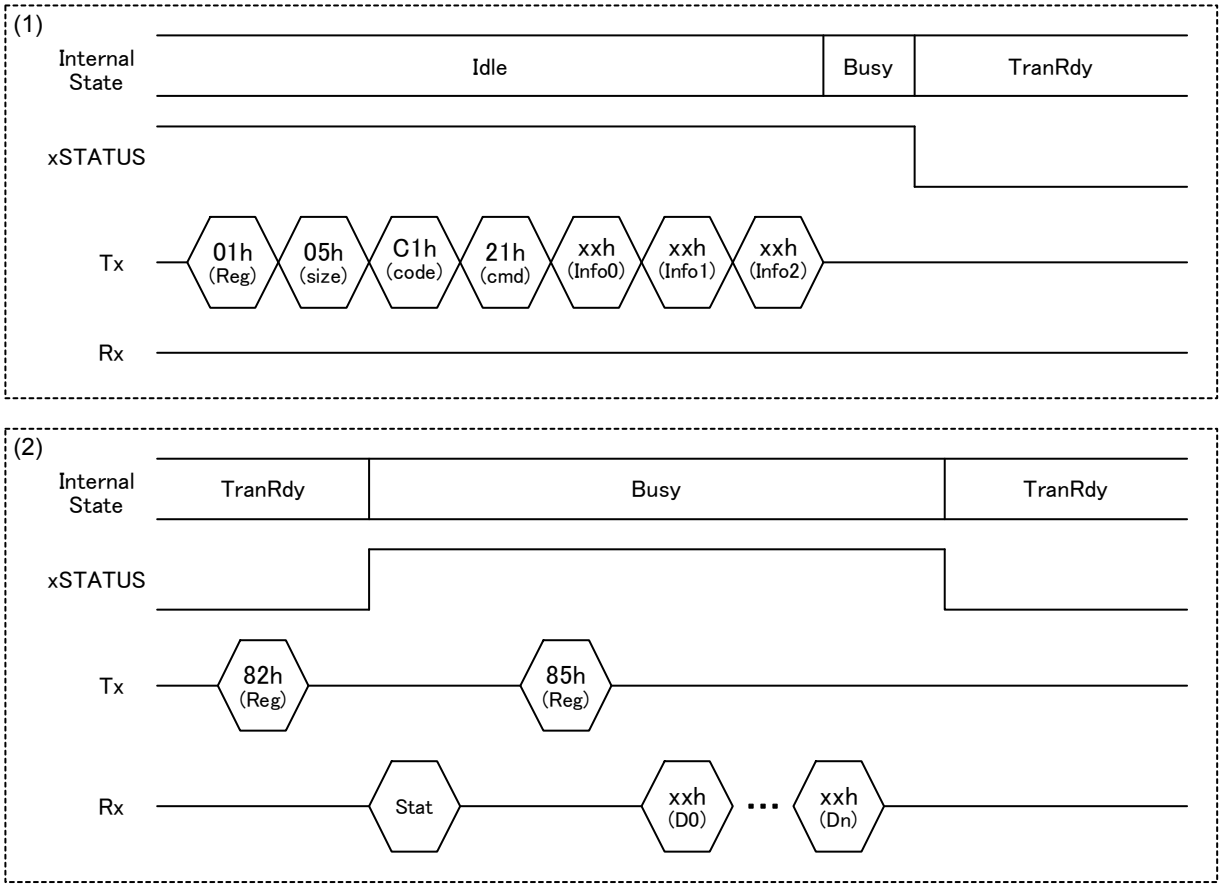
6.8.2 Host

The Host protocol is shown below. Access using protocol procedures (1) to (4). For detailed information on pin negate timing, refer to (1) to (4).

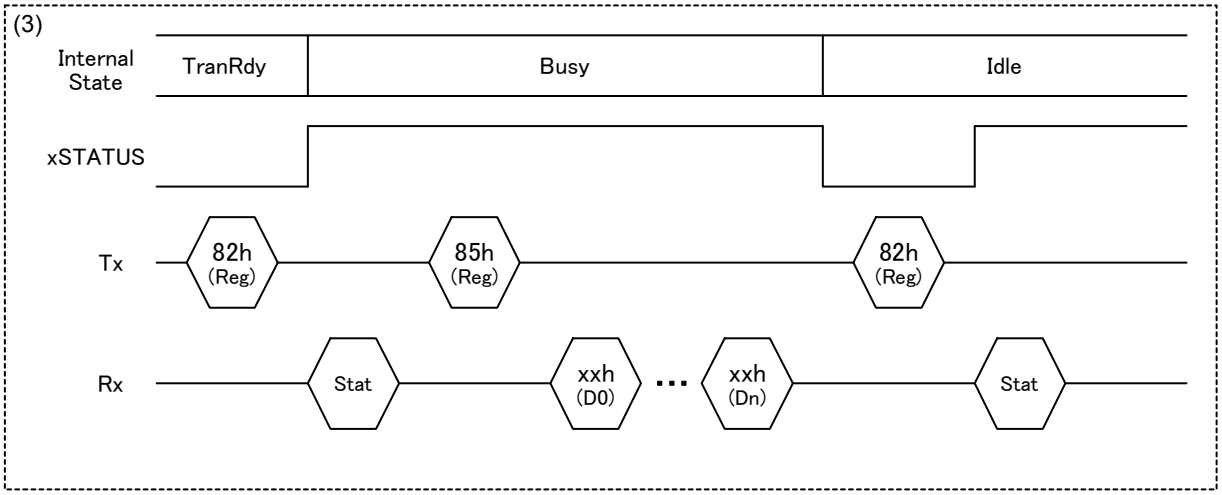
If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

The Main CPU should acquire status information in (2) and read data after confirming that the status information is in the **TranRdy** state. "ReceiveData" (85h) is used for data reading. To continue reading (in Burst units), repeat the protocol in (2).

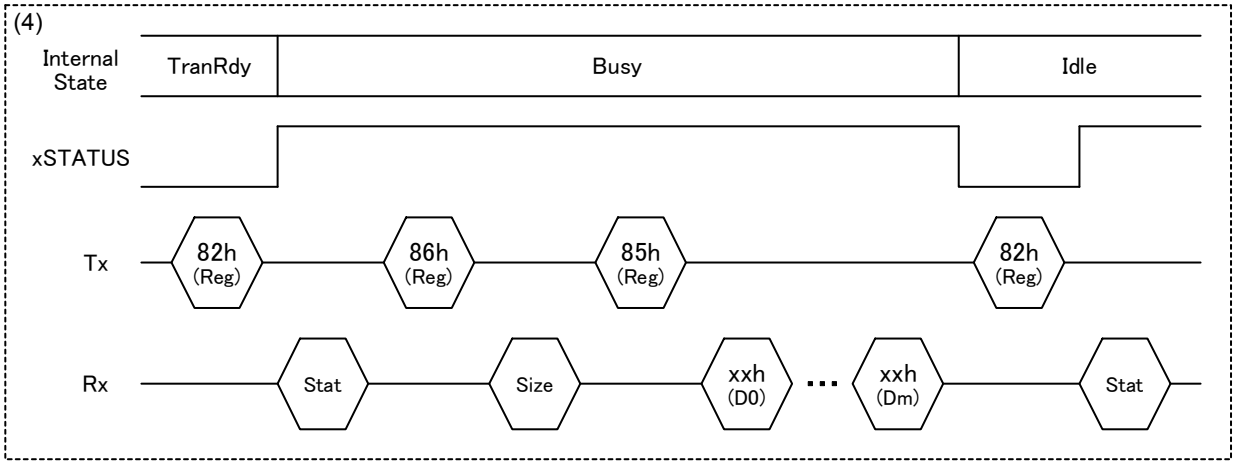
The final protocol for data reading will be one of two types, (3) or (4).



If the status information in (3) is in the **TranRdy** state, read using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. Data reading ends with this protocol.



If the status information in (4) is in the **RcvShort** + **TranRdy** state, check the valid data size using "ReceiveDataSize" (86h). Read the valid data using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. Data reading ends with this protocol.



6.9 22h_SEND REPORT

This writes Report data to the LSI. The Device settings are shown in Table 6.11; the Host settings are shown in Table 6.12.

This command allows multiple Report data to be written together. When Report data is combined, "Write data size" should be set to an integer multiple of the Report data size. For more information on data size, refer to the *S1R72U06 Technical Manual*.

Table 6.11 Device SEND REPORT

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	81h	Fixed value
	EIreq code	2	22h	Fixed value
	Information data	3	xxxxh	Write data size 0001h to 0800h (Block4: MSB, Block3: LSB)
		4		
Data		-	xxh	Report data

Table 6.12 Host SEND REPORT

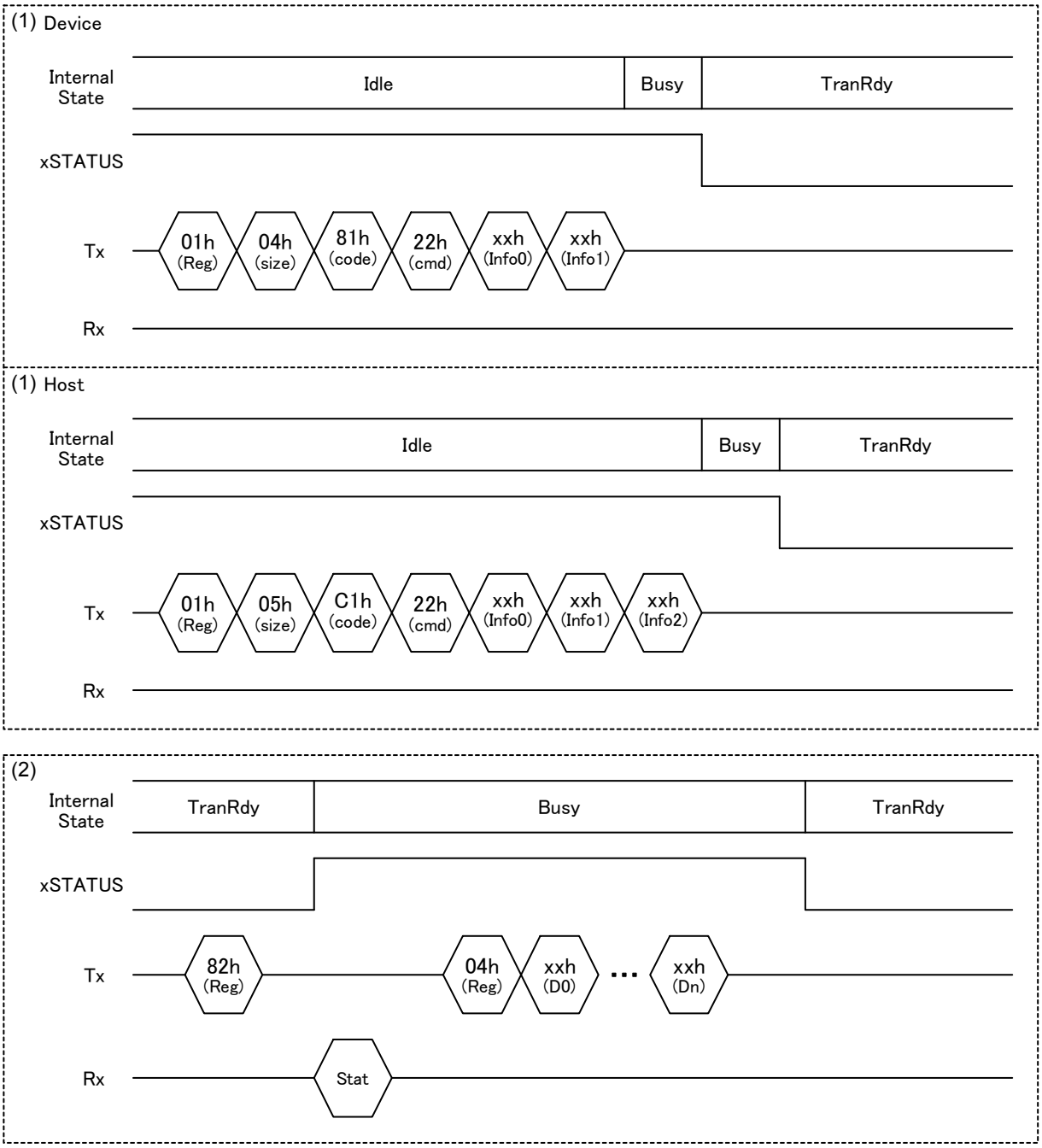
Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	05h	Total for Control code + EIreq code + Information data
	Control code	1	C1h	Fixed value
	EIreq code	2	22h	Fixed value
	Information data	3	00h	Fixed value
		4	xxxxh	Write data size 0001h to 0800h (Block5: MSB, Block4: LSB)
		5		
Data		-	xxh	Report data

Access using protocol procedures (1) to (3). For detailed information on pin negate timing, refer to (1) to (3).

If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

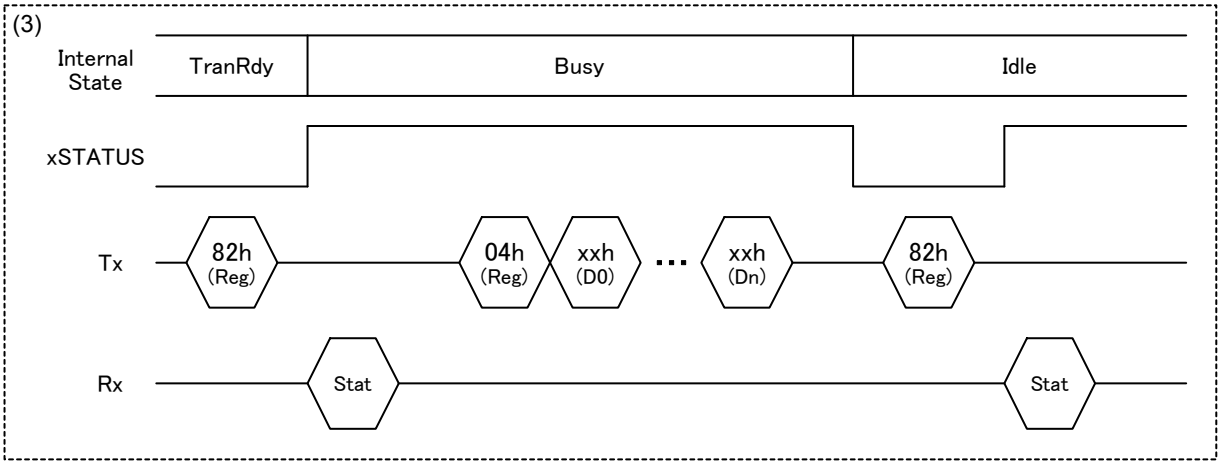
The Main CPU should acquire status information in (2) and write the data after confirming that the status information is in the **TranRdy** state. “SendData” (04h) is used to write data. To continue writing (in Burst units), repeat the protocol in (2).

The final protocol for writing data is as shown in (3).



Confirm that the status information in (3) is in the **TranRdy** state and write using “SendData” (04h). After writing, acquire status information to confirm that the LSI is in the **Idle** state. Data writing ends with this protocol.

When the LSI is operated as a Device, the data is retained until a request is issued by the Host. The transmission timing depends on requests from the Host.



6.10 23h_RECV REPORT

This reads Report data from the LSI. The Device settings are shown in Table 6.13; the Host settings are shown in Table 6.14.

The LSI sets the EIhead "Information data" to the read data size. For more information on data size, refer to the *S1R72U06 Technical Manual*.

Table 6.13 Device RECV REPORT

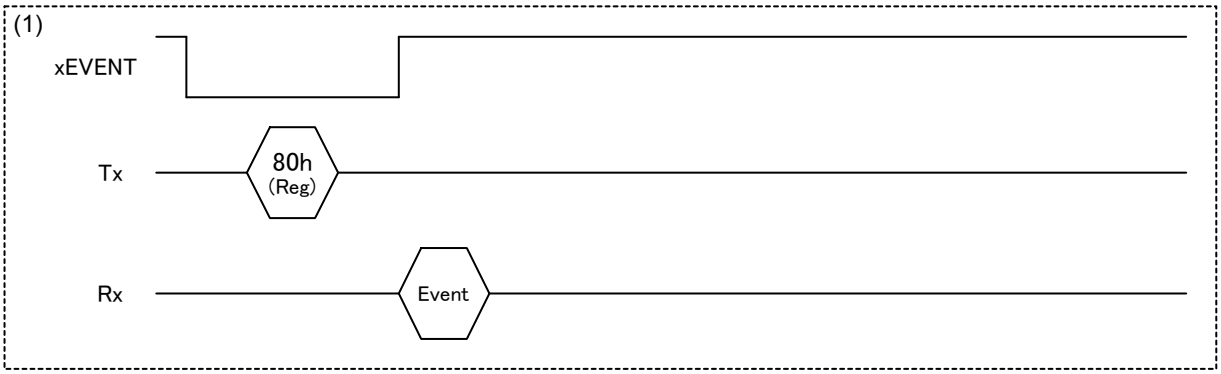
Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	81h	Fixed value
	EIreq code	2	23h	Fixed value
	Information data	3	0000h	Fixed value (Block4: MSB, Block3: LSB) *Indicates read data size for EIhead.
		4		
Data		-	xxh	Report data

Table 6.14 Host RECV REPORT

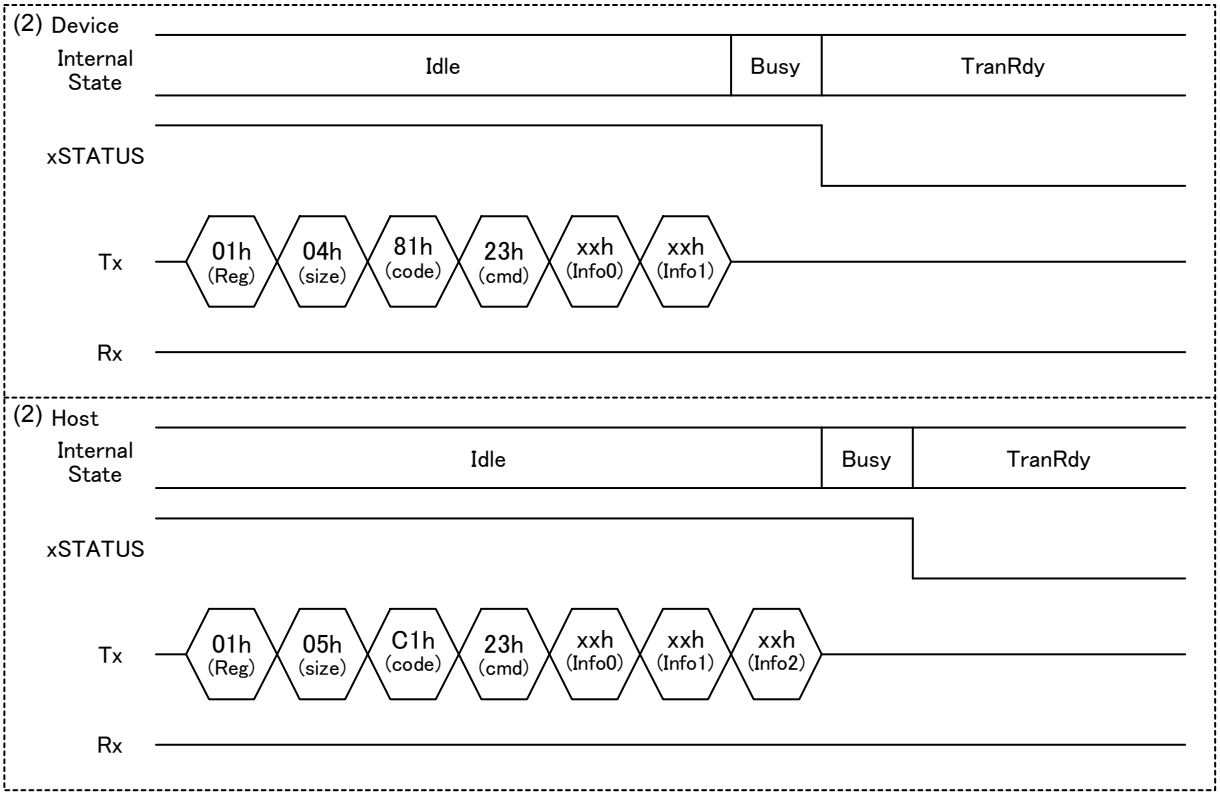
Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	05h	Total for Control code + EIreq code + Information data
	Control code	1	C1h	Fixed value
	EIreq code	2	23h	Fixed value
	Information data	3	00h	Fixed value
		4	0000h	Fixed value (Block5: MSB, Block4: LSB) *Indicates read data size for EIhead.
		5		
Data		-	xxh	Report data

Access using protocol procedures (1) to (5). For detailed information on pin negate timing, refer to (1) to (5).

If the LSI receives Report, xEVENT in (1) is asserted. The Main CPU should acquire event information.

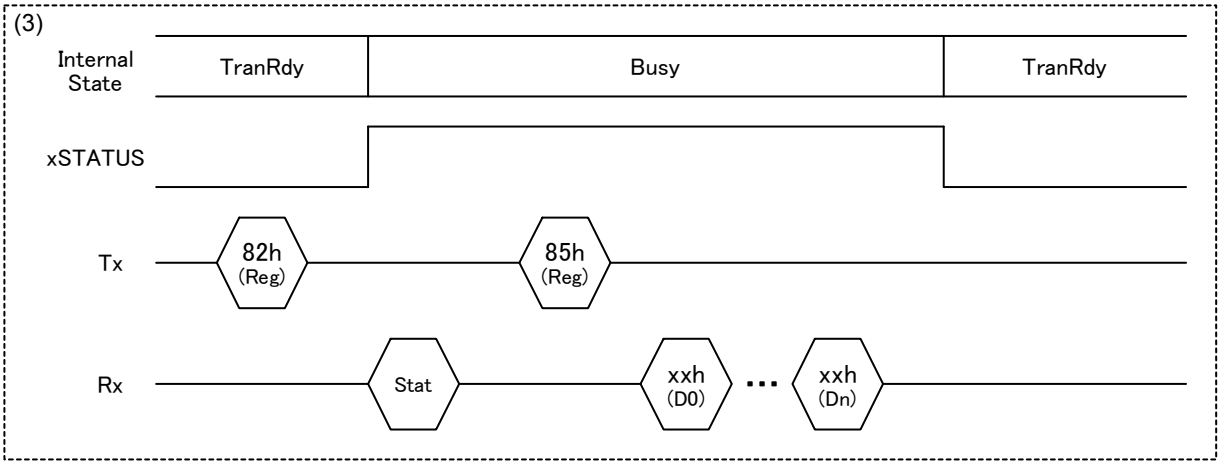


If the LSI switches to the **TranRdy** state, xSTATUS in (2) is asserted.

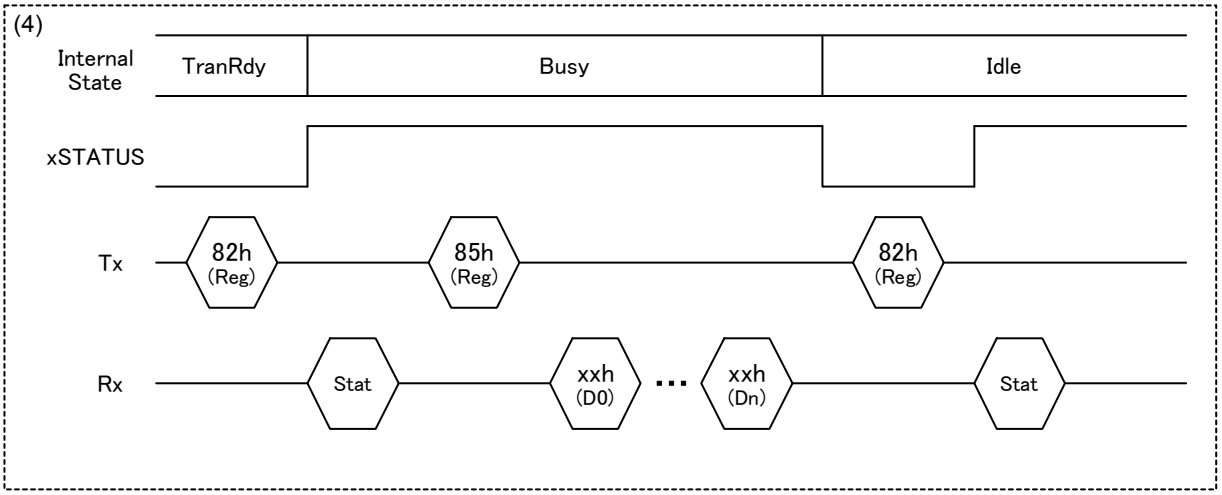


The Main CPU should acquire status information in (3) and read data after confirming that the status information is in the **TranRdy** state. "ReceiveData" (85h) is used for data reading. To continue reading (in Burst units), repeat the protocol in (3).

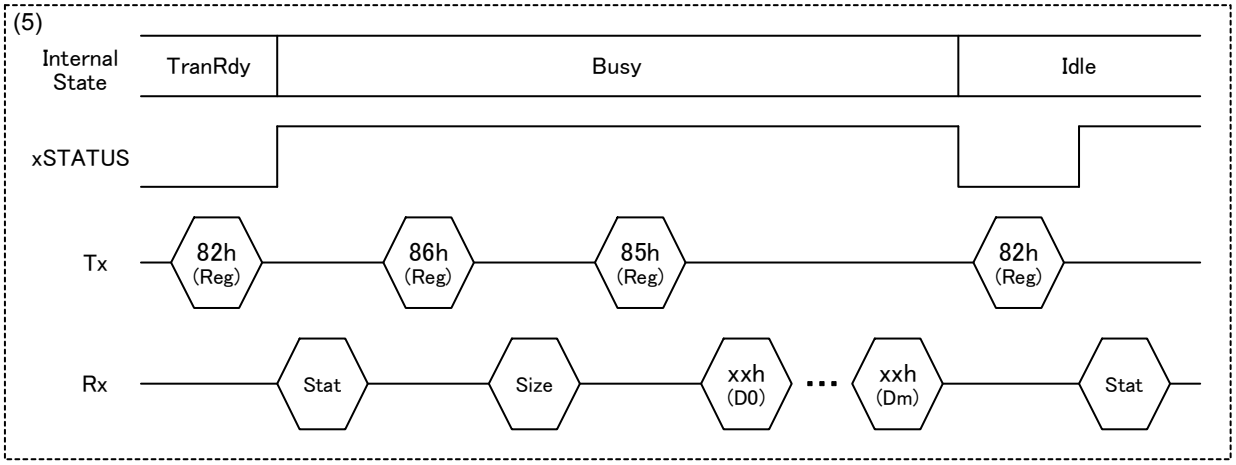
The final protocol for data reading will be one of two types, (4) or (5).



If the status information in (4) is in the **TranRdy** state, read using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. Data reading ends with this protocol.



If the status information in (5) is in the **RcvShort** + **TranRdy** state, check the valid data size using "ReceiveDataSize" (86h). Read the valid data using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. Data reading ends with this protocol.



6.11 24h_INITIAL FEATURE REPORT

This writes Feature Report data initial values to the LSI.

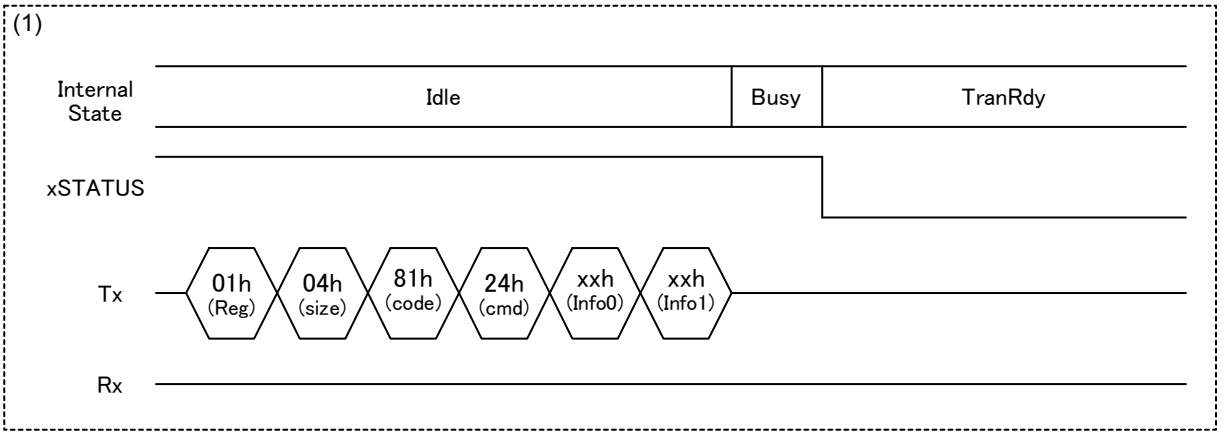
"Write data size" should be set to the Feature Report data size. For more information on data size, refer to the *S1R72U06 Technical Manual*.

Table 6.15 Device INITIAL FEATURE REPORT

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	81h	Fixed value
	EIreq code	2	24h	Fixed value
	Information data	3	xxxxh	Write data size 0001h to 0101h (Block4: MSB, Block3: LSB)
		4		
Data		-	xxh	Feature Report data default value

Access using protocol procedures (1) to (3). For detailed information on pin negate timing, refer to (1) to (3).

If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

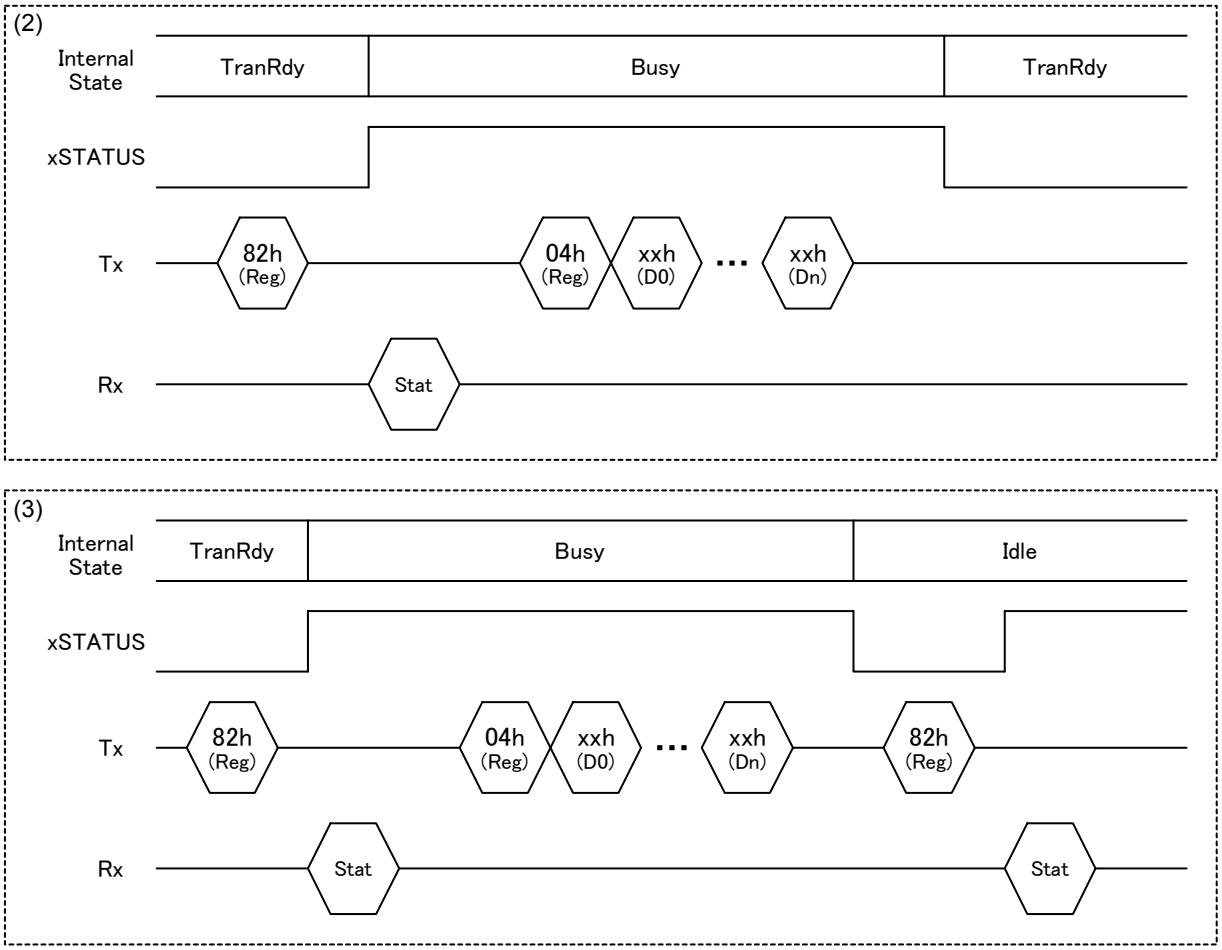


The Main CPU should acquire status information in (2) and write the data after confirming that the status information is in the **TranRdy** state. “SendData” (04h) is used to write data. To continue writing (in Burst units), repeat the protocol in (2).

The final protocol for writing data is as shown in (3).

Confirm that the status information in (3) is in the **TranRdy** state and write using “SendData” (04h). After writing, acquire status information to confirm that the LSI is in the **Idle** state. Data writing ends with this protocol.

The LSI retains the data until a request is issued by the Host. The transmission timing depends on requests from the Host.



6.12 25h_GET PROTOCOL MODE

This reads the protocol mode received from the Host from the LSI.

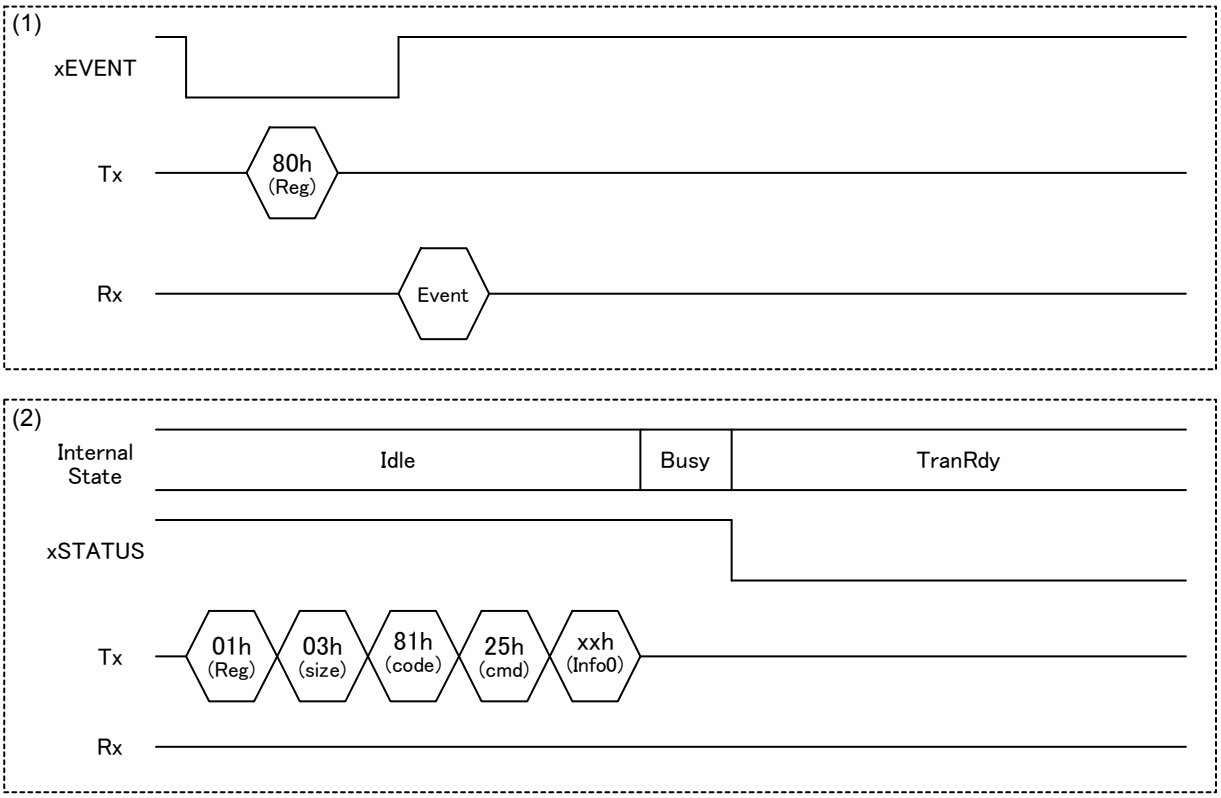
Table 6.16 Device GET PROTOCOL MODE

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	03h	Total for Control code + EIreq code + Information data
	Control code	1	81h	Fixed value
	EIreq code	2	25h	Fixed value
	Information data	3	01h	Read data size (1 byte fixed)
Data		-	xxh	00h: Boot Protocol 01h: Report Protocol

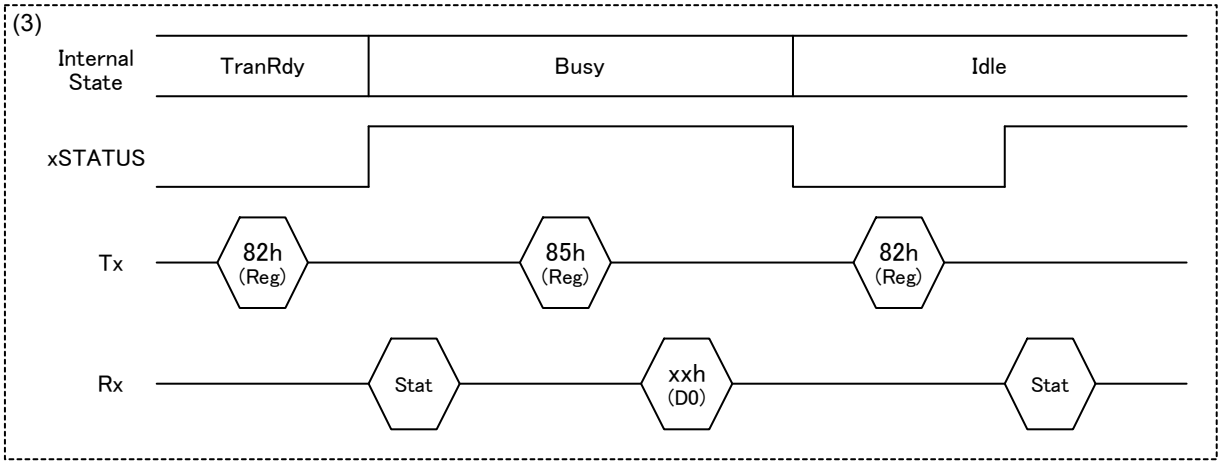
Access using protocol procedures (1) to (3). For detailed information on pin negate timing, refer to (1) to (3).

xEVENT in (1) is asserted if the LSI receives protocol mode settings. The Main CPU should acquire event information.

If the LSI switches to the **TranRdy** state, xSTATUS in (2) is asserted.



The Main CPU should acquire status information in (3) and read data after confirming that the status information is in the **TranRdy** state. “ReceiveData” (85h) is used for data reading. After reading, acquire status information to confirm that the LSI is in the **Idle** state.



6.13 24h_GET DESCRIPTOR

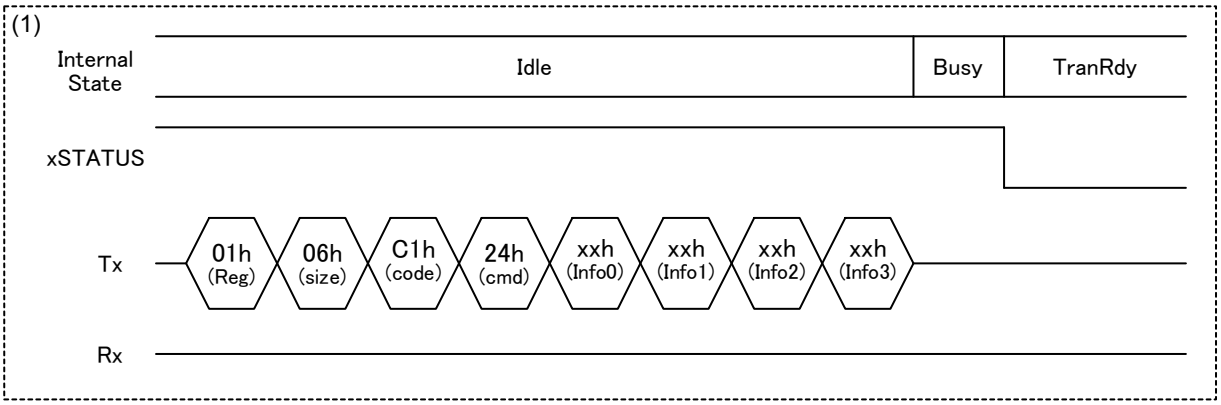
This reads the descriptor received from the Device from the LSI. Configuration Descriptor includes the Interface Descriptor, HID Descriptor, and Endpoint Descriptor.

Table 6.17 Host GET DESCRIPTOR

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	06h	Total for Control code + EIreq code + Information data
	Control code	1	C1h	Fixed value
	EIreq code	2	24h	Fixed value
	Information data	3	xxh	Descriptor type 00h: HID Descriptor 01h: Report Descriptor 02h: String Descriptor 03h: Device Descriptor 04h: Configuration Descriptor 05h to FFh: reserved
		4	xxh	String index number [00h: Not string]
		5	xxxxh	Read size [FFFFh: All Descriptor Read setting] 0001h to FFFFh (Block6: MSB, Block5: LSB)
		6		
Data		-	xxh	Refer to *S1R72U06 Technical Manual* for details.

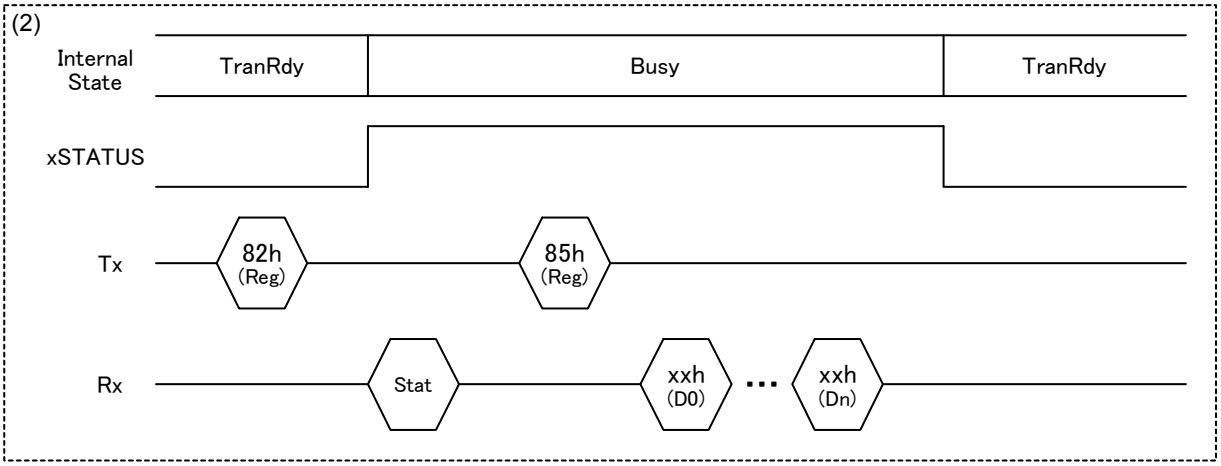
Access using protocol procedures (1) to (4). For detailed information on pin negate timing, refer to (1) to (4).

If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

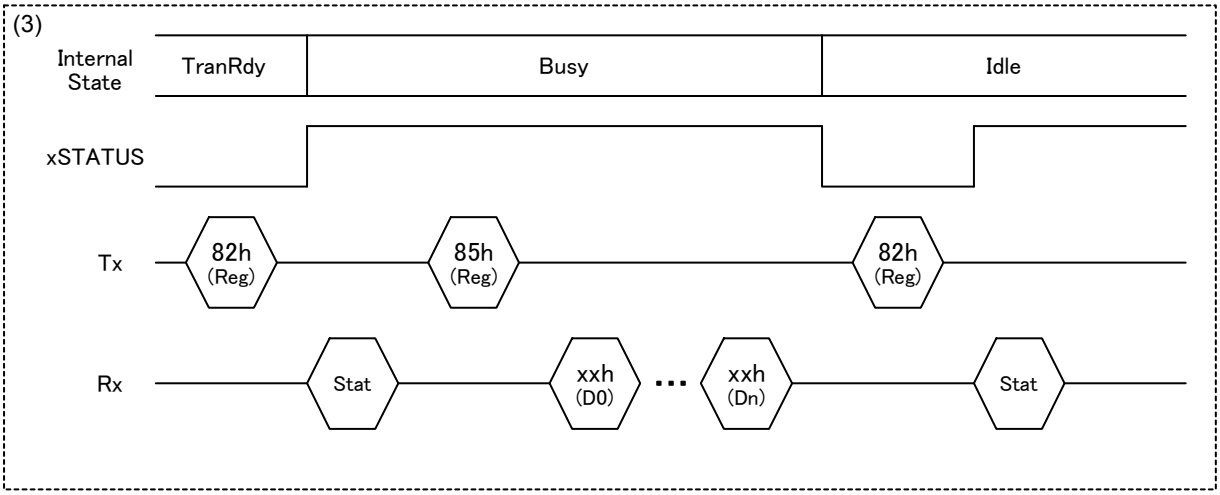


The Main CPU should acquire status information in (2) and read data after confirming that the status information is in the **TranRdy** state. "ReceiveData" (85h) is used for data reading. To continue reading (in Burst units), repeat the protocol in (2).

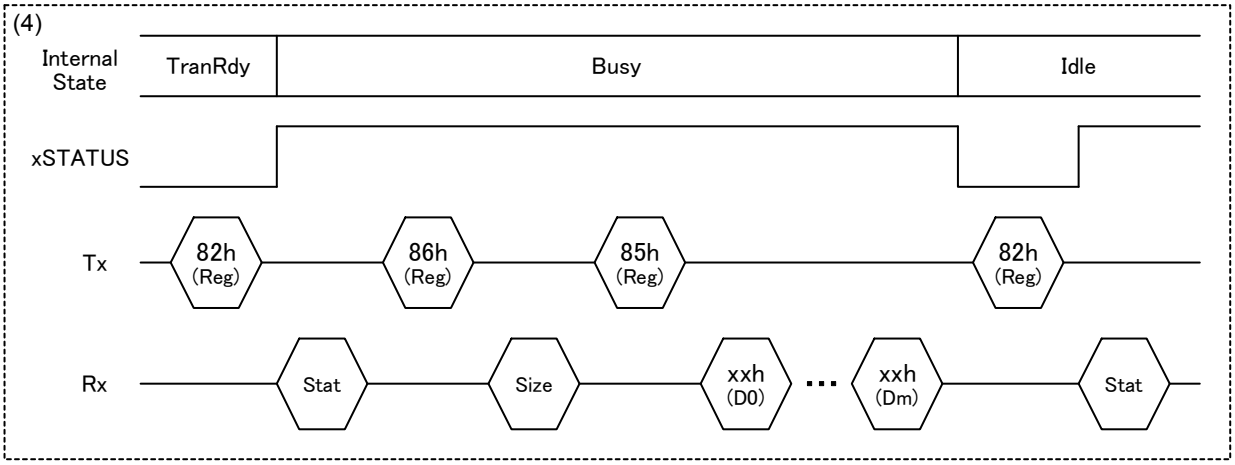
The final protocol for data reading will be one of two types, (3) or (4).



If the status information in (3) is in the **TranRdy** state, read using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. Data reading ends with this protocol.



If the status information in (4) is in the **RcvShort** + **TranRdy** state, check the valid data size using "ReceiveDataSize" (86h). Read the valid data using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. Data reading ends with this protocol.



7. MSC EI Requests

Table 7.1 lists the MSC EI requests. These EIreqs are used for Host MSC only.

The command parameters and protocols are described in the following sections.

Table 7.1 MSC EI requests

Control code	EIreq code	EIreq name	Control	Description
C2h	30h	MSC START	Common	MSC control
	32h	DEVICE POWER MANAGEMENT	Common	Power management
	33h	DEVICE RESET	Common	USB BUS reset
	40h	GET STORAGE INFORMATION	Simple	Storage information read
	41h	START WRITING SECTORS	Simple	Sector write start
	42h	START READING SECTORS	Simple	Sector read start
	3Ah	BLK WRITE DATA	Common	Block transfer data write
	3Bh	BLK READ DATA	Common	Block transfer data read
	48h	STORAGE COMMAND THROUGH (6)	Full	SCSI/ATAPI command (6 bytes)
	49h	STORAGE COMMAND THROUGH (10)	Full	SCSI/ATAPI command (10 bytes)
	4Ah	STORAGE COMMAND THROUGH (12)	Full	SCSI/ATAPI command (12 bytes)
	4Bh	STORAGE COMMAND THROUGH (16)	Full	SCSI/ATAPI command (16 bytes)
	4Ch	STORAGE COMMAND RESULT	Full	SCSI/ATAPI command execution result acquisition

7.1 Usage conditions

(1) MSC EI requests should be used after “MSC START” (30h) has been set to “Start”.

(2) Switching to “Idle” state during block transfer indicates that data transfer is complete. For details, refer to the *S1R72U06 Application Note*.

7.1.1 Simple control

This control method enables USB MSC Devices to be controlled easily without the need for detailed knowledge of SCSI/ATAPI standards.

(1) This control method limits the MSC Devices supported. For details, refer to the *S1R72U06 Application Note*.

(2) This control method should be used with EIreqs indicated as “Common” or “Simple” in the Control column in Table 7.1.

(3) For data size in block transfer, refer to “Appendix B MSC Access Size”.

7.1.2 Full control

This control method allows command control in compliance with the SCSI/ATAPI standards. For details of the standards, refer to "Compliance" in the *S1R72U06 Technical Manual*.

(1) This control method should be used with EIreqs indicated as "Common" or "Full" in the Control column in Table 7.1.

(2) After using the THROUGH command, check the execution results using "STORAGE COMMAND RESULT" (4Ch).

(3) "STORAGE COMMAND RESULT" (4Ch) indicates the "Block Tran Executing" error information until the THROUGH command processing is complete.

(4) The error information for the LSI protocol is separate from errors complying with the SCSI/ATAPI standards. SCSI/ATAPI error information should be acquired using "REQUEST SENSE" of the SCSI/ATAPI command.

(5) If an error occurs in a protocol for the LSI when Ended notification is set to "permitted", the Ended notification setting is canceled.

(6) If Ended notification is set to "prohibited", "STORAGE COMMAND RESULT" (4Ch) should be polled to check that processing is complete.

(7) For SCSI/ATAPI command control details, refer to "Appendix C SCSI/ATAPI Command Control".

7.2 Precautions

(1) If the LSI internal data transfer ends when the Device is disconnected during read block transfer, error information accompanying disconnection is notified. The error information may be delayed, depending on the usage status.

7.2.1 Simple control

(1) If an error occurs in the Device connected, the results for "GET STORAGE INFORMATION" (40h) may be all be "0".

7.2.2 Full control

(1) Error information for "Media Not Found" and "Media Changed" is disabled in this control method.

(2) "STORAGE COMMAND RESULT" (4Ch) is retained until the next THROUGH command is written.

(3) "STORAGE COMMAND RESULT" (4Ch) may not always be updated if an error occurs in a protocol for the LSI.

7.3 30h_MSC START

This sets MSC control for the USB.

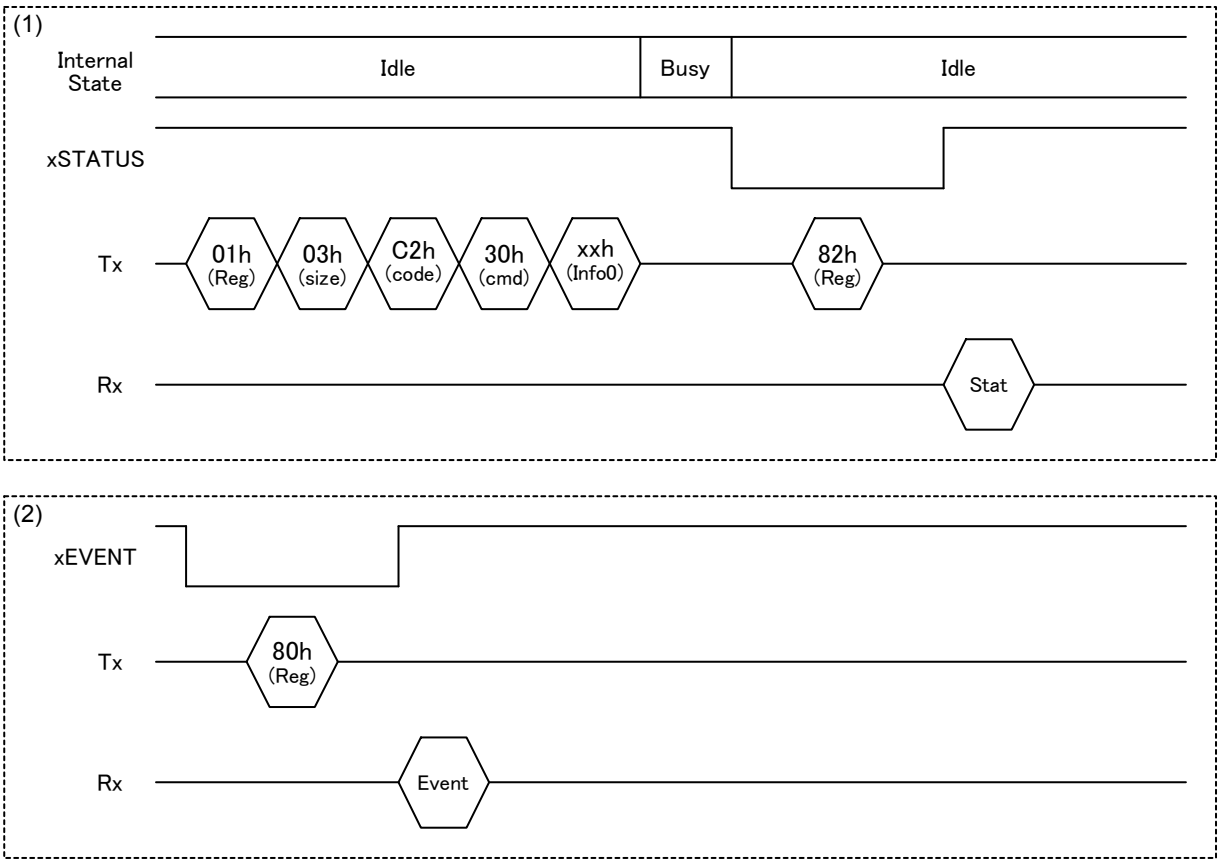
Table 7.2 MSC START

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	03h	Total for Control code + EIreq code + Information data
	Control code	1	C2h	Fixed value
	EIreq code	2	30h	Fixed value
	Information data	3	xxh	Operation setting 00h: MSC Stop (default) 01h: MSC Start 02h to FFh: reserved

Access using protocol procedures (1) and (2). For detailed information on pin negate timing, refer to (1) and (2).

The LSI asserts xSTATUS in (1) when command processing has ended. The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.

When the Device is connected, xEVENT in (2) is asserted. The Main CPU should acquire event information.



7.4 32h_DEVICE POWER MANAGEMENT

This controls the Device Suspend and Resume operations. For more information on control methods, refer to "Power management" in the *S1R72U06 Application Note*.

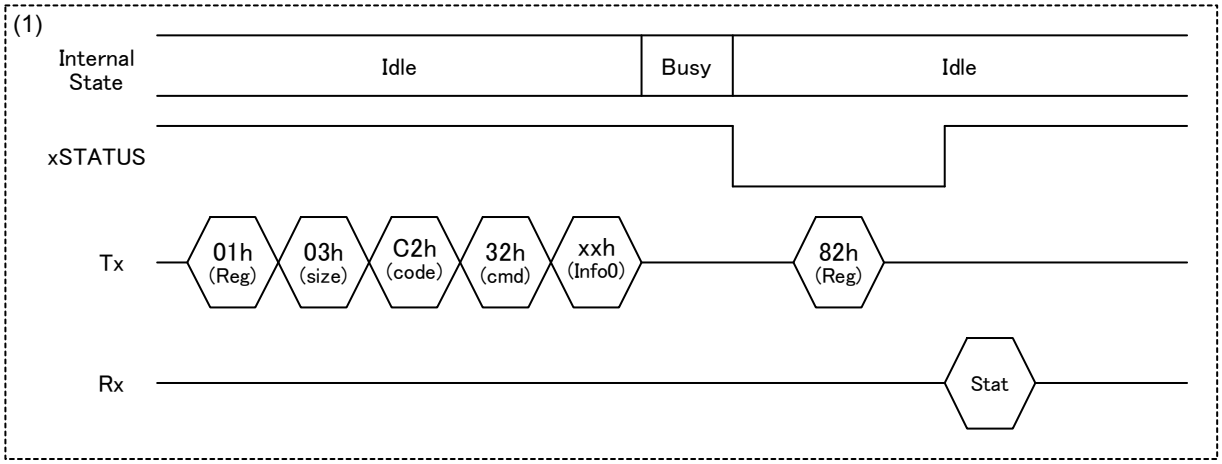
Table 7.3 DEVICE POWER MANAGEMENT

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	03h	Total for Control code + EIreq code + Information data
	Control code	1	C2h	Fixed value
	EIreq code	2	32h	Fixed value
	Information data	3	xxh	Operation setting 01h: Suspend & Remote Wakeup prohibited 02h: Suspend & Remote Wakeup permitted 03h to FFh: reserved

Access using protocol procedure in (1).

The LSI asserts xSTATUS in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.



7.5 33h_DEVICE RESET

This performs a BUS reset for Devices in accordance with the USB standard.

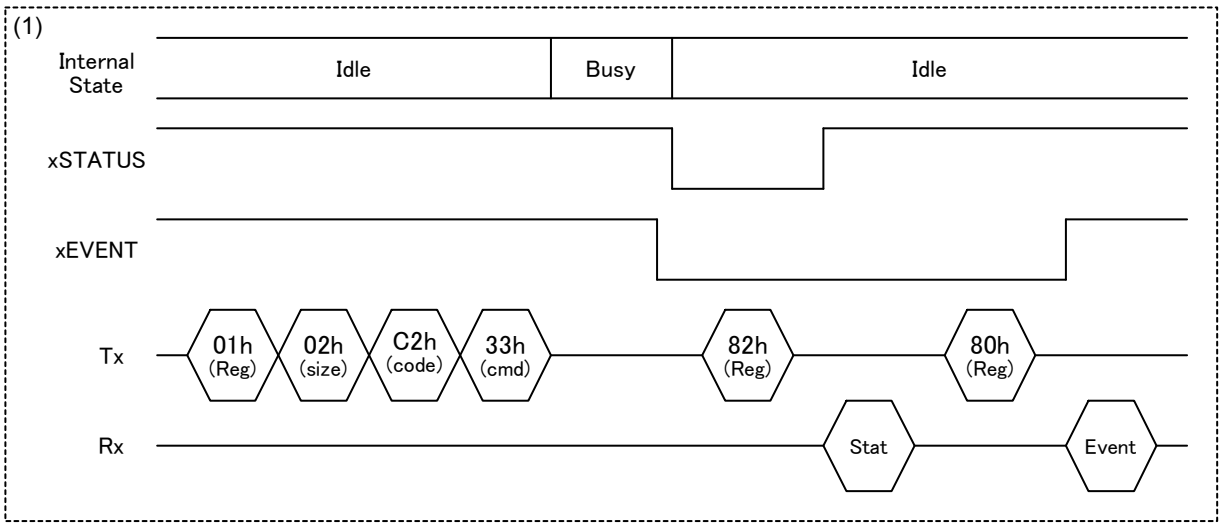
Table 7.4 DEVICE RESET

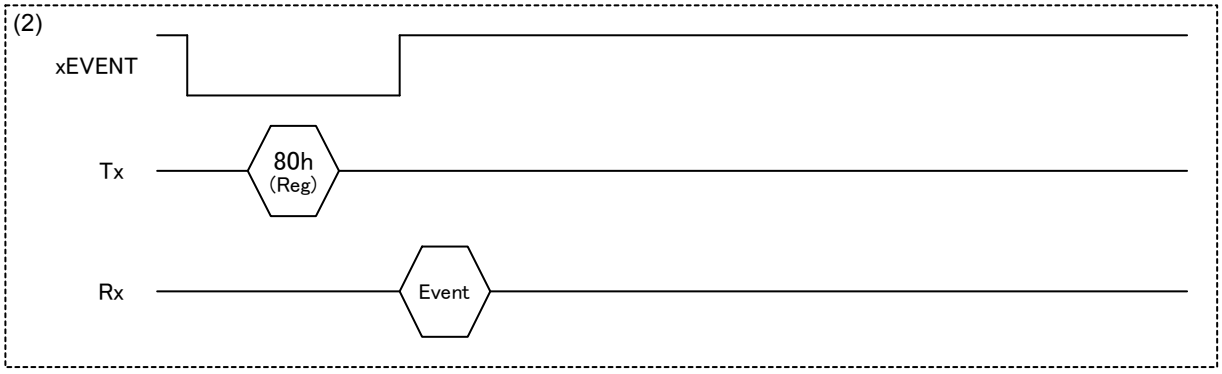
Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	02h	Total for Control code + EIreq code
	Control code	1	C2h	Fixed value
	EIreq code	2	33h	Fixed value

Access using protocol procedures (1) and (2). For detailed information on pin negate timing, refer to (1) and (2).

xEVENT and xSTATUS in (1) are asserted when the Device has been disconnected by the BUS reset (xEVENT changes first). The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state, then acquire event information.

When the Device is reconnected, xEVENT in (2) is asserted. The Main CPU should acquire event information.





7.6 40h_GET STORAGE INFORMATION

This is an EIreq for simple control. This reads the storage information received from the connected Device from the LSI.

Table 7.5 GET STORAGE INFORMATION

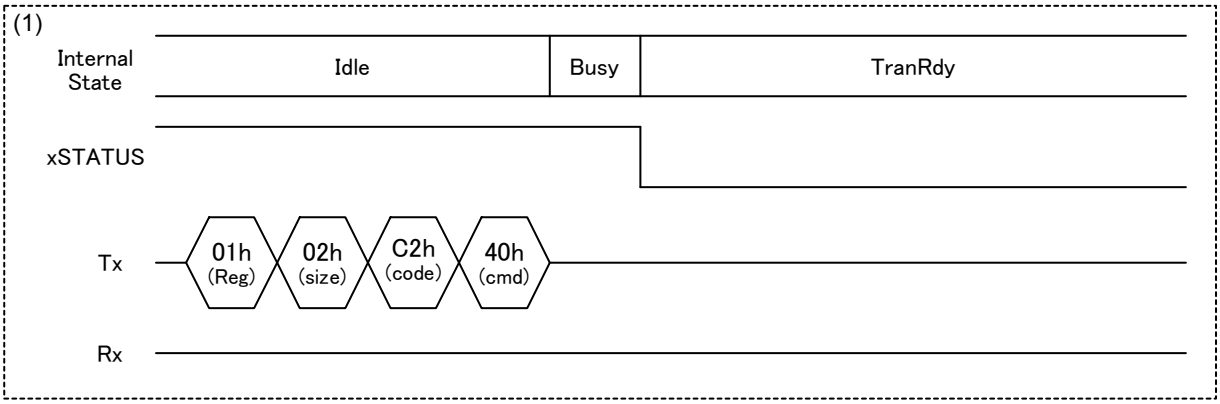
Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	02h	Total for Control code + EIreq code
	Control code	1	C2h	Fixed value
	EIreq code	2	40h	Fixed value
Data		-	xxh	Refer to “Appendix A” for details.

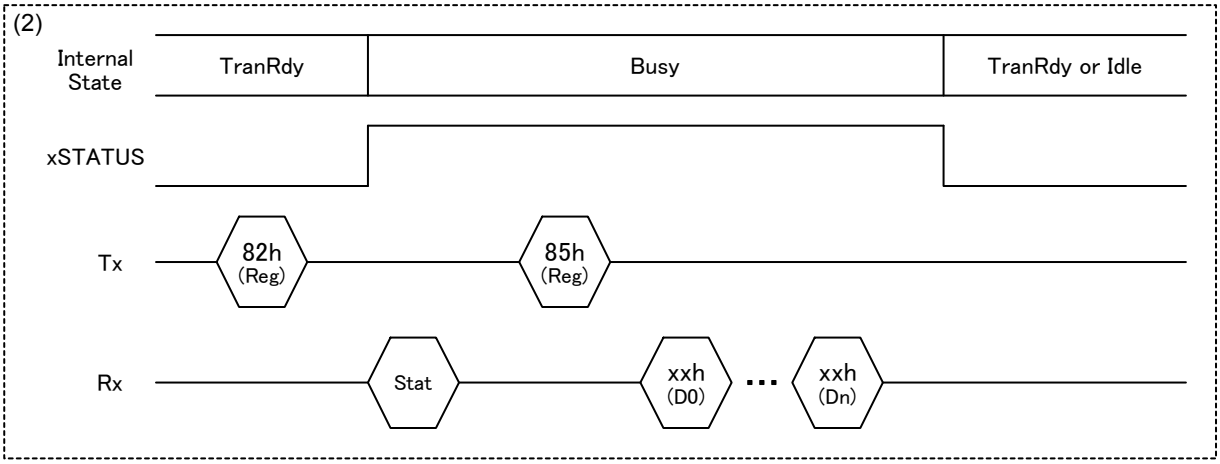
Access using protocol procedures (1) to (4). For detailed information on pin negate timing, refer to (1) to (4).

If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

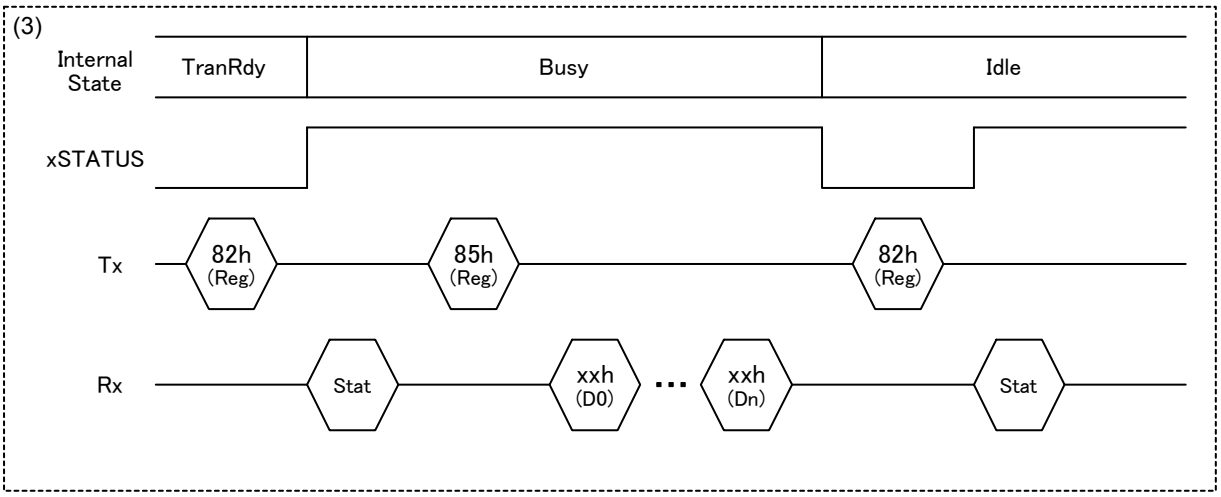
The Main CPU should acquire status information in (2) and read data after confirming that the status information is in the **TranRdy** state. “ReceiveData” (85h) is used for data reading. To continue reading (in Burst units), repeat the protocol in (2).

The final protocol for data reading will be one of two types, (3) or (4).

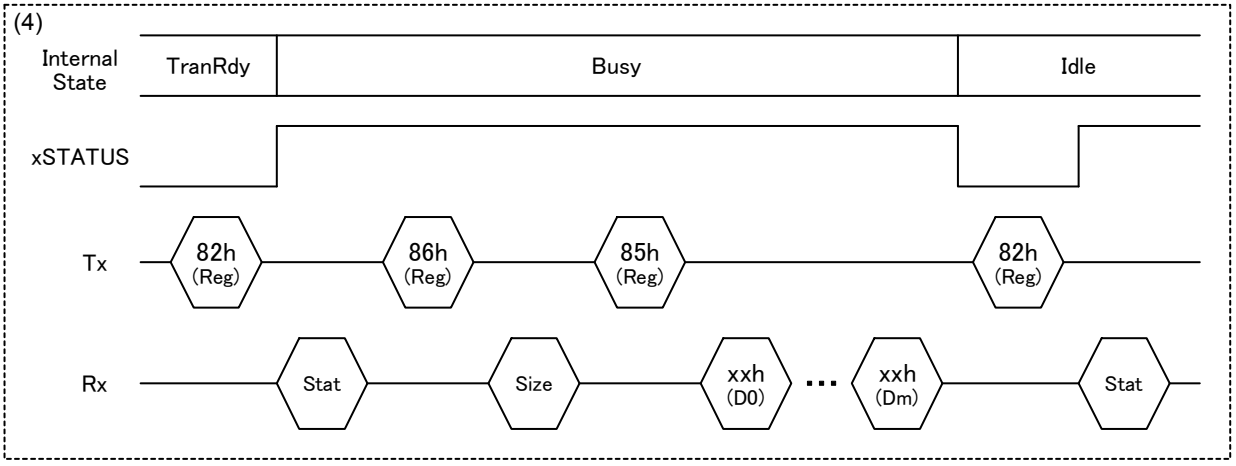




If the status information in (3) is in the **TranRdy** state, read using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. The payload data ends with this protocol.



If the status information in (4) is in the **RcvShort** + **TranRdy** state, check the valid data size using "ReceiveDataSize" (86h). Read the valid data using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. The payload data ends with this protocol.



7.7 41h_START WRITING SECTORS

This is an EIreq for simple control. This writes to the LSI settings to start sector writing (block transfer). The payload data should be written after this EIreq using the procedure described in “7.9 3Ah_BLK WRITE DATA”. For Information data settings, refer to “Appendix B MSC Access Size”.

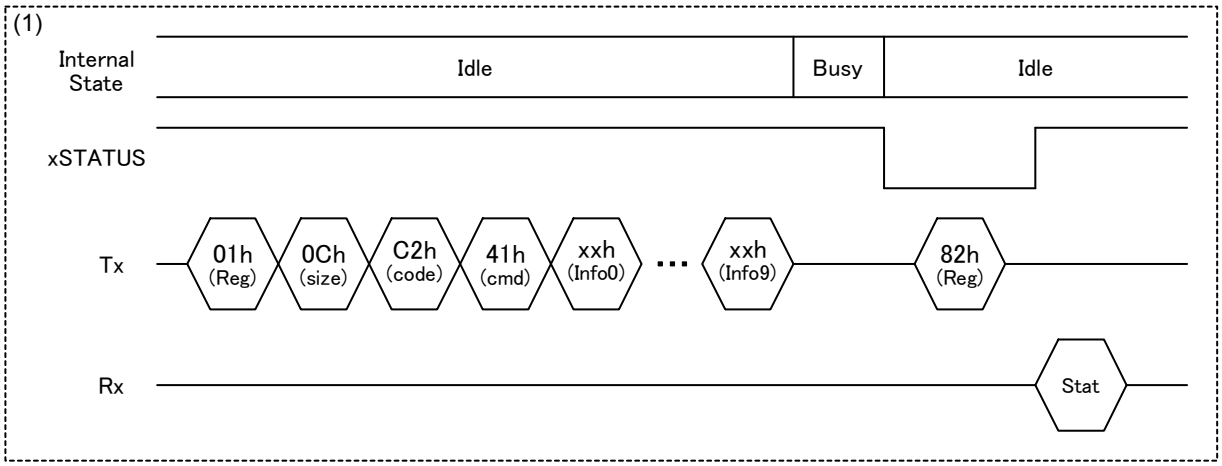
Table 7.6 START WRITING SECTORS

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	0Ch	Total for Control code + EIreq code + Information data
	Control code	1	C2h	Fixed value
	EIreq code	2	41h	Fixed value
	Information data	3	xxxxh	Sector count number 0001h to FFFFh (Block4: MSB, Block3: LSB)
		4		
		5	xxh	Access start LBA [7:0]
		6	xxh	Access start LBA [15:8]
		7	xxh	Access start LBA [23:16]
		8	xxh	Access start LBA [31:24]
		9	xxh	Access start LBA [39:32]
		10	xxh	Access start LBA [47:40]
		11	xxh	Access start LBA [55:48]
		12	xxh	Access start LBA [63:56]

Access using protocol procedure (1).

xSTATUS in (1) is asserted when the command is recognized by the LSI. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.



7.8 42h_START READING SECTORS

This is an EIreq for simple control. This writes to the LSI settings to start sector reading (block transfer). The payload data should be read after this EIreq using the procedure described in “7.10 3Bh_BLK READ DATA”. For Information data settings, refer to “Appendix B MSC Access Size”.

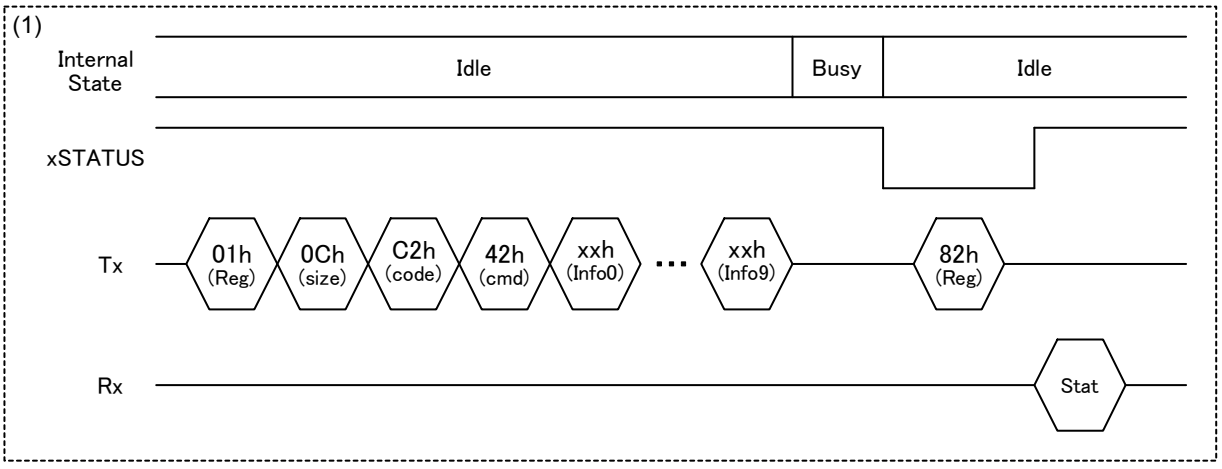
Table 7.7 START WRITING SECTORS

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	0Ch	Total for Control code + EIreq code + Information data
	Control code	1	C2h	Fixed value
	EIreq code	2	42h	Fixed value
	Information data	3	xxxxh	Sector count number 0001h to FFFFh (Block4: MSB, Block3: LSB)
		4		
		5	xxh	Access start LBA [7:0]
		6	xxh	Access start LBA [15:8]
		7	xxh	Access start LBA [23:16]
		8	xxh	Access start LBA [31:24]
		9	xxh	Access start LBA [39:32]
		10	xxh	Access start LBA [47:40]
		11	xxh	Access start LBA [55:48]
		12	xxh	Access start LBA [63:56]

Access using protocol procedure (1).

xSTATUS in (1) is asserted when the command is recognized by the LSI. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.



7.9 3Ah_BLK WRITE DATA

This writes payload data to the LSI (block transfer).

Set start writing before this EIreq using the procedure described in "7.7 41h_START WRITING SECTORS" or the THROUGH command (refer to sections 7.11 to 7.14).

Repeat the protocol procedure if writing multiple payload data.

Table 7.8 BLK WRITE DATA

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	C2h	Fixed value
	EIreq code	2	3Ah	Fixed value
	Information data	3	xxxxh	Block transfer size 0001h to 0C00h (Block4: MSB, Block3: LSB)
		4		
Data		-	xxh	Payload data

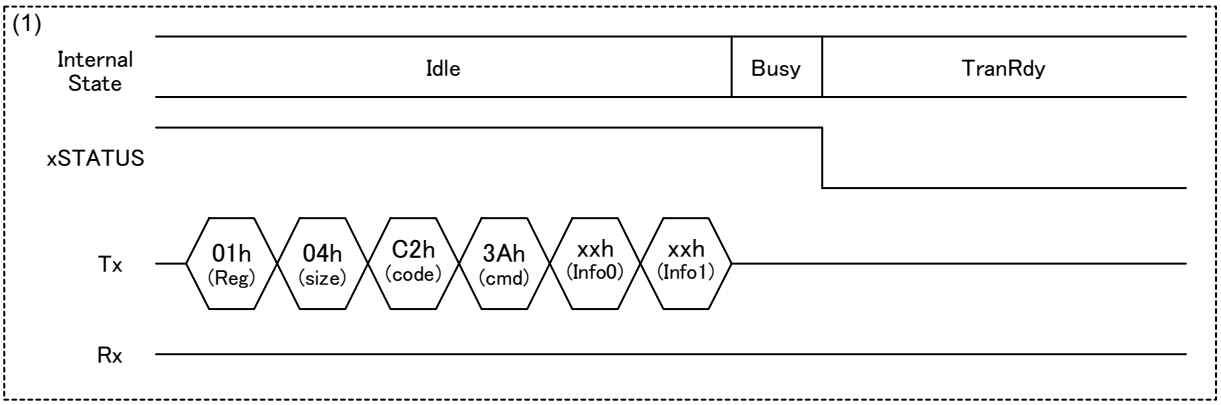
7.9.1 Ended non-notification

This protocol applies to Ended non-notification:

- When using the procedure described in "7.7 41h_START WRITING SECTORS"
- When THROUGH command Ended notification is set to "prohibited"

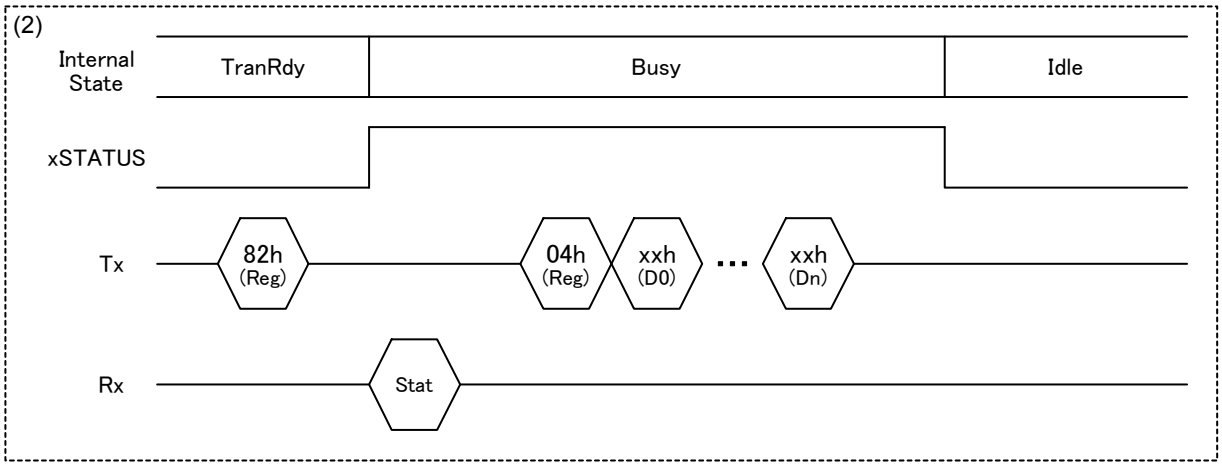
Access using protocol procedures (1) to (3). Repeat the protocol procedure if writing multiple payload data using block transfer. For detailed information on pin negate timing, refer to (1) to (3).

If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

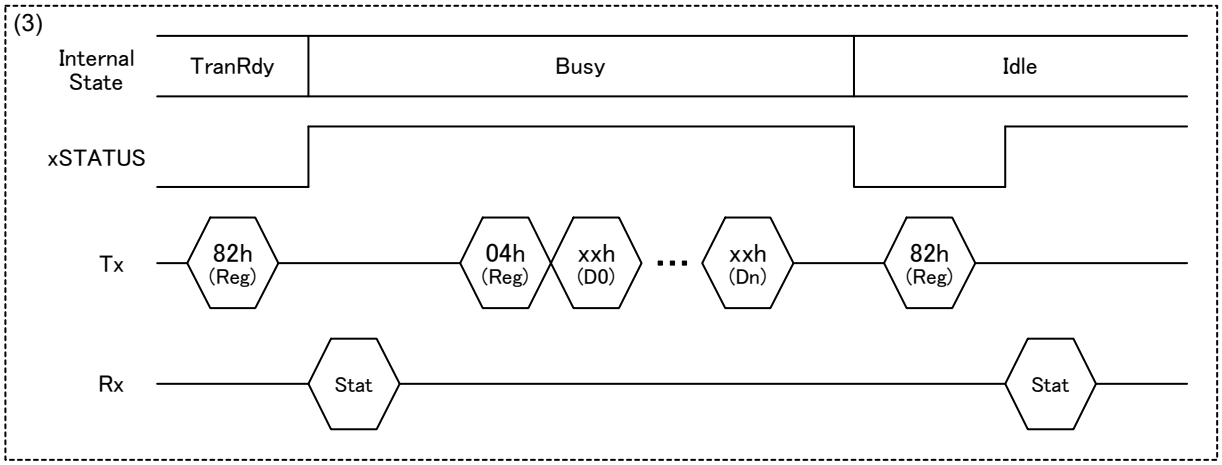


The Main CPU should acquire status information in (2) and write the data after confirming that the status information is in the **TranRdy** state. “SendData” (04h) is used to write data. To continue writing (in Burst units), repeat the protocol in (2).

The final protocol for the payload data is as shown in (3).



Confirm that the status information in (3) is in the **TranRdy** state and write using “SendData” (04h). After writing, acquire status information to confirm that the LSI is in the **Idle** state. The payload data ends with this protocol.



7.9.2 Ended notification

This protocol applies to Ended notification:

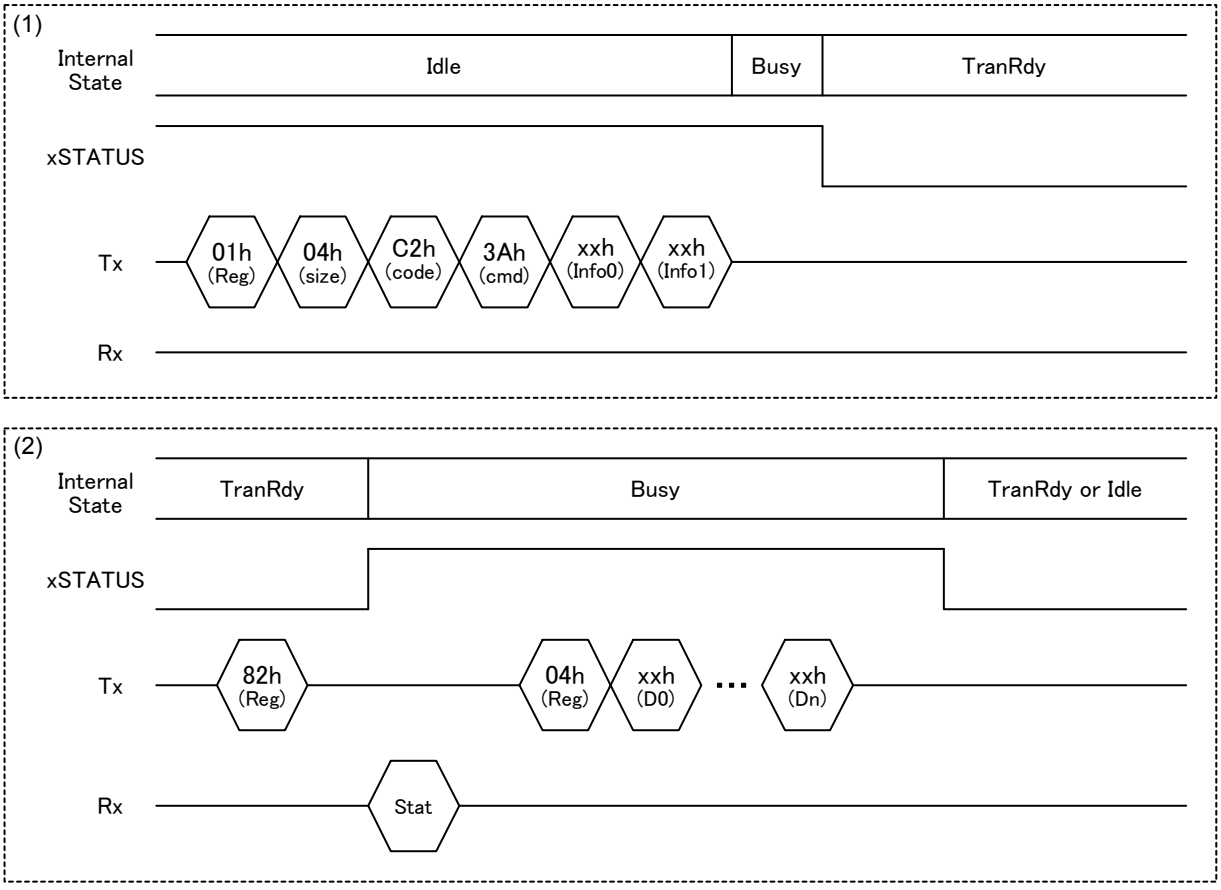
- When THROUGH command Ended notification is set to “permitted”

Access using protocol procedures (1) to (3). Repeat the protocol procedure if writing multiple payload data using block transfer. For detailed information on pin negate timing, refer to (1) to (3).

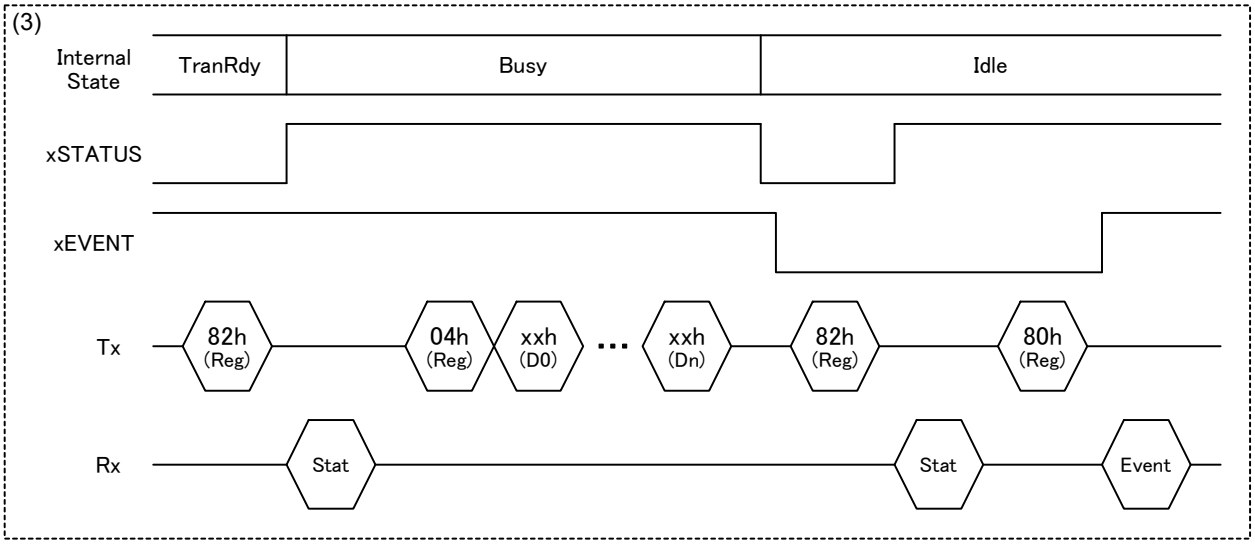
If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

The Main CPU should acquire status information in (2) and write the data after confirming that the status information is in the **TranRdy** state. “SendData” (04h) is used for data writing. To continue writing (in Burst units), repeat the protocol in (2).

The final protocol for the payload data is as shown in (3).



Confirm that the status information in (3) is in the **TranRdy** state and write using “SendData” (04h). After writing, acquire status information to confirm that the LSI is in the **Idle** state. Lastly, acquire event information. The payload data ends with this protocol.



7.10 3Bh_BLK READ DATA

This reads payload data from the LSI (block transfer).

Set start reading before this EIreq using the procedure described in “7.8 42h_START READING SECTORS” or the THROUGH command (refer to sections 7.11 to 7.14).

Repeat the protocol procedure if reading multiple payload data.

Table 7.9 BLK READ DATA

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	04h	Total for Control code + EIreq code + Information data
	Control code	1	C2h	Fixed value
	EIreq code	2	3Bh	Fixed value
	Information data	3	xxxxh	Block transfer size 0001h to 0C00h (Block4: MSB, Block3: LSB)
		4		
Data		-	xxh	Payload data

7.10.1 Ended non-notification

This protocol applies to Ended non-notification:

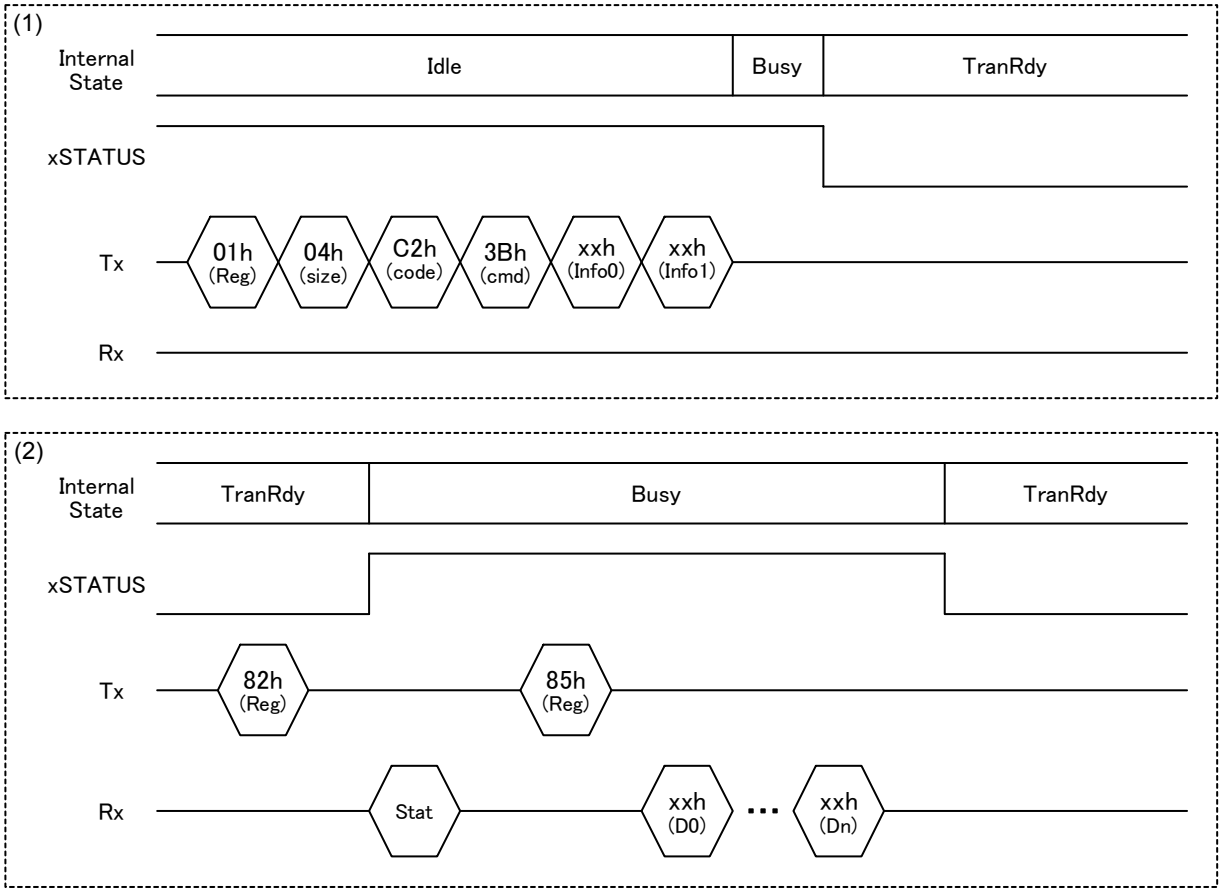
- When using the procedure described in “7.8 42h_START READING SECTORS”
- When THROUGH command Ended notification is set to “prohibited”

Access using protocol procedures (1) to (4). Repeat the protocol procedure if reading multiple payload data using block transfer. For detailed information on pin negate timing, refer to (1) to (4).

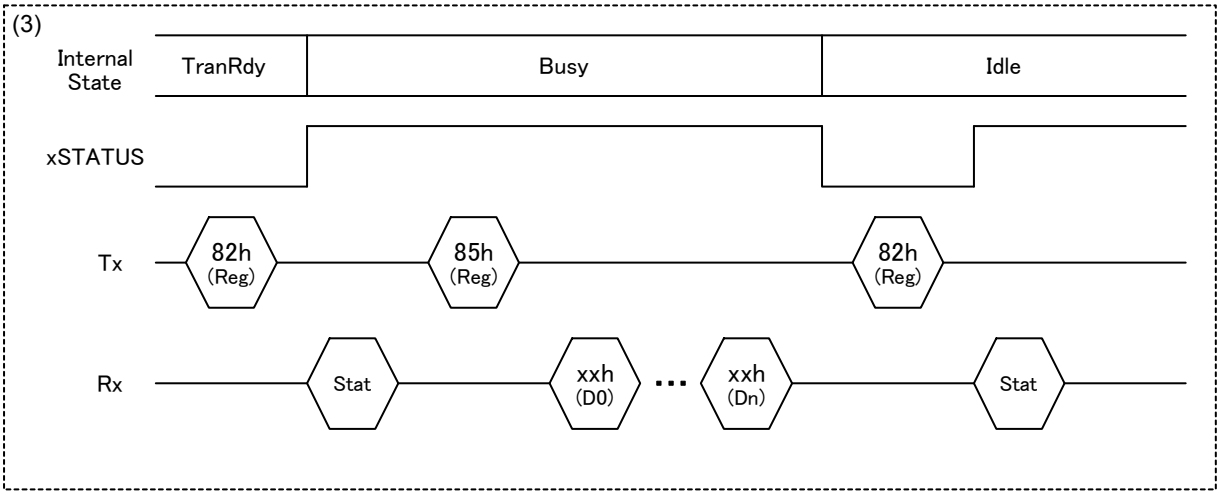
If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

The Main CPU should acquire status information in (2) and read data after confirming that the status information is in the **TranRdy** state. “ReceiveData” (85h) is used for data reading. To continue reading (in Burst units), repeat the protocol in (2).

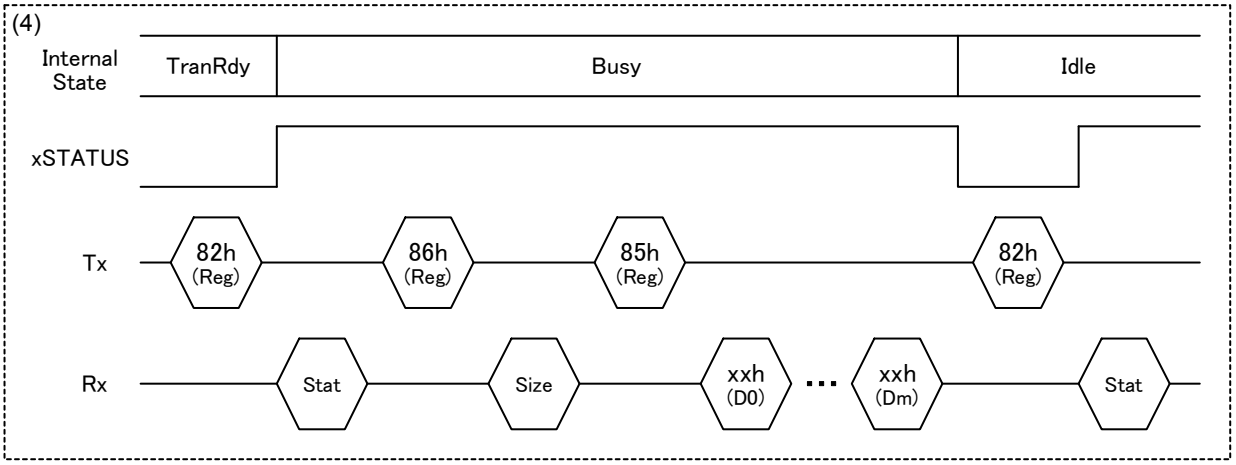
The final protocol for the payload data will be one of two types, (3) or (4).



If the status information in (3) is in the **TranRdy** state, read using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. The payload data ends with this protocol.



If the status information in (4) is in the **RcvShort** + **TranRdy** state, check the valid data size using "ReceiveDataSize" (86h). Read the valid data using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. The payload data ends with this protocol.



7.10.2 Ended notification

This protocol applies to Ended notification:

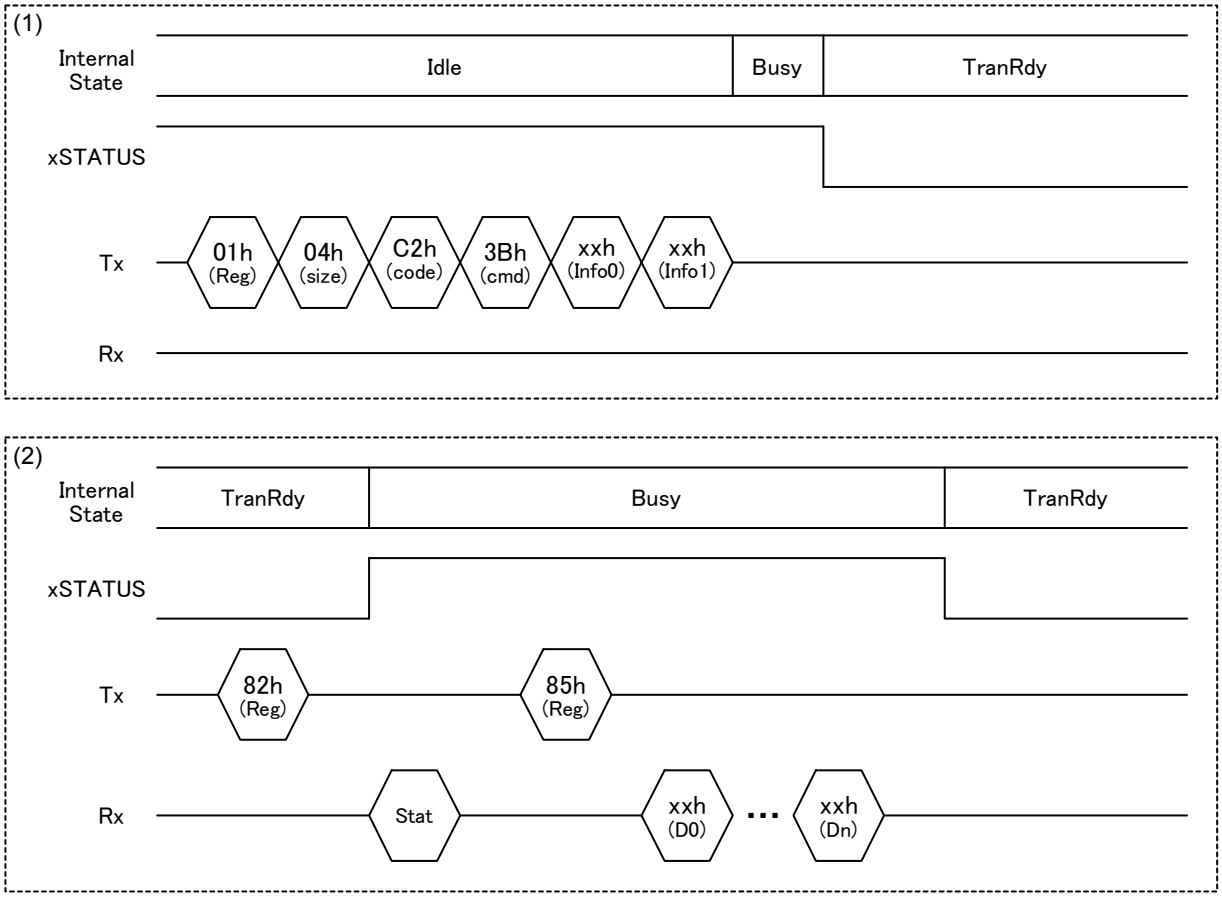
- When THROUGH command Ended notification is set to “permitted”

Access using protocol procedures (1) to (4). Repeat the protocol procedure if reading multiple payload data using block transfer. For detailed information on pin negate timing, refer to (1) to (4).

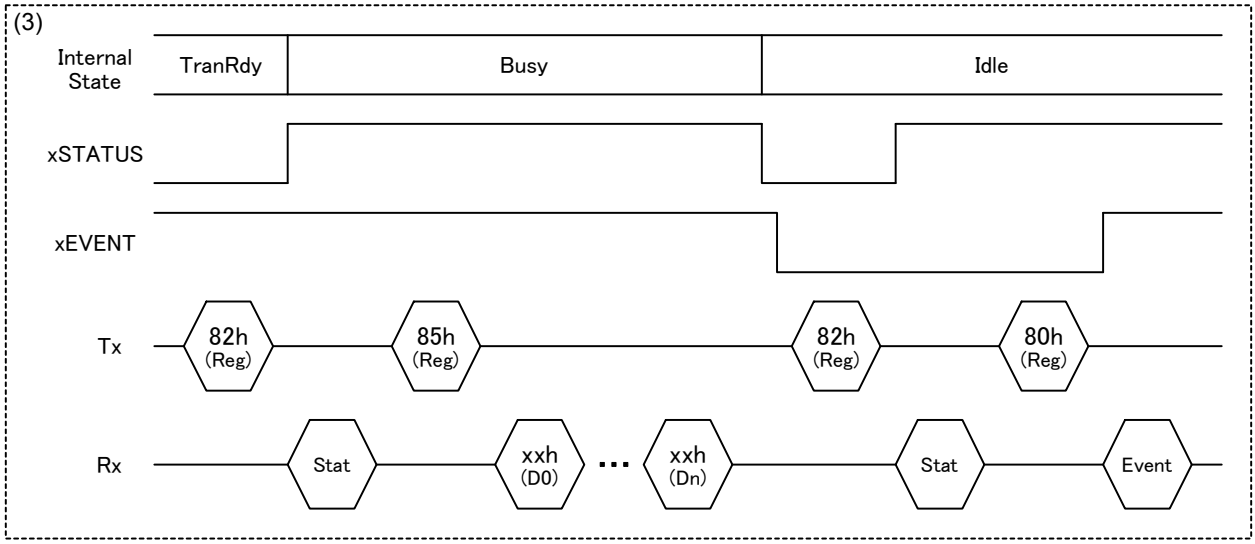
If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

The Main CPU should acquire status information in (2) and read data after confirming that the status information is in the **TranRdy** state. “ReceiveData” (85h) is used for data reading. To continue reading (in Burst units), repeat the protocol in (2).

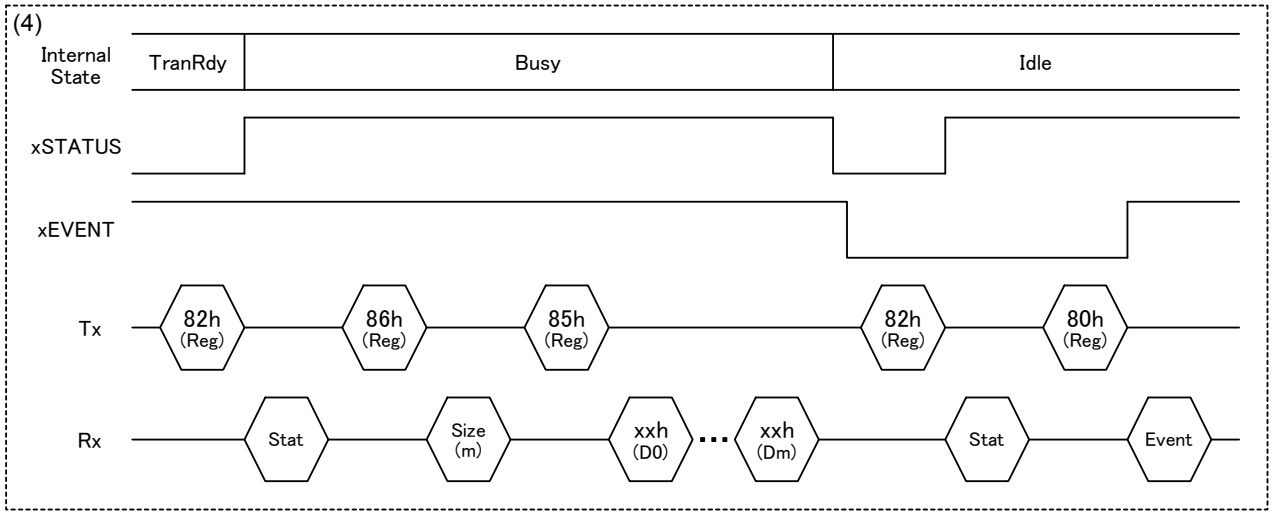
The final protocol for the payload data will be one of two types, (3) or (4).



If the status information in (3) is in the **TranRdy** state, read using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. Lastly, acquire event information. The payload data ends with this protocol.



If the status information in (4) is in the **RcvShort** + **TranRdy** state, check the valid data size using "ReceiveDataSize" (86h). Read the valid data using "ReceiveData" (85h). After reading, acquire status information to confirm that the LSI is in the **Idle** state. Lastly, acquire event information. The payload data ends with this protocol.



7.11 48h_STORAGE COMMAND THROUGH (6)

This is an EIreq for full control. This writes a 6-byte SCSI/ATAPI command to the LSI.

When this accompanies data reading or writing, the payload data should be processed after this EIreq using the procedure described in “7.9 3Ah_BLK WRITE DATA” or “7.10 3Bh_BLK READ DATA”.

In the case of “No data”, the total number of data transfer bytes should be set to “00h”.

Table 7.10 STORAGE COMMAND THROUGH (6)

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	0Dh	Total for Control code + EIreq code + Information data
	Control code	1	C2h	Fixed value
	EIreq code	2	48h	Fixed value
	Information data	3	xxh	Command protocol
		4	xxh	Total number of data transfer bytes [7:0]
		5	xxh	Total number of data transfer bytes [15:8]
		6	xxh	Total number of data transfer bytes [23:16]
		7	xxh	Total number of data transfer bytes [31:24]
		8	xxh	SCSI/ATAPI command packet [0]
		9	xxh	SCSI/ATAPI command packet [1]
		10	xxh	SCSI/ATAPI command packet [2]
		11	xxh	SCSI/ATAPI command packet [3]
		12	xxh	SCSI/ATAPI command packet [4]
		13	xxh	SCSI/ATAPI command packet [5]

Bit	Content	Setting value
7	Command Through Ended event notification setting	0b: prohibited 1b: permitted (default)
6-2	reserved	
1-0	Transfer specification	00b: No data 01b: Read 10b: Write 11b: reserved

7.11.1 Ended non-notification

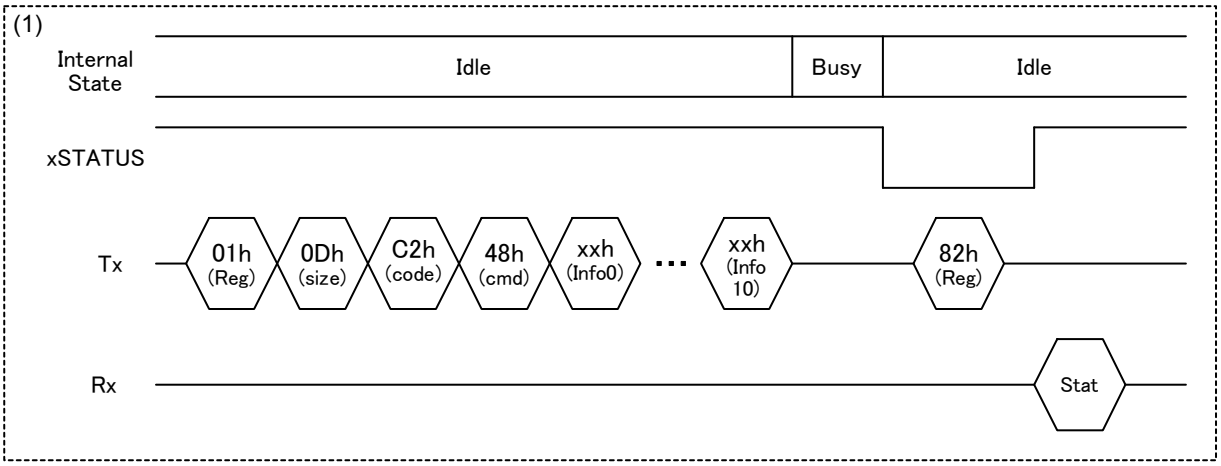
This protocol applies to Ended non-notification:

- When “Read” or “Write” is set
- When Ended notification is set to “prohibited” with “No data”

Access using protocol procedure (1).

The LSI asserts xSTATUS in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.



7.11.2 Ended notification

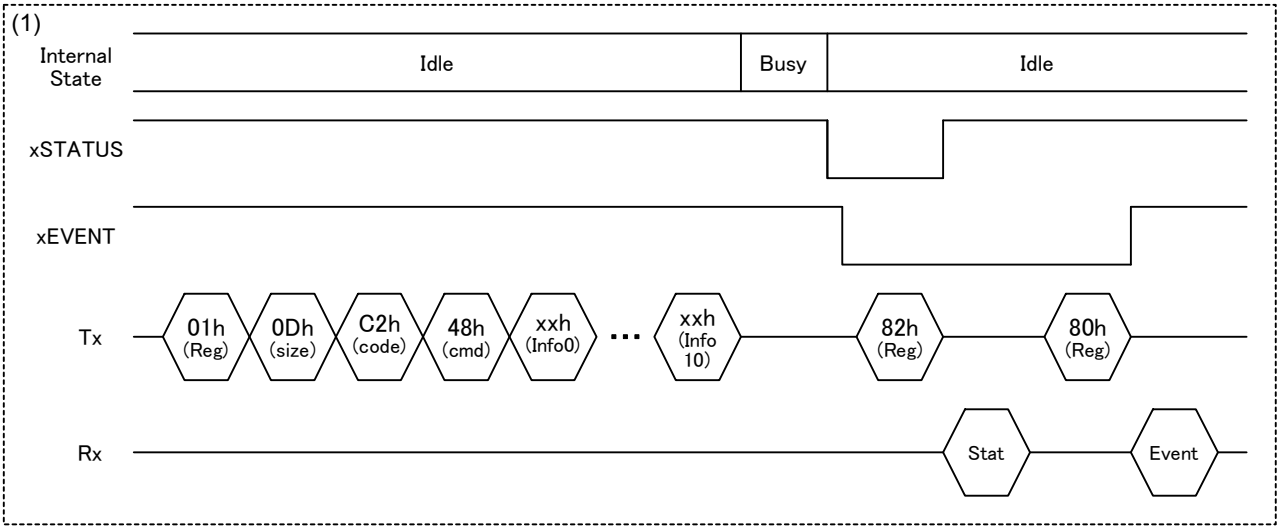
This protocol applies to Ended notification:

- When Ended notification is set to “permitted” with “No data”

Access using protocol procedure (1).

The LSI asserts xSTATUS and xEVENT in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state. Lastly, acquire event information.



7.12 49h_STORAGE COMMAND THROUGH (10)

This is an EIreq for full control. This writes a 10-byte SCSI/ATAPI command to the LSI.

When this accompanies data reading or writing, the payload data should be processed after this EIreq using the procedure described in “7.9 3Ah_BLK WRITE DATA” or “7.10 3Bh_BLK READ DATA”.

In the case of “No data”, the total number of data transfer bytes should be set to “00h”.

Table 7.11 STORAGE COMMAND THROUGH (10)

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	11h	Total for Control code + EIreq code + Information data
	Control code	1	C2h	Fixed value
	EIreq code	2	49h	Fixed value
	Information data	3	xxh	Command protocol
		4	xxh	Total number of data transfer bytes [7:0]
		5	xxh	Total number of data transfer bytes [15:8]
		6	xxh	Total number of data transfer bytes [23:16]
		7	xxh	Total number of data transfer bytes [31:24]
		8	xxh	SCSI/ATAPI command packet [0]
		9	xxh	SCSI/ATAPI command packet [1]
		10	xxh	SCSI/ATAPI command packet [2]
		11	xxh	SCSI/ATAPI command packet [3]
		12	xxh	SCSI/ATAPI command packet [4]
		13	xxh	SCSI/ATAPI command packet [5]
		14	xxh	SCSI/ATAPI command packet [6]
		15	xxh	SCSI/ATAPI command packet [7]
		16	xxh	SCSI/ATAPI command packet [8]
		17	xxh	SCSI/ATAPI command packet [9]

Bit	Content	Setting value
7	Command Through Ended event notification setting	0b: prohibited 1b: permitted (default)
6-2	reserved	
1-0	Transfer specification	00b: No data 01b: Read 10b: Write 11b: reserved

7.12.1 Ended non-notification

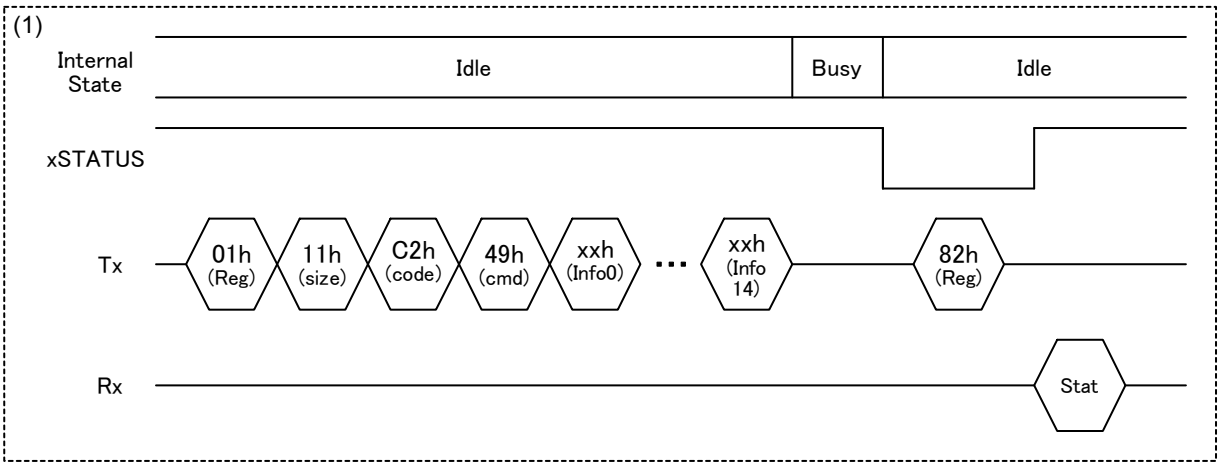
This protocol applies to Ended non-notification:

- When “Read” or “Write” is set
- When Ended notification is set to “prohibited” with “No data”

Access using protocol procedure (1).

The LSI asserts xSTATUS in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.



7.12.2 Ended notification

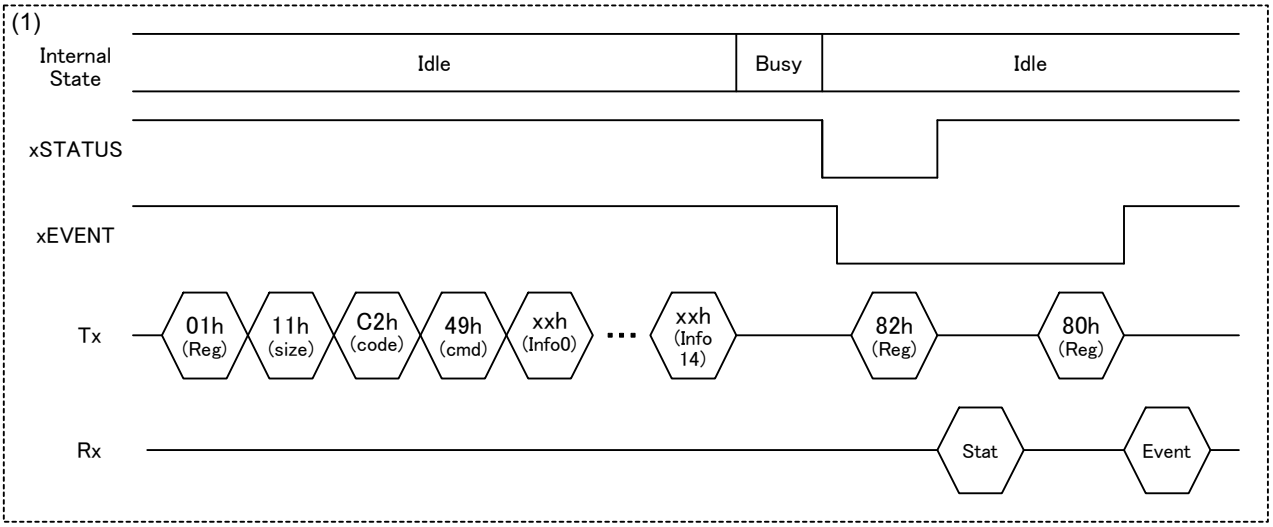
This protocol applies to Ended notification:

- When Ended notification is set to “permitted” with “No data”

Access using protocol procedure (1).

The LSI asserts xSTATUS and xEVENT in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state. Lastly, acquire event information.



7.13 4Ah_STORAGE COMMAND THROUGH (12)

This is an EIreq for full control. This writes a 12-byte SCSI/ATAPI command to the LSI.

When this accompanies data reading or writing, the payload data should be processed after this EIreq using the procedure described in “7.9 3Ah_BLK WRITE DATA” or “7.10 3Bh_BLK READ DATA”.

In the case of “No data”, the total number of data transfer bytes should be set to “00h”.

Table 7.12 STORAGE COMMAND THROUGH (12)

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	13h	Total for Control code + EIreq code + Information data
	Control code	1	C2h	Fixed value
	EIreq code	2	4Ah	Fixed value
	Information data	3	xxh	Command protocol
		4	xxh	Total number of data transfer bytes [7:0]
		5	xxh	Total number of data transfer bytes [15:8]
		6	xxh	Total number of data transfer bytes [23:16]
		7	xxh	Total number of data transfer bytes [31:24]
		8	xxh	SCSI/ATAPI command packet [0]
		9	xxh	SCSI/ATAPI command packet [1]
		10	xxh	SCSI/ATAPI command packet [2]
		11	xxh	SCSI/ATAPI command packet [3]
		12	xxh	SCSI/ATAPI command packet [4]
		13	xxh	SCSI/ATAPI command packet [5]
		14	xxh	SCSI/ATAPI command packet [6]
		15	xxh	SCSI/ATAPI command packet [7]
		16	xxh	SCSI/ATAPI command packet [8]
		17	xxh	SCSI/ATAPI command packet [9]
		18	xxh	SCSI/ATAPI command packet [10]
		19	xxh	SCSI/ATAPI command packet [11]

Command protocol

Bit	Content	Setting value
7	Command Through Ended event notification setting	0b: prohibited 1b: permitted (default)
6-2	reserved	
1-0	Transfer specification	00b: No data 01b: Read 10b: Write 11b: reserved

7.13.1 Ended non-notification

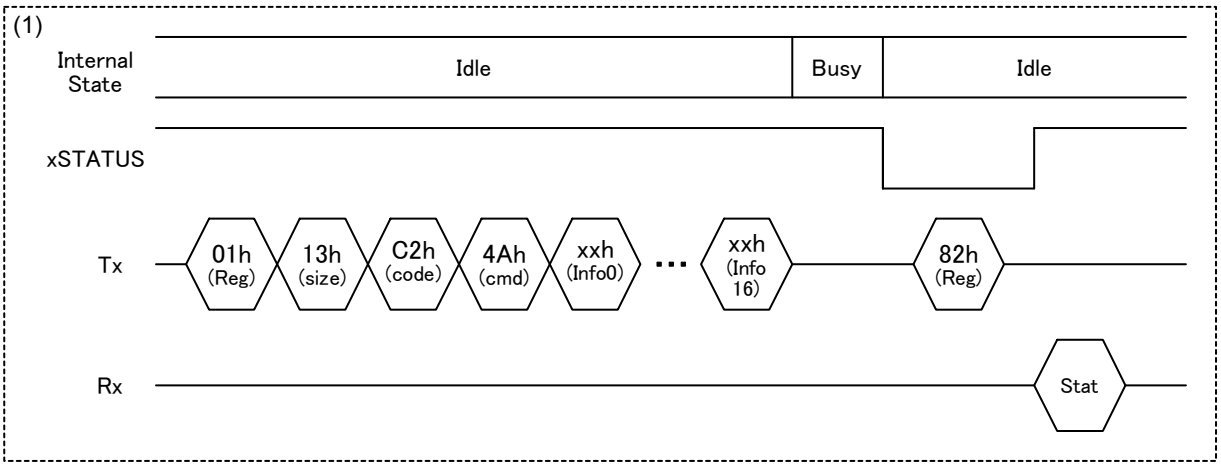
This protocol applies to Ended non-notification:

- When “Read” or “Write” is set
- When Ended notification is set to “prohibited” with “No data”

Access using protocol procedure (1).

The LSI asserts xSTATUS in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.



7.13.2 Ended notification

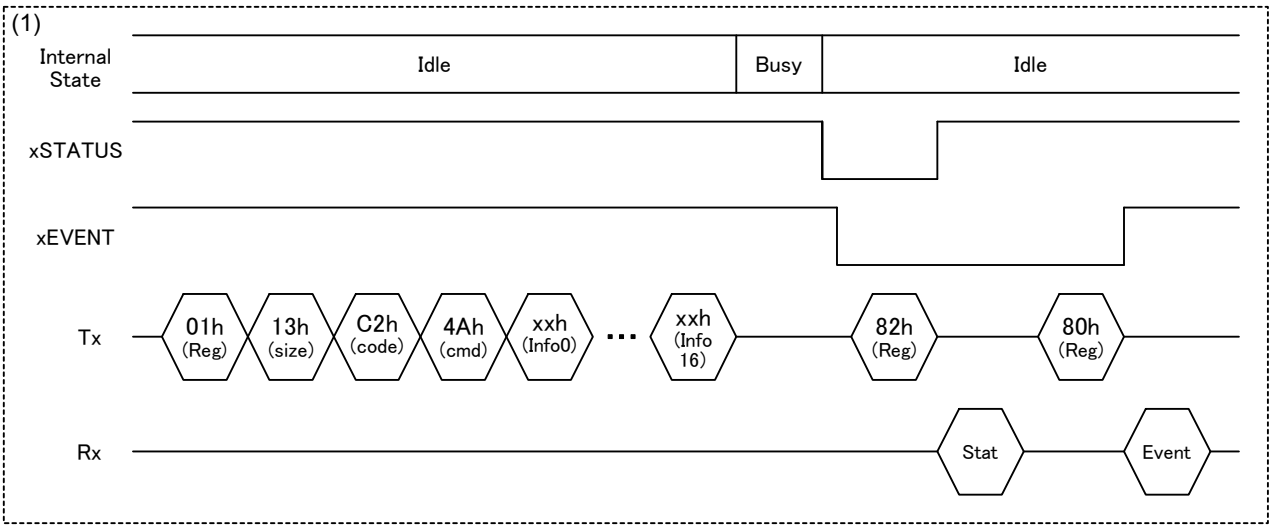
This protocol applies to Ended notification:

- When Ended notification is set to “permitted” with “No data”

Access using protocol procedure (1).

The LSI asserts xSTATUS and xEVENT in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state. Lastly, acquire event information.



7.14 4Bh_STORAGE COMMAND THROUGH (16)

This is an EIreq for full control. This writes a 16-byte SCSI/ATAPI command to the LSI.

When this accompanies data reading or writing, the payload data should be processed after this EIreq using the procedure described in “7.9 3Ah_BLK WRITE DATA” or “7.10 3Bh_BLK READ DATA”.

In the case of “No data”, the total number of data transfer bytes should be set to “00h”.

Table 7.13 STORAGE COMMAND THROUGH (16)

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	17h	Total for Control code + EIreq code + Information data
	Control code	1	C2h	Fixed value
	EIreq code	2	4Bh	Fixed value
	Information data	3	xxh	Command protocol
		4	xxh	Total number of data transfer bytes [7:0]
		5	xxh	Total number of data transfer bytes [15:8]
		6	xxh	Total number of data transfer bytes [23:16]
		7	xxh	Total number of data transfer bytes [31:24]
		8	xxh	SCSI/ATAPI command packet [0]
		9	xxh	SCSI/ATAPI command packet [1]
		10	xxh	SCSI/ATAPI command packet [2]
		11	xxh	SCSI/ATAPI command packet [3]
		12	xxh	SCSI/ATAPI command packet [4]
		13	xxh	SCSI/ATAPI command packet [5]
		14	xxh	SCSI/ATAPI command packet [6]
		15	xxh	SCSI/ATAPI command packet [7]
		16	xxh	SCSI/ATAPI command packet [8]
		17	xxh	SCSI/ATAPI command packet [9]
		18	xxh	SCSI/ATAPI command packet [10]
		19	xxh	SCSI/ATAPI command packet [11]
		20	xxh	SCSI/ATAPI command packet [12]
		21	xxh	SCSI/ATAPI command packet [13]
		22	xxh	SCSI/ATAPI command packet [14]
		23	xxh	SCSI/ATAPI command packet [15]

Command protocol (Information data, Block 3, Value xxh):

Bit	Content	Setting value
7	Command Through Ended event notification setting	0b: prohibited 1b: permitted (default)
6-2	reserved	
1-0	Transfer specification	00b: No data 01b: Read 10b: Write 11b: reserved

7.14.1 Ended non-notification

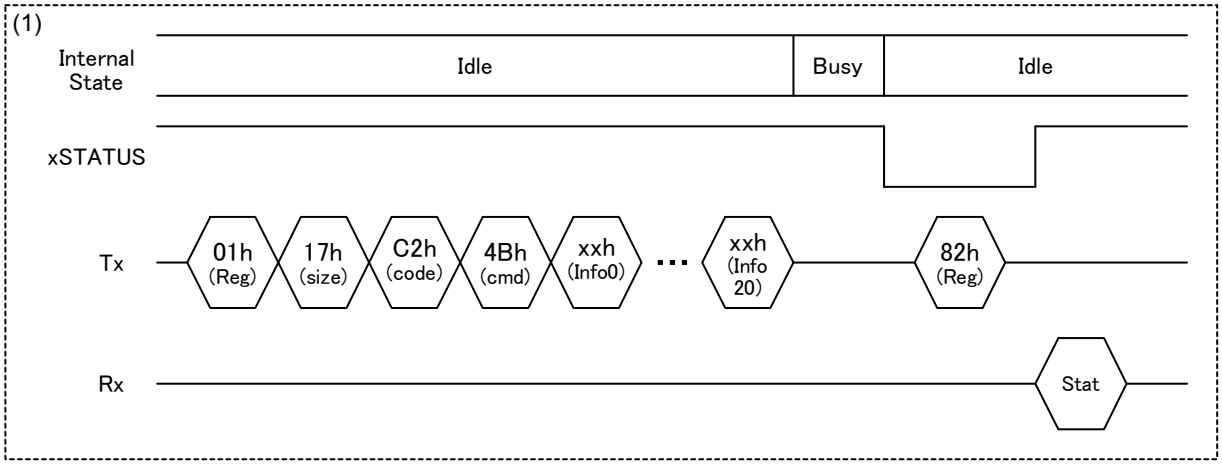
This protocol applies to Ended non-notification:

- When “Read” or “Write” is set
- When Ended notification is set to “prohibited” with “No data”

Access using protocol procedure (1).

The LSI asserts xSTATUS in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state.



7.14.2 Ended notification

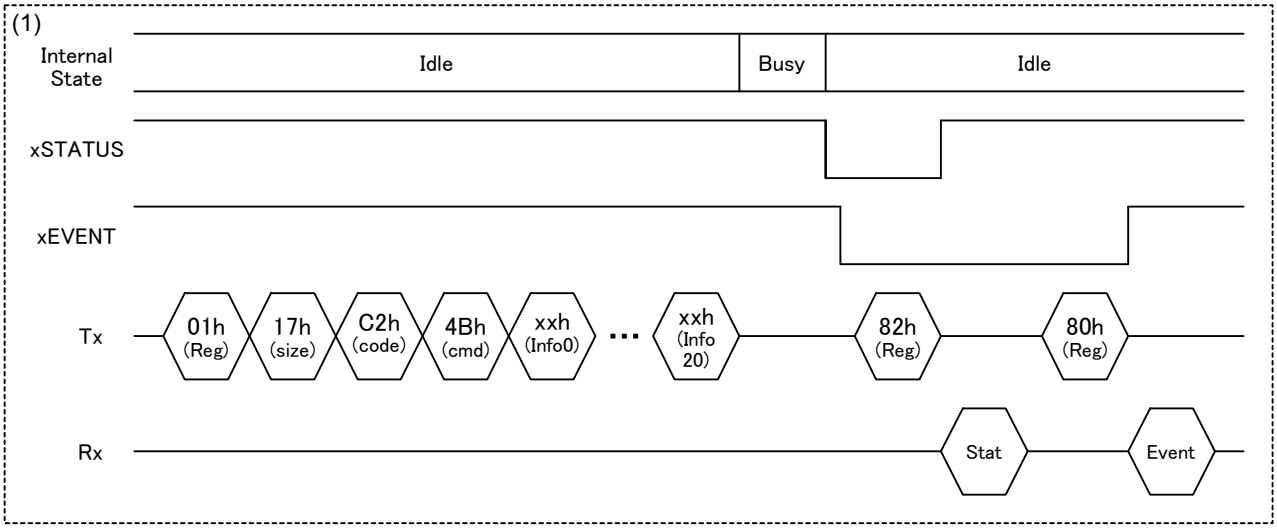
This protocol applies to Ended notification:

- When Ended notification is set to “permitted” with “No data”

Access using protocol procedure (1).

The LSI asserts xSTATUS and xEVENT in (1) when command processing has ended. For detailed information on negate timing, refer to (1).

The Main CPU should acquire status information to confirm that the LSI is in the **Idle** state. Lastly, acquire event information.



7.15 4Ch_STORAGE COMMAND RESULT

This is an EIreq for full control. It checks the SCSI/ATAPI command results using the THROUGH command (refer to sections 7.11 to 7.14).

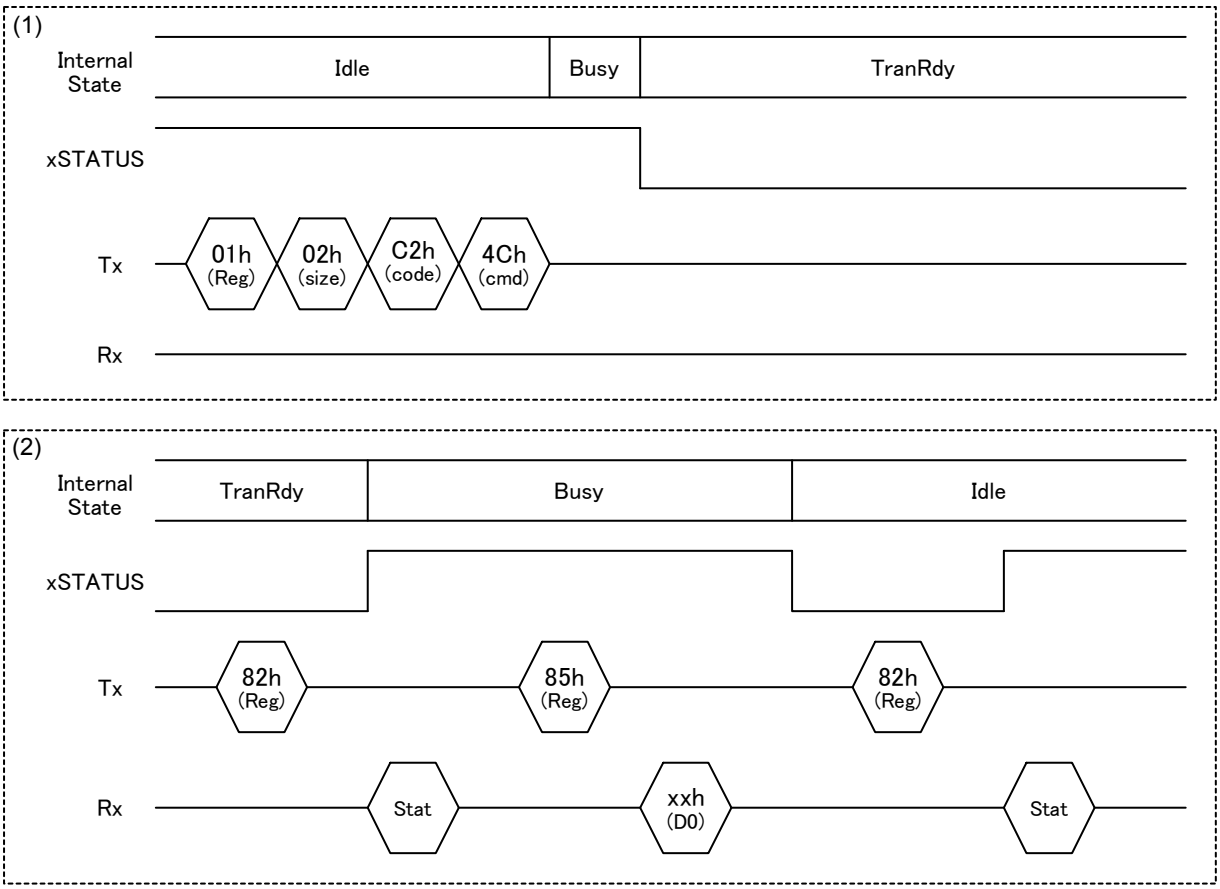
Table 7.14 STORAGE COMMAND RESULT

Content		Block	Value	Description
Register		-	01h	EIRequest
EIreq	Block size	0	02h	Total for Control code + EIreq code
	Control code	1	C2h	Fixed value
	EIreq code	2	4Ch	Fixed value
Data		-	xxh	00h: Success 01h: Failure

Access using protocol procedures (1) and (2). For detailed information on pin negate timing, refer to (1) and (2).

If the LSI switches to the **TranRdy** state, xSTATUS in (1) is asserted.

The Main CPU should acquire status information in (2) and read data after confirming that the status information is in the **TranRdy** state. "ReceiveData" (85h) is used for data reading. After reading, acquire status information to confirm that the LSI is in the **Idle** state.



Appendix A Storage Information

Table A.1 lists the Device storage information that can be obtained using “GET STORAGE INFORMATION” (40h). Storage information is set to a constant 39 bytes of data.

Table A.1 Storage Information

Content	Size (Byte)	Description
Device type	1	Device type 00h: direct access device (e.g HDD) 01h: sequential access device (e.g tape device) 02h: printer device 03h: processor device (e.g graphic display) 04h: write once device (May be included in optical memory device) 05h: CD-ROM device 06h: scanner device 07h: optical memory device (e.g MO) 08h: media changer device (e.g CD changer) 09h: communication device Device type Bit7 has the following meanings: 0b: fixed 1b: removable
vender id	8	Vendor ID (ASCII)
product id	16	Product ID (ASCII)
product revision	4	Product version (ASCII)
sector size	2	Sector size [7:0]
		Sector size [15:8]
Maximum logical block address	8	Max. LBA [7:0]
		Max. LBA [15:8]
		Max. LBA [23:16]
		Max. LBA [31:24]
		Max. LBA [39:32]
		Max. LBA [47:40]
		Max. LBA [55:48]
		Max. LBA [63:56]

Appendix B MSC Access Size

The MSC Device capacity and Access size are explained below.

The Main CPU should check the accessible size using "GET STORAGE INFORMATION" (40h). Figure B.1 illustrates the MSC Device capacity.

The MSC Device capacity accessible by the Main CPU is the total of the individual Sector sizes.

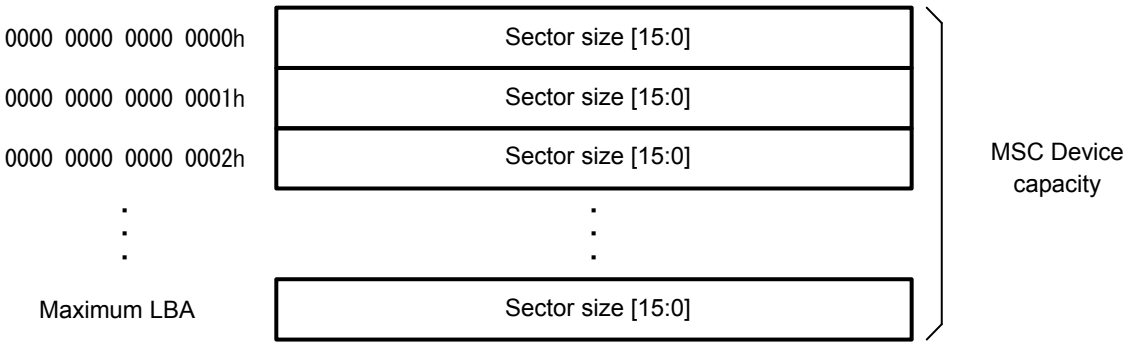


Figure B.1 MSC Device capacity

The example below describes setting the Access size shown in Figure B.2 to EIreq. Figure B.3 illustrates the setting configuration.

In this example, EIreq will be set as shown below. Note that this LSI retains the Sector size information, and so the Main CPU sets the sector count number.

In this setting example, an Access size of 2,048 bytes is set, and data is read in 256-byte block transfers from the 0000 0000 0000 010h LBA.

"START READING SECTORS" (42h)

- Sector count number = 0004h (4 x 512 = 2,048 bytes)
- Access start LBA = 0000 0000 0000 010h

"BLK READ DATA" (3Bh)

- Block transfer size = 0100h (set to an appropriate size as desired)

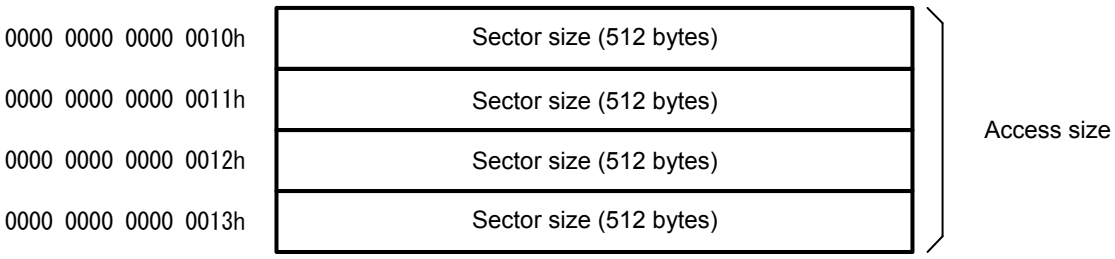


Figure B.2 Access size

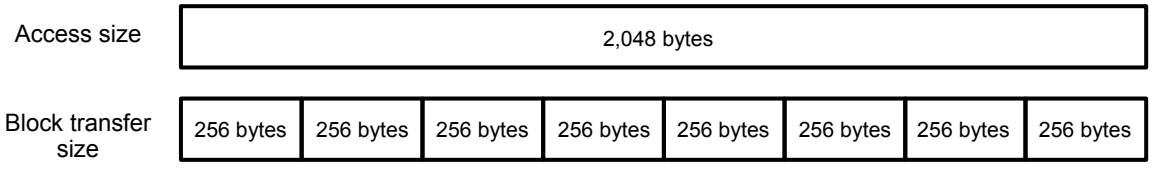


Figure B.3 Setting configuration

Appendix C SCSI/ATAPI Command Control

Table C.1 lists the SCSI/ATAPI command control details.

Table C.1 Control details

Elreq	SCSI/ATAPI command	
GET STORAGE INFORMATION	INQUIRY	*1
	READ CAPACITY(10)	*1, *2
	READ CAPACITY(16)	*1, *2
	REQUEST SENSE	*3
START WRITING SECTORS	WRITE(10)	*2
	WRITE(16)	*2
	REQUEST SENSE	*3
START READING SECTORS	READ(10)	*2
	READ(16)	*2
	REQUEST SENSE	*3
BLK WRITE DATA	None	
BLK READ DATA	None	
STORAGE COMMAND THROUGH (6)	SCSI/ATAPI command packet	*4
STORAGE COMMAND THROUGH (10)	SCSI/ATAPI command packet	*4
STORAGE COMMAND THROUGH (12)	SCSI/ATAPI command packet	*4
STORAGE COMMAND THROUGH (16)	SCSI/ATAPI command packet	*4
STORAGE COMMAND RESULT	None	

*1 Retries for “MEDIUM CHANGED” or “POWER ON RESET”.

*2 Transmits appropriate SCSI/ATAPI command to suit MSC Device.

*3 Transmitted if error occurs in SCSI/ATAPI command.

*4 Transmits SCSI/ATAPI command packet written from Main CPU to MSC Device.

Revision History

Attachment-1

Rev. No.	Date	Page	Category	Revision details (including previous details) and reason
Rev. 1.00	4/6/2009	All	New	Newly established
Rev. 1.01	4/23/2009	3	Add	Added 2.2 (12)

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International Sales Operations

AMERICA

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