Connector Pin Assignment Table of S1R72V03 or S1R72V05 Evaluation Board for CPU Accesssing

2005/6/24

Pin No.	Signal Name (CPU Board/Toya)	Signal Name (S1R72V03 Board)	I/O at V03 Board	Notes
A1	+3.3V	+3.3V	0	Regulator supplies Power to CPU board
A2	+3.3V	+3.3V	O	Regulator supplies Power to CPU board
A3	GND	GND	(GND)	---
A4	+5V	+5V	O	From External Power source
A5	+5V	+5V	O	From External Power source
A6	GND	GND	(GND)	
A7	GND	GND	(GND)	
A8	GND	GND	(GND)	
A9	RESET#/PORRST#	XRESET	I	Reset from CPU board
A10	DACK1#	XDACK1	I	(DMA Ch1) Ack
A11	GND	GND	(GND)	---
A12	DACK0#	XDACK0	I	(DMA Ch0) Ack
A13	GND	GND	(GND)	
A14	SRDY1#	---	---	---
A15	TxD1	---	---	---
A16	GND	GND	(GND)	
A17	GPIOA[1]	---	---	---
A18	MCLK	---	---	---
A19	open	---	---	---
A20	GND	GND	(GND)	
A21	open	---	---	---
A22	WAIT#	---	---	---
A23	MDQM1	XWRH	I	Upper Byte WrEnb
A24	GND	GND	(GND)	
A25	MCS5#	---	---	---
A26	MCS4#	---	---	---
A27	GND	GND	(GND)	
A28	MD15	CD15	I/O	Data_15
A29	MD13	CD13	I/O	Data_13
A30	MD11	CD11	I/O	Data_11
A31	MD9	CD9	I/O	Data_9
A32	GND	GND	(GND)	
A33	MD7	CD7	I/O	Data_7
A34	MD5	CD5	I/O	Data_5
A35	MD3	CD3	I/O	Data_3
A36	MD1	CD1	I/O	Data_1
A37	GND	GND	(GND)	
A38	MA18	---	---	---
A39	MA16	---	---	---
A40	GND	GND	(GND)	
A41	MA14	---	---	---
A42	MA12	---	---	---
A43	MA10	---	---	---
A44	MA8	---	---	---
A45	GND	GND	(GND)	
A46	MA6	CA7	I	Address_7
A47	MA4	CA5	I	Address_5
A48	MA2	CA3	I	Address_3
A49	MA0	CA1	I	Address_1
A50	GND	GND	(GND)	

Pin No.	Signal Name (CPU Board/Toya)	Signal Name (S1R72V03 Board)	I/O at V03 Board	Notes
B1	+3.3V	+3.3V	O	Regulator supplies Power to CPU board
B2	+3.3V	+3.3V	O	Regulator supplies Power to CPU board
B3	GND	GND	(GND)	
B4	+5V	+5V	O	From External Power source
B5	+5V	+5V	O	From External Power source
B6	GND	GND	(GND)	
B7	open	---	---	---
B8	GND	GND	(GND)	
B9	open	---	---	---
B10	DREQ1#	XDREQ1	O	(DMA Ch1) Req
B11	GND	GND	(GND)	
B12	DREQ0#	XDREQ0	O	(DMA Ch0) Req
B13	GND	GND	(GND)	
B14	SCLK1	---	---	---
B15	RxD1	---	---	---
B16	GND	GND	(GND)	
B17	GPIOA[0]	---	---	---
B18	open	---	---	---
B19	INT7	XINT	O	It asserts Interruption to CPU
B20	GND	GND	(GND)	
B21	open	---	---	---
B22	MWE0#	XWRL	I	WrEnb (for Flash, SRAM)
B23	MOE#	XRD	I	OutEnb (for Flash,ROM,SRAM)
B24	GND	GND	(GND)	
B25	MCS1#	XCS	I	CS1 (for target chip)
B26	MCS0#	---	---	---
B27	GND	GND	(GND)	
B28	MD14	CD14	I/O	Data_14
B29	MD12	CD12	I/O	Data_12
B30	MD10	CD10	I/O	Data_10
B31	MD8	CD8	I/O	Data_8
B32	GND	GND	(GND)	
B33	MD6	CD6	I/O	Data_6
B34	MD4	CD4	I/O	Data_4
B35	MD2	CD2	I/O	Data_2
B36	MD0	CD0	I/O	Data_0
B37	GND	GND	(GND)	
B38	MA17	---	---	---
B39	MA15	---	---	---
B40	GND	GND	(GND)	
B40	MA13	---	---	---
B42	MA11	---	---	---
B43	MA9	---	---	---
B44(*1)	MA7	CA8	---	Address_8
B45	GND	GND	(GND)	
B46	MA5	CA6	I	Address_6
B47	MA3	CA4	I	Address_4
B48	MA1	CA2	I	Address_2
B49	MDQM0	XBEL/CA0	I	Lower Byte WrEnb/Address_0
B50	GND	GND	(GND)	

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Caution : CPU's Address Assignment depends on the Data Bus Width or Accessing way.
Connector :NDP100-002-BS (YAMAICHI ELECTRONICS CO., LTD.) , CPU board needs NDS100-002-BS.
(*1) S1R72V05 needs CA8, though V03 does'nt need it.