EPSON

Gate Array

S1L50000 Series
Design Guide

SEIKO EPSON CORPORATION

Rev. 3.3

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Chapter 1 Overview

The S1L50000 Series gate arrays are fabricated on a 0.35µm CMOS process with a sea-of-gates architecture.

1.1 Features

- Process 0.35µm CMOS, 2-, 3-, and 4-layer interconnects
- Maximum gate count 815,468 (2-input NAND gates)
- Operating speed
  - Internal logic gates: 140ps (3.3V, typical conditions)
    (2-input power NAND, F/O = 2, typical wire load capacitance)
  - Input buffers: 380ps (5.0V, typical conditions) using level shifter
    400ps (3.3V, typical conditions)
    (F/O = 2, typical wire load capacitance)
  - Output buffers: 2.12ns (5.0V, typical conditions) using level shifter
    2.02ns (3.3V, typical conditions) (C_L = 15pF)
- I/F levels TTL input, CMOS input/output, and LVTTL compatible
- Input modes TTL, CMOS, LVTTL, TTL Schmitt, CMOS Schmitt, LVTTL Schmitt, PCI, and fail-safe inputs
  With built-in pull-up and pull-down resistors
  (Each resistor has two resistance values.)
- Output modes Normal, 3-state, bi-directional, PCI, and fail-safe outputs
- Output drive I_{OL} = 0.1, 1, 3, 8, 12, 24mA selectable (at 5.0V)
  I_{OL} = 0.1, 1, 2, 6, 12mA selectable (at 3.3V)
- RAM 1-port asynchronous, 2-port asynchronous
  (If you require synchronous RAM, please contact our sales representative.)
- Dual power supply operation by built-in level shifter
  I/O buffers: 5.0V ±0.5V/3.3V ±0.3V mixable interface
  Internal logic: 3.3V ±0.3V operation
- Compatible with single power supply voltage (3.3V ±0.3V)

  If you require the following power supply specifications, please contact our sales representative:
  Single power supply: 2.5V ±0.25V or 2.0V ±0.2V
  Dual power supplies: 3.3V ±0.3V/2.5V ±0.25V or 3.3V ±0.3V/2.0V ±0.2V

1.2 Master Lineup

Fourteen different masters are available for the S1L50000 Series. Select the optimal master from Table 1-1 to suit the required gate count, number of input/output pins (including power supply pins) , and packages used.

Note that the figures provided in Table 1-1 do not account for RAM cell embedding. If you plan to embed RAM in the circuits, please refer to "Chapter 8 RAM Specifications" for estimates. Also note that the RAM cell configuration is fixed, and it may not be possible to apply the formula from the BC count.

Table 1-1 S1L50000 Series Masters

Master	Total BC Count*1	PAD Count*3	BC Count		Cell Utilization U: (%)*2		
			Row	Column	2-LM	3-LM	4-LM
S1L50062/50063/50064	5,760	48	144	40	50	88	95
S1L50122/50123/50124	11,948	56/64	206	58	50	88	95
S1L50282/50283/50284	28,710	88/104	319	90	50	88	95
S1L50552/50553/50554	55,500	124/144	444	125	47	85	95
S1L50752/50753/50754	75,774	144/168	519	146	47	85	95
S1L50992/50993/50994	99,198	168/192	594	167	47	85	95
S1L51252/51253/51254	125,772	188/216	669	188	45	80	95
S1L51772/51773/51774	177,062	224	794	223	45	75	95
S1L52502/52503/52504	250,160	264	944	265	45	75	95
S1L53352/53353/53354	335,858	308	1094	307	43	75	95
S1L54422/54423/54424	442,112	352	1256	352	40	70	90
S1L55062/55063/55064	506,688	376	1344	377	40	70	90
S1L56682/56683/56684	668,552	432	1544	433	40	70	90
S1L58152/58153/58154	815,468	480	1706	478	40	70	90

NOTE: *1: The usable BC (basic cell) count is calculated using the following formula from the total BC count (BC_G) and cell utilization (U) for each master.
Usable BC count (BC_A) estimation formula: $BC_A = BC_G \times U$
Add approximately 350 BCs to the estimation here for use with our recommended test circuit.
*2: Use the cell utilization values here strictly for reference purposes. They will vary depending not just on logic size, but on the numbers of signal lines and nodes per signal.
*3: Some masters are available with two different pad counts.

1.3 Electrical Characteristics and Specifications

1.3.1 Absolute Maximum Ratings

Table 1-2 Absolute Maximum Ratings (for dual power supplies)

(V_{SS} = 0V)

Parameter	Symbol	Limit	Unit
Power Supply Voltage*3	HV_{DD}	V_{SS} – 0.3 to 7.0	V
	LV_{DD}	V_{SS} – 0.3 to 4.0	V
Input Voltage*1	HV_I	V_{SS} – 0.3 to HV_{DD} + 0.5	V
	LV_I	V_{SS} – 0.3 to LV_{DD} + 0.5	V
Output Voltage*1	HV_O	V_{SS} – 0.3 to HV_{DD} + 0.5	V
	LV_O	V_{SS} – 0.3 to LV_{DD} + 0.5	V
Output Current/Pin	I_{OUT}	±30 (±50*2)	mA
Storage Temperature	T_{stg}	-65 to +150	°C

NOTE: *1: For N-channel open drains, input buffers prefixed with LID or HID, and fail-safe buffers, the maximum allowable voltage is 7.0V.
*2: Applicable to buffers with 24mA output current.
*3: $HV_{DD} \geq LV_{DD}$ must be met.

Table 1-3 Absolute Maximum Ratings (for single power supply)

(V_{SS} = 0V)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{DD}	V_{SS} – 0.3 to 4.0	V
Input Voltage*1	V_I	V_{SS} – 0.3 to V_{DD} + 0.5	V
Output Voltage*1	V_O	V_{SS} – 0.3 to V_{DD} + 0.5	V
Output Current/Pin	I_{OUT}	±30	mA
Storage Temperature	T_{stg}	-65 to +150	°C

NOTE: *1: For N-channel open drains, input buffers prefixed with ID, and fail-safe buffers, the maximum allowable voltage is 7.0V.

1.3.2 Recommended Operating Conditions

Table 1-4 Recommended Operating Conditions
(for dual power supply operation with HV_{DD} = 5.0V, LV_{DD} = 3.3V)

(V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (High)	HV_{DD}	4.5	5.0	5.5	V
Power Supply Voltage (Low)	LV_{DD}	3.0	3.3	3.6	V
Input Voltage*1	HV_I	-0.3	—	HV_{DD} + 0.3	V
	LV_I	-0.3	—	LV_{DD} + 0.3	V
Ambient Temperature*2	T_a	-40	25	85	°C
Normal Input Rising Time*3	t_{r1}	—	—	50	ns
Normal Input Falling Time*3	t_{f1}	—	—	50	ns
Schmitt Input Rising Time*3	t_{r2}	—	—	5	ms
Schmitt Input Falling Time*3	t_{f2}	—	—	5	ms

NOTE: *1: For N-channel open drains, input buffers prefixed with LID, the maximum allowable input voltage is 5.8V. For fail-safe buffers, the maximum allowable input voltage is 5.8V. However, do not apply an external voltage exceeding the output voltage when using high level output.
*2: Temperature range recommended when T_j = -40 to +125°C
*3: Period during which the power supply voltage changes by 10 to 90%

Table 1-5 Recommended Operating Conditions
(for single power supply operation with V_{DD} = 3.3V)

(V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Input Voltage*1	V_I	-0.3	—	V_{DD} + 0.3	V
Ambient Temperature*2	T_a	-40	25	85	°C
Normal Input Rising Time*3	t_{r1}	—	—	50	ns
Normal Input Falling Time*3	t_{f1}	—	—	50	ns
Schmitt Input Rising Time*3	t_{r2}	—	—	5	ms
Schmitt Input Falling Time*3	t_{f2}	—	—	5	ms

NOTE: *1: For N-channel open drains, input buffers prefixed with LID, the maximum allowable input voltage is 5.8V. For fail-safe buffers, the maximum allowable input voltage is 5.8V. However, do not apply an external voltage exceeding the output voltage when using high level output.
*2: Temperature range recommended when T_j = -40 to +125°C
*3: Period during which the power supply voltage changes by 10 to 90%

1.3.3 Electrical Characteristics

Table 1-6 Electrical Characteristics

(HV_{DD} = 5.0V ±0.5V, V_{SS} = 0V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-1	—	1	µA
Off State Leakage Current	I_{OZ}	—		-1	—	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1mA (Type S), -1mA (Type M) -3mA (Type 1), -8mA (Type 2) -12mA (Type 3, Type 4) HV_{DD} = Min.		HV_{DD} -0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1mA (Type S), 1mA (Type M) 3mA (Type 1), 8mA (Type 2) 12mA (Type 3), 24mA (Type 4) HV_{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V_{IH1}	CMOS level, HV_{DD} = Max.		3.5	—	HV_{DD} +0.3	V
Low Level Input Voltage	V_{IL1}	CMOS level, HV_{DD} = Min.		-0.3	—	1.0	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		2.0	—	4.0	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.8	—	3.1	V
Hysteresis Voltage	ΔV	CMOS Schmitt		0.3	—	-	V
High Level Input Voltage	V_{IH2}	TTL level, HV_{DD} = Max.		2.0	—	HV_{DD} +0.3	V
Low Level Input Voltage	V_{IL2}	TTL level, HV_{DD} = Min.		-0.3	—	0.8	V
High Level Input Voltage	V_{T2+}	TTL Schmitt		1.2	—	2.4	V
Low Level Input Voltage	V_{T2-}	TTL Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H2}	TTL Schmitt		0.1	—	-	V
High Level Input Voltage*1	V_{IH3}	PCI level, HV_{DD} = Max.		2.0	—	HV_{DD} +0.3	V
Low Level Input Voltage*1	V_{IL3}	PCI level, HV_{DD} = Min.		-0.3	—	0.8	V
Pull-up Resistor	P_{PU}	V_I = 0 V	Type 1	30	60	144	kΩ
			Type 2	60	120	288	kΩ
Pull-down Resistor	P_{PD}	V_I = HV_{DD}	Type 1	30	60	144	kΩ
			Type 2	60	120	288	kΩ
High Level Output Current*1	I_{OH3}	PCI V_{OH} = 1.4V, HV_{DD} = Min. V_{OH} = 3.1V, HV_{DD} = Max.		-44 —	— —	— -142	mA
Low Level Output Current*1	I_{OL3}	PCI V_{OL} = 2.20V, HV_{DD} = Min. V_{OL} = 0.71V, HV_{DD} = Max.		95 —	— —	— 206	mA
High Level Bus Hold Current	I_{BHH}	Bus hold, V_{IN} = 2.0V, HV_{DD} = Min.		—	—	-80	µA
Low Level Bus Hold Current	I_{BHL}	Bus hold, V_{IN} = 0.8V, HV_{DD} = Min.		—	—	33	µA
High Level Overdrive Current	I_{BHHO}	To flip bus hold V_{IN} = 0.8V HV_{DD} = Max.		-550	—	—	µA
Low Level Overdrive Current	I_{BHLO}	To flip bus hold V_{IN} = 2.0 V HV_{DD} = Max.		330	—	—	µA
Input Pin Capacitance	C_I	f = 1MHz, HV_{DD} = 0V		—	—	10	pF
Output Pin Capacitance	C_O	f = 1MHz, HV_{DD} = 0V		—	—	10	pF
IO Pin Capacitance	C_{IO}	f = 1MHz, HV_{DD} = 0V		—	—	10	pF

NOTE: *1: Complies with the PCI standard.

Table 1-7 Electrical Characteristics

(V_{DD} or LV_{DD} = 3.3 ±0.3V, V_{SS} = 0V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-1	—	1	µA
Off State Leakage Current	I_{OZ}	—		-1	—	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1mA (Type S), -1mA (Type M) -2mA (Type 1), -6mA (Type 2) -12mA (Type 3) V_{DD} = Min.		V_{DD} -0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1mA (Type S), 1mA (Type M) 2mA (Type 1), 6mA (Type 2) 12mA (Type 3) V_{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V_{IH2}	LVTTL Level, V_{DD} = Max.		2.0	—	V_{DD} +0.3	V
Low Level Input Voltage	V_{IL2}	LVTTL Level, V_{DD} = Min.		-0.3	—	0.8	V
High Level Input Voltage	V_{T2+}	LVTTL Schmitt		1.1	—	2.4	V
Low Level Input Voltage	V_{T2-}	LVTTL Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H2}	LVTTL Schmitt		0.1	—	—	V
High Level Input Voltage*1	V_{IH3}	PCI Level, V_{DD} = Max.		1.8	—	V_{DD} +0.3	V
Low Level Input Voltage*1	V_{IL3}	PCI Level, V_{DD} = Min.		-0.3	—	0.9	V
Pull-Up Resistor	P_{PU}	V_I = 0V	Type 1	20	50	120	kΩ
			Type 2	40	100	240	kΩ
Pull-Down Resistor	P_{PD}	V_I = HV_{DD}	Type 1	20	50	120	kΩ
			Type 2	40	100	240	kΩ
High Level Output Current*1	I_{OH3}	PCI V_{OH} = 0.90V, V_{DD} = Min. V_{OH} = 2.52V, V_{DD} = Max.		-36 —	— —	— -115	mA
Low Level Output Current*1	I_{OL3}	PCI V_{OL} = 1.80V, V_{DD} = Min. V_{OL} = 0.65V, V_{DD} = Max.		48 —	— —	— 137	mA
High Level Bus Hold Current	I_{BHH}	Bus hold, V_{IN} = 2.0V, V_{DD} = Min.		—	—	-20	µA
Low Level Bus Hold Current	I_{BHL}	Bus hold, V_{IN} = 0.8V, V_{DD} = Min.		—	—	17	µA
High Level Overdrive Current	I_{BHHO}	To flip bus hold V_{IN} = 0.8V V_{DD} = Max.		-350	—	—	µA
Low Level Overdrive Current	I_{BHLO}	To flip bus hold V_{IN} = 2.0V V_{DD} = Max.		210	—	—	µA
Input Pin Capacitance	C_I	f = 1MHz, V_{DD} = 0V		—	—	10	pF
Output Pin Capacitance	C_O	f = 1MHz, V_{DD} = 0V		—	—	10	pF
IO Pin Capacitance	C_{IO}	f = 1MHz, V_{DD} = 0V		—	—	10	pF

NOTE: *1: Complies with the PCI standard.

1.3.4 Overshoot and Undershoot

Depending on usage, if the overshoot or undershoot in input waveforms to an input buffer or bi-directional buffer exceeds the maximum input voltage under the recommended operating conditions in Tables 1-4 and 1-5, overshoot and undershoot are specified within the time periods shown below.

(1) Voltage and time for which overshoot/undershoot is allowed when HV_{DD} = 5.0V ±0.5V

Overshoot maximum peak voltage: V_{DD} + 1.5V[*1]

Overshoot maximum time[*2]: 50ns

Undershoot minimum peak voltage: V_{SS} − 1.5V

Undershoot maximum time[*2]: 50ns

NOTE: *1: For N-channel open drain bi-directional buffers, input buffers with cell names prefixed with HID or LID, and fail-safe buffers, the maximum allowable voltage is 7.0V.
*2: Time refers to the time for which the input voltage exceeds V_{DD} or is below V_{SS}. In the cases marked *1 above, however, it will be the time above 5.8V.

(2) Voltage and time for which overshoot/undershoot is allowed when HV_{DD} or V_{DD} = 3.3V ±0.3V

Overshoot maximum peak voltage: V_{DD} + 1.0V[*1]

Overshoot maximum time[*2]: 50ns

Undershoot minimum peak voltage: V_{SS} − 1.0V

Undershoot maximum time[*2]: 50ns

NOTE: *1: For N-channel open drain bi-directional buffers, input buffers with cell names prefixed with ID, and fail-safe buffers, the maximum allowable voltage is 7.0V.
*2: Time refers to the time for which the input voltage exceeds V_{DD} or is below V_{SS}. In the cases marked *1 above, however, it will be the time above 5.8V.

(Supplement)
In the case of waveforms with large overshoot or undershoot, confirm that the reflected wave meets the V_{IH}/V_{IL} standards for the input. Even if the earlier mentioned standards are met, malfunctions may occur if the reflected wave is within a range that does not meet V_{IH}/V_{IL} standards. (Ideally, the input waveform should be checked directly using an oscilloscope or similar device.)

1.4 Static Current

Table 1-8 Static Current (with dual power supplies)

(Tj = 85°C)

Master	5.0V ±0.5V HI_{DDS} Max.	3.3V ±0.3V LI_{DDS} Max.*1	3.3V ±0.3V HI_{DDS} Max.*1	Unit
S1L50062/50063/50064 S1L50122/50123/50124	11	5	9	µA
S1L50282/50283/50284 S1L50552/50553/50554 S1L50752/50753/50754 S1L50992/50993/50994	30	35	25	µA
S1L51252/51253/51254 S1L51772/51773/51774 S1L52502/52503/52504	45	90	35	µA
S1L53352/53353/53354 S1L54422/54423/54424 S1L55062/55063/55064	65	170	50	µA
S1L56682/56683/56684 S1L58152/58153/58154	80	260	60	µA

NOTE: *1: HI_{DDS}: Static current between HV_{DD} and V_{SS}
LI_{DDS}: Static current between LV_{DD} and V_{SS}

Table 1-9 Static Current (with single power supply)

(Tj = 85°C)

Master	3.3V ±0.3V I_{DDS} Max.*1	Unit
S1L50062/50063/50064 S1L50122/50123/50124	5	µA
S1L50282/50283/50284 S1L50552/50553/50554 S1L50752/50753/50754 S1L50992/50993/50994	35	µA
S1L51252/51253/51254 S1L51772/51773/51774 S1L52502/52503/52504	90	µA
S1L53352/53353/53354 S1L54422/54423/54424 S1L55062/55063/55064	170	µA
S1L56682/56683/56684 S1L58152/58153/58154	260	µA

NOTE: *1: I_{DDS}: Static current between V_{DD} and V_{SS}

Use the following equation to obtain approximate static current when the temperature condition is other than Tj = 85°C. (The equation is applicable only when Tj = -40 to 85°C. When Tj = 125°C, apply temperature coefficient = 12. When Tj = 85°C to 125°C, contact our sale representative.)

I_{DDS} (Tj) = I_{DDS} (Tj = 85°C) × Temperature Coefficient

$$= I_{DDS}\,(Tj = 85°C) \times 10^{\frac{Tj-85}{60}}$$

(Example) When V_{DD} = 3.3V ±0.3V and Tj = 50°C, the approximate static current of S1L55062 is obtained as follows:

$$I_{DDS}\,(Tj = 50°C) = I_{DDS}\,(Tj = 85°C) \times 10^{\frac{50-85}{60}}$$

$$= 170 \times 0.261$$

$$= 44.37\ (\mu A)$$

When the device is operated with dual power supplies, the sum of static currents that flow at voltages used is the total static current (HI_{DDS} + LI_{DDS}).

1.5 Development Flow

Shown here are the development flow including the development start order and data submission from the customer, logic synthesis and placement and routing at Epson, and the flow from test manufacture to the start of mass production.

1.5.1 Development Flow Up to Sign-off

Figure 1-1 shows the development flow up to sign-off for an RTL interface.

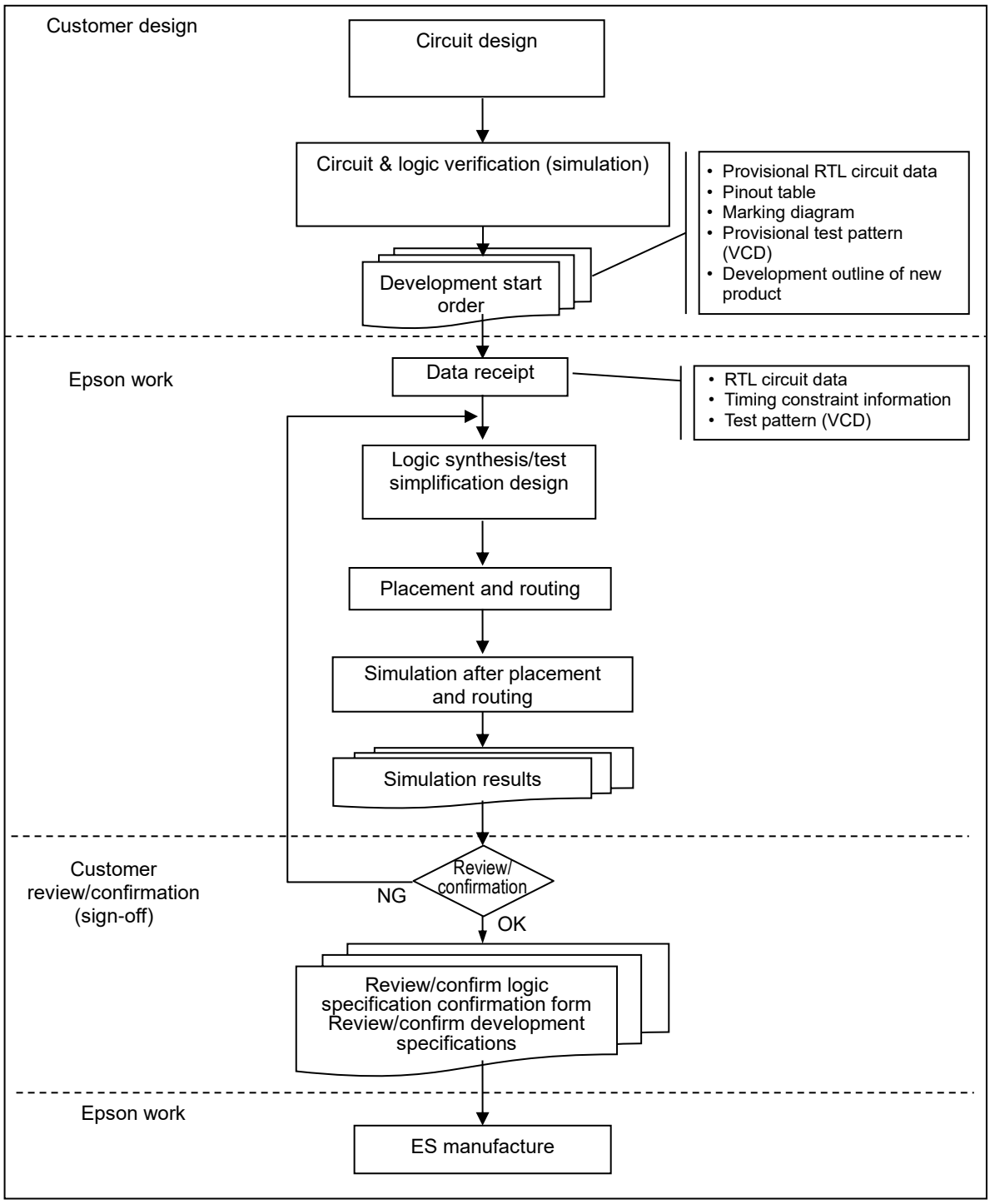


Figure 1-1 Development Flow Up to Sign-off

1.5.2 Logic Synthesis and Placement and Routing Workflow (Epson Work)

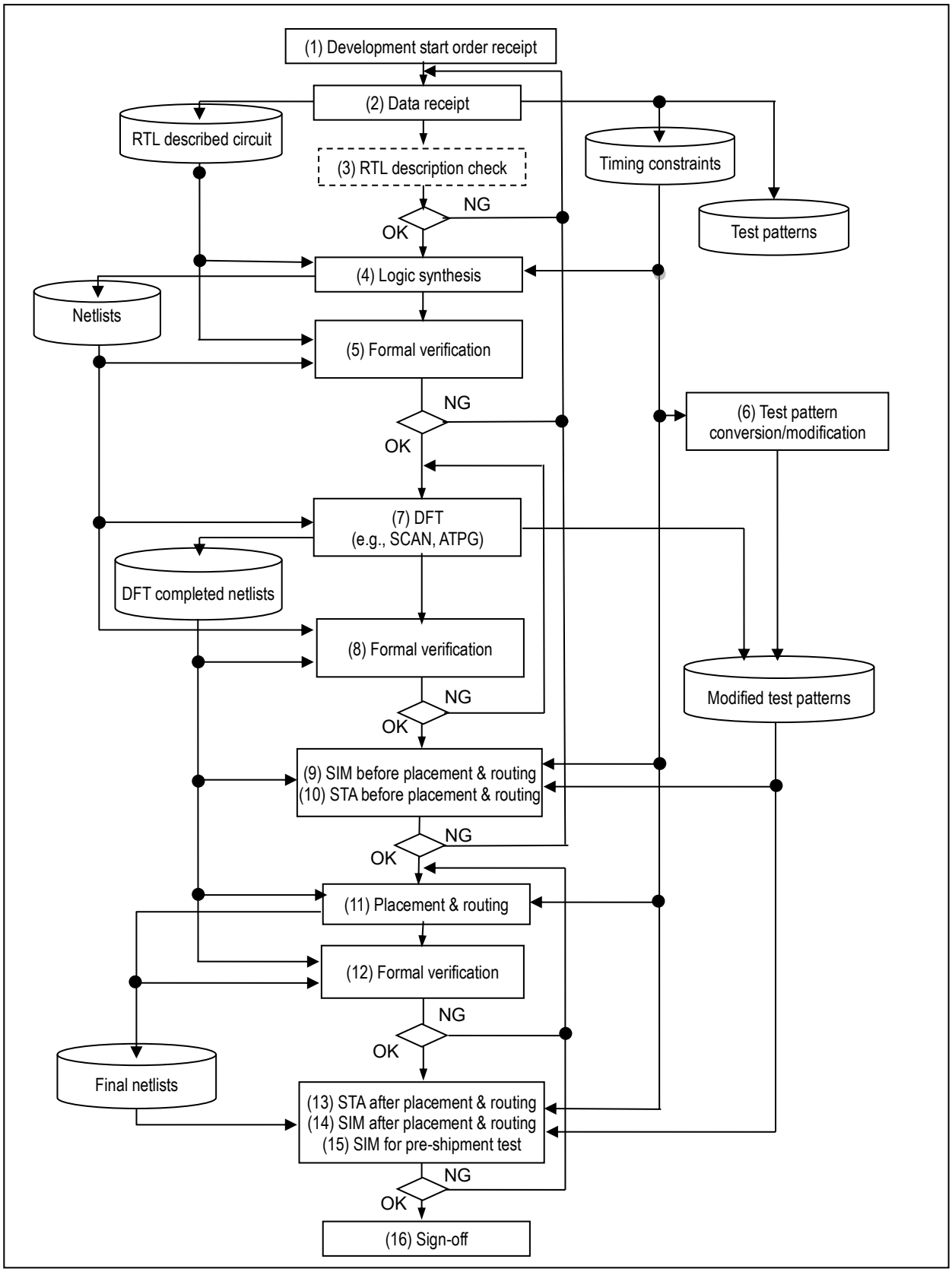


Figure 1-2 Logic Synthesis and Placement and Routing Workflow at Epson

Figure 1-2 shows the logic synthesis and placement and routing workflow from data receipt to sign-off. The individual tasks are outlined as follows.

(1) Development start order receipt

The Epson development start order form is sent by the customer to Epson or to a distributor. Design work commences at Epson once this is received. The customer should also send the following data together with the development start order:

① Provisional RTL circuit data (See "1.5.3 Submitting Provisional (Trial) Data.")

② Pinout table

③ Marking diagram (form created by Epson)

④ Provisional test pattern (VCD format)

⑤ Development outline of new product

(2) Data receipt

The customer should send the following data:

① Formal RTL circuit data

② Timing constraint information

③ Formal test pattern (VCD format)

(3) RTL description check

An RTL checker is used as necessary to check for issues such as syntax errors.

(4) Logic synthesis

Provisional logic is synthesized initially with minimal constraints to check the number of gates and analyze the clocks. If no issues are found, the actual logic is synthesized with the addition of timing constraints.

(5) Formal verification (equivalence check)

Formal verification (equivalence check) is performed between the customer's RTL description and the netlists following logical synthesis.

(6) Test pattern conversion

VCD (value change dump) test pattern files received from the customer are converted to Epson's proprietary APF (advanced press format) files (cycle-based, table format test patterns) .

(7) DFT (e.g., scan insertion, ATPG)

DFT (design for test: addition of dedicated test circuits to increase fault coverage) is performed and scan test circuits inserted. Test patterns are generated using automatic test pattern generation (ATPG). Please inform Epson about the target fault coverage at the start of development.

(8) Formal verification (equivalence check)

Formal verification is performed on the netlists before and after DFT.

(9) Simulation before placement and routing

Simulation is performed using the test patterns in (6) and (7) above together with virtual delay data to confirm that the required functions are achieved in the gate-level netlists. An analysis is conducted if any problems are identified in simulation results.

(10) STA before placement and routing

The timing is checked using STA (static timing analysis) based on the timing constraints received from the customer. If any clearly problematic timing errors are identified, the customer will be contacted and logic synthesis will be repeated.

(11) Placement and routing

Placement and routing is carried out using the data from (10) above. Delay time data is calculated after actual routing based on these results.

(12) Formal verification (equivalence check)

Netlists are formally verified before and after placement and routing.

(13) STA after placement and routing

The timing of the data after placement and routing is checked based on the delay time data after actual routing. If any clearly problematic timing errors are identified, adjustments will be made using ECO (local layout changes) or similar means.

(14) Simulation after placement and routing (real rate)

A simulation is performed using the data after placement and routing under the conditions using the actual IC. The results are returned to the customer for review/confirmation.

(15) Pre-shipment test simulation (test rate)

The test pattern timing conditions are modified for pre-shipment testing, then a simulation is performed using the data after placement and routing. The results are returned to the customer for review/confirmation. The customer should also confirm that the pre-shipment test conditions have been met.

<Sending simulation results>

The simulation results are sent in Epson's proprietary APF (advanced press format; *.sammax and *.sammin) . VCD (value change dump) waveform files can be sent, if requested.

<Sending comparison to simulation results>

The simulation results are compared against the expected values to output comparison files (*.exp_max and *.exp_min) . Comparison file outputs for minimum and maximum results (*.min_max) are also sent in the same way.

For an example of output, refer to "A1.1 Comparison File Example for Simulation Results and Expected Values."

<Sending timing error lists>

List (*.errmax and *.errmin) output will be sent if any timing errors occur during simulation.

For an explanation of timing error lists, refer to "A1.2 Timing Error List."

(16) Sign-off

An Epson form (logic specification confirmation form) will be sent to the customer. The customer should review the details; if no problems are found, the customer is requested to write in the confirmation results, sign and seal the form, and return it to Epson. Engineering sample (ES) manufacture will begin on receipt of this form.

1.5.3 Submitting Provisional (Trial) Data

The customer should submit provisional (trial) data before submitting formal RTL circuit data.

This provisional data is used in preparation work to ensure work proceeds smoothly following receipt of the formal data.

Please inform us when submitting provisional RTL circuit data if the timing constraints are stringent.

(1) Gate count estimate

The provisional RTL circuit data received from the customer can be used to estimate the approximate gate count.

(2) Provisional RTL data checking

The provisional RTL circuit data received from the customer is used for logic synthesis. This enables syntax and post-synthesis issues to be identified in advance. The customer will be notified of any locations where issues arose in the check.

The netlists after logic synthesis will be formally verified (equivalence checked) against the provisional RTL data. The customer will be notified if any logical inconsistencies are found.

(3) Constraint condition setting in logic synthesis

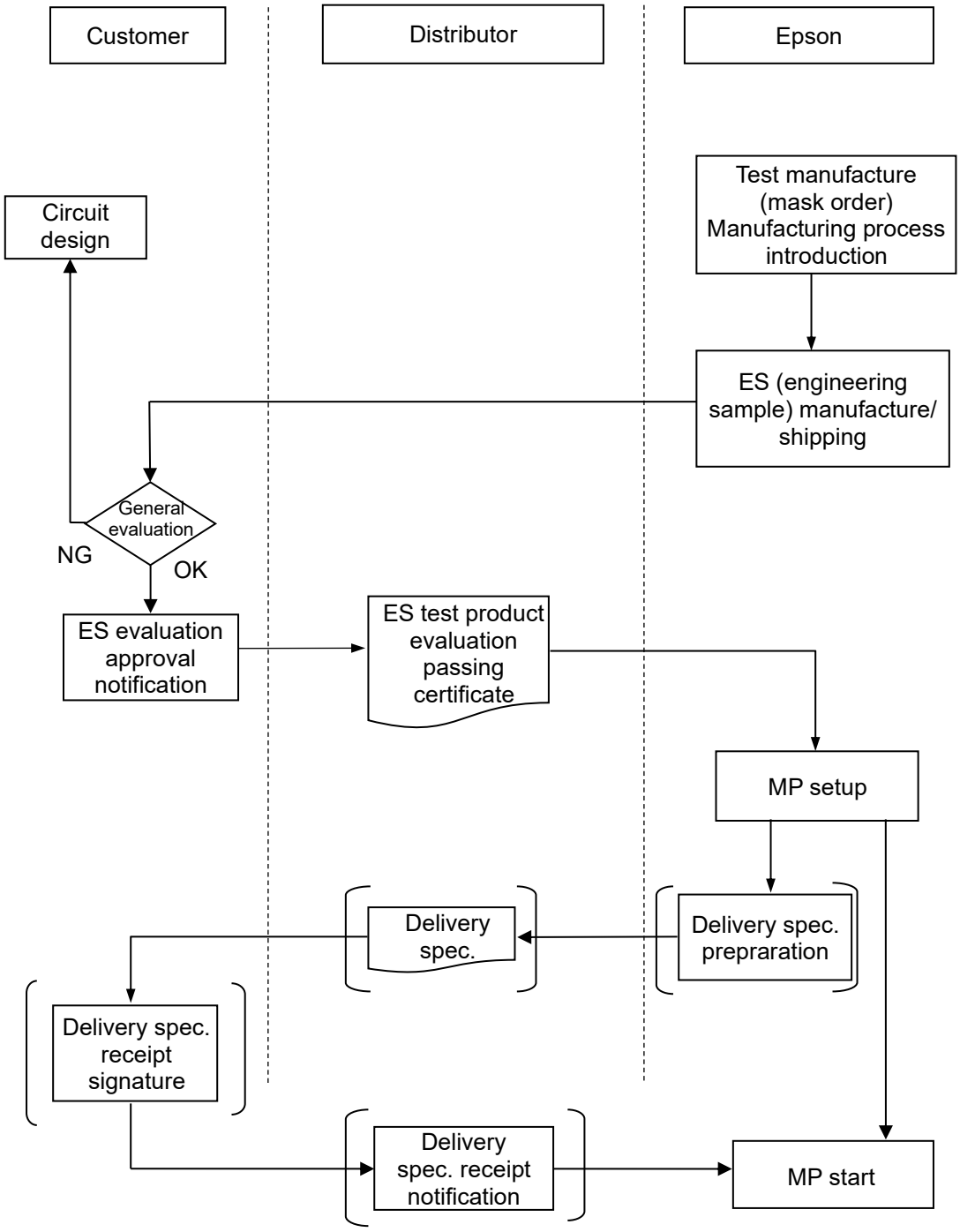
Logic synthesis is performed assuming minimal constraint conditions. Logic synthesis constraint conditions can be adjusted in advance if timing constraint information is provided by the customer. Static timing analysis (STA) constraint conditions can also be created.

(4) Function checking

If the customer provides provisional test patterns, Epson will be able to perform function checking by checking conversion to APF patterns, checking test pattern consistency, and gate level simulations.

1.5.4 Flow from Test Manufacture to Mass Production Setup

Figure 1-3 shows the flow from test manufacture at Epson to mass production setup.



The items in () are performed only when requested by the customer.

Figure 1-3 Flow from Test Manufacture to Mass Production Setup

Chapter 2 RTL Design Restrictions and Limitations (Verilog-HDL)

This chapter describes various precautions regarding RTL design by the customer prior to logic synthesis at Epson. The explanation here assumes use of the Verilog-HD language. Customers using VHDL should refer to "A2. RTL Design Restrictions and Limitations (VHDL)." Inform our sales representative that the design uses VHDL when submitting the development start order.

2.1 Basic Configuration

2.1.1 Provision of RTL Data Allowing Logic Synthesis

The RTL data submitted must include only descriptions that allow logic synthesis. Logic synthesis will not be possible if behavioral-level logic is included here. Provided that it allows logic synthesis, the data may be split into multiple files.

2.1.2 Library Cell Usage

Please inform us of the names of the modules within the RTL calling up Epson library cells and the names of those library cells. Settings will be configured to ensure library cells are not deleted during logic synthesis.

2.1.3 ifdef and parameter

Please inform us if it is necessary to set values from outside the RTL or from other files for ifdef and parameter statements.

2.2 Pin Name Restrictions

The names of external and internal pins are subject to restrictions. We recommend that the customer abide by these restrictions. Please note that names that do not comply with the restrictions may be changed unexpectedly during logic synthesis.

2.2.1 External Pin Name Restrictions

External pin names are subject to the following restrictions:

(1) Describe entirely in upper case.

(2) Only alphanumeric characters and the underscore ("_") character can be used.
However, the first character must be a letter of the alphabet.

(3) Square brackets, "[" and "]" cannot be used. Bus descriptions are also prohibited.

(4) The underscore ("_") character must not be used in succession.

(5) Names must be two to 32 characters long.

2.2.2 Internal Pin Name Restrictions

(1) Names may include both upper and lower case characters. However, identical names cannot be used if they only differ by case.
Example: “ABC” and “Abc” cannot be used at the same time.

(2) Only alphanumeric characters, the underscore (“_”) character, and square brackets “[” and “]” for bus descriptions can be used.

(3) Names must be two to 32 characters long.

2.2.3 Verilog Reserved Words

The following text strings are Verilog reserved words and cannot be used as user-defined names:

always	and	assign	begin	buf	bufif0	bufif1
case	casex	casez	cmos	deassign	default	defparam
disable	edge	else	end	endcase	endmodule	endfunction
endprimitive	endspecify	endtable	endtask	event	for	force
forever	fork	function	highz0	highz1	if	ifnone
initial	inout	input	integer	join	large	macromodule
medium	module	nand	negedge	nmos	nor	not
notif0	notif1	or	output	parameter	pmos	posedge
primitive	pull0	pull1	pullup	pulldown	rcmos	real
realtime	reg	release	repeat	rnmos	rpmos	rtranif0
rtranif1	scalared	small	specify	specparam	strong0	strong1
supply0	supply1	table	task	time	tran	tranif0
tranif1	tri	tri0	triand	trior	trireg	vectored
wait	wand	weak0	weak1	while	wire	wor
xnor	xor					

2.3 Submitting Timing Constraint Information

The customer should send timing constraint information related to clocks, input delays, and external delays at the same time as the RTL data. This information will be used for inclusion in timing constraints created for logic synthesis and STA.

2.3.1 Clock Information

(1) External clocks

Please specify the following details for all external clocks:

① Pin name

② Clock reference cycle

③ Delay from reference cycle start to clock rising edge and falling edge

④ Duty and its variation

⑤ Whether or not clock jitter is present

⑥ Whether or not skew adjustment is required

⑦ Purpose (e.g., main or test)

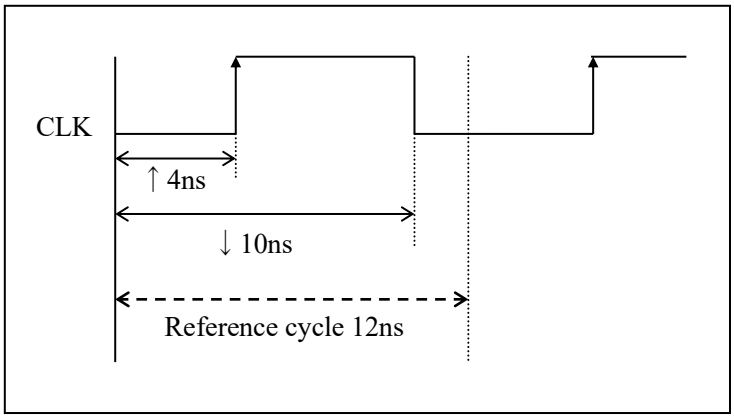


Figure 2-1 External Clock Waveform

For example, in the case shown in Figure 2-1, the external clock pin name is CLK, the clock reference cycle is 12ns, the rising edge delay is 4ns, the falling edge delay is 10ns, and duty is 50 ±0%.

(2) Internally generated clocks

This refers to clocks generated within the circuits by methods such as PLL or division. Please specify the following details for all internally generated clocks:

① Internally generated clock signal name and name of module in which it is generated

② Master clock signal name (or pin name if it is an external clock)

③ Relationship with master clock (division or multiplication rate)

④ Whether or not skew adjustment is required

Figure 2-2 shows an example RTL description generating an internal clock DCLK in which the master clock CLK is divided in two using D-FF. Following logic synthesis, this produces a circuit like that shown in Figure 2-3. Note here that CLK and DCLK will be clocks with different timings. This is because skew corresponding to the propagation delay occurs between CLK and the FF output pin. See Figure 2-4.

```
always @(posedge CLK or negedge RST)
begin
   if(!RST)
      Q <= 1'b0;
   else
      Q <= ~Q;
end

assign DCLK = Q;

always @(posedge DCLK or negedge RST)
                              .
                              .
```

Figure 2-2 Example Description for Internal Clock Generation Using Division

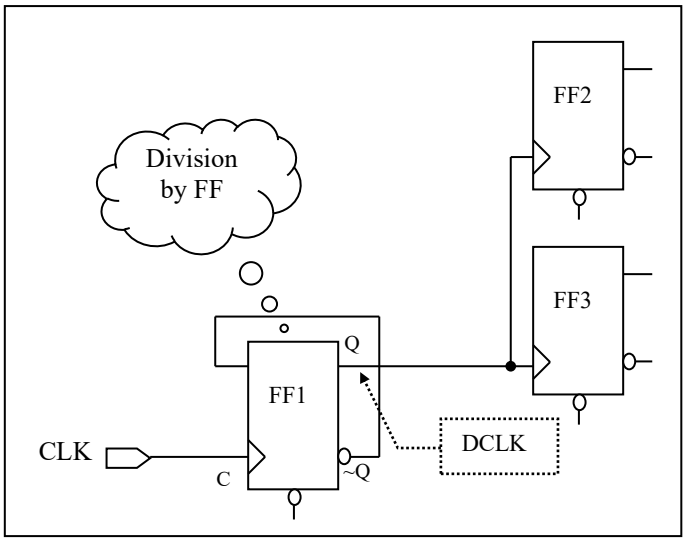


Figure 2-3 Example Circuit Synthesized from Figure 2-2

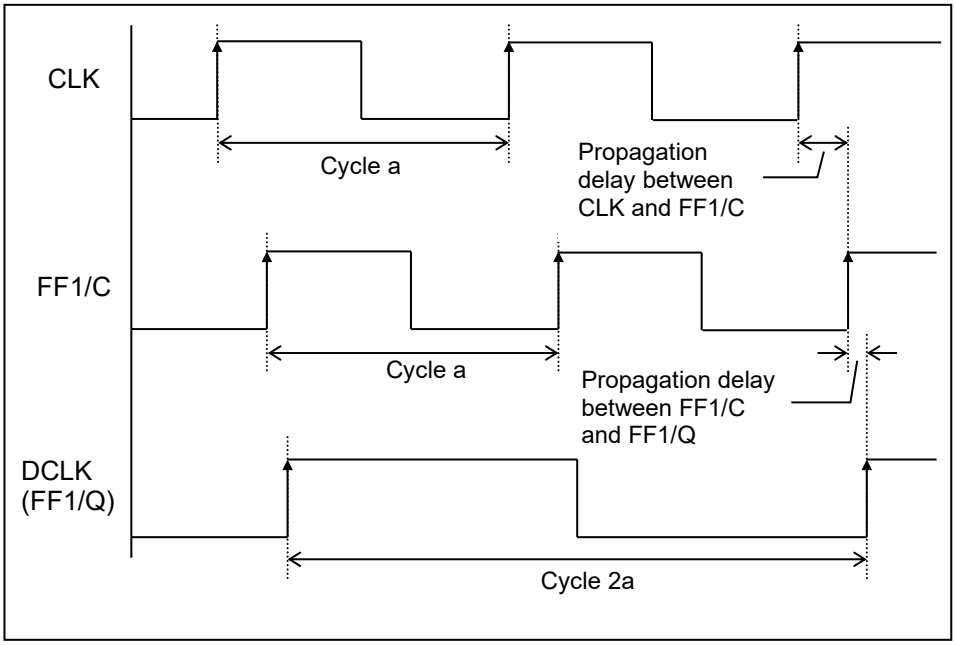


Figure 2-4 Waveform for Circuit in Figure 2-3

(3) Combining multiple clocks

Avoid generating pulses using circuits consisting of multiple clocks. The skew from each clock may result in unpredictable pulses.

(4) Data paths between registers operating using different clocks

The presence of data paths between registers operating using different clocks will make it difficult to guarantee their timing. The design should ensure that data can be received asynchronously. Likewise, in cases in which the edge differs even with the same clock, please specify whether it is acceptable to treat these registers as using different clocks.

2.3.2 External Pin Timing Constraints

(1) External input timing

Please specify the setup time and hold time with respect to the reference clock for external input pins.

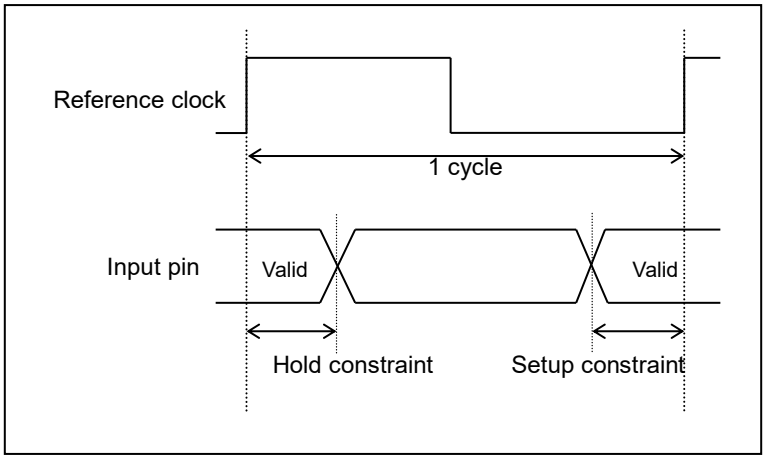


Figure 2-5 External Input Timing

(2) External output timing

Set the output delay with respect to the defined clock for external output pins. Please specify maximum and minimum delays with respect to the reference clock. Specify virtual clock constraints if the circuit lacks a reference clock.

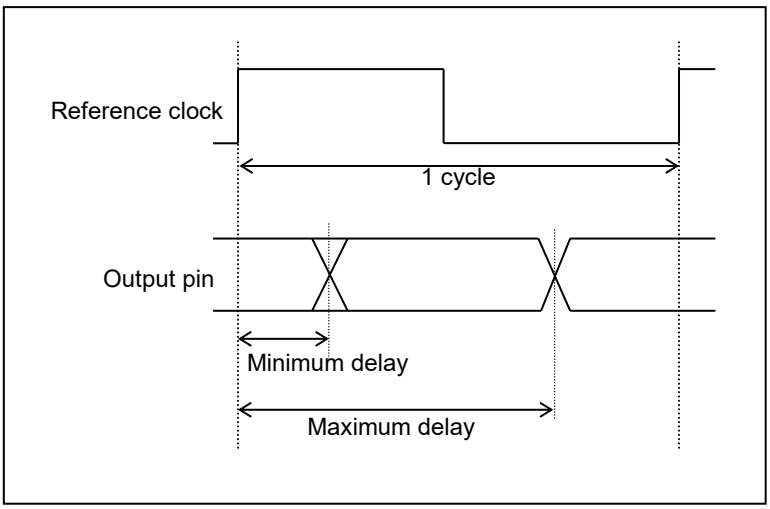


Figure 2-6 External Output Timing

(3) Multi-cycle paths

Figure 2-7 shows an example of a path through a large-scale circuit such as a multiplier. If multiple cycles are required (or the necessity of multiple cycles is allowed) for timing between FF1/Q and FF2/D, specify multi-cycle paths for paths between FF1/Q and FF2/D.

Specify the paths requiring multiple cycles for transferring data and the number of cycles.

For example, if two cycles are required for data propagation on the path between FF1/Q and FF2/D, specify a two-cycle multi-cycle path between FF1/Q and FF2/D, as shown in Figure 2-8.

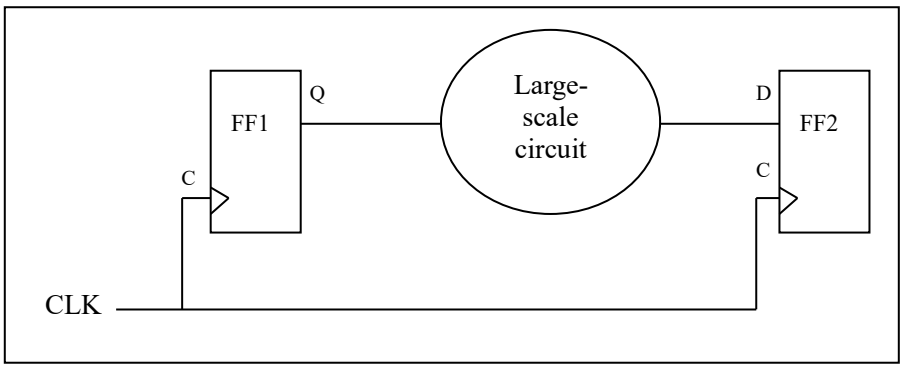


Figure 2-7 Example Path through Large-scale Circuit

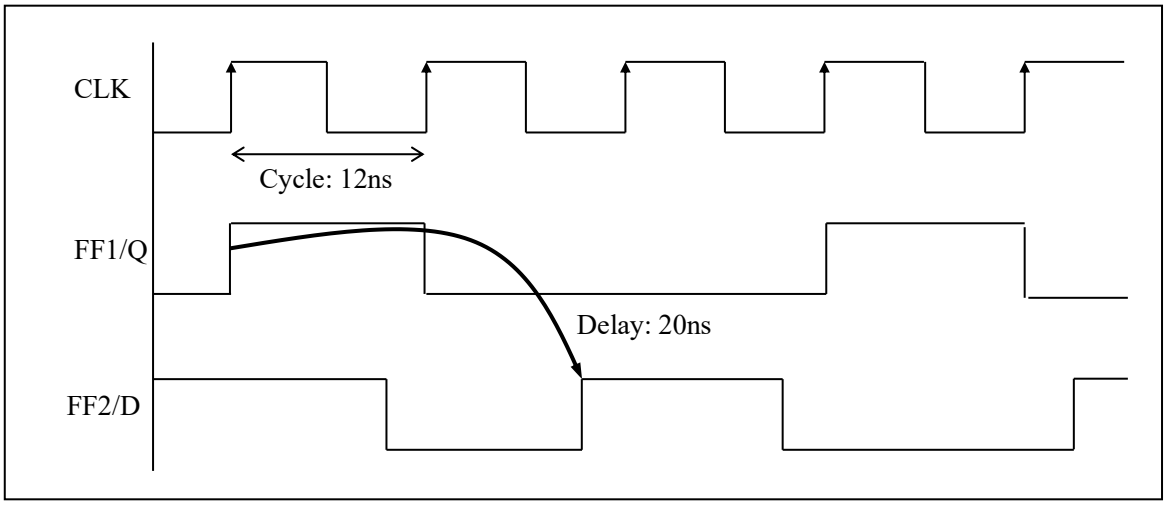


Figure 2-8 Multi-cycle Path

(4) False paths

Where possible, specify paths that are logically infeasible or fall outside specifications. False paths will be excluded from optimization. For example, the path between B and X in Figure 2-9 is logically infeasible, and therefore constitutes a false path.

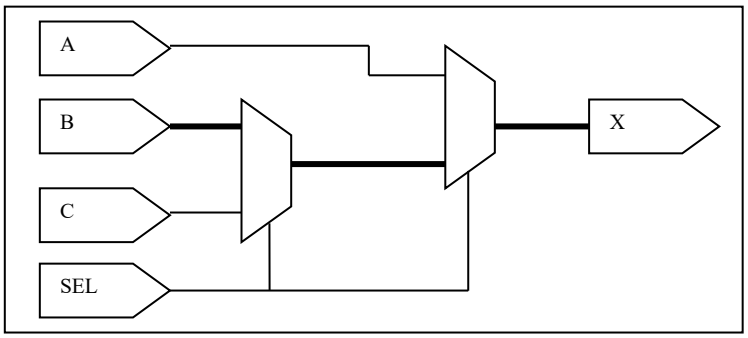


Figure 2-9 False Path

(5) Clock gating

Ideally, clock gating used to reduce power consumption should be performed at higher levels.

Please specify the locations where clock gating is performed. It may be necessary to adjust skew when constructing the clock tree. Additionally, specify if latch-based clock gating cells are used.

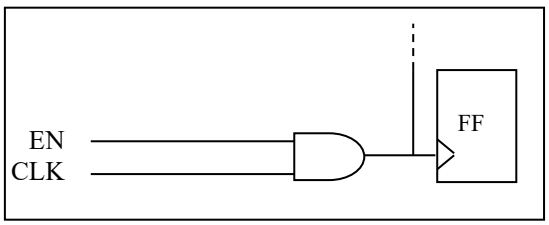


Figure 2-10 Clock Gating Example

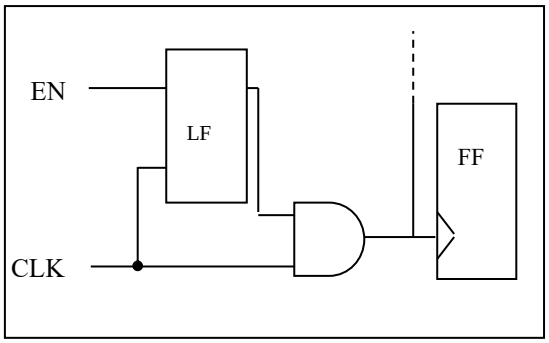


Figure 2-11 Latch-based Clock Gating Example

(6) Precautions for simulations using RTL with clock gating

In RTL simulations, clocks gated as shown in Figure 2-12 will be treated as asynchronous to the clock before gating. If a clock is input with zero delay for both two-stage asynchronous FF, the simulator will determine the one processed first. To avoid this, add a delay description within the RTL to ensure processing is carried out in the desired order. Delay descriptions within the RTL will be ignored during logical synthesis.

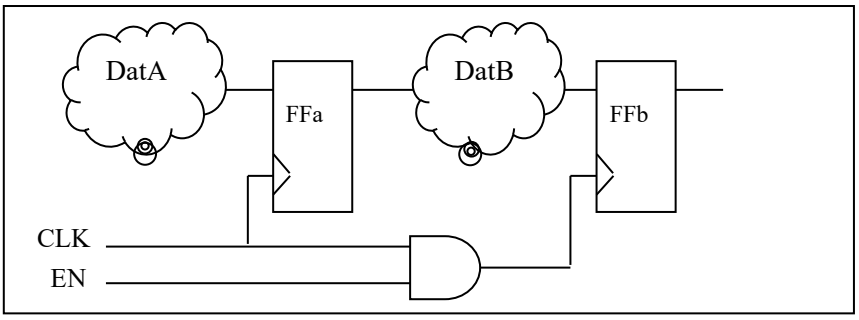


Figure 2-12 Example of Connection with Gated Clock

```
parameter DELAY = 10;
.......
always @(posedge CLK ) begin
      FFa <=   #(DELAY)   DatA;
end
assign ENCLK = CLK & EN;
always @(posedge ENCLK ) begin
      FFb <=   DatB;
end
```

Figure 2-13 Additional Delay Description

(7) Automatic clock gating cell insertion during logical synthesis

Latch-based clock gating cells can be automatically inserted during logical synthesis at Epson to reduce power consumption and gate size.

However, note that adjustment may take several days if timing constraints are stringent, due to the resulting increase in clock skew.

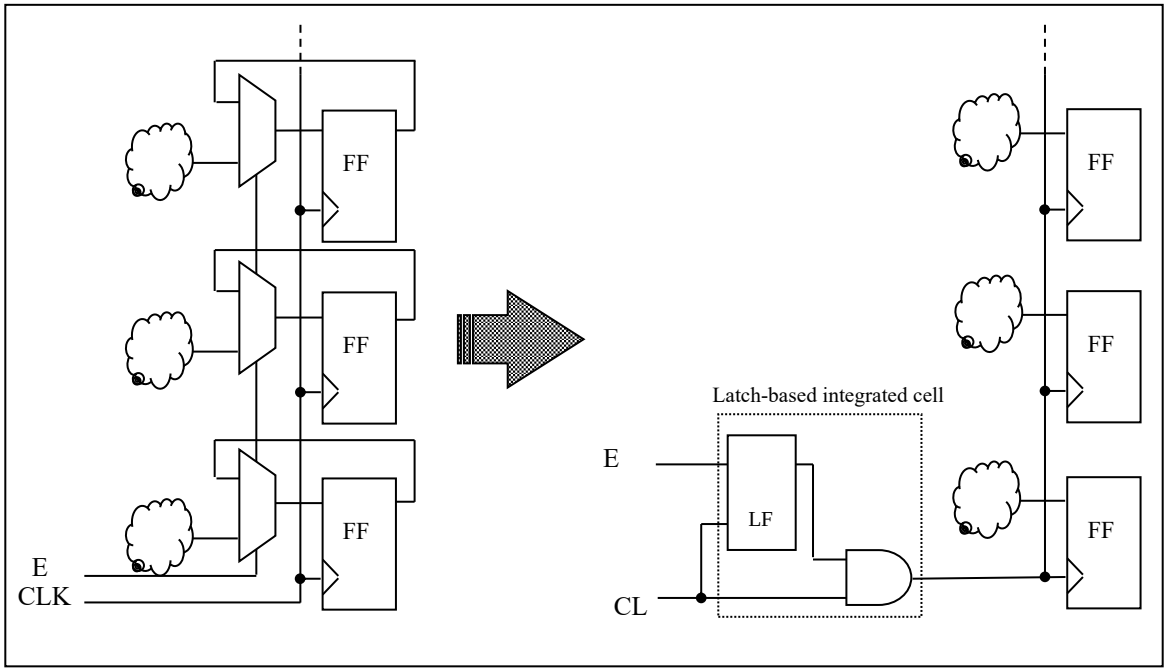


Figure 2-14 Example of Automatic Clock Gating Cell Insertion

(8) Set and reset signals

Please specify whether there are any flip-flops that have both asynchronous set and reset pins as shown in Figure 2-15. The recovery time and removal time cannot be analyzed between setting and resetting flip-flops that have both asynchronous set and reset pins. Similarly, setting and resetting cannot be analyzed for cells with no clock pins.

```
always @(posedge CLK or negedge SET or negedge RST) begin
   if (!SET)
      Q <= 1'b1;
   else if (!RST)
      Q <= 1'b0;
   else
      Q <= D;
end
```

Figure 2-15 Example Description for Flip-flop with Both Set and Reset Pins

2.4 I/O Buffer Insertion

(1) Epson will insert I/O buffers depending on the buffer types in the pinout table sent by the customer.

For information on buffer types and configurations, refer to "Chapter 6 Types of I/O Buffers and Notes on Use."

(2) I/O buffers can be inserted safely and easily by changing the top module from an RTL module to a gate module. The gate top module will be created by Epson. The customer only needs to include descriptions related to input and output in the RTL top module. More specifically, uni-directional ports should be connected only to lower modules on a one-to-one basis. The descriptions for bi-directional ports should include descriptions for bi-directional signals within the top module by extracting input signal ports, output signal ports, and enable signal ports from the lower level.

```
module TOP ( IN1, OUT1, BID1);
   input IN1;
   output OUT1;
   inout BID1;
   assign BID1 = (en) ? 1'bz : bid1_out;
   CORE U_CORE( .in1(IN1),
   .out1(OUT1), .bid1_in(BID1),
   .bid1_out(bid1_out), .en(en) );
endmodule
```

Figure 2-16 Top Module RTL Example

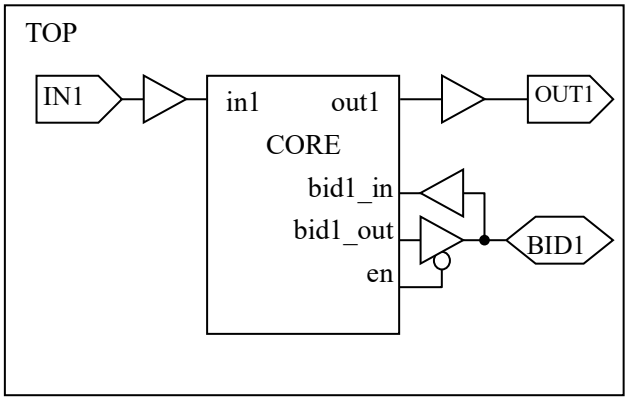


Figure 2-17 Top Module Schematic

2.5 RAM Description

(1) Please check the RAM specifications if RAM is installed. For more information on specifications, refer to "Chapter 8 RAM Specifications."

(2) Epson will provide RAM libraries. Please indicate the required RAM size and quantity in the development start order. Note that it may take several days to provide RAM (model) libraries.

(3) If RAM is described by the customer, please notify us of the model module name.

2.6 Oscillator Cell Description

(1) If oscillator cells are installed, refer to "5.1 Oscillator Circuits" for details on oscillator cells.

(2) Oscillator cells should be instantiated in the RTL description.

(3) If logic synthesis is performed by the customer, add the "dont_touch" attribute using the "set_dont_touch" command to the input and output nets to prevent buffers from being inserted into the nets connecting the external pins of the oscillator cells.

Chapter 3 Test Circuit Design Restrictions and Limitations

Epson carries out test simplification design and test circuit insertion as test circuit design recommendations. For information on the insertion procedure, refer to "1.5 Development Flow."

3.1 Recommended AC/DC Test Circuit Insertion

Epson provides recommended test circuits to ensure efficient pre-shipment testing of AC and DC circuits. These will be inserted into the customer's circuits.

3.1.1 Using Recommended Test Circuits and I/O Buffers with Test Circuits

Epson-recommended AC and DC test circuits will be inserted by Epson into the circuits sent by the customer. I/O buffers with test circuits will be selected to configure the recommended test circuits.

Please provide at least one input pin for use as a dedicated AC/DC test pin.

3.1.2 Cell Names for Output Buffers with Test Circuits and Bi-directional Buffers

The cell names for output buffers with test circuits selected for configuring recommended test circuits will be "O***T" or "TB***T", and the cell names for bi-directional buffers will be "B****T", all suffixed with "T".

3.1.3 Test Circuit Insertion Designed by Customer

Please indicate in the development start order if the test circuits are designed by the customer, if Epson-recommended test circuits cannot be used for reasons involving the customer's circuit configuration, or if an output buffer with test function cannot be used.

3.2 Scan Circuit Insertion

Please indicate in the development start order whether scan circuits are to be inserted. Scan circuits will be inserted by Epson.

If so, provide two dedicated scan test pins for use as circuit input pins.

3.2.1 Scan Circuits

Scan insertion by Epson involves replacing all registers (D-FF and JK-FF) existing in the design created with scan-type registers, then configuring the scan paths (full-scan design) . Using auto test pattern generation (ATPG) with this design generates test patterns with high fault coverage.

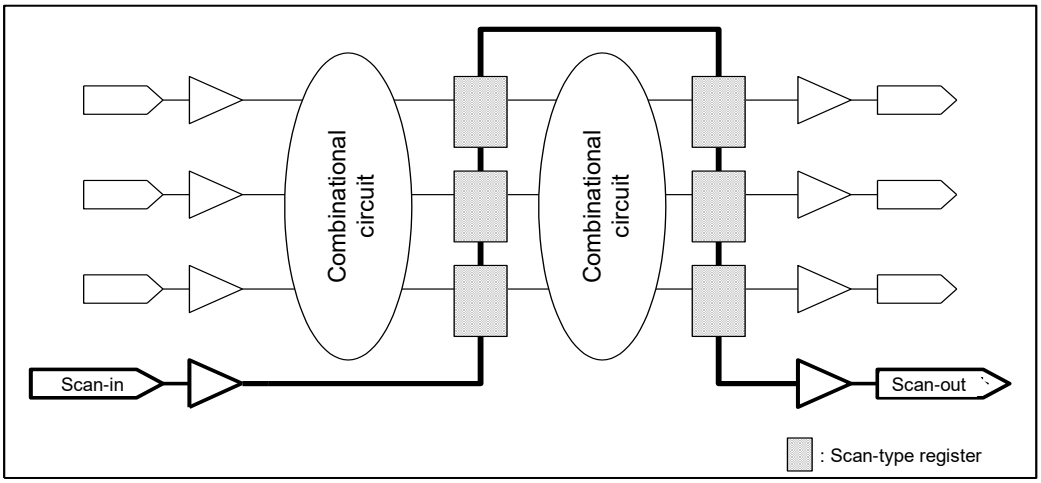


Figure 3-1 Example Scan Circuit

Note: The test patterns generated by ATPG are not intended for use in confirming specifications.
Transparent latches are not replaced with scan-type registers.

3.3 Boundary Scan (JTAG) Circuit Insertion

Please indicate in the development start order whether boundary scan (JTAG) circuits are to be inserted. Boundary scan (JTAG) circuits will be inserted by Epson.

When boundary scan (JTAG) circuits are inserted, boundary scan circuits complying with IEEE 1149.1 and their control circuits (TAP controllers) will be inserted around the logical circuits. A BDSL file containing information on these circuits will be provided at the same time.

The function patterns for the boundary scan circuits inserted will be prepared by Epson. There is no need for the customer to create boundary scan related patterns.

3.3.1 Instructions

The following boundary scan instructions are supported:

Table 3-1 List of Supported Instructions and Codes

Instruction	Code
SAMPLE/PRELOAD	0...10
BYPASS	1...11
EXTEST	0...00
CLAMP	Optional*1
HIGHZ	Optional*1
IDCODE	0...01

NOTE: *1: Epson will assign codes if they are not specified by the customer. Codes must be unique. The instruction bit width should be two to 32 bits. This will also be specified by Epson if not specified by the customer.

3.3.2 Gate Count Estimation

The increase in gate count due to boundary scan circuit insertion varies depending on factors such as supported instructions and instruction bit width. Use the following information to estimate the gate count:

Table 3-2 Gate Count Estimation (BC: Basic cell calculation)

Boundary scan block	Gate count
TAP controller + miscellaneous gates	Approx. 1,000 (BCs)
Input pin	When using normal cells: Approx. 30 (BCs/pin) When using dedicated monitoring cells: Approx. 15 (BCs/pin)
2-state output pin	Approx. 35 (BCs/pin)
3-state output pin	Approx. 65 (BCs/pin)
Bi-directional pin	Approx. 95 (BCs/pin)

3.3.3 Boundary Scan (JTAG) Circuit Insertion in Customer Design

Please observe the following design rules if JTAG circuits are inserted as part of the customer's design:

(1) Boundary scan circuits cannot coexist with AC/DC test circuits

Boundary scan circuits cannot coexist with test circuits recommended by Epson. If boundary scans are supported, the recommended AC/DC test circuits cannot be inserted.

Characters usable for external pin names:

External pin names are subject to the following constraints imposed by the BSDL format rules:

① Only alphanumeric characters (a to z, A to Z, and 0 to 9) and the underscore ("_") character can be used.

② External pin names are not case sensitive. (CLK and clk are considered identical character strings.)

③ External pin names must start with a letter of the alphabet. (0CLK, _CLK are prohibited.)

④ External pin names must not include consecutive underscores. (SYS__CLK is prohibited.)

⑤ External pin names should not end with an underscore. (CLK_ is prohibited.)

(2) Dedicated external pin preparation

Boundary scan circuits always require five dedicated external pins. Insert external pins according to the following rules:

① Clock (TCK)
Clock pin for the boundary scan circuit. Provide an input buffer with the output port not connected to anywhere.

② Mode select (TMS)
Mode select pin for the boundary scan circuit. Provide an input buffer with the output port not connected to anywhere. The input buffer used here should have a pull-up resistor.

③ Data input (TDI)
Scan data input pin for the boundary scan circuit. Provide an input buffer with the output port not connected to anywhere. The input buffer used here should have a pull-up resistor.

④ Data output (TDO)
Scan data output pin for the boundary scan circuit. Use a 3-state output buffer with the input port pulled down.

⑤ Reset (TRST)
Asynchronous reset pin for the boundary scan circuit. Provide an input buffer with the output port not connected to anywhere. The input buffer used here should have a pull-up resistor.

```
IBC U1 ( .PAD(TCK) );                          // IBC:     Normal input cell
IBCP1 U2 ( .PAD(TMS) );                        // IBCP1:   Input cell with pull-up resistor
IBCP1 U3 ( .PAD(TDI) );
IBCP1 U4 ( .PAD(TRST) );
TB1 U5 ( .PAD(TDO), .A(1'b0),.E(1'b0) );       // TB1:     3-state output cell
```

Figure 3-2 Sample Dedicated Pin Descriptions (Using Verilog)

(3) Hierarchical blocks

The hierarchical blocks of the netlist should have the following structure. Hierarchical blocks such as a TAP controller are added after boundary scans are inserted.

- Place the I/O cells in the top block.
- Place other logic elements in the sub block immediately below the top block, where possible.

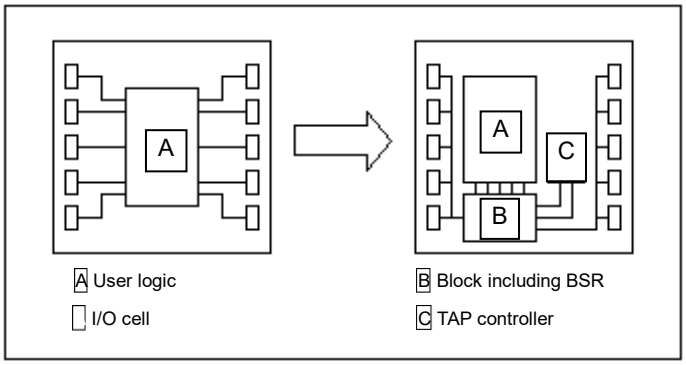


Figure 3-3 Hierarchical Block Structure Schematic

(4) I/O cell types

Boundary scan is not supported if the following I/O cells are used:

- I/O buffer with test mode
- Gated input buffer
- Open drain output buffer

(5) External pins for analog signals

Boundary scan cells are not inserted for oscillator circuit input/output pins and external pins for analog signals.

(6) Package pin and pad constraints

Package pins must be connected individually to pads on the chips on a one-to-one basis.

A package pin cannot be connected to multiple pads on a chip (multi bonding). Multiple pads cannot be interconnected (multi pad).

3.4 RAM Test Circuit: Memory BIST (Built-in Self Test)

Epson provides a memory BIST (built-in self test) in the form of a self-diagnostic circuit used to test the built-in memory.

The memory BIST will be inserted by Epson into the RTL or gate-level netlists provided by the customer.

Chapter 4 Test Pattern Generation Precautions

This chapter describes precautions to note when generating test patterns.

4.1 Sign-off Simulation Test Pattern Generation

4.1.1 Test Pattern Format

Once results have been obtained in the RTL simulation, provide the ASIC primary input/output signal waveform in VCD (value change dump) format. Note that extended VCD formats such as Extended VCD cannot be used. If you use external bi-directional pins, also output the enable signal waveform. Note that test benches described in HDL cannot be used in the Epson sign-off simulation.

Epson will convert the VCD to Epson's proprietary APF (advanced press format) test pattern format to perform the simulation. Figure 4-1 illustrates the conversion from VCD to APF. Each waveform is converted to signal values sampled once every reference cycle. Figure 4-2 shows an APF sample.

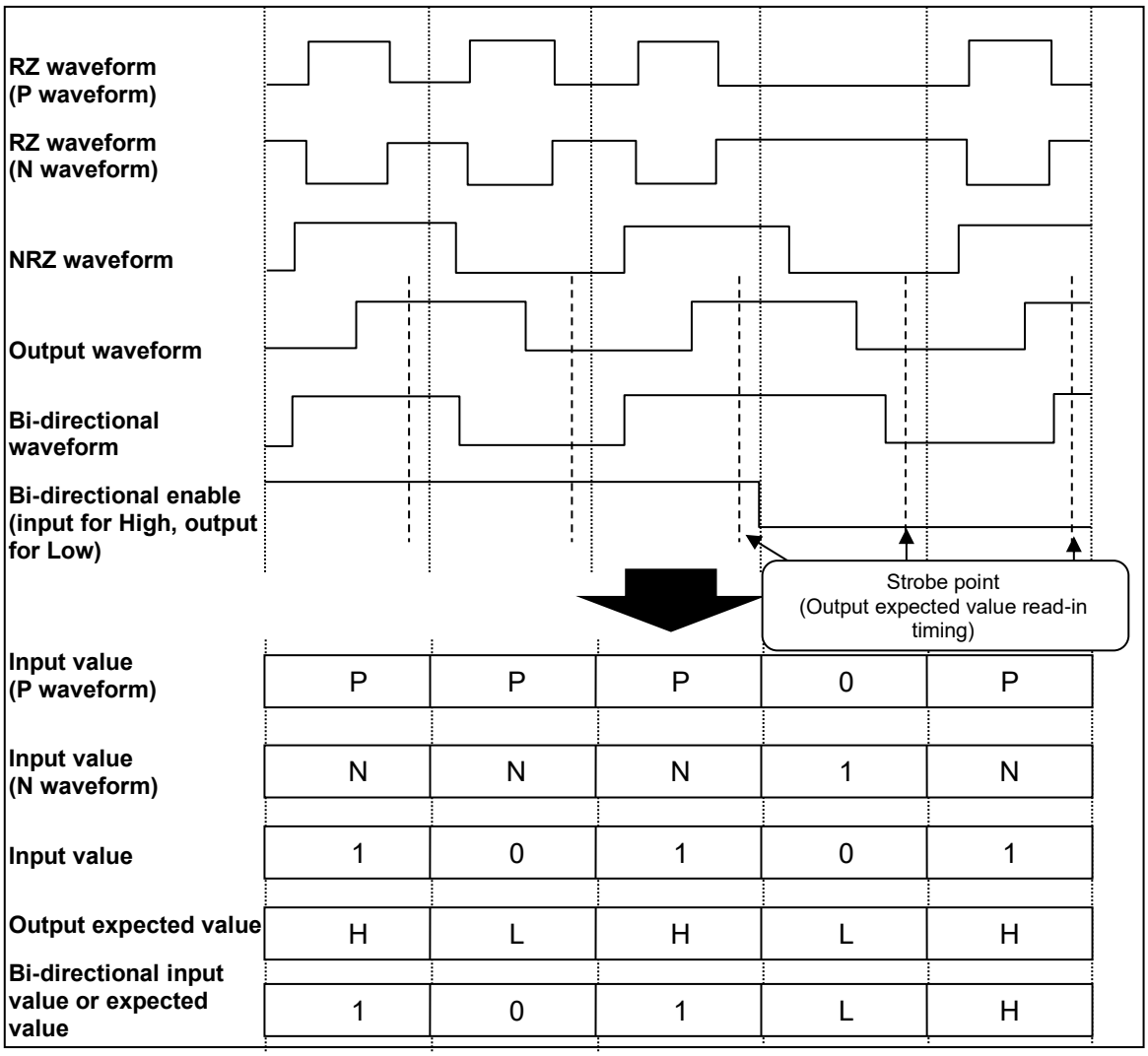


Figure 4-1 Schematic of Waveform Conversion to APF

```
# Create by Netlist Rule Check Utility at Fri Oct 6 11:42:55
$DESIGN     SAMPLE

$RATE           100000          <-- Rate (cycle) 100ns
$RESOLUTION     0.001ns
$STOROBE        85000           <-- Strobe point 85ns

#$HEX
#$ENDHEX

$IOCONT
inst01.ZO       E0      BID1
inst02.ZO       E0      BID2    <-- Internal node controlling bi-directional signal
$ENDIOCONT

$NODE
RST     I       10000           <-- Input pin with 10ns input delay
CLK     P       50000   90000   <-- Input pin with 50ns input delay, 40ns wide RZ waveform (P waveform)
XCLK    N       50000   90000   <-- Input pin with 50ns input delay, 40ns wide RZ waveform (N waveform)
INPUTB  IU      0
INPUTC  IU      0               <-- Input pin with 0ns input delay pull-up resistor
#
OUTA    O                       <-- Output pin
OUTB    O
#
BID1    B       0               <-- Bi-directional pin with 0ns input delay
BID2    B       30000
#
$ENDNODE

        $PATTERN
        #               RCXIIOOBB
        #               SLCNNUUII
        #               TKLPPTTDD   <-- Input/output signal name (comment row)
        #               KUKAB12
        #               TT
        #               BC
        #
        #               IPNIIOBB
        #                           <-- Event number (pattern cycle number)
        #
        0               1PN11XZ1L   <-- Signal value
        1               1PN01XZ0L
        2               1PN11XH1L
        3               10101LHL1
        4               1PN11LHH0

$ENDPATTERN
```

Note: Characters that can be used in signals

O: Input Low	1: Input High	P: P type RZ waveform input	N: N type RZ waveform input
L: Output Low	H: Output High	Z: Output high impedance	X: Unknown

Figure 4-2 APF Sample

4.1.2 Test Pattern Constraints

Epson performs a cycle-based simulation. Test patterns must comply with the constraints indicated below. STA analysis is required if you wish to rigorously check the input and output signal timing.

(1) Do not allow the clock cycle or pulse width to vary within the same VCD.

(2) Do not allow the skew between clocks or correlation between clock and input signal to vary within the same VCD. Ensure a constant input delay for each cycle.

(3) If clocks with different cycles exist within the same VCD, set the cycle for the fastest clock as the reference cycle time and specify cycles for other clocks as multiples of the reference cycle time.

(4) Set the P waveform clock to 0 input to stop it.

(5) Set the N waveform clock to 1 input to stop it.

(6) Unknown (X) and high impedance state (Z) cannot be input.

Figure 4-3 shows examples of input waveforms that cannot be used.

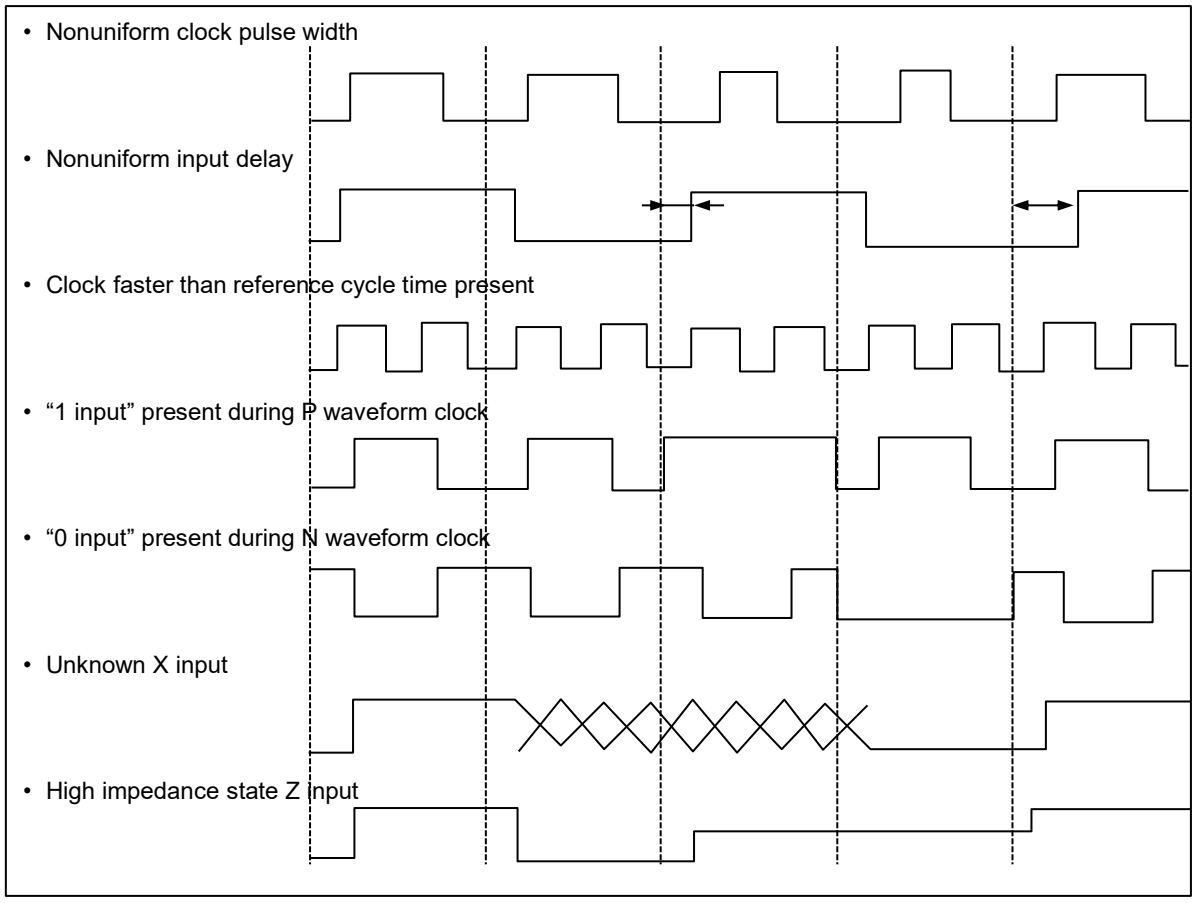


Figure 4-3 Invalid Input Waveform Examples

4.1.3 External Bi-directional Pin Enable Signal

If an external bi-directional pin is used, the waveform of the enable signal should be output accordingly. Here, make sure each external bi-directional pin is operated only by a single enable signal. If bi-directional enable signals within the RTL are configured with multiple signal logic (Figure 4-4), these must be replaced with a single signal (Figure 4-5).

```
inout data;
wire  data, cs, rd;
........
assign data = (cs & rd) ? outdata : 1'bz;
```

Figure 4-4 Bi-directional Enable Configured with Multiple Signal Logic

```
inout data;
wire  data, cs, rd, dataen;
........
assign dataen = cs & rd;
assign data = dataen ? outdata : 1'bz;
```

Figure 4-5 Replacing with Single Signal

4.2 Pre-shipment Test Pattern Generation

Epson will create pre-shipment test patterns based on test patterns received from the customer. Constraints apply due to IC tester capabilities, and changes will be made to ensure that test patterns for IC specification verification conform to the following constraints. Please note that the test patterns may need to be adjusted here in cases in which use of an IC tester is problematic—for example, if the test patterns are extremely long or if there are extremely large numbers of test patterns.

Please inform our sales representative if there are test patterns that do not require conversion for product pre-shipment testing or dedicated product pre-shipment test patterns.

4.2.1 Usable Input Waveforms

Test patterns are normally collections of 0 and 1, but delays may be added to input waveforms and pulses created when executing the simulation or when testing using an IC tester. The following two types of waveforms can be used when creating test patterns:

(1) NRZ (Non Return to Zero)

This is normally used for signals other than clocks. The signal can be varied once within a single rate to add a delay.

(2) RZ (Return to Zero)

This is used for clock and other signals. A positive or negative pulse can be generated within a single rate to efficiently create a clock signal. As with NRZ, a delay can be added.

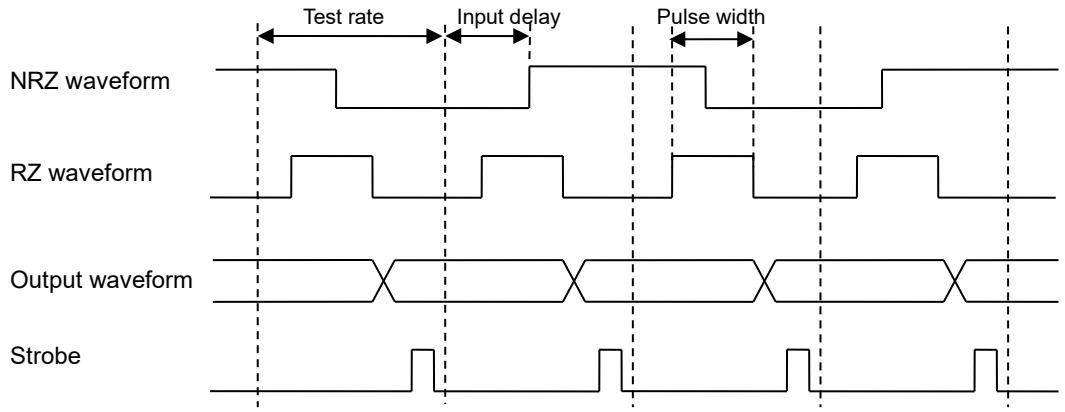


Figure 4-6 Timing Setting Constraints

4.2.2 Constraints on Test Patterns

(1) Test rates and number of events

The constraints on test rates and the number of events are as follows:

Test rate:	100ns or more, in 1ns increments (Standard: 200ns)
Number of events per test pattern:	Up to 256,000 events
Number of test patterns:	Up to 30
Total number of test pattern events:	Up to 1 million events

(2) Input delay

The constraints on input delay are as follows:

① Input delay range
Specify input delays within the range indicated below. For information on strobe point constraints, refer to "4.2.2 (5) Strobes."
0ns ≤ Input delay < Strobe point

② Input delay phase difference
If a phase difference is added to an input delay, the difference should be at least 3ns.

③ Input delay type
No more than eight different input delay types should occur within a single test pattern. A 0ns delay counts as one type here. Even if the delay value is the same, input delays are counted as different types if the waveform (RZ or NRZ) and pulse widths differ.

(3) Pulse width

The pulse width for RZ waveforms should be at least 15ns.

(4) Input waveform format

The input waveforms can use 0, 1, P, or N values. Here, P and N indicate the pulse input in RZ waveforms. P and N values cannot be specified other than as combinations of 0 and P or 1 and N for the same pin within a single test pattern.

For bi-directional pins, RZ waveforms can be input only when there is no output state within a single test pattern.

(5) Strobes

The constraints on strobes are as follows:

① Only one strobe type can be defined for each test pattern.

② The strobe minimum value must be at least 30ns after all output signals have stopped changing due to the applied input signal for all events.

③ The strobe maximum value must be smaller than the test rate minus 15ns.

④ Strobes must be set in 1ns increments.

4.2.3 AC/DC Test Patterns

For AC and DC testing, Epson will create AC and DC test patterns for the recommended Epson test circuits inserted on behalf of the customer.

Customers wishing to insert an AC or DC test circuit on their own should create test patterns, referring to "A3. AC/DC Test Patterns."

4.2.4 Notes on Handling High Impedance State

Epson prohibits the high impedance state of input pins during simulations because correct operation cannot be guaranteed.

I/O cells are available with pull-up or pull-down resistors as a measure against high impedance. However, propagation delay times for pull-up and pull-down resistors are not considered in the simulation for the reasons indicated below. Since this prevents accurate simulation of operations, the open state of bi-directional pins with pull-up or pull-down resistors in input mode is also prohibited.

<Reasons why the propagation delay of pull-up and pull-down resistors is not considered>

(1) Delay varies significantly depending on external load capacitance.

(2) Pull-up and pull-down resistors are intended only to avoid floating gates due to the high impedance state.

Before running the simulation, the test patterns are checked for the above issues using a tool. If "Z" is detected, indicating a high impedance state, the test pattern must be modified.

For the same reasons, a warning is also issued for "Z" with bi-directional pins with pull-up or pull-down resistors. Open drain bi-directional pins are also treated in the same way.

<Measures>

All "Z" occurrences for bi-directional pins are reported as errors in the test pattern check. ("Z" is excluded for 3-state and open drain output pins.)

To avoid these errors, a utility program is provided which replaces "Z" for bi-directional pins with pull-up resistors with "1" and "Z" for bi-directional pins with pull-down resistors with "0."

If a bi-directional pin switches to input mode while "X" is output, "X" is propagated as an input signal during the simulation, whether or not the pin has a pull-up or pull-down resistor, and "?" is output as the simulation result. Correct the "?" and run the simulation again.

Table 4-1 Handling Bi-directional Pin Signals in Simulation

Input pattern	I/O mode	Simulation	Simulation result (output pattern)
"X"	Input mode	"X"	"? "
"1", "H"	Input mode	"1"	"1"
"0", "L"	Input mode	"0"	"0"

Chapter 5 Design Restrictions and Limitations

This chapter describes points to note regarding oscillator circuits, preventing contention with an external bus, and metastable countermeasures.

5.1 Oscillator Circuits

5.1.1 Oscillator Circuit Configuration

Two types of dedicated oscillator cells are provided for configuring oscillator circuits with the S1L50000 Series: crystal oscillation and CR oscillation types. The crystal oscillation type is further subdivided into continuous and intermittent types. Oscillator circuits are configured as follows, depending on the type of oscillator cell used:

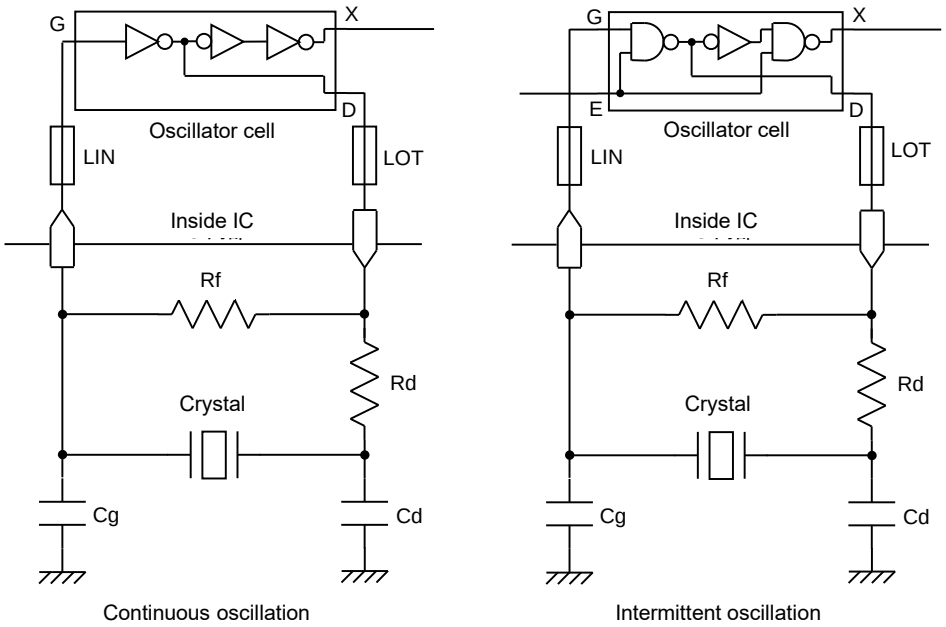


Figure 5-1 Crystal Oscillator Circuits (Internal Cell Type)

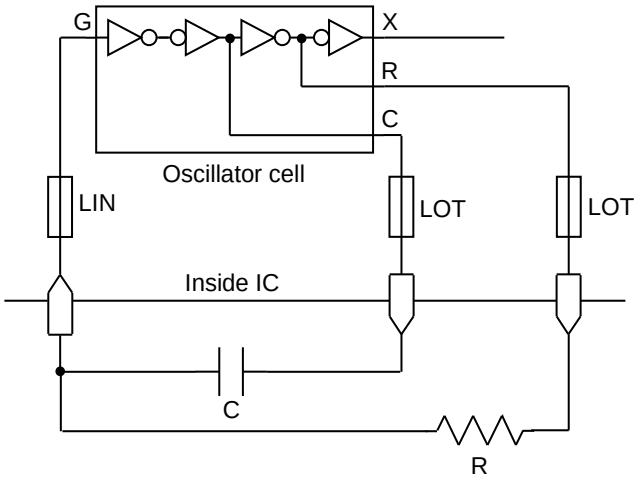


Figure 5-2 CR Oscillator Circuit

5.1.2 Notes When Using Oscillator Circuits

(1) Pinout

① Place the input and output pins of the oscillator circuit next to each other, between the power supply pins (V_{DD}, V_{SS}) on either side.

② Place the input and output pins of the oscillator circuit at a distance from other output pins, especially from those in phase or out of phase with the oscillation waveform. Place these output pins on the opposite side of the package.

③ Place the input and output pins of the oscillator circuit at a distance from input pins that operate at high speed, such as a clock.

④ Place the input and output pins of the oscillator circuit as close as possible to the center of one of the four package sides.

⑤ If multiple oscillator circuits are embedded, place the circuits at a distance from one another to prevent interference.

⑥ If using a BGA or other area array package, contact our sales representative regarding the pinout.

(2) Guide to selecting oscillator cells

Oscillation frequencies range from several tens of kilohertz to several tens of megahertz. For more information, contact our sales representative.

(3) Setting external resistance and capacitance

Oscillator circuit characteristics are dependent on the elements of the circuit (IC, crystal, Rf, Rd, Cg, Cd, and the board). Select the optimal characteristics by mounting the components on the actual board and thoroughly evaluating the values of external Rf, Rd, Cg, and Cd.

(4) Guarantee level

The oscillator circuit characteristics are dependent on the elements of the circuit (IC, crystal, Rf, Rd, Cg, Cd, and the board). Thus, Epson cannot guarantee the oscillation operation or characteristics. The customer should thoroughly evaluate and confirm oscillation characteristics using ES samples.

(5) Clock signal input to the IC internal circuit

Due to the difficulty of specifying the waveform of the clock signal to be generated (signal of the oscillator cell X) in advance, the logic simulator can accurately handle only the clock frequency. For example, the actual clock duty of the IC will differ from simulation results.

Therefore, avoid using circuits utilizing both rising and falling times of the generated clock signal. Doing otherwise may produce circuits with errors not matching simulation results. Use circuits utilizing only the rising or falling time of the generated clock signal.

5.1.3 RTL Description for Oscillator Cells

For information on the RTL description of oscillator cells, refer to "2.6 Oscillator Cell Description."

5.2 Metastable

In the case of FF and latch cell input signals, if they violate timing rules, such as clock and data setup time, hold time, and recovery or removal time of clock set and reset, the FF and latch cell output signals may go neither high or low level. This unstable state of output signals is called “metastable.”

The metastable state ends after some time and output signals enter the defined state of either high or low level. However, the defined levels are not dependent on the data input level, and thus outputs are in unknown state.

When setup/hold and recovery/removal timing specifications are not met, take appropriate measures to prevent the metastable state from propagating to the whole circuit.

The metastable time is estimated using the following formula when setup/hold and recovery/removal time specifications are not met:

Metastable time = $T_{pd} \times 6$

Where T_{pd} is the delay time from the active edge of FF, latch cell clock, set, and reset signals to output change.

Logic simulation does not consider the delay of signals in the metastable state. Ensure that the design meets the timing specifications.

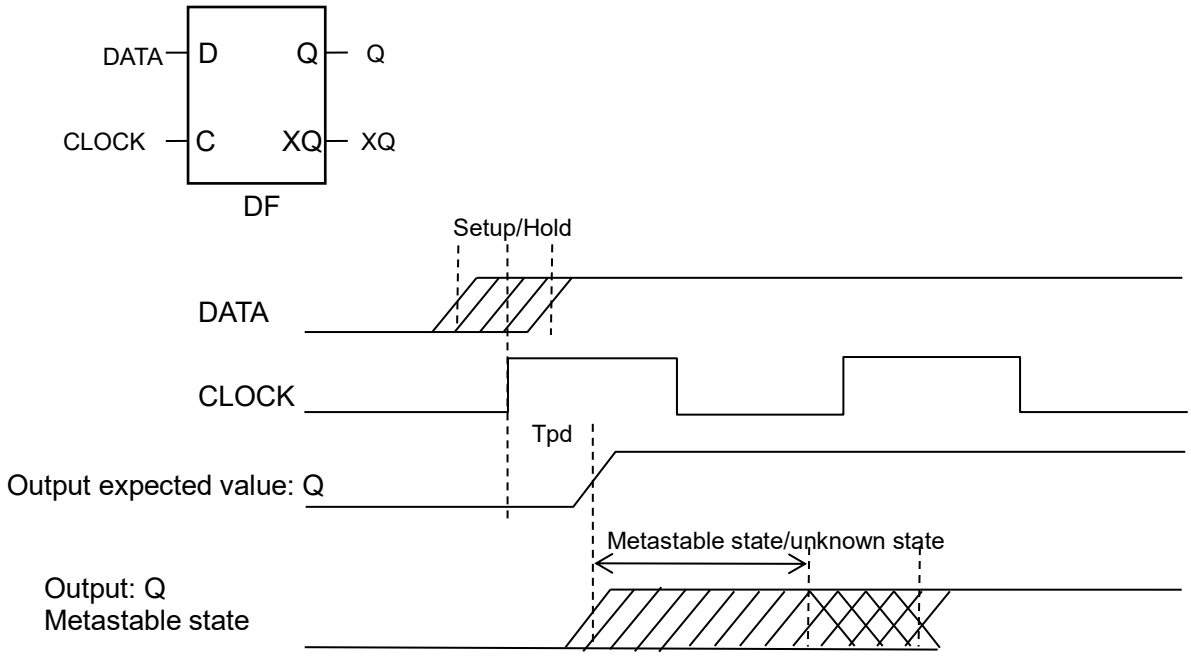


Figure 5-3 DF Metastable State

Chapter 6 Types of I/O Buffers and Notes on Use

This chapter describes in detail how to configure S1L50000 Series input, output, and bi-directional I/O buffers. Note that S1L50000 Series I/O buffers can be used for both dual power supply and single power supply applications.

6.1 I/O Buffer Types and Selection

A wide variety of I/O buffers are available, with different input interface levels, with or without Schmitt trigger input, with or without pull-up or pull-down resistors, with different output drive capability, and with or without noise immunity. Fail-safe buffers and input level shifters are also available to allow signal input at voltages higher than the power supply voltage.

For information on output drive capacity and the electrical characteristics of pull-up and pull-down resistors, refer to Tables 1-6 and 1-7 in "1.3 Electrical Characteristics and Specifications" and "A4. Input/Output Buffer Characteristic Graphs."

6.1.1 Selection of I/O buffers

A tool is provided for the S1L50000 Series to help select I/O buffers. Refer to the following URL:

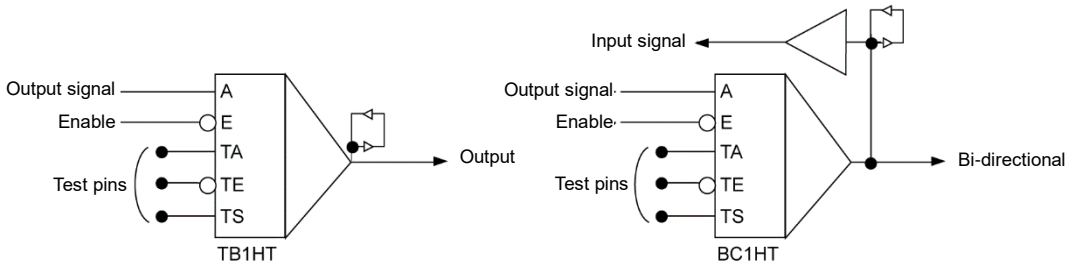
Design Guide supplementary information: S1L50000 Series I/O Buffer List
<https://www.epson.jp/prod/semicon/products/asic/gatearray/s1l50k_io.htm>

6.1.2 I/O Buffers with Bus Hold Function

I/O buffers are available with a bus hold function that retains output pin data to prevent output pins or bi-directional pins from switching to the high impedance state.

Do not use the retained data output as valid data. The holding function of the bus hold circuit is restrained to avoid affecting normal operations. The data may vary easily if any other external data is supplied.

For information on output bus hold current, refer to Tables 1-8 to 1-10 in "1.3 Electrical Characteristics and Specifications."



(a) Output buffer (b) Bi-directional buffer

Figure 6-1 Typical Bus Hold Circuit Symbols

6.2 Notes on Using Dual Power Supplies

Dual power supply capability allows each I/O buffer to interface with either 5.0V or 3.3V signals. The internal cell area operates using a 3.3V single power supply.

6.2.1 Implementing Dual Power Supply Designs

The S1L50000 Series can interface signals with voltages differing from the core cell operating voltage. The following two ways are available to interface with different voltage systems:

- When using a single power supply

In a single power supply design, use of N-channel open drain buffers or fail-safe buffers allows the designer to input higher voltage signals than the power supply voltage. However, it is not possible to output higher voltage signals than the power supply voltage. This requires the use of N-channel open drain type buffers in conjunction with pull-up resistors.

- When using dual power supplies

The use of dedicated dual power supply input buffers allows the designer to input higher voltage signals than the core cell operating voltage. Using dual power supply output buffers also allows the output of higher voltage signals than the core cell operating voltage.

6.2.2 Power Supply for Dual Power Supply Designs

To provide two different voltage power supplies, use two power supply cells: HV_{DD} and LV_{DD}. The HV_{DD} power supply is used for HV_{DD} voltage I/O buffers; the LV_{DD} power supply is used for LV_{DD} voltage I/O buffers and core cells. The power supply voltages must meet the following conditions at all times:

$HV_{DD} \geq LV_{DD}$

Operation cannot be guaranteed if HV_{DD} is less than LV_{DD}. The following operating conditions are recommended:

HV_{DD} = 5.0V, LV_{DD} = 3.3V

6.2.3 Power On-Off Sequence

(1) Power on-off sequence

In case of dual power supply chips, the power on/off sequence is as follows:

To power on:	LV_{DD} → HV_{DD} (I/O core) → Turn on input signals
To power off:	Turn on input signals → HV_{DD} (I/O core) → LV_{DD}

(2) Notes

Note 1: Do not apply only the HV_{DD} voltage continuously (for more than 1 second) when the LV_{DD} power supply is turned off. Doing so may affect chip reliability and cause chip malfunctions.

Application for even less than 1 second may cause the following problems:

① Operation cannot be guaranteed during this period because the pin state is unknown. Note that this means there is a risk of output short-circuiting with external devices connected to the pin or external device malfunctions.

② An unpredictable flow-through current may pass through the HV_{DD} circuit during this period because the HV_{DD} circuit state is unknown. This may result in failure to start due to shortage of external power supply current capacity.

Note 2: Due to power supply noise effects, the core circuit state cannot be guaranteed when the HV_{DD} power supply is returned from the off to the on state. Be sure to initialize the circuit after turning on the power supply.

6.3 I/O Buffers for Dual Power Supply Operation

For dual power supply designs using the S1L50000 Series, use dedicated dual power supply I/O buffers. (Single power supply I/O buffers cannot be used.)

Dedicated dual power supply I/O buffers cannot be used with single power supply I/O buffers.

(1) HV_{DD} I/O buffers

HV_{DD} I/O buffers are available in the form of input buffers for inputting 5.0V (or 3.3V) signals, output buffers for outputting 5.0V (or 3.3V) oscillation signals, and bi-directional buffers for inputting 5.0V (or 3.3V) signals and outputting 5.0V (or 3.3V) oscillation signals.

(2) LV_{DD} I/O buffers

LV_{DD} I/O buffers are available in the form of input buffers for inputting 3.3V signals, output buffers for outputting 3.3V oscillation signals, and bi-directional buffers for inputting 3.3V signals and outputting 3.3V oscillation signals.

Inputting an HV_{DD} signal to an LV_{DD} bi-directional buffer results in an excessive current flowing through the protection diode inside the LV_{DD} buffer, reducing quality. Do not apply a voltage greater than LV_{DD}. (In such cases, use fail-safe I/O buffers described in "6.5. Fail-Safe I/O Buffers".)

6.3.1 Input Buffers

(1) HV_{DD} input buffers

HV_{DD} input buffers convert HV_{DD} signals to LV_{DD} signals and supply these signals to MSI cells (internal cell area).

Table 6-1 lists the HV_{DD} input buffer pull-up and pull-down resistors.

Table 6-1 HV_{DD} Pull-up and Pull-down Resistors

Pull-up/Pull-down Resistors	Resistance		Unit
	HV_{DD} = 5.0V	HV_{DD} = 3.3V	
Type 1	60	100	kΩ
Type 2	120	200	kΩ

Tables 6-2-1 to 6-2-4 list the HV_{DD} input buffers.

Table 6-2-1 HV_{DD} Input Buffers (HV_{DD} = 5.0V)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2*3
HIBC	CMOS	None
HIBCP#	CMOS	Pull-up resistor (60kΩ, 120kΩ)
HIBCD#	CMOS	Pull-down resistor (60kΩ, 120kΩ)
HIBT *4	TTL	None
HIBTP# *4	TTL	Pull-up resistor (60kΩ, 120kΩ)
HIBTD# *4	TTL	Pull-down resistor (60kΩ, 120kΩ)
HIBH	CMOS Schmitt	None
HIBHP#	CMOS Schmitt	Pull-up resistor (60kΩ, 120kΩ)
HIBHD#	CMOS Schmitt	Pull-down resistor (60kΩ, 120kΩ)
HIBS *4	TTL Schmitt	None
HIBSP# *4	TTL Schmitt	Pull-up resistor (60kΩ, 120kΩ)
HIBSD# *4	TTL Schmitt	Pull-down resistor (60kΩ, 120kΩ)
HIBPA *4	PCI-5V	None
HIBPAP# *4	PCI-5V	Pull-up resistor (60kΩ, 120kΩ)
HIBPAD# *4	PCI-5V	Pull-down resistor (60kΩ, 120kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-up and pull-down resistances, refer to Table 1-7 and "A4.1.6."
*3: For the input buffer characteristics graphs, refer to "A4.1.2."
*4: V_{DD} = 5.0V only.

Table 6-2-2 HV_{DD} Input Buffers (HV_{DD} = 3.3V)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2 *3
HIBC	LVTTL	None
HIBCP#	LVTTL	Pull-up resistor (100kΩ, 200kΩ)
HIBCD#	LVTTL	Pull-down resistor (100kΩ, 200kΩ)
HIBH	LVTTL Schmitt	None
HIBHP#	LVTTL Schmitt	Pull-up resistor (100kΩ, 200kΩ)
HIBHD#	LVTTL Schmitt	Pull-down resistor (100kΩ, 200kΩ)
HIBPB	PCI-3V	None
HIBPBP#	PCI-3V	Pull-up resistor (100kΩ, 200kΩ)
HIBPBD#	PCI-3V	Pull-down resistor (100kΩ, 200kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-up and pull-down resistances, refer to Table 1-7 and "A4.2.7."
*3: For the input buffer characteristics graphs, refer to "A4.2.2."

Table 6-2-3 HV_{DD} Input Level Shifters (HV_{DD} = 5.0V)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2
HIDC	CMOS	None
HIDCD#	CMOS	Pull-down resistor (60kΩ, 120kΩ)
HIDH	CMOS Schmitt	None
HIDHD#	CMOS Schmitt	Pull-down resistor (60kΩ, 120kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-down resistances, refer to Table 1-7 and "A4.1.6."

Table 6-2-4 HV_{DD} Input Level Shifters (HV_{DD} = 3.3V) (5V input also permitted)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2
HIDC	LVTTL	None
HIDCD#	LVTTL	Pull-down resistor (100kΩ, 200kΩ)
HIDH	LVTTL Schmitt	None
HIDHD#	LVTTL Schmitt	Pull-down resistor (100kΩ, 200kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-down resistances, refer to Table 1-7 and "A4.2.7."

(2) LV_{DD} input buffers

Table 6-3 lists the LV_{DD} input buffer pull-up and pull-down resistors.

Table 6-3 LV_{DD} Pull-up and Pull-down Resistors

Pull-up/Pull-down Resistors	Resistance	Unit
	LV_{DD} = 3.3V	
Type 1	50	kΩ
Type 2	100	kΩ

Tables 6-4-1 and 6-4-2 list the LV_{DD} input buffers.

Table 6-4-1 LV_{DD} Input Buffers (LV_{DD} = 3.3V)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2*3
LIBC	LVTTL	None
LIBCP#	LVTTL	Pull-up resistor (50kΩ, 100kΩ)
LIBCD#	LVTTL	Pull-down resistor (50kΩ, 100kΩ)
LIBH	LVTTL Schmitt	None
LIBHP#	LVTTL Schmitt	Pull-up resistor (50kΩ, 100kΩ)
LIBHD#	LVTTL Schmitt	Pull-down resistor (50kΩ, 100kΩ)
LIBPB	PCI-3V	None
LIBPBP#	PCI-3V	Pull-up resistor (50kΩ, 100kΩ)
LIBPBD#	PCI-3V	Pull-down resistor (50kΩ, 100kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-up and pull-down resistances, refer to Table 1-7 and "A4.2.7."
*3: For the input buffer characteristics graphs, refer to "A4.2.2."

Table 6-4-2 LV_{DD} Input Level Shifters (LV_{DD} = 3.3V) (5V input also permitted)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2
LIDC	LVTTL	None
LIDCD#	LVTTL	Pull-down resistor (50kΩ, 100kΩ)
LIDH	LVTTL Schmitt	None
LIDHD#	LVTTL Schmitt	Pull-down resistor (50kΩ, 100kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-down resistances, refer to Table 1-7 and "A4.2.7."

6.3.2 Output Buffers

As described in "3.1.2 Cell Names for Output Buffers with Test Circuits and Bi-directional Buffers," cell names for output buffers with test circuits are suffixed with "T."

(1) HV_{DD} output buffers

Table 6-5 shows the I_{OL} and I_{OH} specifications for HV_{DD} output buffers.

Table 6-5 I_{OL} and I_{OH} Specifications for HV_{DD} Output Buffer Voltages

Output Current	I_{OL}*1/I_{OH}*2		Unit
	HV_{DD} = 5.0V	HV_{DD} = 3.3V	
Type S	0.1/-0.1	0.1/-0.1	mA
Type M	1/-1	1/-1	mA
Type 1	3/-3	2/-2	mA
Type 2	8/-8	6/-6	mA
Type 3	12/-12	12/-12	mA
Type 4	24/-12	-	mA

NOTE: *1: V_{OL} = 0.4V
*2: V_{OH} = HV_{DD} − 0.4V

Tables 6-6-1 to 6-6-4 list the HV_{DD} output buffers.

Table 6-6-1 HV_{DD} Output Buffers (HV_{DD} = 5.0V)

Function	I_{OL}/I_{OH} *1 *2	Cell Name
Normal output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HOBST HOBMT HOB1T HOB2T HOB3T HOB4T
Normal Output for PCI	PCI-5V	HOBPAT
Normal output for high speed	12mA/-12mA 24mA/-12mA	HOB3AT HOB4AT
Normal output for low noise	12mA/-12mA 24mA/-12mA	HOB3BT HOB4BT
3-state output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HTBST HTBMT HTB1T HTB2T HTB3T HTB4T
3-state output for high speed	12mA/-12mA 24mA/-12mA	HTB3AT HTB4AT
3-state output for low noise	12mA/-12mA 24mA/-12mA	HTB3BT HTB4BT
3-state output for PCI	PCI-5V	HTBPAT
3-state output (with bus hold function)	1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HTBMHT HTB1HT HTB2HT HTB3HT HTB4HT
3-state output for high speed (with bus hold function)	12mA/-12mA 24mA/-12mA	HTB3AHT HTB4AHT
3-state output for low noise (with bus hold function)	12mA/-12mA 24mA/-12mA	HTB3BHT HTB4BHT

NOTE: *1: V_{OL} = 0.4V, V_{OH} = HV_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.1.3 Output Driver Characteristics."

Table 6-6-2 HV_{DD} Output Buffers (HV_{DD} = 3.3V)

Function	I_{OL}/I_{OH} *1 *2	Cell Name
Normal output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	HOBST HOBMT HOB1T HOB2T HOB3T
Normal output for high speed	12mA/-12mA	HOB3AT
Normal output for low noise	12mA/-12mA	HOB3BT
Normal output for PCI	PCI-3V	HOBPBT
3-state output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	HTBST HTBMT HTB1T HTB2T HTB3T
3-state output for high speed	12mA/-12mA	HTB3AT
3-state output for low noise	12mA/-12mA	HTB3BT
3-state output for PCI	PCI-3V	HTBPBT
3-state output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	HTBMHT HTB1HT HTB2HT HTB3HT
3-state output for high speed (with bus hold function)	12mA/-12mA	HTB3AHT
3-state output for low noise (with bus hold function)	12mA/-12mA	HTB3BHT

NOTE: *1: V_{OL} = 0.4V, V_{OH} = HV_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

Table 6-6-3 HV_{DD} N-Channel Open Drain Output Buffers (HV_{DD} = 5.0V)

Function	I_{OL} *1 *2	Cell Name
Normal output	3mA 8mA 12mA 24mA	HOD1T HOD2T HOD3T HOD4T

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to the graphs in "A4.1.3 Output Driver Characteristics."

Table 6-6-4 HV_{DD} N-Channel Open Drain Output Buffers (HV_{DD} = 3.3V)

Function	I_{OL}*1 *2	Cell Name
Normal output	2mA 6mA 12mA	HOD1T HOD2T HOD3T

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

(2) LV_{DD} output buffers

Table 6-7 shows the I_{OL} and I_{OH} specifications for LV_{DD} output buffers.

Table 6-7 I_{OL} and I_{OH} Specifications for LV_{DD} Output Buffer Voltages

Output Current	I_{OL}*1/I_{OH}*2	Unit
	LV_{DD} = 3.3V	
Type S	0.1/-0.1	mA
Type M	1/-1	mA
Type 1	2/-2	mA
Type 2	6/-6	mA
Type 3	12/-12	mA

NOTE: *1: V_{OL} = 0.4V
*2: $V_{OH} = LV_{DD} - 0.4V$

Tables 6-8-1 to 6-8-3 list the LV_{DD} output buffers.

Table 6-8-1 LV_{DD} Output Buffers (LV_{DD} = 3.3V)

Function	I_{OL}/I_{OH} *1 *2	Cell Name
Normal output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	LOBST LOBMT LOB1T LOB2T LOB3T
Normal output for high speed	12mA/-12mA	LOB3AT
Normal output for low noise	12mA/-12mA	LOB3BT
Normal output for PCI	PCI-3V	LOBPBT
3-state output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	LTBST LTBMT LTB1T LTB2T LTB3T
3-state output for high speed	12mA/-12mA	LTB3AT
3-state output for low noise	12mA/-12mA	LTB3BT
3-state output for PCI	PCI-3V	LTBPBT
3-state output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	LTBMHT LTB1HT LTB2HT LTB3HT
3-state output for high speed (with bus hold function)	12mA/-12mA	LTB3AHT
3-state output for low noise (with bus hold function)	12mA/-12mA	LTB3BHT

NOTE: *1: V_{OL} = 0.4V, V_{OH} = LV_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

Table 6-8-2 LV_{DD} N-Channel Open Drain Output Buffers (LV_{DD} = 3.3V)

Function	I_{OL}*1 *2	Cell Name
Normal output	2mA 6mA 12mA	LOD1T LOD2T LOD3T
High speed output	2mA 6mA	LOD1CT LOD2CT

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

Table 6-8-3 LV_{DD} Fail-Safe Output Buffers (LV_{DD} = 3.3V)

Function	I_{OL}*1 *2	Cell Name
Normal output	2mA 6mA	LTBF1 LTBF2
High speed output	2mA 6mA 12mA	LTBF1C LTBF2C LTBF3A

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

6.3.3 Bi-directional Buffers

(1) HV_{DD} bi-directional buffers

Tables 6-9-1 to 6-9-6 list the HV_{DD} bi-directional buffers.

Table 6-9-1 HV_{DD} Bi-directional Buffers (1/3) (HV_{DD} = 5.0V)

Input Level	Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
TTL	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HBTST HBTMT HBT1T HBT2T HBT3T HBT4T	HBTSD#T HBTMD#T HBT1D#T HBT2D#T HBT3D#T HBT4D#T	HBTSP#T HBTMP#T HBT1P#T HBT2P#T HBT3P#T HBT4P#T
	Bi-directional output for high speed	12mA/-12mA 24mA/-12mA	HBT3AT HBT4AT	HBT3AD#T HBT4AD#T	HBT3AP#T HBT4AP#T
	Bi-directional output for low noise	12mA/-12mA 24mA/-12mA	HBT3BT HBT4BT	HBT3BD#T HBT4BD#T	HBT3BP#T HBT4BP#T
CMOS	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HBCST HBCMT HBC1T HBC2T HBC3T HBC4T	HBCSD#T HBCMD#T HBC1D#T HBC2D#T HBC3D#T HBC4D#T	HBCSP#T HBCMP#T HBC1P#T HBC2P#T HBC3P#T HBC4P#T
	Bi-directional output for high speed	12mA/-12mA 24mA/-12mA	HBC3AT HBC4AT	HBC3AD#T HBC4AD#T	HBC3AP#T HBC4AP#T
	Bi-directional output for low noise	12mA/-12mA 24mA/-12mA	HBC3BT HBC4BT	HBC3BD#T HBC4BD#T	HBC3BP#T HBC4BP#T
PCI	Bi-directional output for PCI	PCI-5V	HBPAT	HBPAD#T	HBPAP#T

NOTE: *1: V_{OL} = 0.4V, V_{OH} = HV_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.1.3 Output Driver Characteristics."
*3: The # symbol corresponds to "1" for a resistance of 60kΩ or "2" for a resistance of 120kΩ.

Table 6-9-2 HV_{DD} Bi-directional Buffers (2/3) (HV_{DD} = 5.0V)

Input Level	Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
TTL Schmitt	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HBSST HBSMT HBS1T HBS2T HBS3T HBS4T	HBSSD*T HBSMD*T HBS1D*T HBS2D*T HBS3D*T HBS4D*T	HBSSP*T HBSMP*T HBS1P*T HBS2P*T HBS3P*T HBS4P*T
	Bi-directional output for high speed	12mA/-12mA 24mA/-12mA	HBS3AT HBS4AT	HBS3AD*T HBS4AD*T	HBS3AP*T HBS4AP*T
	Bi-directional output for low noise	12mA/-12mA 24mA/-12mA	HBS3BT HBS4BT	HBS3BD*T HBS4BD*T	HBS3BP*T HBS4BP*T
CMOS Schmitt	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HBHST HBHMT HBH1T HBH2T HBH3T HBH4T	HBHSD*T HBHMD*T HBH1D*T HBH2D*T HBH3D*T HBH4D*T	HBHSP*T HBHMP*T HBH1P*T HBH2P*T HBH3P*T HBH4P*T
	Bi-directional output for high speed	12mA/-12mA 24mA/-12mA	HBH3AT HBH4AT	HBH3AD*T HBH4AD*T	HBH3AP*T HBH4AP*T
	Bi-directional output for low noise	12mA/-12mA 24mA/-12mA	HBH3BT HBH4BT	HBH3BD*T HBH4BD*T	HBH3BP*T HBH4BP*T

NOTE: *1: V_{OL} = 0.4V, V_{OH} = HV_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.1.3 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 60kΩ or "2" for a resistance of 120kΩ.

Table 6-9-3 HV_{DD} Bi-directional Buffers (3/3) (HV_{DD} = 5.0V)

Input Level	Function	I_{OL}/I_{OH} *1 *2	No Resistor	With Pull-down Resistor	With Pull-up Resistor
TTL	Bi-directional output (with bus hold function)	1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HBTMHT HBT1HT HBT2HT HBT3HT HBT4HT	None	None
	Bi-directional output for high speed (with bus hold function)	12mA/-12mA 24mA/-12mA	HBT3AHT HBT4AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA 24mA/-12mA	HBT3BHT HBT4BHT	None	None
CMOS	Bi-directional output (with bus hold function)	1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HBCMHT HBC1HT HBC2HT HBC3HT HBC4HT	None	None
	Bi-directional output for high speed (with bus hold function)	12mA/-12mA 24mA/-12mA	HBC3AHT HBC4AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA 24mA/-12mA	HBC3BHT HBC4BHT	None	None
TTL Schmitt	Bi-directional output (with bus hold function)	1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HBSMHT HBS1HT HBS2HT HBS3HT HBS4HT	None	None
	Bi-directional output for high speed (with bus hold function)	12mA/-12mA 24mA/-12mA	HBS3AHT HBS4AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA 24mA/-12mA	HBS3BHT HBS4BHT	None	None
CMOS Schmitt	Bi-directional output (with bus hold function)	1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HBHMHT HBH1HT HBH2HT HBH3HT HBH4HT	None	None
	Bi-directional output for high speed (with bus hold function)	12mA/-12mA 24mA/-12mA	HBH3AHT HBH4AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA 24mA/-12mA	HBH3BHT HBH4BHT	None	None

NOTE: *1: V_{OL} = 0.4V, V_{OH} = HV_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.1.3 Output Driver Characteristics."

Table 6-9-4 HV_{DD} Bi-directional Buffers (HV_{DD} = 3.3V)

Input Level	Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
LVTTL	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	HBCST HBCMT HBC1T HBC2T HBC3T	HBCSD*T HBCMD*T HBC1D*T HBC2D*T HBC3D*T	HBCSP*T HBCMP*T HBC1P*T HBC2P*T HBC3P*T
	Bi-directional output for high speed	12mA/-12mA	HBC3AT	HBC3AD*T	HBC3AP*T
	Bi-directional output for low noise	12mA/-12mA	HBC3BT	HBC3BD*T	HBC3BP*T
PCI	Bi-directional output for PCI	PCI-3V	HBPBT	HBPBD*T	HBPBP*T
LVTTL Schmitt	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	HBHST HBHMT HBH1T HBH2T HBH3T	HBHSD*T HBHMD*T HBH1D*T HBH2D*T HBH3D*T	HBHSP*T HBHMP*T HBH1P*T HBH2P*T HBH3P*T
	Bi-directional output for high speed	12mA/-12mA	HBH3AT	HBH3AD*T	HBH3AP*T
	Bi-directional output for low noise	12mA/-12mA	HBH3BT	HBH3BD*T	HBH3BP*T
LVTTL	Bi-directional output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	HBCMHT HBC1HT HBC2HT HBC3HT	None	None
	Bi-directional output for high speed (with bus hold function)	12mA/-12mA	HBC3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA	HBC3BHT	None	None
LVTTL Schmitt	Bi-directional output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	HBHMHT HBH1HT HBH2HT HBH3HT	None	None
	Bi-directional output for high speed (with bus hold function)	12mA/-12mA	HBH3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA	HBH3BHT	None	None

NOTE: *1: V_{OL} = 0.4V, V_{OH} = HV_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 100kΩ or "2" for a resistance of 200kΩ.

Table 6-9-5 HV_{DD} N-Channel Open Drain Bi-directional Buffers (HV_{DD} = 5.0V)

Input Level	Function	I_{OL}*1 *2	Cell Name
TTL	Bi-directional output	3mA 8mA 12mA 24mA	HBDT1T HBDT2T HBDT3T HBDT4T
CMOS	Bi-directional output	3mA 8mA 12mA 24mA	HBDC1T HBDC2T HBDC3T HBDC4T
TTL Schmitt	Bi-directional output	3mA 8mA 12mA 24mA	HBDS1T HBDS2T HBDS3T HBDS4T
CMOS Schmitt	Bi-directional output	3mA 8mA 12mA 24mA	HBDH1T HBDH2T HBDH3T HBDH4T

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to the graphs in "A4.1.3 Output Driver Characteristics."

Table 6-9-6 HV_{DD} N-Channel Open Drain Bi-directional Buffers (HV_{DD} = 3.3V)

Input Level	Function	I_{OL}*1 *2	Cell Name
LVTTL	Bi-directional output	2mA 6mA 12mA	HBDC1T HBDC2T HBDC3T
LVTTL Schmitt	Bi-directional output	2mA 6mA 12mA	HBDH1T HBDH2T HBDH3T

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

(2) LV_{DD} bi-directional buffers

Tables 6-10-1 to 6-10-4 list the LV_{DD} bi-directional buffers.

Table 6-10-1 LV_{DD} Bi-directional Buffers (1/2) (LV_{DD} = 3.3V)

Input Level	Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
LVTTL	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	LBCST LBCMT LBC1T LBC2T LBC3T	LBCSD*T LBCMD*T LBC1D*T LBC2D*T LBC3D*T	LBCSP*T LBCMP*T LBC1P*T LBC2P*T LBC3P*T
	Bi-directional output for high speed	12mA/-12mA	LBC3AT	LBC3AD*T	LBC3AP*T
	Bi-directional output for low noise	12mA/-12mA	LBC3BT	LBC3BD*T	LBC3BP*T
PCI	Bi-directional output for PCI	PCI-3V	LBPBT	LBPBD*T	LBPBP*T
LVTTL Schmitt	Bi-directional for low noise output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	LBHST LBHMT LBH1T LBH2T LBH3T	LBHSD*T LBHMD*T LBH1D*T LBH2D*T LBH3D*T	LBHSP*T LBHMP*T LBH1P*T LBH2P*T LBH3P*T
	Bi-directional output for high speed	12mA/-12mA	LBH3AT	LBH3AD*T	LBH3AP*T
	Bi-directional output for low noise	12mA/-12mA	LBH3BT	LBH3BD*T	LBH3BP*T

NOTE: *1: V_{OL} = 0.4V, V_{OH} = LV_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 50kΩ or "2" for a resistance of 100kΩ.

Table 6-10-2 LV_{DD} Bi-directional Buffers (2/2) (LV_{DD} = 3.3V)

Input Level	Function	I_{OL}/I_{OH} *1 *2	No Resistor	With Pull-down Resistor	With Pull-up Resistor
LVTTL	Bi-directional output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	LBCMHT LBC1HT LBC2HT LBC3HT	None	None
	Bi-directional output for high speed (with bus hold function)	12mA/-12mA	LBC3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA	LBC3BHT	None	None
LVTTL Schmitt	Bi-directional output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	LBHMHT LBH1HT LBH2HT LBH3HT	None	None
	Bi-directional output for high speed (with bus hold function)	12mA/-12mA	LBH3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA	LBH3BHT	None	None

NOTE: *1: V_{OL} = 0.4V, V_{OH} = LV_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

Table 6-10-3 LV_{DD} N-Channel Open Drain Bi-directional Buffers (LV_{DD} = 3.3V)
(5V input also permitted)

Input Level	Function	I_{OL} *1 *2	Cell Name
LVTTL	Bi-directional output	2mA 6mA 12mA	LBDC1T LBDC2T LBDC3T
	Bi-directional output for high speed	2mA 6mA	LBDC1CT LBDC2CT
LVTTL Schmitt	Bi-directional output	2mA 6mA 12mA	LBDH1T LBDH2T LBDH3T
	Bi-directional output for high speed	2mA 6mA	LBDH1CT LBDH2CT

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

Table 6-10-4 LV_{DD} Fail-Safe Bi-directional Buffers (LV_{DD} = 3.3V) (5V input also permitted)

Input Level	Function	I_{OL} *1 *2	Cell Name
LVTTL*2	Bi-directional output	2mA 6mA	LBB1 LBB2
	Bi-directional output for high speed	2mA 6mA 12mA	LBB1C LBB2C LBB3A
LVTTL Schmitt*3	Bi-directional output	2mA 6mA	LBG1 LBG2
	Bi-directional output for high speed	2mA 6mA 12mA	LBG1C LBG2C LBG3A

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

6.4 I/O Buffers for Single Power Supply Operation

When using a single power supply with the S1L50000 Series, use dedicated single power supply I/O buffers.

6.4.1 Input Buffers

Table 6-11 shows pull-up and pull-down resistances for single power supply input buffers.

Table 6-11 Single Power Supply Pull-up and Pull-down Resistances

Pull-up/Pull-down Resistors	Resistance (Typ.)	Unit
	V_{DD} = 3.3V	
Type 1	50	kΩ
Type 2	100	kΩ

Tables 6-12-1 and 6-12-2 list the single power supply input buffers.

Table 6-12-1 Single Power Supply Input Buffers (V_{DD} = 3.3V)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2 *3
IBC	LVTTL	None
IBCP#	LVTTL	Pull-up resistor (50kΩ, 100kΩ)
IBCD#	LVTTL	Pull-down resistor (50kΩ, 100kΩ)
IBH	LVTTL Schmitt	None
IBHP#	LVTTL Schmitt	Pull-up resistor (50kΩ, 100kΩ)
IBHD#	LVTTL Schmitt	Pull-down resistor (50kΩ, 100kΩ)
IBPB	PCI-3V	None
IBPBP#	PCI-3V	Pull-up resistor (50kΩ, 100kΩ)
IBPBD#	PCI-3V	Pull-down resistor (50kΩ, 100kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-up and pull-down resistances, refer to Table 1-7 and "A4.2.7."
*3: For the input buffer characteristics graphs, refer to "A4.2.2."

Table 6-12-2 Input Level Shifters (V_{DD} = 3.3V) (5V input also permitted)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2
IDC	LVTTL	None
IDCD#	LVTTL	Pull-down resistor (50kΩ, 100kΩ)
IDH	LVTTL Schmitt	None
IDHD#	LVTTL Schmitt	Pull-down resistor (50kΩ, 100kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-down resistances, refer to Table 1-7 and "A4.2.7."

6.4.2 Output Buffers

Table 6-13 shows I_{OL} and I_{OH} specifications for single power supply output buffers.

Table 6-13 I_{OL} and I_{OH} Specifications for Single Power Supply Voltages

Output Current	I_{OL}*1/I_{OH}*2	Unit
	V_{DD} = 3.3V	
Type S	0.1/-0.1	mA
Type M	1/-1	mA
Type 1	2/-2	mA
Type 2	6/-6	mA
Type 3	12/-12	mA

NOTE: *1: V_{OL} = 0.4V
*2: $V_{OH} = V_{DD} - 0.4V$

Tables 6-14-1 and 6-14-2 list the single power supply output buffers.

Table 6-14-1 Single Power Supply Output Buffers (V_{DD} = 3.3V)

Function	I_{OL}/I_{OH} *1 *2	Cell Name
Normal output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	OBST OBMT OB1T OB2T OB3T
Output for PCI	PCI-3V	OBPBT
Normal output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	OB1CT OB2CT OB3AT
Normal output for low noise	12mA/-12mA	OB3BT
3-state output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	TBST TBMT TB1T TB2T TB3T
3-state output for PCI	PCI-3V	TBPBT
3-state output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	TB1CT TB2CT TB3AT
3-state output for low noise	-12mA/12mA	TB3BT

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

Table 6-14-2 Single Power Supply N-Channel Open Drain Output Buffers (V_{DD} = 3.3V)

Function	I_{OL} *1 *2	Cell Name
Normal output	2mA 6mA 12mA	OD1T OD2T OD3T
High speed output	2mA 6mA	OD1CT OD2CT

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

6.4.3 Bi-directional Buffers

(1) Bi-directional buffers

Tables 6-15-1 to 6-15-3 list the single power supply bi-directional buffers.

Table 6-15-1 Single Power Supply Bi-directional Buffers (1/2) (V_{DD} = 3.3V)

Input Level	Function	I_{OL}/I_{OH} *1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
LVTTL	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	BCST BCMT BC1T BC2T BC3T	BCSD*T BCMD*T BC1D*T BC2D*T BC3D*T	BCSP*T BCMP*T BC1P*T BC2P*T BC3P*T
	Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	BC1CT BC2CT BC3AT	BC1CD*T BC2CD*T BC3AD*T	BC1CP*T BC2CP*T BC3AP*T
	Bi-directional output for low noise	12mA/-12mA	BC3BT	BC3BD*T	BC3BP*T
PCI-3V	Bi-directional output for PCI	PCI-3V	BPBT	BPBD*T	BPBP*T
LVTTL Schmitt	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	BHST BHMT BH1T BH2T BH3T	BHSD*T BHMD*T BH1D*T BH2D*T BH3D*T	BHSP*T BHMP*T BH1P*T BH2P*T BH3P*T
	Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	BH1CT BH2CT BH3AT	BH1CD*T BH2CD*T BH3AD*T	BH1CP*T BH2CP*T BH3AP*T
	Bi-directional output for low noise	12mA/-12mA	BH3BT	BH3BD*T	BH3BP*T

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 50kΩ or "2" for a resistance of 100kΩ.

Table 6-15-2 Single Power Supply Bi-directional Buffers (2/2) (V_{DD} = 3.3V)

Input Level	Function	I_{OL}/I_{OH} *1 *2	No Resistor	With Pull-down Resistor	With Pull-up Resistor
LVTTL	Bi-directional output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	BCMHT BC1HT BC2HT BC3HT	None	None
	Bi-directional output for high speed (with bus hold function)	2mA/-2mA 6mA/-6mA 12mA/-12mA	BC1CHT BC2CHT BC3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA	BC3BHT	None	None
LVTTL Schmitt	Bi-directional output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 12mA/-12mA	BHMHT BH1HT BH2HT BH3HT	None	None
	Bi-directional output for high speed (with bus hold function)	2mA/-2mA 6mA/-6mA 12mA/-12mA	BH1CHT BH2CHT BH3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA	BH3BHT	None	None

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

Table 6-15-3 Single Power Supply N-Channel Open Drain Bi-directional Buffers (V_{DD} = 3.3V)

Input Level	Function	I_{OL} *1 *2	Cell Name
LVTTL	Bi-directional output	2mA 6mA 12mA	BDC1T BDC2T BDC3T
	Bi-directional output for high speed	2mA 6mA	BDC1CT BDC2CT
LVTTL Schmitt	Bi-directional output	2mA 6mA 12mA	BDH1T BDH2T BDH3T
	Bi-directional output for high speed	2mA 6mA	BDH1CT BDH2CT

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

6.5 Fail-Safe I/O Buffers

6.5.1 Outline

The S1L50000 Series fail-safe buffers for single power supply designs provide the means for interfacing to voltage levels higher than specified value; no dedicated power supply interface is required.

6.5.2 Features

① No constraints apply to cell count and placement, allowing placement to suit requirements.

② No large current flows other than the input leakage current in the fail-safe buffer, even when an input signal exceeding the power supply voltage is applied while the power supply is on.

③ No large current flows other than the input leakage current in the fail-safe buffer, even when an external input signal is applied while the power is cut off.

④ LVTTL/LVTTL Schmitt input levels (V_{DD} = 3.3V) are available.

6.5.3 Notes on Use

① If a signal exceeding the power supply voltage is input in high output mode, a relatively large current will flow in the same way as with regular I/O buffers. Care must be taken because this also happens when an external pull-up resistor greater than the power supply voltage exists.

② Note that the signal voltage that can be applied to a fail-safe buffer must not exceed the absolute maximum rating.

6.5.4 Cell Listing

(1) Fail-safe input buffers

Tables 6-16-1 and 6-16-2 list the fail-safe input buffers.
Input buffers allowing 5V input without pull-up will be input level shifters.

① For single power supply

Table 6-16-1 Fail-Safe Input Buffers (V_{DD} = 3.3V) (5V input also permitted)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2*3
IBBP#	LVTTL	Pull-up resistor (50kΩ, 100kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-up and pull-down resistances, refer to Table 1-7 and "A4.2.7."
*3: For the input buffer characteristics graphs, refer to "A4.2.2."

② For dual power supplies

Table 6-16-2 Fail-Safe Input Buffers (LV_{DD} = 3.3V) (5V input also permitted)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2*3
LIBBP#	LVTTL	Pull-up resistor (50kΩ, 100kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-up and pull-down resistances, refer to Table 1-7 and "A4.2.7."
*3: For the input buffer characteristics graphs, refer to "A4.2.2."

(2) Fail-safe output buffers

Tables 6-17-1 and 6-17-2 list the fail-safe output buffers.

① For single power supply

Table 6-17-1 Fail-Safe Output Buffers (V_{DD} = 3.3V)

Function	I_{OL}/I_{OH} *1 *2	Cell Name
3-state output	2mA/-2mA 6mA/-6mA	TBF1 TBF2
3-state output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	TBF1C TBF2C TBF3A

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

② For dual power supplies

Table 6-17-2 Fail-Safe Output Buffers (LV_{DD} = 3.3V)

Function	I_{OL}/I_{OH} *1 *2	Cell Name
3-state output	2mA/-2mA 6mA/-6mA	LTBF1 LTBF2
3-state output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	LTBF1C LTBF2C LTBF3A

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."

(3) Fail-safe bi-directional buffers

Tables 6-18-1 and 6-18-2 list the fail-safe bi-directional buffers.

① For single power supply

Table 6-18-1 Fail-Safe Bi-directional Buffers (V_{DD} = 3.3V)

Input Level	Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
LVTTL	Bi-directional output	2mA/-2mA 6mA/-6mA	BB1 BB2	BB1D* BB2D*	BB1P* BB2P*
	Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	BB1C BB2C BB3A	BB1CD* BB2CD* BB3AD*	BB1CP* BB2CP* BB3AP*
LVTTL Schmitt	Bi-directional output	2mA/-2mA 6mA/-6mA	BG1 BG2	BG1D* BG2D*	BG1P* BG2P*
	Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	BG1C BG2C BG3A	BG1CD* BG2CD* BG3AD*	BG1CP* BG2CP* BG3AP*

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 50kΩ or "2" for a resistance of 100kΩ.

② For dual power supplies

Table 6-18-2 Fail-Safe Bi-directional Buffers (LV_{DD} = 3.3V)

Input Level	Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
LVTTL	Bi-directional output	2mA/-2mA 6mA/-6mA	LBB1 LBB2	LBB1D* LBB2D*	LBB1P* LBB2P*
	Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	LBB1C LBB2C LBB3A	LBB1CD* LBB2CD* LBB3AD*	LBB1CP* LBB2CP* LBB3AP*
LVTTL Schmitt	Bi-directional output	2mA/-2mA 6mA/-6mA	LBG1 LBG2	LBG1D* LBG2D*	LBG1P* LBG2P*
	Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	LBG1C LBG2C LBG3A	LBG1CD* LBG2CD* LBG3AD*	LBG1CP* LBG2CP* LBG3AP*

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 50kΩ or "2" for a resistance of 100kΩ.

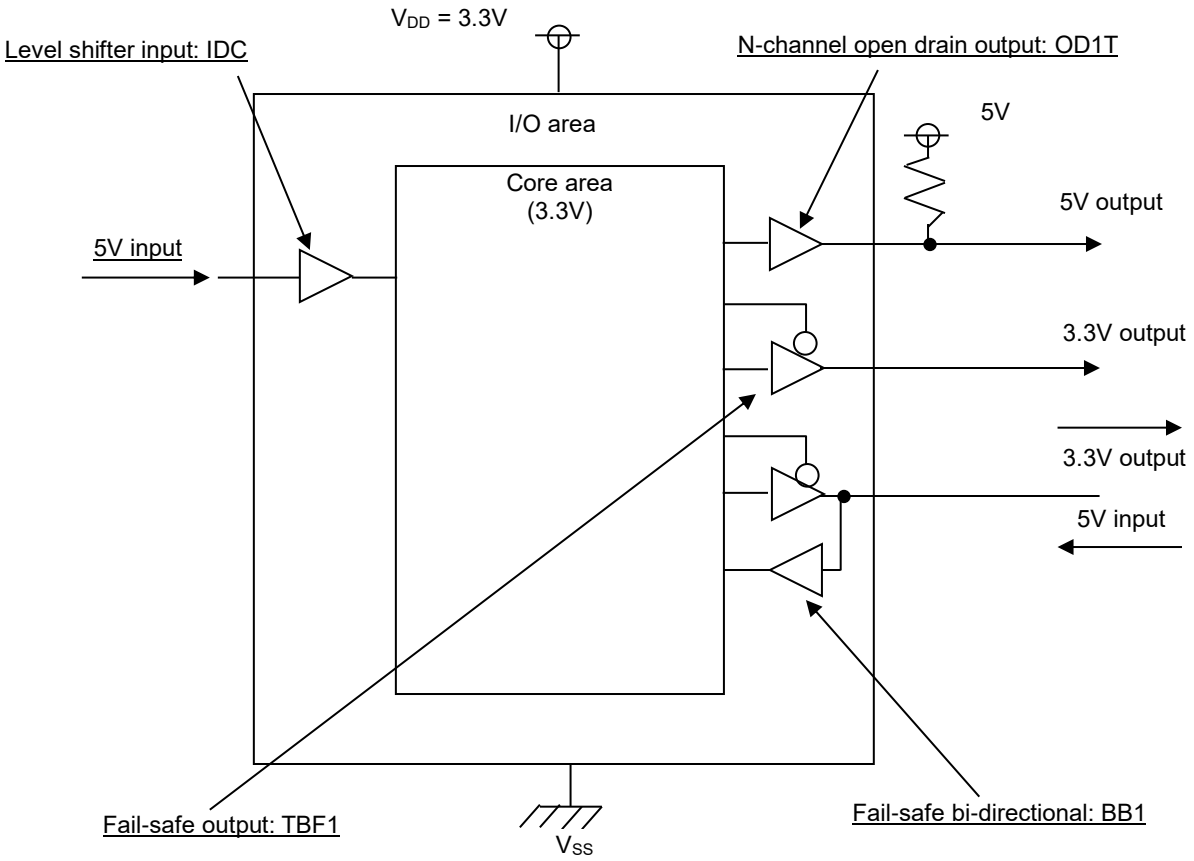


Figure 6-2 V_{DD} = 3.3V Fail-Safe Configuration Example

6.6 Gated I/O Buffers

6.6.1 Outline

The S1L50000 Series gated I/O buffers allow the pin input to be set to floating state—i.e., to the high impedance state—without using a pull-up or pull-down resistor circuit. The gated I/O cell can also cut off the high voltage power supply (HV_{DD}) in dual power supply designs. Buffers are available as types that cut off for a high level control signal and types that cut off for a low level control signal.

6.6.2 Features

(1) No constraints on cell count and placement provide the designer with great flexibility to meet the layout requirement.

(2) Possible to cut off the high voltage power supply (HV_{DD}) in dual power supply designs. However, special processing at Epson is needed for cutting off the high-level voltage supply. When doing so, please contact our sales representative.

(3) Possible to set the input to the high impedance state without using the pull-up or pull-down circuit.

(4) Two types of control signals are available: one for cutting off the current flow at the high level voltage and the other, at the low level voltage.

6.6.3 Notes on Use

(1) If the input changes to the high impedance state, use a control signal to cut off the input signal in advance. If the input changes from high impedance to 0 or 1, cancel the input signal cut-off after the change. A flow-through current may flow if this is not performed.

(2) Use a control signal to cut off the input signal before HV_{DD} is cut off. Likewise, if HV_{DD} turns on from cut-off, cancel the input signal cut-off once the power supply voltage has reached the rated level and the input signal has stabilized at 0 or 1.

(3) Because of the circuit configuration, the input level for gated I/O buffers with dual power supplies will be LV_{DD} CMOS level and not HV_{DD}.

6.6.4 Cell Listing

(1) Gated input buffers

Tables 6-19-1 and 6-19-2 list the gated input buffers.

① For single power supply

Table 6-19-1 Gated Input Buffers (V_{DD} = 3.3V)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2 *3
IBA IBAP# IBAD#	AND Type LVTTL	None Pull-up resistor (50kΩ, 100kΩ) Pull-down resistor (50kΩ, 100kΩ)
IBO IBOP# IBOD#	OR Type LVTTL	None Pull-up resistor (50kΩ, 100kΩ) Pull-down resistor (50kΩ, 100kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-up and pull-down resistances, refer to Table 1-7 and "A4.2.7."
*3: For the input buffer characteristics graphs, refer to "A4.2.2."

② For dual power supplies

Table 6-19-2 Gated Input Buffers (HV_{DD} = 5.0V, LV_{DD} = 3.3V)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2 *3
HIBA HIBAP# HIBAD#	AND Type TTL	None Pull-up resistor (60kΩ, 120kΩ) Pull-down resistor (60kΩ, 120kΩ)
HIBO HIBOP# HIBOD#	OR Type TTL	None Pull-up resistor (60kΩ, 120kΩ) Pull-down resistor (60kΩ, 120kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-up and pull-down resistances, refer to Table 1-6 and "A4.2.7."
*3: For the input buffer characteristics graphs, refer to "A4.2.2."

(2) Gated bi-directional buffers

Tables 6-20-1 and 6-20-2 list the gated bi-directional buffers.

① For single power supply

Table 6-20-1 Gated Bi-directional Buffers (V_{DD} = 3.3V)

Input Level		Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
LVTTL	AND Type	Bi-directional output	2mA/-2mA 6mA/-6mA 12mA/-12mA	BA1T BA2T BA3T	BA1D*T BA2D*T BA3D*T	BA1P*T BA2P*T BA3P*T
		Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	BA1CT BA2CT BA3AT	BA1CD*T BA2CD*T BA3AD*T	BA1CP*T BA2CP*T BA3AP*T
		Bi-directional output for low noise	12mA/-12mA	BA3BT	BA3BD*T	BA3BP*T
	OR Type	Bi-directional output	2mA/-2mA 6mA/-6mA 12mA/-12mA	BO1T BO2T BO3T	BO1D*T BO2D*T BO3D*T	BO1P*T BO2P*T BO3P*T
		Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	BO1CT BO2CT BO3AT	BO1CD*T BO2CD*T BO3AD*T	BO1CP*T BO2CP*T BO3AP*T
		Bi-directional output for low noise	12mA/-12mA	BO3BT	BO3BD*T	BO3BP*T

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.2.4 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 50kΩ or "2" for a resistance of 100kΩ.

② For dual power supplies

Table 6-20-2 Gated Bi-directional Buffers (HV_{DD} = 5.0V, LV_{DD} = 3.3V)

Input Level		Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
TTL	AND Type	Bi-directional output	3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HBA1T HBA2T HBA3T HBA4T	HBA1D*T HBA2D*T HBA3D*T HBA4D*T	HBA1P*T HBA2P*T HBA3P*T HBA4P*T
		Bi-directional output for high speed	12mA/-12mA 24mA/-12mA	HBA3AT HBA4AT	HBA3AD*T HBA4AD*T	HBA3AP*T HBA4AP*T
		Bi-directional output for low noise	12mA/-12mA 24mA/-12mA	HBA3BT HBA4BT	HBA3BD*T HBA4BD*T	HBA3BP*T HBA4BP*T
	OR Type	Bi-directional output	3mA/-3mA 8mA/-8mA 12mA/-12mA 24mA/-12mA	HBO1T HBO2T HBO3T HBO4T	HBO1D*T HBO2D*T HBO3D*T HBO4D*T	HBO1P*T HBO2P*T HBO3P*T HBO4P*T
		Bi-directional output for high speed	12mA/-12mA 24mA/-12mA	HBO3AT HBO4AT	HBO3AD*T HBO4AD*T	HBO3AP*T HBO4AP*T
		Bi-directional output for low noise	12mA/-12mA 24mA/-12mA	HBO3BT HBO4BT	HBO3BD*T HBO4BD*T	HBO3BP*T HBO4BP*T

NOTE: *1: V_{OL} = 0.4V, V_{OH} = HV_{DD} − 0.4V
*2: For output current characteristics, refer to the graphs in "A4.1.3 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 60kΩ or "2" for a resistance of 120kΩ.

Chapter 7 Notes on Pinout

This chapter discusses the points the designer needs to pay special attention when deciding package pinout and adding power supply pins to avoid malfunctions due to simultaneous switching of output buffers.

7.1 Estimating Power Supply Pin Count

The designer needs to estimate the power supply pin count according to the IC power consumption and output buffer count. Care must be taken especially for output buffers, as significant amount of transient current flows when they switch. The greater the output buffer drivability is, the larger transient current flows.

The following describes how to estimate the power supply pin count required for an IC in relation to the consumption current:

7.1.1 Single power supply

If the consumption current is I_{DD} [mA], the dual power supply pin count N_{IDD} is estimated as follows in relation to the consumption current:

$N_{IDD} \geq I_{DD} \div 50$ (pair): That is, up to 50mA can be supplied to one pair of V_{DD} and V_{SS} pins.

Notes: 1. At least one pair of power supply pins must be inserted in each side of the package. That is, at least 4 pairs of V_{DD} and V_{SS} pins are inserted for each package.
To obtain I_{DD}, calculate the power consumption using the formula discussed in "9.1 Calculating Power Consumption," and then divide the power consumption by the operating voltage.
2. If the output buffer is connected to DC load and current steadily flows, power supply pins need to be added. For details, contact our sales representative.

7.1.2 Dual-power supplies

The maximum allowable current for one pair of dual power supplies (both HV_{DD} and LV_{DD} power supplies) is the same as single power supply. Required number of power supply pairs must be separately calculated for HV_{DD} and LV_{DD}.

(1) HV_{DD} power supply pin count

If the HV_{DD} consumption current is I_{DD} (HV_{DD}) [mA], the power supply pin count N_{IDD} (HV_{DD}) for this consumption current is estimated as follows:

N_{IDD} (HV_{DD}) $\geq I_{DD}$ (HV_{DD})/50 * That is, up to 50mA can be supplied to each pin.

(2) LV_{DD} power supply pin count

If the LV_{DD} consumption current is I_{DD} (LV_{DD}) [mA], the power supply pin count N_{IDD} (LV_{DD}) for this current consumption is estimated as follows:

N_{IDD} (LV_{DD}) $\geq I_{DD}$ (LV_{DD}) / 50 * That is, up to 50mA can be supplied to each pin.

(3) V_{SS} power supply pin count

N_{IDD} (V_{SS}) $\geq$ {I_{DD} (HV_{DD}) + I_{DD} (LV_{DD})} / 50 * That is, up to 50mA can be supplied to each pin.

Notes: 1. At least one pin of HV_{DD}, LV_{DD}, and V_{SS} power supplies must be inserted in each side of the package. That is, at least 4 pins of each power supply are inserted for each package.
I_{DD} is the value obtained by dividing the power consumption calculated using the formula in "9.1 Calculating Power Consumption" by the operating voltage.
2. When the output buffer is connected to DC load and current steadily flows, power supply pins need to be inserted. For details, contact our sales representative.
3. When adding power supply pins to cope with simultaneous output switching, add HV_{DD}, LV_{DD}, and V_{SS} power pins separately for HV_{DD} and LV_{DD} output buffers.

7.2 Simultaneous Switching and Power Supply Addition

7.2.1 Notes on Dual Power Supply Usage (HV_{DD} = 5.0V, LV_{DD} = 3.3V)

Switching multiple output buffers simultaneously may generate large noise.

When a number of output buffers simultaneously switch, add power supplies referring to Tables 7-1 to 7-4 to prevent noise-induced errors.

Table 7-1 V_{SS} Power Supply Addition for Output Buffer Simultaneous Switching (HV_{DD} = 5.0V)

Output drivability (I_{OL})	Simultaneous switching count	Number of power supplies to add		
		CL ≤ 50pF	CL ≤ 100pF	CL ≤ 200pF
8mA	≤ 8	0	1	2
	≤ 16	1	2	4
	≤ 24	1	3	6
	≤ 32	2	4	8
12mA	≤ 8	1	2	3
	≤ 16	2	3	5
	≤ 24	2	5	7
	≤ 32	3	6	12
24mA & PCI	≤ 8	2	3	4
	≤ 16	3	4	6
	≤ 24	5	6	8
	≤ 32	6	8	16

Table 7-2 HV_{DD} Power Supply Addition for Output Buffer Simultaneous Switching (HV_{DD} = 5.0V)

Output drivability (I_{OL})	Simultaneous switching count	Number of power supplies to add		
		CL ≤ 50pF	CL ≤ 100pF	CL ≤ 200pF
8mA	≤ 8	0	1	1
	≤ 16	1	1	3
	≤ 24	1	2	4
	≤ 32	1	3	5
12mA & PCI	≤ 8	1	2	3
	≤ 16	2	3	4
	≤ 24	3	4	5
	≤ 32	4	6	10

7.2.2 Notes on Single Power Supply Usage

Table 7-3 V_{SS} Power Supply Addition for Output Buffer Simultaneous Switching (V_{DD} = 3.3V)

Output drivability (I_{OL})	Simultaneous switching count	Number of power supplies to add		
		CL ≤ 50pF	CL ≤ 100pF	CL ≤ 200pF
6mA	≤ 8	0	1	2
	≤ 16	1	2	3
	≤ 24	1	2	4
	≤ 32	2	3	5
12mA	≤ 8	1	2	2
	≤ 16	2	2	3
	≤ 24	2	3	5
	≤ 32	2	4	8
PCI	≤ 8	1	2	3
	≤ 16	2	3	4
	≤ 24	3	4	5
	≤ 32	4	5	10

Table 7-4 V_{DD} Power Supply Addition for Output Buffer Simultaneous Switching (V_{DD} = 3.3V)

Output drivability (I_{OL})	Simultaneous switching count	Number of power supplies to add		
		CL ≤ 50pF	CL ≤ 100pF	CL ≤ 200pF
6mA	≤ 8	0	1	1
	≤ 16	1	1	2
	≤ 24	1	2	3
	≤ 32	1	2	3
12mA & PCI	≤ 8	1	2	2
	≤ 16	2	2	3
	≤ 24	2	3	3
	≤ 32	3	3	6

7.3 Notes on Pinout

After selecting the right device to suit a particular design, determine the package pinout. The power supply pin information and usable I/O pin count will then be estimated.

Please submit the pinout to Epson together with the development start order in the form of a "pinout table" (format unspecified) describing the pinout. Epson will then proceed with the placement and routing process based on the pinout table received from the customer.

7.3.1 Fixed Location Power Supply Pins

Depending on package combinations, some pins may be used only as power supply pins. For more information, please contact our sales representative.

7.3.2 Notes on Pinout

The pinout sometimes affects the IC logic functions and electrical characteristics. Also there may be constraints on pinout because of the IC packaging and the cell or master configurations. The following describes points that must be noted when considering the pinout:

(1) Power supply current (I_{DD}, I_{SS})

Power supply current (I_{DD}, I_{SS}) defines the allowable supply current flowing to the power supply pins when the device is active. If the current exceeding this allowable value flows, the current density in the power lines within the IC becomes too high, and this may lower the IC reliability and even destroys the device. Also, the IC internal voltage either increases or decreases depending on the voltage generated by the current and wire resistance. This voltage change induces functional errors and inversely affects the DC or AC characteristics.

To prevent these problems, the current density and power line impedance need to be lowered. To achieve this, estimate the power consumption in the design phase, and ensure enough power supply pins to prevent excessive current from flowing through each power supply pin. For power supply pins, refer to "7.1 Estimating Power Supply Pin Count." These power supply pins should not be placed close to each other, but should be scattered.

The total power supply pin count should include the power supply pins discussed above and additional power supply pins to reduce noise. For additional power supply pin count, see "7.2 Simultaneous Switching and Power Supply Addition."

(2) Noise caused by output buffer operation

The following two types of noise occur due to the output buffer operation. To reduce these types of noise, one possible solution is to have as many power supplies as possible.

① Noise generated in power supply lines

Noise generated in power supply lines becomes an issue when a large number of output pins simultaneously switch; and it changes the IC input threshold level, which will end up with malfunctions. The noise in power supply lines occurs when large current flows through the power supply lines by the simultaneous switching of output buffers.

Inductance element affects power supply noise. The IC equivalent circuit is illustrated in Figure 7-1. In this circuit, when the output changes from high to low, the current flows into the IC from the output pin through the equivalent inductance L2, which is due to the IC package, etc. When this happens, the equivalent inductance L2 changes the voltage of IC internal V_{SS} power line. The voltage change in this V_{SS} power line is the noise that occurs to the power line. This noise is generated mainly by the equivalent inductance L2, and thus the quicker the power supply current changes, the larger noise occurs.

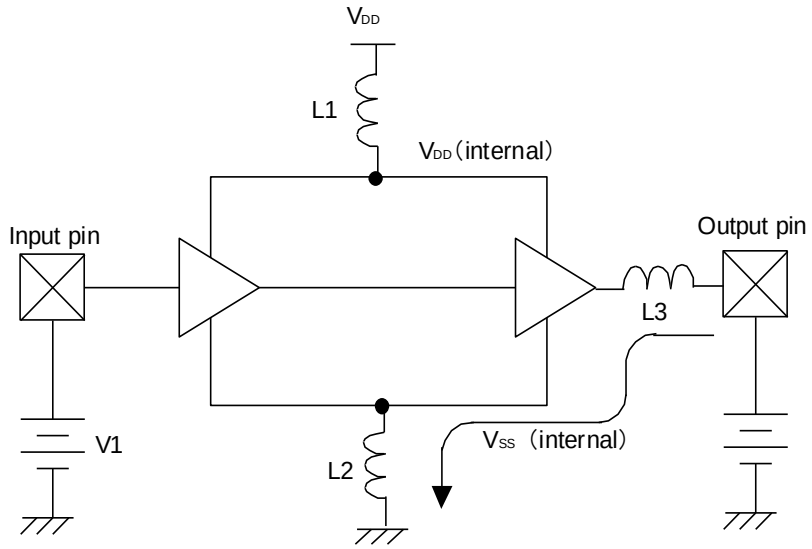


Figure 7-1 IC Equivalent Circuit

② Overshoot, undershoot, and ringing

Noise such as overshoot, undershoot and ringing, occurs due to the equivalent inductance of output pins. The L3 shown in Figure 7-1 is this equivalent inductance. Since inductance has the property to save energy, whether the output goes low or high, the saved energy makes the overshoot or undershoot proportional to the amount of flowing electric current and the rate of current change.

The most effective way to reduce overshoot or undershoot is use of output buffers with small drivability. As the load capacitance increases, overshoot or undershoot noise tends to become smaller. Therefore, care must be taken when using cells with high drivability.

(3) Separating input and output pins

Separating the group of input pins from that of output pins is an important pinout technique to reduce noise effect.

Input pins and bi-directional pins in the input state are vulnerable to noise, and thus they should not be placed close to output pin. Separate the groups of input pins, output pins and bi-directional pins each other by power supply pins (V_{DD}, V_{SS}). (Figure 7-2)

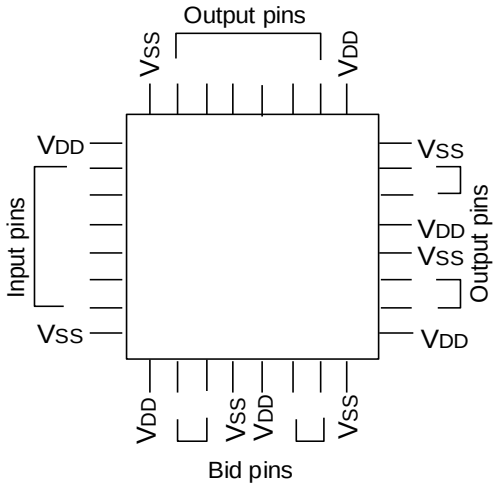


Figure 7-2 Example of Separating Input and Output Pins

(4) Critical signals

Pay attention to the following points for the pinout of critical signal pins such as clock input and high-speed output pins.

① Do not place clock and reset pins, that are vulnerable to noise, close to the output pins, but place them close to the power supply pins. (Figure 7-3)

② Place the oscillator circuit input and output pins (OSCIN, OSCOUNT) close to each other and enclose them by the power supply pins (V_{DD} and V_{SS}). Also, do not place the output pins synchronous to the oscillator circuit close to the output pins. (Figure 7-4)

③ Place the high-speed input and output pins in the middle of the IC (package) side. (Figure 7-3)

④ When the delay from an input pin to an output pin is hard to meet the customer's specification, place these input and output pins close to each other. (Figure 7-3)

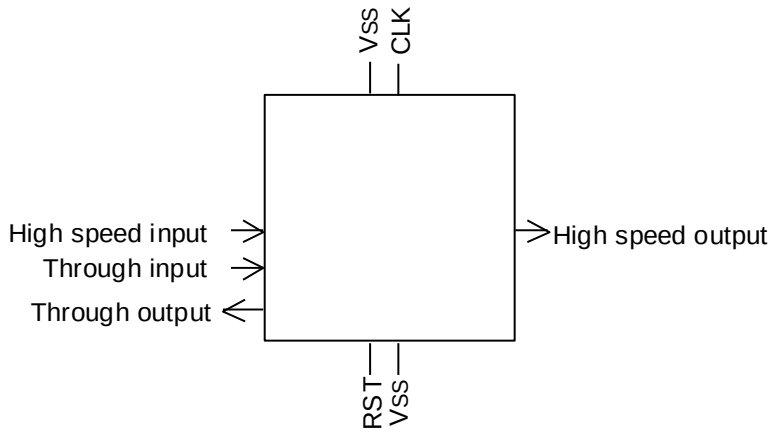


Figure 7-3 Critical Signal Pinout Example 1

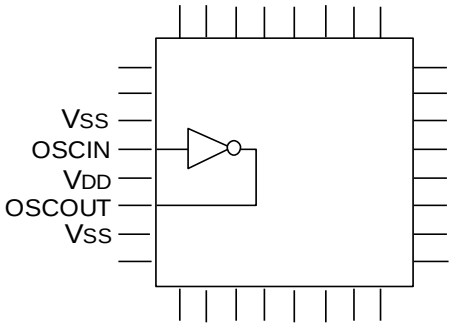


Figure 7-4 Critical Signal Pinout Example 2

(5) Pull-up/pull-down resistance input

Pull-up/pull-down resistance is relatively large, from some tens of kilo-ohm to some hundreds of kilo-ohm, and dependent on the power supply voltage due to the resistor structure.

Note the following points when using these pins in the open state—for example, for testing purposes. They are susceptible to noise and may cause malfunctions.

① Place pull-up/pull-down resistor pins as far away from high-speed input pins (clock input pins, etc.) as possible. (Figure 7-5)

② Place pull-up/pull-down resistor pins away from the output pins (especially from the high current output pins). (Figure 7-6)

Consider the following points in addition to notes on pinout:

- Perform pull-up or pull-down process on the printed circuit board wherever possible.
- Select pins with the smallest possible resistance.

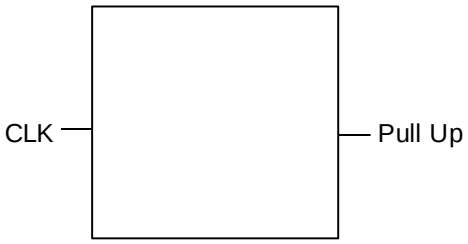


Figure 7-5 Pull-up and Pull-down Pinout Example 1

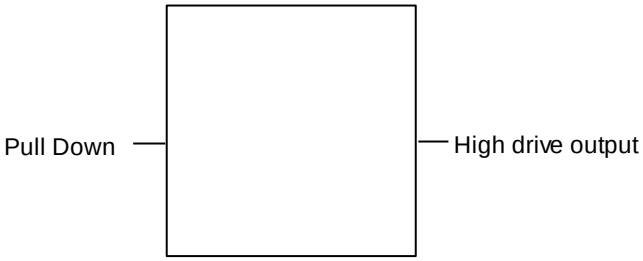


Figure 7-6 Pull-up and Pull-down Pinout Example 2

(6) Simultaneous output switching

Noise caused by simultaneous switching of output pins induces IC malfunctions. When switching many output pins simultaneously, add power supply pins to the group of output pins to avoid errors by noise. As for the number of required power supply pins and how to place additional power pins, refer to "7.2 Simultaneous Switching and Power Supply Addition." (Figure 7-7)

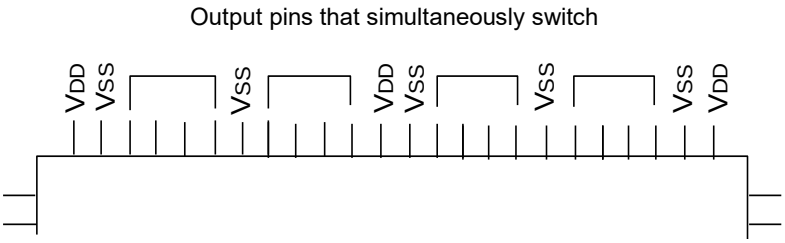


Figure 7-7 Example of Adding Power Supply Pins

Simultaneous signal switching of output buffers can be reduced by inserting a delay cell at the input of the output buffers in one group. This reduces noise as well. (Figure 7-8)

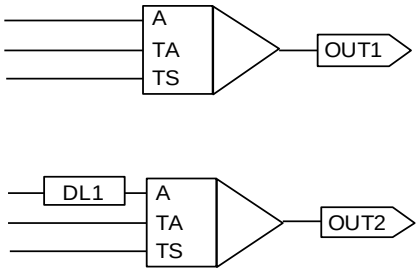


Figure 7-8 Example of Adding a Delay Cell

(7) High current drivers

When used with high current drivers, the pinout must comply with the following constraints:

① Constraint on power supply enhancement

Since high current drivers have high drivability, the noise that would occur when output buffers are active is also large, sometimes causing malfunctions to IC.

When using high current drivers, place the power supply pins close to the driver pins to secure power supply. (Figure 7-9)

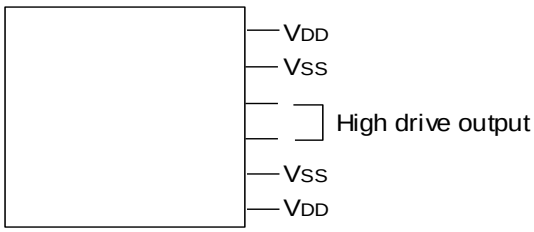


Figure 7-9 Example of Power Supply Enhancement

(8) Other notes

① NC pins (non-connection)

Do not connect anything to the NC pin.

7.3.3 Recommended Pinout

The pinout is important to have IC devices function correctly. The following is a pinout example that meets the constraints discussed above (Figure 7-10). Determine the pinout referring to the following example.

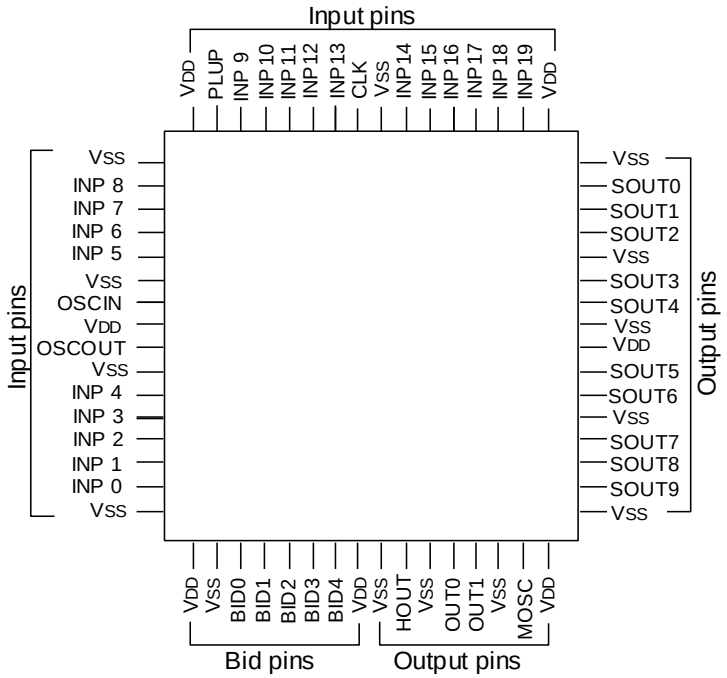


Figure 7-10 Recommended Pinout Example

The input pins are placed at the upper and left sides of the package, the output pins that simultaneously switch are placed at the right side, and bi-directional and other output pins are placed at the lower side of the package.

Table 7-5 Description of Pinout Example

Place	Pin Name	Pin Name Description	Pinout Description
Upper Side	PLUP	Pull-up input pin	Place in the location where noise effect is small
	CLK	Clock input pin	Place in the middle of the package side, and close to the power supply pin
Left Side	OSCIN	Oscillator pin	Place in the middle of the package side, and close to the power supply pin
	OSCOUT		Place in the middle of the package side, and close to the power supply pin
	INP0–19	Input pins	Separate from other pins by the power supply pin
Right Side	SOUT0–9	Simultaneous switching output pins	Separate from other pins by the power supply pin, and add power supply pins
Lower Side	BID0–4	Bi-directional pins	Separate from other pins by the power supply pin
	MOSC	Oscillation monitor output pin	Place away from the oscillator pin, and close to the power supply pin
	HOUT	High-drivability output pin	Place close to the power supply pin
	OUT01	Output pin	Separate from other pins by the power supply pin
All Sides	V_{DD}	V_{DD} power supply pin	
	V_{SS}	V_{SS} (GND) power supply pin	

Chapter 8 RAM Specifications

The S1L50000 Series supports asynchronous 1-port/2-port RAM and synchronous 1-port/2-port RAM. Please contact our sales representative if you need synchronous RAM.

8.1 Asynchronous 1-port RAM

8.1.1 Features

(1) Asynchronous

(2) Fully static operation

(3) One address port (shared read/write), one input data port, one output data port

(4) 8- to 256-word deep, configurable in 4-word increments
1- to 32-bit wide, configurable in 1-bit increments

(5) Maximum size: 8K bits/module

8.1.2 Word-Bit Configurations and RAM cell names

Table 8-1 shows the RAM cell names for typical Word/Bit configurations. The RAM cell names are determined the Word/Bit configuration according to the following rules.

1port RAM “U XXX YY” XXX: Word (Hex), YY: Bit (Hex)

If you need an asynchronous RAM whose word/bit configuration exceeds the configuration range, please configure it by combining multiple asynchronous RAMs.

Table 8-1 Asynchronous 1-port RAM cell name examples

Bit count / Word count	4 Bit	8 Bit	16 Bit	32 Bit
32 Word	U02004	U02008	U02010	U02020
64 Word	U04004	U04008	U04010	U04020
128 Word	U08004	U08008	U08010	U08020
256 Word	U10004	U10008	U10010	U10020

8.1.3 RAM size

The X and Y direction sizes of the RAM and the number of BCs to be used are calculated using the following formula.

X direction size: RX = Word + Bit/2 + 13

Y direction size: RY = 2 × Bit + 10

BC count: RAMBCS = RX × RX

Table 8-2 Asynchronous 1-port RAM cell BC count examples

Bit count / Word count	4 Bit	8 Bit	16 Bit	32 Bit
32 Word	846 (47 × 18)	1,274 (49 × 26)	2,226 (53 × 42)	4,514 (61 × 74)
64 Word	1,422 (79 × 18)	2,106 (81 × 26)	3,570 (85 × 42)	6,882 (93 × 74)
128 Word	2,574 (143 × 18)	3,770 (145 × 26)	6,258 (149 × 42)	11,618 (157 × 74)
256 Word	4,878 (271 × 18)	7,098 (273 × 26)	11,634 (277 × 42)	21,090 (285 × 74)

8.1.4 Function Descriptions

Table 8-3-1 Asynchronous 1-port RAM Signal Descriptions

Signal name	I/O	Function
CS	IN	Chip select signal, H: RAM active
RW	IN	Read/Write signal, H: Read, L: Write
A0, A1, ..., A (m-1)	IN	Read/Write address port, A0 : LSB
D0, D1, ..., D (n-1)	IN	Data input port, D0: LSB
Y0, Y1, ..., Y (n-1)	OUT	Data output port, Y0: LSB

Table 8-3-2 Asynchronous 1-port RAM Truth Table

CS	RW	A0, A1, ..., A (m-1)	Y0, Y1, ..., Y (n-1)	Mode
0	X	X	Unknown	Standby
1	0	Stable	Unknown	Write
1	1	Stable	Read data	Read

X: High or Low

(1) Data read

Set address with CS and RW held High to read data.

(2) Data write

There are two ways to write data:

(1) Set address with CS held High, and input Low-level pulse to RW.

(2) Set address with RW held Low, and input High-level pulse to CS.

In both cases, the RAM latches the data at the falling edge of the pulse.

(3) Standby state

When CS is Low, the 1-port RAM goes standby and only holds data. The current that flows through the RAM is only leakage current and the consumption current is almost 0.

8.1.5 Timing Chart of Asynchronous 1-port RAM

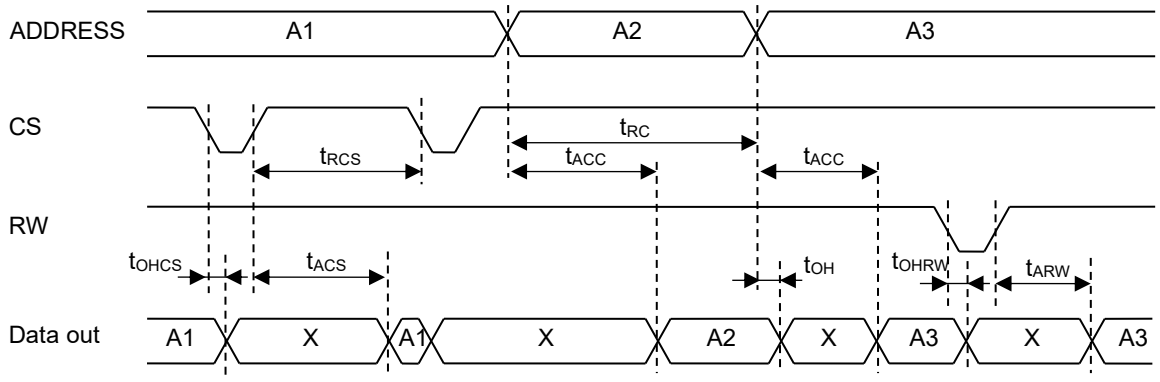


Figure 8-1 Read Cycle

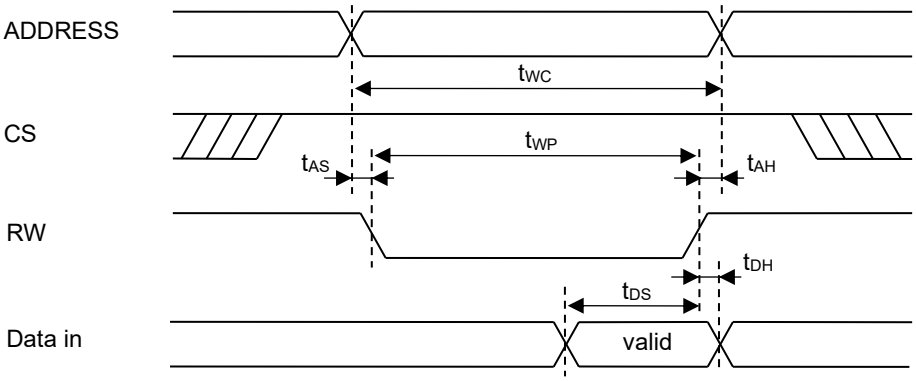


Figure 8-2 Write Cycle (RW Control)

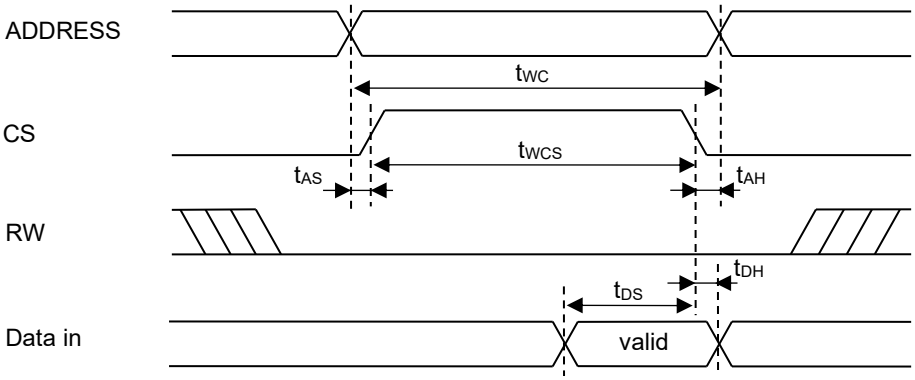


Figure 8-3 Write Cycle (CS Control)

8.2 Asynchronous 2-port RAM

8.2.1 Features

(1) Asynchronous

(2) Fully static operation

(3) Two address ports (separate read/write), one input data port, one output data port

(4) 8- to 256-word deep, configurable in 4-word increments
1- to 32-bit wide, configurable in 1-bit increments

(5) Maximum size: 8K bits/module

8.2.2 Word-Bit Configurations and RAM cell names

Table 8-4 shows the RAM cell names for typical Word/Bit configurations. The RAM cell names are determined the Word/Bit configuration according to the following rules.

2port RAM "V XXX YY" XXX: Word (Hex), YY: Bit (Hex)

Table 8-4 2-port RAM Simulation Models with Different Word-Bit Configurations

Bit count / Word count	4 Bit	8 Bit	16 Bit	32 Bit
32 Word	V02004	V02008	V02010	V02020
64 Word	V04004	V04008	V04010	V04020
128 Word	V08004	V08008	V08010	V08020
256 Word	V10004	V10008	V10010	V10020

8.2.3 RAM size

The X and Y direction sizes of the RAM and the number of BCs to be used are calculated using the following formula.

X direction size: RX = Word + Bit/2 + 13

Y direction size: RY = 2 × Bit + 14

BC count: RAMBCS = RX × RX

Table 8-5 Asynchronous 2-port RAM cell BC count examples

Bit count / Word count	4 Bit	8 Bit	16 Bit	32 Bit
32 Word	1,034 (47×22)	1,470 (49×30)	2,438 (53×46)	4,758 (61×78)
64 Word	1,738 (79×22)	2,430 (81×30)	3,910 (85×46)	7,254 (93×78)
128 Word	3,146 (143×22)	4,350 (145×30)	6,854 (149×46)	12,246 (157×78)
256 Word	5,962 (271×22)	8,190 (273×30)	12,742 (277×46)	22,230 (285×78)

8.2.4 Function Descriptions

Table 8-6-1 Asynchronous 2-port RAM Signal Descriptions

Signal name	I/O	Function
CS	IN	Chip select signal, H: RAM active
RD	IN	Read signal, H: Read enable
WR	IN	Write signal, H: Write enable
RA0, ... RA (m-1)	IN	Read address port, RA0: LSB
WA0, ... WA (m-1)	IN	Write address port, WA0: LSB
D0, D1, ... D (n-1)	IN	Data input port, D0: LSB
Y0, Y1, ... Y (n-1)	OUT	Data output port, Y0: LSB

Table 8-6-2 Asynchronous 2-port RAM Truth Table

CS	RD	WR	RA0, ..., RA (n-1)	WA0, ..., WA (m-1)	Y0, ..., Y (n-1)	Mode
0	X	X	X	X	Unknown	Standby
1	0	0	X	X	Unknown	Standby
1	0	1	X	Stable	Unknown	Write
1	1	0	Stable	X	Read data	Read
1	1	1	Stable	Stable	Read data	Read & Write

X: High or Low

(1) Data read

Set address with CS and RD held High to read data.

(2) Data write

There are two ways to write data:

① Set address with CS held High, and input High-level pulse to WR.

② Set address with WR held High, and input High-level pulse to CS.

(3) Data read and write

Simultaneous read and write is possible using read and write addresses, though simultaneous read and write access to the same address is prohibited. As described in Section “8.3 Delay parameters” the read cycle access time is applicable to the data for which write operation is finished.

(4) Standby state

In the following conditions, 2-port RAM goes standby and only holds data. The current that flows through the RAM is only leakage current and the consumption current is almost 0.

① CS is Low.

② CS is High, RD and WR are Low.

8.2.5 Timing Chart of Asynchronous 2-port RAM

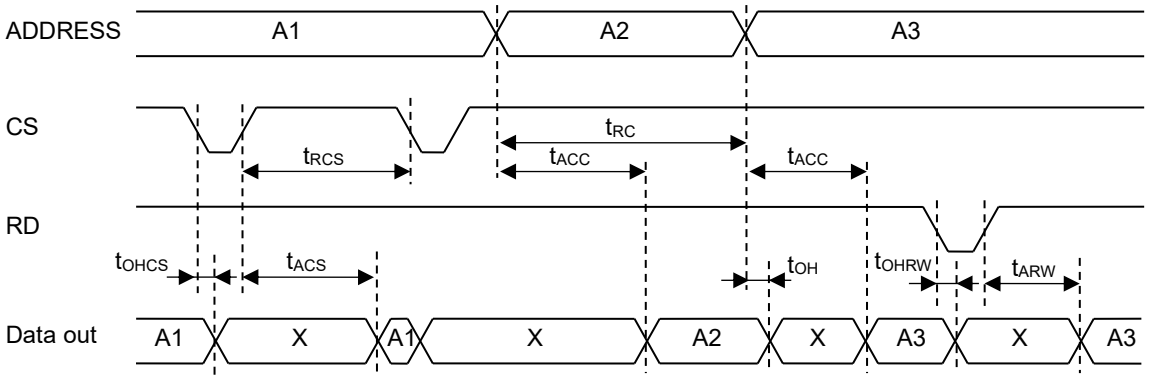


Figure 8-4 Read Cycle

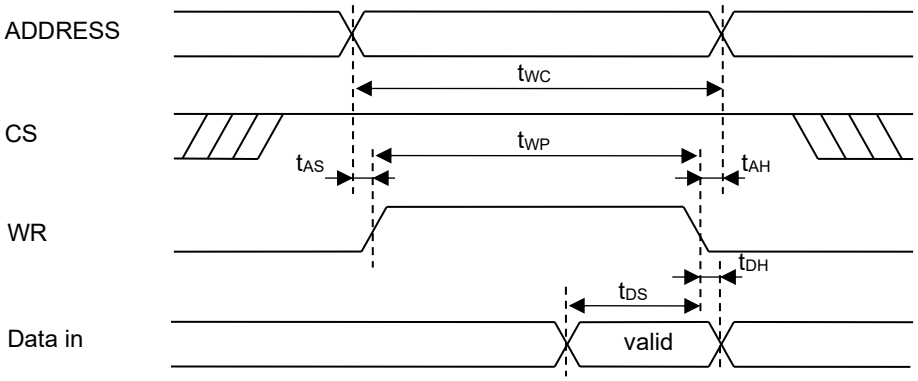


Figure 8-5 Write Cycle (WR Control)

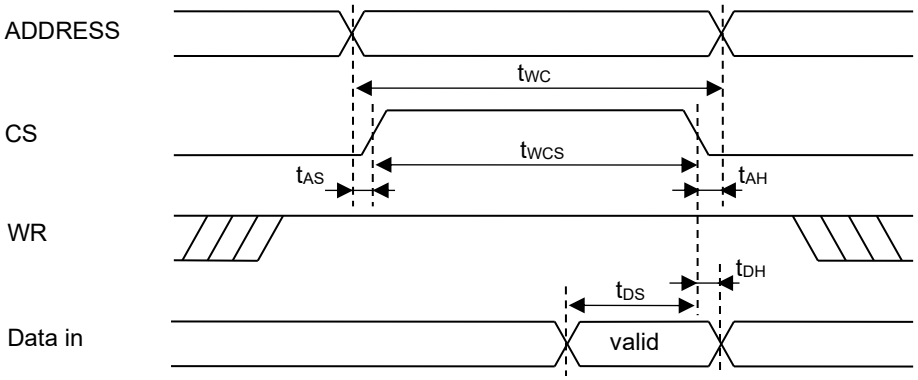


Figure 8-6 Write Cycle (CS Control)

8.3 Delay Parameters of Asynchronous RAM

The delay parameters of RAM change depending on the word-bit configuration, and we provide a simulation model for each word-bit configuration.

Here we describe the delay prameters of 1-port/2-port RAM with typical word-bit configurations. For detailed delay parameters of each RAM, please refer to the library we provide.

8.3.1 3.3V Specifications (V_{DD} = 3.3V ±0.3V, T_a = -40 to +85°C)

Table 8-7-1 Asynchronous 1-port/2-port RAM Read Cycle (1/2)

Parameter	Symbol	32word x 16bit U/V02010		32word x 32bit U/V02020		64word x 16bit U/V04010		64word x 32bit U/V04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	4.35	—	4.77	—	5.19	—	5.61	—	ns
Address access time	t_{ACC}	—	4.35	—	4.77	—	5.19	—	5.61	
CS access time	t_{ACS}	—	4.35	—	4.77	—	5.19	—	5.61	
RW access time	t_{ARW}	—	4.35	—	4.77	—	5.19	—	5.61	
CS active time	t_{RCS}	4.35	—	4.77	—	5.19	—	5.61	—	
Output hold time after address change	t_{OH}	0.08	—	0.14	—	0.08	—	0.14	—	
Output hold time after CS is disabled	t_{OHCS}	0.08	—	0.14	—	0.08	—	0.14	—	
Output hold time after RW is disabled	t_{OHRW}	0.08	—	0.14	—	0.08	—	0.14	—	

Table 8-7-2 Asynchronous 1-port/2-port RAM Read Cycle (2/2)

Parameter	Symbol	128word x 16bit U/V08010		128word x 32bit U/V08020		256word x 16bit U/V10010		256word x 32bit U/V10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	6.86	—	6.86	—	10.22	—	10.64	—	ns
Address access time	t_{ACC}	—	6.86	—	6.86	—	10.22	—	10.64	
CS access time	t_{ACS}	—	6.86	—	6.86	—	10.22	—	10.64	
RW access time	t_{ARW}	—	6.86	—	6.86	—	10.22	—	10.64	
CS active time	t_{RCS}	6.86	—	4.77	—	10.22	—	10.64	—	
Output hold time after address change	t_{OH}	0.08	—	0.14	—	0.08	—	0.14	—	
Output hold time after CS is disabled	t_{OHCS}	0.08	—	0.14	—	0.08	—	0.14	—	
Output hold time after RW is disabled	t_{OHRW}	0.08	—	0.14	—	0.08	—	0.14	—	

Table 8-7-3 Asynchronous 1-port/2-port RAM Write Cycle (1/2)

Parameter	Symbol	32word x 16bit U/V02010		32word x 32bit U/V02020		64word x 16bit U/V04010		64word x 32bit U/V04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.82	—	5.07	—	3.93	—	5.17	—	ns
Write pulse width	t_{WP}	1.87	—	3.11	—	1.91	—	3.16	—	
CS active time	t_{WCS}	1.87	—	3.11	—	1.91	—	3.16	—	
Address setup time	t_{AS}	0.63	—	0.63	—	0.68	—	0.68	—	
Address hold time	T_{AH}	1.33	—	1.33	—	1.33	—	1.33	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	2.33	—	3.33	—	2.37	—	3.37	—	

Table 8-7-4 Asynchronous 1-port/2-port RAM Write Cycle (2/2)

Parameter	Symbol	128word x 16bit U/V08010		128word x 32bit U/V08020		256word x 16bit U/V10010		256word x 32bit U/V10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	4.15	—	5.40	—	4.65	—	5.89	—	ns
Write pulse width	t_{WP}	2.02	—	3.27	—	2.29	—	3.54	—	
CS active time	t_{WCS}	2.02	—	3.27	—	2.29	—	3.54	—	
Address setup time	t_{AS}	0.80	—	0.80	—	1.02	—	1.02	—	
Address hold time	T_{AH}	1.33	—	1.33	—	1.33	—	1.33	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	2.46	—	3.46	—	2.63	—	3.63	—	

8.4 Estimation of asynchronous RAM installation

The X -Y dimensions of the place where a RAM is going to be embedded must exceed the RAM size, in terms of the number of basic cells used.

When multiple RAMs are used, they should be placed next to each other. In the formula mentioned earlier, wiring area around the RAM is included, and thus to see whether the RAM block is embeddable not, simply add the RX and RY sizes. For each master's basic cell count in the X and Y directions, see Table 1-1.

The following is an example to see if S1L50282 and S1L50752 can integrate 4 cells of 1-port RAM 256-word deep and 8-bit wide.

As shown in Figure 8-1, the RAM layout size is estimated as follows:

X direction: 273 BCs
Y direction: 104 BCs

Therefore:

S1L50282 with BC counts in (X, Y) directions = (319, 90), and thus the RAM block is not embeddable.
S1L50752 with BC counts in (X, Y) directions = (519, 146), and thus the RAM block is embeddable.

Use the following formula to calculate the BC count available for random logic excluding RAM.

0.9 × cell utilization × (total embedded BC count per master − RAM BC count)

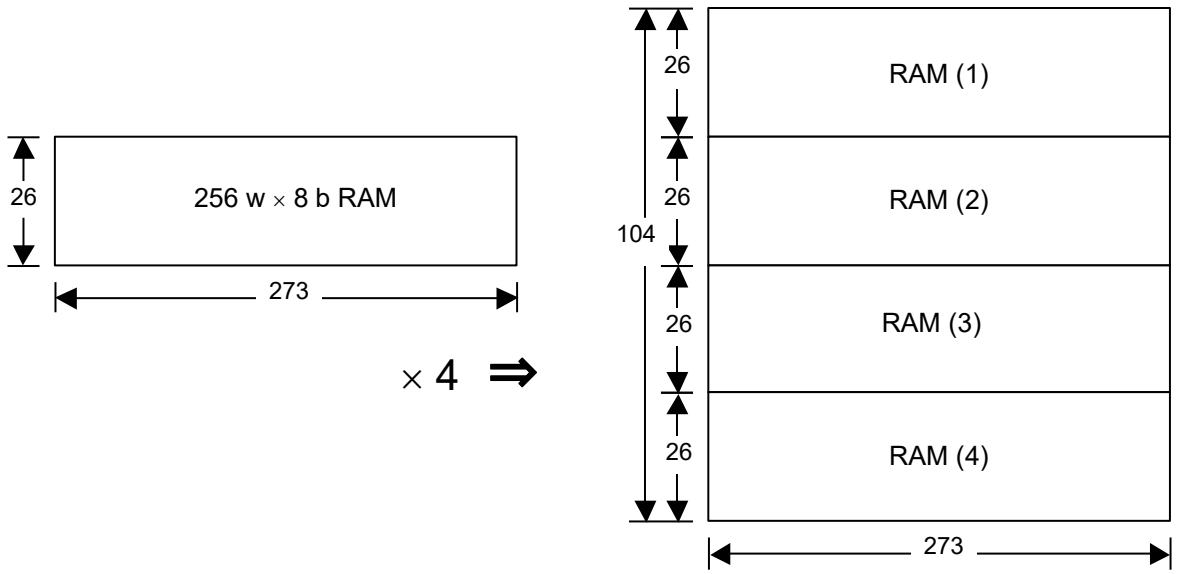


Figure 8-7 RAM Layout Example

8.5 Access to Invalid Addresses

If the RAM has 48- or 88-word deep configuration, access to invalid addresses may occur.

If an invalid address is accessed to read data in the actual IC, all word lines go to the off state and all bit lines go floating. Access to invalid addresses is therefore prohibited for the following reasons:

(1) Read operation with all bit lines floating outputs unknown to all the RAM output bits.

(2) Read operation with all bit lines floating generates a current flow path in the circuit. The value of this current varies depending on the RAM size or configuration; but it deviates the IC's dynamic and static current values from the specified values.

In the logic simulation, invalid addresses are checked at the rising time of the clock signal in the read/write operation, and if an invalid address is accessed, a timing error is output.

Chapter 9 Calculating Total Power Consumption

The power consumption values calculated in this chapter are not guaranteed figures and should be used strictly for reference purposes. Calculate power consumption as a reference for determining whether the power consumption is within the allowable range.

9.1 Calculating Power Consumption

The power consumption is dependent on operating frequency, load capacitance, and power supply (except special circuits with steady state currents).

To estimate IC total power consumption, obtain the power consumption of each block in the internal circuit first, and add them up. Then obtain the power consumption of input and output buffers, and add up these values, too.

9.1.1 Power Consumption Calculation for Dual Power Supplies

Calculating the power consumption for dual power supplies requires calculating the power consumption separately for the HV_{DD} and LV_{DD} circuits.

Total power consumption P_{total} is calculated using the following formula:

$P_{total} = P_{int} + P_i(HV_{DD}) + P_i(LV_{DD}) + P_o(HV_{DD}) + P_o(LV_{DD})$

where

P_{int}: Power consumption of internal circuits
P_i: Power consumption of input buffers
P_o: Power consumption of output buffers

(1) Internal cell power consumption (P_{int})

$$P_{int} = \sum_{i=1}^{K} \{(Nb \times U) \times fi \times Spi \times Kpint\} \text{ [W]}$$

where

Nb: Total number of basic cells
U: Cell utilization ratio
K: Total number of internal cells
fi: Ith operating frequency [MHz]
Spi: Ratio of the number of basic cells operating at operating frequency fi [MHz] to the total number of cells (Depends on system details; should ideally be 20% to 30%.)
Kpint: Power consumption per BC
(Table 9-1 shows the values corresponding to LV_{DD}.)

Table 9-1 S1L50000 Series Dual Power Supply Kpint per BC

LV_{DD} (TYP)	Kpi
3.3V	0.70µW/MHz

(2) Input buffer (P_i) power consumption ($P_i(HV_{DD})$ and $P_i(LV_{DD})$)

If the HV_{DD} power consumption is $P_i(HV_{DD})$ and LV_{DD} power consumption is $P_i(LV_{DD})$, the input buffer power consumption will be the sum of the frequencies f [MHz] of the signals input to each buffer multiplied by Kpi [µW/MHz].

$$P_i(HV_{DD}) = \sum_{i=1}^{K}(Kpi \times fi)\ [\mu W],\ P_i(LV_{DD}) = \sum_{i=1}^{K}(Kpi \times fi)\ [\mu W]$$

where

K: Total number of internal cells
fi: Ith input buffer operating frequency [MHz]
Kpi: Input buffer voltage coefficient (See Table 9-2.)

The sum of $P_i(HV_{DD})$ and $P_i(LV_{DD})$ given in the formulas above is input buffer power consumption. Calculate for HV_{DD} input buffers using the 5.0V (or 3.3V) Kpi value and for LV_{DD} buffers using the 3.3V Kpi value. Table 9-2 shows the Kpi values.

Table 9-2 S1L50000 Series Dual Power Supply Input Buffer Kpi Values

V_{DD} (TYP)	Kpi
HV_{DD} = 5.0V	17.7µW/MHz
HV_{DD} (or LV_{DD}) = 3.3V	6.2µW/MHz

(3) Output buffer power consumption ($P_o(HV_{DD})$ and $P_o(LV_{DD})$)

If the HV_{DD} power consumption is $P_o(HV_{DD})$ and LV_{DD} power consumption is $P_o(LV_{DD})$, the total power consumption P_o(total) is calculated as follows:

$P_o(total) = P_o(HV_{DD}) + P_o(LV_{DD})$

If the output buffer AC power consumption is P_{AC} and DC power consumption is P_{DC}, $P_o(HV_{DD})$ and $P_o(LV_{DD})$ are calculated as follows:

$P_o(HV_{DD}) = \Sigma\{P_{AC}(HV_{DD}) + P_{DC}(HV_{DD})\}$

$P_o(LV_{DD}) = \Sigma\{P_{AC}(LV_{DD}) + P_{DC}(LV_{DD})\}$

① AC power consumption (P_{AC})

The total output buffer power consumption for an AC load can be estimated using the following formula:

$$P_{AC} = \sum_{i=1}^{K}\{fi \times C_L i \times (V_{DD})^2\}$$

where

K: Total number of internal cells
fi: ith output buffer operating frequency [Hz]
C_L: Output load capacitance [F]
V_{DD}: Power supply voltage [V]

② DC Power Consumption (P_{DC})

Approximate DC power consumption is obtained by the following formula:

$P_{DC} = P_{DCH} + P_{DCL}$

$P_{DCH} = |I_{OH}| \times (V_{DD} - V_{OH})$
$P_{DCL} = I_{OL} \times V_{OL}$

The ratio of P_{DCH} to P_{DCL} is determined by the duty ratio of output signal.

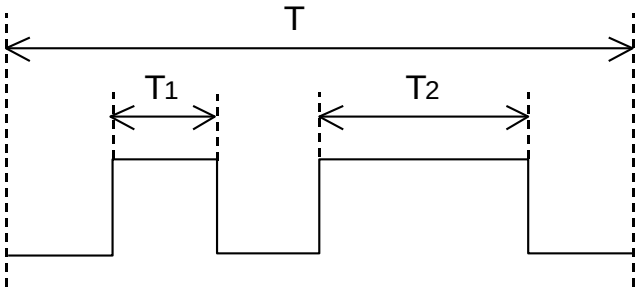


Figure 9-1 Example of Duty Cycle

In Figure 9-1,

Duty H = $(T_1 + T_2) \div T$
Duty L = $(T - T_1 - T_2) \div T$

Therefore

$$P_{DC} = P_{DCH} + P_{DCL} = \sum_{i=1}^{K} \{(V_{DD} - V_{OH}i) \times I_{OH}i \times \text{Duty H}\} + \sum_{i=1}^{K} (V_{OL}i \times I_{OL}i \times \text{Duty L})$$

The output buffer power consumption value P_o to be determined is as follows:

$$P_o(HV_{DD}) = \sum_{i=1}^{K} \{fi \times C_L i \times (HV_{DD})^2\} + \sum_{i=1}^{K} \{fi \times C_L i \times (HV_{DD} - V_{OH}i) \times |I_{OH}i| \times \text{DutyH}\} + \sum_{i=1}^{K} \{V_{OL}i \times I_{OL}i \times \text{DutyL}\}$$

$$P_o(LV_{DD}) = \sum_{i=1}^{K} \{fi \times C_L i \times (LV_{DD})^2\} + \sum_{i=1}^{K} \{fi \times C_L i \times (LV_{DD} - V_{OH}i) \times |I_{OH}i| \times \text{DutyH}\} + \sum_{i=1}^{K} \{V_{OL}i \times I_{OL}i \times \text{DutyL}\}$$

9.1.2 Power Consumption Calculation for Single Power Supply

(1) Internal cell (P_{int})

The power consumption by internal cells is dependent on the used gate count, cell utilization, operating frequency and the ratio of cells that operate at the operating frequency. To calculate, use the following formula:

$$P_{int} = \sum_{i=1}^{K} \{(Nb \times U) \times fi \times Spi \times Kpint\} \ [\mu W]$$

where
Nb: Total number of basic cells
U: Cell utilization ratio
fi: Ith operating frequency [MHz]
Spi: Ratio of basic cells that operate at operating frequency fi [MHz] to the total basic cell count (target 20 to 30%, depending on the system, though.)
Kpint: Power consumption per BC. See Table 9-3.

Table 9-3 S1L50000 Series Single Power Supply Kpint per BC

V_{DD} (TYP)	Kpi
3.3V	0.70µW/MHz

(2) Input Buffers (P_i)

The power consumption by input buffers is the total sum of the products of the operating frequency f in MHz and the power coefficient Kpi [µW/MHz].

$$P_i = \sum_{i=1}^{K} (Kpi \times fi) \ [\mu W]$$

fi: Ith input buffer operating frequency [MHz]
Kpi: Input buffer voltage coefficient (See Table 9-4.)

Table 9-4 S1L50000 Series Single Power Supply Input Buffer Kpi Value

V_{DD} (TYP)	Kpi
3.3V	6.2µW/MHz

(3) Output Buffers (P_o)

The power consumption by output buffers is different depending on whether the load is DC load (resistive load by the connection with TTL device) or AC load (capacitive load by the connection with CMOS device).

If the output buffer DC power consumption is P_{DC} and AC power consumption is P_{AC}, the total power consumption of output buffers P_o is given by the following formula:

$$P_o = P_{AC} + P_{DC}$$

① AC power consumption (P_{AC})

Approximate AC power consumption is obtained by the following formula:

$$P_{AC} = \sum_{i=1}^{K} \{fi \times C_L i \times (V_{DD})^2\}$$

where
fi: ith output buffer operating frequency [Hz]
C_L: Output load capacitance [F]
V_{DD}: Power supply voltage [V]

② DC power consumption (P_{DC})

Approximate DC power consumption is obtained by the following formula:

$P_{DC} = P_{DCH} + P_{DCL}$
$P_{DCH} = |I_{OH}| \times (V_{DD} - V_{OH})$
$P_{DCL} = I_{OL} \times V_{OL}$

The ratio of P_{DCH} to P_{DCL} is determined by the duty ratio of output signal.

In Figure 9-1,

Duty H = $(T_1 + T_2) \div T$
Duty L = $(T - T_1 - T_2) \div T$

Therefore
$P_{DC} = P_{DCH} + P_{DCL}$
$= \sum_{i=1}^{K} \{ (V_{DD} - V_{OH}i) \times I_{OH}i \times \text{Duty H} \} + \sum_{i=1}^{K} (V_{OL}i \times I_{OL}i \times \text{Duty L})$

9.1.3 Low Power Cells

Low power cells are available to achieve lower power consumption operation. Using low power cells increases the propagation delay time compared to the normal cells, but the power consumption decreases to about 80%.

When using low power cells, calculate power consumption by multiplying the Kpint values in Tables 9-1 and 9-3 by 0.8. Table 9-5 shows the examples of low power cells.

9.1.4 Low Noise Cells

Low noise cells are effective to reduce EMI noise to the customer's product. The peak operating current due to the flip-flop cell operation is lowered while reducing the effect on the propagation delay as much as possible.

When using low noise cells, calculate power consumption by multiplying the Kpint values in Tables 9-1 and 9-3 by 0.7. Table 9-5 shows a low noise cell example.

Table 9-5 S1L50000 Series Low Power/Noise Cells

Type	Normal cell	Low power cell	Low noise cell
D-Flip Flop*1	DF	DFL	DFLQ
JK-Flip Flop*1	JKR	JKRL	-
Latch	LF	LFL	-

NOTE: *1: In addition to the cells shown above, scan cells are also available.

Figure 9-2 illustrates how effectively low noise cells reduce the EMI noise. The data shown is an example obtained from the evaluation using Epson's test samples, and thus they are not guaranteed in the customer's designs.

Please contact our sales representative for more information.

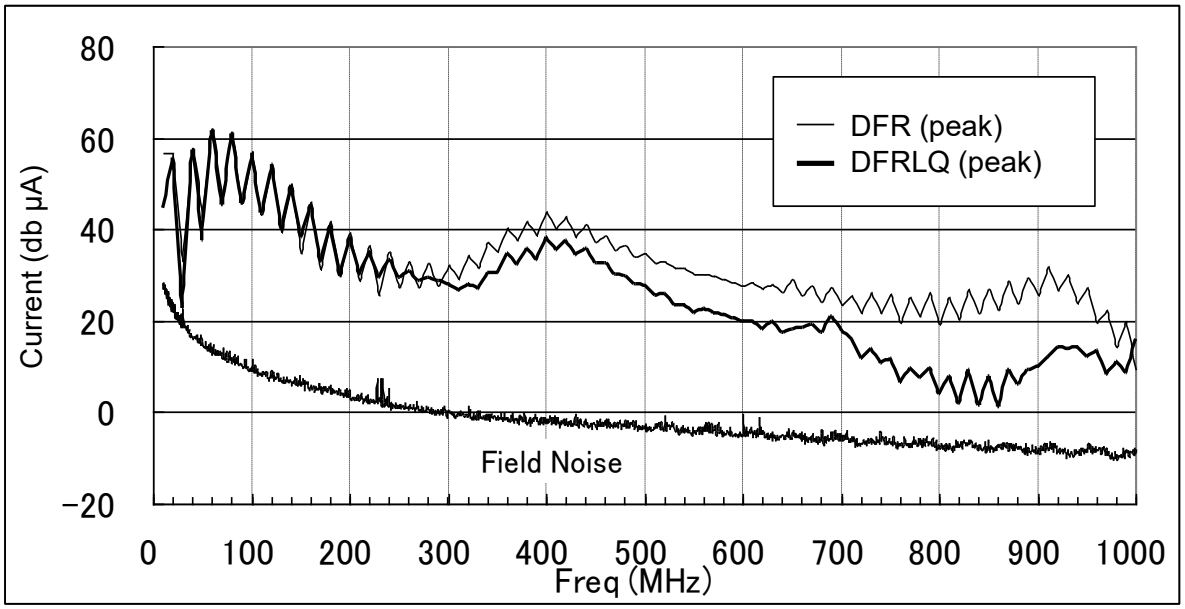


Figure 9-2 V_{DD} Current Spectrum According to the IEC 61967-1, 6 (MP Method)

9.2 Limit on Power Consumption

The chip temperature will increase with power consumption. The IC delay will also vary depending on the IC chip junction temperature Tj. Standard IC specifications are indicated using Ta, but the correlation between Tj and Ta is not constant, and will vary depending on the thermal resistance and power consumption for that IC package.

The IC chip temperature can be calculated as follows from the ambient temperature Ta, package thermal resistance θj-a, and power consumption PD. For the thermal resistance of each package, refer to our web site: www.global.epson.com/products_and_drivers/semicon/products/asic/package_list.html#ac06.

Chip temperature (Tj) = Ta + (P_D × θj-a) (°C)

Specifications are normally stipulated using Ta, so the delay library is provided using the following guide:

* For Ta = -40 to 85 [°C], Tj = -40 to 125 [°C] library

Please note that Epson may add other conditions in cases in which the correlation between Ta and Tj varies significantly depending on the package and estimated power consumption.

Use the S1L50000 Series with a chip temperature (Tj) not exceeding 125°C.

Appendix

A1. Simulation Results Example

A1.1 Comparison File Example for Simulation Results and Expected Values

```
# APF file comparison program (apfcomp)
# version 2.70 Copyright (c) 1995-2003. SEIKO EPSON CORPORATION
#       EXPECT        : samp.apf                          ← Expected value file name to be compared
#       COMPARE       : samp.sammax                       ← APF file name to be compared
#       RESULT        : samp.expmax                       ← Comparison results file
#       RUN DATE      : Wed Feb 13 15:03:14 2008          ← Program run date/time
#       DON'T CARE :                                      ← "X" if "-noxcare" option was specified; "." if "-nodotcare" was specified
#       IGNORE RZ   : NO                                  ← "YES" if "-norzcare" was specified
#
$DESIGN    sample

$RATE    100000
$STROBE    98000
$RESOLUTION    0.001ns

$IOCONT
I_14.E    E0    DATA3
I_15.E    E0    DATA2
I_16.E    E0    DATA1
$ENDIOCONT

$NODE
SEL       I     0
CK        N     0    50000
RESET     I     0
DATA1     BU    0
DATA2     BU    0
DATA3     BU    0
$ENDNODE
# Compared      ......

$PATTERN
#                 SCRDDD
#                 EKEAAA
#                 L STTT
#                    EAAA
#                    T123
#
#                 INIBBB
#                     UUU
#
              3     0N0LLL
#Mismatch             H                                    ← Mismatch line and mismatch value
             10     0N1LLH
#Mismatch             HX                                   ← Mismatch line and mismatch value
             12     0N1LHL
#Mismatch             H ?                                  ← Mismatch line and mismatch value
$ENDPATTERN
#         3 Mismatch lines found.    93.2% Matched         ← Number of mismatch lines and matched percentage within pattern
# End event of EXPECT_file    = 43                        ← End event of expected value file
# End event of COMPARE_file = 43                          ← End event of APF file
# MISMATCH SIGNAL         Actual / Total number of mismatches at each node.
# * Actual = Total number of mismatches at each node minus(-) number of "?".
# <<    DATA1       >>        COUNT =        3/3          ← Mismatch signal name and number of mismatches
# <<    DATA2       >>        COUNT =        1/1               Number of mismatches excluding COUNT=? out of total mismatches
# <<    DATA3       >>        COUNT =        0/1
```

Mismatches arising in the comparison file may be due to the following causes:

(1) Flip-flop mismatch
Note that errors will not appear on the timing error list if the setup time or hold time constraints are exceeded.

(2) Strobe point exceeded due to output delay
This may occur in cases in which the output results from one output pin appear to change constantly with a delay corresponding to one cycle from the expected output value. The delay may occur for L output or H output only.

(3) Combination circuit hazard at output end stage
Hazards (glitches, spike pulses) occurring in combination circuits may be output externally. This can be confirmed in the NARROW report on the timing error list. To avoid this, signals from combination circuits should first be received using a flip-flop before being output.

(4) Unknown value (X) propagation
The RAM and flip-flop output is unknown before initialization.
If combination circuits exist on the clock line, the flip-flop output will be unknown if hazards occurring due to variations coinciding with input are input to that flip-flop clock pin.
Likewise, if a composite cell for clock gating (e.g., CLPSAD2V) is inserted using Power Compiler or similar tool, the output clock will be unknown if an unknown signal is input to the enable pin.

A1.2 Timing Error List

A list (*.errmax, *.errmin) like that shown in Figure A1-1 is output if a timing error occurs during simulation. This section describes how to read the timing list in conjunction with Figure A2-2. (a) to (g) in Figure A1-1 correspond to (a) to (g) in Figure A1-2.

```
*
*OUTPUT NAME VALUE OFFSET/EVENT NUMBER
**--------------------------------------------------------------------------------
I=top.ffreg1_reg(a) (D ->posedge C &&& (VM6 != 0)(b) ==SETUP TIME ERROR(c) ...SPEC =325(d) )
323(e) 471(f)/   3 35 120 185(g)
**-------------------------------------------------------------------SUB_TOT 4(h)
I=top.ffreg5_reg (posedge C ->D ==HOLD TIME ERROR ...SPEC =106 )
93 474/    3
**-------------------------------------------------------------------SUB_TOT 1
I=top.sub1.flag_a_0 (negedge R ->posedge C &&&(D !==0)  ==SETUP TIME ERROR ...SPEC =334 )
320 482/   3 276
309 482/   405
309 419/   797 961 1221 1477 1649 3017
309 447/   2722
**-------------------------------------------------------------------SUB_TOT 10
*-------------------------------------------------------------------TOTAL 15(i)
```

Figure A1-1 Timing Error List Example

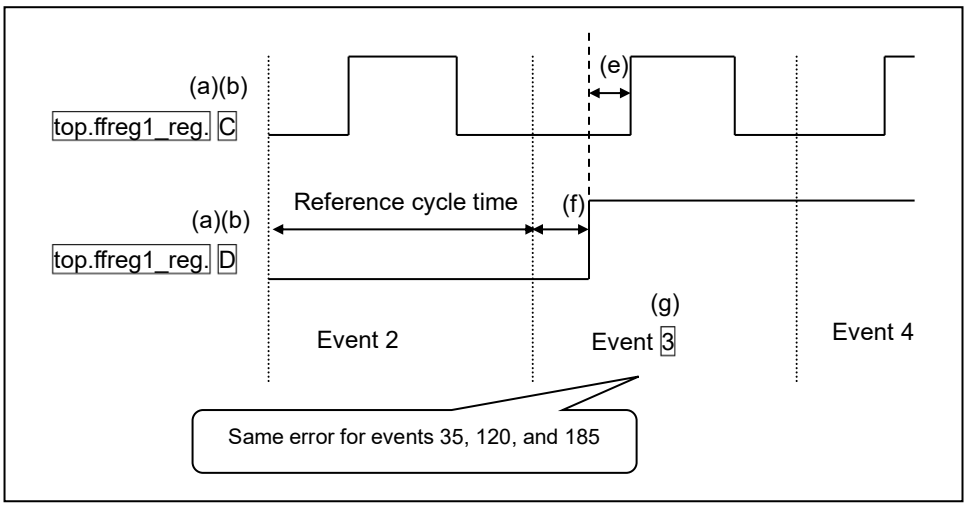


Figure A1-2 Illustration with Waveform

Explanation of (a) to (i) in Figure A1-1 example

(a) Timing error instance name

Displays the instance name for the timing error as a full path.

In the case shown in Figure A1-1, the error instance name is the FF “top.ffreg1_reg”. The instance name can be used to determine whether the timing error constitutes a problem location. Note that the instance name may change during logic synthesis.

(b) Timing error detection conditions

The specific conditions under which a timing error occurs.

“A ->B&&&(C)” indicates that “B changes after A changes under condition C”.

In the case shown in Figure A1-1, the condition corresponds to “A rising signal is input to pin C after the pin D signal changes while flag VM6 is at a state other than 0”. “VM*” indicates the timing error detection flag in the cell (FF in this case) simulation model. Ignore this if the condition statement is “VM*”. In this example, check only the relationship between pins C and D.

If “NARROW*” is indicated, refer to the description from “MINIMUM PULSE WIDTH” onward in (c) below.

(c) Types of timing constraints

The following are the major types of timing constraints causing errors:

SETUP TIME:	Setup time constraint
HOLD TIME:	Hold time constraint
MINIMUM PULSE WIDTH:	Minimum pulse width constraint

“NARROW*” may be indicated in section (b). This indicates that the length is 75% or less of the rate (reference cycle time), since it is difficult to check the output waveform in detail when checking simulation results using the sampled data (apf). The “NARROW*” indication does not necessarily mean that this error must be fixed. Check the circuit specifications to determine that this causes no issues.

(d) Timing error detection standards (units: ps)

The minimum value for which no error occurs

In the case shown in Figure A1-2, an interval of at least 325ps must be left between the “D” change and “posedge C” to prevent a SETUP error from occurring.

(e) Actual timing value (units: ps)

In the case shown in Figure A1-2, the SETUP constraint was short by 2ps (= 325ps − 323ps).

(f) Timing error offset (units: ps)

The time from event start until an error occurs

In the case shown in Figure A1-1, this indicates that a timing error occurred 471ps after the event start.

(g) Timing error event (cycle) number

This lists the event numbers for which timing errors have occurred. In the case shown in Figure A1-1, errors have occurred for event numbers 3, 35, 120, and 185. Check against the simulation results to determine whether this constitutes a problem with circuit specifications.

(h) Timing error subtotal

Number of timing errors with the same instance name, error detection conditions, and timing constraints

(i) Timing error total

Total number of timing errors

A2. RTL Design Restrictions and Limitations (VHDL)

As described in section 1.5.3, provisional circuit data provided by the customer can be used to identify problems in the RTL description in advance. However, depending on the description, errors may also be detected in locations not intended by the customer. Circuits should be designed in accordance with the general RTL design style guide to avoid such issues.

A2.1 Provision of RTL Supporting Logic Synthesis

The RTL provided should use only descriptions that allow logic synthesis. Logic synthesis is not possible if behavior level descriptions are included. If the description supports logic synthesis, splitting into separate files should not give rise to problems.

A2.2 Provision of Hierarchical Design Diagrams

The module may be a hierarchical design. If a hierarchical design is used, please send hierarchical structure diagrams (tree diagrams) or documentation showing the hierarchical relationship between modules.

A2.3 RAM Description

Epson can provide RAM VITAL models. Please specify the required RAM size and quantities. Please note that providing RAM VITAL models may require several days.

If RAM models are described by the customer, please ensure that these comply with the specifications described in "Chapter 8 RAM Specifications" of the Design Guide. Additionally, provide module names for the model.

A2.4 Constant Assignment to Input Ports

Constants cannot be assigned directly to input ports using the port_map statement. Likewise, it is not possible to assign "open" or to omit the description. Otherwise, errors will occur during logic synthesis. To avoid this, map "signal" with a constant.

```
Architecture BEHAVIOR of example3_4
signal dummy0 std_logic;
signal dummy1 std_logic;
begin
  dummy0 <= 0;
  dummy1 <= 1;
  port map abcx ( a => dummy0, b=> dummy1, c=> data_in, x => data_out )
end BEHAVIOR;
```

Figure A2-1 Mapping "signal" with a Constant

A2.5 Pin Name Constraints

We recommend that the names of external and internal pins conform to the constraints described in the design guide. Please note that names that fail to comply with the constraints may be changed to unintended names during logic synthesis.

(1) External pin name constraints

① Names must be specified entirely in upper case.

② Only alphanumeric characters and the underscore ("_") character can be used.
The first character must be a letter of the alphabet and the last character must be an alphanumeric character.

③ The underscore ("_") character cannot be used in succession.

④ Names must be two to 32 characters long.

⑤ "read" and "write" cannot be used. (Reserved for system use)

(2) Internal pin name constraints

① Names may include both upper and lower case characters. However, identical names cannot be used if they differ by upper or lower case.
Example: "ABC" and "Abc" cannot be used at the same time.

② Only alphanumeric characters, the underscore ("_") character, and parentheses "(" and ")" for bus descriptions can be used.

③ Names must be two to 32 characters long.

(3) VHDL reserved words

The following text strings cannot be used as user-defined names:

abs	access	after	alias	all	and	architecture
array	assert	attribute	begin	block	body	buffer
bus	case	component	configuration	constant	disconnect	downto
else	elsif	end	entity	exit	file	for
function	generate	generic	guarded	if	in	inout
is	label	library	linkage	loop	map	mod
nand	new	next	nor	not	null	of
on	open	or	others	out	pakage	port
procedure	process	range	record	register	rem	report
return	select	severity	signal	subtype	then	to
transport	type	units	until	use	variable	wait
when	while	with	xor			

(4) Verilog-HDL reserved words

VHDL-RTL needs to be converted to Verilog netlists for compatibility with the tools used in the work carried out at Epson.

Thus, the following text strings cannot be used as user-defined names:

always	and	assign	begin	buf	bufif0	bufif1
case	casex	casez	cmos	deassign	default	defparam
disable	edge	else	end	endcase	endmodule	endfunction
endprimitive	endspecify	endtable	endtask	event	for	force
forever	fork	function	highz0	highz1	if	ifnone
initial	inout	input	integer	join	large	macromodule
medium	module	nand	negedge	nmos	nor	not
notif0	notif1	or	output	parameter	pmos	posedge
primitive	pull0	pull1	pullup	pulldown	rcmos	real
realtime	reg	release	repeat	rnmos	rpmos	rtranif0
rtranif1	scalared	small	specify	specparam	strong0	strong1
supply0	supply1	table	task	time	tran	tranif0
tranif1	tri	tri0	triand	trior	trireg	vectored
wait	wand	weak0	weak1	while	wire	wor
xnor	xor					

A2.6 Port Data Format

Only the std_logic data format can be used for the uppermost module ports. Bus descriptions are not permitted. Use std_logic and std_logic_vector for all other module ports. Note that bus descriptions may be expanded during logic synthesis at Epson.

A2.7 “integer” Usage

Care is required with the bit width when using “integer”. We recommend making “signal” declarations using std_logic_vector, then converting with conv_integer when calculating.

A2.8 I/O Buffers

I/O buffers will be added at Epson. Please provide pinout tables specifying buffer types and output load capacitances. If the timing conditions are exacting or if special buffers such as fail-safe buffers are used, specify this when submitting the provisional data.

The top module of I/O buffers can be safely and easily changed from an RTL type to a gate type. A top module for gate use will be created at Epson. The customer only need include descriptions related to input and output in the RTL top module. More specifically, uni-directional ports should only be connected to lower modules on a one-to-one basis. Bi-directional ports should include description for bi-directional signals within the top module extracting the input signal ports, output signal ports, and enable signal ports from the lower layers.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
entity TOP is
   port( IN1 : in std_logic;    OUT1 : out std_logic;    BID1 : inout std_logic);
end TOP;

architecture rtl of TOP is
   signal en, bid1_out : std_logic;
   component CORE
      port( in1, bid1_in             : in    std_logic ;
            out1, bid1_out, en : out std_logic    );
   end component;

begin
      U_CORE : CORE port map( in1 => IN1, out1 => OUT1, bid1_in => BID1,
                                          bid1_out => bid1_out, en => en);
      BID1 <= 'Z' when en = '1' else bid1_out ;
end rtl;

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity CORE is
   port( in1, bid1_in             : in    std_logic ;
         out1, bid1_out, en : out std_logic    );
end CORE;

architecture rtl of CORE is
begin
end rtl;
```

Figure A2-2 Top Module RTL Example

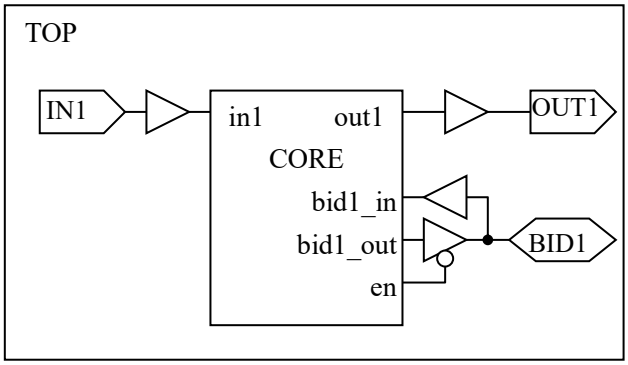


Figure A2-3 Top Module Schematic

A2.9 Primitive Cell Usage

Please notify us of module names within the RTL calling up Epson primitive cells as well as the primitive cell names. The settings will be configured to ensure that primitive cells are not deleted during logic synthesis. Additionally, delete statements related to Epson libraries described during simulation. Asynchronous RAM model library statements should also be deleted.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

----- comment out -----
-- library S1L50000_TYP,S1L50000_RAM;
-- use S1L50000_TYP.all;
-- use S1L50000_TYP.all;
----- comment out -----
```

Figure A2-4 Commenting Out Epson Library Statements

A3. AC/DC Test Patterns

A3.1 DC Test Patterns

The following test items should be taken into consideration if the customer prepares DC test circuits.

DC testing verifies the DC characteristics of the IC. The test makes its measurements at the end of a test event. The pins tested should remain in the same state in the test event after the strobe.

The following DC characteristics are measured:

(1) Static current ($I_{DDS)}$ test

Static current is leakage current that flows through the IC power supplies when input signals are stable. This leakage current is normally extremely small and must be measured with no other currents flowing. All of the following conditions must be met to achieve this. Additionally, there must be at least two events in which the static current is measurable.

① All input pins must be stable.

② There must be high or low level input or output to/from bi-directional pins.

③ There must be no active elements such as oscillators in the circuit.

④ Internal 3-state buffers (internal bus) must be neither floating nor in contention.

⑤ Current must not be flowing through function cells such as RAM.

⑥ There must be high level input to input pins with pull-up resistors.

⑦ There must be high level input or output to/from bi-directional pins with pull-up resistors.

(2) Input current test

This tests parameters related to the input of input buffers, including input leakage current and pull-up and pull-down currents. The test measures the current flowing when V_{DD} or V_{SS} level voltage is applied to the target pin. That is, either high or low level voltage is applied to the pins under test.

For example, if a V_{DD} level (high level) voltage is applied to a target pin with a low level voltage applied, the target pin state will change from low to high, and the IC may behave unexpectedly.

To test the input current, the V_{DD} level voltage is applied to the target pin in an event in the test pattern in which the pin is subjected to high input, and the V_{SS} level voltage is applied in an event in which the pin is subjected to low input. These target pin states must therefore exist in the test patterns to enable testing.

(3) Input leakage current test (I_{IH}, I_{IL})

This tests parameters related to the input current of input buffers without pull-up or pull-down resistors.

The current that flows when high level voltage is applied to the input buffer is called I_{IH}. This is guaranteed up to the maximum current. Test patterns for this test must contain events with high level input to the pins under test. In the case of bi-directional pins, there must be high level input while in the input state.

The current that flows when low level voltage is applied to the input buffer is called I_{IL}. This is guaranteed up to the maximum current. Test patterns for this test must contain events with low level input to the pins under test. In the case of bi-directional pins, there must be low level input while in the input state.

(4) Pull-up current test (I_{PU})

This measures the current flowing when the low level voltage is applied to an input buffer with a pull-up resistor. Test patterns for this test must contain events in which low level signals are input to the pins under test. In the case of bi-directional pins, low level signals must be input while in the input state.

(5) Pull-down current test (I_{PD})

This measures the current flowing when the high level voltage is applied to an input buffer with a pull-down resistor. Test patterns for this test must contain events with high level input to the pins under test. In the case of bi-directional pins, there must be high level input while in the input state.

(6) Output voltage test (V_{OH}, V_{OL})

This tests the current drivability of output buffers. With the test pins driven to the target output level, the voltage drop is measured when the specified current load is applied.

To test the output characteristics, the test patterns must include all possible target pin states. Also, those states must remain unchanged during the test event even if the test rate is indefinitely extended.

(7) Off-state leakage current (I_{OZ})

This measures the leakage current that flows to an open drain or 3-state output buffer when the output state is high impedance. It actually measures the current when the V_{DD} level or V_{SS} level voltage is applied to the test pins in the high impedance state. This means the test patterns must contain events in which the test pins are in the high impedance state.

A3.2 AC Test Patterns

AC testing measures the time taken for a signal change occurring in an input pin to propagate to an output pin. If the customer prepares the AC test circuit, the customer should select the AC test path.

(1) Constraints on test events

This test method is typically performed by the binary search method. The target test pin (output pin subject to change) must have only a single change point within a test event. (Pins that output RZ waveforms cannot be tested. Pins that output hazard in the test event cannot be tested, either.) The tested signal changes must be “High” to “Low” or “Low” to “High.” (Changes related to Z cannot be tested.)

Take care to avoid selecting test events in which multiple output signals change simultaneously or bi-directional and IC tester signals are in contention. The presence of simultaneous signal changes or signal contention destabilizes the IC power supply, affecting the output waveforms of the test pins and preventing accurate testing.

(2) Constraints on AC test points

The number of AC test points must be four or fewer.

(3) Constraints on test path delay

Testing accuracy increases with increased test path delay. Set the test path delay to at least 30ns and less than the strobe point for the test simulation maximum condition.

(4) Other constraints

① Do not specify paths from oscillator circuits.

② Specify paths not passing through the internal 3-state circuit (internal bus).

③ Do not specify paths passing through other bi-directional buffers between the test path input buffer and an output buffer.

④ If the IC has multiple operating voltage ranges, test within one voltage range.

(5) Constraints on bi-directional pin test patterns

It is not possible to switch the input and output modes of bi-directional pins multiple times within one event due to the limits of the tester. Generate test patterns to ensure that the RZ waveform is not used to switch the input and output modes of bi-directional buffers.

A4. Input/Output Buffer Characteristic Graphs

A4.1 5.0V Operation

A4.1.1 Output Current Characteristics (5.0V ±0.5V)

Table A4-1 Output Current Characteristics (5.0V ±0.5V)

	Output current	
Type No.	**I_{OL} (mA)**	**I_{OH} (mA)**
TYPE S	0.1	-0.1
TYPE M	1	-1
TYPE 1	3	-3
TYPE 2	8	-8
TYPE 3	12	-12
TYPE 4	24	-12
PCI	Conformed to the PCI Standard	

"S," "M," and "1" through "4" following "TYPE*" are the numbers indicated in the "XX*X" section of the names of output cells.
Example: OB3T indicates TYPE 3.

A4.1.2 Input Buffer Characteristics (5.0V ±0.5V)

- Standard cell input buffer

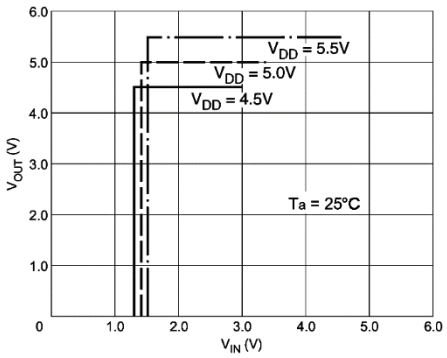


Figure A4.1-1 Input Characteristic (TTL Level)

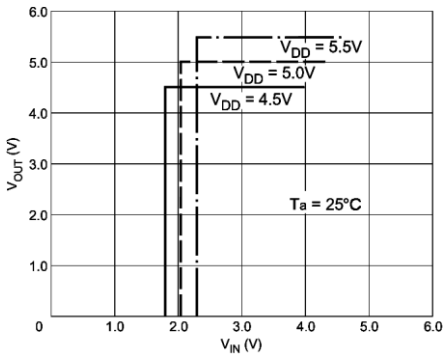


Figure A4.1-2 Input Characteristic (CMOS Level)

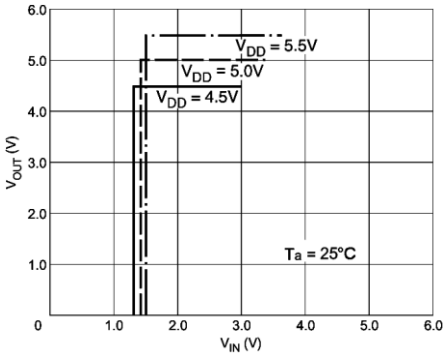


Figure A4.1-3 Input Characteristic (5V PCI Level)

- Schmitt trigger cell input buffer

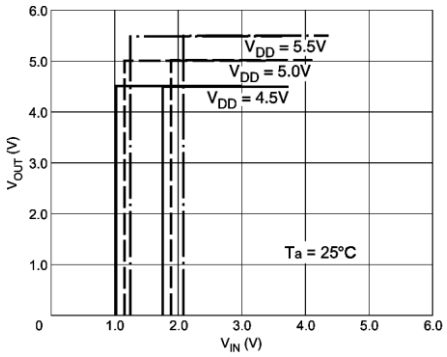


Figure A4.1-4 Input Characteristic (TTL Level)

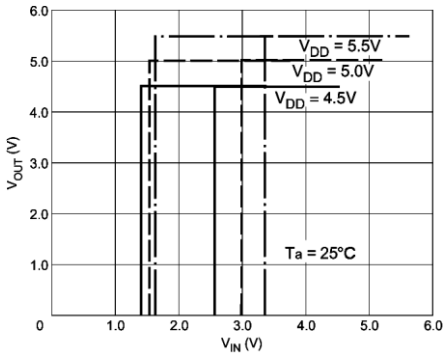


Figure A4.1-5 Input Characteristic (CMOS Level)

A4.1.3 Output Driver Characteristics

- Low-level output current

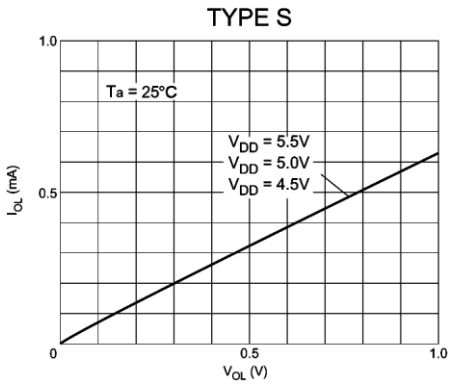


Figure A4.1-6

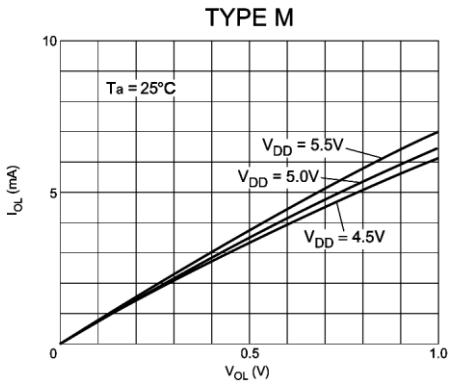


Figure A4.1-7

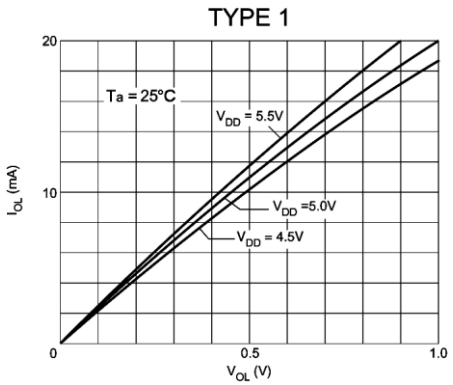


Figure A4.1-8

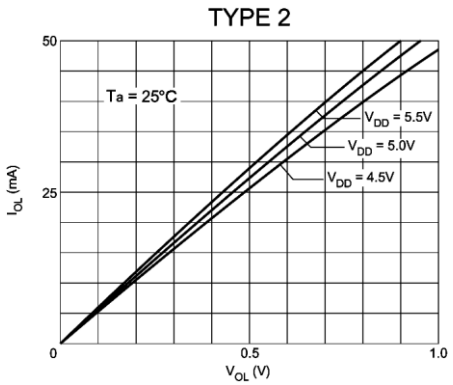


Figure A4.1-9

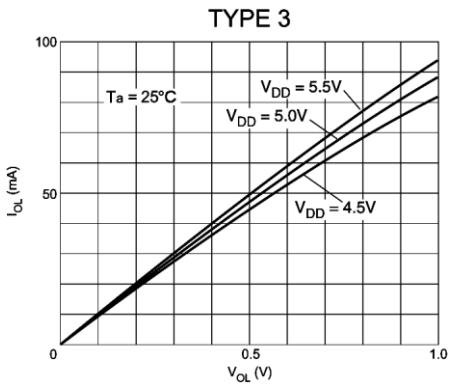


Figure A4.1-10

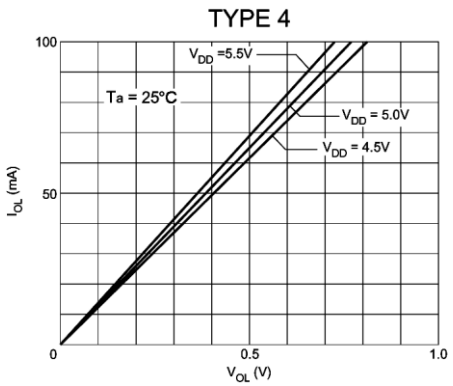


Figure A4.1-11

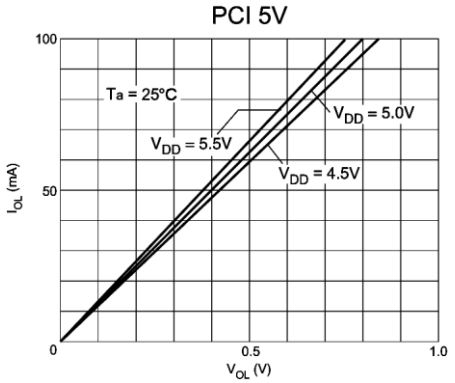


Figure A4.1-12

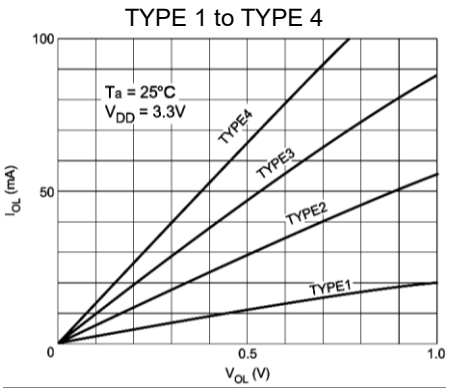


Figure A4.1-13

- High level output current

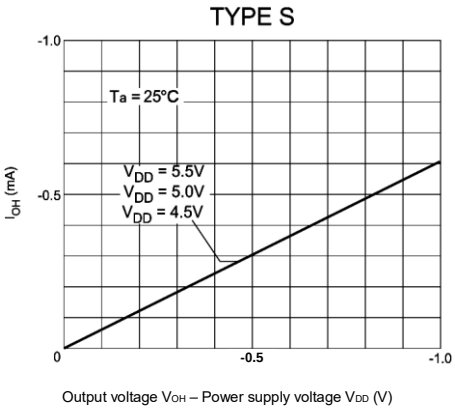


Figure A4.1-14

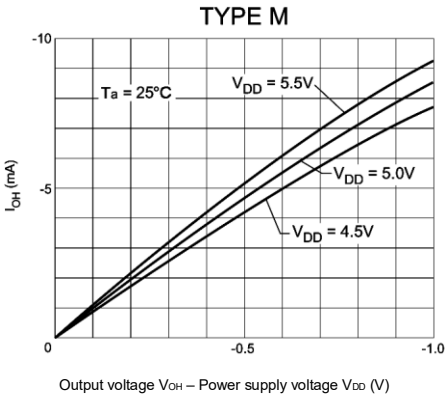


Figure A4.1-15

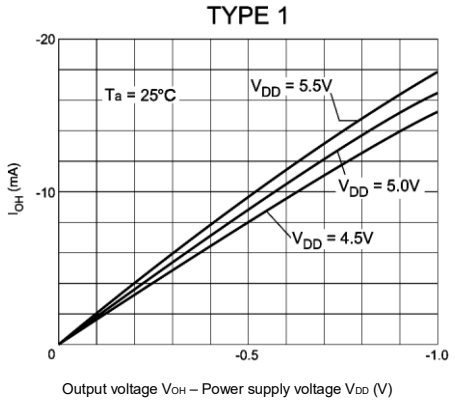


Figure A4.1-16

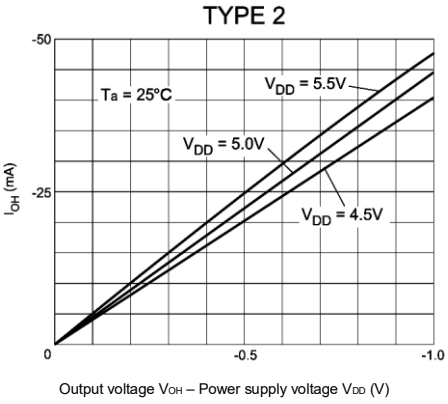


Figure A4.1-17

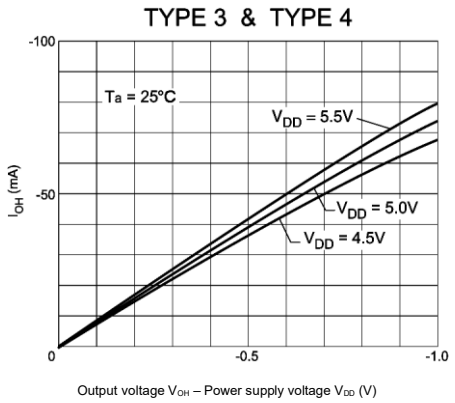


Figure A4.1-18

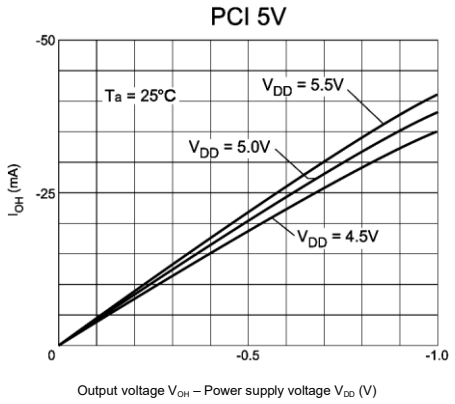


Figure A4.1-19

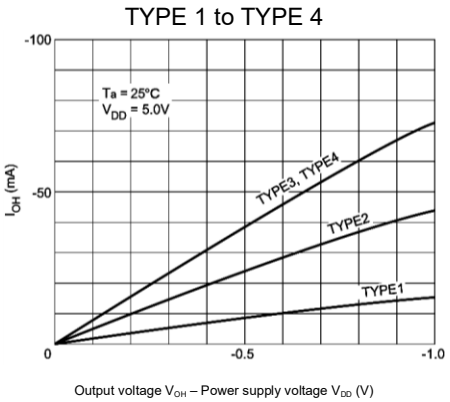


Figure A4.1-20

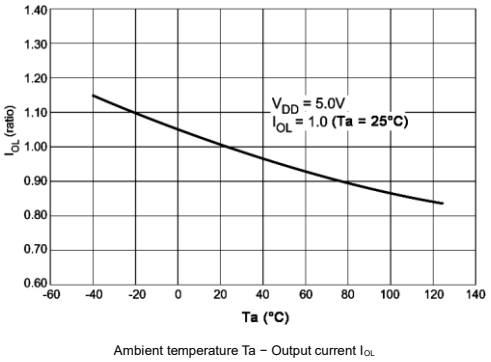


Figure A4.1-21

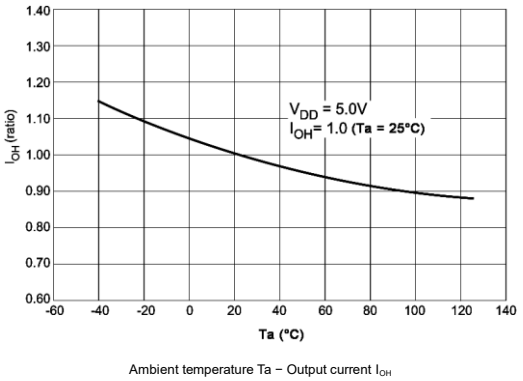


Figure A4.1-22

A4.1.4 Output Delay Time vs. Output Load Capacitance (C_L)

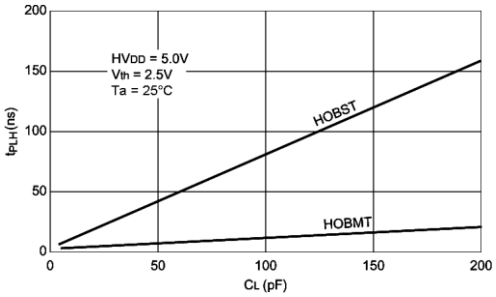


Figure A4.1-23 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

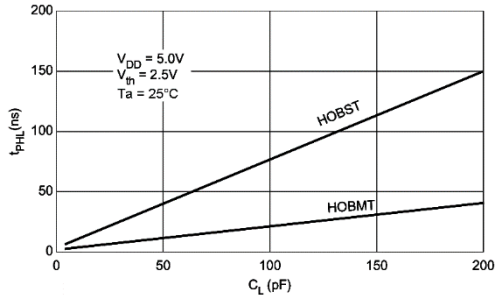


Figure A4.1-24 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

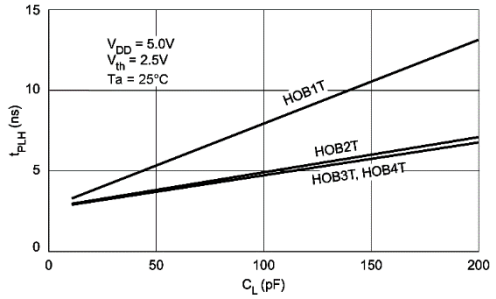


Figure A4.1-25 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

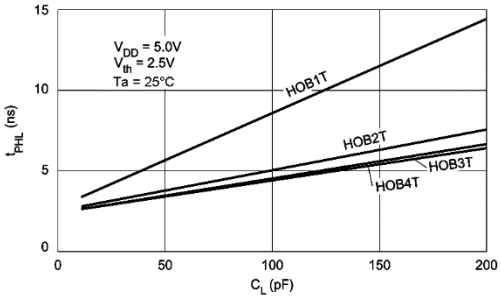


Figure A4.1-26 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

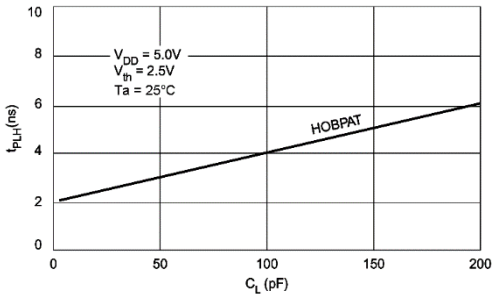


Figure A4.1-27 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

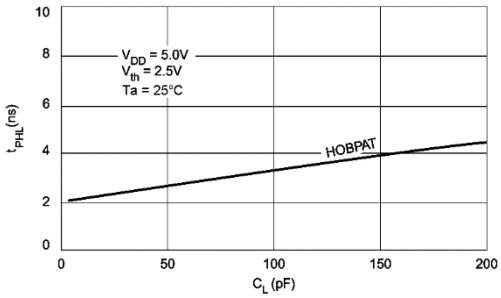


Figure A4.1-28 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

A4.1.5 Output Buffer Rising/Falling Time vs. Output Load Capacitance (C_L)

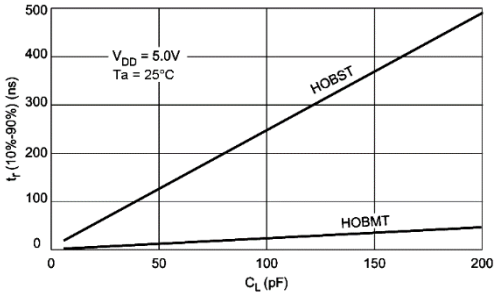


Figure A4.1-29 Rising Time (t_r) vs. Output Load Capacitance (C_L)

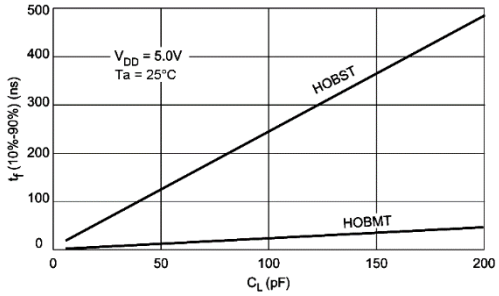


Figure A4.1-30 Falling Time (t_f) vs. Output Load Capacitance (C_L)

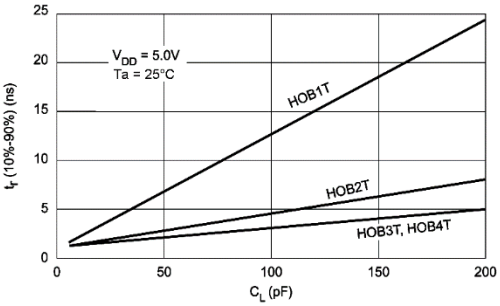


Figure A4.1-31 Rising Time (t_r) vs. Output Load Capacitance (C_L)

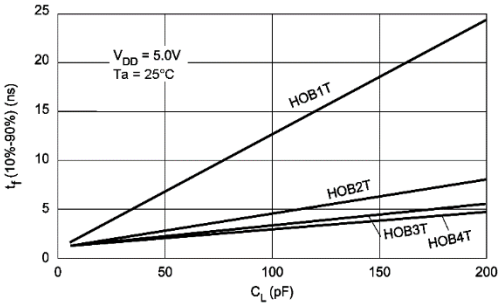


Figure A4.1-32 Falling Time (t_f) vs. Output Load Capacitance (C_L)

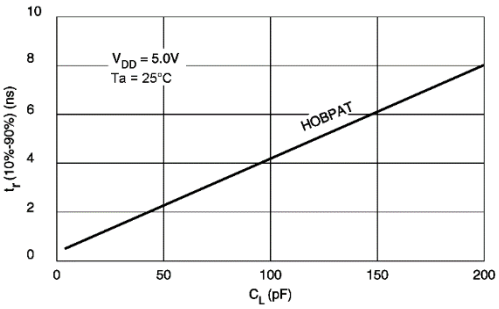


Figure A4.1-33 Rising Time (t_r) vs. Output Load Capacitance (C_L)

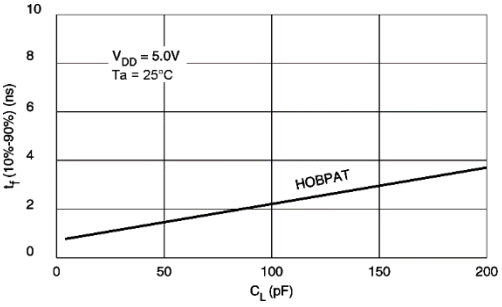


Figure A4.1-34 Falling Time (t_f) vs. Output Load Capacitance (C_L)

A4.1.6 Pull-up, pull-down Resistance

- Pull-up characteristics

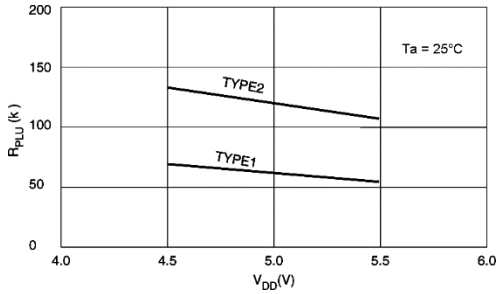


Figure A4.1-35 Power Supply Voltage Dependency of Pull-up Resistance

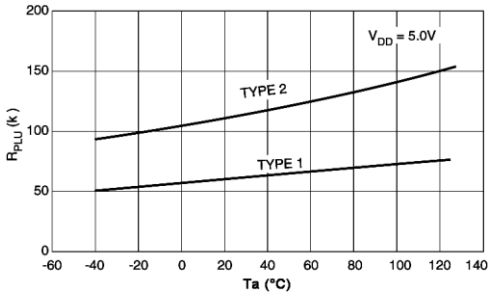


Figure A4.1-36 Ambient Temperature Dependency of Pull-up Resistance

- Pull-down characteristics

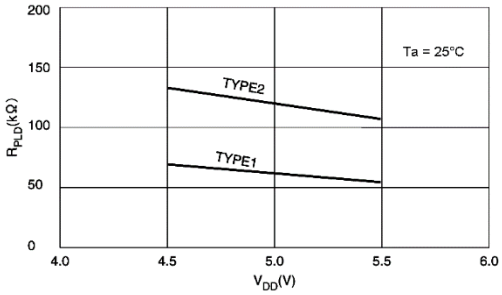


Figure A4.1-37 Power Supply Voltage Dependency of Pull-down Resistance

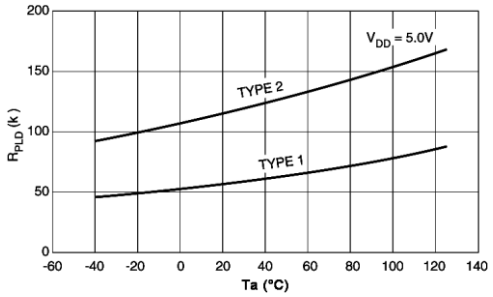


Figure A4.1-38 Ambient Temperature Dependency of Pull-down Resistance

A4.1.7 Output Waveforms

- High-speed type output buffer waveform (HOB3AT)

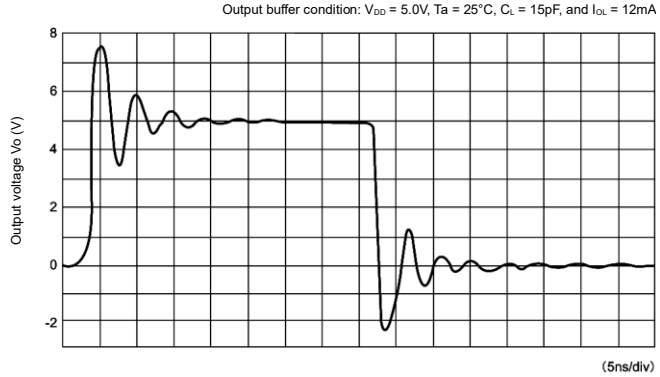


Figure A4.1-39

- Normal type output buffer waveform (HOB3T)

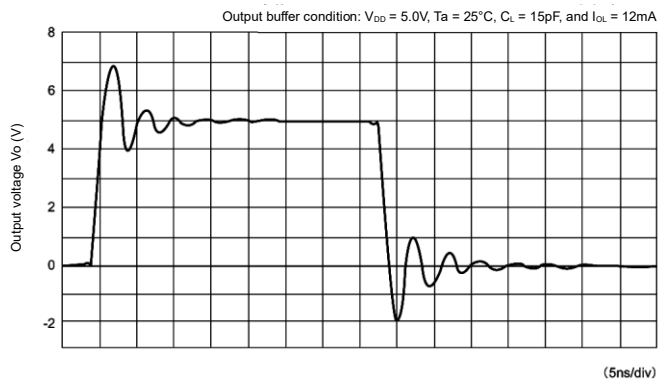


Figure A4.1-40

- Low noise type output buffer waveform (HOB3BT)

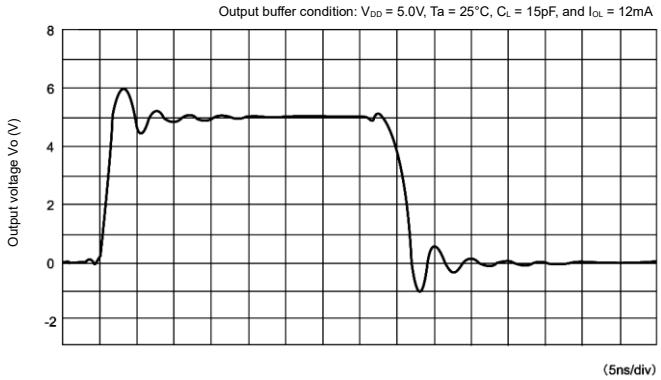


Figure A4.1-41

A4.2 3.3V Operation

A4.2.1 Output Current Characteristics (3.3V ±0.3V)

Table A4-2 Output Current Characteristics (3.3V ±0.3V)

	Output current	
Type No.	**I_{OL} (mA)**	**I_{OH} (mA)**
TYPE S	0.1	-0.1
TYPE M	1	-1
TYPE 1	2	-2
TYPE 2	6	-6
TYPE 3	12	-12
PCI	Conformed to the PCI Standard	

"S," "M," and "1" through "3" following "TYPE*" are the numbers indicated in the "XX*X" section of the names of output cells.
Example: OB3T indicates TYPE 3.

A4.2.2 Input Buffer Characteristics (3.3V ±0.3V)

- Standard cell buffer

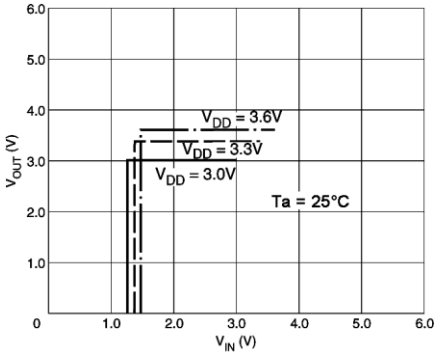


Figure A4.2-1 Input Characteristic (LVTTL Level)

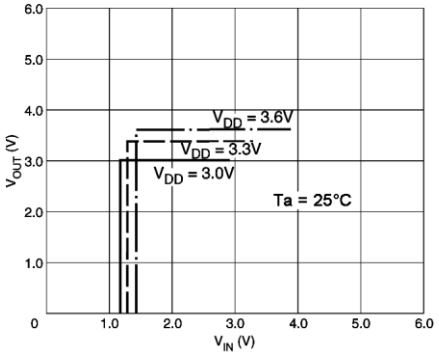


Figure A4.2-2 Input Characteristic (3V PCI Level)

- Schmitt trigger cell input buffer

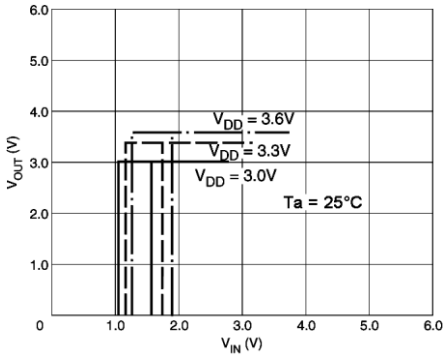


Figure A4.2-3 Input Characteristic (LVTTL Level)

A4.2.3 Delay Characteristics

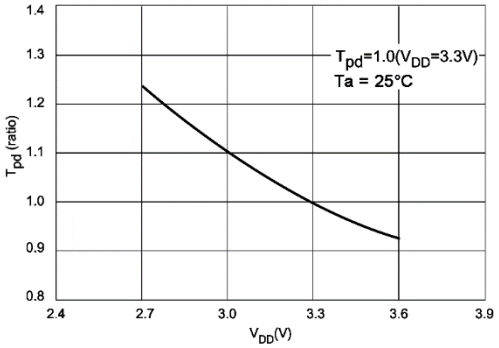


Figure A4.2-4 Propagation Time - Power Supply Voltage Characteristic

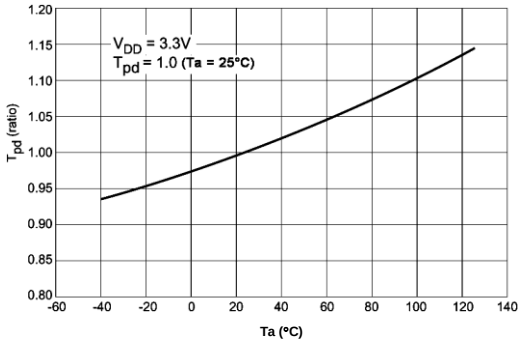


Figure A4.2-5 Propagation Time - Ambient Temperature Characteristic

A4.2.4 Output Driver Characteristics

- Low level output current

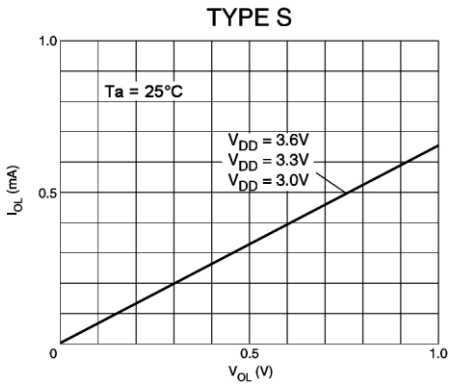


Figure A4.2-6

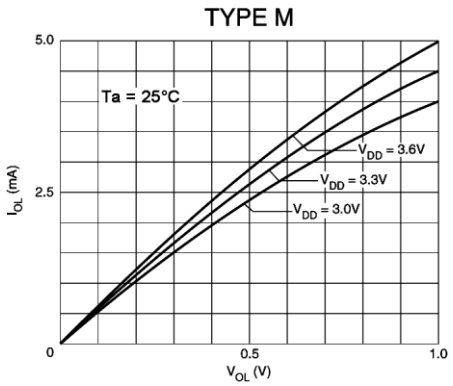


Figure A4.2-7

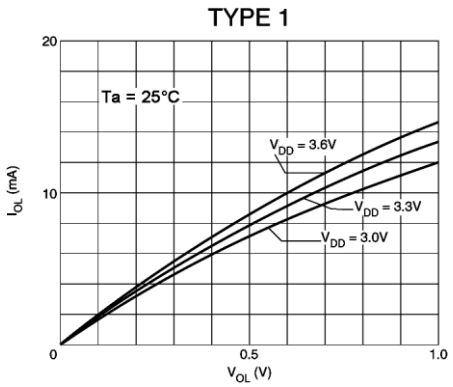


Figure A4.2-8

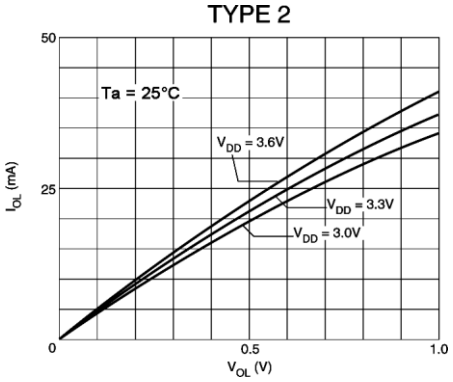


Figure A4.2-9

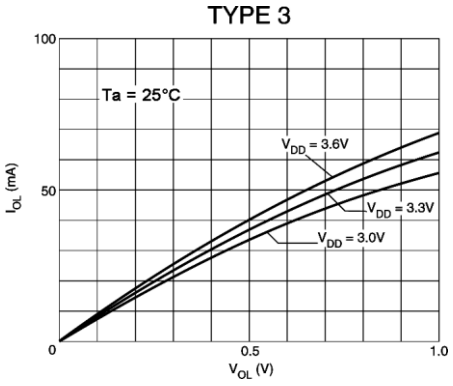


Figure A4.2-10

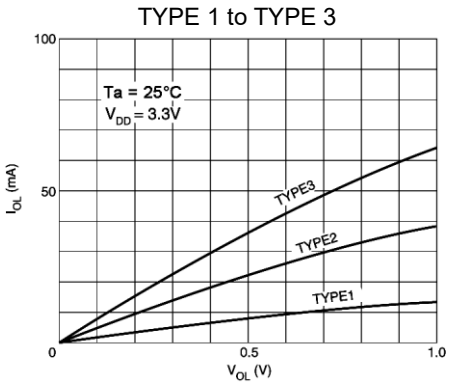


Figure A4.2-11

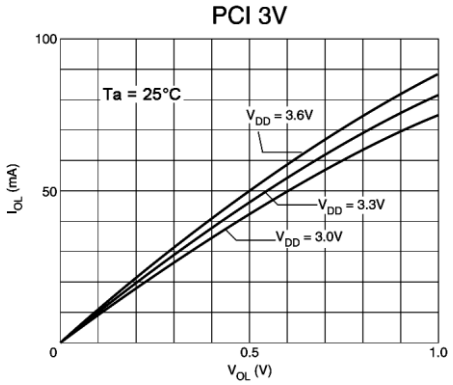


Figure A4.2-12

- High level output current

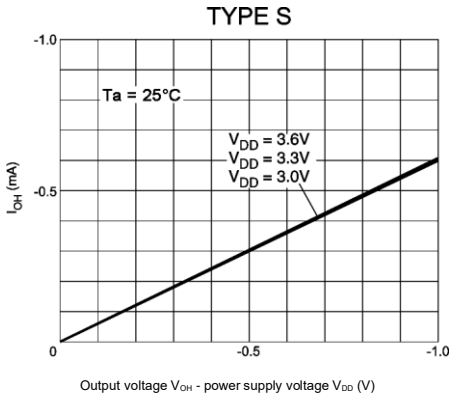


Figure A4.2-13

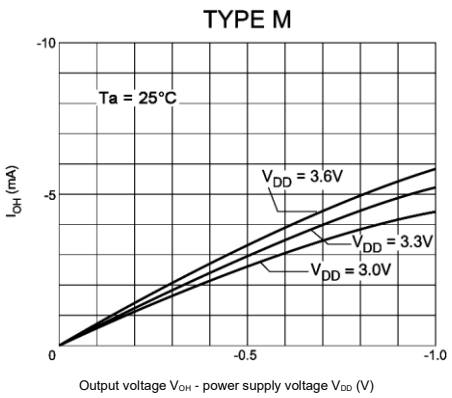


Figure A4.2-14

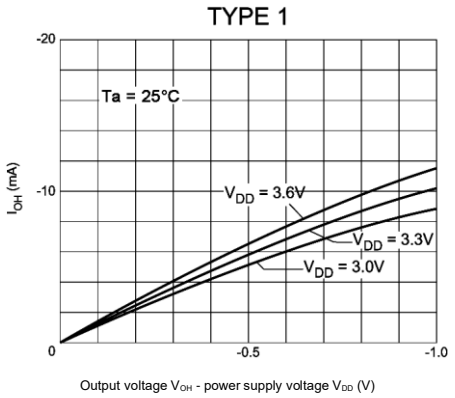


Figure A4.2-15

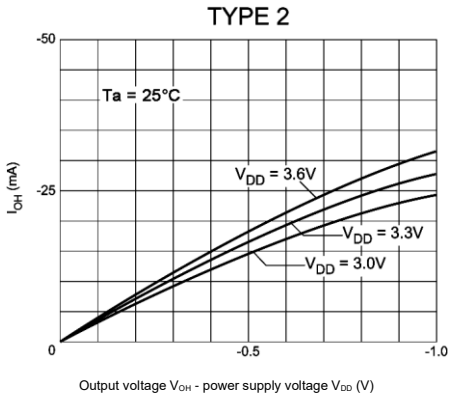


Figure A4.2-16

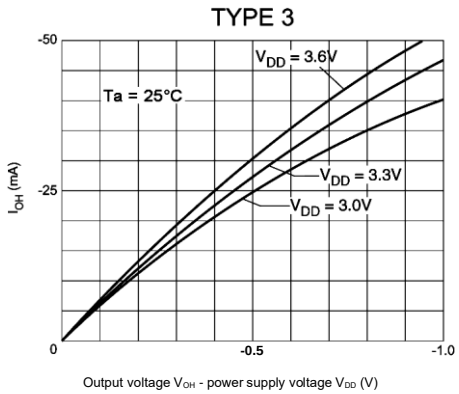


Figure A4.2-17

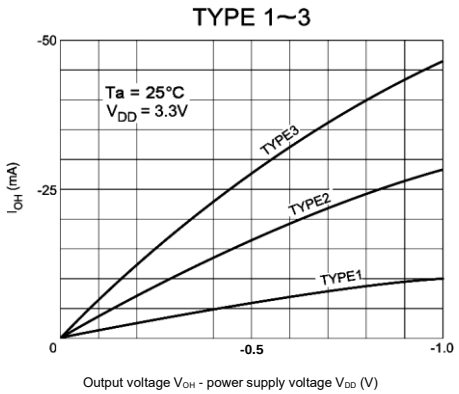


Figure A4.2-18

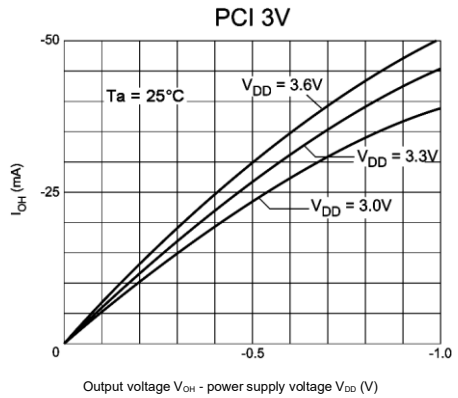


Figure A4.2-19

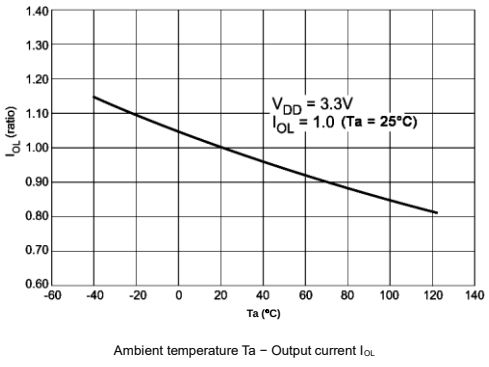


Figure A4.2-20

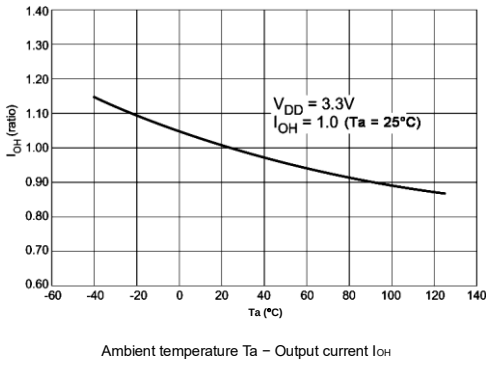


Figure A4.2-21

A4.2.5 Output Delay Time vs. Output Load Capacitance (C_L)

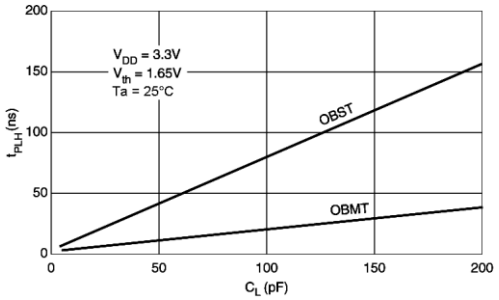


Figure A4.2-22 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

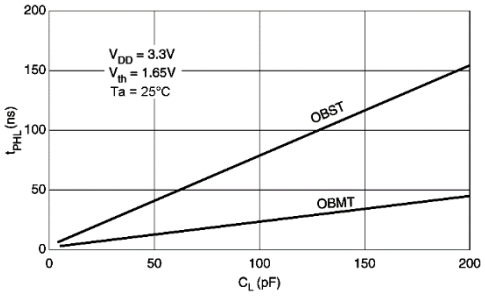


Figure A4.2-23 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

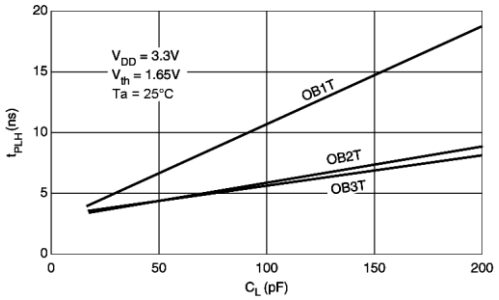


Figure A4.2-24 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

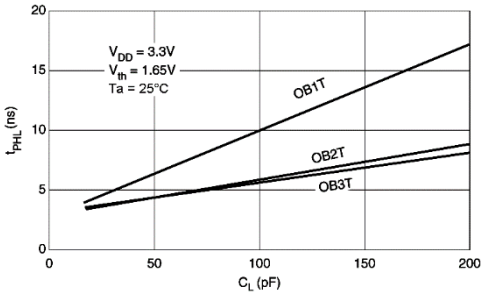


Figure A4.2-25 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

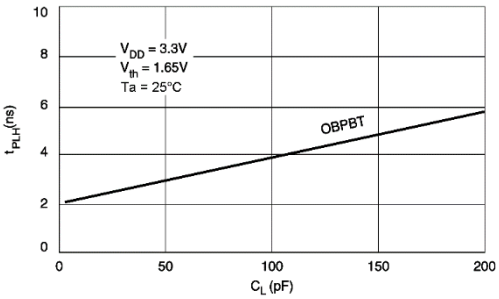


Figure A4.2-26 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

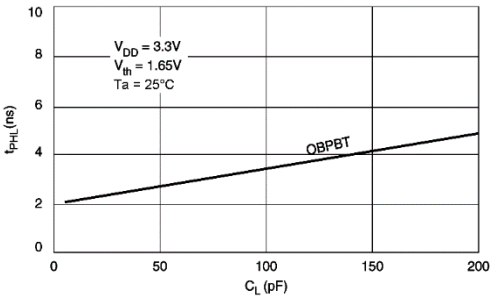


Figure A4.2-27 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

A4.2.6 Output Buffer Rising/Falling Time vs. Output Load Capacitance (C_L)

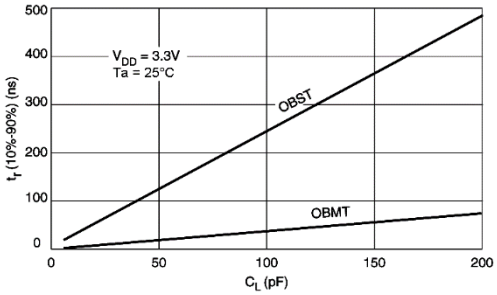


Figure A4.2-28 Rising Time (t_r) vs. Output Load Capacitance (C_L)

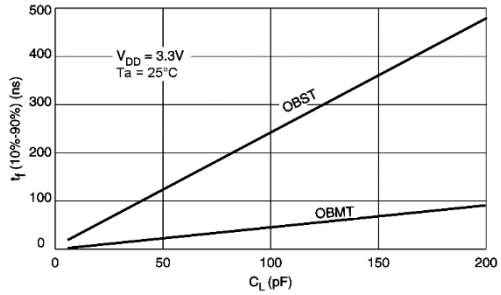


Figure A4.2-29 Falling Time (t_f) vs. Output Load Capacitance (C_L)

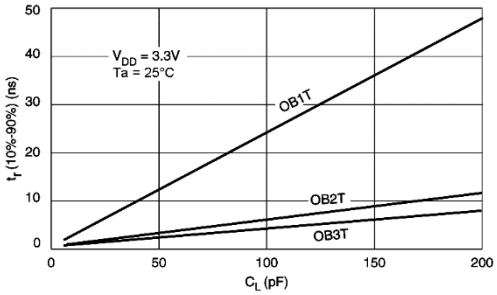


Figure A4.2-30 Rising Time (t_r) vs. Output Load Capacitance (C_L)

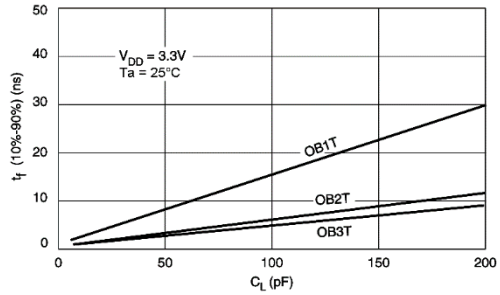


Figure A4.2-31 Falling Time (t_f) vs. Output Load Capacitance (C_L)

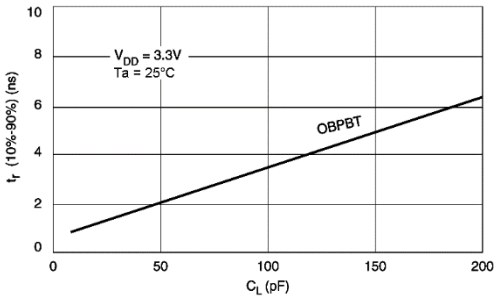


Figure A4.2-32 Rising Time (t_r) vs. Output Load Capacitance (C_L)

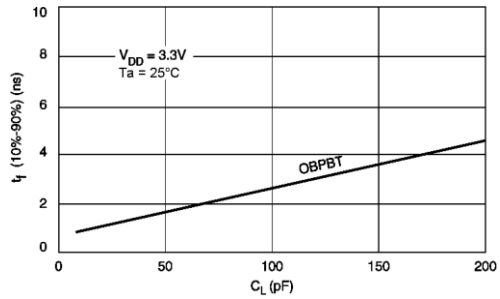


Figure A4.2-33 Falling Time (t_f) vs. Output Load Capacitance (C_L)

A4.2.7 Pull-up, Pull-down Resistance

- Pull-up characteristics

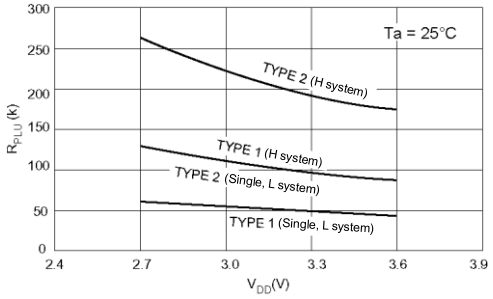


Figure A4.2-34 Power Supply Voltage Dependency of Pull-up Resistance

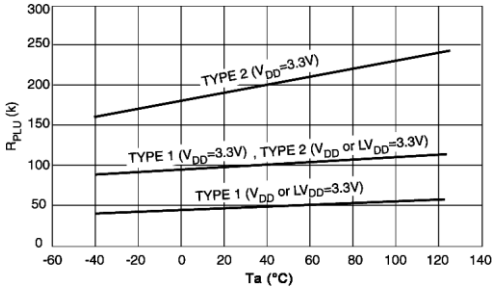


Figure A4.2-35 Ambient Temperature Dependency of Pull-up Resistance

- Pull-down characteristics

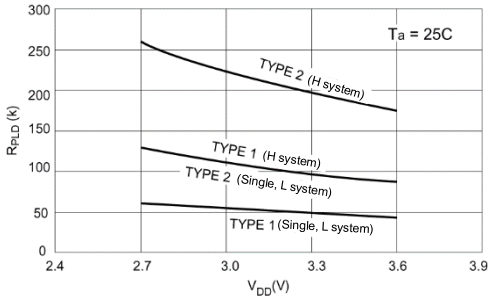


Figure A4.2-36 Power Supply Voltage Dependency of Pull-down Resistance

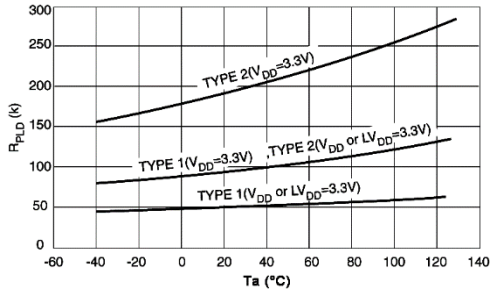


Figure A4.2-37 Ambient Temperature Dependency of Pull-down Resistance

A4.2.8 Power Consumption Characteristics

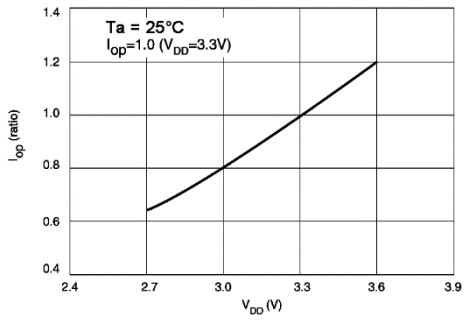


Figure A4.2-38 Power Supply Voltage Dependency of Power Consumption

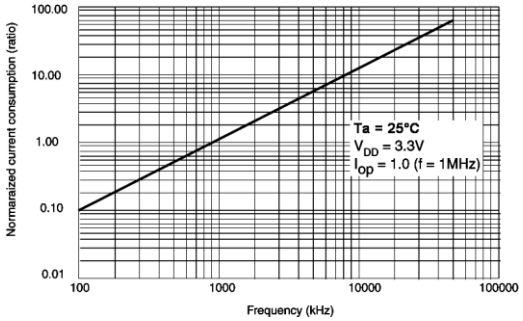


Figure A4.2-39 Operating Frequency Dependency of Power Consumption

A4.2.9 Output Waveforms

- High-speed type output buffer waveform (OB3AT)

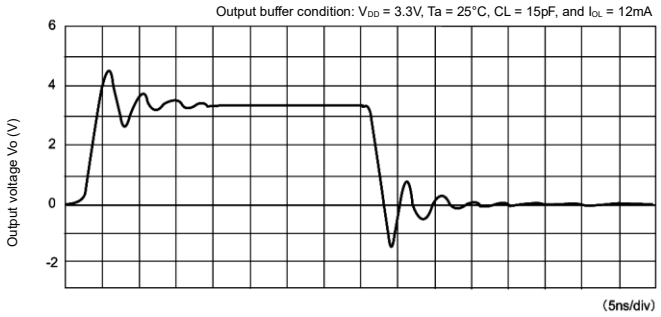


Figure A4.2-40

- Normal type output buffer waveform (OB3T)

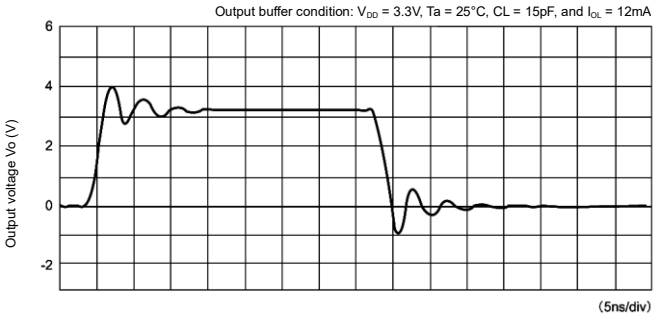


Figure A4.2-41

- Low noise type output buffer waveform (OB3BT)

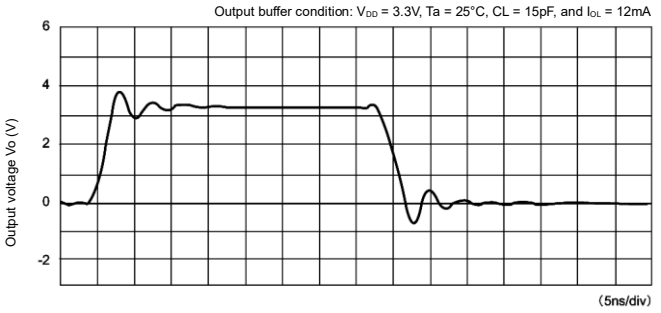


Figure A4.2-42

A4.3 Schmitt Input Buffer Electrical Characteristics

Figure A4-3 shows the electrical characteristics of Schmitt input buffers. VT+ and VT− are within the respective maximum and minimum specifications and vary depending on individual and environmental conditions. The difference between the two is more than the minimum value for VH.

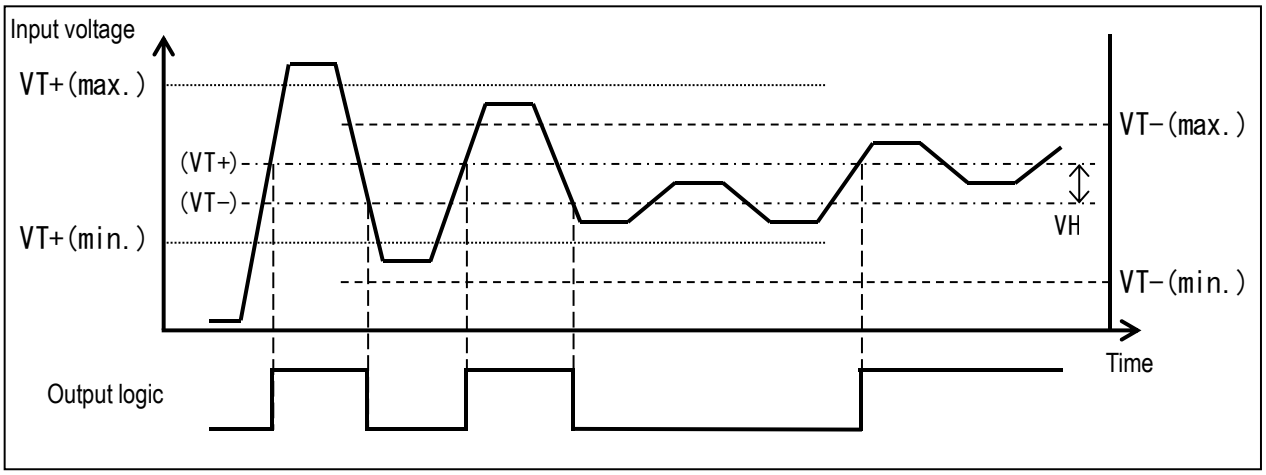


Figure A4-3 Correlation Between Input Voltage and Logic Values for Schmitt Input Buffers

VT+: Voltage at which High is detected when the input signal changes from Low to High

VT−: Voltage at which Low is detected when the input signal changes from High to Low

VH: Voltage difference required to detect the time point when a signal previously detected as High (or Low) changes to Low (or High)

Revision History

Attachment-1

Rev. No.	Year/Month	Page	Category	Revision Details (incl. previous details) and Reason for Revision
Rev.1.0	1998/04	All pages	New	New issue
Rev.1.1	2006/09	All pages	Revision	Overall reorganization, consistent with S1X60000 Series 404486609 Document final edition
Rev.1.2	2007/09	Specific pages	Revision	Appendix: Addition of I/O buffer characteristics graphs, etc. 404486610
Rev.2.0	2015/04	All pages	Revision	Overall reorganization, consistent with S1X50000 Series (RTL-I/F) 404486611
Rev.2.1	2015/06	Chapters 1 and 6	Revision	Table 1-8: Correction of values in Pull-up/Pull-down Resistance Table 6-32: Correction of values in Pull-down Resistance 404486612
Rev.2.2	2016/04	Appendix	Revision	A2: Addition of VHDL to Notes on RTL Design A3.1: Correction of Scan 404486613
Rev.2.3	2017/06	P.7-9	Revision	Tables 1-8 to 1-10: Correction of specification values in Electrical Characteristics
Rev.2.4	2017/06	P.3-6	Revision	Correction and addition of notes in 1.3.1 Absolute Maximum Ratings and 1.3.2 Recommended Operating Conditions
Rev.2.5	2017/12	P.86	Revision	Correction of fail-safe description in ② of 6.5.3 Notes on Usage
		P.89-90	Revision	Tables 6-21-2, 6-22-1, and 6-22-2: Correction of cell names
Rev.2.6	2019/04	Appendix	Revision	Correction of figures and tables in A5.1 and A5.2 A5.4: Addition to Schmitt Input Buffer Electrical Characteristics
Rev.3.0	2019/09	All pages	Revision	Overall reorganization
Rev.3.1	2020/05	All pages	Revision	Correction of errors
Rev. 3.2	2021/03	P.112	Revision	Change description of 9.2 Limit on power consumption
Rev. 3.3	2024/09	5.2 and 8	Revision	Delete 5.2 Internal Bus Configuration Revision of Chapter 8 RAM specifications

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Document Code: 404486910
First Issue April 1998
Revised September 2024 in JAPAN Ⓓ