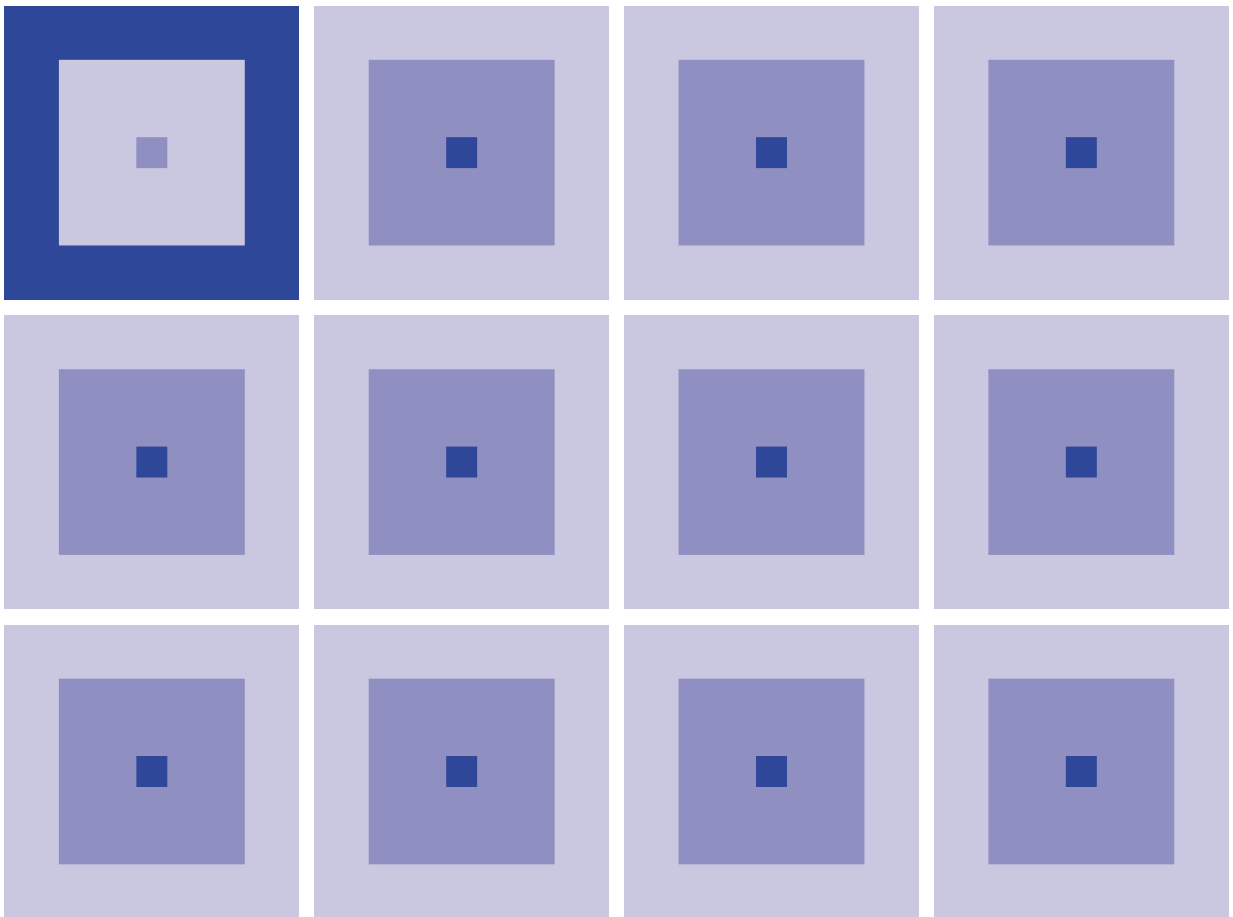
MF1244-03a

EPSON

GATE ARRAY

S1L50000 Series

2.5 Voltage Library DESIGN GUIDE



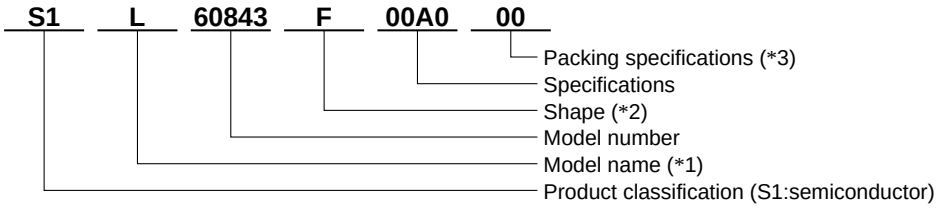
SEIKO EPSON CORPORATION

NOTICE

No part of this material may be reproduced or duplicated in any from or by any means without the written permission of EPSON. EPSON reserves the right to make changes to this material without notice. EPSON does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this marerial will be free from any patent or copyright infringement of a third party. This material or portions there of may contain techology or the subject relating to strategic products under the control of the Forign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of international Trade and Industry or other approval from another government agency.

Configuration of product number

●DEVICES



*1: Model name

K	Standard Cell
L	Gate Array
X	Embedded Array

*2: Shape

B	Assembled on board, COB, BGA
C	Plastic DIP
D	Bare Chip
F	Plastic QFP
H	Ceramic DIP
L	Ceramic QFP

M	Plastic SOP
R	TAB–QFP
T	Tape Carrier (TAB)
2	TSOP (Standard Bent)
3	TSOP (Reverse Bent)

*3: Packing Specifications

14th	15th	Packing Specifications
0	0	Besides tape & reel
0	A	TCP BL 2 directions
0	B	Tape & reel Back
0	C	TCP BR 2 directions
0	D	TCP BT 2 directions
0	E	TCP BD 2 directions
0	F	Tape & reel FRONT
0	G	TCP BT 4 directions
0	H	TCP BD 4 directions
0	J	TCP SL 2 directions
0	K	TCP SR 2 directions
0	L	Tape & reel LEFT
0	M	TCP ST 2 directions
0	N	TCP SD 2 directions
0	P	TCP ST 4 directions
0	Q	TCP SD 4 directions
0	R	Tape & reel RIGHT
9	9	Specs not fixed

CONTENTS

Introduction

This document entitled “Gate Array S1L50000 Series 2.5 Voltage Library Design Guide” describes how to use the cells of S1L50000 series at 2.5V±10% single power voltage or an internal voltage of 2.5V±10% and I / O buffers at 3.3V±0.3V. When using them at other voltage combinations, refer to “Gate Array S1L50000 Series Design Guide (MF1087-05)” in detail.

Chapter 1: Overview

The S1L50000 Series is a family of ultra high-speed VLSI CMOS gate arrays utilizing a 0.35µm "sea-of-gates" architecture.

1.1 Features

• Integration	A Max. of 815,468 gates (2 input NAND gate equivalent)
• Operating Speed	Internal gates: 170ps (2.5V Typ.) (2-input pair NAND, F/O = 2, Typical wire load) Input buffer: 400ps (3.3V Typ.) Built-in level shifter is used. 600ps (2.5V Typ.) (F/O = 2, Typical wire load) Output buffer: 2.02 ns (3.3 V Typ.) Built-in level shifter is used. 2.70 ns (2.5V Typ.) (C_L = 15pF)
• Process	0.35 µm 2/3/4 layer metalization CMOS process
• I/F Levels	Input/Output TTL/CMOS/LVTTL compatible
• Input Modes	CMOS, LVTTL, CMOS Schmitt, LVTTL Schmitt, PCI Built-in pull-up and pull-down resistors can be usable. (2 types for each resistor value)
• Output Modes	Normal, 3-state, bi-directional, PCI
• Output Drive	I_{OL} = 0.1, 1, 2, 6, 12mA selectable (at 3.3V) I_{OL} = 0.1, 0.5, 1, 3, 6mA selectable (at 2.5V)
• RAM	Asynchronous 1-port, asynchronous 2-port
• Dual Power	Operation supported by using level-shifter circuit Internal logic: operation supported by low voltage I / O Buffer: built-in interfaces of both high and low voltages possible

1.2 Master Structure

The S1L50000 Series comprises 12 types of masters, from which the customer is able to select the master most suitable.

Table 1-1 Overview

Master	Total BC (Raw Gates)	Number of Pads	Number of Columns (X)	Number of Rows (Y)	Cell utilization ratio(U)*1		
					2-layer metal	3-layer metal	4-layer metal
S1L50282/50283/50284	28710	88	319	90	50%	88%	95%
S1L50552/50553/50554	55500	124	444	125	47%	85%	95%
S1L50752/50753/50754	75774	144	519	146	47%	85%	95%
S1L50992/50993/50994	99198	168	594	167	47%	85%	95%
S1L51252/51253/51254	125772	188	669	188	45%	80%	95%
S1L51772/51773/51774	177062	224	794	223	45%	75%	95%
S1L52502/52503/52504	250160	264	944	265	45%	75%	95%
S1L53352/53353/53354	335858	308	1094	307	43%	75%	95%
S1L54422/54423/54424	442112	352	1256	352	40%	70%	90%
S1L55062/55063/55064	506688	376	1344	377	40%	70%	90%
S1L56682/56683/56684	668552	432	1544	433	40%	70%	90%
S1L58152/58153/58154	815468	480	1706	478	40%	70%	90%

NOTE: *1: This is the value when there are no cells, such as RAM cells. The cell use effciency is, dependent not only on the scope of the circuits, but also on the number of signals, the number of branches per signal, etc. ; thus, use the values in this table only as an estimate.

1.3 Electrical Characteristics and Specifications

Table 1-2 Absolute Max. Ratings (For Single Power Supplies)

(V_{SS}=0V)

Item	Symbol	Limits	Unit
Power Supply Voltage	V_{DD}	-0.3 to 4.0	V
Input Voltage	V_I	-0.3 to V_{DD} + 0.5*1	V
Output Voltage	V_O	-0.3 to V_{DD} + 0.5*1	V
Output Current/Pin	I_{OUT}	± 30	mA
Storage Temperature	T_{stg}	-65 to 150	°C

*1: Possibles to use from -0.3V to 7.0V of the open-drain systems of N channel, input buffer in the IDC and IDH systems and Fail-Safe cell.

Table 1-3 Absolute Max. Ratings (For Dual Power Supplies)

(V_{SS}=0V)

Item	Symbol	Limits	Unit
Power Supply Voltage	HV_{DD}	-0.3 to 7.0	V
	LV_{DD}	-0.3 to 4.0	V
Input Voltage	HV_I	-0.3 to HV_{DD} + 0.5*1	V
	LV_I	-0.3 to LV_{DD} + 0.5*1	V
Output Voltage	HV_O	-0.3 to HV_{DD} + 0.5*1	V
	LV_O	-0.3 to LV_{DD} + 0.5	V
Output Current/Pin	I_{OUT}	± 30 (± 50*2)	mA
Storage Temperature	T_{stg}	-65 to 150	°C

*1: Possibles to use from -0.3V to 7.0V of the open-drain systems of N channel, input buffer in the LIDC and LIDH systems or the HIDC and HIDH systems and Fail-Safe cell.

*2: Possibles to use for 24mA of output buffer.

Table 1-4 Recommended Operating Conditions (For Single Power Supplies)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	2.25	2.50	2.75	V
Input Voltage	V_I	V_{SS}	—	V_{DD}*1	V
Ambient Temperature	Ta	0 -40	25 25	70*2 85*3	°C
Normal Input Rising Time*4	t_{ri}	—	—	100	ns
Normal Input Falling Time*4	t_{fa}	—	—	100	ns
Schmitt Input Rising Time*4	t_{ri}	—	—	10	ms
Schmitt Input Falling Time*4	t_{fa}	—	—	10	ms

*1: Possibles to use 5.50V of the open-drain systems of N channel and input buffer in the IDC and IDH systems.
*2: The ambient temperature range is recommended for Tj= 0 to 85 °C
*3: The ambient temperature range is recommended for Tj= -40 to 125 °C
*4: This time represents the 10% to 90% change times of V_{DD}.

Table 1-5 Recommended Operating Conditions (For Dual Power Supplies)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (High Voltage)	HV_{DD}	3.00	3.30	3.60	V
Power Supply Voltage (Low Voltage)	LV_{DD}	2.25	2.50	2.75	V
Input Voltage	HV_I	V_{SS}	—	HV_{DD}*1	V
	LV_I	V_{SS}	—	LV_{DD}*1	
Ambient Temperature	Ta	0 -40	25 25	70*2 85*3	°C
Normal Input Rising Time*4	Ht_{ri}	—	—	50	ns
	Lt_{ri}	—	—	100	
Normal Input Falling Time*4	Ht_{fa}	—	—	50	ns
	Lt_{fa}	—	—	100	
Schmitt Input Rising Time*4	Ht_{ri}	—	—	5	ms
	Lt_{ri}	—	—	10	
Schmitt Input Falling Time*4	Ht_{fa}	—	—	5	ms
	Lt_{fa}	—	—	10	

*1: Possibles to use 5.50V of the open-drain systems of N channel and input buffer in the LIDC and LIDH systems or HIDC and HIDH systems.
*2: The ambient temperature range is recommended for Tj = 0 to 85 °C
*3: The ambient temperature range is recommended for Tj = -40 to 125 °C
*4: This time represents the 10% to 90% change times of V_{DD}.

Table 1-6 Electrical Characterisics

(HV_{DD}=3.3V±0.3V, V_{SS}=0V, Ta=-40 to 85°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-1	—	1	µA
Off State Leakage Current	I_{OZ}	—		-1	—	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1mA (Type S), -1mA (Type M) -2 mA (Type 1), -6mA (Type 2) -12mA (Type 3, Type 4) HV_{DD} = Min.		HV_{DD} -0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1mA (Type S), 1mA (Type M) 2mA(Type 1), 6mA (Type 2) 12mA (Type 3), 24mA (Type 4) HV_{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V_{IH1}	LVTTL Level, HV_{DD} = Max.		2.0	—	—	V
Low Level Input Voltage	V_{IL1}	LVTTL Level, HV_{DD} = Min.		—	—	0.8	V
High Level Input Voltage	V_{T1+}	LVTTL Schmitt		1.1	—	2.4	V
Low Level Input Voltage	V_{T1-}	LVTTL Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H1}	LVTTL Schmitt		0.1	—	—	V
High Level Input Voltage	V_{IH3}	PCI Level, HV_{DD} = Max.		1.8	—	—	V
Low Level Input Voltage	V_{IL3}	PCI Level, HV_{DD} = Min.		—	—	0.9	V
High Level Output Current	I_{OH3}	PCI Response V_{OH} = 0.90V, HV_{DD} = Min. V_{OH} = 2.52V, HV_{DD} = Max.		-36 —	— —	— -115	mA mA
Low Level Output Current	I_{OL3}	PCI Response V_{OL} = 1.80V, HV_{DD} = Min. V_{OL} = 0.65V, HV_{DD} = Max.		48 —	— —	— 137	mA mA
Pull-up Resistance *	R_{PU}	V_I = 0V	Type 1	40	100	(200) 240	kΩ
			Type 2	80	200	(400) 480	
Pull-down Resistance *	R_{PD}	V_I = HV_{DD}	Type 1	40	100	(200) 240	kΩ
			Type 2	80	200	(400) 480	
High Level Maintenance Current	I_{BHH2}	Bus Hold Response V_{IN} = 2.0V HV_{DD} = Min.		—	—	-20	µA
Low Level Maintenance Current	I_{BHL2}	Bus Hold Response V_{IN} = 0.8V HV_{DD} = Min.		—	—	17	µA
High Level Reversal Current	I_{BHHO2}	Bus Hold Response V_{IN} = 0.8V HV_{DD} = Max.		-350	—	—	µA
Low Level Reversal Current	I_{BHLO2}	Bus Hold Response V_{IN} = 2.0V HV_{DD} = Max.		210	—	—	µA
Input Terminal Capacitance	C_I	f = 1MHz, HV_{DD} = 0V		—	—	10	pF
Output Terminal Capacitance	C_O	f = 1MHz, HV_{DD} = 0V		—	—	10	pF
Input/Output Terminal Capacitance	C_O	f = 1MHz, HV_{DD} = 0V		—	—	10	pF

* The values parenthesized means in case of Ta= 0 to 70°C.

Table 1-7 Electrical Characteristics

(V_{DD} or LV_{DD} = 2.5V ± 0.25V, V_{SS} = 0V, Ta = -40 to 85°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-1	—	1	µA
Off State Leakage Current	I_{OZ}	—		-1	—	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1mA (Type S), -0.5mA (Type M) -1mA (Type 1), -3mA (Type 2) -6mA (Type 3) V_{DD} or LV_{DD}= Min.		V_{DD} or LV_{DD} -0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1mA (Type S), 0.5mA (Type M) 1mA(Type 1), 3mA (Type 2) 6mA (Type 3), V_{DD} or LV_{DD}= Min.		—	—	0.4	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} or LV_{DD} = Max.		1.7	—	—	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} or LV_{DD} = Min.		—	—	0.7	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		0.6	—	1.7	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.7	—	1.3	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0.03	—	—	V
Pull-up Resistance*	R_{PU}	V_I = 0V	Type 1	25	75	(150) 180	kΩ
			Type 2	50	150	(300) 360	
Pull-down Resistance*	R_{PD}	V_I = V_{DD} or LV_{DD}	Type 1	25	75	(150) 180	kΩ
			Type 2	50	150	(300) 360	
High Level Maintenance Current	I_{BHH2}	Bus Hold Response V_{IN} = 1.7V V_{DD} or LV_{DD} = Min.		—	—	-5	µA
Low Level Maintenance Current	I_{BHL2}	Bus Hold Response V_{IN} = 0.7V V_{DD} or LV_{DD} = Min.		—	—	5	µA
High Level Reversal Current	I_{BHHO2}	Bus Hold Response V_{IN} = 0.7V V_{DD} or LV_{DD} = Max.		-280	—	—	µA
Low Level Reversal Current	I_{BHLO2}	Bus Hold Response V_{IN} = 1.7V V_{DD} or LV_{DD} = Max.		170	—	—	µA
Input Terminal Capacitance	C_I	f = 1MHz, V_{DD} or LV_{DD} = 0V		—	—	10	pF
Output Terminal Capacitance	C_O	f = 1MHz, V_{DD} or LV_{DD} = 0V		—	—	10	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1MHz, V_{DD} or LV_{DD} = 0V		—	—	10	pF

* The values parenthesized means in case of Ta + 0 to 70°C.

Table 1-8 Quiescent Current (For Single Power Supplies)

(Tj= 85°C)

Master	2.5V ± 0.25V I_{DDS} Max.	Unit
S1L50282/50283/50284 S1L50552/50553/50554 S1L50752/50753/50754 S1L50992/50993/50994	33	µA
S1L51252/51253/51254 S1L51772/51773/51774 S1L52502/52503/52504	84	µA
S1L53352/53353/53354 S1L54422/54423/54424 S1L55062/55063/55064	160	µA
S1L56682/56683/56684 S1L58152/58153/58154	242	µA

Table 1-9 Quiescent Current (For Dual Power supplies)

(Tj= 85°C)

Master	3.3 V ± 0.3V HI_{DDS} Max.	2.5 V ± 0.25 V LI_{DDS} Max.	Unit
S1L50282/50283/50284 S1L50552/50553/50554 S1L50752/50753/50754 S1L50992/50993/50994	25	33	µA
S1L51252/51253/51254 S1L51772/51773/51774 S1L52502/52503/52504	35	84	µA
S1L53352/53353/53354 S1L54422/54423/54424 S1L55062/55063/55064	50	160	µA
S1L56682/56683/56684 S1L58152/58153/58154	60	242	µA

HI_{DDS}: The quiescent current between HV_{DD} and V_{SS}
LI_{DDS}: The quiescent current between LV_{DD} and V_{SS}

* The value of quiescent current, except when chip temperature Tj=85°C, can be estimated from the following formula: (Tj = - 40 to 85°C. For Tj=125°C, the estimated quiescent current is calculated from the temperature coefficient = 12. For Tj = 85 to 125°C, please consult Seiko Epson or its distributor.)

$$I_{DDS}(Tj) = I_{DDS}(Tj=85°C) \times \text{Temperature coefficient}$$
$$= I_{DDS}(Tj=85°C) \times 10^{\frac{Tj - 85}{60}}$$

(Example) The value of quiescent current of S1L55062 for V_{DD} = 2.5V ± 0.25V and Tj = 50°C is estimated.

$$I_{DDS}(Tj=50°C) = I_{DDS}(Tj=85°C) \times 10^{\frac{50 - 85}{60}}$$
$$= 160 \times 0.261$$
$$= 41.76\ (\mu A)$$

** For the case of dual power supplies, the sum of the quiescent current for both of the voltages used is given as the total quiescent current (HI_{DDS} + LI_{DDS}).

1.4 Overview of Gate Array Development Flow

Gate arrays are developed jointly by the customer and EPSON. System design, circuit design, and test pattern design is performed by the customer, based on various reference materials, including the cell libraries provided to the customer by EPSON.

Various modes of interface, listed below, are possible between the customer and EPSON during design, depending on the stage in gate array development wherein the customer interfaces with EPSON.

When interfacing with EPSON, the customer is to provide the necessary data and documents to EPSON.

Customers are expected to perform simulation, analysis, and other necessary work on the target project using available software and EPITS (*1) or Auklet (*2) by Seiko Epson. When the customer has completed this work, Seiko Epson will undertake placement and wiring work on that project.

Note 1: EPITS is Seiko Epson's ASIC design support system that runs on an MS-Windows NT4.0 or SUN-Solaris platforms. It does not include any simulation or synthesis functions.

Note 2: Auklet is Seiko Epson's ASIC design support system that runs on an MS-Windows 95/98 or NT4.0.

The following lists the EDA software that EPITS currently supports:

- Verilog-XL (*1)
- ModelSim (*2)

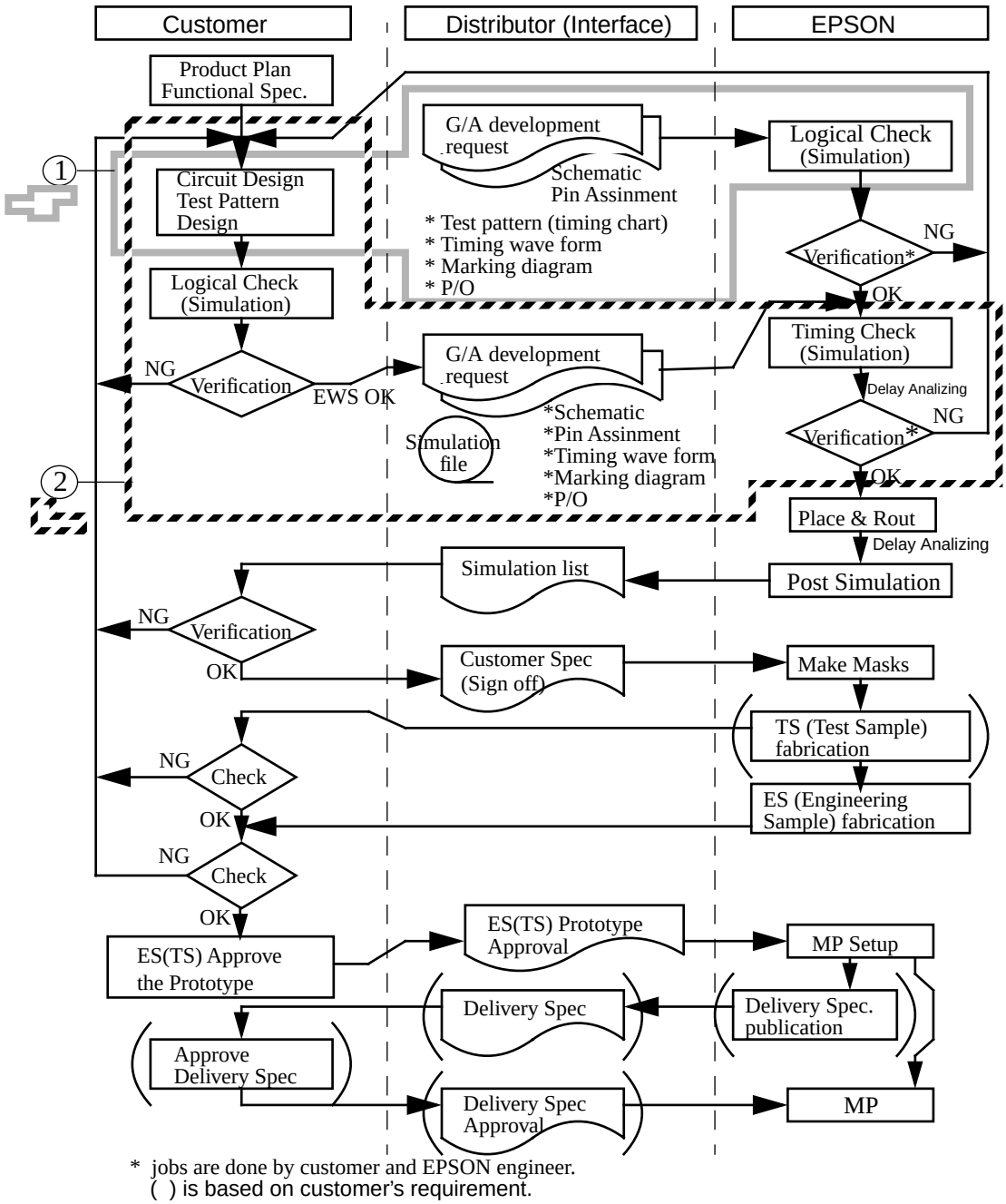
The following lists the EDA software that Auklet currently supports:

- Verilog-XL
- Polaris (*3)

Note) *1 : Verilog-XL is a registered trademark of Cadence Desgin Systems Corporation, USA.
*2: ModelSim is a registered trademark of Mentor Graphics of the U.S.
*3: Polaris is a registered trademark of AVANT! of the U.S.

For more information, refer to the Gate Array Technical Guide or contact to our sales office for technical support.

The process flow of the gate array development process is shown below:



NOTE: When the customer performs all tasks to the point of logical simulations and delay simulations on engineering workstations, etc., the route taken is (2). When EPSON performs the logical simulations, the route taken is (1).

Chapter 2: Estimating Gate Density and Selecting the Master

Methods and guidelines are described below to assist in defining the logic which will be integrated into a gate array, estimating the array requirements, and determining the appropriate master for a given application.

2.1 Dividing Up Logic Between Chips

When extracting logic, which is to be integrated into gate arrays from the system being created by the user, the logic should be selected with the following criteria in mind.

- Integration Criteria
  - (1) Logic size to be integrated (Gate count)
  - (2) Number of I /O pins required (Pin count)
  - (3) Package to be used
  - (4) Power consumption

Generally, the larger the gate size, the more power is consumed, and the more input and output terminals required. Because of this, it may be better, from the perspective of total cost or from the perspective of power consumption, etc., to divide the circuit into multiple chips, rather than forcing them into a single chip.

2.2 Determining Gate Size

In the case of gate arrays, the scope of the array is defined as the sum of gates or basic cells (BCs) used. One gate or basic cell is typically defined as being equivalent to one two-input NAND gate (or four transistors). The “Gate Array S1L50000 Series MSI Cell Library” can be used as reference to facilitate gate count estimation.

2.3 Estimating the Number of Input/Output Pins

Defining the number of I/O signals, test signals and power pins required for a given application has a bearing on the array member suitable for that application. The appropriate number of I/O pads must be available on the array member to satisfy the application signal requirements. Estimate the number of power supply pins using the method discussed in Chapter 10.

2.4 Selecting the Master

Select the appropriate master from Table1.1, based on the estimated number of BCs, the number of required input and output pins (including power supply pins) and the package to be used.

The actual number of BCs (BC_A) which can be used for each device type is estimated using the following formula from the gross number of BCs (BC_G) loaded on each master (shown in Table 1.1 of the previous chapter) and the cell utilization ratio (U).

$$BC_A = U \times BC_G$$

where U = 0.40 to 0.50 for double layer metal (DLM) or
U = 0.70 to 0.88 for triple layer metal (TLM)
U = 0.90 to 0.95 for four layer metal (FLM)

NOTE: When a RAM circuit is included, this estimate should be made after refering to the following section and after refering to Chapter 5. Also when a circuit is used by dual power, the estimate should be made after refering to Chapter 11.

2.5 Estimating the BCs That can be Used in Circuits Which Include RAM

RAM blocks, in comparison to MSI cells, are extremely large and have fixed shapes (defined vertical and horizontal dimensions). Because of this, some RAM blocks which may appear to fit on the chip because of calculations based on the number of BCs may, in actuality, not be placable on a given master. Thus, the first decision is that of whether or not the RAM configuration is available on a given master. Please refer to Chapter 5.

Once the masters which can accommodate the RAM have been selected, it becomes possible to estimate the number of BCs (BC_{AWR}) of random logic (excluding RAM) available using the formula below.

$$BC_{AWR} = 0.9 \times U \times (BC_G - BC_{RAM})$$

where BC_{AWR} is the number of BCs available for random logic
BC_G is the total BCs available on a mater (raw gates)
BC_{RAM} is the BC use of RAM(s) (See Chapter 5 for BC calculation)
U is the utilization ratio.

NOTE: Actual BCs available (BC_{AWR}) is design dependent.
Use the formula above for estimation purposes only.
Please consult EPSON for design specific information.

Chapter 3: Cautions and Notes Regarding Circuit Design

3.1 Inserting I/O Buffers

All external (or primary) input, output and bi-directional signals must be attached to I/O buffers. Due to CMOS IC's extreme vulnerability to electrical static discharge (ESD), protection circuitry has been incorporated within the I/O buffers to ensure device reliability and quality.

3.2 The Use of Differentiating Circuits is Forbidden

The propagation delay (t_{pd}) of internal cells within a gate array vary, depending on process variance during mass production and environment variance during device usage. Differentiating circuits such as the one shown in Figure 3.1 should be avoided due to difficulties associated with control of the resultant pulse width relative to variances in propagation delays through each logic element .

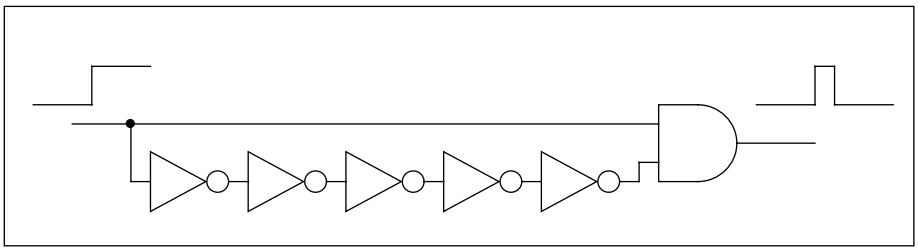


Figure 3-1 Example of a Differentiating Circuit

3.3 Wired Logic is Forbidden

Wired logic, available in bipolar devices, is not allowable in the S1L50000 Series, a CMOS technology. Consequently, cell output pins cannot be wired together, such as shown in Figure 3.2, with the exception of internal 3-state bus elements.

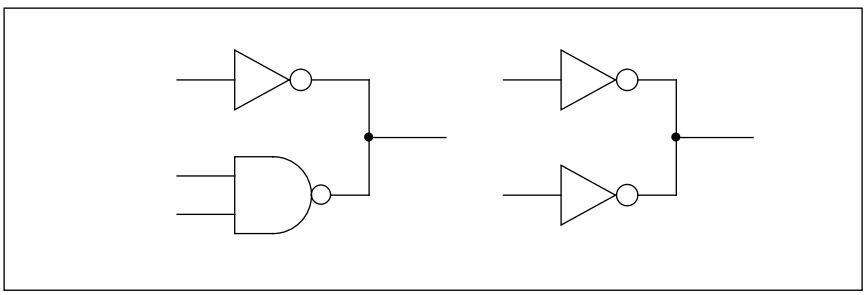


Figure 3-2 Examples of Forbidden Wired Logic

3.4 Hazard Countermeasures

In circuits such as decoders and multiplexors which are structured from combinational functions such as NAND gates or NOR gates, extremely short pulses can be produced by differences in the gate delay times. These short pulses are called hazards, and when these hazards propagate to clock, reset or set pins of sequential elements, malfunctions may occur.

Because of this, it is necessary to use caution when designing circuits which may produce hazards, creating circuit structures which do not propagate hazards, having decoder circuits with “enable” terminals, etc.

3.5 Fan-out Constraints

Cell propagation delay is determined, in part, by the load capacitance at the output terminals. When the load capacitance is too large, the propagation delay increases, and malfunctions may result. Because of this, there are limitations on the number of loads which can be connected to the output terminals of each cell, and these limitations are referred to as “fan-out constraints.”

The input terminal capacitance of each gate differs from gate input to gate input. The input capacitance of each gate input is defined relative to the input capacitance of an inverter (which is defined as being equal to 1) is called the “fan-in.”

Circuits should be designed so that the sum of the fan-ins connected to the output terminals of each gate does not exceed the fan-out constraints of that output terminal.

Also, high speed clock lines (40 MHz or more), should be designed so that the output terminal load of the associated logic gates is about half of the fan-out constraints to ensure high performance.

3.6 Bus Circuits

Internal 3-state bus circuits are constructed, using 3-state logic gates. The 3-state logic gates output terminals can be wired together if at all times one, and only one 3-state logic gate is active at a given time (while the remaining 3-state logic gate outputs are put in high impedance state). This circuit allows multiple signal sources to share a given net at different time intervals during circuit operation.

Please keep the following recommendations in mind when bus circuits are used:

Notes Regarding the Use of Bus Circuits:

(1) Bus cells cannot be used except in bus circuits. (Please refer to Table 3.1 regarding S1L50000 Series bus cells.)

(2) When bus cells are used, please attach one (and only one) BLT cell (bus latch) to each 3-state bus net.

(3) A maximum of 32 bus cells can be attached to a single bus. (Fan-out = 32)

(4) One, and only one, 3-state cell can be active (output terminal driving a logic 0 state or logic 1 state) at a time. All other 3-state bus cells connected to that net must be inactive (output terminal in high impedance Z state).

(5) If all 3-state bus cells are inactive (output terminals in high impedance Z state) on a given bus net, the BLT (bus latch) will maintain the last valid state (either logic 1 state or logic 0 state). The BLT function is merely to avoid bus floating, therefore, the processing of internal 3-state bus latch data must be performed while 3-state bus drivers are active rather than processing data while BLTs control bus data.

(6) In order to improve testability, design the 3-state bus such that it can be initialized easily and quickly during device testing. This can be done by utilizing a separate test pin to control the 3-state bus, or by instantiating default 3-sate bus drivers.

(7) The 3-state cell control terminals must change only once during a single test vector event (cycle) to allow test vector set usage during IC device testing.

(8) High speed 3-state bus operation may be inhibited by large fan-out loading on 3-state bus drivers.

Table 3.1 shows a table of the bus cells which can be used in the S1L50000 Series.

Table 3-1 S1L50000 Series Bus Cells

Cell Type	Cell Name		
	1 Bit	4 Bit	8 Bit
Bus latches	BLT 1	BLT 4	BLT 8
Bus drier	TSB, TSBP	T244H	T244
Inverting bus driver	TSV, TSVP	T240H	T240
Transparent latches with reset and 3-state output	—	T373H	T373
D-flip flops with rest and 3-state output	—	T374H	T374
1-bit RAM	RM1	—	—

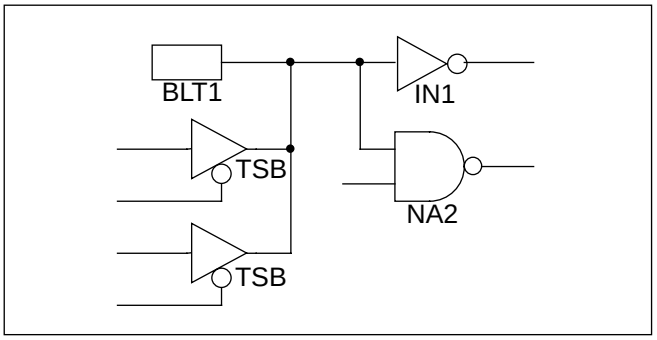


Figure 3-3 Example of Bus Cell Circuit Structure

3.7 Schematic Capture Guidelines

Please adhere to the following conventions when designing an ASIC via manual schematic entry:

- Use logic cells found in “Gate Array S1L50000 Series MSI Cell Library”.
- Use orthogonal (not oblique) connections when wiring logic cells to one another.
- Primary uni-directional I/O and bi-directional I/O signal names must be 2 to 32 characters in length, and must begin with an alphabetic character.

3.8 Bus Hold Circuits

In the S1L50000 Series, I/O buffers with an added bus hold function (to maintain the output signal pin data) have been provided, so that output signal pin (or bi-directional signal pin) does not enter high-impedance state.

However, to prevent these circuits from affecting normal operation, the latching capability of the bus hold circuit is weak; thus, the stored data output should not be used as valid data. This pin state can be overriden easily by an externally supplied signal.

Moreover, the bus hold circuit is disabled in test mode when the AC and DC recommended test circuitry described in Chapter 6.5 is used.

Please refer to the S1L50000 Series electrical characteristics in Tables 1-6 and 1-7 regarding the output maintenance current of the bus hold circuit. Figure 3-4 shows examples of structures of the bus hold circuits.

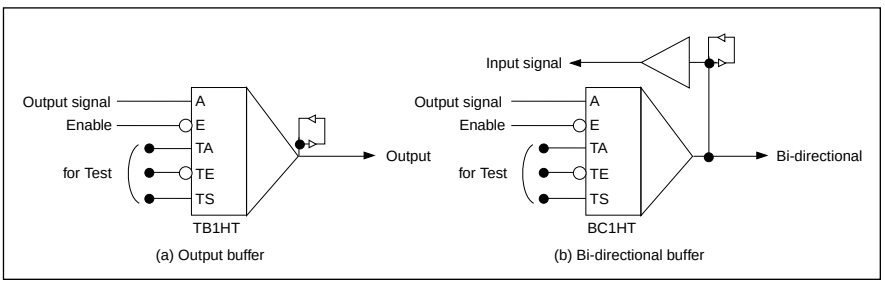


Figure 3-4 Examples of Structures of Bus Hold Circuits

3.9 Clock Tree Synthesis

(1) Overview

Clock Tree Synthesis is a support that automatically inserts the ClockTree into the buffer group that optimizes the skew and delay time of "ClockLine". If a customer has a program to insert ClockTree to adjust the Fan-out of "ClockLine", clock skew may be large, so the P & R tool is started and the placing and routing for designing the gate array are executed voluntarily. Also, the propagation delay time may be longer than estimated because there are many cases it is difficult to maintain a good balance between the wire interconnecting load and the intrinsic cell delay. The Clock Tree Synthesis is used to solve this problem. Refer to the actual results to use the Clock Tree Synthesis as follows:

Table 3-2 S1L35000, Number of Gates: 16K

Net Name	Number of driving cells	Skew value	Delay value	Additional number of cells	Number of stages
netA	4453	187ps	4804ps	104	6

(2) How to Examine the Clock Tree Synthesis

When the clock tree is inserted automatically, the customer must insert the special buffer to the Clock Line for the following three purposes.

- Judging the place to insert the Clock Tree Synthesis.
- Estimating the delay time of the Clock Tree inserted and execute the simulation of virtual wire interconnecting level (pre-simulation).
- Back annotate the delay time of the inserted Clock Tree to accurately estimate the post-simulation.

Select the special buffer for the Clock Tree Synthesis in the table of special buffers mentioned later.Then insert the special buffer selected from the table into the Clock Line taking into consideration the restriction or notes mentioned later and the same placing as the normal cells. Otherwise, if the logic are designed by HDL, as the special buffer can not insert automatically the Clock Line, assign directly the HDL of the content using the script language. Note that another buffer is not combined in the clock Line inserted in the special buffer, and execute the following command:

set_don’t_touch_net *net_name*

[The special buffer]

Select the special buffer from the table below corresponding to the estimated number of fan-outs.

S1L9000F, S1L30000, S1L50000 Series		
Cell Name	To Max. (ns)	Estimated number of fan-out
CRBF2	2.00	0 to 500
CRBF3	3.00	500 to 3000
CRBF4	4.00	3000 to 10000
CRBF5	5.00	Over 10000
CRBF6	6.00	
CRBF7	7.00	
CRBF8	8.00	

S1L35000 Series		
Cell Name	To Max. (ns)	Estimated number of fan-out
XCRBF2	2.00	0 to 500
XCRBF3	3.00	500 to 3000
XCRBF4	4.00	3000 to 10000
XCRBF5	5.00	Over 10000
XCRBF6	6.00	
XCRBF7	7.00	
XCRBF8	8.00	

Note 1: The value "K" (load delay of fan-out) of these cells is set "0" at the pre-simulation.
Note 2: The number of fan-outs of these cells is set to the infinity.
Note 3: Please consider that the load delay for the number of fan-outs is not accurately and only estimated.

[Restriction and Notes]

- Target series: S1L9000F, S1L30000, S1L35000, S1L50000
- The special buffer can not be used for any purpose other than the Clock Tree Synthesis.
- The Clock Tree Synthesis can also be used for data line and other control signals.
  However, when the nets used in the synthesis are increased, the skew and propagation delay also became larger. Therefore, the number of nets to be used in the synthesis is less than 10 and the net which has a critical and large fan-out should be used.
- If a net which has a small fan-out is used for the Clock Tree Synthesis, the propagation delay and skew may be larger. The target net with fan-out should be used more than scores.
- As there are cases corresponding to the skew adjustment between multiple Clock lines, contact EPSON for handing in the detail schematic (the clock line configuration is described very clearly) to be checked.
- For the Clock group separated into multiple Clock Lines with the same Root of Clock by the gates, contact EPSON to obtain the materials of "Gated Clock Tree Synthesis Explanations".

[Necessary Information from a Customer]

Send the following information until the data is released, because the Clock Tree Synthesis is used efficiently.

Instance name of CRBF*	Target skew value	Target propagation delay

Note 1: The target values on the table are needed to estimate to use the Synthesis. The target values are not always satisfied.
Note 2: If there is no target values, write the comments for each item in the table.
Example: As smaller as possible

[Imaging schematic]

The schematic created by a customer and the layout schematic after executing the Clock Tree Synthesis in EPSON are shown as follows:

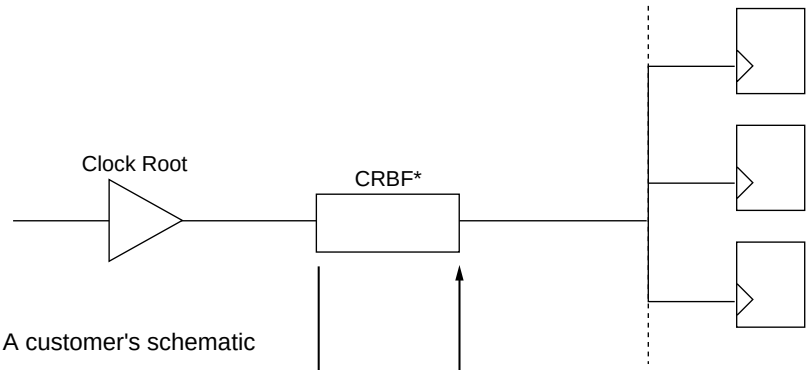


Figure 3-5 A customer's schematic

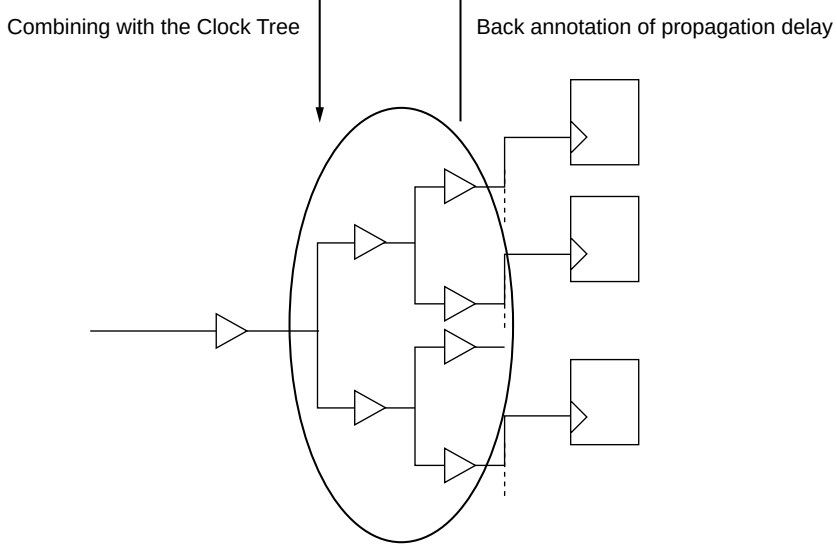


Figure 3-6 Layout schematic after executing the Clock Tree Synthesis in EPSON

3.10 ATPG (Auto Test Pattern Generation)

(1) Introduction

The so-called “ATPG” means tools to automatically generate test patterns that are released by tool-producing vendors. The “TestGen” of the tool executed to “ATPG” supplied by Synopsys Inc. is used in ASIC design at EPSON. By using “TestGen”, the scanning circuit can be inserted to the original circuit and the test patterns can be generated automatically.

The word “control” described in this chapter is used to specify free level to the target pin without passing to the sequential circuit. This “control” meaning should be noted because it can not be used for dividing clocks and so on needed in some cycles to set the state. For example, when using "control" where a clock of each flip-flop circuit can be controlled externally, the circuit means that the external input clock (source clock) can reach each flip-flop circuit.

(2) Outline

When the scanning circuit is inserted into the design ruled circuit for “ATPG” support, some faults are detected in the circuit when using the “ATPG” tool. However, internal nodes are forced to move from external pins through the scanning circuit and are observed. Therefore, the test patterns outputted from the “ATPG” tool can not be used to check the operations of the user’s circuit.

Users need to create the test patterns to check the standard operations of their circuit. The test patterns outputted from the “ATPG” tool can only be used to reach the level of the fault detecting rate in the circuit.

When using the “ATPG” tool, the test patterns to get 100% of fault detecting can be generated, except that nodes can not to be tested and faults can not be tested logically. The “ATPG” method is adapted to full scanning using “MUXSCAN type FF (Flip-flop)”.

(3) Fault Detecting Definition

The single stuck-at fault mode is used.

SA0: stack-at-zero fault (shorted)
SA1: stack-at-one fault (shorted)

The following test pattern circuit is created using TestGen of the ATPG tool.

The circuit set to SA0, SA1 to respective nodes is created to observe detection of faults. In other words, a test pattern circuit should be created that causes malfunctions when each node is set to “0” or “1”.

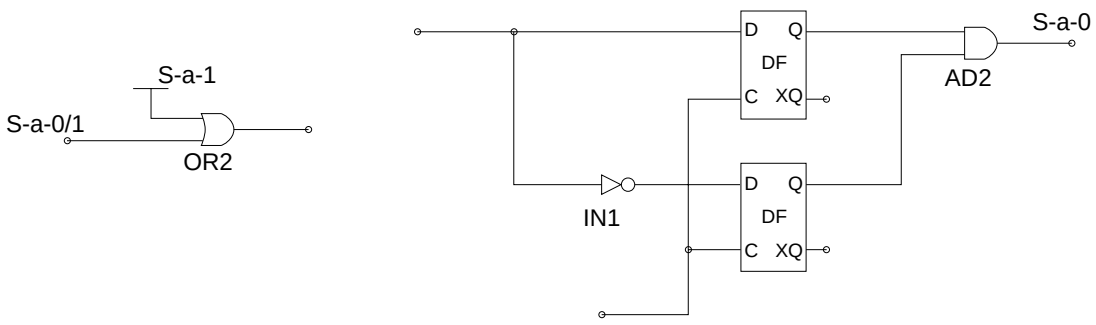


Figure 3-7 Example of Untestable fault

(4) Design Flow (1/2)

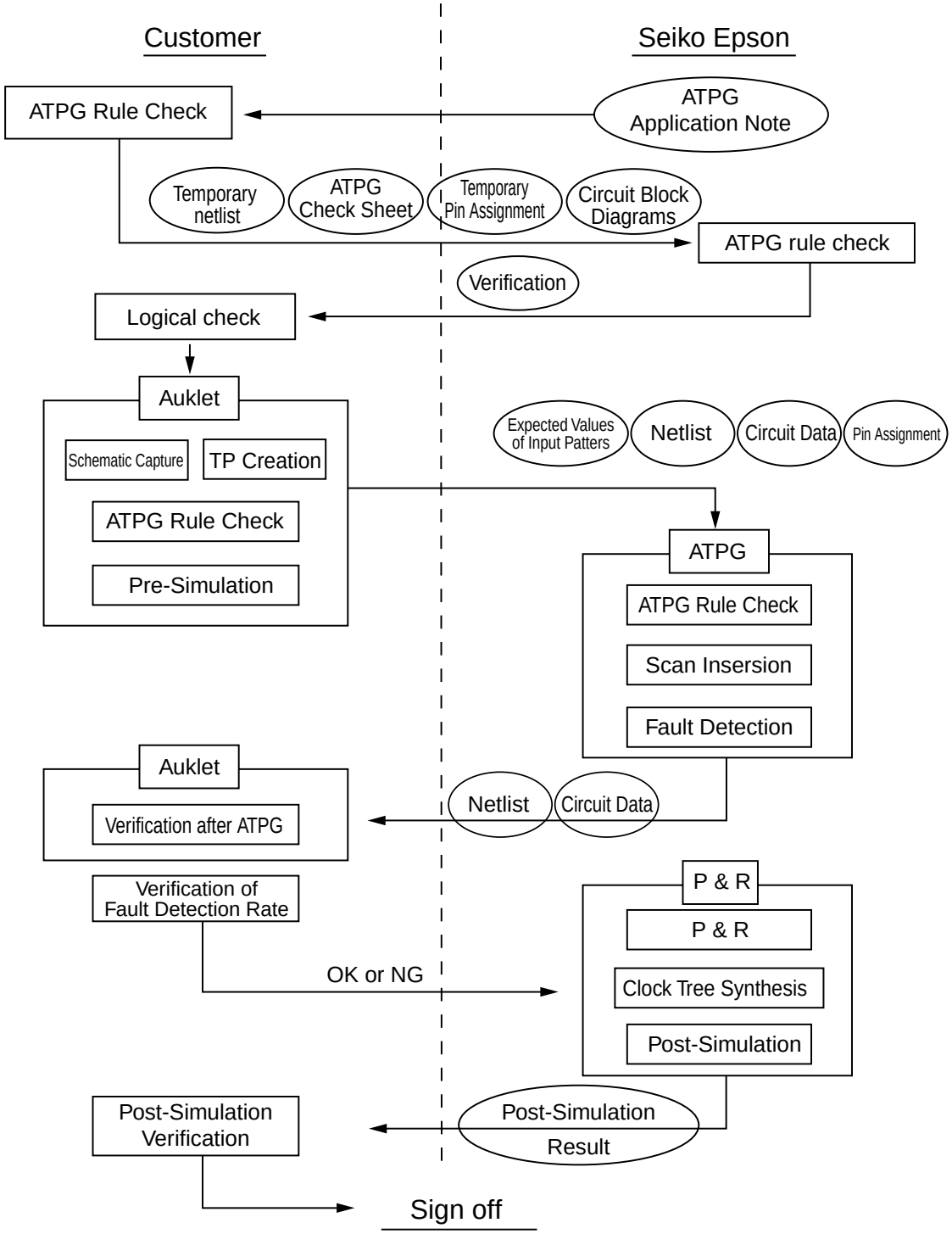


Figure 3-8 ATPG flow when designing by Auklet

(4) Design Flow (2/2)

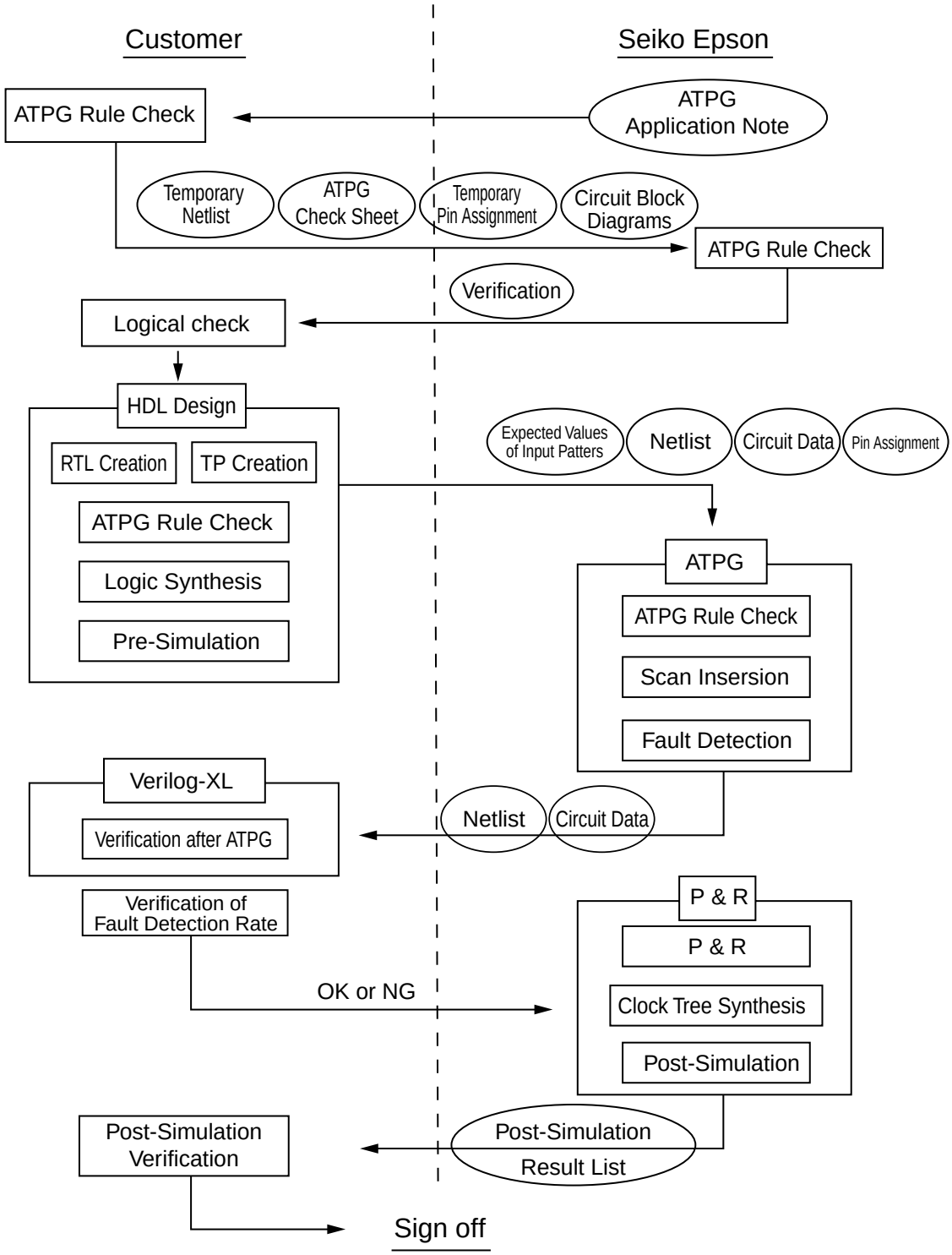


Figure 3-9 ATPG flow when designing by logic synthesis

(5) Test pattern composition created by ATPG

There are two test patters generated by ATPG, and their modes must be exchanged at the scanning enable input pin (SCANEN). The SCANEN pin needs to be used as the dedicated input pin because it is connected when the circuit is scanned.

- Scanning shift mode
  This mode is used when the memory element (scan FF) in the circuit composed for the shift register is inputted or outputted data.

- Scanning test mode
  This mode is used when the data inputted to the memory element on the scanning shift mode is used to operate on the circuit by the clock input.

(6) I / O Pins for ATPG

If two pins of SCANEN and ATPGEN are used, the ATPG can execute very efficiently. As a result, the delivery time is shortened and the fault detection rate goes up. The following explanation describes the pins needed to execute the ATPG.

- Scan Enable Input Terminal (SCANEN)
  This pin is used to exchange the scan shift mode with the scan test mode. It is also used when resetting or setting to FF (Flip Flop) and to fix the bi-directional I / O exchange signals while shifting each FF to scan. This pin must be ready for the dedicated pin because it is definitely needed to scan FF.

- Test input pin for ATPG (ATPGEN)
  This pin is used to make the circuit suitable for ATPG. For example, the asynchronous part of the circuit should be fixed by using the test input pin and if the clock line cannot be controlled externally, it can be controlled by using the pin for exchange. If the original circuit is adequate to the rule of ATPG, the pin is not needed for ATPG and the dedicated pin is used.

- Scan data input pin
  This scan data input pin is used to set the data to the shift register generated by scanning FF. In case of multi-scan FF, the number of scan data input pins is increased. These pins can be shared with others. However, they can not be used to share with the control pin to set or reset to the scan data or the clock and other pins to scan FF. If the scan data input pins are used to share with the bi-directional pins, they should be designed to be always used for input by utilizing the ATPGEN pin.

- Scan data output pin
  This scan data output pin is used to read the data from the shift register generated by scanning FF. In case of multi-scan FF, the number of scan data output pins is increased. These pins can be shared with other pins. If the scan data output pins are used to share with bi-directional pins, they should be designed to be always used for output by considering utilizing the ATPGEN pin.

- Scan clock input pin
  This pin is the clock input pin at the test pattern generated by ATPG. This pin usually utilizes the system clock in normal operation.

(7) Logic circuit design rule for ATPG (DFT)

To operate ATPG, the logic circuits should be scanned. According to the following rules, the original circuits that are observed to check very well should be designed. The following contents show a concrete example, so please contact EPSON Sales division if logic circuit design has difficulty handling the ATPG design.

- Target series: S1L50000, S1L30000,
  S1L9000F, S1X50000
- Only one pin is needed for the dedicated pin used as the scan enable pin (SCANEN).
- Please send the trial data to EPSON about a week before sending the formal data. EPSON will check the trial data of the logic circuit before getting the formal data. The process after obtaining the formal logic circuit data should be highly efficient and the fault detection rate of the logic circuit must go up.
- The clock, setting and resetting to the scan data in all of FF scanned must be controlled directly at the external pin.

  → If they cannot be controlled, use the ATPG test pin (ATPGEN) separated from the SCANEN pin and design the logic circuit so that it can be controlled.

  → When the logic circuit is configured to input multiple clocks from the external pin, the ATPGEN pin should be designed to be operated again in the active state by inputting only one clock for all FF scanned. However, if there is only one circuit, please contact EPSON sales division about the multiple circuits in this case.

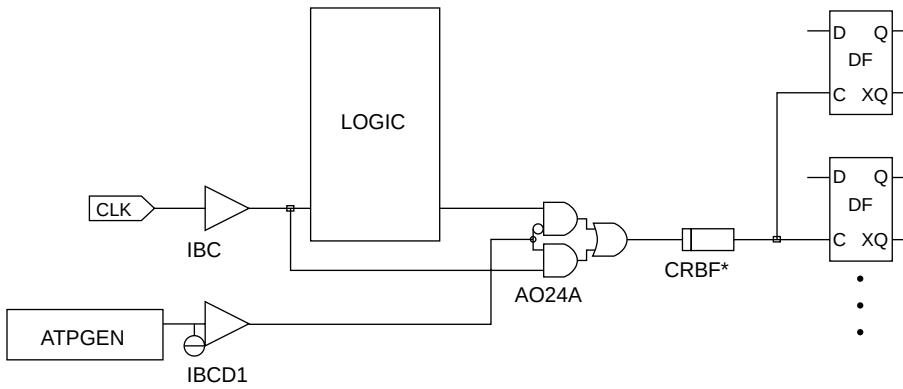


Figure 3-10 Example of Clock Line Process

- It is forbidden to design the circuit used to scan FF at the original circuit.
- Cope with the clock skew of clock nets by using Clock Tree Synthesis.
- Allocate I /O cells at the top of the hierarchical design.

- Do not use the internal 3-state bus.

  → The internal 3-state bus should be composed of the multiplexer and so on. However, if the circuit design needs an internal 3-state bus by any means, use the ATPGEN pin and the bus circuit must be designed never to cause a contention. When the circuit is designed by using the internal 3-state bus, the fault detection rate in the circuit does not always go up. Please contact EPSON sales division if a high fault detection rate is desired.

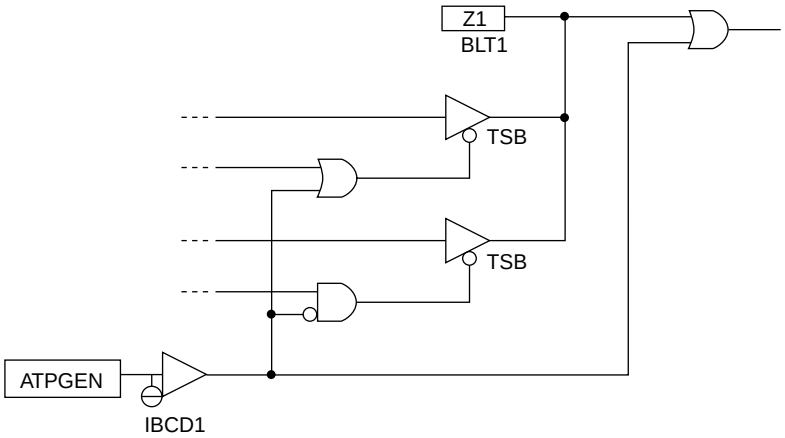


Figure 3-11 Process Example of Internal 3-state

- When using the macro cells, for example-RAM, ROM, Mega cell and so on, design the circuit inserted in the scanned FF before or after the I / O ports of the macro cells.

  → If circuit design is impossible, the faults can not often be detected before or after the macro cells.

- Keep away using MSI macro cells included in the Flip flop, for example-T175, A161 and so on.

  → The MSI cells can not scan. Do not use them if a high fault detection rate is desired.

- Do not use the asynchronous circuit and a circuit that causes racing at the RS latch, differentiating circuit and so on.

  → If these circuits are used, fix their output by using the ATPGEN pin. Furthermore, as the fault detection rate is not always up, do not use the circuit if a high fault detection rate is desired.

- Fix the latch cell by using the ATPGEN so that it is always through.

  → As the fault detection rate is not always up, do not use the circuit if a high fault detection rate is desired.

- Design the bi-directional pin to be state of input in the scan shifting mode.

  → If the bi-directional pin must be assigned to the scan data input and output pins, fix it to be state of each condition.

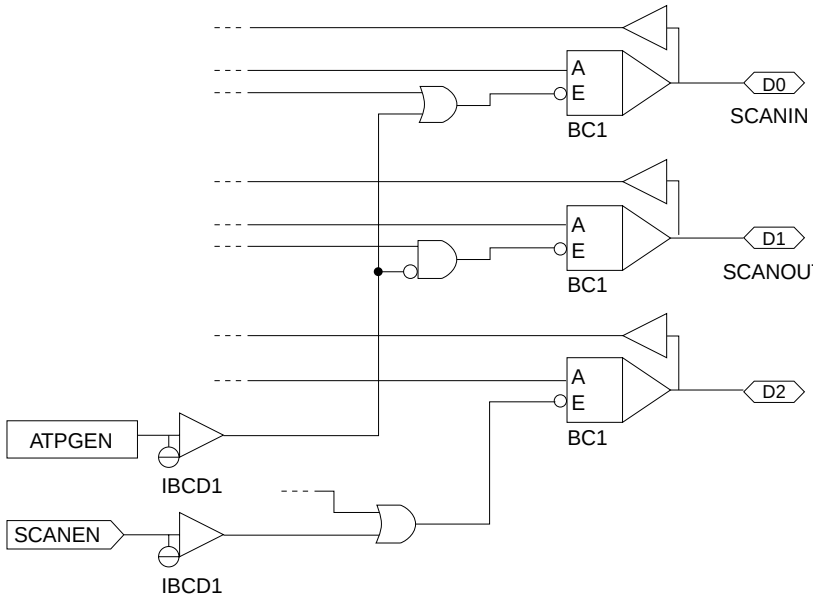


Figure 3-12 Process Example of bi-directional pins

- Fix the FF so that it is not scanned

  → As the T-FF, MSI macro cells include the FF, and the output from the FF not to be scanned causes a malfunction in the ATPG test patterns. Also, fault detection of the circuit often can not be executed, so if possible they should be fixed by the ATPGEN.

(8) Others

- The number of gates goes up about 15 to 20 % compared to the original circuit, but it depends on the number of scanned FFs.
- The working period for DFT and ATDG depends on the circuit configuration and the scale of gates. At least three working days are needed for DFT and ATPG at EPSON. (In an unusual case, about ten working days may be needed depending on the circuit configuration. Please refer to this book for the circuit configuration before designing it.)
- Please send the papers on “ATPG check sheet” and “External pin information” to EPSON before sending the logic circuit data. If there are problems with the logic circuit, EPSON may ask to change the design. Please define the external pins (ATPGEN, SCANEN and so on) added to scan FFs at the test patterns interfaced to EPSON. Please send the information required for Clock Tree Synthesis on page 20 at the same time, because when placing cells and routing interconnections, they are requested to cope with CTS (Clock Tree Synthesis).

(9) ATPG check sheet

Never delay sending this sheet a week before sending the logic circuit data. Please mark “Yes” or “No” at each item.

1.	Which the netlist format (gate level) interfaced to EPSON?	Verilog or EDIF
2.	Is the scanned FF used at the original circuit? (Note 1)	Yes or No
3.	Do you use macro cells, MSI cells and interval oscillator cells?	Yes or No
4.	If you answer “Yes” to the question above, write the cell name. :	
5.	Do you use the internal 3-state bus?	Yes or No
6.	Does your logic circuit have RS latch, differential circuit and asynchronous circuit?	Yes or No
7.	Do you use latch cells?	Yes or No
8.	Is there a bi-direction pin?	Yes or No
9.	Are there clocks that can not be directly controlled externally?	Yes or No
10.	Are there FF, reset and set pins of latch cells that can not be directly controlled externally?	Yes or No
11.	If the answers are “Yes” to question Nos.3 to 10, does the circuit design correspond to the DFT rule? (Note 2)	Yes or No
12.	Are I/O cells arranged on the top of the hierarchy?	Yes or No
13.	Do the clocknets cope with skew by CTS?	Yes or No

Note1: If you answered “Yes”, please design the logic circuit again, because the circuit can not scan.

Note2: If you answered “No”, please insert the DFT, because the circuit can not scan. Also, if you ask to insert the DFT to EPSON, please contact EPSON sales division, because circuit information in addition to that on this sheet is required.

(10) External Terminals

Enter the terminal names corresponding to the pin layout Table.

The specific terminals required vary by circuit configuration. (Be sure to enter all the terminal names you need.)

• Clock Input Terminal

Terminal name: _____ Operation edge: rise • fall

Terminal name: _____ Operation edge: rise • fall

Terminal name: _____ Operation edge: rise • fall

Terminal name: _____ Operation edge: rise • fall

Terminal name: _____ Operation edge: rise • fall

• Scan Enable Input Terminal (Note 3) ..... Yes • No

Terminal name: _____ Active level: High • Low

• ATPG Test Input Terminal ..... Yes • No

Terminal name: _____ Active level: High • Low

• Clear/Preset Input Terminals ..... Yes • No

Terminal name: _____ Active level: High • Low

• Other ATPG Mode Terminals ..... Yes • No

a) Terminal name: _____

Contents of control, operating level, etc.

: _____

b) Terminal name: _____

Contents of control, operating level, etc.

: _____

c) Terminal name: _____

Contents of control, operating level, etc.

: _____

d) Terminal name: _____

Contents of control, operating level, etc.

: _____

• Input terminals that cannot be assigned to the scan data input terminal (Note 4)

_____

_____

• Output terminals that cannot be assigned to the scan data output terminal (Note 4)

_____

_____

• Remarks

_____

_____

_____

_____

_____

_____

_____

_____

<Others>

• Number of gates before scan cell insertion (BC): _____

• Number of sets of D-FF and JK-FF : _____

• Date of trial data submission: (_____Month, _____day, _____year)

(Trial data: Check sheet, provisional net list, provisional pin layout Table, circuit block diagram)

• Required error detection rate: _____ %

• Along with this sheet, please submit circuit blocks and hierarchies (module and instance names) and information confirming the data path between the clock line and blocks.

(Note 3) If the insertion does not involve the original circuit, please specify the required contents.
(Note 4) If this is left unspecified, a selection will be assigned by SEIKO EPSON.

3.11 Restrictions and Constraints on VHDL/Verilog-HDL Netlist

The VHDL/Verilog-HDL net list to be interfaced to EPSON shall be a pure gate-level net list (not containing description of operation). The restrictions and constraints in developing EPSON ASIC using VHDL/Verilog HDL are as follows.

3.11.1 Common Restrictions and Constraints

(1) Names of External Terminal (I/O Terminal)

- Use only upper-case letters.
- Number of characters: 2 to 32
- Usable characters : Alphanumeric characters and "_." Use an alphabetical letter at the head.
- Examples of prohibited character strings :

  2 INPUT : A digit is at the head.
  \2INPUT : "\" is at the head.
  InputA : Lower-case letters are included.
  INPUTA : "" is at the head.
  TNA[3:0] : A bus is used for the name of the external terminal.
  INA[3] : A bus is used for the name of the external terminal.

(2) Names of Internal Terminal (including bus net names)

- Upper-and lower-case letters can be used in combination, except the following. Combinations of the same words expressed in upper-and lower-case letters, such as "_RESET_" and "_Reset_."
- Number of characters : 2 to 32
- Usable characters : Alphanumeric characters, "_," "_[ ]_" (Verilog bus blanket), and "_()_" (VHDL bus blanket) with an alphabetical letter at the head.

(3) Bus description is prohibited at the most significant place of the module.

Examples : DATA [0:3], DATA [3], and DATA [2] are prohibited.
DATA0, DATA1, and DATA2 are all allowed.

(4) You can use I/O cells of the same library series, but cannot combine those of different series.

(5) It is not possible to describe operations in behaviors or in the C language. Such descriptions existing in the net list are invalid.

(6) Precision of the time scale of the library of each series is 1 ps.

3.11.2 Restrictions and Constraints for Verilog Netlist

(7) Descriptions using the functions "assign" and "tran" are prohibited in the gate-level Verilog net list.

(8) Descriptions of connection with cell pin names are recommended in the Verilog net list.

Example : Connection with pin names: IN2 inst_1 (.A(inst_2),.X(inst_3)); Recommended
Connection with net names: IN2 inst_1(net1, net2):

(9) You cannot use the Verilog command "force" as a description of flip-flop operation.(Example: force logic .singal = 0;)

(10) The time scale description is added at the head of the gate-level net list generated by the Synopsys design compiler.
Set it at the value described in the EPSON Verilog library. See (6) for the time scale of each series.

Example : 'timescale 1ps/1ps

(11) EPSON prohibits combination of a bus single port name and a name that includes "__", such as the following, in the same module.

input A [0];

wire \A [0];

(12) The following letter strings are reserved for Verilog, which cannot be used as a user-defined name.

always, and, assign, begin, buf, bufif0, bufif1, case, design,default, defparam, disable, else, end, endcase, endfunction, endmodule, endtask, event, for, force, forever, fork, function, highz0, highz1, if, initial, inout, input, integer, join, large, medium, module, nand, negedge, nor, not, notif0, notif1, or, output, parameter, posedge, pull0, pull1, reg, release, repeat, scalared, small, specify, strong0, strong1, supply0, supply1, task, time, tri, tri0, tri1, trinand, trior, trireg, vectored, wait, wand, weak0, weak1, while, wire, wor, xor, xnor

3.11.3 Restrictions and Constraints on VHDL Netlist

(13) In addition to the constraints in (1), the following letter strings are also prohibited.

INPUTA_ : "_" is used at the end.

INPUT_ _A : "_" is used twice or more in succession.

read : Used in the system.

write : Used in the system.

(14) The following letter strings are reserved for VHDL, which cannot be used as a user-defined name.

abs, access, after, alias, all, and, architecture, array, assert, attribute, begin, block, body, buffer, bus, case, component, configuration, constant, disconnect, downto, else, elsif, end, entity, exit, file, for, function, generate, generic, guarded, if, in, inout, is, label, library, linkage, loop, map, mod, nand, new, next, nor, not, null, of, on, open, or, others, out, package, port, procedure, process, range, record, register, rem, report, return, select, severity, signal, subtype, then, to, transport, type, units, until, use, variable, wait, when, while, with, xor

(15) To use EPSON utilities and tools, it is necessary to change the VHDL format into the Verilog format. Therefore, the letter strings reserved for Verilog in (12) are also prohibited.

Chapter 4: Input/Out Cells Buffers and Their Use

4.1 Types of Input/Output Buffer in the S1L50000 Series

Various I/O buffers types of the S1L50000 Series are available according to the input inter-face level, schmitt trigger input or not, output drive capacity, use or no use of pull-up and pull-down resistors, and the pull-up and pull-down resistors. You can select the ones appropriate to your needs. For I/O buffers, keep in mind that these are two ways to use, which one is used for the single power system (2.5V), the other is used for the dual power system (3.3V/2.5V).

4.1.1 Selecting I/O Buffer

(1) Selecting the Input Buffer

a) Is the required interface level a CMOS level or a LVTTL level?

b) Is a schmitt trigger input necessary? (Are hysteresis characteristics necessary?)

c) Is it necessary to add pull-up/pull-down resistors?

(2) Selecting the Output Buffer

a) How much output current must be driven?(I_{OL} / I_{OH})

b) Are noise countermeasures necessary?

c) Is a bus hold circuit necessary?

(3) Selecting Bi-directional Buffer

Select the bi-directional buffer by examining both sets of criteria for selecting the input buffer and selecting the output buffer.

• I/O Interface Level

1) 3.3V system dual power supply

Input level
LVTTL Level, LVTTL Schmitt, PCI*

Output level
LVTTL Level, PCI*

2) 2.5V system dual power supply

Input level
CMOS Level, CMOS Schmit

Output level
CMOS Level

NOTE 1 : When a single power (2.5V) supply is used, LVTTL level input cannot be used.
* For PCI interface, contact to our sales office.

• **Output Drive Capability**
See the electrical characteristics (Tables 1-6 to 1-7).

• **Pull-up/Pull-down Resistance**
See the electrical characteristics (Tables 1-6 to 1-7).

The input buffer, output buffer, and bi-directional buffer configuration for single power supplies are expained in detail biginning with Section 4.2. Also, I/O buffer configuration for dual power supplies are explained in Chapter 11.

4.2 I/O Buffer Configurations with a Single Power Supply

When using a single power supply, the power supply voltage (V_{DD}) can be used only 2.5V.

I/O buffer configurations with a single power supply are explained below.

4.2.1 I/O Buffer Configurations with a Single Power Supply

4.2.1.1 Input Buffer Configurations with a Single Power Supply

The input buffer function is structured of I / O cells only.

Table 4-1 Input Buffer List (V_{DD}=2.5V)

Cell Name	Input Level	Function	Pull-up/Pull-down Resistance
IBC IBCP✻ IBCD✻	CMOS CMOS CMOS	Buffer Buffer Buffer	None Pull-up resistance (75kΩ, 150kΩ) Pull-down resistance (75kΩ, 150kΩ)
IBH IBHP✻ IBHD✻	CMOS Schmitt CMOS Schmitt CMOS Schmitt	Buffer Buffer Buffer	None Pull-up resistance (75kΩ, 150kΩ) Pull-down resistance (75kΩ, 150kΩ)

NOTE: When ✻ value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:75kΩ, 2:150kΩ respecively.

• IDC, IDH (Input Buffers)

These input buffers are used to input the single 5.0V power supply or single 3.3V power supply and the functions of them as a simple level shifter in place of the protective diode on the side of V_{DD}.

Table 4-2 Input Level Shifter (V_{DD}=2.5V)

Cell Name	Input Level	Function	Pull-up/Pull-down Resistance
IDC IDCD✻	CMOS CMOS	Buffer Buffer	None Pull-down resistance (75kΩ, 150kΩ)
IDH IDHD✻	CMOS Schmitt CMOS Schmitt	Buffer Buffer	None Pull-down resistance (75kΩ, 150kΩ)

NOTE: When ✻ value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:75kΩ, 2:150kΩ respecively.

4.2.1.2 Output Buffer Configurations with a Single Power Supply

See Figure 4.1 for connectivity and reference Table 4-3, 4-4 below regarding the list of output buffers of S1L50000.

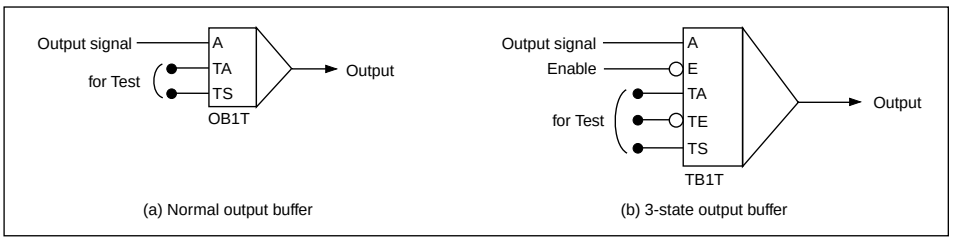


Figure 4-1 Examples of Output Buffer Symbols

Table 4-3 Output Buffers (V_{DD}=2.5V)

Function	I_{OL}* / I_{OH}**	Cell Name***
Normal output	0.1mA/-0.1mA 0.5mA/-0.5mA 1mA/-1mA 3mA/-3mA 6mA/-6mA	OBST OBMT OB1T OB2T OB3T
Normal output for high speed	6mA/-6mA	OB3AT
Normal output for low noise	6mA/-6mA	OB3BT
3-state output	0.1mA/-0.1mA 0.5mA/-0.5mA 1mA/-1mA 3mA/-3mA 6mA/-6mA	TBST TBMT TB1T TB2T TB3T
3-state output for high speed	6mA/-6mA	TB3AT
3-state output for low noise	6mA/-6mA	TB3BT
3-state output (Bus hold circuit)	0.5mA/-0.5mA 1mA/-1mA 3mA/-3mA 6mA/-6mA	TBMHT TB1HT TB2HT TB3HT
3-state output for high speed (Bus hold circuit)	6mA/-6mA	TB3AHT
3-state output for low noise (Bus hold circuit)	6mA/-6mA	TB3BHT

NOTES: * V_{OL} = 0.4V (V_{DD} = 2.5V)
** V_{OH} = V_{DD} - 0.4V (V_{DD} = 2.5V)
*** In addition to the configurations in Table 4-3, the output buffers may be configured which do not have test terminals. Customers desiring to use such structures should direct inquiries to EPSON.

• OD System (Output Buffers)

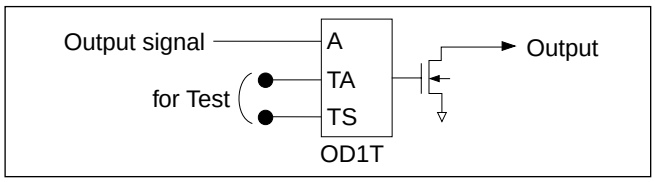


Figure 4-2 Example of N Channel Open Drain Buffer Symbol Configuration

Table 4-4 N channel Open Drain Output Buffers (V_{DD}=2.5V)

Function	I_{OL}* / I_{OH}	Cell Name**
Normal output	1mA 3mA 6mA	OD1T OD2T OD3T

NOTES: * V_{OL} = 0.4V (V_{DD} = 2.5V)
** In addition to the configurations in Table 4-4, N channel open drain output buffers may be configured which do not have test terminals. Customers desiring to use such structures should direct inquiries to EPSON.

4.2.1.3 Bi-directional Buffer Configurations with a Single Power Supply

The bi-directional buffers list are shown in the Table 4-5, 4-6.

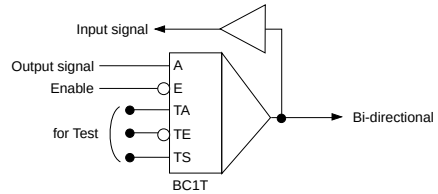


Figure 4-3 Examples of Bi-directional Buffer Symbols

Table 4-5 Bi-directional Buffers (V_{DD}=2.5V)

Input Level	Function	I_{OL}*/I_{OH}**	Cell Name***
CMOS	Bi-directional output	0.1mA/-0.1mA 0.5mA/-0.5mA 1mA/-1mA 3mA/-3mA 6mA/-6mA	BCST BCMT BC1T BC2T BC3T
	Bi-directional output for high speed	6mA/-6mA	BC3AT
	Bi-directional output for low noise	6mA/-6mA	BC3BT
CMOS Schmitt	Bi-directional output	0.1mA/-0.1mA 0.5mA/-0.5mA 1mA/-1mA 3mA/-3mA 6mA/-6mA	BHST BHMT BH1T BH2T BH3T
	Bi-directional output for high speed	6mA/-6mA	BH3AT
	Bi-directional output for low noise	6mA/-6mA	BH3BT
CMOS	Bi-directional output (Bus hold circuit)	0.5mA/-0.5mA 1mA/-1mA 3mA/-3mA 6mA/-6mA	BCMHT BC1HT BC2HT BC3HT
	Bi-directional output for high speed (Bus hold circuit)	6mA/-6mA	BC3AHT
	Bi-directional output for low noise (Bus hold circuit)	6mA/-6mA	BC3BHT
CMOS Schmitt	Bi-directional output (Bus hold circuit)	0.5mA/-0.5mA 1mA/-1mA 3mA/-3mA 6mA/-6mA	BHMHT BH1HT BH2HT BH3HT
	Bi-directional output for high speed (Bus hold circuit)	6mA/-6mA	BH3AHT
	Bi-directional output for low noise (Bus hold circuit)	6mA/-6mA	BH3BHT

NOTES: * V_{OL} = 0.4V (V_{DD} = 2.5V)

** V_{OH} = V_{DD} - 0.4V (V_{DD} = 2.5V)

*** In addition to the configurations in Table 4-5, bi-directional buffers may be configured with pull-up and pull-down resistances which do not have test terminals. Customers desiring to use such structures should direct inquiries to EPSON.

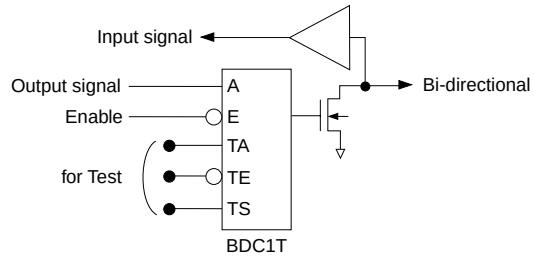


Figure 4-4 N Channel Open Drain Bi-directional Buffer Symbol

Table 4-6 N Channel Open Drain Bi-directional Buffers (V_{DD}=2.5V)

Input Level	Function	I_{OL}*	Cell Name***
CMOS	Bi-directional output	1mA 3mA 6mA	BDC1T BDC2T BDC3T
CMOS Schmitt	Bi-directional output	1mA 3mA 6mA	BDH1T BDH2T BDH3T

NOTES: * V_{OL} = 0.4V (V_{DD} = 2.5V)

** In addition to the configurations in Table 4-6, N channel open drain bi-directional buffers may be configured with pull-down resistances which do not have test terminals.
Customers desiring to use such structures should direct inquiries to EPSON.

4.3 Oscillation Circuit

4.3.1 Oscillation Circuit Configurations

Oscillation circuits should be configured, as shown in Figure 4-5. Both standard and gated oscillation circuit configurations are supported as shown.

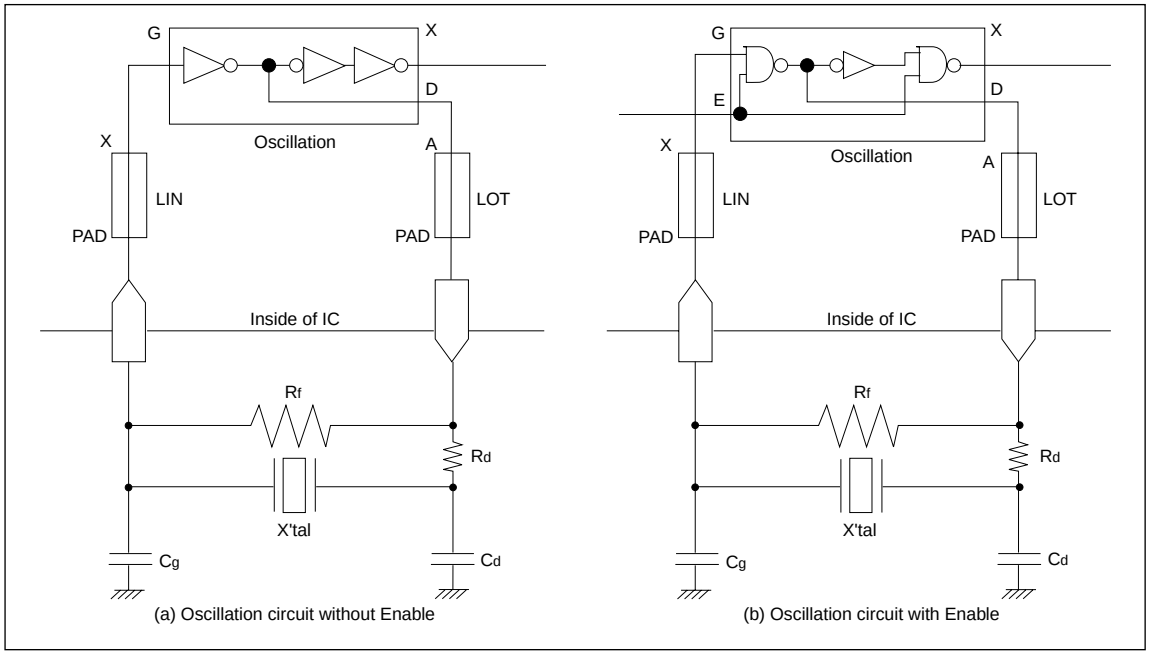


Figure 4-5 Method of Structuring the Oscillator

4.3.2 Oscillation Circuit Considerations

(1) Pin Layout

For QFP packages, the rules described below should be followed when placing schematics. For non-QFP packages, a separate examination is needed, so contact Seiko Epson or its distributor.

The inputs and outputs of the oscillation circuits should be positioned on adjacent pins, and should be located between power supply pins (V_{DD}, V_{SS}). Do not locate high drive output pins near the input/output pins of the oscillation circuit. Be especially careful to locate any outputs having the same phase or the opposite phase of the oscillating wave form as far as possible from the oscillation circuit input/output pins. Whenever possible, locate the input/output pins of the oscillation circuit near the center of the edge of the package.

(2) Oscillation Cell Selection Criteria

The frequency at which oscillation is possible is approximately several 10 KHz to mega hertz (MHz). For details, please direct inquiries to EPSON.

(3) Selecting the Values for the Resistances and Capacitors to be Attached

The characteristics of oscillation depends on the capacitive and resistive biasing elements (e.g. IC, X'tal, Rf, Rd, Cg, Cd, Board).

Because of this, the capacitive and resistive values must be adjusted, depending on the crystal which will be used on the actual board. Consequently, the optimal values should be chosen through spending adequate time evaluating available engineering samples.

(4) Assurance Levels

The characteristics of oscillation depends on the capacitive and resistive biasing elements (e.g. IC, X'tal, Rf, Rd, Cg, Cd, Board).

EPSON is unable to guarantee the function or characteristics of the oscillation. EPSON can warrantee only the oscillation cell. Because of this, it is necessary for the customer to spend adequate time evaluating the engineering samples in terms of their oscillation characteristics.

(5) Structuring Oscillation Circuits for Dual Power Supplies

The structure of oscillation circuits for dual power supplies is essentially no different than the structure for single power supplies. The oscillation circuit operates on the LV_{DD} system. Moreover, for input/output cells LIN and LOT, use LLIN and LLOT, which each have the prefix "L" to denote operation using LV_{DD}.

4.4 Gated I/O Cells

4.4.1 Overview of Gated I/O Cells

Gated I/O cells can use the input of pins to be floated or Hi-Z state, in other words, without using the pull up or down resistor that is impossible as usual. Also, if they are used, the power source of the high voltage side (HVDD) designed at the multiple power sources circuit can be cut off. There are two types; one is cut off at the High level of the control signal and the other at the Low level of the control signal, so it is selectable depending on the circuit design.

4.4.2 Feature of Gated I/O Cell

(1) There is no limitation on how many Gated cells are used and arranged, so they can be used to correspond to need to design a logic circuit.

(2) The power source of the high voltage side (HV_{DD}) designed at the multiple power source can be cut off.

(3) The input can be changed to Hi-Z state without using pull up or pull down resister.

(4) The input level corresponds with LVTTL (HV_{DD}/LV_{DD} = 3.3/2.5V), CMOS (HV_{DD}/LV_{DD} = 2.5/2.5V or V_{DD} = 2.5V) level.

(5) There are two types: one is off at the High level of the control signal and the other at the Low level of the control signal.

(6) The gated I/O cells are composed by the complete CMOS structure, so they can operate at low power.

4.4.3 Notes on Using Gated I/O Cell

(1) The EPSON standard input level of gated cells can not judge for its logic circuit composition. Therefore, if the user needs to know its input level, a test circuit should be composed (Refer to Fig.4-6).

(2) When the input of pins are set to Hi-Z state by using the Gated I/O cells, the cut off of power source must be operated by using the control of the Gated I/O cells before the input of cells set to Hi-Z state. If this operation is not executed and the input of cells is set to Hi-Z state, large current flows to the input cell in the same manner as normal cells and the LSI elements may be destroyed. Otherwise, when the input cells are set to Hi-Z state and a connecting operation is executed by using the control of the gated cell, a large current flows to the input cell in the same manner as for normal cells and the LSI elements may be destroyed. In this case, EPSON does not guarantee the logic levels in the internal device.

(3) When the power source of high voltage side (HV_{DD}) is cut off by using the Gated I/O cells, the same process as in (2) needs to be carried out. Also, when the process was not carried out, EPSON does not guarantee the logic levels in the internal device.

Table 4-7-1 Gated Input Cell List

Drain Type	Input Level		Without Resistor	Pull Down *1		Pull Up *1	
				75kΩ	150kΩ	75kΩ	150kΩ
Normal	CMOS	AND	IBA	IBAD1	IBAD2	IBAP1	IBAP2
		OR	IBO	IBOD1	IBOD2	IBOP1	IBOP2

*1: The value at V_{DD}=2.5V

Table 4-7-2 Gated Input Cell List

Drain Type	Input Level		Without Resistor	Pull Down *1		Pull Up *1	
				100kΩ	200kΩ	100kΩ	200kΩ
Normal	LVTTL*1 CMOS*2	AND	HIBA	HIBAD1	HIBAD2	HIBAP1	HIBAP2
		OR	HIBO	HIBOD1	HIBOD2	HIBOP1	HIBOP2

*1: The value at HV_{DD}=3.3V
*2: The value at HV_{DD}=2.5V

Table 4-7-3 Gated Bi-directional Cell List (AND Type)

Inpur Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA)*1	Without Resistor	Pull Down *1		Pull Up *1	
							75kΩ	150kΩ	75kΩ	150kΩ
CMOS	Normal	Exist	None-exist	NORMAL	– 1 / 1	BA1T	BA1D1T	BA1D2T	BA1P1T	BA1P2T
					– 3 / 3	BA2T	BA2D1T	BA2D2T	BA2P1T	BA2P2T
					– 6 / 6	BA3T	BA3D1T	BA3D2T	BA3P1T	BA3P2T
				HIGH SPEED	– 1 / 1	BA1CT	BA1CD1T	BA1CD2T	BA1CP1T	BA1CP2T
					– 3 / 3	BA2CT	BA2CD1T	BA2CD2T	BA2CP1T	BA2CP2T
					– 6 / 6	BA3AT	BA3AD1T	BA3AD2T	BA3AP1T	BA3AP2T
				LOW NOISE	– 6 / 6	BA3BT	BA3BD1T	BA3BD2T	BA3BP1T	BA3BP2T
		None-exist	None-exist	NORMAL	– 1 / 1	BA1	BA1D1	BA1D2	BA1P1	BA1P2
					– 3 / 3	BA2	BA2D1	BA2D2	BA2P1	BA2P2
					– 6 / 6	BA3	BA3D1	BA3D2	BA3P1	BA3P2
				HIGH SPEED	– 1 / 1	BA1C	BA1CD1	BA1CD2	BA1CP1	BA1CP2
					– 3 / 3	BA2C	BA2CD1	BA2CD2	BA2CP1	BA2CP2
					– 6 / 6	BA3A	BA3AD1	BA3AD2	BA3AP1	BA3AP2
				LOW NOISE	– 6 / 6	BA3B	BA3BD1	BA3BD2	BA3BP1	BA3BP2

*1: The value at V_{DD}=2.5V

Table 4-7-4 Gated Bi-directional Cell List (OR Type)

Inpur Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA)*1	Without Resistor	Pull Down *1		Pull Up *1	
							75kΩ	150kΩ	75kΩ	150kΩ
CMOS	Normal	Exist	None-exist	NORMAL	– 1 / 1	BO1T	BO1D1T	BO1D2T	BO1P1T	BO1P2T
					– 3 / 3	BO2T	BO2D1T	BO2D2T	BO2P1T	BO2P2T
					– 6 / 6	BO3T	BO3D1T	BO3D2T	BO3P1T	BO3P2T
				HIGH SPEED	– 1 / 1	BO1CT	BO1CD1T	BO1CD2T	BO1CP1T	BO1CP2T
					– 3 / 3	BO2CT	BO2CD1T	BO2CD2T	BO2CP1T	BO2CP2T
					– 6 / 6	BO3AT	BO3AD1T	BO3AD2T	BO3AP1T	BO3AP2T
				LOW NOISE	– 6 / 6	BO3BT	BO3BD1T	BO3BD2T	BO3BP1T	BO3BP2T
		None-exist	None-exist	NORMAL	– 1 / 1	BO1	BO1D1	BO1D2	BO1P1	BO1P2
					– 3 / 3	BO2	BO2D1	BO2D2	BO2P1	BO2P2
					– 6 / 6	BO3	BO3D1	BO3D2	BO3P1	BO3P2
				HIGH SPEED	– 1 / 1	BO1C	BO1CD1	BO1CD2	BO1CP1	BO1CP2
					– 3 / 3	BO2C	BO2CD1	BO2CD2	BO2CP1	BO2CP2
					– 6 / 6	BO3A	BO3AD1	BO3AD2	BO3AP1	BO3AP2
				LOW NOISE	– 6 / 6	BO3B	BO3BD1	BO3BD2	BO3BP1	BO3BP2

*1: The value at V_{DD}=2.5V

Table 4-7-5 Gated Bi-directional Cell List (AND Type)

Inpur Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA)*1	Without Resistor	Pull Down *1		Pull Up *1	
							100kΩ	200kΩ	100kΩ	200kΩ
LVTTL*1 CMOS*2	Normal	Exist	None-exist	NORMAL	– 2 / 2	HBA1T	HBA1D1T	HBA1D2T	HBA1P1T	HBA1P2T
					– 6 / 6	HBA2T	HBA2D1T	HBA2D2T	HBA2P1T	HBA2P2T
					–12 / 12	HBA3T	HBA3D1T	HBA3D2T	HBA3P1T	HBA3P2T
				HIGH SPEED	–12 / 12	HBA3AT	HBA3AD1T	HBA3AD2T	HBA3AP1T	HBA3AP2T
				LOW NOISE	–12 / 12	HBA3BT	HBA3BD1T	HBA3BD2T	HBA3BP1T	HBA3BP2T
		None-exist	None-exist	NORMAL	– 2 / 2	HBA1	HBA1D1	HBA1D2	HBA1P1	HBA1P2
					– 6 / 6	HBA2	HBA2D1	HBA2D2	HBA2P1	HBA2P2
					–12 / 12	HBA3	HBA3D1	HBA3D2	HBA3P1	HBA3P2
				HIGH SPEED	–12 / 12	HBA3A	HBA3AD1	HBA3AD2	HBA3AP1	HBA3AP2
				LOW NOISE	–12 / 12	HBA3B	HBA3BD1	HBA3BD2	HBA3BP1	HBA3BP2

*1: The value at HV_{DD}=3.3V
*2: The value at HV_{DD}=2.5V

Table 4-7-6 Gated Bi-directional Cell List (OR Type)

Inpur Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA)*1	Without Resistor	Pull Down *1		Pull Up *1	
							100kΩ	200kΩ	100kΩ	200kΩ
LVTTL*1 CMOS*2	Normal	Exist	None-exist	NORMAL	– 2 / 2	HBO1T	HBO1D1T	HBO1D2T	HBO1P1T	HBO1P2T
					– 6 / 6	HBO2T	HBO2D1T	HBO2D2T	HBO2P1T	HBO2P2T
					–12 / 12	HBOT	HBO3D1T	HBO3D2T	HBO3P1T	HBO3P2T
				HIGH SPEED	–12 / 12	HBO3AT	HBO3AD1T	HBO3AD2T	HBO3AP1T	HBO3AP2T
				LOW NOISE	–12 / 12	HBO3BT	HBO3BD1T	HBO3BD2T	HBO3BP1T	HBO3BP2T
		None-exist	None-exist	NORMAL	– 2 / 2	HBO1	HBO1D1	HBO1D2	HBO1P1	HBO1P2
					– 6 / 6	HBO2	HBO2D1	HBO2D2	HBO2P1	HBO2P2
					–12 / 12	HBO3	HBO3D1	HBO3D2	HBO3P1	HBO3P2
				HIGH SPEED	–12 / 12	HBO3A	HBO3AD1	HBO3AD2	HBO3AP1	HBO3AP2
				LOW NOISE	–12 / 12	HBO3B	HBO3BD1	HBO3BD2	HBO3BP1	HBO3BP2

*1: The value at HV_{DD}=3.3V
*2: The value at HV_{DD}=2.5V

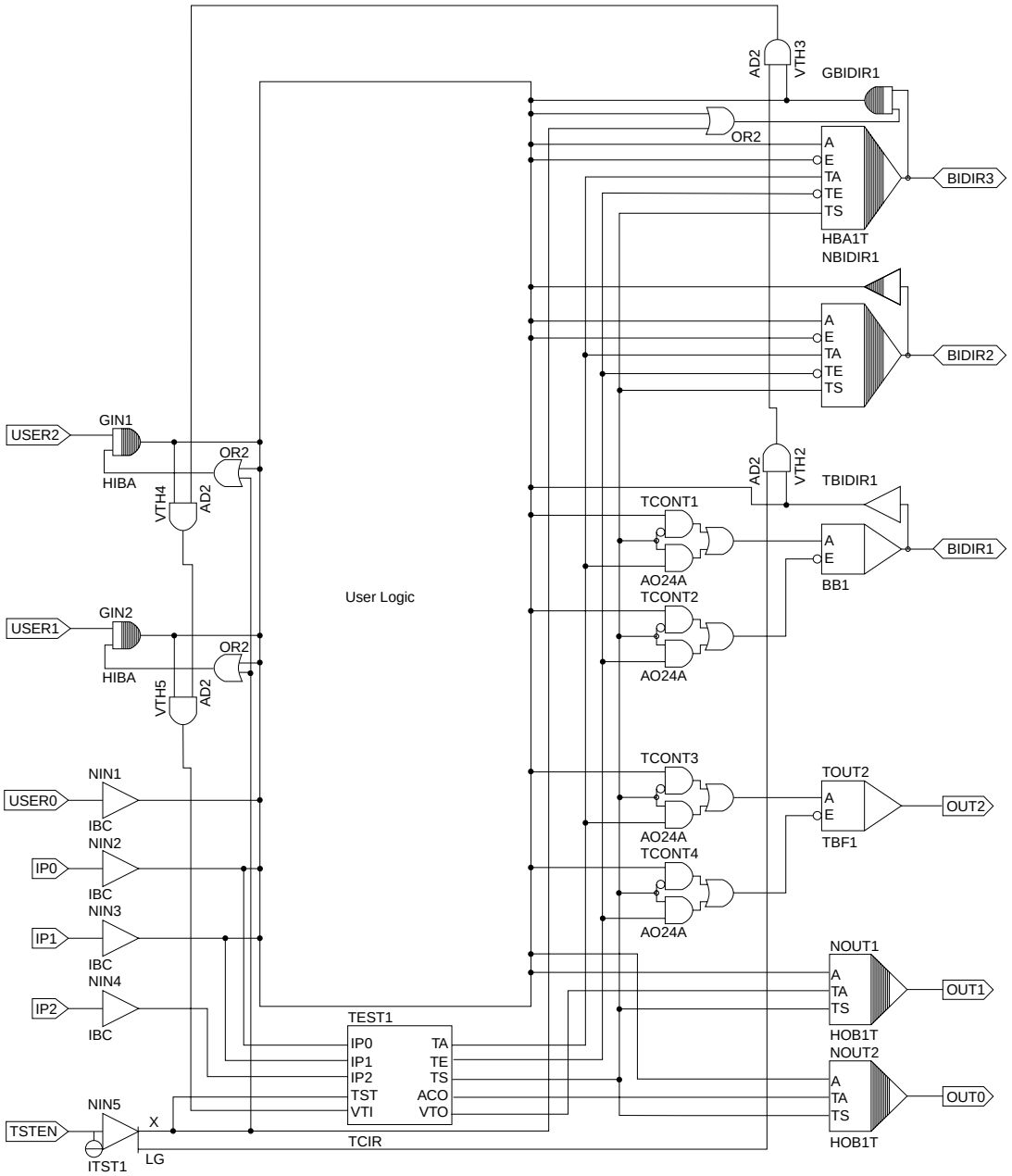


Figure 4-6 Example of Test Circuits for 3 State Type Fail-Safe and Gated Cells

Chapter 5: RAM

The S1L50000 Series supports 1 port RAM and 2 port RAM.

5.1 Features

(1) 1-Port RAM

- Asynchronous
- Static operation
- 1 read/write address port, 1 input data port, 1 output data port
- RAM configurations supported: Word Depth = 8 to 256 (incremental by 4 words)
  Bit Width = 1 to 32 (incremental by 1 bit)
- Maximum size: 8 K bits/module (256 words × 32 bits)

(2) 2-Port RAM

- Asynchronous
- Static operation
- 1 read address port, 1 write address port, 1 input data port, 1 output data port
- RAM configurations supported: Word Depth = 8 to 256 (incremental by 4 words)
  Bit Width = 1 to 32 (incremental by 1 bit)
- Maximum size: 8 K bits/module (256 words × 32 bits)

5.2 RAM Configuration and Simulation Model Selection

RAM delay parameters change depending on the word/bit structure. Six simulation models (three 1-port RAM models and three 2-port RAM models) have been prepared using performance characteristics indicative to the RAM word/bit configuration.

The 1-port RAM and 2-port RAM word/bit structure simulation models are shown in Table 5-1 and 5-2 respectively.

For RAM with word/bit structures exceeding the limitations in the tables below, use combinations of multiple RAMs.

Table 5-1 Simulation Model Selection Chart (1-Port RAM Word/Bit Structure)

Word depth / Bit width	8 to 32	36 to 64	68 to 96	100 to 128	132 to 160	164 to 192	196 to 224	228 to 256
1 to 16	RAM1P1	RAM1P3	RAM1P5	RAM1P7	RAM1P9	RAM1P11	RAM1P13	RAM1P15
17 to 32	RAM1P2	RAM1P4	RAM1P6	RAM1P8	RAM1P10	RAM1P12	RAM1P14	RAM1P16

Table 5-2 Simulation Model Selection Chart (2-Port RAM Word/Bit Structure)

Word depth / Bit width	8 to 32	36 to 64	68 to 96	100 to 128	132 to 160	164 to 192	196 to 224	228 to 256
1 to 16	RAM2P1	RAM2P3	RAM2P5	RAM2P7	RAM2P9	RAM2P11	RAM2P13	RAM2P15
17 to 32	RAM2P2	RAM2P4	RAM2P6	RAM2P8	RAM2P10	RAM2P12	RAM2P14	RAM2P16

5.3 RAM Size

The X-direction size, Y-direction size, and number of BCs used in the RAM are calculated using the formulas below. The formulas below include the interconnect region contained in the RAM. Use these formulas when investigating master selection when RAM is included (see Section 2.5).

(1) 1-Port RAM

Size in the X direction: RX = Word + Bit/2 + 13 (Round up to the nearest whole number)

Size in the Y direction: RY = 2 × Bit + 10

Number of BCs: $BC_{RAM} = RX \times RY$

Table 5-3 An Example of the Structure of 1-Port RAM

Word depth \ Bit width	4	8	16	32
32	846 (47 × 18)	1274 (49 × 26)	2226 (53 × 42)	4514 (61 × 74)
64	1422 (79 × 18)	2106 (81 × 26)	3570 (85 × 42)	6882 (93 × 74)
128	2574 (143 × 18)	3770 (145 × 26)	6258 (149 × 42)	11618 (157 × 74)
256	4878 (271 × 18)	7098 (273 × 26)	11634 (277 × 42)	21090(285 × 74)

NOTE: The numbers within this chart indicate BC_{RAM} (RX × RY) which includes interconnect area.

(2) 2-Port RAM

Size in the X direction: RX = Word + Bit/2 + 13 (Round up to the nearest whole number)

Size in the Y direction: RY = 2 × Bit + 14

Number of BCs: $BC_{RAM} = RX \times RY$

Table 5-4 An Example of the Structure of 2-Port RAM

Word depth \ Bit width	4	8	16	32
32	1034 (47 × 22)	1470 (49 × 30)	2438 (53 × 46)	4758(61 × 78)
64	1738 (79 × 22)	2430(81 × 30)	3910 (85 × 46)	7254 (93 × 78)
128	3146 (143 × 22)	4350 (145 × 30)	6854 (149 × 46)	12246(157 × 78)
256	5962 (271 × 22)	8190 (273 × 30)	12742(277 × 46)	22230(285 × 78)

NOTE: The numbers within this chart indicate BC_{RAM} (RX × RY), which includes interconnect area.

5.4 Investigating RAM Placement on Master Slice

When investigating RAM placement on a master slice, please insure that sufficient area is available in both the X direction (column) and the Y direction (row). When loading RAM onto a chip, it is necessary to insure that the capacity of the master exceeds the required RAM area in both the X and Y directions.

When multiple RAMs are used, RAM blocks are placed adjacent to each other either horizontally or vertically; the decision regarding master slice selection is based simply on RX and RY. Please see Table 1.1 of Chapter 1 regarding the number of columns (X-direction) and number of rows (Y-direction).

For example, if four 256 word × 8 bit 1-port RAMs are required.

As shown in Figure 5-1, the total RAM layout area would be:

X direction: 273 BCs
Y direction: 104 BCs (26 × 4)

Because of this,

S1L50282 is (X, Y) = (319, 90) is impossible due to area constraints, however,
S1L50752 is (X, Y) = (519, 146) is possible.

See Section 2.5 pertaining to estimating the number of gates, BC_{AWR}, which can be used for random logic.

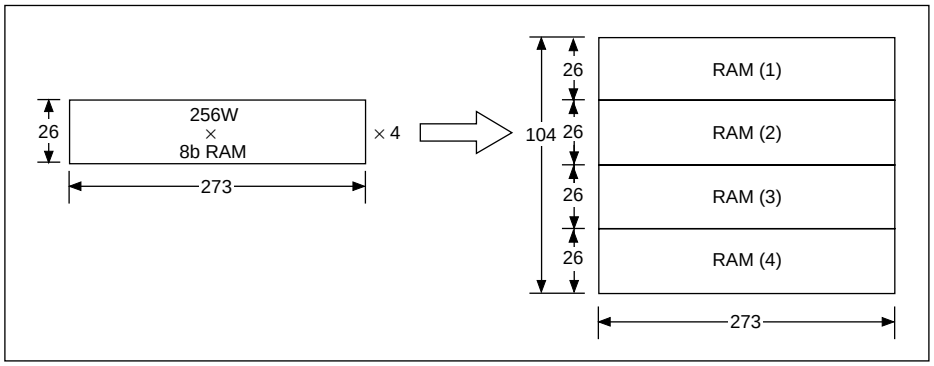


Figure 5-1 Example of RAM Layout

5.5 Explanation of Functions

(1) 1-Port RAM

Table 5-5 1-Port RAM Signals

Signal Name	I/O	Function	Notes
CS	IN	Chip select signal, H: RAM active	FI = 1LU
RW	IN	Read/write signal, H: Read, L: Write	FI = 1LU
A0, A1 ... A(m-1)	IN	Read/write address port, A0: LSB	FI = 1LU
D0, D1 ... D(n-1)	IN	Data input port, D0: LSB	FI = 1LU
Y0, Y1 ... Y(n-1)	OUT	Data output port, Y0: LSB	FO = 55LU corresponds to K:IN2

Table 5-6 1-Port RAM Truth Table

CS	RW	A0, A1 ... A(m-1)	Y0, Y1 ... Y(n-1)	Mode
0	X	X	Unknown	Wait
1	0	Stable	Unknown	Write
1	1	Stable	Read Data	Read

X: "High" or "Low"

• Data Read

The data is read by holding CS at "High" and RW at "High" and setting the address.

• Data Write

The data can be written in either of the following two ways:

(1) Holding CS at "High", setting the address, and sending a negative pulse to RW.

(2) Holding RW at "Low", setting the address, and sending a positive pulse to CS.

When either method is used, the data is latched to the RAM at the trailing edge of the pulse.

• The Wait State

When CS is "Low", the 1 port RAM enters a wait state and only maintains the data. The current consumed by the RAM is merely the leakage current, and is almost zero.

(2) 2-Port RAM

Table 5-7 2-Port RAM Signals

Signal Name	I/O	Function	Notes
CS	IN	Chip select signal, H: RAM active	FI = 1LU
RD	IN	Read signal, H: Read enable	FI = 1LU
WR	IN	Write signal, H: Write enable	FI = 1LU
RA0, . . . RA(m-1)	IN	Read address port, RA0: LSB	FI = 1LU
WA0, . . . WA(m-1)	IN	Write address port, WA0: LSB	FI = 1LU
D0, D1, . . . D(n-1)	IN	Data input port, D0: LSB	FI = 1LU
Y0, Y1, . . . Y(n-1)	OUT	Data output port, Y0: LSB	F0 = 55LU corresponds to K:IN2

Table 5-8 2-Port RAM Truth Table

CS	RD	WR	RA0, ... RA(n-1)	WA0, ...WA(m-1)	Y0, ... Y(n-1)	Mode
0	X	X	X	X	Unknown	Wait
1	0	0	X	X	Unknown	Wait
1	0	1	X	Stable	Unknown	Write
1	1	0	Stable	X	Read Data	Read
1	1	1	Stable	Stable	Read Data	Read & Write

X: “High” or “Low”

Data Read

The data is read by holding CS at “High” and RD at “High” and setting the read address.

Data Write

he data can be written in either of the following two ways:

(1) Holding CS at “High”, setting the write address, and sending a positive pulse to WR.
(2) Holding WR at “High”, setting the write address, and sending a positive pulse to CS.

• Data Read/Write

When reading is done at the same time as writing, it is possible by performing the respective methods simultaneously. However, these two operations cannot be performed simultaneously on the same address. The read cycle access time applies to data for which the writing has already been completed.

• The Wait State

The 2 port RAM enters a wait state in either of the situations below, and does nothing but maintain its data. The current consumed by the RAM is merely the leakage current, and is almost 0.

(1) CS is “Low”.
(2) CS is “High”, RD is “Low”, and WR is “Low”.

5.6 Delay Parameters

(1) 2.5V Specifications (V_{DD} = 2.25 to 2.75V ; Ta = -40 to 85°C)

Table 5-9 1-Port RAM Read Cycle (1/4)

Parameter	Signal	RAM1P1		RAM1P 2		RAM1P 3		RAM1P 4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	9.69	—	10.49	—	11.66	—	12.46	—	ns
Address access time	t_{ACC}	—	9.69	—	10.49	—	11.66	—	12.46	
CS access time	t_{ACS}	—	9.69	—	10.49	—	11.66	—	12.46	
RW access time	t_{ARW}	—	9.69	—	10.49	—	11.66	—	12.46	
CS active time	t_{RCS}	9.69	—	10.49	—	11.66	—	12.46	—	
Output hold time after address change	t_{OH}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after CS disable	t_{OHCS}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after RW disable	t_{OHRW}	0.16	—	0.23	—	0.16	—	0.23	—	

Table 5-9 1-Port RAM Read Cycle (2/4)

Parameter	Signal	RAM1P 5		RAM1P 6		RAM1P7		RAM1P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	13.63	—	14.42	—	15.59	—	16.39	—	ns
Address access time	t_{ACC}	—	13.63	—	14.42	—	15.59	—	16.39	
CS access time	t_{ACS}	—	13.63	—	14.42	—	15.59	—	16.39	
R/W access time	t_{ARW}	—	13.63	—	14.42	—	15.59	—	16.39	
CS active time	t_{RCS}	13.63	—	14.42	—	15.59	—	16.39	—	
Output hold time after address change	t_{OH}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after CS disable	t_{OHCS}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after R/W disable	t_{OHRW}	0.16	—	0.23	—	0.16	—	0.23	—	

Table 5-9 1-Port RAM Read Cycle (3/4)

Parameter	Signal	RAM1P 9		RAM1P10		RAM1P11		RAM1P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	17.56	—	18.36	—	19.53	—	20.33	—	ns
Address access time	t_{ACC}	—	17.56	—	18.36	—	19.53	—	20.33	
CS access time	t_{ACS}	—	17.56	—	18.36	—	19.53	—	20.33	
R/W access time	t_{ARW}	—	17.56	—	18.36	—	19.53	—	20.33	
CS active time	t_{RCS}	17.56	—	18.36	—	19.53	—	20.33	—	
Output hold time after address change	t_{OH}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after CS disable	t_{OHCS}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after R/W disable	t_{OHRW}	0.16	—	0.23	—	0.16	—	0.23	—	

Table 5-9 1-Port RAM Read Cycle (4/4)

Parameter	Signal	RAM1P13		RAM1P14		RAM1P15		RAM1P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	21.50	—	22.30	—	23.47	—	24.26	—	ns
Address access time	t_{ACC}	—	21.50	—	22.30	—	23.47		24.26	
CS access time	t_{ACS}	—	21.50	—	22.30	—	23.47		24.26	
R/W access time	t_{ARW}	—	21.50	—	22.30	—	23.47		24.26	
CS active time	t_{RCS}	21.50	—	22.30	—	23.47	—	24.26	—	
Output hold time after address change	t_{OH}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after CS disable	t_{OHCS}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after R/W disable	t_{OHRW}	0.16	—	0.23	—	0.16	—	0.23	—	

Table 5-10 1-Port RAM Write Cycle (1/4)

Parameter	Signal	RAM1P1		RAM1P 2		RAM1P 3		RAM1P 4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	7.33	—	9.71	—	7.47	—	9.85	—	ns
Write pulse width	t_{WP}	4.16	—	6.54	—	4.22	—	6.60	—	
CS active time	t_{WCS}	4.16	—	6.54	—	4.22	—	6.60	—	
Address setup time	t_{AS}	1.01	—	1.01	—	1.09	—	1.09	—	
Address hold time	t_{AH}	2.16	—	2.16	—	2.16	—	2.16	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	4.05	—	5.69	—	4.12	—	5.76	—	

Table 5-10 1-Port RAM Write Cycle (2/4)

Parameter	Signal	RAM1P 5		RAM1P 6		RAM1P 7		RAM1P 8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	7.62	—	10.00	—	7.78	—	10.16	—	ns
Write pulse width	t_{WP}	4.30	—	6.68	—	4.38	—	6.76	—	
CS active time	t_{WCS}	4.30	—	6.68	—	4.38	—	6.76	—	
Address setup time	t_{AS}	1.16	—	1.16	—	1.24	—	1.24	—	
Address hold time	t_{AH}	2.16	—	2.16	—	2.16	—	2.16	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	4.19	—	5.84	—	4.26	—	5.91	—	

Table 5-10 1-Port RAM Write Cycle (3/4)

Parameter	Signal	RAM1P9		RAM1P10		RAM1P11		RAM1P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	7.96	—	10.34	—	8.14	—	10.52	—	ns
Write pulse width	t_{WP}	4.48	—	6.86	—	4.59	—	6.97	—	
CS active time	t_{WCS}	4.48	—	6.86	—	4.59	—	6.97	—	
Address setup time	t_{AS}	1.32	—	1.32	—	1.39	—	1.39	—	
Address hold time	t_{AH}	2.16	—	2.16	—	2.16	—	2.16	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	4.33	—	5.98	—	4.40	—	6.05	—	

Table 5-10 1-Port RAM Write Cycle (4/4)

Parameter	Signal	RAM1P13		RAM1P14		RAM1P15		RAM1P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	8.33	—	10.71	—	8.54	—	10.92	—	ns
Write pulse width	t_{WP}	4.70	—	7.08	—	4.83	—	7.21	—	
CS active time	t_{WCS}	4.70	—	7.08	—	4.83	—	7.21	—	
Address setup time	t_{AS}	1.47	—	1.47	—	1.55	—	1.55	—	
Address hold time	t_{AH}	2.16	—	2.16	—	2.16	—	2.16	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	4.48	—	6.12	—	4.55	—	6.19	—	

Table 5-11 2-Port RAM Read Cycle (1/4)

Parameter	Signal	RAM 2P1		RAM 2P2		RAM 2P3		RAM 2P4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	9.69	—	10.49	—	11.66	—	12.46	—	ns
Address access time	t_{ACC}	—	9.69	—	10.49	—	11.06	—	12.46	
CS access time	t_{ACS}	—	9.69	—	10.49	—	11.06	—	12.46	
RW access time	t_{ARW}	—	9.69	—	10.49	—	11.06	—	12.46	
CS active time	t_{RCS}	9.69	—	10.49	—	11.66	—	12.46	—	
Output hold time after address change	t_{OH}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after CS disable	t_{OHCS}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after RW disable	t_{OHRW}	0.16	—	0.23	—	0.16	—	0.23	—	

Table 5-11 2-Port RAM Read Cycle (2/4)

Parameter	Signal	RAM 2P5		RAM 2P6		RAM 2P7		RAM 2P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	13.63	—	14.42	—	15.59	—	16.39	—	ns
Address access time	t_{ACC}	—	13.63	—	14.42	—	15.59	—	16.39	
CS access time	t_{ACS}	—	13.63	—	14.42	—	15.59	—	16.39	
R/W access time	t_{ARW}	—	13.63	—	14.42	—	15.59	—	16.39	
CS active time	t_{RCS}	13.63	—	14.42	—	15.59	—	16.39	—	
Output hold time after address change	t_{OH}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after CS disable	t_{OHCS}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after R/W disable	t_{OHRW}	0.16	—	0.23	—	0.16	—	0.23	—	

Table 5-11 2-Port RAM Read Cycle (3/4)

Parameter	Signal	RAM 2P9		RAM 2P10		RAM 2P11		RAM 2P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	17.56	—	18.36	—	19.53	—	20.33	—	ns
Address access time	t_{ACC}	—	17.56	—	18.36	—	19.53	—	20.33	
CS access time	t_{ACS}	—	17.56	—	18.36	—	19.53	—	20.33	
R/W access time	t_{ARW}	—	17.56	—	18.36	—	19.53	—	20.33	
CS active time	t_{RCS}	17.56	—	18.36	—	19.53	—	20.33	—	
Output hold time after address change	t_{OH}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after CS disable	t_{OHCS}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after R/W disable	t_{OHRW}	0.16	—	0.23	—	0.16	—	0.23	—	

Table 5-11 2-Port RAM Read Cycle (4/4)

Parameter	Signal	RAM 2P13		RAM 2P14		RAM 2P15		RAM 2P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	21.50	—	22.30	—	23.47	—	24.26	—	ns
Address access time	t_{ACC}	—	21.50	—	22.30	—	23.47	—	24.26	
CS access time	t_{ACS}	—	21.50	—	22.30	—	23.47	—	24.26	
R/W access time	t_{ARW}	—	21.50	—	22.30	—	23.47	—	24.26	
CS active time	t_{RCS}	21.50	—	22.30	—	23.47	—	24.26	—	
Output hold time after address change	t_{OH}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after CS disable	t_{OHCS}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after R/W disable	t_{OHRW}	0.16	—	0.23	—	0.16	—	0.23	—	

Table 5-12 2-Port RAM Write Cycle (1/4)

Parameter	Signal	RAM 2P1		RAM 2P2		RAM2P3		RAM2P4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	7.33	—	9.71	—	7.47	—	9.85	—	ns
Write pulse width	t_{WP}	4.16	—	6.54	—	4.22	—	6.60	—	
CS active time	t_{WCS}	4.16	—	6.54	—	4.22	—	6.60	—	
Address setup time	t_{AS}	1.01	—	1.01	—	1.09	—	1.09	—	
Address hold time	t_{AH}	2.16	—	2.16	—	2.16	—	2.16	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	4.05	—	5.69	—	4.12	—	5.76	—	

Table 5-12 2-Port RAM Write Cycle (2/4)

Parameter	Signal	RAM 2P5		RAM 2P6		RAM2P7		RAM2P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	7.62	—	10.00	—	7.78	—	10.16	—	ns
Write pulse width	t_{WP}	4.30	—	6.68	—	4.38	—	6.76	—	
CS active time	t_{WCS}	4.30	—	6.68	—	4.38	—	6.76	—	
Address setup time	t_{AS}	1.16	—	1.16	—	1.24	—	1.24	—	
Address hold time	t_{AH}	2.16	—	2.16	—	2.16	—	2.16	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	4.19	—	5.84	—	4.26	—	5.91	—	

Table 5-12 2-Port RAM Write Cycle (3/4)

Parameter	Signal	RAM 2P9		RAM 2P10		RAM2P11		RAM2P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	7.96	—	10.34	—	8.14	—	10.52	—	ns
Write pulse width	t_{WP}	4.48	—	6.86	—	4.59	—	6.97	—	
CS active time	t_{WCS}	4.48	—	6.86	—	4.59	—	6.97	—	
Address setup time	t_{AS}	1.32	—	1.32	—	1.39	—	1.39	—	
Address hold time	t_{AH}	2.16	—	2.16	—	2.16	—	2.16	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	4.33	—	5.98	—	4.40	—	6.05	—	

Table 5-12 2-Port RAM Write Cycle (4/4)

Parameter	Signal	RAM 2P13		RAM 2P14		RAM2P15		RAM2P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	8.33	—	10.71	—	8.54	—	10.92	—	ns
Write pulse width	t_{WP}	4.70	—	7.08	—	4.83	—	7.21	—	
CS active time	t_{WCS}	4.70	—	7.08	—	4.83	—	7.21	—	
Address setup time	t_{AS}	1.47	—	1.47	—	1.55	—	1.55	—	
Address hold time	t_{AH}	2.16	—	2.16	—	2.16	—	2.16	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	4.48	—	6.12	—	4.55	—	6.19	—	

(2) 2.5V Specification (V_{DD} = 2.25 to 2.75V; Ta = 0 to 70°C)

Propagation delay parameter of RAM for V_{DD} = 2.25 to 2.75V and Ta=0 to 70°C is calculated by multiplying the following coefficient for the parameters for V_{DD} = 2.25 to 2.75V and Ta=-40 to 85°C.

(1) 2.5V Specifications (V_{DD} = 2.25 to 2.75V ; Ta = -40 to 85ºC)

Table 5-9 1-Port RAM Read Cycle (1/4)

Parameter	Signal	RAM1P1		RAM1P 2		RAM1P 3		RAM1P 4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	9.69	—	10.49	—	11.66	—	12.46	—	ns
Address access time	t_{ACC}	—	9.69	—	10.49	—	11.66	—	12.46	
CS access time	t_{ACS}	—	9.69	—	10.49	—	11.66	—	12.46	
RW access time	t_{ARW}	—	9.69	—	10.49	—	11.66	—	12.46	
CS active time	t_{RCS}	9.69	—	10.49	—	11.66	—	12.46	—	
Output hold time after address change	t_{OH}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after CS disable	t_{OHCS}	0.16	—	0.23	—	0.16	—	0.23	—	
Output hold time after RW disable	t_{OHRW}	0.16	—	0.23	—	0.16	—	0.23	—	

Each value of "Min."or"Max." × **0.97**

Each value of "Min." × **1.04**

Table 5-10 1-Port RAM Write Cycle (1/4)

Parameter	Signal	RAM1P1		RAM1P 2		RAM1P 3		RAM1P 4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	7.33	—	9.71	—	7.47	—	9.85	—	ns
Write pulse width	t_{WP}	4.16	—	6.54	—	4.22	—	6.60	—	
CS active time	t_{WCS}	4.16	—	6.54	—	4.22	—	6.60	—	
Address setup time	t_{AS}	1.01	—	1.01	—	1.09	—	1.09	—	
Address hold time	t_{AH}	2.16	—	2.16	—	2.16	—	2.16	—	
Data setup time	t_{DS}	0.00	—	0.00	—	0.00	—	0.00	—	
Data hold time	t_{DH}	4.05	—	5.69	—	4.12	—	5.76	—	

Each values of "Min." × **0.97**

Figure 5-2 Example of RAM Delay Parameters Calculation for V_{DD} = 2.25 to 2.75V and Ta = 0 to 70°C

5.7 Timing Charts

(1) 1-Port RAM

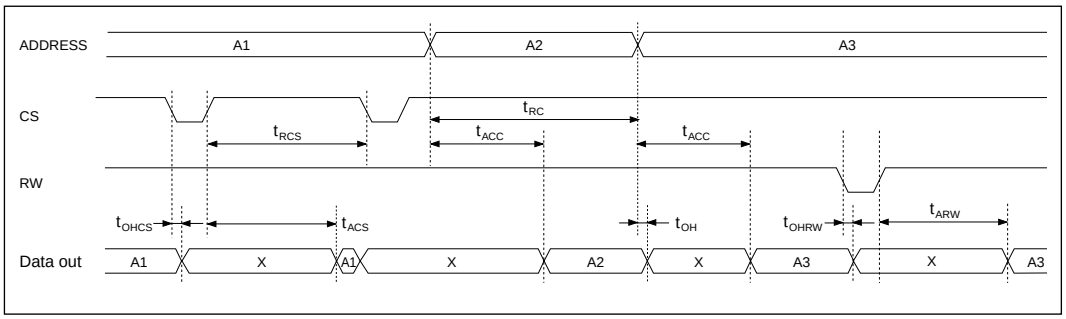


Figure 5-3 Read Cycle

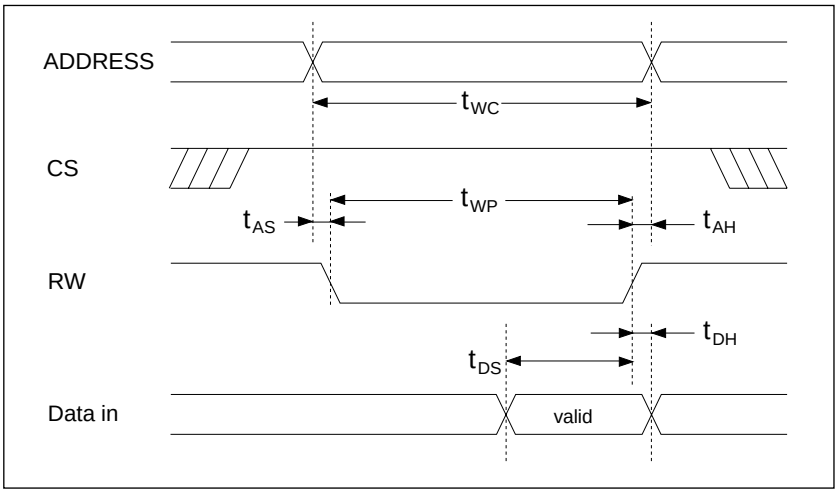


Figure 5-4 Write Cycle (R/W Control)

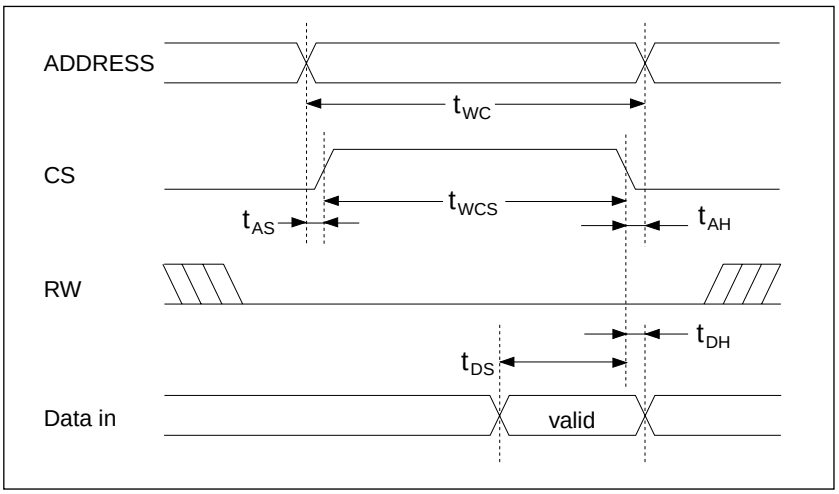


Figure 5-5 Write Cycle (CS Control)

(2) 2-Port RAM

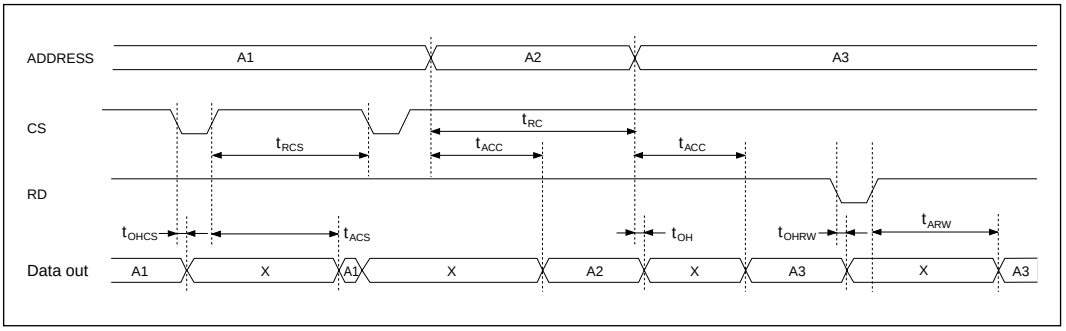


Figure 5-6 Read Cycle

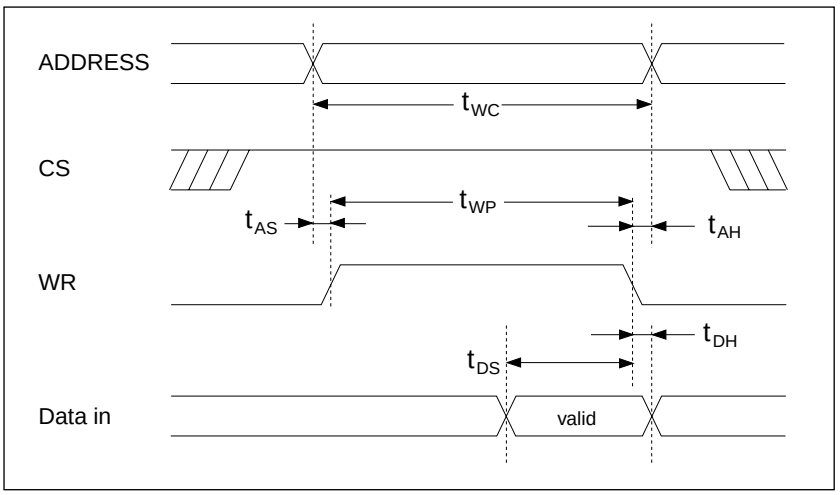


Figure 5-7 Write Cycle (Write Control)

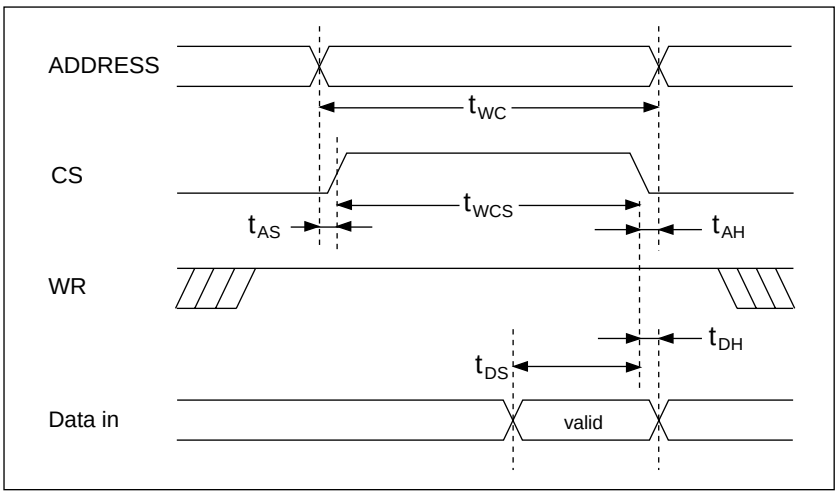


Figure 5-8 Write Cycle (CS Control)

5.8 RAM Test Method

When it comes to internal RAM, specialized tests are performed corresponding to the RAM, separate from the ramdom logic. Please structure test circuits which facilitate direct access to the internal RAM from external pins for this purpose. See Section 6.3 of Chapter 6 regarding the method of structuring the RAM test circuits.

Also, although EPSON will generate an independent test pattern for the RAM, the customer should provide test patterns for the remaining random logic, in addition to a RAM test pattern template, as shown in Section 6.3.1.

5.9 Estimating RAM Current Consumption

The method for estimating the current consumption at V_{DD} (Typ.) = 2.5V is given below.

(1) 1-Port RAM

At standby (CS = 0):	0	[µA/Bit]	
During operation (CS = 1):	$\underline{0.050} \times f$	[µA/Bit]	f: MHz (average access cycles)

(2) 2-Port RAM

At standby (CS = 0):	0	[µA/Bit]	
During operation (CS = 1):	$\underline{0.050} \times f$	[µA/Bit]	f: MHz (average access cycles)

5.10 RAM Symbols and How They Are Used

When the 1 port RAM uses a 16 word × 8 bit structure, the use of symbols is as given in Figure 5.8. This structure requires 4 address pins and 8 data input pins. As is shown in Figure 5.8, any unused address pins or data input pins should be tied to "Low" beginning with the most significant bits.

Furthermore, if multiple RAMs are used, the circuit shoud be configured by using the same numbers of symbols as RAMs.

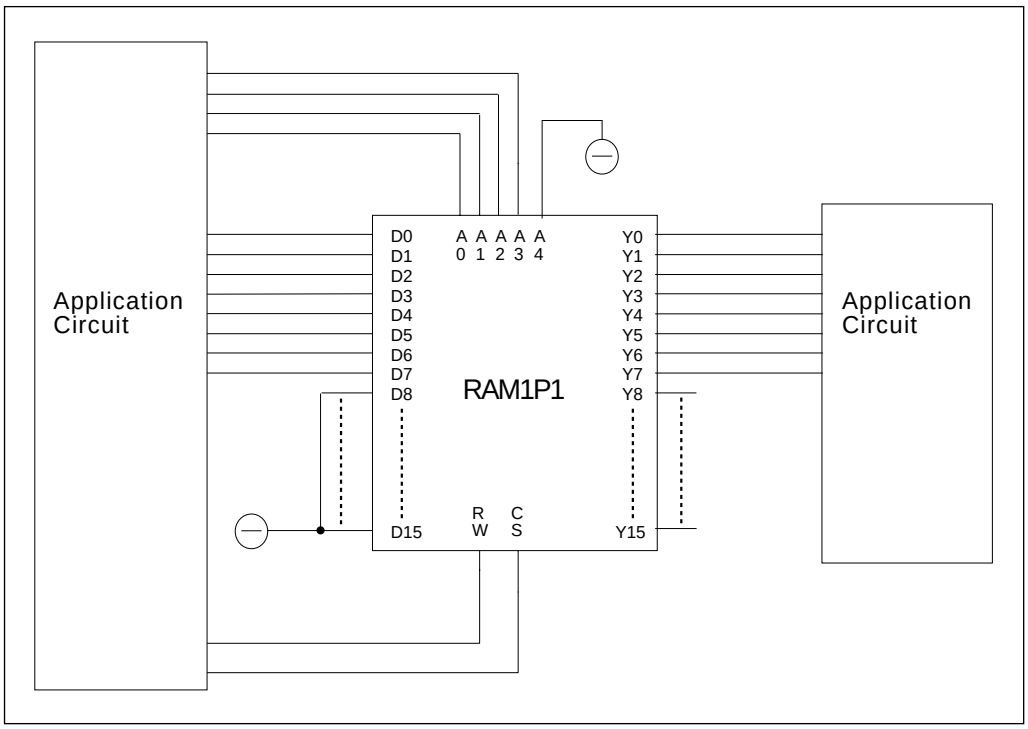


Figure 5-9 Example of the Use of RAM Symbols (RAM1P1: 16 words × 8 Bits)

Chapter 6: Circuit Design Taking Testability Into Account

Before a gate array is shipped the product is tested using an LSI tester. It is necessary to design the circuit keeping testability in mind to facilitate this testing. When designing the circuit, the following points should be carefully considered.

6.1 Considerations Regarding Circuit Initialization

When testing ICs using an LSI tester, or when verifying circuit functionality using a software simulator, the initial state of all sequential element is X (unknown). Consequently, very large test patterns may be necessary, depending on the circuit structure, to initialize the sequential elements or it may not be possible to initialize the circuits at all. Because of this, the circuits should be structured to facilitate easy initialization when they are designed (for example, by using sequential elements which have reset, set or preset functions).

6.2 Considerations Regarding Compressing the Test Patterns

As the gate densities of circuits increase, there is a tendency for test patterns to become larger as well. However, one must understand that there are constraints, such as shown below, to the LSI device tests.

Number of events per test pattern:	256K events or less
Number of test patterns:	30 test patterns or less
Total number of test pattern events:	1M events or less

These event and test pattern constraints include the test patterns for test patterns for leakage testing, test patterns for test circuits, and it includes the test pattern for ROM and megabyte- cell prepared by EPSON. Contact our sales office for the number of test patterns for ROM and megabyte cells. Although the RAM test patterns prepared by a customer are restricted, there is no restriction on the full test pattern prepared by EPSON.

When designing, please structure circuits in such a way as to increase the testability of the circuit (and to allow the compression of the test patterns), using methods such as including test pins which allow the input of clocks between the counter stages and adding test pins by which to monitor internal signals.

6.3 RAM Test Circuit

When a RAM is used it is necessary to test all bits before shipping the product. RAM terminals must be accessible via primary I/O pins. RAM test circuitry can be implemented, which multiplexes existing pin functionality with direct RAM access functionality so as to avoid increasing the designs pin count.

Also, when multiple RAMs are used, we recommend that each RAM's pins be accessible via unique I/O pins. However, when the number of external I/O pins is inadequate, each RAM's pins may share common external I/O pins. Please insure that while in RAM test mode, all RAM CS pins can be held "Low" simultaneously to facilitate quiescent current meas urement.

Figure 6-1 is an example of a test circuit for two word x 2 bit RAMs. When the test pin "TEST" is "Low", then normal functioning is performed. However, when the test pin "TEST" is "High", then the external pins ICS, IRW, ID0, ID1, and IA0 can write data directly to the RAM, and at the same time the RAM outputs can be read from the external pins AY0 and AY1.

Although it is possible to share the RAM pins with bi-directional pins or 3-state output pins, it is necessary to tie the bi-directional pins to either an input or an output state during RAM test. However, please do not share a bi-directional buffer with a pull-up resistor with the RAM output, and do not share a input buffer with a pull-up with the RAM CS pin, because doing so would make it impossible to measure the quiescent current.

When multiple RAMs are used, all RAM CS pins can be held “Low” simultaneously to facilitate quiecent current measurement.

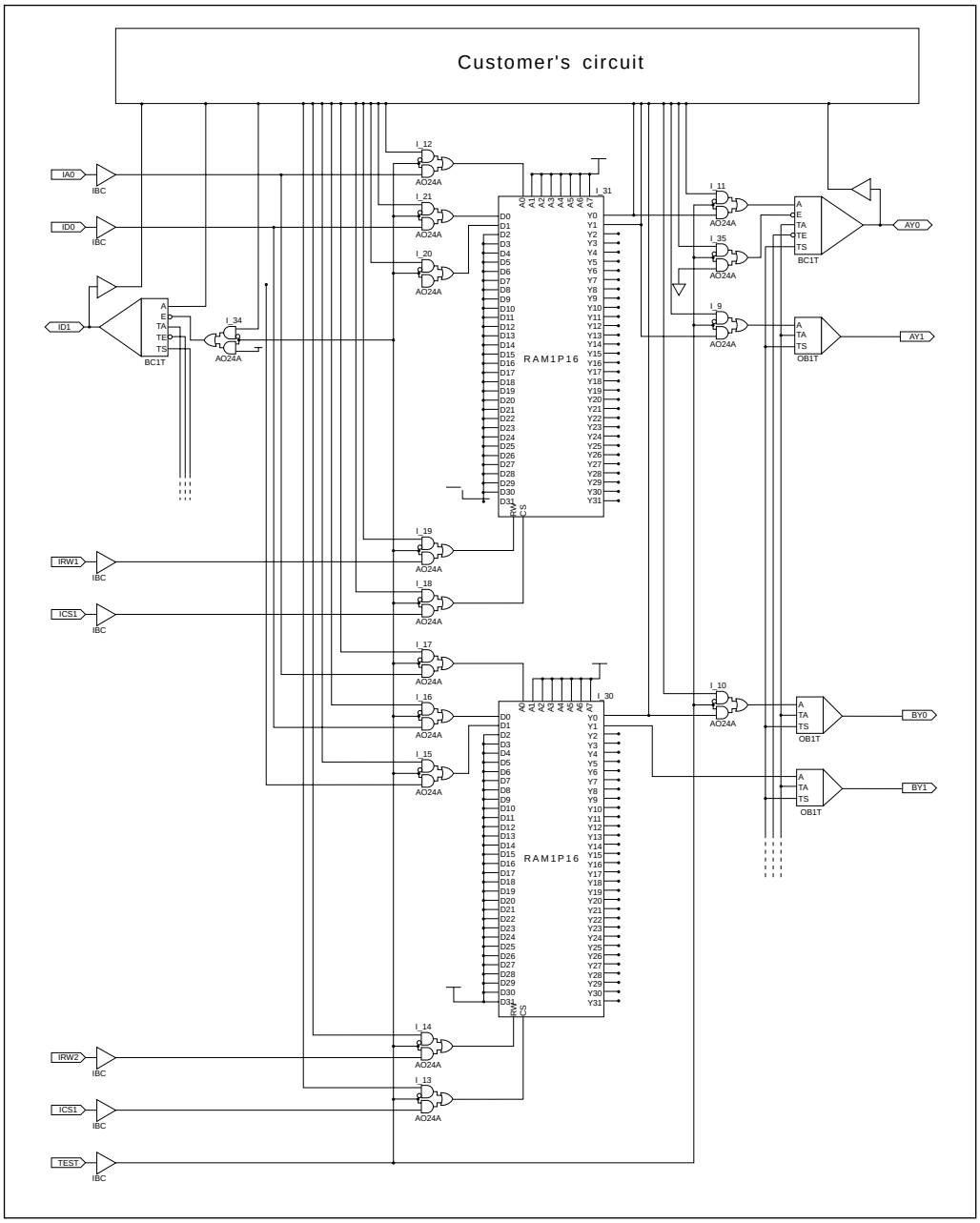


Figure 6-1 Example of a RAM Test Circuit

6.3.1 RAM Test Patterns

After incorporating RAM test circuitry, it is necessary to make test patterns for both the normal operating state and the test state of the chip. Checks are performed in the normal state to verify the connection with the user circuits, and are performed to insure that the test circuit is correct in the test state. Also, we request a test pattern to serve as a template when EPSON generates the RAM test pattern. See Figure 6-2 and 6-3 for an outline of how to generate this test pattern.

This pattern serves as a template for 1-port RAM tests.

< Example of APF Format >

```
$RATE  200000
$STROBE 185000
$RESOLUTION 0.001ns

$NODE
INPA     I  0
INPB     I  0
INPC     I  0
INPD     I  0
INPE     I  0
INPF     I  0
INPG     I  0
INPH     N  20000 120000
INPI     I  0
TESTEN   I  0
   .
   .
OUTA     0
OUTB     0
OUTC     0
OUTD     0
   .
   .
$ENDNODE

$PATTERN
#                AAADDDDRC    YYYY
#                0120123WS    0123
#
            0    0001010101..XXXX..
            1    0001010N11..XXXX..
            2    0001010111..HLHL..
            3    1011111101..XXXX..
            4    1011111N11..XXXX..
            5    1011111111..HHHH..
            6    1110101101..XXXX..
            7    1110101N11..XXXX..
            8    1110101111..LHLH..
```

Please provide all I/O pins used in performing simulation.
Reference the timing chart below to set timing.

It is useful to place comments here.

When a sequence is necessary to set the test mode, input the pattern here.

[1] Access the lowest address, a middle address and the highest address.
[2] Structure a single access from 3 events (test cycles). In the first event, set the data and the address. in the next event, perform a write. In the third event, perform a read.
[3] Use an RZ waveform to describe the RW signal so that the write operation can be completed in a signal event.
[4] Change the data to be written for each address tested.
[5] Verify that the results are the same as expected form the results of the simulations.

Timing Chart

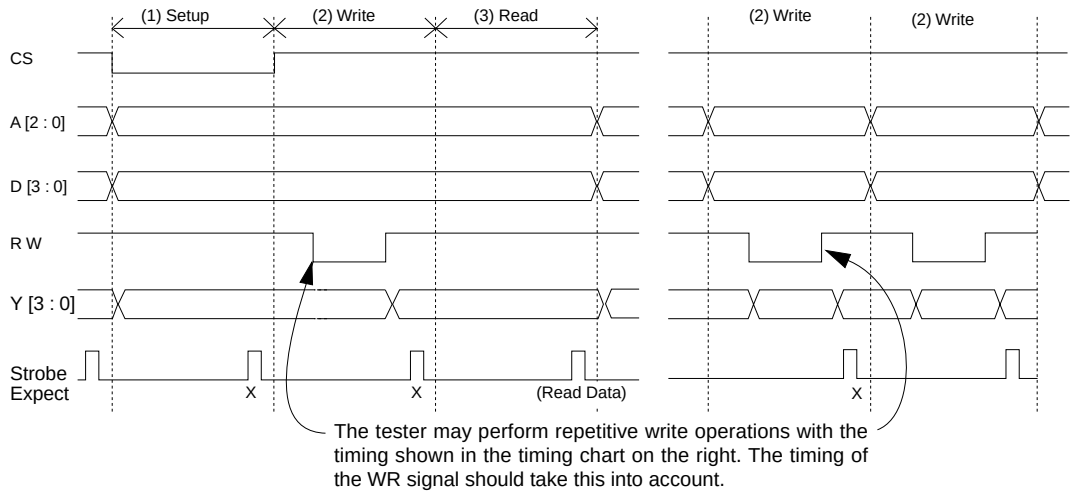


Figure 6-2 Generating 1-port RAM Test Pattern

This pattern serves as a template for 2-port RAM tests.

< Example of APF Format >

```
$RATE  200000
$STROBE 185000
$RESOLUTION 0.001ns

$NODE
INPA     I  0
INPB     I  0
INPC     I  0
INPD     I  0
INPE     I  0
INPF     I  0
INPG     I  0
INPH     I  0
INPI     I  0
INPJ     I  0
INPK     I  0
INPL     N  20000 120000
INPM     I  0
TESTEN   I  0
   .
   .
OUTA     0
OUTB     0
OUTC     0
OUTD     0
   .
   .
$ENDNODE

$PATTERN
#                RRRWWW
#                AAAAAADDDDRWC..YYYY..
#                0120120123DRS..0123..
#
            0    00000010100001.XXXX..
            1    00000010100P11.XXXX..
            2    00000010101011.HLHL..
            3    10110111110001.XXXX..
            4    10110111110P11.XXXX..
            5    10110111111011.HHHH..
            6    11111101010001.XXXX..
            7    11111101010P11.XXXX..
            8    11111101011011.LHLH..
```

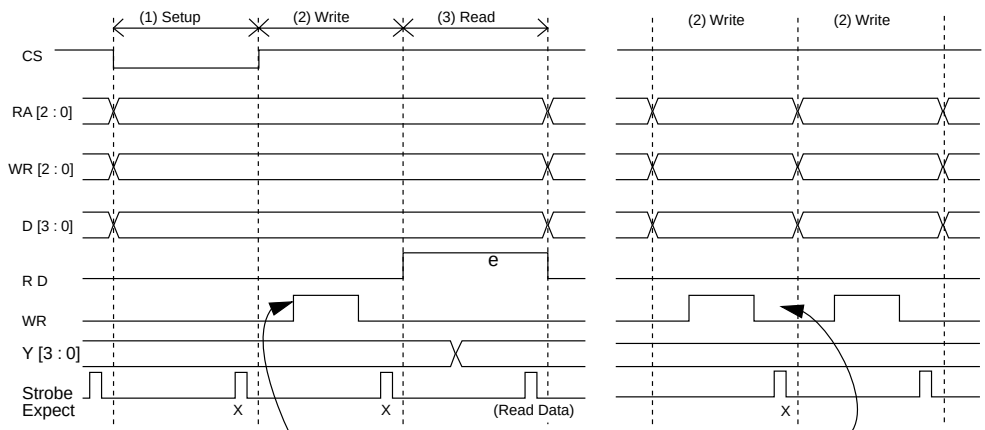
Please provide all I/O pins used in performing simulation.
Reference the timing chart below to set timing.

It is useful to place comments here.

When a sequence is necessary to set the test mode, input the pattern here.

[1] Access the lowest address, a middle address and the highest address.
[2] Structure a single access from 3 events (test cycles). In the first event, set the data and the address. in the next event, perform a write. In the third event, perform a read.
[3] Use an RZ waveform to describe the RW signal so that the write operation can be completed in a signal event.
[4] Change the data to be written for each address tested.
[5] Verify that the results are the same as expected form the results of the simulations.
[6] Set all bits of data to "1" when reading. However, if the write data consists entirely of logic 1 bits, all bits of data should be set to 0 when read out.

Timing Chart



The tester may perform repetitive write operations with the timing shown in the timing chart on the right. The timing of th WR signal should take this into account.

Figure 6-3 Generating 2-port RAM Test Pattern

6.4 Function Cell Test Circuits

When function cells are used, then testing the operation of all circuits (including the user circuits) requires a vast number of test patterns and a great amount of time. It is because of this that it is necessary to design test circuits able to verify the operation of each independent functional cell and user circuit, as was done with the RAM blocks. When designing the test circuits, please keep the following cautions and considerations in mind. For more details, contact EPSON.

6.4.1 Test Circuit Structures

(1) Provide test circuitry which facilitates direct access to all pins of each functional cell via I/O pins. Add a test circuit (connected to a terminal) which isolates each functional cell from the surrounding circuits.

(2) Even when functional cell input pins are fixed to V_{SS} or V_{DD}, design test circuitry which insures access to all functional cell pins.

(3) Even when functional cell output pins are not used, design test circuitry which insures access to all functional cell pins.

(4) Each functional cell pin must be connected to a unique I/O pin.

(5) Do not use sequential elements in the test circuitry for functional cells.

(6) Do not invert the input signal from the test input terminal and input it into the functional cell. Similarly, do not invert the functional cell output signal and output it to the test output terminal.

(7) There is no need to design a test circuit when the functional cell input pins and output pins are directly connected to the I/O pins.

(8) Do not use an input cell with pull-up or a bi-directional cell with pull-up as the test mode switch pin (although a bi-directional cell with pull-down may be used).

6.4.2 Test Patterns

The test patterns can be categorized into the following three types:

1) Test patterns to test only the user's circuit.
2) Test patterns to test all circuits.
3) Test patterns to test the functional cells only.

Test patterns that the customers generateare of type 1 and 2. Customers are not required to generate test patterns of type 3. EPSON maintains test patterns to be used for type 3. Please be advised that EPSON will not disclose information pertaining to the functional cell test patterns.

6.4.3 Test Circuit Data

Please provide the following information regarding functional test circuitry. This information is required for functional cell testing during simulation and IC device testing.

(1) Please clearly define the I/O pin to functional cell pin connectivity while in test mode.

(2) When the test circuits are structured in such a way that a single test terminal is able to test multiple functional cells, please clearly define the names of the functional cells which can be selected and the type of the test modes, and their relationships.

(3) Please clearly define pass numbers on the names of the functional cells on the drawings, and clearly define the test terminals and their association with functional cells, especially when identical functional cells are used more than once.

(4) Please clearly define the method of switching into test mode.

Please keep in mind to contact to our sales office when using functional cells and refer to "Functional Cells Design Guide".

6.5 Test Circuit Which Simplifies AC and DC Testing

Test Circuit Structure

The S1L50000 Series requires the construction of test circuits so that DC testing and AC testing can be done efficiently.

If the customer experiences difficulties while implementing test circuitry, then the customer should contact EPSON.

Figure 6-4 shows specific examples of test circuits. This figure should be referenced when designing test circuits. Recommended test circuit control and monitor pin configurations are shown below.

(1) Test Circuit Control and Monitor Pins

Please add or select the following 4 types of test pins.

- Dedicated input pin for testing: 1 pin (test enable signal:three pin [TSTEN,INP0,INP2] if it is possible.)
- Test mode select input pin: 3 pins (can be functionally shared with input pins of application)
- Monitor output pin for AC testing: 1 pin (can be functionally shared with output pin of application)
- Monitor output pin for DC testing: 1 pin (can be functionally shared with output pin of application)

Table 6-1 Test Terminal Constraints

Test Pin Type	Number of Pins	Name of Pins (See Fig. 6.4)	Constraints, Notes, Etc.
Test Enable Pin	1 Pin	TSTEN	Dedicated input pin Use ITST1. H: Test mode L: Normal mode
Test Mode Pins	3 Pins	INP0 INP1 INP2	May be shared with existing input pin. Do not share with an input pin associated with a critical path.
Monitor output pin for AC testing	1Pin	OUT3	May be shared with existing I/O buffers. Do not share with an N-channel open-drain cell.
Monitor output pin for DC testing	1Pin	OUT4	May be shared with existing I/O buffers. Do not share with an N-channel open-drain cell.
All output and bi-directional pins	—	—	Uses I/O buffers with test mode select .

(2) DC Test

Measurements are performed to insure that all input and output pins adhere to DC characteristic specifications. When test circuitry is not implemented, it is necessary for the customer to generate test patterns by which the DC characteristics can be measured. The amount of work in generating the test patterns may increase dramatically when there are no test circuits.

The task of generating test patterns and measuring the DC chracteristics is simplified by using test circuits.

(3) AC Testing

AC testing is a pin-to-pin (i.e. input pin to output pin) delay measurement. If device testing is not performed at actual operating frequency, device performance is assured through delay measurements along specific paths.

Also, the AC test monitor output pin is used to evaluate the variance between lots in the manufacturing process by measuring a defined AC path (cell name: ACP1). (When test circuits are used, be sure to insert cell ACP1 when designing the AC path test circuit.)

(4) Adding the Test Mode Control Circuit

The following items (a through j) pertain to test circuit implementation. Please refer to the test circuit examples of Figure 6-4.

a. Select 4 test input pins and 2 output pins

• Dedicated input pin for testing:	1pin (test enable signal:three pin [TSTEN,INP0,INP2] if it is possible.)
• Test mode select input pin: (Shared input pins)	3 pins (if there are three dedicated input pins, only a shared input pin is used.)
• Monitor output pin for AC testing: (Shared output pins)	1 pin
• Monitor output pin for DC testing: (Shared output pins)	1 pin

b. The dedicated input pin for test enable/disable (TSTEN) must use cell ITST1. If three pins for testing can be selected, do not use ITST1 to the second and third input cells. In this case, the second and third dedicated input pins correspond to INP0, INP2.

c. The dedicated or shared input pins for test mode selection (INP0, INP1 and INP2) can use any input buffer cell type. Avoid sharing these test inputs with critical path input pins of the application.

d. The dedicated or shared output pins for AC monitoring (OUT3 and OUT4) can use any uni-directional output buffer type (except 3-state type). Avoid sharing these test outputs with critical path output pins of the application.

e. All I/O buffers for output and bi-directional pin configurations must have test mode functionality.

f. Please utilize the test mode control circuit (TCIR).

g. The primary test enable/disable signal (output pin ‘IN’ of cell ITST1) should be connected to the ‘TST’ and ‘VTI’ input pins of functional block TCIR. When this signal is enabled (set to logic “High”), the test mode control circuitry (block TCIR) becomes functional and facili tates AC and quiescent current testing.

h. Three dedicated shared input signals (output pins of uni-directional input buffer cells) tates AC and quiescent current testing.
A first dedicated/shared input signal (INP0 in Figure 6-4) should be connected to input pin ‘IP0’ of functional block TCIR. This signal will control the mode of all bi-directional I/O cells which utilize pre-drivers with test functionality. When ‘IP0’ is state ‘High’ and ‘IP2’ is state ‘High’ , all bi-directional I/O will be placed in input mode, and all 3-state outputs will be in high-impedance state. When ‘IP0’ is state ‘Low’, all bi-directional and 3-state I/O will be in output mode.

A second dedicated/shared input signal (INP1 in Figure 6.4) should be connected to input pin 'IP1' of functional block TCIR. This signal controls output data while in test mode. The data which appears at pin 'IP1' will be passed to all output and bi-directional I/O cells when 'IP2' is state 'L'.

A third dedicated/shared input signal (INP2 in Figure 6.4) should be connected to input signal pin 'IP2' of functional block TCIR. This signal controls all output and bi-directional signals excluding the AC monitor output pin during AC testing. When input signal 'IP2' is state 'H' and all outputs remain in stable state 'H' so as to minimize switching noise during AC testing.

i. The following describes the recommended connections for the output pins of the test circuit functional block TCIR.

The TCIR output pin 'ACO' is used for AC characterization testing. This output of TCIR must be connected to one and only one 'TA' input pin of a user selected I/O buffers (OUT3), which is connected to a uni-directional output driver (not 3-state).

The TCIR output pin 'TS' is the test mode control signal. This output is used to put all I/O buffers connected to output and bi-directional I/O's into test mode. When 'TS' is state 'H', all I/O buffers are in test mode

The TCIR output pin 'TA' is the test mode control signal. This output is used to put all I/O buffers 'TA' input pin for the test pins (OUT3, OUT4).

The TCIR output pin 'TE' is used for test mode bi-directional enable (or control). This output is connected to all 3-state and bi-directional I/O buffers 'TE' input pin. when 'TE' is state 'L', all 3-state (OUT2) and bi-directional drivers (BID1) are placed in output mode.

The TCIR output pin 'VTO' is used for DC characterization testing. The output of TCIR must be connected to 'TA' input pin of a user selected I/O buffers (OUT4).

j. Fan-out violations which may occur on TCIR I/O buffers 'TA', 'TE' and 'TS' can be ignored.

(5) Setting the Test Mode (Please refer to Figure 6.4)

a. DC Test

• Quiescent Current Measurement Mode

TSTEN	. . . High
INP0	. . . Low
NP1	. . . High or Low
INP2	. . . Low

• Output Characteristics (V_{OH}/V_{OL}) Measurement Mode

TSTEN	. . . High
INP0	. . . High
INP1	. . . High for V_{OH} test and Low for V_{OL} test
INP2	. . . This controls the bi-directional pin mode
High	. . . Hi-Z (input) mode*
Low	. . . Output mode

* Can be used as bi-directional off-state leakage current measurement mode.

• Input Logic Level Mode

TSTEN	. . . High
INP0	. . . High
INP1	. . . High or Low
INP2	. . . High
Measurement pin	. . . Input of High or Low
OUT4	. . .Output of High or Low

• Dedicated AC Path Measurement Mode

TSTEN	. . . High
INP0	. . . Low
INP1	. . . Input of High or Low
OUT3	. . . Outpout of High or Low
INP2	. . . High

Generating the Test Pattern

It is necessary for the customer to design test patterns at the same time that the customer designs the test circuits so that the DC testing and the AC testing can be performed in an efficient manner.

Figure 6-5 shows a specific example of the test pattern related to the test circuits in Figure 6.4. The following should be kept in mind when generating the test patterns:

a. Please generate a test pattern to exercise test circuitry separate from standard application functional test patterns. The test patterns on the checking mode at the level of input logic circuits can only be created by EPSON.

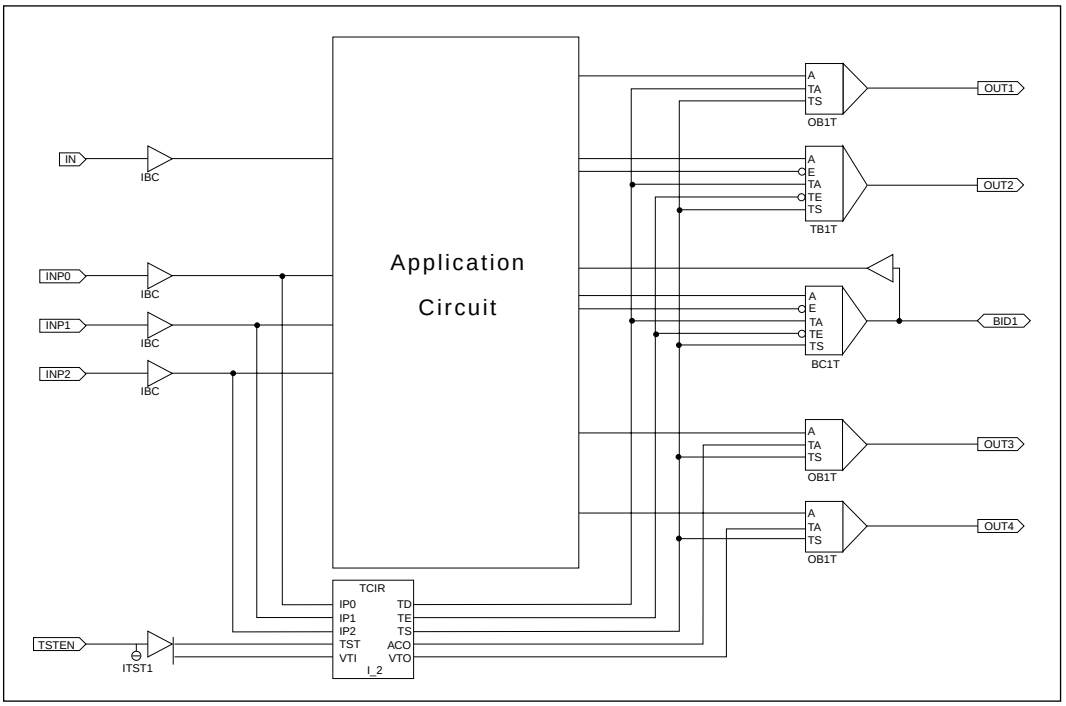
b. Test circuit test patterns must specify all input, output and bi-directional I/O signals.

c. Please insure that the dedicated test enable pin (i.e. TESTEN in Figure 6.4) is present and set to state “0” in the standard application functional test patterns.

d. When the input level (TSTEN) of test terminal is set to “1” all pull-up resistance are non-active (off).

Notes on the test circuit

When the dedicated input pin for test is only one, input logic levels assigned for INP0 and INP2 of test mode selectable pins can not be measured on the condition of testing input logic level testing mode.



<Test mode control circuit "TCIR">

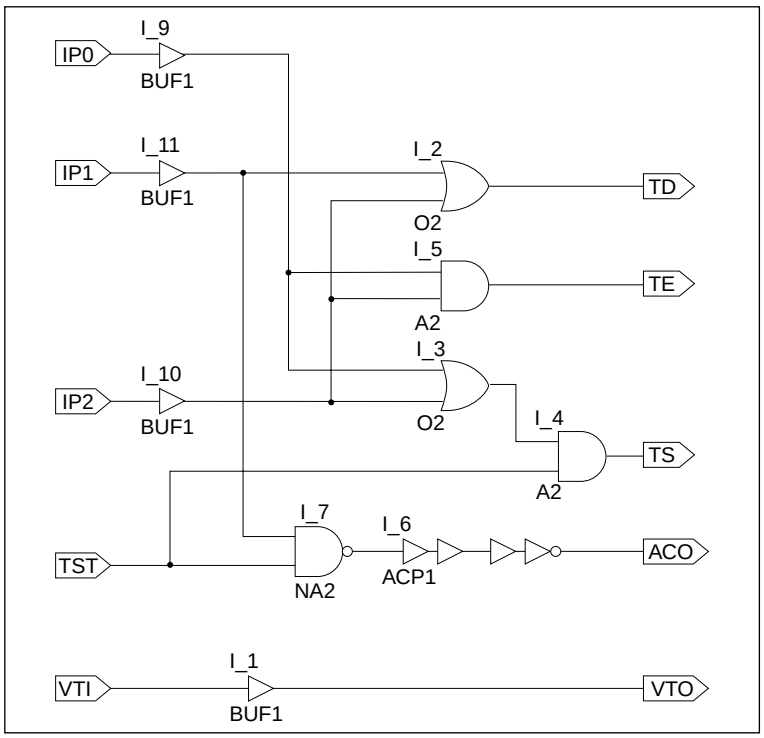


Figure 6-4 Example of Test Circuit

< Example of APF Format >

```
* EXAMPLE of Test Pattern for AC & DC Test
  $DESIGN  ram_demo

  $RATE 200000
  $STROBE 185000
  $RESOLUTION 0.001ns

  $IOCONT
  AA08.E  E0  BID1
  $ENDIOCONT

  $NODE
  TSTEN   I  0
  INP0    I  0
  INP1    I  0
  INP2    I  0
  IN      I  0
  BID1    BU 0
  OUT1    0
  OUT2    0
  OUT3    0
  OUT4    0
  $ENDNODE

  $PATTERN
  #            TIIIIBOOOO
  #            SNNNNIUUUU
  #            TPPP DTTTT
  #            E012 11234
  #            N
  #
  #            IIIIIBOOOO
  #                 U
  #

           0   0000..LXXXX
           1   1000..LXXXX ; Pull-up/down off
           2   1001..HHHLX ; AC path (L), other output all High
           3   1011..HHHHX ; AC path (H), other output all High
           4   1001..HHHLX ; AC path (L), other output all High
           5   1101..0HZLX ; Off state except normal output (Low input)
           6   1111..1HZHX ; Off state except normal output (High input)
           7   1100..LLLLX ; Output all Low
           8   1110..HHHHX ; Output all High

  $ENDPATTERN

  #
  # EOF
```

Measurement Process
→Static current consumption
→Dedicated AC path
→ ↑
→ ↑
→Off state leak current
→ ↑
→Output characteristics
→ ↑

note)
. is 1 or 0 input

Figure 6-5 Example of the generation of a test pattern when there is a test option

Chapter 7: Propagation Delay and Timing

Propagation delay time is determined by the intrinsic cell delay and by the per-load delay, which is a function of the wire interconnect and fan-in capacitances.

Delay times vary depending upon power supply voltage, ambient temperature, and process conditions. They also vary depending on factors involved in the structure of the circuit, input waveform, input logic level, and the mirror effect.

Post Simulation uses more acculate environment. At the development of S1L50000 series cells, the support tools can be used to calculate highly accurate delay times in the several cases that happened to change. Therefore, the delay time values calculated by the formula described later are different from the values listed at the "Gate Array S1L50000 Series MSI Cell Library".

7.1 Notes on the relationship between Ta and Tj

The propagation delay of C-MOS IC is basically changed by Tj (i.e. temperature at junctions). The IC is specified by Ta. However, the relation between Tj and Ta is not constant, but changes with thermal resistance and power consumption. (Refer to chapter 9. 2 for detail.)

In ASIC design, each package and IC power consumption is changed by a circuit and an application. Therefore, it is very difficult to specify according to Ta. Then, in the S1L50000 series, propagation delay libraries are ready for checking at initial design under the following conditions:

* Tj = 0 to 85°C library using for Ta = 0 to 70°C
* Tj = -40 to 125°C library using for Ta = -40 to 85°C

When the relation between Ta and Tj is very different from the normal values by estimating the package and application, the Tj=-40 to 125°C library can be used for Ta=0 to 70°C or other conditions should be considered if necessary.

7.2 Simple Delay Models

Simple propagation delay time t_{pd} can be calculated using the following formula:

$$t_{pd} = T_0 + K \times (\sum \text{Load A} + \text{Load B})$$

where,	T_0:	Intrinsic cell delay [ps]
	K:	Load delay coefficient [ps/Lu]
	Load A:	The input load capacitance due to fan-in [Lu]
	Load B:	The interconnect load capacitance [Lu]

Note: The values for T_0 and K differ depending upon the operating voltage, the ambient temperature, and the process conditions. Use the values provided in the "Gate Array S1L50000 Series MSI Cell Library." The unit "LU" stands for loading unit, which is equivalent to one "IN1" input fan-in.

Typ. values for T_0 and K (V_{DD} = nominal value, Ta = 25°C, and process = nominal value) are found in the "Gate Array S1L50000 Series MSI Cell Library". Select Typ. values for T_0 and K according to the target power supply voltage.

The Min. value for T_0 and K (where V_{DD} is the Max. value, Ta = Min. value and process = fast) and the Max. value for T_0 and K (where V_{DD} = Min. value, Ta = Max. value, and process = slow) are calculated by multiplying the Typ. value, described above, by the delay coefficient M. (These Min. and Max. values are required to verify ASIC operation over commercial and industrial variances in supply voltage, ambient temperature and process.)

The delay coefficient M can be calculated using the following formula:

$$M = M_V \times M_T \times M_P$$

where, M_V: Delay Multiplier due to voltage variation
M_T: Delay Multiplier due to temperature variation
M_P: Delay Multiplier due to process variation

Although values for M_V and M_T can be obtained by reading them off of the characteristic graphs in the "Gate Array S1L50000 Series MSI Cell Library," please use the duration delay coefficient vaues M, given in Table 7.1. Also, please direct inquiries to the EPSON regarding ASIC operation outside of the limits shown in Table 7-1.

Note 1:The delay for the pre-driver with level shifter cannot be calculated by merely multiplying a coefficient as shown above. Pre-calculated Min. values and Max. values are listed in the "Gate Array S1L50000 Series MSI Cell Library" along with the Typ. values. Please see "11.4 Delay Calculations for Dual Power Supplies."

Table 7-1 Delay Coefficient M
(Used for All Cells Excluding Pre-driver with Level Shifter)

Conditions	M Value			Usage
	$M_{min.}$	$M_{typ.}$	$M_{max.}$	
Power supply voltage: 3.3V ± 0.3V; Ta: 0 to 70°C*1	0.60 (0.65)	1.00 (1.00)	1.60 (1.51)	Use after multiplying the Typ. values of T_0 and K for V_{DD} = 3.3V
Power supply voltage: 3.3V ± 0.3V; Ta: -40 to 85°C*2	0.58 (0.62)	1.00 (1.00)	1.67 (1.57)	
Power supply voltage: 2.5V ± 0.25V; Ta: 0 to 70°C*1	0.53 (0.57)	1.00 (1.00)	1.84 (1.73)	Use after multiplying the Typ. values of T_0 and K for V_{DD} = 2.5V
Power supply voltage: 2.5V ± 0.25V; Ta: -40 to 85°C*2	0.51 (0.55)	1.00 (1.00)	1.91 (1.80)	

The valule included the parenthesis are given for I/O buffer and others are given for MSI Cells.

*1: The temperature range is set to Tj=0 to 85°C.

*2: The temperature range is set to Tj=-40 to 125°C.

7.3 Load Due to Input Capacitance (Load A)

Cell propagation delay is dependent upon the sum of input pin capacitances (Load A) attached to the cell's output terminal (i.e. the sum of the fan-ins). The input capacitances (fan-ins) of each gate and the output terminal load constraints (fan-outs) are listed in the "Gate Array S1L50000 Series MSI Cell Library". Cell output terminal fan-out must not exceed the listed Max. value. A Load A calculation example is shown in Figure 7-1 and Table 7-2.

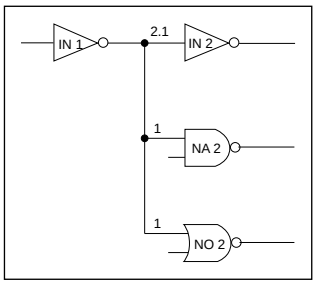


Figure 7-1 Example Calculating Load A

Table 7-2 Data Used in the Example of Calculating Load A

Cell	Input		Output	
	Pin	Fan-in	Pin	Fan-out
IN1	A	1.0	X	23.6
IN2	A	2.1	X	47.3
NA2	A1 A2	1.0 1.0	X	23.2
NO2	A1 A2	1.0 1.0	X	12.0

The fan-in values for IN2, NA2, and NO2 can be obtained from Table 7.2. Their sum is the Load A value, as seen by the IN1 output terminal in load units (LU).

ΣLoad A (IN1) = (Fan-in of IN2) + (Fan-in of NA2) + (Fan-in of NO2)
= 2.1LU+ 1LU + 1LU = 4.1LU

7.4 Load Due to Interconnect Capacitance (Load B)

The load resulting from the capacitance of the interconnect between cells (Load B) cannot be accurately calculated until the ASIC layout has been performed. However, Load B is correlated with the number of branches (number of nodes) connected to the wire, so it is possible to statistically estimate the Load B value. The estimated interconnect capacitance for each master is listed in the "Gate Array S1L50000 Series MSI Cell Library".

7.5 Propagation Delay Calculations

Below we present a sample propagation delay time calculation using the circuit shown in Figure 7.2 (assume an operating voltage of 3.3V) and the data of Table 7.3.

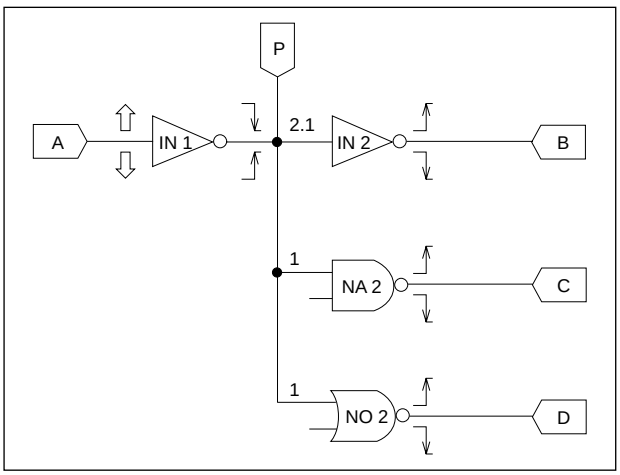


Figure 7-2 Circuit for the Sample Calculation of the Propagation Delay Time

Table 7-3 Characteristics (Power Supply Voltage = 3.3V)

Cell	Input		Output		t_{pd} (Typ.)				
	Pin	Fan-in	Pin	Fan-out	From	To	Edge	t_0 (ps)	K (ps/LU)
IN1	A	1.0	X	23.6	A	X	↑	77	23.2
							↓	81	12.7
IN2	A	2.1	X	47.3	A	X	↑	63	11.6
							↓	62	6.4
NA2	A1	1.0	X	23.2	A	X	↑	94	23.2
							↓	87	21.9
NO2	A1	1.0	X	12.0	A	X	↑	90	45.0
							↓	92	12.8

For this example, assume that Load B of NODE P = 2 (LU), and assume that Load B of Nodes B, C and D = 0 (LU). Also, note that propagation delay varies depending on the output terminal state transition (rising or falling edge). Below please find examples calculating the propagation delays for paths A to P, A to B, A to C and A to D for both rising and falling cases under typical operating conditions at 3.3V.

1. PATH A to P: $t_{pd} = t_{pd}$ (IN1)

   t_{pd} (A_{rising} to $P_{falling}$) $= T_0 + K \times$ (Load A + Load B)
   $= 81 + 12.7 \times (4.1+2)$
   $= 158.5$(ps)

   t_{pd} (A_{rising} to $P_{falling}$) $= T_0 + K \times$ (Load A + Load B)
   $= 77 + 23.2 \times (4.1+2)$
   $= 218.5$(ps)

2. PATH A to B: $t_{pd} = t_{pd}$ (IN1) + t_{pd} (IN2)

   t_{pd} (A_{rising} to B_{rising}) $= t_{pd}$ (A_{rising} to $P_{falling}$) + t_{pd} ($P_{falling}$ to B_{rising})
   $= 158.5 + t_0$
   $= 158.5 + 63$
   $= 221.5$(ps)

   t_{pd} ($A_{falling}$ to $B_{falling}$) $= t_{pd}$ ($A_{falling}$ to P_{rising}) + t_{pd} (P_{rising} to $B_{falling}$)
   $= 218.5 + t_0$
   $= 218.5 + 62$
   $= 280.5$(ps)

3. PATH A to C: $t_{pd} = t_{pd}$ (IN1) + t_{pd} (NA2)

   t_{pd} (A_{rising} to C_{rising}) $= t_{pd}$ (A_{rising} to $P_{falling}$) + t_{pd} ($P_{falling}$ to C_{rising})
   $= 158.5 + t_0$
   $= 158.5 + 94$
   $= 252.5$(ps)

   t_{pd} ($A_{falling}$ to $C_{falling}$) $= t_{pd}$ ($A_{falling}$ to P_{rising}) + t_{pd} (P_{rising} to $C_{falling}$)
   $= 218.5 + t_0$
   $= 218.5 + 87$
   $= 305.5$(ps)

4. PATH A to D: $t_{pd} = t_{pd}$ (IN1) + t_{pd} (NO2)

   t_{pd} (A_{rising} to D_{rising}) $= t_{pd}$ (A_{rising} to $P_{falling}$) + t_{pd} ($P_{falling}$ to D_{rising})
   $= 158.5 + t_0$
   $= 158.5 + 90$
   $= 248.5$(ps)

   t_{pd} ($A_{falling}$ to $D_{falling}$) $= t_{pd}$ ($A_{falling}$ to P_{rising}) + t_{pd} (P_{rising} to $D_{falling}$)
   $= 218.5 + t_0$
   $= 218.5 + 92$
   $= 310.5$(ps)

7.6 Calculating Output Buffer Delay

Assuming that the load capacitance connected to the output buffer is C_L, the delay time t_{pd} is calculated as follows:

$t_{pd} = T_0$ (Output cell) + K (Output cell) $\times C_L/10$

T_0 (Output cell)	:	The intrinsic delay of the output cell	[ps]
K (Output cell)	:	The output cell load delay coefficient	[ps/10pF]
C_L	:	The load capacitance connected	[pF]

Please reference the “Gate Array S1L50000 Series MSI Cell Library” regarding the intrinsic delays and load delay coefficients of the output cells and pre-drivers.

7.7 Sequential Buffer Setup/Hold Time

A critical factor to analyze when designing an ASIC is sequential cell usage and operation. Data which is to be stored by sequential logic must arrive before the gating or clock signal to insure sufficient data setup and proper operation. That same data must remain unchanged or held subsequent to the gating or clock signal. These timing rules and others (see below) must be taken into consideration when designing sequential logic. Sequential cell specific timing values can be found in the “Gate Array S1L50000 Series MSI Cell Library”.

(1) Min. Pulse Width: TPWC, TPWS or TPWR

The Min. pulse width refers to the Min. value of the time between a leading edge and a trailing edge of an input pulse waveform, as seen at the clock, set, preset or reset terminal of a sequential cell. Circuit malfunction may occur when a narrow pulse is applied which volates this constraint.

The Min. pulse widths may be of the following three types:

- Clock signal Min. pulse width violation.
- Set signal Min. pulse width violation.
- Reset signal Min. pulse width violation.

(2) Setup Time:

“Setup time” refers to the required time interval in which the data state must be set before the active edge transition of the gate or clock signal in order to correctly store the data in a sequential cell or an MSI function which is made up of sequential cells.

(3) Hold Time:

“Hold time” refers to the required time interval in which the data state must be held after the active edge of the gate or clock signal in order to correctly store the data in a sequential cell or an MSI function which is made up of sequential cells.

(4) Release Time (Setup):

“Release time” (setup) refers to the required time interval between a set/reset signal transition to inactive and the active edge of the gate or clock signal in a sequential cell of an MSI function which is made up of sequential cells.

(5) Release Time (Hold):

“Release time” (Hold) refers to the required time interval between a set/reset signal transition to active and the active edge of the gate or clock signal in a sequential cell or an MSI function which is made up of sequential cells.

(6) Set/Reset (Setup):

"Set/Reset" (Setup) refers to the required time interval after a set input state is released until it is possible to have a rising edge on a reset input in a sequential cell or MSI function which is made up of sequential cells.

(7) Set/Reset (Hold):

The "Set/Reset" (Hold) refers to the required time interval after a reset input state is released until it is possible to have a rising edge on a set input in a sequential cell or MSI function which is made up of sequential cells.Figure 7.3: DFSR (Example)

Please refer to each tool manual about timing error messages when simulating.

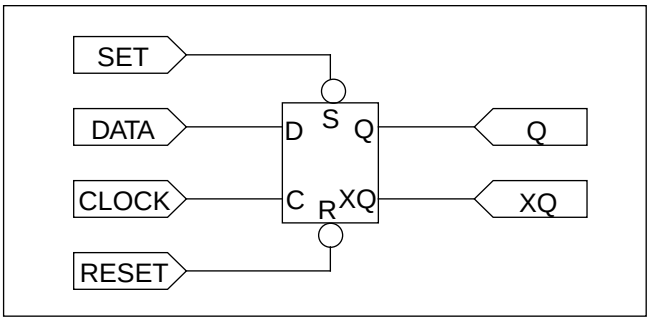


Figure 7-3 DFSR (Example)

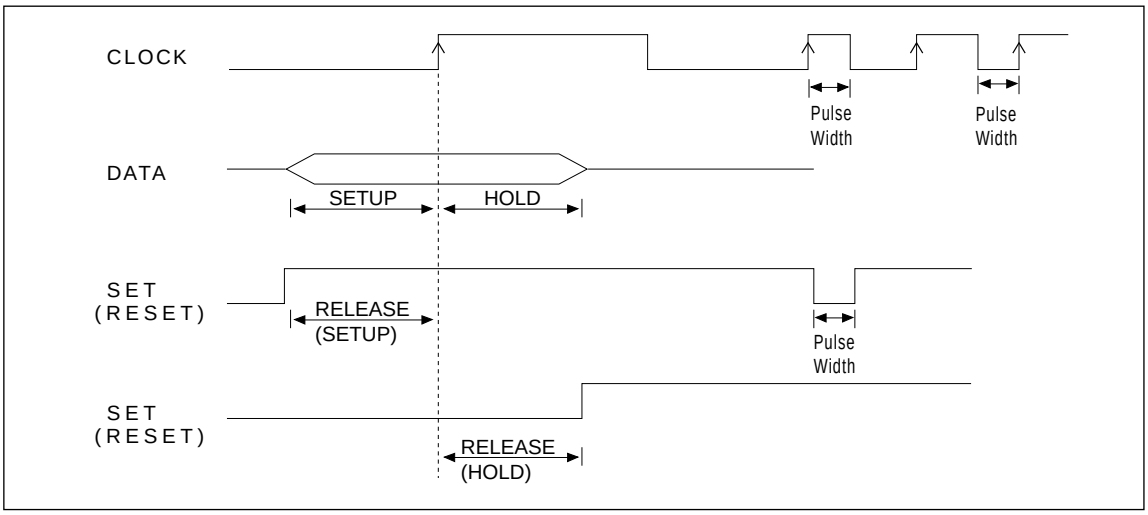


Figure 7-4 Timing Wave Form (Explanatory Diagram for Numbers 1-5)

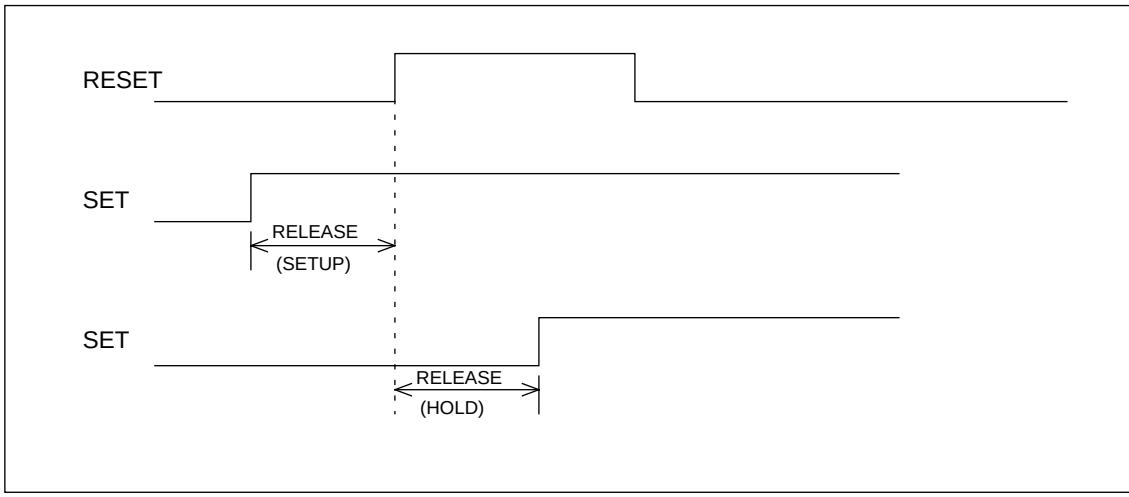


Figure 7-5 Timing Wave Form (Explanatory Diagram for Numbers 6-7)

The Flip-Flop set-up / hold time of the S1L50000 series is discribed at “Cell Library” on the same format shown in Table 7. 4. When using it , refer to each cell’s characteristics.

Table 7-4 DFSR Timing Characteristics (Example)

Pin	Setup time1 t_{su} (ps)	Hold time,t_h (ps)	Pulse width, t_w (ps)	Setup time, t_{su} (ps)	Hold time, t_h (ps)	Pulse width, t_w (ps)
	Typ.(V_{DD}=3.3V)	Typ.(V_{DD}=3.3V)	Typ.(V_{DD}=3.3V)	Typ.(V_{DD}=2.0V)	Typ.(V_{DD}=2.0V)	Typ.(V_{DD}=2.0V)
C(P) to D	567	149	—	966	314	—
C(P) to R	338	413	—	555	674	—
C(P) to S	408	393	—	687	645	—
R(P) to S(P)	530	—	—	879	—	—
C(P)	—	—	773	—	—	1306
C(N)	—	—	788	—	—	1323
R(N)	—	—	842	—	—	1416
S(N)	—	—	736	—	—	1258

Note : P = transition from 0 to 1 level or Positive pulse
N = transition from 1 to 0 level or Negative pulse

7.8 How to Use Cell

(1) *V or *O added

The *V mark, which is added for inverters and AND gates, indicates accelerated speed compared to the normal fan-out gate.

(2) “H” added at the end of the flip-flop cell name (DF system or LF system)

Though cells to which “H” is added at the end of the flip-flop cell name have the same gates and delay time of C to Q as a normal cell, they are set to a longer set-up time and shorter hold time. If there is some margin for set-up time in the set-up, it can be used as a technique for preventing holding time errors caused by clock skew.

(3) “L” added at the end of flip-flop-cell name (DF, LF, JK, and T systems)

Though cells to which “L” is added at the end of the flip-flop cell name have some delay time compared with normal cells of non-existing “L”, their power consumption is reduced by a half. When estimating the current consumption, the value of Kint should first be set to “0.5”. Furthermore, when designing a scanning type cell, replace it with the cell to which “L” is added at the end of scanning type cell name.

7.9 Chip Internal Skew

Because of transistor characteristic variance within an ASIC, the t_{pd} of similar gates within an ASIC may vary. Skew is a term used to describe this variance. Skew must be taken into account so as to provide margin in timing critical portions of logic to insure proper operation.

Table 7-5 Skew Within the Chip

Cell	Layout Area	Skew
Internal cells	All the regions	5%
I/O cell	All the regions	5%

Chapter 8: Test Pattern Generation

Test patterns must be generated once the logical design has been completed. Test patterns are used to simulate and verify circuit functionality. Test patterns are also used for product inspection prior to shipment. Please keep the following guidelines in mind when generating test patterns, thereby improving manufacturability and insuring product quality.

8.1 Testability Considerations

Because the test pattern is used in the final inspection of the product before it is shipped, it must be able to test all circuits within the LSI. If there are areas within the circuits of the LSI which are untested, it will not be possible to test those areas before the product is shipped, and thus there will be the danger of shipping defective product.

It is difficult to test all of the circuits within the LSI, so it is important to consider testability during the process of designing the circuit.

If the EPSON recommended test circuit is insert to the internal circuit of LSI, some conditions of DC test needed test patterns can be setting easily. Refer to the section 6.5 about DC or AC test in detail.

8.2 Waveform Types

Although the test pattern is normally a series of “0” and “1” when a simulation is performed or the LSI tester are run, the input wave forms can be delayed, and the wave forms can be changed. The wave forms which can be used when the test pattern is generated include the following two types:

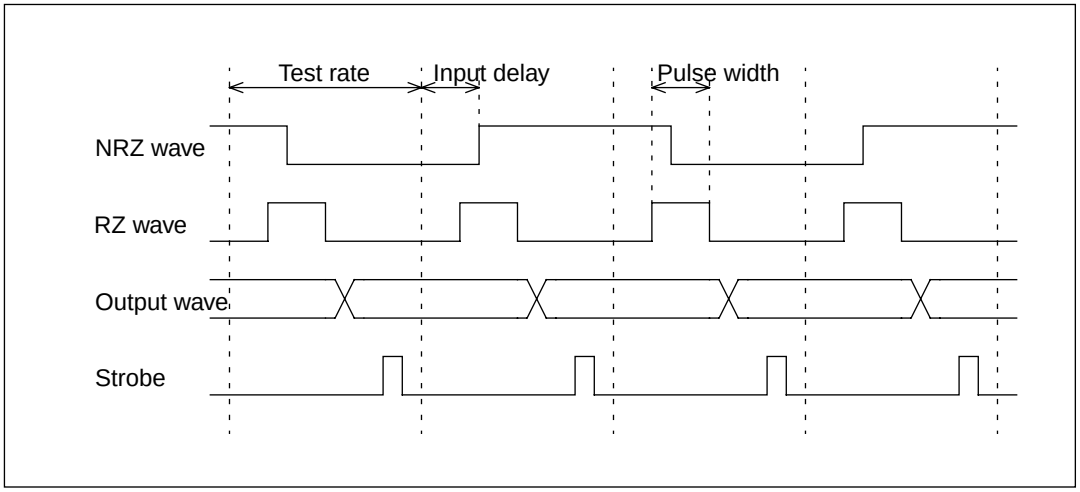


Figure 8-1 Constraints on Timing Settings

NRZ (Non Return to Zero)

A signal whose state changes no more than once per test period cycle is defined as being an NRZ type waveform. This waveform type can be delayed by a constant offset from the beginning of the test period cycle boundary.

RZ (Return to Zero)

A signal whose state may change twice per test period cycle is defined as being an RZ type waveform. This waveform type can be delayed by a constant offset from the beginning of the test period cycle boundary. This waveform type is useful for defining clock signals using positive or negative pulse definitions.

8.3 Constraints on the Types of Test Patterns

During design verification, test patterns can be set to accurately reflect actual operating frequency, yet in order to be used in final device inspection, the test patterns must adhere to constraints of the LSI tester. These constraints are explained below and should be kept in mind during test period development.

8.3.1 Test Period

The test period must be 100 nsec or longer in duration and is defined in 1 nsec intervals. (Recommended test period: 200nsec.)
The limitation described on the "8.3.5 Strobe" should be satisfied and defined the test period.

Number of events per test pattern:	256K events or less
Number of test patterns:	30 test patterns or less
Total number of test pattern events:	1M events or less

8.3.2 Input Delay

(a) Range of Input Delays

0 nsec ≤ input delay value < strobe point.
The input delay is defined in 1 nsec step within the range above. See Section 8.3.5 below regarding constraints on the strobe point.

(b) Input delay values must have a Min. of 3 nsec resolution from one another.

(c) Types of input delays

No more than 8 types of input delays can be used in a single test pattern. A 0 nsec delay is also counted as 1 type. When there are identical delays on an RZ wave form as on an NRZ wave form, these are counted as different delay types. When RZ wave form has identical delay value or NRZ wave form has identical delay value, these are counted as identical delay types.

8.3.3 Pulse Width

Pulse widths for RZ wave forms must be 15 nsec or more.

8.3.4 Input Waveform Format

The input wave form must assume a value of "0", "1", "P", or "N". "P" and "N" indicate RZ positive pulse and negative pulse type. Use state "0" to disable positive pulse RZ waveform, and state "1" to disable negative pulse RZ waveform (i.e. RZ type state combinations of (0,P) and (1,N) are valid, while state combinations of (0,N) and (1,P) are invalid).

Do not use a bi-directional pin as the clock.

8.3.5 Strobe

The constraints on the strobe are as follows.

(a) Only a single strobe may be used within a single test pattern event.

(b) The Min. value for a strobe should be at least 30 nsec after the completion of all output signal changes, where the change results from input signals state change applied during that event.

(c) The Max. value for the strobe should be the test period minus 15 nsec.

(d) The strobe is defined in 1 nsec step.

8.4 Notes Regarding DC Testing

The test pattern is used for functional testing and DC testing of the LSI. Please generate the test patterns so that the following DC tests can be performed.

DC tests are performed to verify the DC parameters of the LSI. Because the DC tests perform measurements on the trailing edge of the measurement events, those terminals which are measured must not have state changes after the strobe during the measurement events.

The DC parameters measured are as described below:

(a) Output Driver Test (V_{OH}, V_{OL})

The output buffer current driving capabilities are tested. The terminals which are to be tested are caused to enter the output level through the operation of the device, the specified current load is applied, and the level of the voltage drop is measured.

In order to perform the output driver tests, it is necessary for the test pattern to cause all of the terminals to enter all of the states which are obtained when the device is operating. Also, the states must be such that they do not change even if the measurement event extends the test period indefinitely.

(b) Quiescent Current Test (I_{DDS})

The quiescent current is the leakage current which flows to the LSI power supply when the input is in an fixed state. While generally this current is extremely small, this measurement must be done in a state where there are no other currents flowing aside from the leakage current. To do this, all of the following conditions must be fulfilled, and there must be two or more places wherein there are events which can measure the quiescent current.

(1) The input terminals are all in a fixed state.

(2) The bi-directional terminals are given “High” level or “Low” level inputs or are in an output state.

(3) There are no oscillators or operating functions within the circuit.

(4) None of the internal 3-state buffers (internal bus) are in a floating or a contention state.

(5) The RAM, the ROM, and the megacells are not in states wherein current is flowing.

(6) A “High” level input is applied to input terminals which have pull-up resistors.

(7) Bi-directional terminals with pull-up resistors attached are either given “High” level inputs or are producing “High” level outputs.

(8) Bi-directional terminals with pull-down resistors are either in an input state or are producing “Low” level outputs.

(c) The Input Current Test

The input current test measures the inputs to the input buffer. The test items include measurements of input leakage current and of pull-up/pull-down currents. The tests for these measurement items are performed by applying a V_{DD} level or V_{SS} level voltage to the terminal being measured, and measuring the current which flows. In other words, the test is performed by applying either a "High" level or a "Low" level voltage to the terminal being measured. For example, when a V_{DD} ("High" level) signal is applied during the test to a terminal being measured and which is in a state having a "Low" level, then there is the potential for this to cause the state to change from "Low" to "High" in the terminal being measured, and the potential that this will cause the LSI to function incorrectly.

In order to measure the input current tests, a test where a V_{DD} level is applied at an event where there is a "High" input to the terminal being measured in the test pattern, and a test is performed where a V_{SS} level is applied in the event where a "Low" is applied. Because of this, it is not possible to perform these tests when the terminals being measured are not in these states in the test pattern.

The input current tests are further broken down into the following classifications.

(1) Input Leakage Current Test (I_{IH}. I_{IL})

Measurements are performed regarding the input current of the input buffers which have no pull-up/pull-down resistors.

The current which flows when a "High" level voltage is applied to the input buffer is called I_{IH}, and its Max. current value is guaranteed. In order to perform this test there must be an event in the test pattern which causes the input terminal to be measured to have a "High" level input. Bi-directional terminals must have "High" level inputs in the input state.

The current which flows when a "Low" level voltage is applied to the input buffer is called I_{IL}, and its Max. value is guaranteed. In order to perform this test there must be an event in the test pattern which causes the input terminal to be measured to have a "Low" level input. Bi-directional terminals must have "Low" level inputs in the input state.

(2) Pull-up Current Tests (I_{PU})

This test measures the current which flows when a "Low" level voltage is applied to an input buffer having a pull-up resistance. In order to perform this test there must be an event in the test pattern which causes the input terminal to be measured to have a "Low" level input. Bi-directional terminals must have "Low" level inputs in the input state.

(3) Pull-down Current Tests (I_{PD})

This test measures the current which flows when a "High" level voltage is applied to an input buffer having a pull-down resistance. In order to perform this test there must be an event in the test pattern which causes the input terminal to be measured to have a "High" level input. Bi-directional terminals must have "High" level inputs in the input state.

(4) Off State Leakage Current (Ioz)

This measures the leakage current which flows when the output is a high-impedance state in output buffers which have open drains or which are 3-state output buffers. The actual measurement is the measurement of the currents when a V_{DD} level voltage is applied, and when a V_{SS} level voltage is applied to the terminal being measured when the terminal is in a high-impedance state. Because of this, the terminal being measured must enter into a high impedance state in the test pattern.

8.5 Notes Regarding the Use of Oscillation Circuits

An example of an oscillation circuit (oscillator, interval oscillator) is shown below.

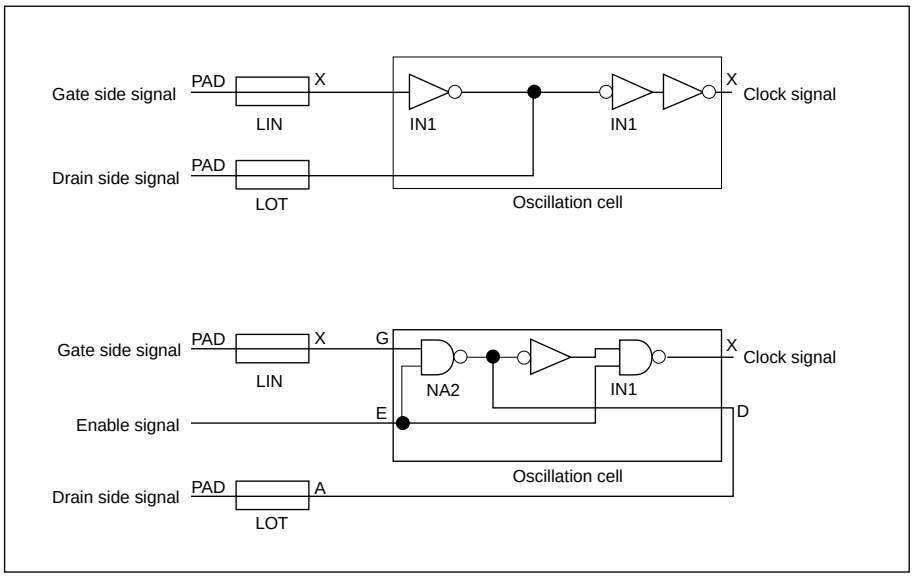


Figure 8-2 Example of Oscillation Circuits

Generally when oscillation circuits are used, the driving power of the oscillation inverter is small and the output wave form of the oscillation circuit is influenced by the load of the measurement environment. Thus the oscillation circuit is unable to transmit precise wave forms to the next-stage gates.

Because of this, in order to reproduce the conditions of the simulation in the tests, a procedure known as “reverse drive” (i.e. a procedure wherein a signal having the same wave form as the output from the drain is input to the drain terminal) is used.

When the oscillation inverter is structured as an inverter, it is possible to generate a reverse drive signal if the signal input from the drain is simply a reverse-phase input of the signal applied to the gate; however, in the case of NAND gate structures (known as interval oscillators or gated-OSC), then decisions cannot be made simply based on the gate signal alone, but rather the reverse drive wave form must be determined by looking at the expected. values of the drain terminal.

In this method, if the input wave form is the NRZ wave form and the strobe is at the end of the test period, then the input wave form is put to the drain terminal expected value directly and a reverse drive wave form can be generated. However, in the case of the RZ wave form, then the expected value of the drain terminal is fixed to either a “High” or a “Low” whether or oscillator is in a oscillating state or an oscillation stop state, so it is not possible to determine a reverse drive wave form by examining the expected state of the drain terminal.

Because of this, please keep the following cautions and notes in mind when a circuit having a interval oscillator is used:

(1) An RZ wave form cannot be used as the input signal.
(2) Do not cause transitions in the clock signal by transitions in the enable signal.

8.6 Regarding AC Testing

AC testing measures the time it takes for a signal to propagate to the output terminal when there has been a transition at the input terminal during a single event. The AC testing can be performed on a measurement path selected by the customer.

8.6.1 Constraints Regarding Measurement Events

Because this test is done using a testing method known as the "normal binary search method," the terminal being measured (i.e. the output terminal wherein there is a transition) must have only a single transition point within a measurement event. (Measurements cannot be performed on terminals having an RZ wave form output, nor can they be performed in situations where a hazard is output during the measurement event.) Also, the state transitions of the signal being measure must be either "High" to "Low" or "Low" to "High". (Transitions involving a high-impedance state cannot be measured.)

Other cautions and notes include the necessity for selecting events so that there are no signal contentions between the bi-directional terminals and the LSI tester, and that there are no situations where many output terminals have simultaneous transitions at the measurement event. This is because the LSI power source is overwhelmed when there are simultaneous transitions or signal contentions, affecting the output wave form of the terminals being measured and making it impossible to get an accurate measurement.

8.6.2 Constraints on the Measurement Locations for AC Testing

Please use only 4 or less measurement locations in the AC testing.

8.6.3 Constraints Regarding the Path Delay Which is Tested

The longer the delay in the AC measurement, the more accurate the measurement. The measurement path delay time should be recorded using Max. delay simulation conditions targeting a path delay value of 30 nsec or more, and less than the strobe point.

8.6.4 Other Constraints

(1) Do not designate a path from the oscillator circuit.

(2) Designate a path which does not pass through a circuit having an internal 3-state unit (i.e. the internal bus).

(3) Do not designate a path passing through other bi-directional cells between the input cell and the output cell of the measurement path.

(4) When there are two or more voltage ranges used, reconcile these to a single AC test measurement voltages.

8.7 Test Pattern Constraints for Bi-directional Pins

By the constraints of testing, the bi-directional pins cannot switch between input mode and output mode more than once within a single event. Because of this, the test pattern generated should not use an RZ wave form for controlling the bi-directional cell input/output mode switching.

Also, an RZ wave form cannot be used as an input to the bi-directional pin.

8.8 Notes on Devices at High Impedance

EPSON can not guarantee to operate the input pins of CMOS devices at high impedance, so EPSON forbids such operation when simulating the logic circuit. EPSON supplies the I/O cells with pull up or pull down resistor to prepare for high impedance. For the following reason, however, the changes in the signal due to pull up or pull down resistors do not reflect the propagation delay time in the simulation. This is because accurate operation can not be simulated, so EPSON forbids the use of I/O cells (including bi-directional pins) with pull up or pull down resistor not to be inputted at the input mode when simulating the logic circuit.

<Reasons Why Propagation Delay Time of Pull up or Pull down Resistor is not Considered>

- Propagation is greatly changed by the capacity of the external load.
- The pull up or pull down resistor is only used to prevent to be floating gates at the high impedance.

Before the simulation, EPSON checks the test pattern for the above contents using the tool. Correct the test pattern if "Z" is detected to represent the high impedance state at the bi-directional pins (including those with Nch open drain output).

For the above reason, also correct the test pattern if "Z" is detected at the bi-directional pins with a pull up or pull down resistor or at the open drain bi-directional pins.

<Countermeasure>

When checking the test patterns, all of the “Z” values indicated to bi-directional pins are indicated to be in error. (Except for “Z” outputted at the output pins of 3-state, Nch and open drain)

EPSON supports the utility program for modifying the test patterns such that if “Z” is outputted at the bi-directional pin with pull up resistor, replace “1” and if “Z” is outputted at the bi-directional pin with pull down resistor, replace “0”.

If the bi-directional pin indicated by “X” is set to be the input mode, “X” is transferred at the simulation and the “?” is outputted as the simulation result. The “?” must be corrected, and then the simulation is executed again.

Table 8-1 Handling the Signal at the Bi-Directional Pins in Simulation

Input Pattern	I/O mode	Simulation	Simulation Result (Outpout Pattern)
“X”	Inuput mode	“X’	“?”
“1”, “High”	Inuput mode	“1”	“1”
“0”, “Low”	Inuput mode	“0”	“0”

Chapter 9: Estimating the Power Consumption

CMOS LSIs consume very little current when they are not operating. However, when they are operating, the power they consume depends on the operating frequency. When the power consumed is large, then the temperature of the LSI chip increases, and the quality of the LSI can be negatively affected if the temperature of the chip gets too high.

Because of this, it is necessary to calculate the power consumption and to check whether or not the power consumption is within allowable tolerances.

9.1 Calculating the Power Consumption

The power consumption of a CMOS circuit is generally dependent on the operating frequency, the capacitance, and the power supply voltage. (This excludes those special situations where there is a normal current through RAM/ROM, etc.) Here the CMOS gate array power consumption can be calculated easily if the operating frequencies and load captaincies of the various cells used within the circuit are known. However, because it is difficult to calculate the load captaincies for each internal cell, use the rough calculations described below.

After the power consumption for the input buffers, the output buffers and the internal cells are calculated, and these values are summed to produce the total power consumption.

Because of this, the total power consumption P_{total} is calculated as follows:

$$P_{total} = P_i + P_O + P_{int}$$

P_i : Power consumption of input buffer
P_o : Power consumption of output buffer
P_{int} : Power consumption of internal cells

Please see Chapter 11 regarding power consumption calculations for dual power supplies.

(1) The Input buffer Power Consumption (P_i)

The input buffer power consumption is the sum of the products of the signal frequencies (MHz) input into each buffer, and the input buffer power coefficient K_{pi} (µW/MHz) for each buffer.

$$P_i = \sum_{i=1}^{K} (K_{pi} \times f_i) \quad (W)$$

K_{pi} : Input Buffer Power Coefficient (Refer to Table 9-1.)
f_i : The operating frequency of the ith input buffer (MHz)

Table 9-1 K_{pi} of input buffer in the S1L50000 Series

V_{DD} (Typ)	K_{pi}
3.3V	6.2µW/MHz
2.5V	3.6µW/MHz

(2) Output Buffer Power Consumption (Po)

The output buffer power consumption differs depending on whether the load is a direct current load (such as resistive loads, TTL device connections, etc.) or whether the loads are alternating current loads (such as capacitance loads, CMOS device connections, etc.).

In the case of alternating current loads, the output buffer power consumption is calculated from the load capacitance C_L as follows:

• Alternating current power consumption

$$P_{AC} = f \times C_L \times (V_{DD})^2 \quad (W)$$

f: Output buffer operating frequency (Hz)
C_L: Load capacitance (F)
V_{DD}: Power supply voltage (V)

In the case of the direct current load, the power consumed in the direct current load is added to the power consumed in the alternating current load.

• Direct current power consumption

$$P_{DC} = P_{DCH} + P_{DCL}$$

Where,

$$P_{DCH} = |I_{OH}| \times (V_{DD} - V_{OH}) \quad (W)$$

$$P_{DCL} = I_{OL} \times V_{OL} \quad (W)$$

The ratio of P_{DCH} and P_{DCL} is determined by the output signal duty cycle.

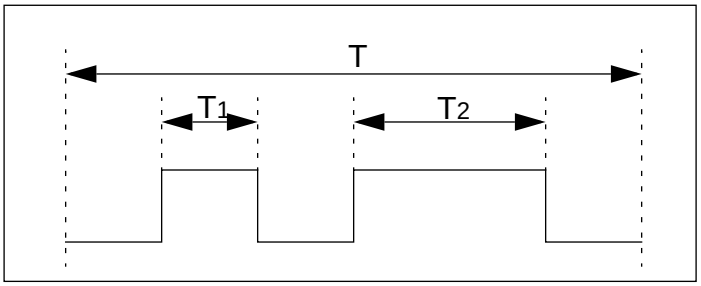


Figure 9-1 Example of the Duty Cycle

Duty H = $(T_1 + T_2) / T$
Duty L = $(T - T_1 - T_2) / T$

Because of this,

$P_{DC} = P_{DCH} + P_{DCL}$

$$= \sum_{i=1}^{K} \{(V_{DD}-V_{OHi}) \times | I_{OHi} | \times \text{Duty H}\} + \sum_{i=1}^{K} \{V_{OLi} \times I_{OLi} \times \text{Duty L}\}$$

Consequently, the power consumption Po of the output buffer is calculated by:

$$P_O = \sum (P_{AC} + P_{DC})$$

$$= \sum_{i=1}^{K} \{ f i \times C_{Li} \times (V_{DD})^2 \} + \sum_{i=1}^{K} \{(V_{DD} - V_{OHi}) \times I_{OHi} \times \text{Duty H} \}$$

$$+ \sum_{i=1}^{K} \{ V_{OLi} \times I_{OLi} \times \text{Duty L} \}$$

(3) Internal Cell Power Consumption (P_{int})

The internal cell power consumption depends on the type of device used, the cell use efficiency, the operating frequency, and the ratio of cells operating at the operating frequency. It is calculated as follows:

$$P_{int} = \sum_{i=1}^{K} \{ (Nb \times U) \times fi \times S_{pi} \times (K_{pint}) \} \text{ (W)}$$

Nb: Total number of BCs in the device type used.

U: Cell use ratio (Use 40%-50% for DLM, use 70%-88% for TLM)

fi: Operating frequency of the ith group (MHz)

S_{pi}: Percentage of cells operating at frequency fi.(Use 20% to 30%, though it depends on system.)

K_{pint}: Internal cell power coefficient (Refer to Table 9.2.)

Table 9-2 K_{pint} for 1BC in the S1L50000 Series

V_{DD} (Typ)	K_{pint}
2.5V	0.34µW/MHz

Low power cells of the low power consumption type can be used to operate with the low power consumption. With low power cells, the propagation delay time compared with normal cell is only slightly shortened, but the power consumption per gate can be decreased by a half.

The power consumption when using low power cells should be calculated as a half the Kpint of the internal cells in S1L50000 series.

Low power cells are indicated by “L” added to the end of the normal flip-flop cell name. (There is a total of 31.)

Table 9-3 Example of Low Power Cell in S1L50000 Series

Normal Cells	Low power cells
DF D-Flip Flop	**DFL** D-Flip Flop(Low power)
JKR JK-Flip Flop	**JKRL** JK-Flip Flop
LF Latch	**LFL** Latch(Low power)

*1 The scan cells except for those listed above are prepared. (There is a total of 31.)
Refer to “Gate Array S1L50000 Series MSI Cell Library” in detail.

9.2 Constraints on Power Consumption

The LSI chip heats up according to the power consumption within the LSI. The temperature of the LSI chip when it is mounted in a package can be calculated from the ambient temperature Ta, the thermal resistance(q_{j-a}) of the of the package, and the power consumption P_D.

The chip temperature (T_j) = Ta + ($P_D \times q_{j-a}$) (°C)

In normal use, the chip temperature (T_j) should be less than about 85°C.

Please reference table 9-4 for the thermal resistances of each of the various packages. Because the thermal resistances listed in Table 9-4 are thermal resistances in a situation where there is no air circulation, these values will change substantially depending on the mounting of the packages on the circuit board and depending on whether or not there is forced air cooling.

Table 9-4 Thermal Resistances of Various Packages (Without Air Circulation)

ALLOY42

PKG	PIN	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
QFP5	100	110(°C/W)	75	60	55
QFP5	128	110	75	60	55
QFP8	128	65	—	—	—
QFP8	208	45	—	—	—
QFP12	48	230	—	—	—
QFP13	64	170	—	—	—
QFP14	80	110	—	—	—
QFP15	100	115	50	45	35
QFP20	144	85	70	50	40
TQFP14	80	100	—	—	—
TQFP14	100	100	—	—	—
TQFP15	100	110	—	—	—

CFLGA (Board installation under the windless condition)

Package type	Customer's board size	Chip Size		
		3.82 mm × 3.82 mm	5.73 mm × 5.73 mm	9.55 mm × 9.55 mm
CFLGA424	75mm	44.0(°C/W)	32.9	24.6
	50mm	46.9	36.4	27.8
	30mm	61.1	50.1	42.1
CFLGA307	75mm	44.0	33.1	24.9
	50mm	47.1	37.4	28.5
	30mm	61.7	51.5	43.1
CFLGA239	75mm	44.0	33.1	25.1
	50mm	47.3	38.3	29.2
	30mm	62.2	52.9	43.9
CFLGA152	75mm	44.8	34.4	—
	50mm	48.8	39.7	—
	30mm	63.3	53.9	—
CFLGA104	75mm	45.5	35.6	—
	50mm	50.3	41.1	—
	30mm	64.3	54.9	—

Cu-L/F

PKG	PIN	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
QFP5	80	85(°C/W)	55	45	40
QFP5	100	80	55	35	30
QFP5	128	80	55	35	30
QFP8	160	45	32	25	23
QFP8	256	50	—	—	—
QFP10	304	35	20	16	—
QFP12	48	175	120	90	80
QFP13	64	130	80	55	50
QFP14	80	110	—	—	—
QFP15	100	90	—	—	—
QFP20	184	65	—	—	—
QFP21	176	55	—	—	—
QFP21	216	55	—	—	—
QFP22	208	45	35	25	23
QFP22	256	45	35	25	23
QFP23	184	40	—	—	—
QFP23	240	40	—	—	—
TQFP12	48	165	—	—	—
TQFP13	64	140	—	—	—
TQFP15	128	105	—	—	—
TQFP24	144	80	—	—	—
HQFP5	128	60	—	—	—
HQFP8	160	32	19	12	10
H2QFP8	208	34	—	—	—
H2QFP23	240	30	—	—	—
H3QFP15	128	85	—	—	—

PBGA

PKG	PIN	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
PBGA	225	72(°C/W)	46	37	—
PBGA	256	53	33	25	—
PBGA	388	45	—	—	—

Chapter 10: Pin Layout Considerations

10.1 Estimating the Number of Power Supply Pins

It is necessary to estimate the number of power supply pins required based on the power consumed by the LSI and on the number of output buffers. The output buffers use a large current when switching. This current increases with larger output buffer drive capabilities.

The number of power supply pins required by the LSI can be estimated by its relationship with the current consumed as shown below.

If the current consumed is I_{DD} (mA), then the number of power supply pins required (N_{IDD}) to supply the consumption current I_{DD} is as follows:

$$N_{IDD} \geq I_{DD} / 50 \text{ (pairs)}$$

NOTE : Insert a minimum of 2 pairs of power pins N_{IDD}.
I_{DD}: Calculate I_{DD} by dividing the power consumption calculated in Chapter 9 by the operating voltage.

See Chapter 11 regarding the estimation of the number of power pins for dual power supplies.

NOTE: When the DC load is connected to the output buffer, if the current is flowed at the steady-state, power supply pins should be added.For more infomation, contact to our sales office for tecnichal support.

10.2 Number of Simultaneous Operations and Adding Power Supplies

In the S1L50000 Series, the output drive capability is extremely large at a maximum of 6mA, and thus the noise generated by the output buffers when they are operating is also extremely large.

The power supplies need to be added, as shown in Table 10-1 to 10-2 to prevent malfunction from the noise when multiple output buffers operate at the same time.

Table 10-1 Number of additional V_{SS} Power Supplies Depending on the Simultaneous Operation of Output Buffers (V_{DD}=2.5V)

Output Drive Ability (I_{OL})	Number of Output Buffers Operating Simultaneously	Number of Additional Power Supplies		
		$C_L \leq 50pF$	$C_L \leq 100pF$	$C_L \leq 200pF$
6mA	≤8	0	1	2
	≤16	1	2	3
	≤24	1	2	4
	≤32	2	3	5

Table 10-2 Number of additional V_{DD} Power Supplies Depending on the Simultaneous Operation of Output Buffers (V_{DD}=2.5V)

Output Drive Ability (I_{OH})	Number of Output Buffers Operating Simultaneously	Number of Additional Power Supplies		
		$C_L \leq 50pF$	$C_L \leq 100pF$	$C_L \leq 200pF$
6mA	≤8	0	1	1
	≤16	1	1	2
	≤24	1	2	3
	≤32	1	2	3

10.3 Cautions and Notes Regarding the Layout of Pins

Once the package to be used has been selected, then it is time to layout the pins. Please see the specific "Pin Layout Table" regarding the number of power supply pins and useable input/output pins in the various S1L50000 Series Packages.

Once the pin layout has been established, submit to EPSON a pin assignment specification

which has been filled out with the pin layout. EPSON will layout the interconnections according to the specification submitted by the customer, so we request that the customer carefully check this specification.

The pin layout is one of the critical specifications which controls the quality of the LSI. It is especially important in avoiding malfunctions due to noise. Moreover, problems with noise are difficult to check for in simulations. So that there will be are no malfunctions with non-traceable causes in the customer's LSI, we urge the customer to carefully study the guidelines detailed in this chapter before generating the pin layout.

10.3.1 Fixed Power Supply Pins

There are some pins which can only be used for power supply, depending on the combination of each device and package in this series. Because there are some pins which must be set to V_{DD} pins and some pins which must be set to V_{SS} pins please consult with EPSON when selecting a package.

10.3.2 Cautions and Notes Regarding the Pin Layout

The pin layout influences the logical functioning and electrical characteristics of the LSI. Moreover, the pin layout may be constrained by the construction of the LSI, the structuring of the cells and the bulk, etc. Because of this, we will explain factors which must be researched when creating the pin layout, factors such as the power supply current, the input pin/output pin isolation, the critical signals, the pull-up/pull-down resistor inputs, simultaneous output, current drivers, etc.

(1) Power Supply Current (I_{DD}, I_{SS})

When it comes to the power supply current (I_{DD}, I_{SS}) there are limitations on the tolerable levels for current from the power supply through the power supply pins when in an operating state. When the tolerable levels are exceeded, the current density within the power supply interconnects within the LSI becomes too high, and the voltage generated by the current and the resistance within the interconnects increases or decreases. This may lead to malfunctioning and may have an impact on DC or AC characteristics.

In order to avoid these types of problems, it is necessary to reduce the current density and the power supply interconnect line impedance. To do this, it is necessary to estimate the power consumption during the design of the gate array, and to make sure that there are enough power supply pins so that the current through each of the power supply pins does not exceed tolerances. Moreover, the layout should be such that the power supply pins are not concentrated all in one location, but rather are spread out. See Section 10.1, "Estimating the Number of Power Supply Pins" about number of power supply pins.

However, the final power supply pin count may require the addition of power supply pins according to the above, and the power supply pin count must include additional power supply pins for the purpose of reducing noise, etc. See Section 10.2, "Number of Simultaneous Operations and Adding Power Supplies", regarding additional the number of additional power supply pins.

(2) Noise Resulting from the Operation of Output Cells

The noise resulting from the operation of the output cells can be broadly divided into two categories. To reduce this noise as many power supplies should be added as possible as the countermeasure.

a) Noise Generated in the Power Supply Lines

When many outputs switch simultaneously, there will be problems with noise generated in the power supply line. This can change the LSI input threshold levels, causing malfunctions. This power supply line noise is a result of the large current which is caused to flow in the power supply lines when output cells switch simultaneously. The power supply noise exerts an especially large impact on the interface components. Because of this, the LSI equivalent circuits can be represented as shown in Figure 10-1. The output of this circuit diagram shows that when there is a "High" to "Low" transition, the current from the output pin flows through the components within the LSI, and flows through the equivalent inductance L_2 of the LSI package, etc. At this time, the voltage in the V_{SS} power supply line within the LSI is distorted by the equivalent inductance L_2. This voltage distortion in the V_{SS} power supply line is the noise that is generated within the power supply line. The noise which is generated within the power supply lines is primarily a result of the equivalent inductance L_2, so a large amount of noise is generated when power supply currents change rapidly.

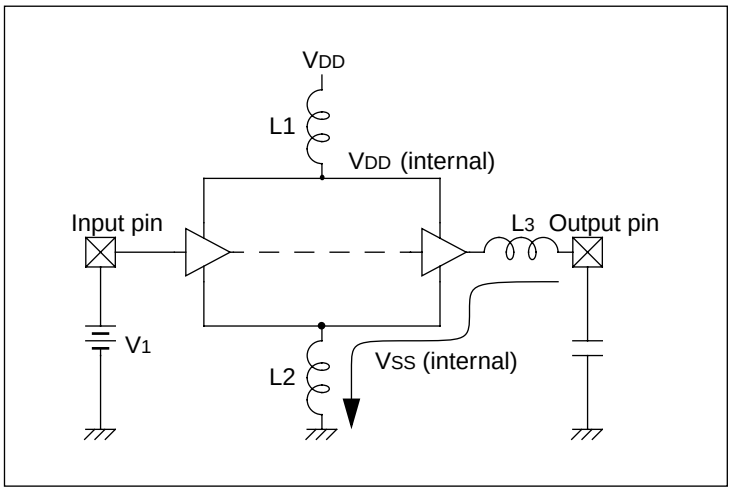


Figure 10-1 An LSI Equivalent Circuit

b) The equivalent inductance in the output pins causes noises known as "overshoot," "undershoot" and "ringing." This equivalent inductance is marked by L_3 in Figure 10-1. Because inductance has the property of storing energy, this overshoot, undershoot or ringing is the result of the output becoming either low or high. When there is a transition, the overshoot and undershoot is proportional to the size of the current to the rate of change of the current.

The most effective way to reduce overshoot and undershoot is to use output cells with relatively small drive current, and there is a tendency for the overshoot and undershoot to be reduced when there is a relatively large load capacitance. Because of this, there is a need for caution when using cells with especially large current driving capabilities.

(3) Isolating Input Pins and Output Pins

Separating the input pin group from the output pin group in the pin layout is an important technique for reducing the impact of noise.

Because input pins and bi-directional pins in the input state are especially susceptible to noise, one should avoid mixing these pins with output pins whenever possible, and the input pin group, the output pin group, and the bi-directional pin group should be separated from each other by the power supply pins (V_{DD}, V_{SS}).

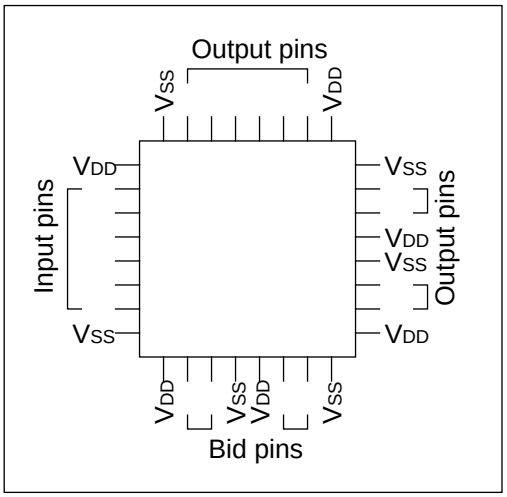


Figure 10-2 Example of Separating Input Pins and Output Pins

(4) Critical Signals

The following cautions and notes should be kept in mind when laying out the pins for critical signals such as clock input pins and high-speed output pins.

a) Pins for which it is necessary to reduce the noise, such as clock and reset pins, should be placed near the power supply pins and far from the output pins. (See Figure 10-3)

b) Oscillator circuit pins should be placed near one another, sandwiched between power supply pins (V_{DD}, V_{SS}). Moreover, they should not be placed near output pins. (See Figure 10-4.)

c) High-speed input and output pins should be placed near the center of the edge of the chip (of the package). (See Figure 10-3.)

d) When there is little margin in the customer specifications for delays between the input pins and the output pins, these input and output pins should be placed near to one another. (See Figure 10-3.)

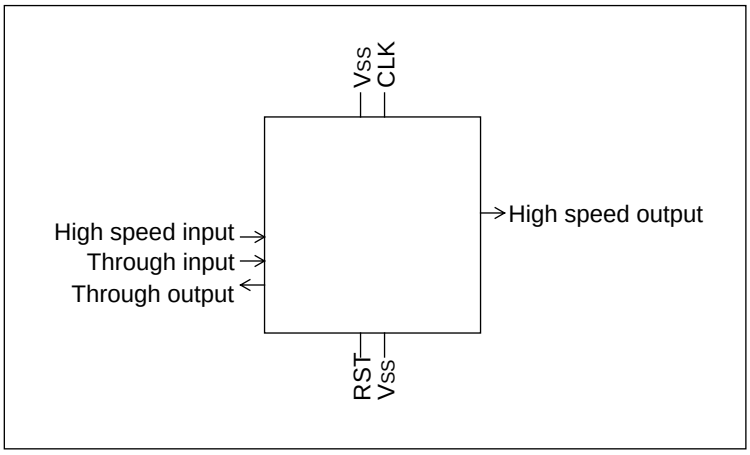


Figure 10-3 Example 1 of a Layout for Critical Signals

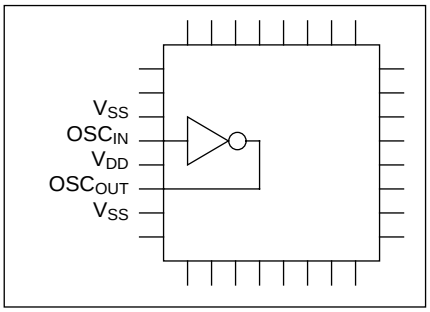


Figure 10-4 Example 2 of a Layout for Critical Signals

(5) Pull-up/Pull-down Resistor Inputs

The pull-up and pull-down resistance values are relatively large, ranging from a few dozen to a few hundred kohms. The structure of the resistors depends on the power supply voltage. Because of this, the pins are especially vulnerable to noise coming from the power supply. The following cautions should be carefully considered when creating the pin layout in order to prevent this noise from causing malfunctions.

a) Locate as far as possible from high-speed inputs (such as clock pins). (See Figure 10-5.)
b) Locate away from output pins (especially large-current output pins). (See Figure 10-6.)

Please consider the following points prior to pin layout.

- Perform pull-up and pull-down processes on the PCB itself whenever possible.
- Select resistors with low resistances whenever possible.

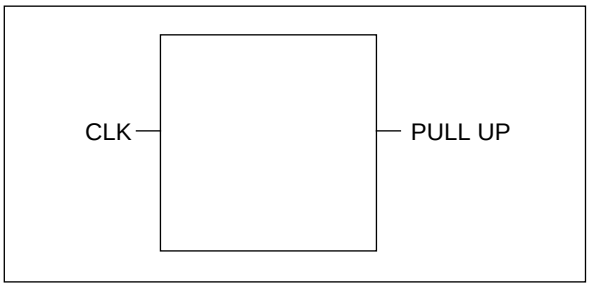


Figure 10-5 Example 1 of Placement of Pull-up and Pull-down Resistors

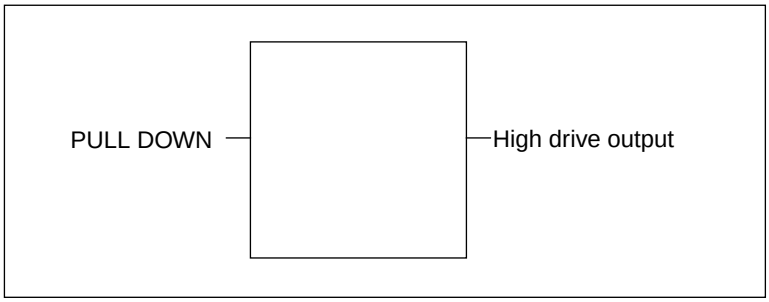


Figure 10-6 Example 2 of Placement of Pull-up and Pull-down Resistors

(6) Simultaneous Switching of Outputs

Noise is generated when multiple output pins change at the same time, which may cause malfunctioning of the LSI. In order to reduce the risk of malfunction due to noise when multiple output pins change at the same time, a power supply pin should be added to the group of output pins which are changing simultaneously. See section 10.2 regarding the number of power supply pins which must be added and the method for laying out these power supply pins. In order to reduce this noise, one may alternatively add a cell to delay the previous stage of these output cell groups, thereby reducing the amount of simultaneous changes of the output cells, thereby reducing noise as well. (See Figure 10-8.)

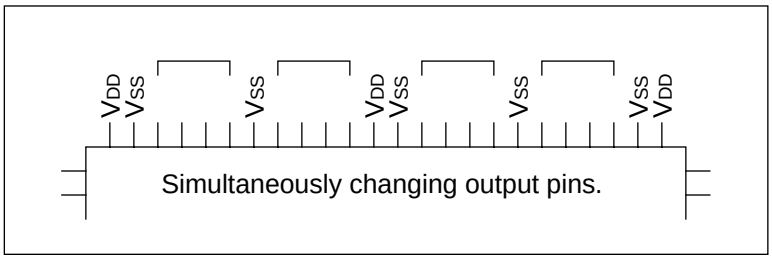


Figure 10-7 Example of Adding Power Supply Pins

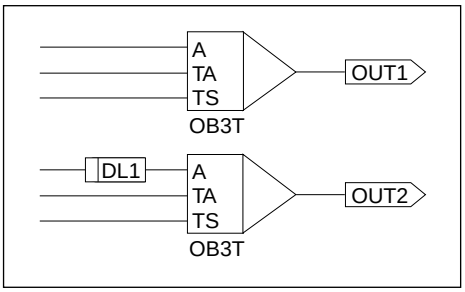


Figure 10-8 Example of Adding Delay Cells

(7) Large Current Drivers

When outputs are used which drive large currents (I_{OL} = 12 mA, 24mA, PCI/HV_{DD} = 3.3V), pin layout should be performed following the constraints below:

a) Constraints on Strengthening the Power Supplies
Power supply pins should be located near the large-current driver pins to minimize switching niose. (See Figure 10-9.)

b) Low-Noise Pre-drivers
Low-noise output buffers have been prepared in order to reduce the noise generated by the operation of output cells with large current drivers. See Chapter 4 regarding recommended.

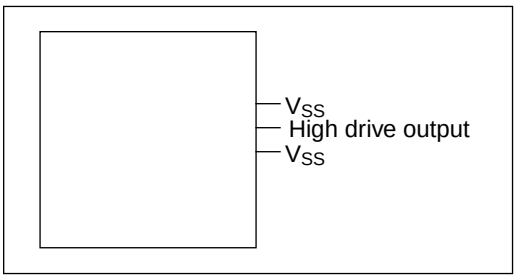


Figure 10-9 Example of Strengthening Power Supplies

(8) Other Cautions and Notes

The relationship between the package pins and the LSI pads is already established by the combination of each series device type and package type. Because of this, there may be constraints on the use of pins because of the package, and constraints on the pin layout due to the I/O cell types.

Notes and cautions regarding these restraints are described below; these should be kept in mind when determining the pin layouts.

a) NC Pins (non-connection)
A pin might be unavailable for use when the number of pads on the LSI is less than the number of pins on the package, or when the LSI pad cannot be connected to one of the package pins.

Mark these with a double asterisk (**) on the pin layout table.

b) Tab Hanger Pins
Tab hanger pins are package pins which are connected directly the LSI substrate. For reasons discussed above, these pins are at a V_{SS} (GND) level even if they are not externally connected to the power supply.

Normally these pins should be left open on the circuit board.

These pins should be marked with double pound signs (“##”) on the pin layout table form.

10.3.3 Examples of Recommended Pin Connections

The pin layout is a critical point in ensuring that the LSI operates correctly. Determine pin layouts after referencing the example pin layout (Figure 10-10) which takes into consideration the entire content explained in this chapter.

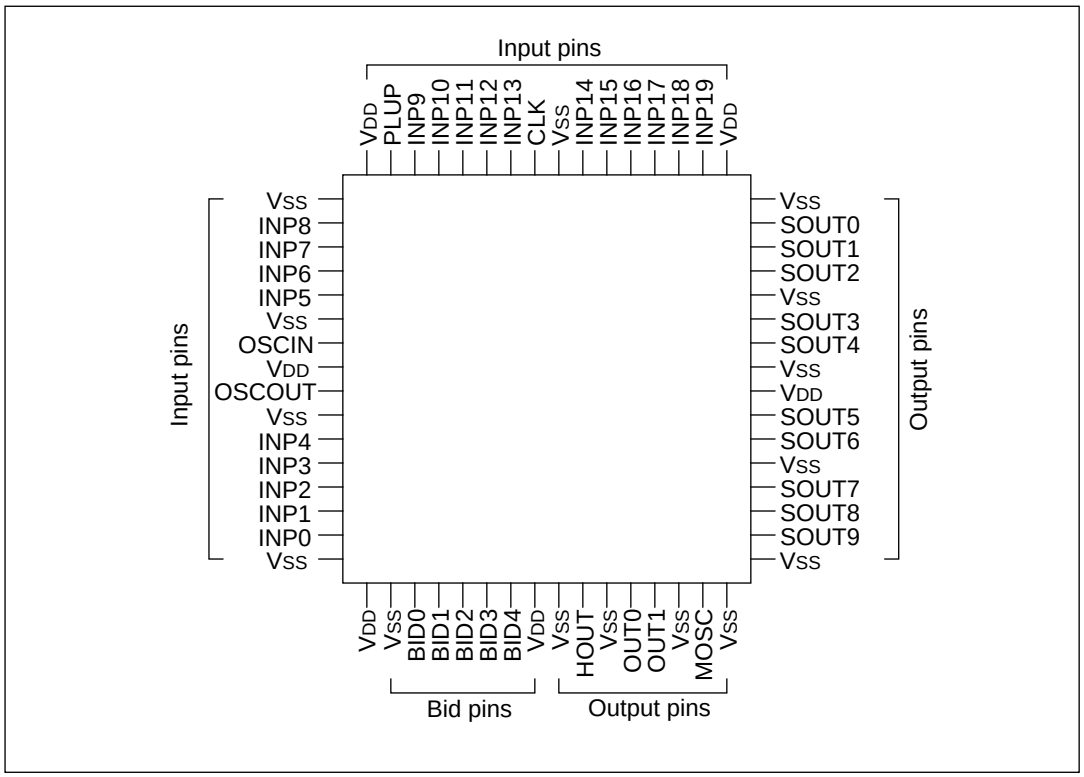


Figure 10-10 Example of Recommended Pin Layout

Input pins are located on the upper and left hand edges of the package, output pins which change simultaneously are located on the right hand side of the package, and bi-directional pins and other output pins are located on the bottom edge of the package.

Table 10-3 Pin Layout Example

Location	Pin Name	Explanation of Pin Name	Detailed Explanation of the Position of Each Pin
Upper Edge	PULP CLK	Input pins with pull-up Input pins for the clock	Located where the impact of noise is the least. Located near the center of the package, and near power supply pins.
Left Edge	OSCIN, OSCOUT INP0 to19	Oscillator pins Input pins	Located near the center of the package, and near power supply pins. Located with power supply pins, away from other pins.
Right-hand Edge	SOUT0 to 9	Simultaneously changing output pins	Located near power supply pins and separated from other pins with additional power supply pins.
Bottom Edge	BID0 to 4 MOSC HOUT OUT01	Bi-directional pins Oscillator monitor output pins High-drive output pins Output pins	Located near power supply pins and separated from other pins. Located separated from oscillator pins and near power supply pins. Located near power supply pins. Located near power supply pins and separated from other pins.
All Edges	V_{DD} V_{SS}	V_{DD} power supply pins V_{SS} (GND) power supply pins	

Chapter 11: Dual Power Supplies Guidelines

By using dual power supplies (3.3V/2.5V systems) the S1L50000 Series is able to interface with either 3.3V or 2.5V system signal for each I/O cell. The internal cell region operates on only the single 2.5V system power supply.

11.1 The Method of Adapting to Dual Power Supplies

The S1L50000 Series is of capable of interfacing with signals of a voltage which is different than the internal operating voltage. There are two methods by which to interface with systems of different voltages.

- The Single Power Supply Method

  With a single power supply, it is possible to input a signals with operating voltage that are higher than the supply voltage, by using an Nch open-drain buffer. However, it is not possible to output signals with operating voltages that are higher than the supply voltage, unless an Nch open-drain buffer and an external pull-up resister are combined.

- The Dual Power Supply Method

  It is possible to input a signal of a higher voltage than the internal operating voltage through the use of special dual power supply compatible input butters. Also, the use of output buffers with level shifters makes it possible to output signals of voltages higher than internal operating voltage.

11.2 Power Supplies for Dual Power Operation

When two power supplies are applied, use the unique power supply identifiers, HV_{DD} and LV_{DD}. HV_{DD} is used to supply power for HV_{DD}' I/O cells. LV_{DD} is used to supply power for LV_{DD}' I/O cells and all internal cells. The power supply voltages must always fulfill the following inequality:

$HV_{DD} \geq LV_{DD}$

Caution is necessary because operation cannot be assured if HV_{DD} is less than LV_{DD}. The following two conditions are recommended operating conditions.

- HV_{DD} = 3.3V, LV_{DD} = 2.5V

Below is an example of use in a situation where a dual power supply is supplied to the S1L50000 Series.

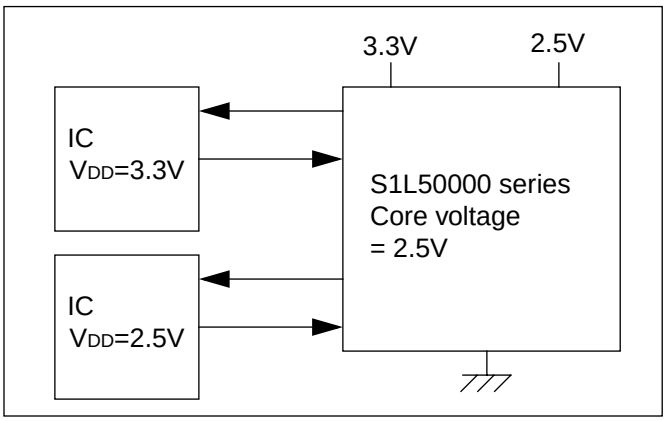


Figure 11-1 Example of Use Where a Dual Power Supply is Supplied to the S1L50000 Series

11.3 Turning Dual Power On and Off

For dual-power supply chips, the following power-on/off sequences are recommended.

When powering on: LV_{DD} (internal) → HV_{DD} (I/O unit) → signals

When powering off: Signals → HV_{DD} (I/O unit) → LV_{DD} (internal)

Take care not to leave HV_{DD} turned on while LV_{DD} is off, as this condition adversely affects the chip's reliability.

When HV_{DD} is turned back on from the off state, be sure to initialize the internal circuits after power-on. This is because the circuit status cannot be guaranteed due to noise on the power supply, etc. that develops at power-on.

11.4 I/O Buffers Compatible with Dual Power Supplies

When a dual power supply is used, dual power supply-compatibility I/O buffers should be used as well. Care must be taken so that I/O buffers for single power supply are not used. Because of this, I/O buffers for single power supplies and I/O buffers for dual power supplies cannot be mixed. However, buffers for testing (ITST1) are buffers for both dual power supplies and signal power supplies.

11.4.1 I/O Buffers for the LV_{DD} System

LV_{DD} system I/O buffers include input buffers which input 2.5V signals, output buffers which output 2.5V amplitude signals, and bi-directional buffers which can input 2.5V signals and which can output 2.5V amplitude signals.

When HV_{DD} system signals are input into LV_{DD} system input buffers, a very large current flows through the guard diode within the LV_{DD} system buffers, damaging the quality of the buffers; thus voltages of more than the LV_{DD} voltage should not be applied.

11.4.1.1 Input Buffers for the LV_{DD} System

The input buffer is comprised of only input cells. The LV_{DD} system input signals include those shown in Table 11-1.

Table 11-1 LV_{DD} System Input Buffers

(LV_{DD} = 2.5V)

Cell Name	Input Level	Function	Pull-up/Pull-down Resistors
LIBC	CMOS	Buffer	None
LIBCP✻	CMOS	Buffer	Pull-up Resistor (75kΩ, 150kΩ)
LIBCD✻	CMOS	Buffer	Pull-down Resistor (75kΩ, 150kΩ)
LIBH	CMOS Schmitt	Buffer	None
LIBHP✻	CMOS Schmitt	Buffer	Pull-up Resistor (75kΩ, 150kΩ)
LIBHD✻	CMOS Schmitt	Buffer	Pull-down Resistor (75kΩ, 150kΩ)

NOTE : When ✻ value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:75kΩ, 2:150kΩ respectively.

Table 11-2 LV_{DD} Input Level Shifters

(LV_{DD} = 2.5V)

Cell Name	Input Level	Function	Pull-up/Pull-down Resistors
LIDC	CMOS	Buffer	None
LIDCD✻	CMOS	Buffer	Pull-down Resistor (75kΩ, 150kΩ)
LIDH	CMOS Schmitt	Buffer	None
LIDHD✻	CMOS Schmitt	Buffer	Pull-down Resistor (75kΩ, 150kΩ)

NOTE : When ✻ value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:75kΩ, 2:150kΩ respectively.

11.4.1.2 Output Buffers for the LV_{DD} System

Use a combination of internal basic cells and output cells when structuring the LV_{DD} system output buffers. See Table 11-3 to Table 11-4 on the next page, regarding the combinations.

Table 11-3 LV_{DD} System Output Buffers

(LV_{DD} = 2.5V)

Function	I_{OL}* / I_{OH} **	Cell Name ***
Normal output	0.1mA / -0.1mA 0.5mA / -0.5mA 1mA / -1mA 3mA / -3mA 6mA / -6mA	LOBST LOBMT LOB1T LOB2T LOB3T
Normal output for high speed	6mA / -6mA	LOB3AT
Normal output for low noise	6mA / -6mA	LOB3BT
3-state output	0.1mA / -0.1mA 0.5mA / -0.5mA 1mA / -1mA 3mA / -3mA 6mA / -6mA	LTBST LTBMT LTB1T LTB2T LTB3T
3-state output for high speed	6mA / -6mA	LTB3AT
3-state output for low noise	6mA / -6mA	LTB3BT
3-state output for (Bus hold circuit)	0.5mA / -0.5mA 1mA / -1mA 3mA / -3mA 6mA / -6mA	LTBMHT LTB1HT LTB2HT LTB3HT
3-state output for high speed (Bus hold circuit)	6mA / -6mA	LTB3AHT
3-state output for low noise (Bus hold circuit)	6mA / -6mA	LTB3BHT

NOTES) * : V_{OL} = 0.4V (LV_{DD} = 2.5V)
** : V_{OH} = LV_{DD} - 0.4V (LV_{DD} = 2.5V)
*** : Along with the structuring method shown in Table 11-3, the output buffer structure may include structures which have no test pins. Those customers wishing to use a structure without test pins should direct their inquiries to EPSON.

Table 11-4 N Channel Open Drain Output Buffers

(LV_{DD} = 2.5V)

Function	I_{OL}**	Cell Name**
Normal output	1mA 3mA 6mA	LOD1T LOD2T LOD3T

NOTES) * : V_{OL} = 0.4V (LV_{DD} = 2.5V)
** : Along with the structuring method shown in Table 11-4, the N channel open drain output buffer structure may include structures which have no test pins. Those customers wishing to use a structure without test pins should direct their inquiries to EPSON.

11.4.1.3 Bi-directional Buffers for the LV_{DD} System

See Table 11-5 to Table 11-6 regarding these combinations.

Table 11-5 LV_{DD} System Bi-directional Buffers

(LV_{DD} = 2.5V)

Input Level	Function	I_{OL}* / I_{OH}**	Cell Name***
CMOS	Bi-directional output	0.1mA / -0.1mA 0.5mA / -0.5mA 1mA / -1mA 3mA / -3mA 6mA / -6mA	LBCST LBCMT LBC1T LBC2T LBC3T
	Bi-directional output for high speed	6mA / -6mA	LBC3AT
	Bi-directional output for low noise	6mA / -6mA	LBC3BT
CMOS Schmitt	Bi-directional for low noise output	0.1mA / -0.1mA 0.5mA / -0.5mA 1mA / -1mA 3mA / -3mA 6mA / -6mA	LBHST LBHMT LBH1T LBH2T LBH3T
	Bi-directional output for high speed	6mA / -6mA	LBH3AT
	Bi-directional output for low noise	6mA / -6mA	LBH3BT
CMOS	Bi-directional output (Bus hold circuit)	0.5mA / -0.5mA 1mA / -1mA 3mA / -3mA 6mA / -6mA	LBCMHT LBC1HT LBC2HT LBC3HT
	Bi-directional output for high speed (Bus hold circuit)	6mA / -6mA	LBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	6mA / -6mA	LBC3BHT
CMOS Schmitt	Bi-directional output (Bus hold circuit)	0.5mA / -0.5mA 1mA / -1mA 3mA / -3mA 6mA / -6mA	LBHMHT LBH1HT LBH2HT LBH3HT
	Bi-directional output for high speed (Bus hold circuit)	6mA / -6mA	LBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	6mA / -6mA	LBH3BHT

NOTES) * : V_{OL} = 0.4V (LV_{DD} = 2.5V)
** : V_{OH} = LV_{DD} - 0.4V (LV_{DD} = 2.5V)
*** : Along with the structuring method shown in Table 11-5, the bi-directional buffer may be structured with pull-up or pull-down resistors without test pins. Those customers wishing to use a structure without test pins should direc their inquiries to EPSON.

Table 11-6 LV_{DD} System N-Channel Open Drain Bi-directional Buffers

(LV_{DD} = 2.5V)

Input Level	Function	I_{OL}*	Cell Name**
CMOS	Bi-directional output	1mA 3mA 6mA	LBDC1T LBDC2T LBDC3T
CMOS Schmitt	Bi-directional output	1mA 3mA 6mA	LBDH1T LBDH2T LBDH3T

NOTES) * : V_{OL} = 0.4V (LV_{DD} = 2.5V)

** : Along with the structuring method shown in Table 11-6, the N channel open drain bi=directional buffer may be strucutured with pull-down resistors without test pins. Those customers wishing to use a structure without test pins should direct their inquiries to EPSON.

11.4.2 I/O Buffers for the HV_{DD} System

The HV_{DD} system I/O cells include input cells which input 3.3V signals, output cells which output 3.3V amplitude signals, and bi-directional cells which input 3.3V signals and output 3.3V amplitude signals.

11.4.2.1 Input Buffers for the HV_{DD} System

Inputs are structured from input cells alone. The HV_{DD} input buffers are comprised of the HV_{DD} system circuits for the initial-stage input, and the next-stage is comprised of LV_{DD} system circuits. The HV_{DD} system signals are converted to LV_{DD} system signals after which these signals are supplied to the MSI cells (internal cell region). The HV_{DD} system input buffers are as shown in Table 11-7 to Table 11-8.

Table 11-7 HV_{DD} System Input Buffers

(HV_{DD} = 3.3V)

Cell Name	Input Level	Function	Pull-up/Pull-down Resistors
HIBC HIBCP✻ HIBCD✻	LVTTL LVTTL LVTTL	Buffer Buffer Buffer	None Pull-up Resistor (100kΩ, 200kΩ) Pull-down Resistor (100kΩ, 200kΩ)
HIBH HIBHP✻ HIBHD✻	LVTTL Schmitt LVTTL Schmitt LVTTL Schmitt	Buffer Buffer Buffer	None Pull-up Resistor (100kΩ, 200kΩ) Pull-down Resistor (100kΩ, 200kΩ)
HIBPB HIBPBP✻ HIBPBD✻	PCI-3V PCI-3V PCI-3V	Buffer Buffer Buffer	None Pull-up Resistor (100kΩ, 200kΩ) Pull-down Resistor (100kΩ, 200kΩ)

NOTE : When ✻ value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:100kΩ, 2:200kΩ respectively.

Table 11-8 HV_{DD} Input Level Shifters

(HV_{DD} = 3.3V)

Cell Name	Input Level	Function	Pull-up/Pull-down Resistors
HIDC HIDCD✻	LVTTL LVTTL	Buffer Buffer	None Pull-down Resistor (100kΩ, 200kΩ)
HIDH HIDHD✻	LVTTL Schmitt LVTTL Schmitt	Buffer Buffer	None Pull-down Resistor (100kΩ, 200kΩ)

NOTE : When ✻ value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:100kΩ, 2:200kΩ respectively.

11.4.2.2 Output Buffers for the HV_{DD} System

See Table 11-9 to Table 11-10 regarding these combinations.

Table 11-9 HV_{DD} System Output Buffers

(HV_{DD} = 3.3V)

Function	I_{OL}* / I_{OH}**	Cell Name***
Normal output	0.1mA / -0.1mA 1mA / -1mA 2mA / -2mA 6mA / -6mA 12mA / -12mA	HOBST HOBMT HOB1T HOB2T HOB3T
Output for PCI	PCI-3V	HOBPBT
Normal output for high speed	12mA / -12mA	HOB3AT
Normal output for low noise	12mA / -12mA	HOB3BT
3-state output	0.1mA / -0.1mA 1mA / -1mA 2mA / -2mA 6mA / -6mA 12mA / -12mA	HTBST HTBMT HTB1T HTB2T HTB3T
Output for PCI	PCI-3V	HTBPBT
3-state output for high speed	12mA / -12mA	HTB3AT
3-state output for low noise	12mA / -12mA	HTB3BT
3-state output (Bus hold circuit)	1mA / -1mA 2mA / -2mA 6mA / -6mA 12mA / -12mA	HTBMHT HTB1HT HTB2HT HTB3HT
3-state output for high speed (Bus hold circuit)	12mA / -12mA	HTB3AHT
3-state output for low noise (Bus hold circuit)	12mA / -12mA	HTB3BHT

NOTES) * : V_{OL} = 0.4V (HV_{DD} = 3.3V)
** : V_{OH} =HV_{DD} - 0.4V (HV_{DD} = 3.3V)
*** : The output buffer can create the configuration without test pins, except as shown in Table 11-9. If these output buffers are required, contact the sales division of EPSON.

Table 11-10 HV_{DD} System N-Channel Open Drain Output Buffers

(HV_{DD} = 3.3V)

Function	I_{OL}*	Cell Name**
Nomal output	2mA 6mA 12mA	HOD1T HOD2T HOD3T

NOTES) * : V_{OL} = 0.4V (HV_{DD} = 3.3V)
** : The N-channel open drain output buffer can create the configuration without test pins, except as shown in Table 11-10. If these output buffers are required, contact the sales division of EPSON.

11.4.2.3 Bi-directional Buffers for the HV_{DD} System

The HV_{DD} system input buffers are as shown in Table 11-11 to Table 11-12.

Table 11-11 HV_{DD} Systerm Bi-directional Buffers

(HV_{DD} = 3.3V)

Input Level	Function	I_{OL}* / I_{OH}**	Cell Name***
LVTTL	Bi-directional output	0.1mA / -0.1mA 1mA / -1mA 2mA / -2mA 6mA / -6mA 12mA / -12mA	HBCST HBCMT HBC1T HBC2T HBC3T
	Bi-directional output for high speed	12mA / -12mA	HBC3AT
	Bi-directional output for low noise	12mA / -12mA	HBC3BT
PCI	Bi-directional output for PCI	PCI-3V	HBPBT
LVTTL Schmitt	Bi-directional output	0.1mA / -0.1mA 1mA / -1mA 2mA / -2mA 6mA / -6mA 12mA / -12mA	HBHST HBHMT HBH1T HBH2T HBH3T
	Bi-directional output for high speed	12mA / -12mA	HBH3AT
	Bi-directional output for low noise	12mA / -12mA	HBH3BT
LVTTL	Bi-directional output (Bus hold circuit)	1mA / -1mA 2mA / -2mA 6mA / -6mA 12mA / -12mA	HBCMHT HBC1HT HBC2HT HBC3HT
	Bi-directional output for high speed (Bus hold circuit)	12mA / -12mA	HBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	12mA / -12mA	HBC3BHT
LVTTL Schmitt	Bi-directional output (Bus hold circuit)	1mA / -1mA 2mA / -2mA 6mA / -6mA 12mA / -12mA	HBHMHT HBH1HT HBH2HT HBH3HT
	Bi-directional output for high speed (Bus hold circuit)	12mA / -12mA	HBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	12mA / -12mA	HBH3BHT

NOTES) * : V_{OL} = 0.4V (HV_{DD} = 3.3V)

** : V_{OH} =HV_{DD} - 0.4V (HV_{DD} = 3.3V)

*** : The configurations of the bi-directional buffer can create other patterns as shown in Tqable 11-11, when there are pull-up or pull-down connected to the bi-directional buffer, and there are no test pins. If a bi-directional buffer is required without test pins, contact the sales division of EPSON.

Table 11-12 HV_{DD} System N-Channel Open Drain Bi-directional Buffers

(HV_{DD} = 3.3V)

Input Level	Function	I_{OL}*	Cell Name**
LVTTL	Bi-directional output	2mA 6mA 12mA	HBDC1T HBDC2T HBDC3T
LVTTL Schmitt	Bi-directional output	2mA 6mA 12mA	HBDH1T HBDH2T HBDH3T

NOTES: * V_{OL} = 0.4V (HV_{DD} = 3.3V)

** The configurations of the N-channel open drain bi-directional buffer can create other patterns as shown in Table 11-12, when there are pull-up or pull-down connected to the bi-directional buffer, and there are no test pins. If a bi-directional buffer is required without test pins, contact the sales division of EPSON.

11.5 Delay Calculation for Dual Power Supplies

When dual power supplies are used, there will be cells wherein the delay coefficient variability M of Table 7-1 (Chapter 7) cannot be used in situations such as shown below:

Cells where the "Delay Coefficient Variability M" of Table 7.1 cannot be used

- HV_{DD} system input buffers (such as HIBC, HIBH, etc.)
- HV_{DD} system bi-directional buffers (such as HBC∗T, HBH∗T, etc.)

T_0 and K Min., Typ., and Max. values for these cells are listed in the "Gate Array S1L50000 Series MSI Cell Library". Calculate the delay times using these values of T_0 and K.

(1) The Delay Time (Typ. value) Calculation

The method for calculating the delay time (Typ. value) for dual power supplies is the same as the method for calculating the delay time (Typ. value) for a single power supply. Because a high-precision delay calculation environment is provided, one must note that the calculated delay times do not match those delay times which are calculated by using the values listed in the "Gate Array S1L50000 Series MSI Cell Library". For input and output buffers, use the values of T_0 (Typ.) and K (Typ.) corresponding to the appropriate operating voltage of the HV_{DD} and the LV_{DD} system buffers.

When calculating the delay time (Typ. value) of the internal cells, use the T_0 (Typ.) and K (Typ.) values for the power supply voltage of the LV_{DD} system.

(2) Delay Time (Min., Max. values) Calculation and Variability in the Delay Coefficient

In the case of single power supplies, the Typ. value is multiplied by the delay variability coefficient M (Table 7.1) to obtain the Max. and Min. values of the delay times. In contrast, when dual power supplies are used, the delay variability coefficients for the LV_{DD} system and the HV_{DD} system are different, so the Min. values and Max. values of the delay time for each cell are calculated separately. The Min. value and Max. value of the delay time for a circuit is obtained by adding the delay times calculated for each cell.

However, when dual power supplies are used, the delay coefficient variability M listed in Table 7.1 cannot be used for buffers such as HIBC, HBC∗T, etc. For these type of buffers, the Min. value of the delay time, for example, would be calculated by using the Min. values of T_0 and K in the cell library. Also, when calculating the Max. value for the delay time, the Max. values of T_0 and K from the cell library are used in the calculation.

11.6 Cautions and Notes Regarding Power Consumption Calculations When Using Dual Power Supplies

The power consumption calculations compatible with dual power supplies require the calculation of power consumption to be split into HV_{DD} and LV_{DD} systems.

(1) Input Buffer Power Consumption (P_i [HV_{DD}] and P_i [LV_{DD}])

The formula is not different from the formula for single power supply. If we define the power consumption for the HV_{DD} system as P_i (HV_{DD}) and the power consumption for the LV_{DD} system as P_i (LV_{DD}) then:

$$P_i\ (HV_{DD}) = \sum_{i=1}^{K} (K_{pi} \times f_i) \quad (W)$$

$$P_i\ (LV_{DD}) = \sum_{i=1}^{K} (K_{pi} \times f_i) \quad (W)$$

The sum of P_i (HV_{DD}) and P_i (LV_{DD}) from the formulas above is the power consumption of the input buffer. For input buffer in HV_{DD} systems, replace the 3.3V K_{pi} when performing calculations with a 2.5V K_{pi} in the case of the LV_{DD} system. See Table 11.13 for K_{pi} values.

Table 11-13 Kpi of Input Buffers in the S1L50000 Series

V_{DD} (Typ.)	Kpi
HV_{DD} = 3.3V	6.2µW/MHz
LV_{DD} = 2.5V	3.6µW/MHz

(2) Output Buffer Power Consumption (Po (HV_{DD}) and Po (LV_{DD}))

The formula is not different from the formula for single power supply. If we define the power consumption for the HV_{DD} system as Po (HV_{DD}) and the power consumption for the LV_{DD} system as Po (LV_{DD}) then

$$Po\ (HV_{DD}) = \sum (P_{AC} + P_{DC})$$

$$= \sum_{i=1}^{K} \{fi \times C_{Li} \times (HV_{DD})^2\} + \sum_{i=1}^{K} \{(HV_{DD} - V_{OH\,i}) \times |I_{OH\,i}| \times \text{Duty H}\}$$

$$+ \sum_{i=1}^{K} \{V_{OL\,i} \times I_{OL\,i} \times \text{Duty L}\}$$

$$Po\ (LV_{DD}) = \Sigma\ (P_{AC} + P_{DC})$$

$$= \sum_{i=1}^{K} \{fi \times C_{Li} \times (LV_{DD})^2\} + \sum_{i=1}^{K} \{(LV_{DD} - V_{OH\,i}) \times |I_{OH\,i}| \times Duty\ H\}$$

$$+ \sum_{i=1}^{K} \{V_{OL\,i} \times I_{OL\,i} \times Duty\ L\}$$

The output buffer power consumption is the sum of Po (HV_{DD}) and Po (LV_{DD}) of the formulas above. When performing these calculations, be aware that the V_{DD} values in the HV_{DD} and LV_{DD} systems are different.

Note: Be aware that the value for V_{OHi} is different in the HV_{DD} system than it is in the LV_{DD} system.

(3) Internal Cell Power Consumption (P_{int})

This formula is not different from the formula for the single power supply.

$$P_{int} = \sum_{i=1}^{K} \{(Nb \times U) \times f_i \times S_{pi} \times K_{pint}\} \quad (W)$$

The power consumption in the internal cells is calculated using the above formula.Replace K_{pit} with the appropriate LV_{DD} K_{pint} when performing the calculation. See Table 9.2 of Chapter 9 for the K_{pit} values. Using the above, the P_{total} power consumpition is calculatption as follows.

P_{total} = Pi (HV_{DD}) + Pi (LV_{DD}) + Po (HV_{DD}) + Po (LV_{DD}) + P_{int}

11.7 Estimating the Number of Power Supply Pins When Using Dual Power Supplies

Even when using a dual power supply system, the magnitude of the allowable current per pair of power supplies (for both the HV_{DD} and the LV_{DD} system) is the same as for the single power supply case. Calculate the required number of power supplies separately for the HV_{DD} system and the LV_{DD} system.

* Assuming the current consumption of the HV_{DD} system to be I_{DD} (HV_{DD}) [mA], the number of pairs of power supply pins N_{IDD} (HV_{DD}) for the current consumed I_{DD} (HV_{DD}) is given by:

  N_{IDD} (HV_{DD}) ≥ I_{DD} (HV_{DD}) / 50 (pairs) : possible to supply 50mA per one pair

* Assuming the current consumption of the LV_{DD} system to be I_{DD} (LV_{DD}) [mA], the number of pairs of power supply pins N_{IDD} (LV_{DD}) for the current consumed IDD (LV_{DD}) is given by:

  N_{IDD} (LV_{DD}) ≥ I_{DD} (LV_{DD}) / 50 (pairs) : possible to supply 50mA per one pair

In this case, there must be a minimum of two pairs of power supply pins for the HV_{DD} system and a minimum of two pairs for the LV_{DD} system.

NOTE: When adding power supplies in response to the simultaneous switching of outputs, distinctions should be drawn between the HV_{DD} system output buffers and the LV_{DD} system output buffers. Reference Chapter 10 (Table 10-1 to 10-2) when adding power supply systems for 2.5V system to each. Also, Reference (Table 11-4 and 11-15) when adding power supply systems for 3.3V system to each.

Table 11-14 Number of Additional V_{SS} Power Supplies Depending on the Simultaneous Operation of Output Buffers

(HV_{DD} = 3.3V)

Output Drive Ability (I_{OL})	Number of Output Buffers Operating Simultaneously	Number of Additional Power Supplies		
		CL≤50pF	CL≤100pF	CL≤200pF
6mA	≤8	0	1	2
	≤16	1	2	3
	≤24	1	2	4
	≤32	2	3	5
12mA	≤8	1	2	2
	≤16	2	2	3
	≤24	2	3	5
	≤32	2	4	8
PCI	≤8	1	2	3
	≤16	2	3	4
	≤24	3	4	5
	≤32	4	5	10

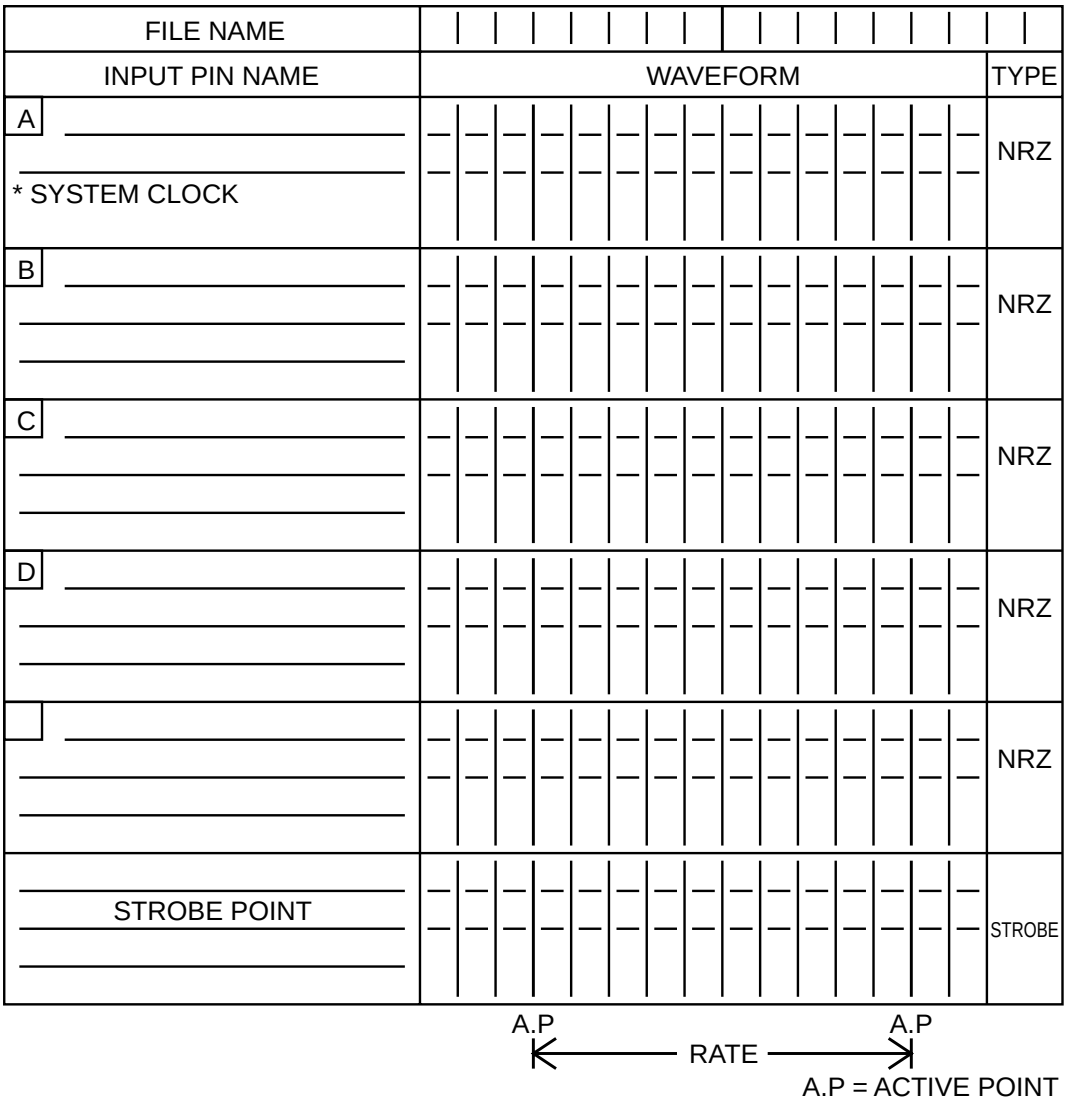
Table 11-15 Number of Additional HV_{DD} Power Supplies Depending on the Simultaneous Operation of Output Buffers

(HV_{DD} = 3.3V)

Output Drive Ability (I_{OH})	Number of Output Buffers Operating Simultaneously	Number of Additional Power Supplies		
		CL≤50pF	CL≤100pF	CL≤200pF
6mA	≤8	0	1	1
	≤16	1	1	2
	≤24	1	2	3
	≤32	1	2	3
12mA & PCI	≤8	1	2	2
	≤16	2	2	3
	≤24	2	3	3
	≤32	3	3	6

Simulation Input Timing Waveforms

*The about timing might change with the limitation of the measuring system including a tester.



RATE (ns)	•	(SYSTEM CLOCK)
	DELAY (ns)	COMMENT
A	•	Duty
B	•	
C	•	
D	•	
E	•	

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

- HEADQUARTERS -
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

- SALES OFFICES -

West
1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300 Fax: +1-310-955-5400

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630 Fax: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 Fax: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020 Fax: +1-770-777-2637

- DESIGN SUPPORT CENTERS -

San Jose Asic Design Center
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH

- HEADQUARTERS -
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

DÜSSELDORF BRANCH OFFICE

Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)2171-5045-0 Fax: +49-(0)2171-5045-10

UK & IRELAND BRANCH OFFICE

Unit 2.4, Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

FRENCH BRANCH OFFICE

1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

BARCELONA BRANCH OFFICE

Barcelona Design Center

Edificio Testa
Adva. Alcalde Barrils num. 64-68
E-08190 Sant Cugat del Vallès, SPAIN
Phone: +34-93-544-2490 Fax: +34-93-544-2491

Scotland Design Center
Integration House, The Alba Campus
Livingston West Lothian, EH54 7EG, SCOTLAND
Phone: +44-1506-605040 Fax: +44-1506-605041

ASIA

EPSON (CHINA) CO., LTD.

23F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: 64106655 Fax: 64107319

SHANGHAI BRANCH

7F, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: 86-21-5423-5577 Fax: 86-21-5423-4677

EPSON HONG KONG LTD.

20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.

14F, No. 7, Song Ren Road,
Taipei 110
Phone: 02-8786-6688 Fax: 02-8786-6660

HSINCHU OFFICE

13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300
Phone: 03-573-9900 Fax: 03-573-9169

EPSON SINGAPORE PTE., LTD.

No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-6337-7911 Fax: +65-6334-2716

SEIKO EPSON CORPORATION KOREA OFFICE

50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

GUMI OFFICE

6F, Good Morning Securities Bldg.
56 Songjeong-Dong, Gumi-City, 730-090, KOREA
Phone: 054-454-6027 Fax: 054-454-6093

SEIKO EPSON CORPORATION ELECTRONIC DEVICES MARKETING DIVISION

IC Marketing Department

IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5117

S1L50000 Series 2.5 Voltage Library
DESIGN GUIDE

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

■ **EPSON Electronic Devices Website**

http://www.epsondevice.com

Document code: 404507603
First issue April,1998 Ⓓ
Printed June, 2002 in Japan ©A