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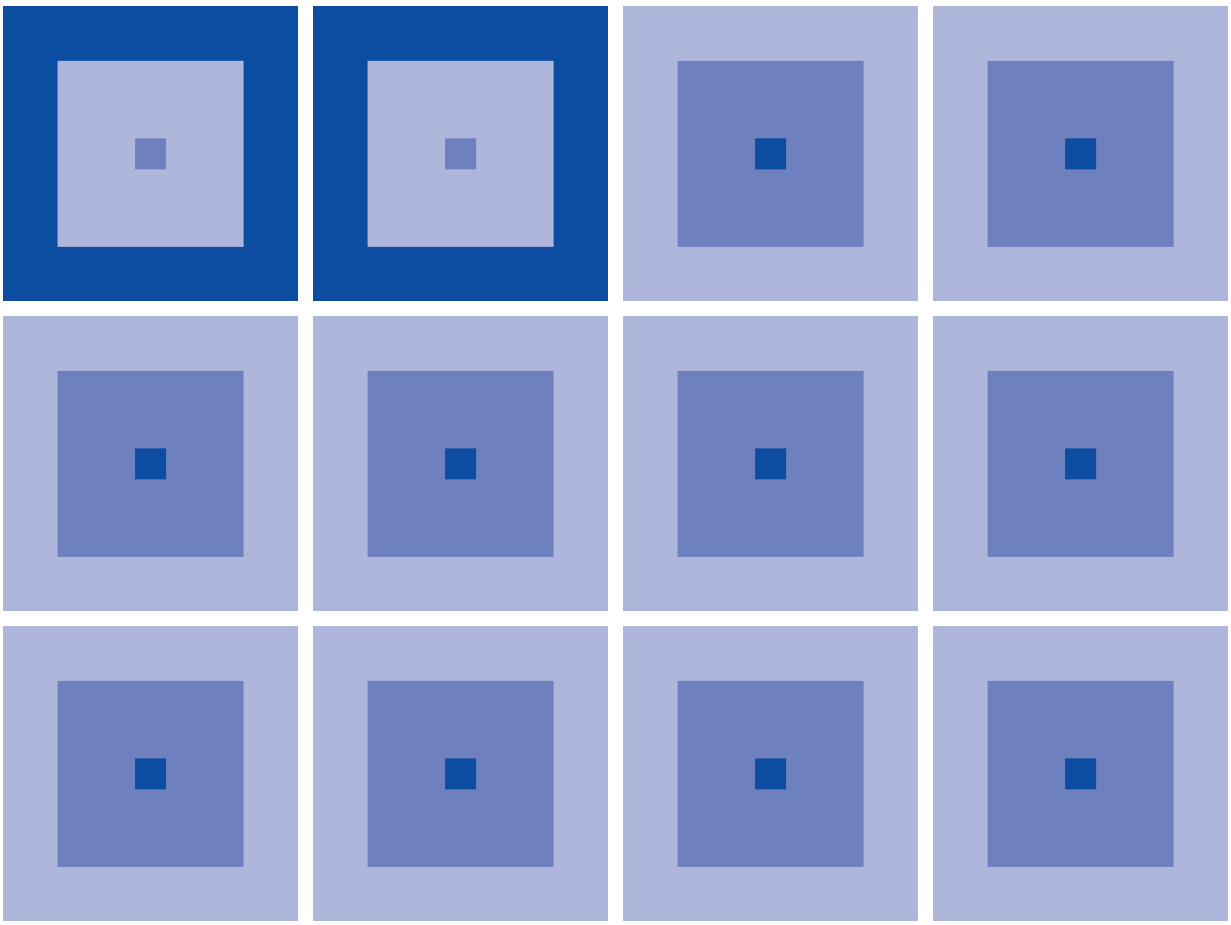
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

S1C63656

Technical Manual

S1C63656 Technical Hardware



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NOTICE

Revisions and Additions for this manual

Chapter	Section	Page	Item	Contents
1	1.1	1	Features	Explanation was revised.
	1.5	5–8	Mask Option	Explanation was revised.
2	2.2.2	13	Simultaneous high input to terminals K00–K03	Explanation was revised. Table 2.2.2.1 was revised.
4	4.1	22	Memory Map	Table 4.1.1(e) was revised.
	4.7.1	48	Configuration of LCD driver	Explanation was revised.
	4.7.2	48	Power supply for LCD driving	Explanation was revised.
	4.7.3	51	Control of LCD display and drive waveform	Explanation was revised. A note was added.
	4.10.1	72	Configuration of programmable timer	Explanation was revised.
	4.14.3	112–113	Operation of R/f conversion	Explanation was revised. Figures 4.14.3.1–4.14.3.2 were revised.
	4.14.4	115–116	Interrupt function	Explanation was revised. Figures 4.14.4.1–4.14.4.4 were revised.
	4.14.5	117, 119	I/O memory of R/f converter	Table 4.14.5.1 was revised. Explanation was revised.
	4.14.6	120	Programming notes	Explanation was revised.
5	5.2	142	Summary of Notes by Function	Explanation was revised.
7	7.1	146	Absolute Maximum Rating	Table was revised.
	7.2	146	Recommended Operating Conditions	Table was revised.
	7.3	146	DC Characteristics	Table was revised.
9	9.1	155	Diagram of Pad Layout	Figure was revised.
Appendix	A.4.2	166	Differences with the actual IC	Explanation was revised. Figure was deleted.

Configuration of product number

Devices

S1 C 63158 F 0A01 00

Packing specifications
- 00 : Besides tape & reel
- 0A : TCP BL 2 directions
- 0B : Tape & reel BACK
- 0C : TCP BR 2 directions
- 0D : TCP BT 2 directions
- 0E : TCP BD 2 directions
- 0F : Tape & reel FRONT
- 0G : TCP BT 4 directions
- 0H : TCP BD 4 directions
- 0J : TCP SL 2 directions
- 0K : TCP SR 2 directions
- 0L : Tape & reel LEFT
- 0M : TCP ST 2 directions
- 0N : TCP SD 2 directions
- 0P : TCP ST 4 directions
- 0Q : TCP SD 4 directions
- 0R : Tape & reel RIGHT
- 99 : Specs not fixed

Specification

Package
[D: die form; F: QFP, B: BGA]

Model number

Model name
[C: microcomputer, digital products]

Product classification
[S1: semiconductor]

Development tools

S5U1 C 63000 A1 1 00

Packing specifications
[00: standard packing]

Version
[1: Version 1]

Tool type
- Hx : ICE
- Ex : EVA board
- Px : Peripheral board
- Wx : Flash ROM writer for the microcomputer
- Xx : ROM writer peripheral board
- Cx : C compiler package
- Ax : Assembler package
- Dx : Utility tool by the model
- Qx : Soft simulator

Corresponding model number
[63000: common to S1C63 Family]

Tool classification
[C: microcomputer use]

Product classification
[S5U1: development tool for semiconductor products]

CONTENTS

CHAPTER 1 OUTLINE

The S1C63656 is a microcomputer which has a high-performance 4-bit CPU S1C63000 as the core CPU, ROM (6,144 words × 13 bits), RAM (1,024 words × 4 bits), multiply-divide circuit, serial interface, watchdog timer, programmable timer, time base counters (2 systems), an LCD driver that can drive a maximum 38 segments × 4 commons, sound generator, R/f converter and stepping motor driver built-in. The S1C63656 features low current consumption, this makes it suitable for battery driven clocks and watches with temperature and humidity measurement functions.

1.1 Features

OSC1 oscillation circuit	32.768 kHz (Typ.) crystal oscillation circuit
OSC3 oscillation circuit	4 MHz (Max.) ceramic (2 MHz Max. when OSC3 is used as the R/f converter operating clock), 1.1 MHz (Typ.) CR oscillation circuit or not used (∗1)
Instruction set	Basic instruction: 46 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time	During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec During operation at 4 MHz: 0.5 µsec 1 µsec 1.5 µsec
ROM capacity	Code ROM: 6,144 words × 13 bits Data ROM: 1,024 words × 4 bits
RAM capacity	Data memory: 1,024 words × 4 bits Display memory: 48 words × 4 bits
Input port	8 bits (Pull-down resistors may be supplemented ∗1)
Output port	4 bits (It is possible to switch the 2 bits to special output ∗2)
I/O port	8 bits (It is possible to switch the 4 bits to serial I/F input/output ∗2)
Serial interface	1 port (8-bit clock synchronous system)
LCD driver	38 segments × 4 or 3 commons (∗2)
Time base counter	Clock timer Stopwatch timer (1/1000 sec, with direct key input function)
Programmable timer	8-bit PWM × 2 ch. or 16-bit PWM × 1 ch. (∗2)
Watchdog timer	Built-in
Sound generator	With envelope and 1-shot output functions
R/f converter	2 ch., CR oscillation type, 20-bit counter Supports resistive humidity sensors
Multiply-divide circuit	8-bit accumulator × 1 ch. Multiplication: 8 bits × 8 bits → 16-bit product Division: 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder
Stepping motor driver	2 ch., a clock or watch controller can be implemented
Supply voltage detection (SVD) circuit	Criteria voltages: 1.85–2.90 V (1.13–1.64 V when OSC3 is not used) are selectable (∗2)
External interrupt	Input port interrupt: 2 systems
Internal interrupt	Clock timer interrupt: 5 systems Stopwatch timer interrupt: 4 systems Programmable timer interrupt: 4 systems Serial interface interrupt: 1 system R/f converter interrupt: 2 systems Motor driver interrupt: 2 systems
Power supply voltage	2.4 to 3.6 V: Max. 4 MHz operation (when OSC3 is used) 1.1 to 3.6 V: 32 kHz operation (when OSC3 is not used)
Operating temperature range	-20 to 70°C
Current consumption (Typ.)	Low-speed operation (OSC1 = 32 kHz crystal oscillation): During HALT 3.0 V (LCD ON) 0.60 µA During operation 3.0 V (LCD ON) 2.50 µA High-speed operation (OSC3 ceramic oscillation): During operation 3.0 V (LCD ON) 1.0 mA
Package	QFP20-144pin (plastic) or chip

∗1: Can be selected with mask option ∗2: Can be selected with software

1.2 Block Diagram

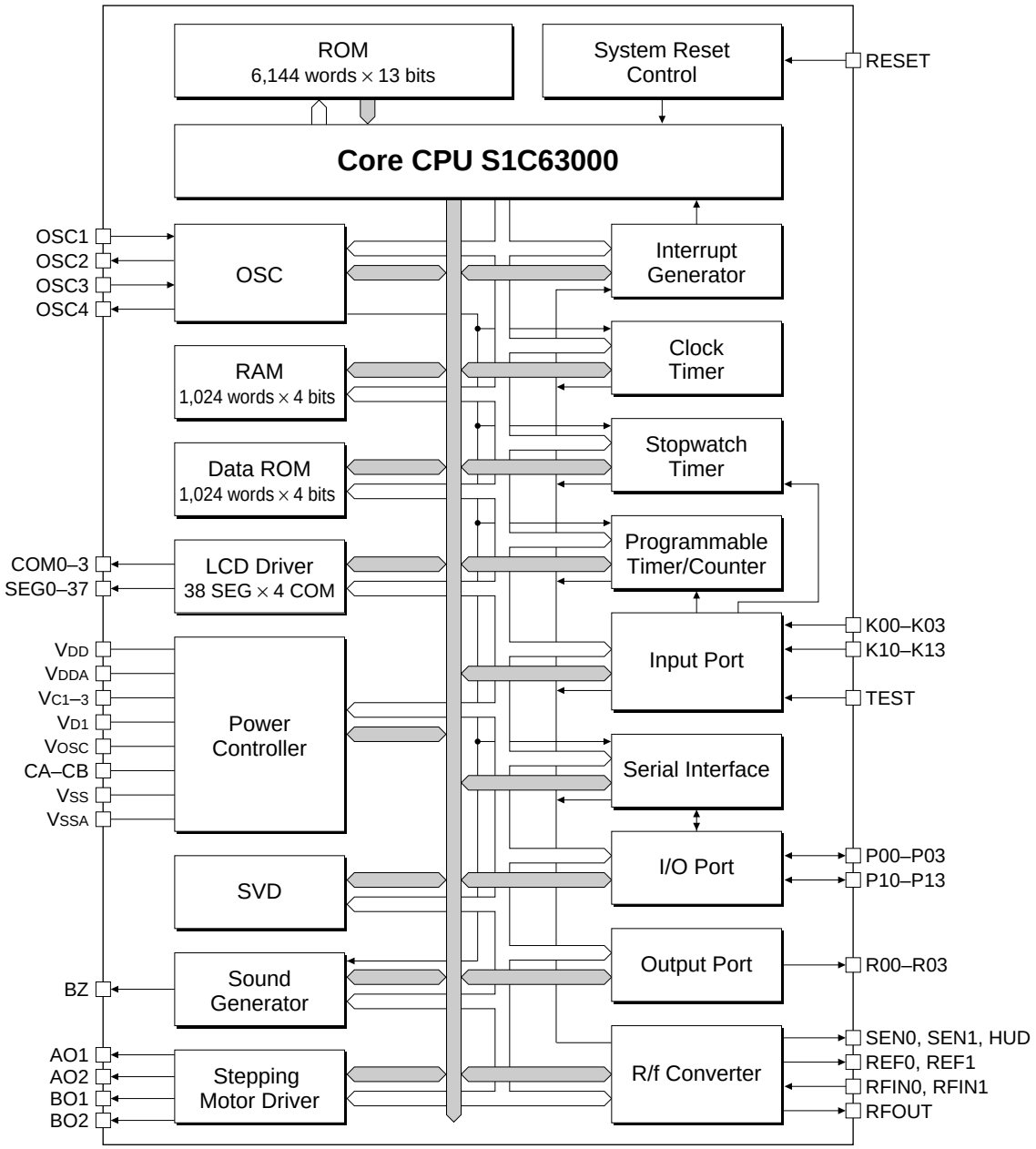
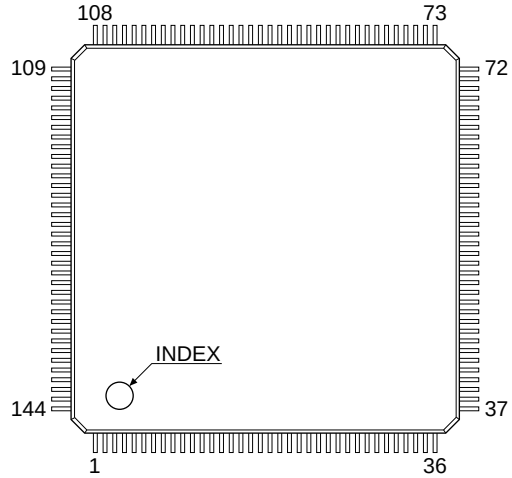


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP20-144pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	CB	37	RESET	73	V_{DD}	109	V_{DD}
2	V_{C1}	38	N.C.	74	K00	110	N.C.
3	V_{C2}	39	N.C.	75	K01	111	N.C.
4	V_{C3}	40	N.C.	76	K02	112	N.C.
5	V_{SSA}	41	N.C.	77	N.C.	113	N.C.
6	RFOUT	42	N.C.	78	K03	114	N.C.
7	N.C.	43	N.C.	79	K10	115	N.C.
8	RFIN0	44	N.C.	80	K11	116	N.C.
9	RFIN1	45	N.C.	81	K12	117	N.C.
10	REF0	46	SEG19	82	K13	118	SEG0
11	SEN0	47	SEG20	83	N.C.	119	SEG1
12	REF1	48	SEG21	84	N.C.	120	SEG2
13	SEN1	49	SEG22	85	P00	121	SEG3
14	N.C.	50	SEG23	86	N.C.	122	SEG4
15	N.C.	51	SEG24	87	P01	123	SEG5
16	HUD	52	SEG25	88	P02	124	SEG6
17	N.C.	53	SEG26	89	P03	125	SEG7
18	N.C.	54	SEG27	90	N.C.	126	SEG8
19	N.C.	55	SEG28	91	N.C.	127	SEG9
20	N.C.	56	SEG29	92	P10	128	SEG10
21	N.C.	57	SEG30	93	P11	129	SEG11
22	V_{DDA}	58	SEG31	94	P12	130	SEG12
23	V_{DDA}	59	SEG32	95	N.C.	131	SEG13
24	V_{OSC}	60	SEG33	96	P13	132	SEG14
25	N.C.	61	SEG34	97	R00	133	SEG15
26	N.C.	62	SEG35	98	N.C.	134	SEG16
27	N.C.	63	SEG36	99	R01	135	SEG17
28	N.C.	64	SEG37	100	R02	136	SEG18
29	OSC1	65	N.C.	101	N.C.	137	N.C.
30	OSC2	66	N.C.	102	R03	138	N.C.
31	V_{D1}	67	N.C.	103	BZ	139	N.C.
32	N.C.	68	N.C.	104	V_{SS}	140	N.C.
33	OSC3	69	N.C.	105	AO1	141	N.C.
34	OSC4	70	N.C.	106	AO2	142	COM0
35	V_{SS}	71	COM2	107	BO1	143	COM1
36	TEST	72	COM3	108	BO2	144	CA

N.C. : No Connection

Fig. 1.3.1 Pin layout diagram (QFP20-144pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	I/O	Function
V_{DD}	73, 109	–	Power (+) supply pin
V_{SS}	35, 104	–	Power (–) supply pin
V_{DDA}	22, 23	–	Analog system power (+) supply pin (=V_{DD})
V_{SSA}	5	–	Analog system power (–) supply pin (=V_{SS})
V_{D1}	31	–	Internal logic operating voltage output pin
V_{OSC}	24	–	Oscillation system regulated voltage output pin
V_{C1}–V_{C3}	2–4	–	LCD system power supply pin
CA, CB	144, 1	–	LCD system voltage booster capacitor connecting pin
OSC1	29	I	Crystal oscillation input pin
OSC2	30	O	Crystal oscillation output pin
OSC3	33	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	34	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	74–76, 78	I	Input port pins
K10–K13	79–82	I	Input port pins
P00–P03	85, 87–89	I/O	I/O port pins
P10	92	I/O	I/O port or serial I/F data input pin (selected by software)
P11	93	I/O	I/O port or serial I/F data output pin (selected by software)
P12	94	I/O	I/O port or serial I/F clock I/O pin (selected by software)
P13	96	I/O	I/O port or serial I/F ready signal output pin (selected by software)
R00	97	O	Output port pin
R01	99	O	Output port pin
R02	100	O	Output port or TOUT output pin (selected by software)
R03	102	O	Output port or FOUT output pin (selected by software)
AO1	105	O	Motor driver Ch. 1 drive pulse output pin 1
AO2	106	O	Motor driver Ch. 1 drive pulse output pin 2
BO1	107	O	Motor driver Ch. 2 drive pulse output pin 1
BO2	108	O	Motor driver Ch. 2 drive pulse output pin 2
COM0–COM3	142, 143, 71, 72	O	LCD common output pin (1/4 or 1/3 duty is selectable by software)
SEG0–SEG37	118–136, 46–64	O	LCD segment output pin
SEN0	11	O	R/f converter Ch. 0 CR oscillation output pin
SEN1	13	O	R/f converter Ch. 1 CR oscillation output pin
REF0	10	O	R/f converter Ch. 0 reference resistor CR oscillation output pin
REF1	12	O	R/f converter Ch. 1 reference resistor CR oscillation output pin
HUD	16	O	R/f converter AC-bias oscillation output pin for humidity sensor
RFIN0	8	I	R/f converter Ch. 0 CR oscillation input pin
RFIN1	9	I	R/f converter Ch. 1 CR oscillation input pin
RFOUT	6	O	R/f converter oscillation frequency output pin
BZ	103	O	Sound output pin
RESET	37	I	Initial reset input pin
TEST	36	I	Testing input pin

1.5 Mask Option

Mask options shown below are provided for the S1C63656. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator winfog and segment option generator winsog, that have been prepared as the development software tool of S1C63656, are used for this selection. Mask pattern of the IC is finally generated based on the data created by winfog and winsog. Refer to the "S5U1C63000A Manual" for winfog and winsog.

<Outline of the mask option>

(1) OSC1 oscillation circuit

The OSC1 oscillation circuit is fixed at crystal oscillation. Refer to Section 4.3.2, "OSC1 oscillation circuit", for details.

(2) OSC3 oscillation circuit

The OSC3 oscillator type can be selected from ceramic oscillation, CR oscillation (external R), CR oscillation (built-in R) and no operation (not used). Refer to Section 4.3.3, "OSC3 oscillation circuit", for details.

(3) Input port pull-down resistor

The mask option is used to select whether the pull-down resistor is supplemented to the input ports or not. It is possible to select for each bit of the input ports. Refer to Section 4.4.3, "Mask option", for details.

(4) RESET terminal pull-down resistor

This option is used to select whether the pull-down resistor is supplemented to the RESET terminal or not. Refer to Section 2.2.1, "Reset terminal (RESET)", for details.

(5) I/O port pull-down resistor

The mask option is used to select whether the pull-down resistor working in the input mode is supplemented to the I/O ports or not. It is possible to select for each bit of the input ports. Refer to Section 4.6.2, "Mask option", for details.

(6) Output specification of the output port

Either complementary output or P-channel open drain output can be selected as the output specification for the output ports R00–R03. The selection is done in 1-bit units. Refer to Section 4.5.2, "Mask option", for details.

(7) Output specification of the I/O port

For the output specification when the I/O ports P00–P03 and P10–P13 are in the output mode, either complementary output or P-channel open drain output can be selected in 1-bit units. Refer to Section 4.6.2, "Mask option", for details.

(8) External reset by simultaneous high input to the input port (K00–K03)

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected. Refer to Section 2.2.2, "Simultaneous high input to terminals K00–K03", for details.

(9) Time authorize circuit for the simultaneous high input reset function

When the external reset function (shown in 8 above) is used, the time authorize circuit is enabled. The reset function works only when the input time of simultaneous low is more than the rule time if the time authorize circuit is being used. When the external reset function is not used, the time authorize circuit cannot be used. Refer to Section 2.2.2, "Simultaneous high input to terminals K00–K03", for details.

(10) Synchronous clock polarity in the serial interface

The polarity of the synchronous clock SCLK and the SRDY signal in slave mode of the serial interface is selected by mask option. Either positive polarity or negative polarity can be selected. Refer to Section 4.11.2, "Mask option", for details.

(11) LCD drive power

Either the internal power supply or an external power supply can be selected for driving LCD. Refer to Section 4.7.2, "Power supply for LCD driving", for details.

(12) LCD segment specification

The display memory can be allocated to the optional SEG terminal. It is also possible to set the optional SEG terminal for DC output. Refer to Section 4.7.5, "Segment option", for details.

<Option list>

The following is the option list for the S1C63656.
Multiple selections are available in each option item as indicated in the option list. Select the specifications that meet the target system and check the appropriate box. Be sure to record the specifications for unused functions too.

1. OSC1 SYSTEM CLOCK

☐ 1. Crystal

2. OSC3 SYSTEM CLOCK

☐ 1. CR (built-in R)
☐ 2. CR (external R)
☐ 3. Ceramic
☐ 4. No Operation (disabled)

3. INPUT PORT PULL DOWN RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• K11	☐ 1. With Resistor	☐ 2. Gate Direct
• K12	☐ 1. With Resistor	☐ 2. Gate Direct
• K13	☐ 1. With Resistor	☐ 2. Gate Direct

4. RESET PORT PULL DOWN RESISTOR

• RESET	☐ 1. With Resistor	☐ 2. Gate Direct

5. I/O PORT PULL DOWN RESISTOR

• P00	☐ 1. With Resistor	☐ 2. Gate Direct
• P01	☐ 1. With Resistor	☐ 2. Gate Direct
• P02	☐ 1. With Resistor	☐ 2. Gate Direct
• P03	☐ 1. With Resistor	☐ 2. Gate Direct
• P10	☐ 1. With Resistor	☐ 2. Gate Direct
• P11	☐ 1. With Resistor	☐ 2. Gate Direct
• P12	☐ 1. With Resistor	☐ 2. Gate Direct
• P13	☐ 1. With Resistor	☐ 2. Gate Direct

6. OUTPUT PORT OUTPUT SPECIFICATION

• R00	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• R01	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• R02	☐ 1. Complementary	☐ 2. Pch-OpenDrain
• R03	☐ 1. Complementary	☐ 2. Pch-OpenDrain

7. I/O PORT OUTPUT SPECIFICATION

- P00 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P01 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P02 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P03 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P10 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P11 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P12 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P13 ☐ 1. Complementary ☐ 2. Pch-OpenDrain

8. MULTIPLE KEY ENTRY RESET COMBINATION

☐ 1. Not Use
☐ 2. Use (K00, K01)
☐ 3. Use (K00, K01, K02)
☐ 4. Use (K00, K01, K02, K03)

9. MULTIPLE KEY ENTRY RESET TIME AUTHORIZE

☐ 1. Not Use
☐ 2. Use

10. SIO SYNC CLOCK & SRDY

☐ 1. Negative
☐ 2. Positive

11. LCD DRIVING POWER

☐ 1. Internal Power (3.0 V panel, normal mode with contrast adjustment function)
☐ 2. External Power 1/3 bias, V_{DD}=V_{C2} (4.5 V panel)
☐ 3. External Power 1/3 bias, V_{DD}=V_{C3} (3.0 V panel)
☐ 4. External Power 1/2 bias, V_{DD}=V_{C3}, V_{C1}=V_{C2} (3.0 V panel)
☐ 5. Internal Power (3.0 V panel, low-power mode without contrast adjustment function)

12. SEGMENT OPTION

Pin name	Address (F0xx)												Output specification
	COM0			COM1			COM2			COM3			
	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0													SEG output ☐ S
SEG1													DC output ☐ C ☐ N
SEG2													SEG output ☐ S
SEG3													DC output ☐ C ☐ N
SEG4													SEG output ☐ S
SEG5													DC output ☐ C ☐ N
SEG6													SEG output ☐ S
SEG7													DC output ☐ C ☐ N
SEG8													SEG output ☐ S
SEG9													DC output ☐ C ☐ N
SEG10													SEG output ☐ S
SEG11													DC output ☐ C ☐ N
SEG12													SEG output ☐ S
SEG13													DC output ☐ C ☐ N
SEG14													SEG output ☐ S
SEG15													DC output ☐ C ☐ N
SEG16													SEG output ☐ S
SEG17													DC output ☐ C ☐ N
SEG18													SEG output ☐ S
SEG19													DC output ☐ C ☐ N
SEG20													SEG output ☐ S
SEG21													DC output ☐ C ☐ N
SEG22													SEG output ☐ S
SEG23													DC output ☐ C ☐ N
SEG24													SEG output ☐ S
SEG25													DC output ☐ C ☐ N
SEG26													SEG output ☐ S
SEG27													DC output ☐ C ☐ N
SEG28													SEG output ☐ S
SEG29													DC output ☐ C ☐ N
SEG30													SEG output ☐ S
SEG31													DC output ☐ C ☐ N
SEG32													SEG output ☐ S
SEG33													DC output ☐ C ☐ N
SEG34													SEG output ☐ S
SEG35													DC output ☐ C ☐ N
SEG36													SEG output ☐ S
SEG37													DC output ☐ C ☐ N

<address> H: RAM data high-order address (0–9)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The S1C63656 operating power voltage is as follows. The operating power voltage range depends on a mask option selection whether the OSC3 clock is used or not.

Table 2.1.1 Operating voltage

OSC3 oscillation circuit	Maximum operating frequency	Operating voltage
Used	4 MHz (OSC3)	2.4 V to 3.6 V
Not used	32 kHz (OSC1 only)	1.1 V to 3.6 V

The S1C63656 operates by applying a single power supply within the above range between VDD and VSS. The S1C63656 itself generates the voltage necessary for all the internal circuits by the built-in power supply circuits shown in Table 2.1.2.

Table 2.1.2 Power supply circuits

Circuit	Power supply	Output voltage
OSC1 circuit	Voltage regulator for OSC1 oscillation circuit	VOSC
Internal circuits (when OSC3 is not used)	Voltage regulator for OSC1 oscillation circuit	VOSC
OSC3 and internal circuits (when OSC3 is used)	High-speed operation voltage regulator	VD3
LCD driver	LCD system voltage circuit	VC1–VC3

Note: • Do not drive external loads with the output voltage from the internal power supply circuits.
• See Chapter 7, "Electrical Characteristics", for voltage values and drive capability.

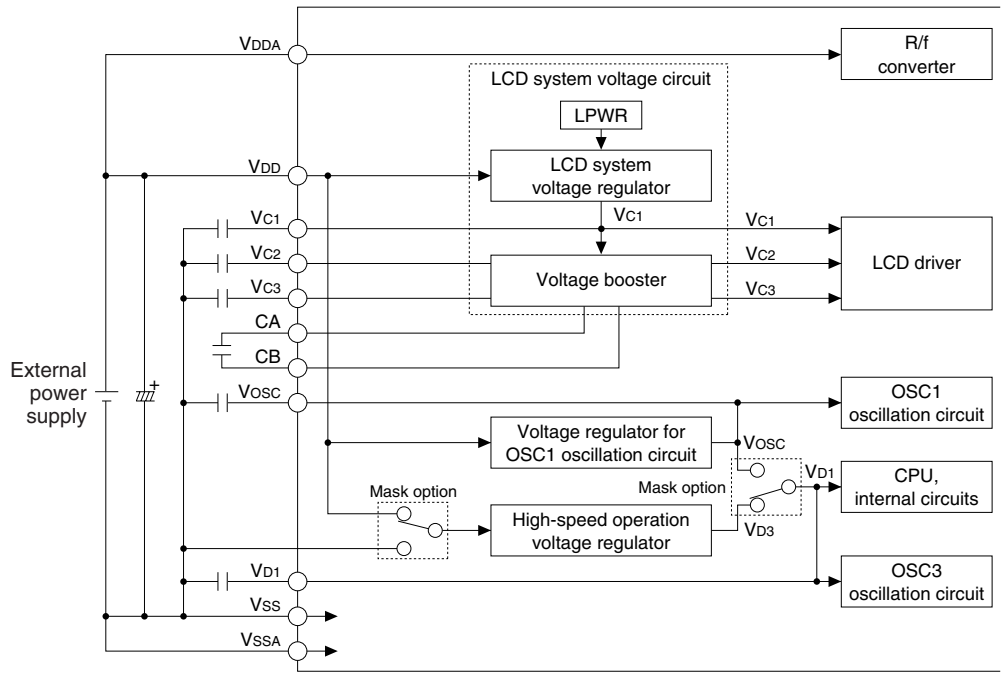


Fig. 2.1.1 Configuration of power supply

The two switches in dotted boxes shown in Figure 2.1.1 are mask options for the OSC3 oscillation circuit. The figure shows the switch status when an option (an oscillator type) that uses the OSC3 oscillation circuit has been selected. When the option (No Operation) to disable the OSC3 oscillation circuit is selected, both the switches are flipped to the other position.

2.1.1 Voltage regulator for OSC1 oscillation circuit

This voltage regulator generates the VOSC voltage (0.98 V Typ.) for driving the OSC1 oscillation circuit. This regulator always operates to drive the OSC1 oscillation circuit.

2.1.2 High-speed operation voltage regulator

The high-speed operation voltage regulator generates the VD3 voltage (2.0 V Typ.) for driving the OSC3 oscillation circuit and the internal logic circuits in high-speed mode. When a mask option for using OSC3 is selected, this voltage regulator always operates. When the option to disable OSC3 is selected, this voltage regulator does not operate and current consumption can be reduced.

2.1.3 Internal operating voltage VD1

VD1 is the operating voltage for the CPU and internal logic circuits. The OSC1 clock allows operation with low-power voltage and low-current consumption as compared with the OSC3 clock for high-speed operation. To take advantage of this feature, the power source of the VD1 voltage is switched according to the mask option selection whether OSC3 is used or not.
When the option to disable OSC3, VOSC (0.98 V Typ.) generated by the voltage regulator for the OSC1 oscillation circuit is used as VD1.
When an option for using OSC3, VD3 (2.0 V Typ.) generated by the high-speed operation voltage regulator is used as VD1.

2.1.4 LCD system voltage circuit

The LCD system voltage circuit generates the LCD drive voltage. This circuit allows the software to turn on and off. Turn this circuit on before starting display on the LCD. The LCD system voltage circuit generates VC1 with the voltage regulator built-in, and generates two other voltages (VC2 = 2VC1, VC3 = 3VC1) by boosting VC1.
The voltage regulator that generates VC1 provides two operating modes, normal mode that allows adjustment of LCD contrast and low-power mode without a contrast adjustment function. One of them can be selected by mask option.
When normal mode is selected, the VC1 voltage can be adjusted to 16 steps (1.03–1.40 V), as a result the LCD contrast changes.
When low-power mode is selected, current consumption can be reduced but the contrast adjustment function is not available.

The LCD system voltage regulator can be disabled by mask option. In this case, external elements can be minimized because the external capacitors for the LCD system voltage regulator are not necessary. However when the LCD system voltage regulator is not used, the display quality of the LCD panel, when the supply voltage fluctuates (drops), is inferior to when the LCD system voltage regulator is used. Figure 2.1.4.1 shows the external element configuration when the LCD system voltage regulator is not used.

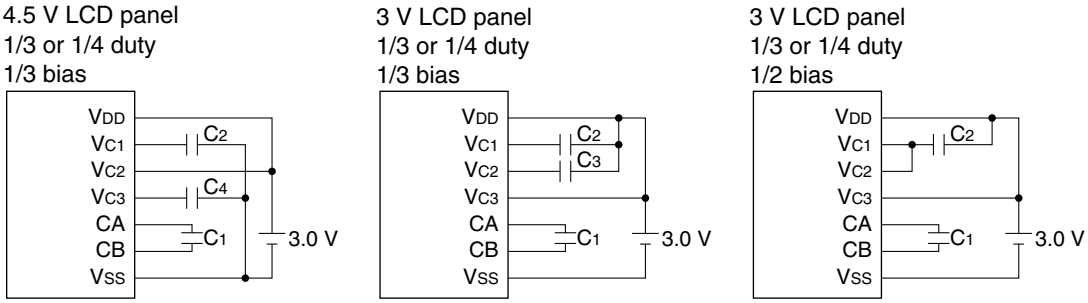


Fig. 2.1.4.1 External elements when LCD system voltage regulator is not used

Refer to Section 4.7, "LCD Driver", for control of the LCD drive voltage.

2.1.5 Analog system power supply

The VDDA and VSSA power supply terminals are provided only for the R/f converter in order to avoid decreasing the conversion accuracy due to noise. However, the same voltage level as the VDD–VSS must be supplied to the VDDA–VSSA.
VDDA = VDD, VSSA = VSS

2.2 Initial Reset

To initialize the S1C63656 circuits, initial reset must be executed. There are two ways of doing this.

(1) External initial reset by the RESET terminal
(2) External initial reset by simultaneous high input to terminals K00–K03 (mask option setting)

The circuits are initialized by either (1) or (2). When the power is turned on, be sure to initialize using the reset function. It is not guaranteed that the circuits are initialized by only turning the power on.

Figure 2.2.1 shows the configuration of the initial reset circuit.

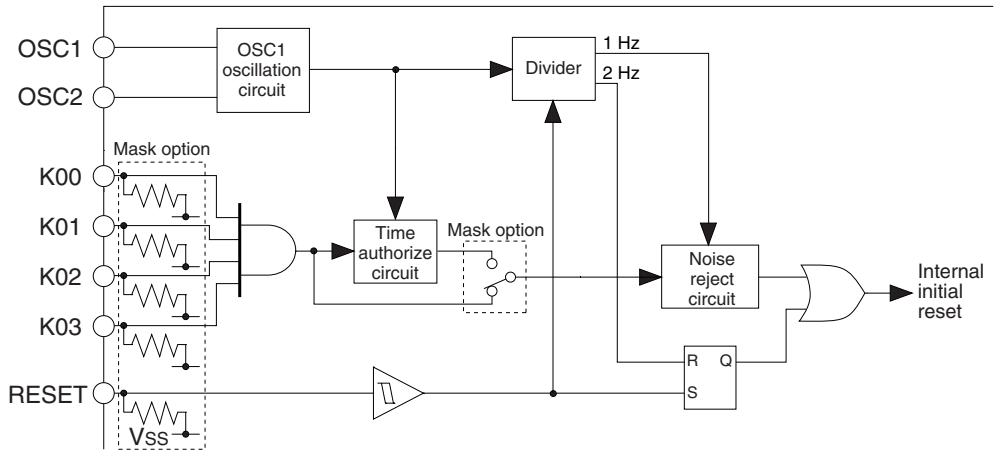


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a high level (V_{DD}). After that the initial reset is released by setting the reset terminal to a low level (V_{SS}) and the CPU starts operation.
The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 2 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 250 msec (when f_{OSC1} = 32.768 kHz) is needed until the internal initial reset is released after the reset terminal goes to low level. Be sure to maintain a reset input of 0.1 msec or more. However, when turning the power on, the reset terminal should be set at a high level as in the timing shown in Figure 2.2.1.1.
Note that a reset pulse shorter than 100 nsec is rejected as noise.

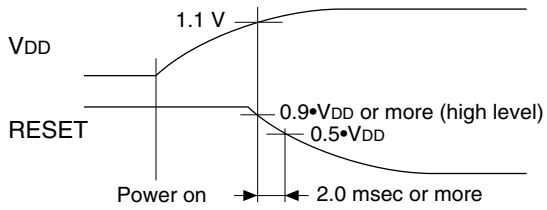


Fig. 2.2.1.1 Initial reset at power on

The reset terminal should be set to 0.9•V_{DD} or more (high level) until the supply voltage becomes 1.1 V or more.
After that, a level of 0.5•V_{DD} or more should be maintained more than 2.0 msec.

The reset terminal incorporates a pull-down resistor and a mask option is provided to select whether the resistor is used or not.

2.2.2 Simultaneous high input to terminals K00–K03

Another way of executing initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option.
Since this initial reset passes through the noise reject circuit, maintain the specified input port terminals at high level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) during normal operation. The noise reject circuit does not operate immediately after turning the power on until the oscillation circuit starts oscillating. Therefore, maintain the specified input port terminals at high level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) after oscillation starts.
Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not use
2	K00∗K01
3	K00∗K01∗K02
4	K00∗K01∗K02∗K03

When, for instance, mask option 4 (K00∗K01∗K02∗K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time. When 2 or 3 is selected, the initial reset is done when a key entry including a combination of selected input ports is made.

Further, the time authorize circuit mask option is selected when this reset function is selected. The time authorize circuit checks the input time of the simultaneous high input and performs initial reset if that time is the defined time (1 to 2 sec) or more.
If using this function, make sure that the specified ports do not go high at the same time during ordinary operation.

2.2.3 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.3.1.
The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.
In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.
When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.
Refer to the "S1C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.3.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	–	∗

∗ See Section 4.1, "Memory Map".

2.2.4 Terminal settings at initial resetting

The output port (R) terminals and I/O port (P) terminals are shared with special output terminals and input/output terminals of the serial interface. These functions are selected by the software. At initial reset, these terminals are set to the general purpose output port terminals and I/O port terminals. Set them according to the system in the initial routine. In addition, take care of the initial status of output terminals when designing a system.
Table 2.2.4.1 shows the list of the shared terminal settings.

Table 2.2.4.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	Special output		Serial I/F	
		TOUT	FOUT	Master	Slave
R00	R00 (LOW output)				
R01	R01 (LOW output)				
R02	R02 (LOW output)	TOUT			
R03	R03 (LOW output)		FOUT		
P00–P03	P00–P03 (Input & pulled down∗)				
P10	P10 (Input & pulled down∗)			SIN(I)	SIN(I)
P11	P11 (Input & pulled down∗)			SOUT(O)	SOUT(O)
P12	P12 (Input & pulled down∗)			SCLK(O)	SCLK(I)
P13	P13 (Input & pulled down∗)				SRDY(O)

∗ When "With Pull-Down" is selected by mask option (high impedance when "Gate Direct" is selected)

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal (TEST)

This is the terminal used for the factory inspection of the IC. During normal operation, connect the TEST terminal to VSS.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C63656 has a 4-bit core CPU S1C63000 built-in as its CPU part.
Refer to the "S1C63000 Core CPU Manual" for the S1C63000.

Note: The SLP instruction cannot be used because the SLEEP operation is not assumed in the S1C63656.

3.2 Code ROM

The built-in code ROM is a mask ROM for loading programs, and has a capacity of 6,144 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the S1C63656 is step 0000H to step 17FFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0102H–010EH, respectively.

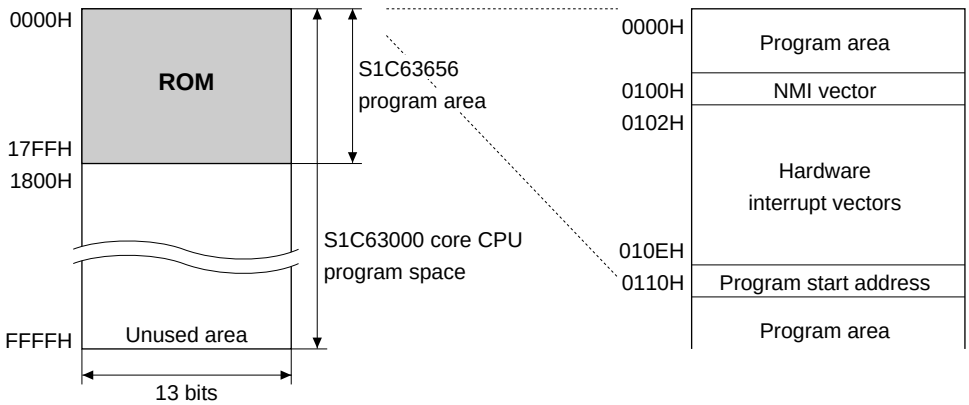


Fig. 3.2.1 Configuration of code ROM

3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 1,024 words × 4 bits. The RAM area is assigned to addresses 0000H to 03FFH on the data memory map. Addresses 0100H to 01FFH are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data. When programming, keep the following points in mind.

(1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(2) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63656 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

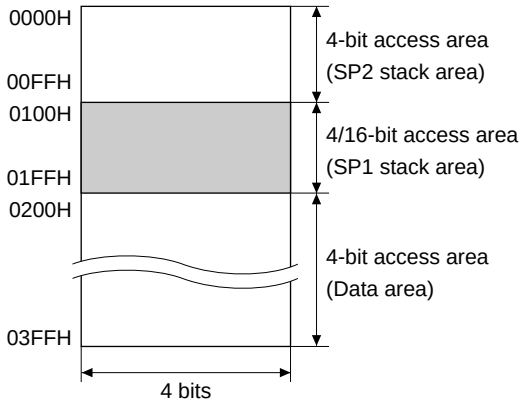


Fig. 3.3.1 Configuration of data RAM

3.4 Data ROM

The data ROM is a mask ROM for loading various static data such as a character generator, and has a capacity of 1,024 words × 4 bits. The data ROM is assigned to addresses 8000H to 83FFH on the data memory map, and the data can be read using the same data memory access instructions as the RAM.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of S1C63656 (timer, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions. The following sections explain the detailed operation of each peripheral circuit.

4.1 Memory Map

The S1C63656 data memory consists of 1,024-word RAM, 1,024-word data ROM, 48-word display memory and 101-word peripheral I/O memory. Figure 4.1.1 shows the overall memory map of the S1C63656, and Table 4.1.1 the peripheral circuits' (I/O space) memory maps.

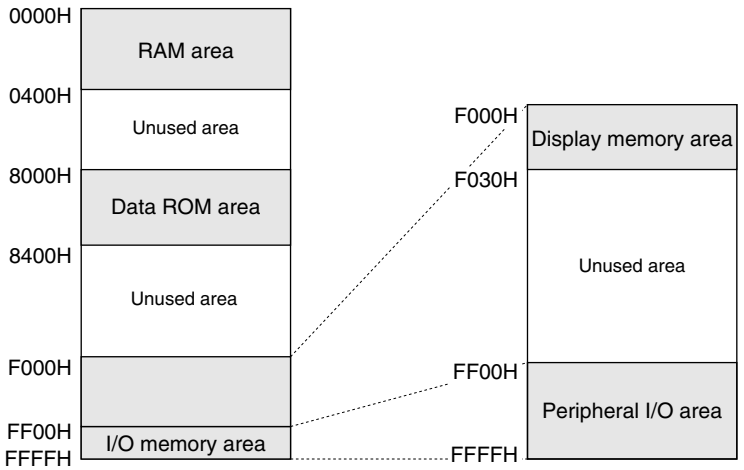


Fig. 4.1.1 Memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Table 4.1.1 for the peripheral I/O area.

Table 4.1.1 (a) I/O memory map (FF01H–FF20H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF01H	CLKCHG	OSCC	0	0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused
FF04H	0	SVDS2	SVDS1	SVDS0	0 *3	– *2			Unused
					SVDS2	0			SVD criteria voltage setting (V1: when OSC3 is used, V2: when OSC3 is not used)
	R	R/W			SVDS1	0			[SVDS2–0] 0 1 2 3 4 5 6 7
					SVDS0	0			V1 (V) 1.85 2.00 2.15 2.30 2.45 2.60 2.75 2.90
									V2 (V) – 1.13 1.22 1.30 1.39 1.47 1.56 1.64
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					SWDIR	0			Stopwatch direct input switch
	R/W								0: K00=Run/Stop, K01=Lap 1: K00=Lap, K01=Run/Stop
					FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3
					FOFQ0	0			Frequency fOSC1/64 fOSC1/8 fOSC1 fOSC3
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)
FF10H	0	0	FTRG2	FTRG1	0 *3	– *2			Unused
					0 *3	– *2			Unused
			FRUN2	FRUN1	FTRG2	– *2	Trigger	Invalid	Motor driver Ch. 2 trigger (writing)
	R		W	W	FRUN2	0	Run	Stop	Motor driver Ch. 2 status (reading)
					FTRG1	– *2	Trigger	Invalid	Motor driver Ch. 1 trigger (writing)
			R	R	FRUN1	0	Run	Stop	Motor driver Ch. 1 status (reading)
FF11H	0	0	0	PFWA4	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					PFWA4	0			Motor driver Ch. 1 pulse width selection
FF12H	PFWA3	PFWA2	PFWA1	PFWA0	PFWA3	0			
					PFWA2	0			
	R/W				PFWA1	0			
					PFWA0	0			
FF13H	0	0	0	PFWB4	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					PFWB4	0			Motor driver Ch. 2 pulse width selection
FF14H	PFWB3	PFWB2	PFWB1	PFWB0	PFWB3	0			
					PFWB2	0			
	R/W				PFWB1	0			
					PFWB0	0			
FF15H	0	0	0	PFTYP	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					PFTYP	0	Short	Long	Pulse width base clock selection
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	

[PFWA4–0] / [PFWB4–0] — Pulse width (PFTYP = "1") — (PFTYP = "0")

00H	1.46 msec	11.72 msec
01H	1.71 msec	13.67 msec
02H	1.95 msec	15.63 msec
03H	2.20 msec	17.58 msec
04H	2.44 msec	19.53 msec
05H	2.69 msec	21.48 msec
06H	2.93 msec	23.44 msec
07H	3.17 msec	25.39 msec
08H	3.42 msec	27.34 msec
09H	3.66 msec	29.30 msec
0AH	3.91 msec	31.25 msec
0BH	4.15 msec	33.20 msec
0CH	4.40 msec	35.16 msec
0DH	4.64 msec	37.11 msec
0EH	4.88 msec	39.06 msec
0FH	5.13 msec	41.02 msec
10H	5.37 msec	42.97 msec
11H	5.62 msec	44.92 msec
12H	5.86 msec	46.88 msec
13H	6.10 msec	48.83 msec
14H	6.35 msec	50.78 msec
15H	6.59 msec	52.73 msec
16H	6.84 msec	54.69 msec
17H	7.08 msec	56.64 msec
18H–1FH	3.42 msec	27.34 msec

Remarks

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF21H–FF45H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	Hi-Z	Output	R03 (FOUTE=0)/FOUT (FOUTE=1) Hi-Z control
					R02HIZ	0	Hi-Z	Output	R02 (PTOUT=0)/TOUT (PTOUT=1) Hi-Z control
	R/W				R01HIZ	0	Hi-Z	Output	R01 Hi-Z control
					R00HIZ	0	Hi-Z	Output	R00 Hi-Z control
FF31H	R03	R02	R01	R00	R03	0	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used.
					R02	0	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used.
	R/W				R01	0	High	Low	R01 output port data
					R00	0	High	Low	R00 output port data
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-down control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-down control register (ESIF=0) functions as a general-purpose register when SIF (master) is selected SCLK (I) pull-down control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-down control register (ESIF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-down control register (ESIF=0) SIN pull-down control register when SIF is selected

Table 4.1.1 (c) I/O memory map (FF46H–FF73H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF46H	P13 (XSRDY)	P12 (XSCLK)	P11 (SOUT)	P10 (SIN)	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
FF60H	LDUTY1	LDUTY0	STCD	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0]: 0 = 1/4 Duty, 1,2 = 1/3 Duty, 3 = 1/3 Duty
					LDUTY0	0			
	R/W				STCD	0	Static	Dynamic	LCD drive switch
					LPWR	0	On	Off	LCD power On/Off
FF61H	0	ALOFF	ALON	0	0 *3	– *2			Unused
					ALOFF	1	All Off	Normal	LCD all Off control
	R	R/W		R	ALON	0	All On	Normal	LCD all On control
					0 *3	– *2			Unused
FF62H	LC3	LC2	LC1	LC0	LC3	0			LCD contrast adjustment [LC3–0]: 0 – 15 Contrast: Light – Dark
					LC2	0			
	R/W				LC1	0			
					LC0	0			
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
FF6DH	0	BZSTP	BZSHT	SHTPW	0 *3	– *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0 *3	– *2			Unused
					BZFQ2	0			Buzzer frequency selection [BZFQ2, 1, 0]: 0 / 1 / 2 / 3 Frequency (Hz): 4096.0 / 3276.8 / 2730.7 / 2340.6 [BZFQ2, 1, 0]: 4 / 5 / 6 / 7 Frequency (Hz): 2048.0 / 1638.4 / 1365.3 / 1170.3
	R	R/W			BZFQ1	0			
					BZFQ0	0			
FF6FH	0	BDTY2	BDTY1	BDTY0	0 *3	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
	R	R/W			BDTY1	0			
					BDTY0	0			
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R	R/W					Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
					SCPS	0			Serial I/F clock phase selection –Negative polarity (mask option) –Positive polarity (mask option)
	R/W				SCS1	0			Serial I/F clock mode selection [SCS1, 0]: 0 / 1 Clock: Slave / PT [SCS1, 0]: 2 / 3 Clock: OSC1/2 / OSC1
					SCS0	0			
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
					SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
	R/W				SD1	– *2	High	Low	
					SD0	– *2	High	Low	LSB
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
					SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
	R/W				SD5	– *2	High	Low	
					SD4	– *2	High	Low	LSB

Table 4.1.1 (d) I/O memory map (FF74H–FF85H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF74H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF75H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF76H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FF78H	EDIR	DKM2	DKM1	DKM0	EDIR	0	Enable	Disable	Direct input enable
					DKM2	0			Key mask selection [DKM2, 1, 0] 0: Key mask None; 1: K02; 2: K02–03; 3: K02–03,10; [DKM2, 1, 0] 4: Key mask K10; 5: K10–11; 6: K10–12; 7: K10–13
	R/W				DKM1	0			
					DKM0	0			
FF79H	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Request	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
FF7AH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/1000 sec)
					SWD2	0			
	R				SWD1	0			
					SWD0	0			
FF7BH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/100 sec)
					SWD6	0			
	R				SWD5	0			
					SWD4	0			
FF7CH	SWD11	SWD10	SWD9	SWD8	SWD11	0			Stopwatch timer data BCD (1/10 sec)
					SWD10	0			
	R				SWD9	0			
					SWD8	0			
FF80H	SR3	SR2	SR1	SR0	SR3	– *2			Source register (low-order 4 bits)
					SR2	– *2			
	R/W				SR1	– *2			
					SR0	– *2			LSB
FF81H	SR7	SR6	SR5	SR4	SR7	– *2			MSB
					SR6	– *2			Source register (high-order 4 bits)
	R/W				SR5	– *2			
					SR4	– *2			
FF82H	DRL3	DRL2	DRL1	DRL0	DRL3	– *2			Low-order 8-bit destination register (low-order 4 bits)
					DRL2	– *2			
	R/W				DRL1	– *2			
					DRL0	– *2			LSB
FF83H	DRL7	DRL6	DRL5	DRL4	DRL7	– *2			MSB
					DRL6	– *2			Low-order 8-bit destination register (high-order 4 bits)
	R/W				DRL5	– *2			
					DRL4	– *2			
FF84H	DRH3	DRH2	DRH1	DRH0	DRH3	– *2			High-order 8-bit destination register (low-order 4 bits)
					DRH2	– *2			
	R/W				DRH1	– *2			
					DRH0	– *2			LSB
FF85H	DRH7	DRH6	DRH5	DRH4	DRH7	– *2			MSB
					DRH6	– *2			High-order 8-bit destination register (high-order 4 bits)
	R/W				DRH5	– *2			
					DRH4	– *2			

Table 4.1.1 (e) I/O memory map (FF86H–FFC0H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF86H	NF	VF	ZF	CALMD	NF	0	Negative	Positive	Negative flag
					VF	0	Overflow	No	Overflow flag
					ZF	0	Zero	No	Zero flag
	R			R/W	CALMD	0	Run	Stop	Operation status (reading)
							Div.	Mult.	Calculation mode selection (writing)
FF90H	0	RFCLK	RFSEL	SENSEL	0 *3	– *2			Unused
					RFCLK	0	OSC3	OSC1	R/f conversion clock selection
	R	R/W			RFSEL	0	AC	DC	Ch. 1 sensor type selection
					SENSEL	0	Ch. 1	Ch. 0	Conversion channel selection
FF91H	OVTBC	OVMC	RFRUNR	RFRUNS	OVTBC	0	Overflow	Non-ov	Time base counter overflow flag
					OVMC	0	Overflow	Non-ov	Measurement counter overflow flag
	R/W				RFRUNR	0	Run	Stop	Reference oscillation Run control/status (writing "0" is ineffective)
					RFRUNS	0	Run	Stop	Sensor oscillation Run control/status (writing "0" is ineffective)
FF92H	MC3	MC2	MC1	MC0	MC3	– *2			Measurement counter MC0–MC3
					MC2	– *2			
	R/W				MC1	– *2			
					MC0	– *2			LSB
FF93H	MC7	MC6	MC5	MC4	MC7	– *2			Measurement counter MC4–MC7
					MC6	– *2			
	R/W				MC5	– *2			
					MC4	– *2			
FF94H	MC11	MC10	MC9	MC8	MC11	– *2			Measurement counter MC8–MC11
					MC10	– *2			
	R/W				MC9	– *2			
					MC8	– *2			
FF95H	MC15	MC14	MC13	MC12	MC15	– *2			Measurement counter MC12–MC15
					MC14	– *2			
	R/W				MC13	– *2			
					MC12	– *2			
FF96H	MC19	MC18	MC17	MC16	MC19	– *2			MSB
					MC18	– *2			Measurement counter MC16–MC19
	R/W				MC17	– *2			
					MC16	– *2			
FF97H	TC3	TC2	TC1	TC0	TC3	– *2			Time base counter TC0–TC3
					TC2	– *2			
	R/W				TC1	– *2			
					TC0	– *2			LSB
FF98H	TC7	TC6	TC5	TC4	TC7	– *2			Time base counter TC4–TC7
					TC6	– *2			
	R/W				TC5	– *2			
					TC4	– *2			
FF99H	TC11	TC10	TC9	TC8	TC11	– *2			Time base counter TC8–TC11
					TC10	– *2			
	R/W				TC9	– *2			
					TC8	– *2			
FF9AH	TC15	TC14	TC13	TC12	TC15	– *2			Time base counter TC12–TC15
					TC14	– *2			
	R/W				TC13	– *2			
					TC12	– *2			
FF9BH	TC19	TC18	TC17	TC16	TC19	– *2			MSB
					TC18	– *2			Time base counter TC16–TC19
	R/W				TC17	– *2			
					TC16	– *2			
FFC0H	MOD16	EVCNT	FCSEL	PLPOL	MOD16	0	16 bits	8 bits	16-bit mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R/W				FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)

Table 4.1.1 (f) I/O memory map (FFC1H–FFD3H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFC1H	0	0	CHSEL0	PTOUT	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		CHSEL0	0	Timer 1	Timer 0	TOUT output selection
					PTOUT	0	On	Off	TOUT output control
FFC2H	0	0	CKSEL1	CKSEL0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC3H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC4H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC6H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FFC7H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FFC8H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FFC9H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FFCCH	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFCDH	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FFCEH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCFH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FFD2H	CD03	CD02	CD01	CD00	CD03	0			MSB
					CD02	0			Programmable timer 0 compare data (low-order 4 bits)
	R/W				CD01	0			
					CD00	0			LSB
FFD3H	CD07	CD06	CD05	CD04	CD07	0			MSB
					CD06	0			Programmable timer 0 compare data (high-order 4 bits)
	R/W				CD05	0			
					CD04	0			LSB

Table 4.1.1 (g) I/O memory map (FFD4H–FFF0H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFD4H	CD13	CD12	CD11	CD10	CD13	0			MSB
					CD12	0			Programmable timer 1 compare data (low-order 4 bits)
	R/W				CD11	0			
					CD10	0			LSB
FFD5H	CD17	CD16	CD15	CD14	CD17	0			MSB
					CD16	0			Programmable timer 1 compare data (high-order 4 bits)
	R/W				CD15	0			
					CD14	0			LSB
FFD8H	0	0	PTSEL1	PTSEL0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		PTSEL1	0	PWM	Normal	Programmable timer 1 PWM output selection
					PTSEL0	0	PWM	Normal	Programmable timer 0 PWM output selection
FFE0H	0	0	ECTC1	ECTC0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		ECTC1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 compare match)
					ECTC0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 compare match)
FFE1H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 underflow)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 underflow)
FFE2H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFE3H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE4H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE5H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE6H	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFE7H	0	0	EIRFB	EIRFM	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIRFB	0	Enable	Mask	Interrupt mask register (R/f converter reference oscillate completion)
					EIRFM	0	Enable	Mask	Interrupt mask register (R/f converter sensor oscillate completion)
FFE8H	0	0	EISMD2	EISMD1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EISMD2	0	Enable	Mask	Interrupt mask register (Motor driver Ch. 2)
					EISMD1	0	Enable	Mask	Interrupt mask register (Motor driver Ch. 1)
FFE9H	0	0	0	EIT4	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIT4	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFF0H	0	0	ICTC1	ICTC0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ICTC1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1 compare match)
					ICTC0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0 compare match)

Table 4.1.1 (h) I/O memory map (FFF1H–FFF9H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFF1H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1 underflow)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0 underflow)
FFF2H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)
FFF3H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF4H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF5H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF6H	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)
FFF7H	0	0	IRFB	IRFM	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IRFB	0	(W)	(W)	Interrupt factor flag (R/f converter reference oscillate completion)
					IRFM	0	Reset	Invalid	Interrupt factor flag (R/f converter sensor oscillate completion)
FFF8H	0	0	ISMD2	ISMD1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISMD2	0	(W)	(W)	Interrupt factor flag (Motor driver Ch. 2)
					ISMD1	0	Reset	Invalid	Interrupt factor flag (Motor driver Ch. 1)
FFF9H	0	0	0	IT4	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IT4	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)

4.2 Watchdog Timer

4.2.1 Configuration of watchdog timer

The S1C63656 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

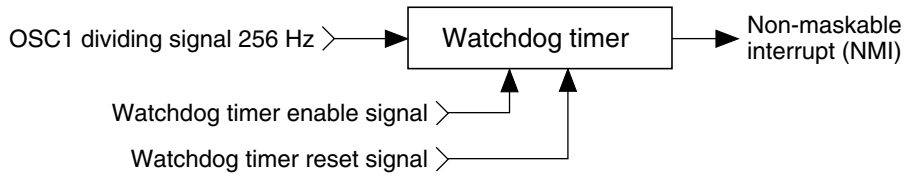


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

4.2.2 Interrupt function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "0"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

4.2.3 I/O memory of watchdog timer

Table 4.2.3.1 shows the I/O address and control bits for the watchdog timer.

Table 4.2.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

WDEN: Watchdog timer enable register (FF07H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI).
At initial reset, this register is set to "1".

WDRST: Watchdog timer reset (FF07H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.2.4 Programming notes

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The S1C63656 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the S1C63656 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software.
If the application needs low-voltage and low-power operations precedence to performance, the OSC3 oscillation circuit and the high-speed operation voltage regulator can be disabled by mask option.
Figure 4.3.1.1 is the block diagram of this oscillation system.

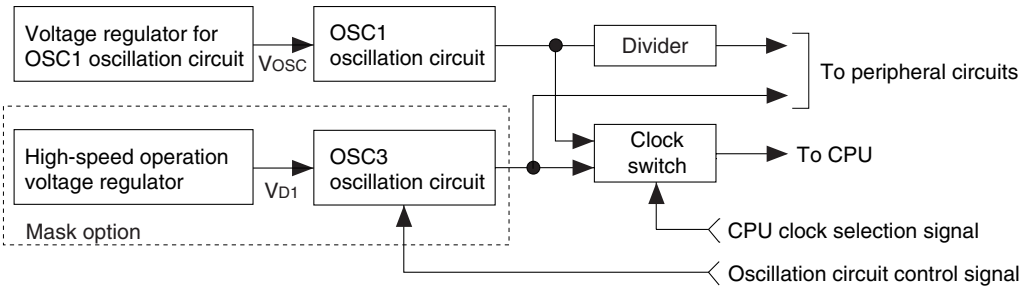


Fig. 4.3.1.1 Oscillation system block diagram

4.3.2 OSC1 oscillation circuit

The OSC1 crystal oscillation circuit generates the main clock for the CPU and the peripheral circuits. The oscillation frequency is 32.768 kHz (Typ.).
Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

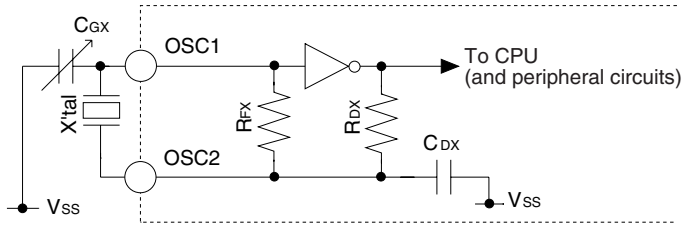


Fig. 4.3.2.1 OSC1 oscillation circuit

As shown in Figure 4.3.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) of 32.768 kHz (Typ.) between the OSC1 and OSC2 terminals and the trimmer capacitor (C_{GX}) between the OSC1 and V_{SS} terminals.

4.3.3 OSC3 oscillation circuit

The S1C63656 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Max. 4 MHz) for high speed operation and the source clock for peripheral circuits needing a high speed clock (programmable timer, FOUT output). The mask option enables selection of the oscillator type from CR (external R type), CR (built-in R type) and ceramic oscillation circuit. When CR oscillation (external R type) is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required. When CR oscillation (built-in R type) is selected, no external element is required. If the application needs low-voltage and low-power operations precedence to performance, the OSC3 oscillation circuit and the high-speed operation voltage regulator can be disabled by mask option.
Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.

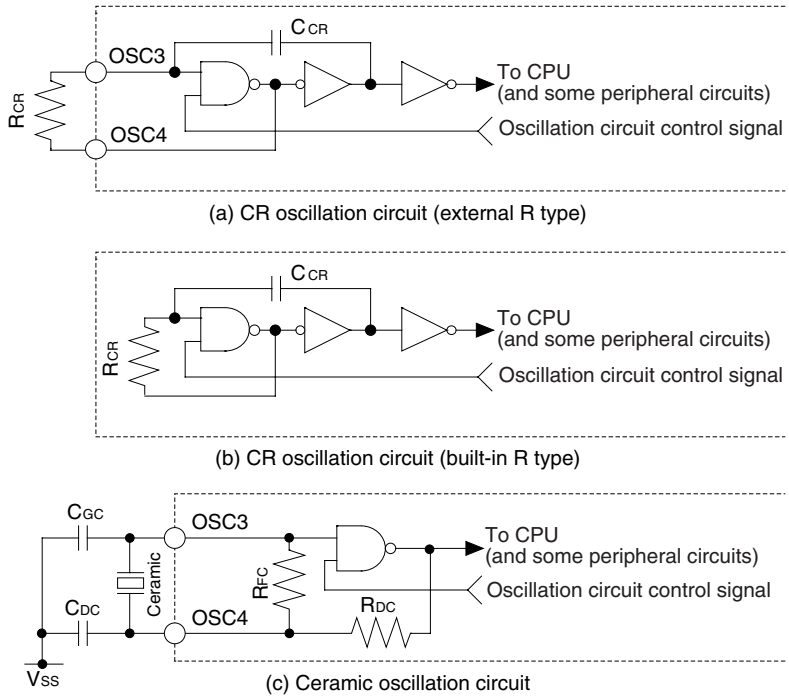


Fig. 4.3.3.1 OSC3 oscillation circuit

As shown in Figure 4.3.3.1, the CR oscillation circuit (external R type) can be configured simply by connecting the resistor RCR between the OSC3 and OSC4 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics" for resistance value of RCR.
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Max. 4 MHz) between the OSC3 and OSC4 terminals, capacitor CGC between the OSC3 and OSC4 terminals, and capacitor CDC between the OSC4 and VSS terminals. For both CGC and CDC, connect capacitors that are about 30 pF. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

Table 4.3.3.1 OSC3 oscillation frequency

Oscillation circuit	Oscillation frequency
Ceramic oscillation	Max. 4 MHz (2 MHz [Note])
CR oscillation (built-in R type)	Typ. 1.1 MHz ±30%
CR oscillation (external R type)	200 kHz to 2 MHz

Note: When selecting OSC3 for the time base counter clock of the R/f converter, the maximum frequency of the OSC3 clock is limited to 2 MHz.

4.3.4 Switching of CPU clock

In the system that uses the OSC3 oscillation circuit (selected by mask option), the system clock can be selected between OSC1 and OSC3 with software (using the CLKCHG register). The control sequence described below is not necessary in the system that uses the OSC1 oscillation circuit only.
The CPU clock should be switched using the following procedure. Pay special attention to the stability waiting time for oscillation.

OSC1 → OSC3

1. Set OSCC to "1". (OSC3 oscillation: off → on)
2. Wait 5 msec or more.
3. Set CLKCHG to "1". (CPU clock: OSC1 → OSC3)

Note: It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

OSC3 → OSC1

1. Set CLKCHG to "0". (CPU clock: OSC3 → OSC1)
2. Set OSCC to "0". (OSC3 oscillation: on → off)

Note: When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

4.3.5 Clock frequency and instruction execution time

Table 4.3.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.3.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μsec)		
	1-cycle instruction	2-cycle instruction	3-cycle instruction
OSC1: 32.768 kHz	61	122	183
OSC3: 1.1 MHz	1.8	3.6	5.5
OSC3: 2 MHz	1	2	3
OSC3: 4 MHz	0.5	1	1.5

4.3.6 I/O memory of oscillation circuit

Table 4.3.6.1 shows the I/O address and the control bits for the oscillation circuit.

Note: The control bits for the oscillation circuit described below are effective only when the OSC3 oscillation circuit is used. If the system uses the OSC1 oscillation circuit only, do not change the default settings.

Table 4.3.6.1 Control bits of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF01H	CLKCHG	OSCC	0	0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

OSCC: OSC3 oscillation control register (FF01H•D2)

Turns the OSC3 oscillation circuit on and off.

When "1" is written: OSC3 oscillation On
When "0" is written: OSC3 oscillation Off
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption.
At initial reset, this register is set to "0".

CLKCHG: CPU system clock switching register (FF01H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
After turning the OSC3 oscillation on (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.
At initial reset, this register is set to "0".

4.3.7 Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) When selecting OSC3 for the time base counter clock of the R/f converter, the maximum frequency of the OSC3 clock is limited to 2 MHz.

4.4 Input Ports (K00–K03 and K10–K13)

4.4.1 Configuration of input ports

The S1C63656 has eight bits of general-purpose input ports (K00–K03, K10–K13). Each input port terminal provides an internal pull-down resistor that can be enabled by mask option.
Figure 4.4.1.1 shows the configuration of input port.

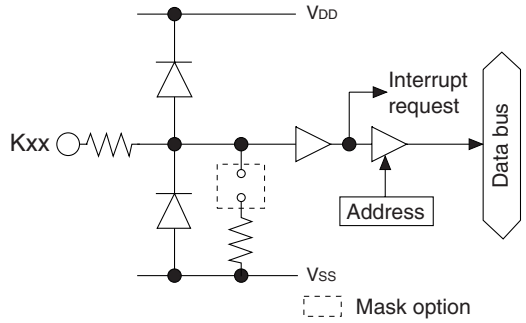


Fig. 4.4.1.1 Configuration of input port

Selection of "With pull-down resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.
The K00 and K01 input ports can also be used as the Run/Stop and Lap direct inputs for the stopwatch timer, and the K13 port can also be used as the event counter input for the programmable timer.

4.4.2 Interrupt function

All eight bits of the input ports (K00–K03, K10–K13) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software.
Figure 4.4.2.1 shows the configuration of K00–K03 (K10–K13) interrupt circuit.

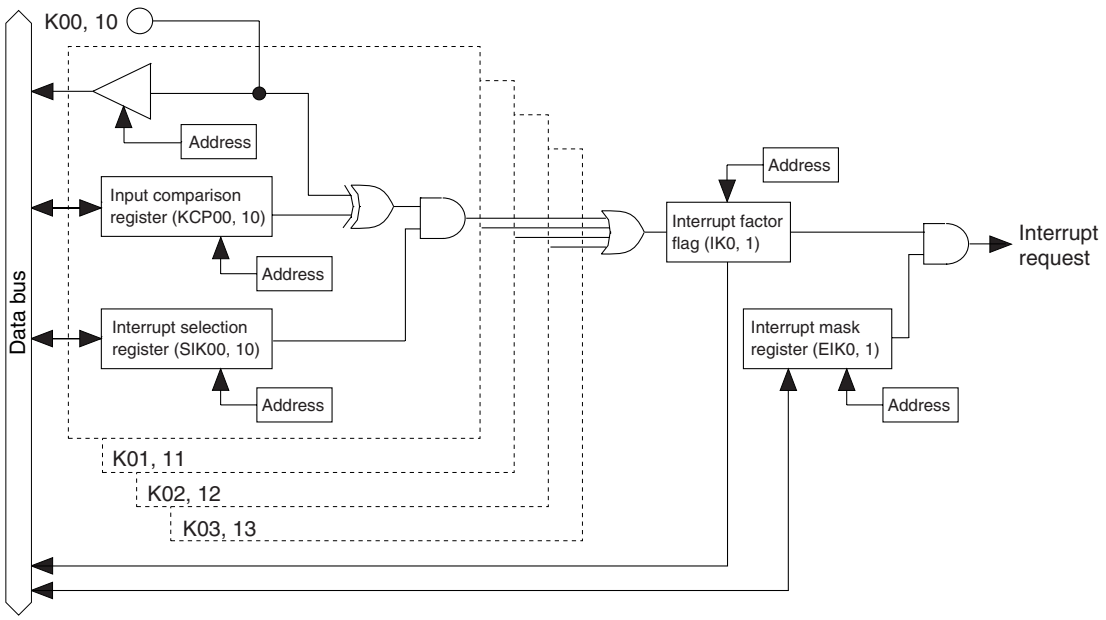


Fig. 4.4.2.1 Input interrupt circuit configuration

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03 and K10–K13, and can specify the terminals for generating interrupt and interrupt timing.
The interrupt selection registers (SIK00–SIK03, SIK10–SIK13) select what input of K00–K03 and K10–K13 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.
The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP00–KCP03, KCP10–KCP13).
By setting these two conditions, the interrupt for K00–K03 or K10–K13 is generated when input ports in which an interrupt has been enabled by the input selection registers and the contents of the input comparison registers have been changed from matching to no matching.
The interrupt mask registers (EIK0, EIK1) enable the interrupt mask to be selected for K00–K03 and K10–K13.
When the interrupt is generated, the interrupt factor flag (IK0, IK1) is set to "1".
Figure 4.4.2.2 shows an example of an interrupt for K00–K03.

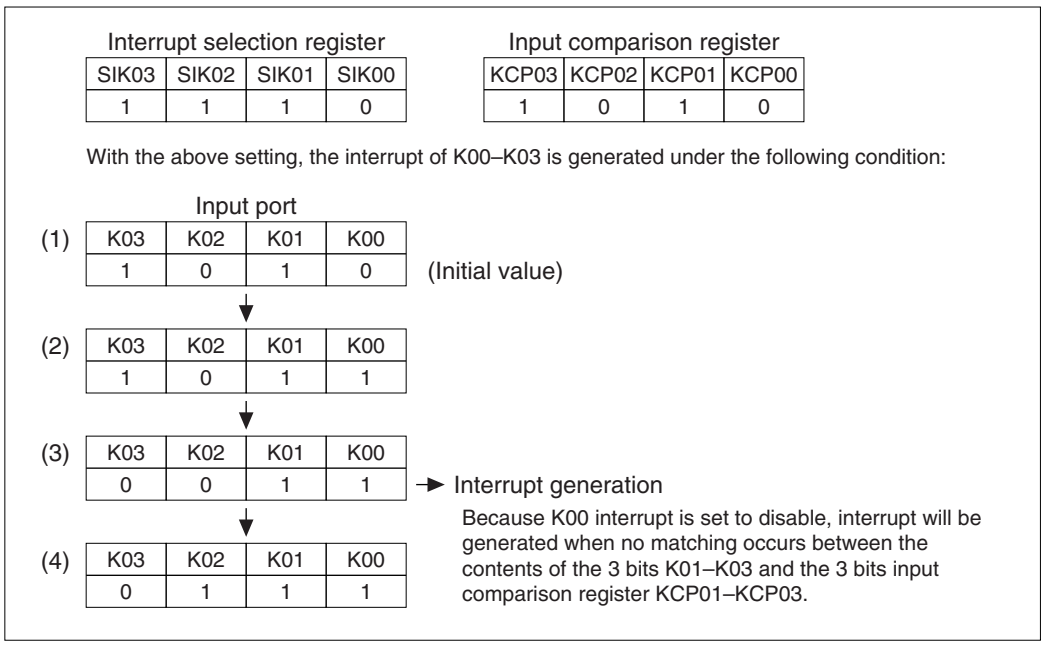


Fig. 4.4.2.2 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminals that are interrupt enabled no longer match the data of the input comparison registers, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison registers from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.4.3 Mask option

Internal pull-down resistor can be selected for each of the eight bits of the input ports (K00–K03, K10–K13) with the input port mask option.
When "Gate direct" is selected, take care that the floating status does not occur for the input. Select "With pull-down resistor" for input ports that are not being used.

4.4.4 I/O memory of input ports

Table 4.4.4.1 shows the I/O addresses and the control bits for the input ports.

Table 4.4.4.1 Control bits of input ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FFE3H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE4H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFF3H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF4H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

K00–K03: K0 port input port data (FF21H)
K10–K13: K1 port input port data (FF25H)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of the eight bits of the input ports (K00–K03, K10–K13) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK03: K0 port interrupt selection register (FF20H)
SIK10–SIK13: K1 port interrupt selection register (FF24H)
Selects the ports to be used for the K00–K03 and K10–K13 input interrupts.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Enables the interrupt for the input ports (K00–K03, K10–K13) for which "1" has been written into the interrupt selection registers (SIK00–SIK03, SIK10–SIK13). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

KCP00–KCP03: K0 port input comparison register (FF22H)
KCP10–KCP13: K1 port input comparison register (FF26H)
Interrupt conditions for terminals K00–K03 and K10–K13 can be set with these registers.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the eight bits (K00–K03 and K10–K13), through the input comparison registers (KCP00–KCP03 and KCP10–KCP13).
For KCP00–KCP03, a comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers. For KCP10–KCP13, a comparison is done only with the ports that are enabled by the interrupt among K10–K13 by means of the SIK10–SIK13 registers.
At initial reset, these registers are set to "1".

EIK0: K0 input interrupt mask register (FFE3H•D0)
EIK1: K1 input interrupt mask register (FFE4H•D0)
Masking the interrupt of the input port can be selected with these registers.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

With these registers, masking of the input port interrupt can be selected for each of the two systems (K00–K03, K10–K13).
At initial reset, these registers are set to "0".

IK0: K0 input interrupt factor flag (FFF3H•D0)
IK1: K1 input interrupt factor flag (FFF4H•D0)
These flags indicate the occurrence of input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.4.5 Programming notes

(1) When input ports are changed from high to low by pull-down resistors, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.5 Output Ports (R00–R03)

4.5.1 Configuration of output ports

The S1C63656 has four bits of general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and P-channel open drain output.
Figure 4.5.1.1 shows the configuration of the output port.

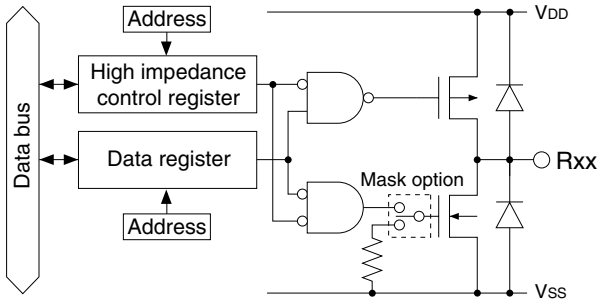


Fig. 4.5.1.1 Configuration of output port

The R02 and R03 output terminals are shared with special output terminals (TOUT, FOUT), and this function is selected by the software.
At initial reset, these are all set to the general purpose output port.
Table 4.5.1.1 shows the setting of the output terminals by function selection.

Table 4.5.1.1 Function setting of output terminals

Terminal name	Terminal status at initial reset	Special output	
		TOUT	FOUT
R00	R00 (Low output)	R00	R00
R01	R01 (Low output)	R01	R01
R02	R02 (Low output)	TOUT	
R03	R03 (Low output)		FOUT

When using the output port (R02, R03) as the special output port, the data register must be fixed at "1" and the high impedance control register must be fixed at "0" (data output).

4.5.2 Mask option

Output specifications of the output ports are selected by mask option.
Either complementary output or P-channel open drain output can be selected individually (in 1-bit units). However, when P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the output port.

4.5.3 High impedance control

The output ports can be set into a high impedance status. This control is done using the high impedance control registers.
The high impedance control registers are provided to correspond with the output ports as shown below.

High impedance control register	Corresponding output port
R00HIZ	R00 (1 bit)
R01HIZ	R01 (1 bit)
R02HIZ	R02 (1 bit)
R03HIZ	R03 (1 bit)

When "1" is written to the high impedance control register, the corresponding output port terminal goes into high impedance status. When "0" is written, the port outputs a signal according to the data register.

4.5.4 Special output

In addition to the regular DC output, special output can be selected for the output ports R02 and R03 as shown in Table 4.5.4.1 with the software.
Figure 4.5.4.1 shows the configuration of the R02 and R03 output ports.

Table 4.5.4.1 Special output

Terminal	Special output	Output control register
R03	FOUT	FOUTE
R02	TOUT	PTOUT

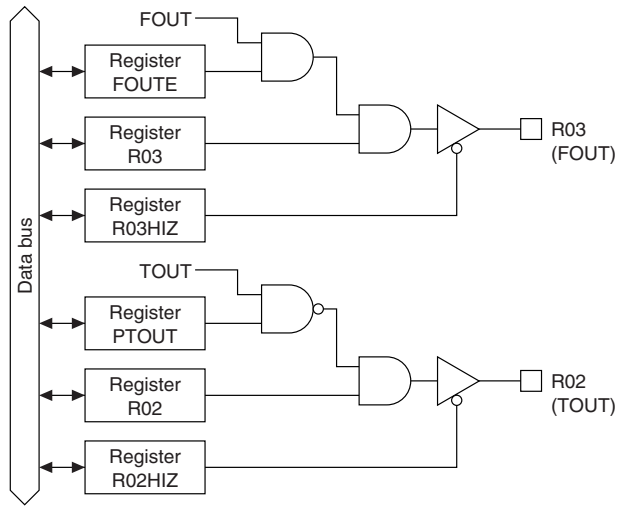


Fig. 4.5.4.1 Configuration of R02 and R03 output ports

At initial reset, the output port data register is set to "0" and the high impedance control register is set to "0". Consequently, the output terminal goes low (VSS).
When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output). The respective signal should be turned on and off using the special output control register.

Note: • Be aware that the output terminal is fixed at a low (VSS) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.

• Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

- **TOUT (R02)**

  The R02 terminal can output a TOUT signal.
  The TOUT signal is the clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.
  To output the TOUT signal, fix the R02 register at "1" and the R02HIZ register at "0", and turn the signal on and off using the PTOUT register. It is, however, necessary to control the programmable timer.
  Refer to Section 4.10, "Programmable Timer" for details of the programmable timer.

Note: A hazard may occur when the TOUT signal is turned on and off.

Figure 4.5.4.2 shows the output waveform of the TOUT signal.

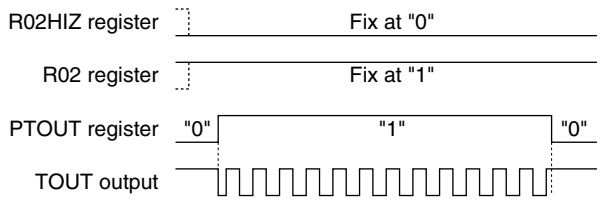


Fig. 4.5.4.2 Output waveform of TOUT signal

- **FOUT (R03)**

  The R03 terminal can output an FOUT signal.
  The FOUT signal is a clock (f_{OSC1} or f_{OSC3}) that is output from the oscillation circuit or a clock that the f_{OSC1} clock has divided in the internal circuit, and can be used to provide a clock signal to an external device.
  To output the FOUT signal, fix the R03 register at "1" and the R03HIZ register at "0", and turn the signal on and off using the FOUTE register.
  The frequency of the output clock may be selected from among 4 types shown in Table 4.5.4.2 by setting the FOFQ0 and FOFQ1 registers.

Table 4.5.4.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$
0	0	$f_{OSC1} \times 1/64$

f_{OSC1}: Clock that is output from the OSC1 oscillation circuit
f_{OSC3}: Clock that is output from the OSC3 oscillation circuit

When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.3, "Oscillation Circuit", for the control and notes.
f_{OSC3} is available when a mask option for using the OSC3 oscillation circuit is selected. If the system uses the OSC1 oscillation circuit only, do not set the FOFQ register to "11".

Note: A hazard may occur when the FOUT signal is turned on and off.

Figure 4.5.4.3 shows the output waveform of the FOUT signal.

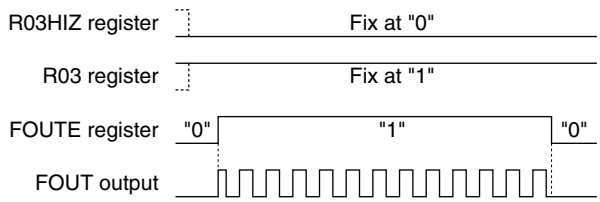


Fig. 4.5.4.3 Output waveform of FOUT signal

4.5.5 I/O memory of output ports

Table 4.5.5.1 shows the I/O addresses and control bits for the output ports.

Table 4.5.5.1 Control bits of output ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					SWDIR	0			Stopwatch direct input switch
	R/W								0: K00=Run/Stop, K01=Lap 1: K00=Lap, K01=Run/Stop
					FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3
					FOFQ0	0			Frequency fOSC1/64 fOSC1/8 fOSC1 fOSC3
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	Hi-Z	Output	R03 (FOUTE=0)/FOUT (FOUTE=1) Hi-Z control
					R02HIZ	0	Hi-Z	Output	R02 (PTOUT=0)/TOUT (PTOUT=1) Hi-Z control
	R/W				R01HIZ	0	Hi-Z	Output	R01 Hi-Z control
					R00HIZ	0	Hi-Z	Output	R00 Hi-Z control
FF31H	R03	R02	R01	R00	R03	0	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used.
					R02	0	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used.
	R/W				R01	0	High	Low	R01 output port data
					R00	0	High	Low	R00 output port data
FFC1H	0	0	CHSEL0	PTOUT	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		CHSEL0	0	Timer 1	Timer 0	TOUT output selection
					PTOUT	0	On	Off	TOUT output control

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

R00HIZ–R03HIZ: R0 port high impedance control register (FF30H)

Controls high impedance output of the output port.

When "1" is written: High impedance
When "0" is written: Data output
Reading: Valid

By writing "0" to the high impedance control register, the corresponding output terminal outputs according to the data register. When "1" is written, it shifts into high impedance status.
When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02HIZ register and the R03HIZ register at "0" (data output).
At initial reset, these registers are set to "0".

R00–R03: R0 output port data register (FF31H)

Set the output data for the output ports.

When "1" is written: High level output
When "0" is written: Low level output
Reading: Valid

The output port terminals output the data written in the corresponding data registers without changing it. When "1" is written to the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02 register and the R03 register at "1".
At initial reset, these registers are all set to "0".

FOUTE: FOUT output control register (FF06H•D3)

Controls the FOUT output.

When "1" is written: FOUT output On
When "0" is written: FOUT output Off
Reading: Valid

By writing "1" to the FOUTE register when the R03 register has been set to "1" and the R03HIZ register has been set to "0", the FOUT signal is output from the R03 terminal. When "0" is written, the R03 terminal goes low (V_{SS}).
When using the R03 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

FOFQ0, FOFQ1: FOUT frequency selection register (FF06H•D0, D1)

Selects a frequency of the FOUT signal.

Table 4.5.5.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$
0	0	$f_{OSC1} \times 1/64$

At initial reset, this register is set to "0".

Note: f_{OSC3} is available when a mask option for using the OSC3 oscillation circuit is selected. If the system uses the OSC1 oscillation circuit only, do not set the FOFQ register to "11".

PTOUT: TOUT output control register (FFC1H•D0)

Controls the TOUT output.

When "1" is written: TOUT output On
When "0" is written: TOUT output Off
Reading: Valid

By writing "1" to the PTOUT register when the R02 register has been set to "1" and the R02HIZ register has been set to "0", the TOUT signal is output from the R02 terminal. When "0" is written, the R02 terminal goes high (V_{DD}).
When using the R02 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

4.5.6 Programming notes

(1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

(2) A hazard may occur when the FOUT signal and the TOUT signal are turned on and off.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output. Refer to Section 4.3, "Oscillation Circuit", for the control and notes.
f_{OSC3} is available when a mask option for using the OSC3 oscillation circuit is selected. If the system uses the OSC1 oscillation circuit only, do not set the FOFQ register to "11".

4.6 I/O Ports (P00–P03 and P10–P13)

4.6.1 Configuration of I/O ports

The S1C63656 has eight bits of general-purpose I/O ports. Figure 4.6.1.1 shows the configuration of the I/O port.

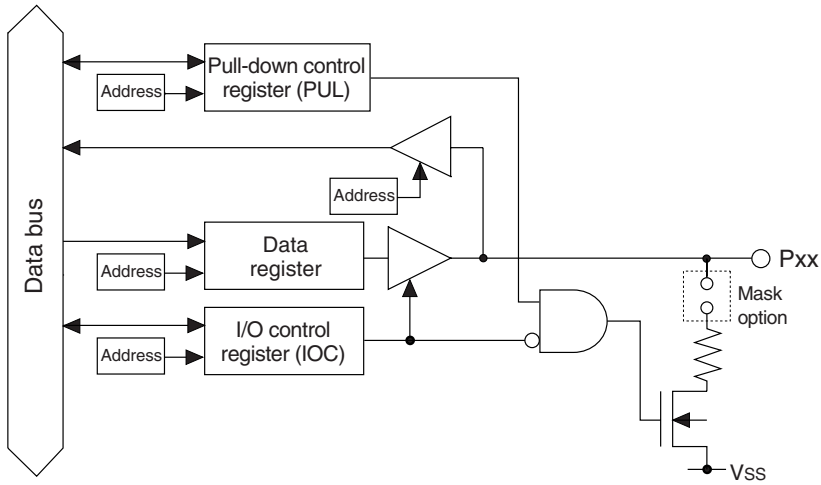


Fig. 4.6.1.1 Configuration of I/O port

The I/O port terminals P10 to P13 are shared with the serial interface input/output terminals. The software can select the function to be used.
At initial reset, these terminals are all set to the I/O port.
Table 4.6.1.1 shows the setting of the input/output terminals by function selection.

Table 4.6.1.1 Function setting of input/output terminals

Terminal	Terminal status at initial reset	Serial I/F	
		Master	Slave
P00–P03	P00–P03 (Input & pull-down *)	P00–P03	P00–P03
P10	P10 (Input & pull-down *)	SIN(I)	SIN(I)
P11	P11 (Input & pull-down *)	SOUT(O)	SOUT(O)
P12	P12 (Input & pull-down *)	SCLK(O)	SCLK(I)
P13	P13 (Input & pull-down *)	P13	SRDY(O)

* When "with pull-down resistor" is selected by the mask option (high impedance when "gate direct" is set)

When these ports are used as I/O ports, the ports can be set to either input mode or output mode individually (in 1-bit unit). Modes can be set by writing data to the I/O control registers.
Refer to Section 4.11, "Serial Interface", for control of the serial interface.

4.6.2 Mask option

The output specification of each I/O port during output mode can be selected from either complementary output or P-channel open drain output by mask option. This selection can be done in 1-bit units. When P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the port.

The mask option also permits selection of whether the pull-down resistor is used or not during input mode. This selection can be done in 1-bit units.
When "without pull-down" during the input mode is selected, take care that the floating status does not occur.

The pull-down resistor for input mode and output specification (complementary output or P-channel open drain output) selected by mask option are effective even when I/O ports are used for input/output of the serial interface.

4.6.3 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the corresponding I/O control registers IOCxx.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull-down explained in the following section has been set by software, the input line is pulled down only during this input mode.

To set the output mode, write "1" is to the I/O control register. When an I/O port is set to output mode, it works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O ports enter the input mode.

The I/O control registers of the ports that are set as input/output for the serial interface can be used as general purpose registers that do not affect the I/O control. (See Table 4.6.1.1.)

4.6.4 Pull-down during input mode

A pull-down resistor that operates during the input mode is built into each I/O port of the S1C63656. Mask option can set the use or non-use of this pull-down.

The pull-down resistor becomes effective by writing "1" to the pull-down control register PULxx that corresponds to each port, and the input line is pulled down during the input mode. When "0" has been written, no pull-down is done.
At initial reset, the pull-down control registers are set to "1".

The pull-down control registers of the ports in which "gate direct" has been selected can be used as general purpose registers.
Even when "with pull-down" has been selected, the pull-down control registers of the ports, that are set as output for the serial interface, can be used as general purpose registers that do not affect the pull-down control. (See Table 4.6.1.1.)
The pull-down control registers of the port, that are set as input for the serial interface, function the same as the I/O port.

4.6.5 I/O memory of I/O ports

Table 4.6.5.1 shows the I/O addresses and the control bits for the I/O ports.

Table 4.6.5.1 Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-down control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-down control register (ESIF=0) functions as a general-purpose register when SIF (master) is selected SCLK (I) pull-down control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-down control register (ESIF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-down control register (ESIF=0) SIN pull-down control register when SIF is selected
FF46H	P13 (XSRDY)	P12 (XSCLK)	P11 (SOUT)	P10 (SIN)	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R	R/W					Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

(1) Selection of port function

ESIF: Serial interface enable register (FF70H•D0)

Selects function for P10–P13.

When "1" is written: Serial interface input/output port
When "0" is written: I/O port
Reading: Valid

When using the serial interface, write "1" to this register and when P10–P13 are used as the I/O port, write "0". The configuration of the terminals within P10–P13 that are used for the serial interface is decided by the mode selected with the SCS1 and SCS0 registers (see Section 4.11).
In the slave mode, all the P10–P13 ports are set to the serial interface input/output port. In the master mode, P10–P12 are set to the serial interface input/output port and P13 can be used as the I/O port. Furthermore, when the SOUT terminal is disabled (ESOUT = "0"), P11 can be used as the I/O port.
At initial reset, this register is set to "0".

(2) I/O port control

P00–P03: P0 I/O port data register (FF42H)
P10–P13: P1 I/O port data register (FF46H)

I/O port data can be read and output data can be set through these registers.

• ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the terminal goes low (V_{SS}).
Port data can be written also in the input mode.

• ***When reading data***

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When "with pull-down resistor" has been selected with the mask option and the PUL register is set to "1", the built-in pull-down resistor goes on during input mode, so that the I/O port terminal is pulled down.

The data registers of the port, which are set for the input/output of the serial interface (P10–P13), become general-purpose registers that do not affect the input/output.

Note: When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

IOC00–IOC03: P0 port I/O control register (FF40H)
IOC10–IOC13: P1 port I/O control register (FF44H)

The input and output modes of the I/O ports are set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are all set to "0", so the I/O ports are in the input mode.
The I/O control registers of the port, which are set for the input/output of the serial interface (P10–P13), become general-purpose registers that do not affect the input/output.

PUL00–PUL03: P0 port pull-down control register (FF41H)
PUL10–PUL13: P1 port pull-down control register (FF45H)

The pull-down during the input mode are set with these registers.

When "1" is written: Pull-down On
When "0" is written: Pull-down Off
Reading: Valid

The built-in pull-down resistor which is turned on during input mode is set to enable in 1-bit units. (The pull-down resistor is included into the ports selected by mask option.)
By writing "1" to the pull-down control register, the corresponding I/O ports are pulled down (during input mode), while writing "0" disables the pull-down function.
At initial reset, these registers are all set to "1", so the pull-down function is enabled.

The pull-down control registers of the ports in which the pull-down resistor is not included become the general purpose register. The registers of the ports that are set as output for the serial interface can also be used as general purpose registers that do not affect the pull-down control.
The pull-down control registers of the port that are set as input for the serial interface function the same as the I/O port.

4.6.6 Programming note

When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

4.7 LCD Driver (COM0–COM3, SEG0–SEG37)

4.7.1 Configuration of LCD driver

The S1C63656 has four common terminals (COM0–COM3) and 38 segment terminals (SEG0–SEG37), so that it can drive an LCD with a maximum of 152 (38 × 4) segments.
The driving method is 1/4 duty or 1/3 duty dynamic drive with three voltages (1/3 bias), V_{C1}, V_{C2} and V_{C3}.
LCD display on/off can be controlled by the software.

4.7.2 Power supply for LCD driving

The power supply for driving LCD can be selected from the internal power supply and an external power supply.

When the internal power supply is selected, the LCD drive voltages V_{C1}–V_{C3} are generated by the built-in LCD system voltage circuit. The LCD system voltage circuit is turned on and off using the LPWR register. When LPWR is set to "1", the LCD system voltage circuit outputs the LCD drive voltages V_{C1}–V_{C3} to the LCD driver. The LCD system voltage circuit generates V_{C1} with the voltage regulator built-in, and generates two other voltages ($V_{C2} = 2V_{C1}$, $V_{C3} = 3V_{C1}$) by boosting V_{C1}.

When using an external power supply, select the voltage from the following 3 types and supply the LCD drive voltage to the V_{C1}–V_{C3} terminals.
1) External power supply 1/3 bias (for 4.5 V panel) $V_{DD} = V_{C2}$
2) External power supply 1/3 bias (for 3.0 V panel) $V_{DD} = V_{C3}$
3) External power supply 1/2 bias (for 3.0 V panel) $V_{DD} = V_{C3}$, $V_{C1} = V_{C2}$ (static drive function is available)

Note that the power control using the LPWR register is necessary even if an external power supply is used. SEG output ports that are set for DC output by the mask option operate same as the output (R) port regardless of the power on/off control by the LPWR register.

4.7.3 Control of LCD display and drive waveform

(1) Display on/off control

The S1C63656 incorporates the ALON and ALOFF registers to blink display. When "1" is written to ALON, all the segments go on, and when "1" is written to ALOFF, all the segments go off. At such a time, an on waveform or an off waveform is output from SEG terminals. When "0" is written to these registers, normal display is performed. Furthermore, when "1" is written to both of the ALON and ALOFF, ALON (all on) has priority over the ALOFF (all off).

(2) Setting of drive duty

In the S1C63656, the drive duty can be set to 1/4 or 1/3 using the LDUTY1 and LDUTY0 registers as shown in Table 4.7.3.1.

Table 4.7.3.1 LCD drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	1	1/3	COM0–COM2	114 (38 × 3)
1	0	–	–	–
0	1	–	–	–
0	0	1/4	COM0–COM3	152 (38 × 4)

Table 4.7.3.2 shows the frame frequency corresponding to the drive duty.

Table 4.7.3.2 Frame frequency

OSC1 oscillation frequency	When 1/3 duty is selected	When 1/4 duty is selected
32.768 kHz	42.7 Hz	32 Hz

Figures 4.7.3.1 and 4.7.3.2 show the dynamic drive waveform according to the duty.

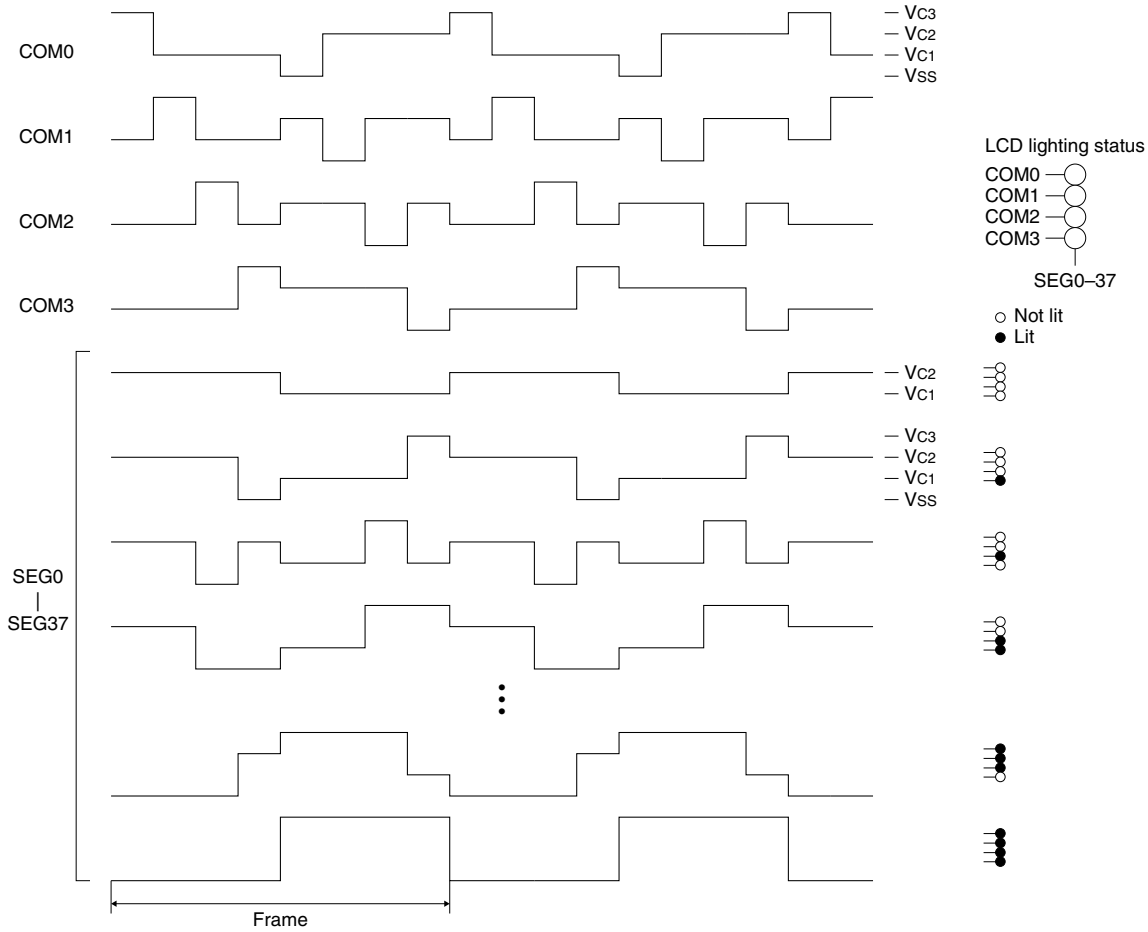


Fig. 4.7.3.1 Dynamic drive waveform for 1/4 duty

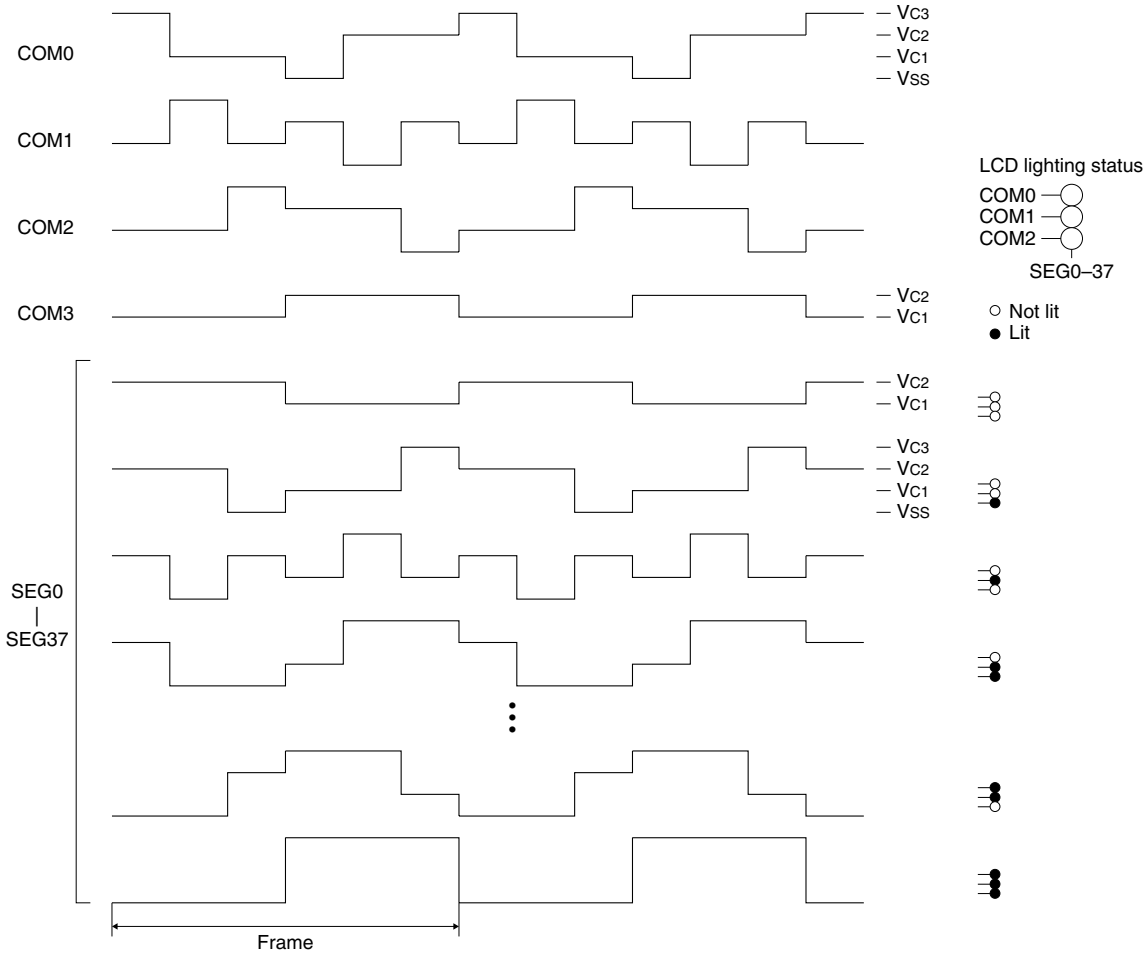


Fig. 4.7.3.2 Dynamic drive waveform for 1/3 duty

(3) Static drive

The S1C63656 provides software setting of the LCD static drive. However, this function is available only when "External power supply 1/2 bias (for 3.0 V panel)" is selected by mask option.
To set in static drive, write "1" to the common output signal control register STCD. Then, by writing "1" to any one of COM0 to COM3 (display memory) corresponding to the SEG terminal, the SEG terminal outputs a static on waveform. When all the COM0 to COM3 bits are set to "0", the SEG terminal outputs a dynamic off waveform.
Figure 4.7.3.3 shows the static drive waveform.

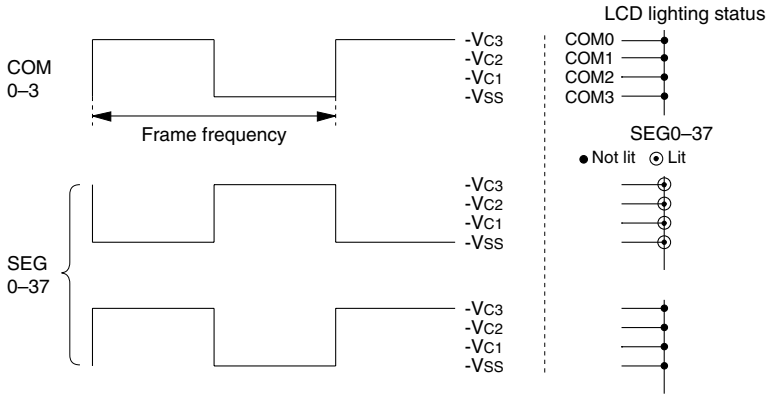


Fig. 4.7.3.3 Static drive waveform

Note: To use the static drive function, select the "External power supply 1/2 bias (for 3.0 V panel)" mask option. When an option for using the internal power supply or a 1/3 bias external power supply is selected, static drive cannot be set using the STCD register.

4.7.4 Display memory

The display memory is allocated to F000H–F02FH in the data memory area and each data bit can be allocated to an segment terminal (SEG0–SEG37) by mask option.
When a bit in the display memory is set to "1", the corresponding LCD segment goes on, and when it is set to "0", the segment goes off.
At initial reset, the data memory content becomes undefined hence, there is need to initialize using the software.
The display memory has read/write capability, and the addresses that have not been used for LCD display can be used as general purpose registers.

4.7.5 Segment option

Segment allocation

The LCD driver has a segment decoder built-in, and the data bit (D0–D3) of the optional address in the display memory area (F000H–F02FH) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.
Figure 4.7.5.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/4 duty.

Address	Data			
	D3	D2	D1	D0
F020H	d	c	b	a
F021H	p	g	f	e

Display memory allocation

	Common 0	Common 1	Common 2	Common 3
SEG10	21, D1 (f)	21, D0 (e)	20, D2 (c)	20, D3 (d)
SEG11	20, D0 (a)	21, D2 (g)	20, D1 (b)	21, D3 (p)

Pin address allocation

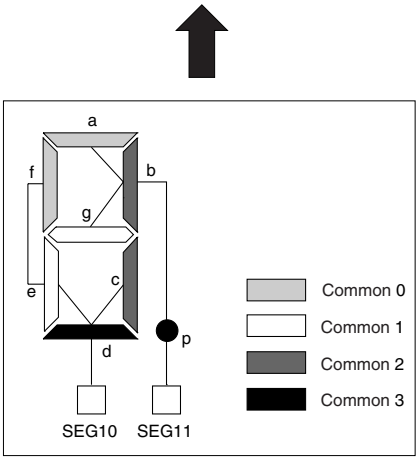


Fig. 4.7.5.1 Segment allocation

Output specification

1. The segment terminals (SEG0–SEG37) can be selected with the mask option in pairs* for either segment signal output or DC output (V_{DD} and V_{SS} binary output).
   When DC output is selected, the data corresponding to COM0 of each segment terminal is output.
2. When DC output is selected, either complementary output or N-channel open drain output can be selected for each terminal with the mask option.

* The terminal pairs are combination of SEG2 × n and SEG2 × n + 1 (where n is an integer from 0 to 18).

Segment option list

Pin name	Address (F0xx)												Output specification
	COM0			COM1			COM2			COM3			
	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0													SEG output ☐ S
SEG1													DC output ☐ C ☐ N
SEG2													SEG output ☐ S
SEG3													DC output ☐ C ☐ N
SEG4													SEG output ☐ S
SEG5													DC output ☐ C ☐ N
SEG6													SEG output ☐ S
SEG7													DC output ☐ C ☐ N
SEG8													SEG output ☐ S
SEG9													DC output ☐ C ☐ N
SEG10													SEG output ☐ S
SEG11													DC output ☐ C ☐ N
SEG12													SEG output ☐ S
SEG13													DC output ☐ C ☐ N
SEG14													SEG output ☐ S
SEG15													DC output ☐ C ☐ N
SEG16													SEG output ☐ S
SEG17													DC output ☐ C ☐ N
SEG18													SEG output ☐ S
SEG19													DC output ☐ C ☐ N
SEG20													SEG output ☐ S
SEG21													DC output ☐ C ☐ N
SEG22													SEG output ☐ S
SEG23													DC output ☐ C ☐ N
SEG24													SEG output ☐ S
SEG25													DC output ☐ C ☐ N
SEG26													SEG output ☐ S
SEG27													DC output ☐ C ☐ N
SEG28													SEG output ☐ S
SEG29													DC output ☐ C ☐ N
SEG30													SEG output ☐ S
SEG31													DC output ☐ C ☐ N
SEG32													SEG output ☐ S
SEG33													DC output ☐ C ☐ N
SEG34													SEG output ☐ S
SEG35													DC output ☐ C ☐ N
SEG36													SEG output ☐ S
SEG37													DC output ☐ C ☐ N

<address> H: RAM data high-order address (0–9)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

4.7.6 LCD contrast adjustment

When "Internal power supply (normal mode)" is selected by mask option for the LCD drive power, software can adjust the LCD contrast.
It is realized by controlling the voltages V_{C1}, V_{C2} and V_{C3} output from the LCD system voltage circuit. The contrast can be adjusted to 16 levels as shown in Table 4.7.6.1. V_{C1} is changed within the range from 1.03 to 1.40 V, and other voltages change according to V_{C1}.

Table 4.7.6.1 LCD contrast

No.	LC3	LC2	LC1	LC0	V_{C1} (V)	Contrast
0	0	0	0	0	1.03	light
1	0	0	0	1	1.06	↑
2	0	0	1	0	1.09	
3	0	0	1	1	1.12	
4	0	1	0	0	1.15	
5	0	1	0	1	1.18	
6	0	1	1	0	1.20	
7	0	1	1	1	1.23	
8	1	0	0	0	1.26	
9	1	0	0	1	1.28	
10	1	0	1	0	1.30	
11	1	0	1	1	1.32	
12	1	1	0	0	1.34	
13	1	1	0	1	1.36	
14	1	1	1	0	1.38	↓
15	1	1	1	1	1.40	dark

At initial reset, the LC0–LC3 are set to 0000B. The software should initialize the register to get the desired contrast.
When an external power supply is selected by mask option, the LC0–LC3 register becomes invalid. Furthermore, the contrast adjustment function cannot be used when "Internal power supply (low-power mode)" is selected. Setting the above register is ignored.
In this case, the V_{C1} voltage is fixed at 0.98 V (Typ.).

4.7.7 I/O memory of LCD driver

Table 4.7.7.1 shows the I/O addresses and the control bits for the LCD driver. Figure 4.7.7.1 shows the display memory map.

Table 4.7.7.1 Control bits of LCD driver

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF60H	LDUTY1	LDUTY0	STCD	LPWR	LDUTY1	0			LCD drive duty switch: [LDUTY1, 0] 0 (Duty 1/4), 1,2 (–), 3 (1/3)
					LDUTY0	0			
	R/W				STCD	0	Static	Dynamic	LCD drive switch
					LPWR	0	On	Off	LCD power On/Off
FF61H	0	ALOFF	ALON	0	0 *3	– *2			Unused
					ALOFF	1	All Off	Normal	LCD all Off control
	R	R/W		R	ALON	0	All On	Normal	LCD all On control
					0 *3	– *2			Unused
FF62H	LC3	LC2	LC1	LC0	LC3	0			LCD contrast adjustment: [LC3–0] 0 (Contrast Light) – 15 (Dark)
	R/W				LC2	0			
					LC1	0			
					LC0	0			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Address Base \ Low	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F000H	Display memory (48 words × 4 bits) R/W															
F010H																
F020H																

Fig. 4.7.7.1 Display memory map

LPWR: LCD power control (on/off) register (FF60H•D0)

Turns the LCD system voltage circuit on and off.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to the LPWR register, the LCD system voltage circuit goes on and generates the LCD drive voltage. When "0" is written, all the LCD drive voltages go to VSS level.
It takes about 100 msec for the LCD drive voltage to stabilize after starting up the LCD system voltage circuit by writing "1" to the LPWR register.
This control does not affect to SEG terminals that have been set for DC output.
At initial reset, this register is set to "0".

LDUTY0, LDUTY1: LCD drive duty switching register (FF60H•D2, D3)

Selects the LCD drive duty.

Table 4.7.7.2 Drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	1	1/3	COM0–COM2	114 (38 × 3)
1	0	–	–	–
0	1	–	–	–
0	0	1/4	COM0–COM3	152 (38 × 4)

At initial reset, this register is set to "0".

STCD: LCD drive switch register (FF60H•D1)

Switches the LCD driving method.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Reading: Valid

By writing "1" to STCD, static drive is selected, and dynamic drive is selected when "0" is written.
At initial reset, this register is set to "0".

ALON: LCD all on control register (FF61H•D1)

Displays the all LCD segments on.

When "1" is written: All LCD segments displayed
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALON register, all the LCD segments go on, and when "0" is written, it returns to normal display. This function outputs an on waveform to the SEG terminals, and segments not affect the content of the display memory. ALON has priority over ALOFF.
At initial reset, this register is set to "0".

ALOFF: LCD all OFF control register (FF61H•D2)

Fade outs the all LCD segments.

When "1" is written: All LCD segments fade out
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALOFF register, all the LCD segments go off, and when "0" is written, it returns to normal display. This function outputs an off waveform to the SEG terminals, and does not affect the content of the display memory.
ALON (FF61H•D1) has priority over ALOFF, so all the LCD segments go on when ALON and ALOFF are set to "1" simultaneously.
At initial reset, this register is set to "1".

LC3–LC0: LCD contrast adjustment register (FF62H)

Adjusts the LCD contrast.

LC3–LC0 = 0000B light
: :
LC3–LC0 = 1111B dark

When the LCD drive voltage is supplied from outside by mask option selection, this adjustment becomes invalid. Furthermore, the contrast adjustment function cannot be used when "Internal power supply (low-power mode)" is selected. Setting of this register is ignored.
At initial reset, LC0–LC3 is set to 0000B.

4.7.8 Programming note

Because at initial reset, the contents of display memory are undefined and LC3–LC0 (LCD contrast) is set to 0000B, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes off.

4.8 Clock Timer

4.8.1 Configuration of clock timer

The S1C63656 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of an 8-bit binary counter that serves as the input clock, fOSC1 divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.8.1.1 is the block diagram for the clock timer.

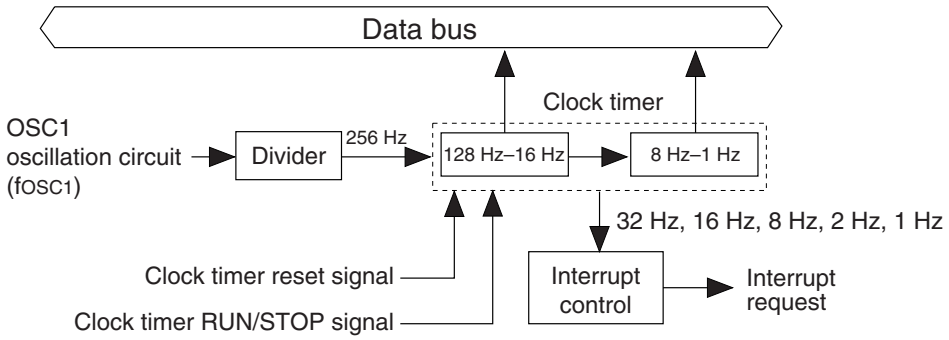


Fig. 4.8.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

4.8.2 Data reading and hold function

The 8 bits timer data are allocated to the address FF75H and FF76H.

<FF75H>	D0: TM0 = 128 Hz	D1: TM1 = 64 Hz	D2: TM2 = 32 Hz	D3: TM3 = 16 Hz
<FF76H>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the S1C63656 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (Varies due to the read timing.)

Note: Since the low-order data is not held when the high-order data has previously been read, the low-order data should be read first.

4.8.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz, 2 Hz, 1 Hz and 16 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.8.3.1 is the timing chart of the clock timer.

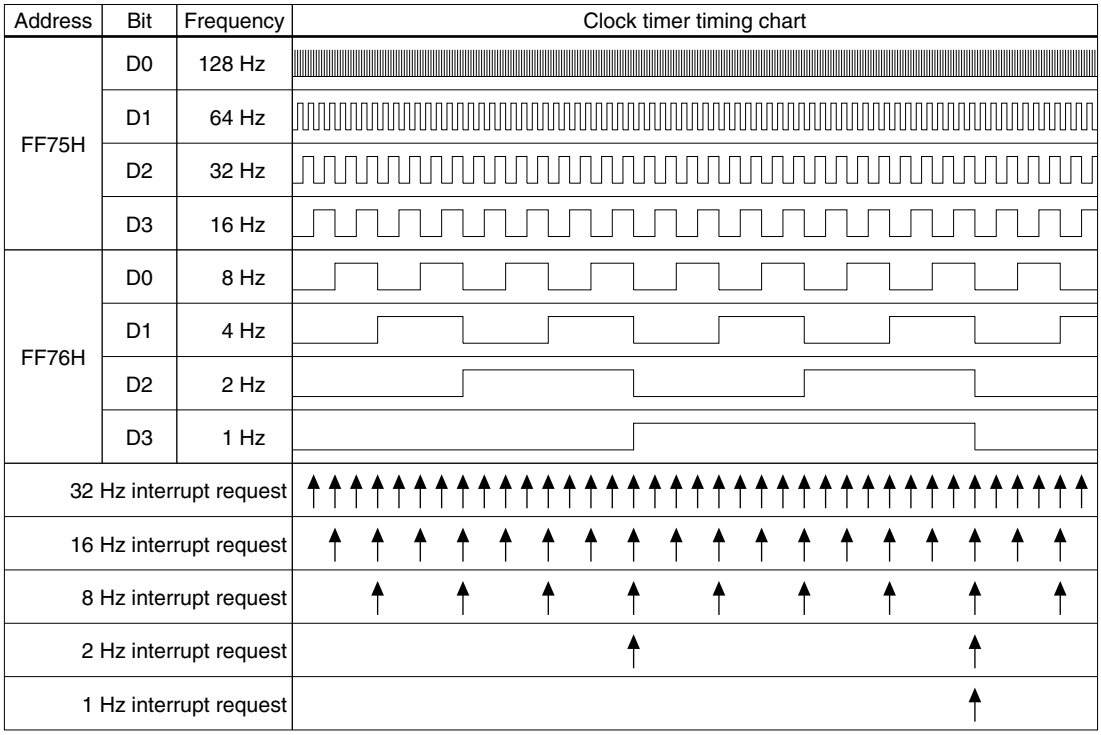


Fig. 4.8.3.1 Timing chart of clock timer

As shown in Figure 4.8.3.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz, 16 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3, IT4) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3, EIT4). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.8.4 I/O memory of clock timer

Table 4.8.4.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.8.4.1 Control bits of clock timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF74H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF75H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF76H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFE5H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE9H	0	0	0	EIT4	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIT4	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFF5H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF9H	0	0	0	IT4	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IT4	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

TM0–TM7: Timer data (FF75H, FF76H)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.

By reading the low-order data (FF75H), the high-order data (FF76H) is held until reading or for 0.48–1.5 msec (one of shorter of them).

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (FF74H•D1)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.

This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP control register (FF74H•D0)

Controls RUN/STOP of the clock timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The clock timer enters the RUN status when "1" is written to the TMRUN register, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.
At initial reset, this register is set to "0".

EIT0: 32 Hz interrupt mask register (FFE5H•D0)
EIT1: 8 Hz interrupt mask register (FFE5H•D1)
EIT2: 2 Hz interrupt mask register (FFE5H•D2)
EIT3: 1 Hz interrupt mask register (FFE5H•D3)
EIT4: 16 Hz interrupt mask register (FFE9H•D0)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3, EIT4) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz, 16 Hz).
At initial reset, these registers are set to "0".

IT0: 32 Hz interrupt factor flag (FFF5H•D0)
IT1: 8 Hz interrupt factor flag (FFF5H•D1)
IT2: 2 Hz interrupt factor flag (FFF5H•D2)
IT3: 1 Hz interrupt factor flag (FFF5H•D3)
IT4: 16 Hz interrupt factor flag (FFF9H•D0)

These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3, IT4) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz, 16 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.8.5 Programming notes

(1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.9 Stopwatch Timer

4.9.1 Configuration of stopwatch timer

The S1C63656 has a 1/1,000 sec stopwatch timer. The stopwatch timer is configured of a 3-stage, 4-bit BCD counter serving as the input clock of a 1,000 Hz signal output from the prescaler. Data can be read out four bits (1/1,000 sec, 1/100 sec and 1/10 sec) at a time by the software.
In addition it has a direct input function that controls the stopwatch timer RUN/STOP and LAP using the input ports K00 and K01.
Figure 4.9.1.1 is the block diagram of the stopwatch timer.

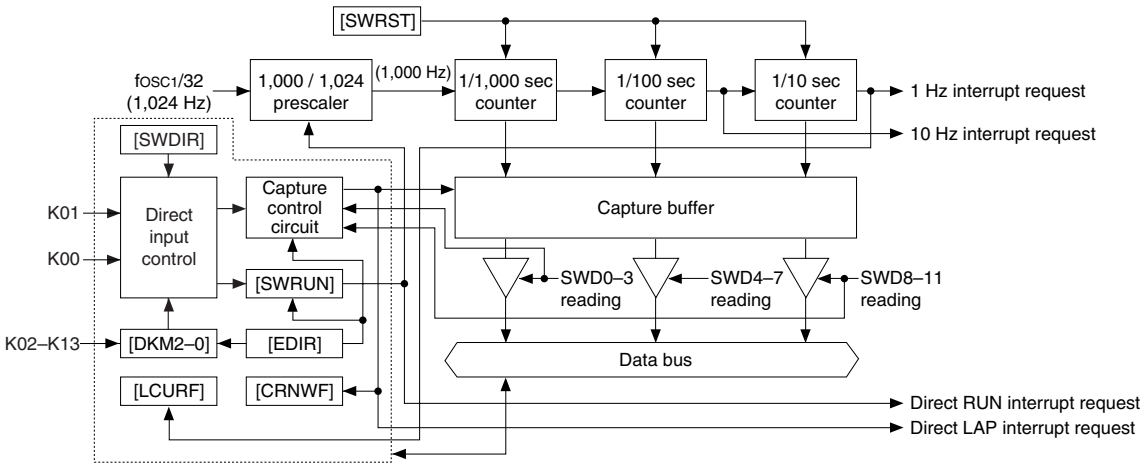


Fig. 4.9.1.1 Block diagram of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

4.9.2 Counter and prescaler

The stopwatch timer is configured of four-bit BCD counters SWD0–3, SWD4–7 and SWD8–11.
The counter SWD0–3, at the stage preceding the stopwatch timer, has a 1,000 Hz signal generated by the prescaler for the input clock. It counts up every 1/1,000 sec, and generates 100 Hz signal. The counter SWD4–7 has a 100 Hz signal generated by the counter SWD0–3 for the input clock. It count-up every 1/100 sec, and generated 10 Hz signal. The counter SWD8–11 has an approximated 10 Hz signal generated by the counter SWD4–7 for the input clock. It count-up every 1/10 sec, and generated 1 Hz signal.

The prescaler inputs a 1,024 Hz clock dividing fOSC1 (output from the OSC1 oscillation circuit), and outputs 1,000 Hz counting clock for SWD0–3. To generate a 1,000 Hz clock from 1,024 Hz, 24 pulses from 1,024 pulses that are input to the prescaler every second are taken out.
When the counter becomes the value indicated below, one pulse (1,024 Hz) that is input immediately after to the prescaler will be pulled out.

<Counter value (msec) in which the pulse correction is performed>
39, 79, 139, 179, 219, 259, 299, 319, 359, 399, 439, 479, 539, 579, 619, 659, 699, 719, 759, 799, 839, 879, 939, 979

Figure 4.9.2.1 shows the operation of the prescaler.

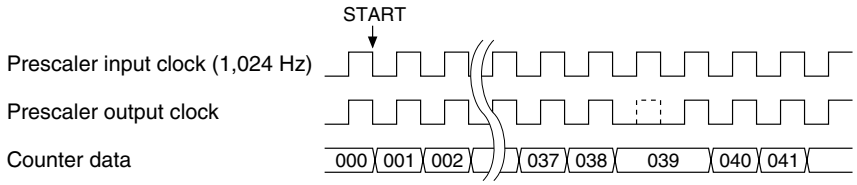


Fig. 4.9.2.1 Timing of the prescaler operation

For the above reason, the counting clock is 1,024 Hz (0.9765625 msec) except during pulse correction. Consequently, frequency of the prescaler output clock (1,000 Hz), 100 Hz generated by SWD0–3 and 10 Hz generated by SWD4–7 are approximate values.

4.9.3 Capture buffer and hold function

The stopwatch data, 1/1,000 sec, 1/100 sec and 1/10 sec, can be read from SWD0–3 (FF7AH), SWD4–7 (FF7BH) and SWD8–11 (FF7CH), respectively. The counter data are latched in the capture buffer when reading, and are held until reading of three words is completed. For this reason, correct data can be read even when a carry from lower digits occurs during reading the three words. Further, three counter data are latched in the capture buffer at the same time when SWD0–3 (1/1,000 sec) is read. The data hold is released when SWD8–11 (1/10 sec) reading is completed. Therefore, data should be read in order of SWD0–3 → SWD4–7 → SWD8–11. If SWD4–7 or SWD8–11 is first read when data have not been held, the hold function does not work and data in the counter is directly read out. When data that has not been held is read in the stopwatch timer RUN status, you cannot judge whether it is correct or not.

The stopwatch timer has a LAP function using an external key input (explained later). The capture buffer is also used to hold LAP data. In this case, data is held until SWD8–11 is read. However, when a LAP input is performed before completing the reading, the content of the capture buffer is renewed at that point. Remaining data that have not been read become invalid by the renewal, and the hold status is not released if SWD8–11 is read. When SWD8–11 is read after the capture buffer is updated, the capture renewal flag is set to "1" at that point. In this case, it is necessary to read from SWD0–3 again. The capture renewal flag is renewed by reading SWD8–11.

Figure 4.9.3.1 shows the timing for data holding and reading.

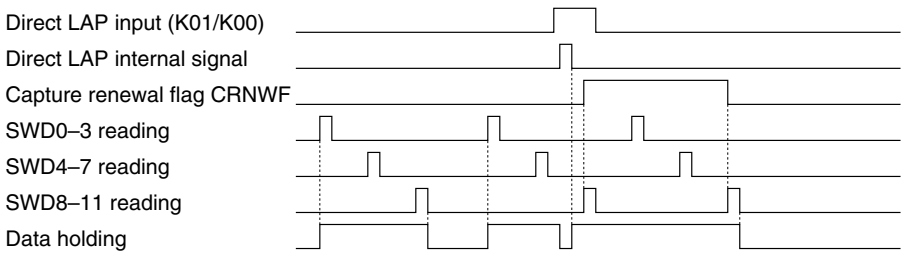


Fig. 4.9.3.1 Timing for data holding and reading

4.9.4 Stopwatch timer RUN/STOP and reset

RUN/STOP control and reset of the stopwatch timer can be done by the software.

Stopwatch timer RUN/STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count. The RUN/STOP operation of the stopwatch timer by writing to the SWRUN register is performed in synchronization with the falling edge of the 1,024 Hz same as the prescaler input clock. The SWRUN register can be read, and in this case it indicates the operating status of the stopwatch timer.

Figure 4.9.4.1 shows the operating timing when controlling the SWRUN register.

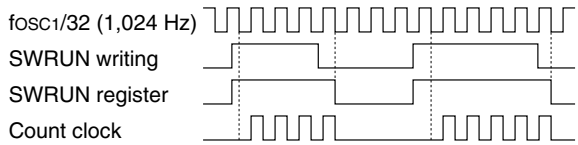


Fig. 4.9.4.1 Operating timing when controlling SWRUN

When the direct input function (explained in next section) is set, RUN/STOP control is done by an external key input. In this case, SWRUN becomes read only register that indicates the operating status of the stopwatch timer.

Stopwatch timer reset

The stopwatch timer is reset when "1" is written to SWRST. With this, the counter value is cleared to "000". Since this resetting does not affect the capture buffer, data that has been held in the capture buffer is not cleared and is maintained as is. When the stopwatch timer is reset in the RUN status, counting restarts from count "000". Also, in the STOP status the reset data "000" is maintained until the next RUN.

4.9.5 Direct input function and key mask

The stopwatch timer has a direct input function that can control the RUN/STOP and LAP operation of the stopwatch timer by external key input. This function is set by writing "1" to the EDIR register. When EDIR is set to "0", only the software control is possible as explained in the previous section.

Input port configuration

In the direct input function, the input ports K00 and K01 are used as the RUN/STOP and LAP input ports. The key assignment can be selected using the SWDIR register.

Table 4.9.5.1 RUN/STOP and LAP input ports

SWDIR	K00	K01
0	RUN/STOP	LAP
1	LAP	RUN/STOP

Direct RUN

When the direct input function is selected, RUN/STOP operation of the stopwatch timer can be controlled by using the key connected to the input port K00/K01 (selected by SWDIR). K00/K01 works as a normal input port, but the input signal is sent to the stopwatch control circuit. The key input signal from the K00/K01 port works as a toggle switch. When it is input in STOP status, the stopwatch timer runs, and in RUN status, the stopwatch timer stops. RUN/STOP status of the stopwatch timer can be checked by reading the SWRUN register. An interrupt is generated by direct RUN input.

The sampling for key input signal is performed at the falling edge of 1,024 Hz signal same as the SWRUN control. The chattering judgment is performed at the point where the key turns off, and a chattering less than 46.8–62.5 msec is removed. Therefore, more time is needed for an interval between RUN and STOP key inputs.

Figure 4.9.5.1 shows the operating timing for the direct RUN input.

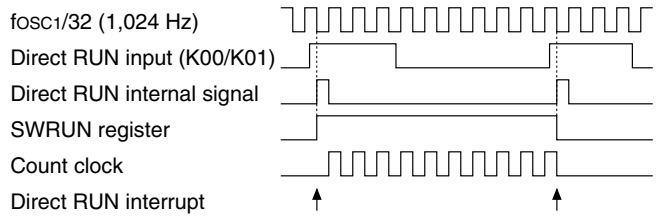


Fig. 4.9.5.1 Operating timing for direct RUN input

Direct LAP

Control for the LAP can also be done by key input same as the direct RUN. When the direct input function is selected, the input port K01/K00 (selected by SWDIR) becomes the LAP key input port. Sampling for the input signal and the chattering judgment are the same as a direct RUN.
By entering the LAP key, the counter data at that point is latched into the capture buffer and is held. The counter continues counting operation. Furthermore, an interrupt occurs by direct LAP input.
As stated above, the capture buffer data is held until SWD8–11 is read. If the LAP key is input when data has been already held, it renews the content of the capture buffer. When SWD8–11 is read after renewing, the capture renewal flag is set to "1". In this case, the hold status is not released by reading SWD8–11, and it continues. Normally the LAP data should be read after the interrupt is generated. After that, be sure to check the capture renewal flag. When the capture renewal flag is set, renewed data is held in the capture buffer. So it is necessary to read from SWD0–3 again.
The stopwatch timer sets the 1 Hz interrupt factor flag ISW1 to "1" when requiring a carry-up to 1-sec digit by an SWD8–11 overflow. If the capture buffer shifts into hold status (when SWD0–3 is read or when LAP is input) while the 1 Hz interrupt factor flag ISW1 is set to "1", the lap data carry-up request flag LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required for the processing of LAP input. In normal software processing, LAP processing may take precedence over 1-sec or higher digits processing by a 1 Hz interrupt, therefore carry-up processing using this flag should be used for time display in the LAP processing to prevent the 1-sec digit data decreasing by 1 second. This flag is renewed when the capture buffer shifts into hold status.
Figure 4.9.5.2 shows the operating timing for the direct LAP input, and Figure 4.9.5.3 shows the timings for data holding and reading during a direct LAP input and reading.

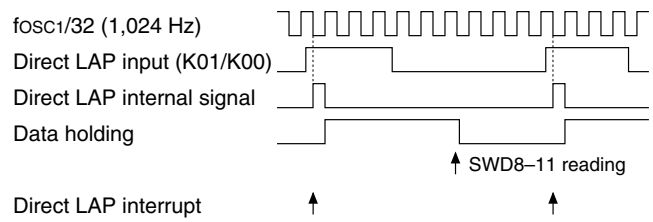


Fig. 4.9.5.2 Operating timing for direct LAP input

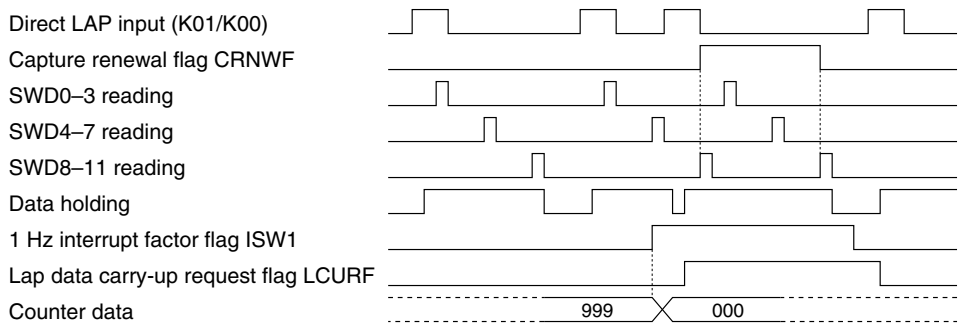


Fig. 4.9.5.3 Timing for data holding and reading during direct LAP input

Key mask

In stopwatch applications, some functions may be controlled by a combination of keys including direct RUN or direct LAP. For instance, the RUN key can be used for other functions, such as reset and setting a watch, by pressing the RUN key with another key. In this case, the direct RUN function or direct LAP function must be invalid so that it does not function. For this purpose, the key mask function is set so that it judges concurrence of input keys and invalidates RUN and LAP functions. A combination of the key inputs for this judgment can be selected using the DKM0–DKM2 registers.

Table 4.9.5.2 Key mask selection

DKM2	DKM1	DKM0	Mask key combination
0	0	0	None (at initial reset)
0	0	1	K02
0	1	0	K02, K03
0	1	1	K02, K03, K10
1	0	0	K10
1	0	1	K10, K11
1	1	0	K10, K11, K12
1	1	1	K10, K11, K12, K13

RUN or LAP inputs become invalid in the following status.

1. The RUN or LAP key is pressed when one or more keys that are included in the selected combination (here in after referred to as mask) are held down.
2. The RUN or LAP key has been pressed when the mask is released.

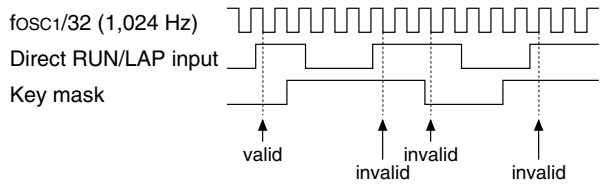


Fig. 4.9.5.4 Operation of key mask

RUN or LAP inputs become valid in the following status.

1. Either the RUN or LAP key is pressed independently if no other key is been held down.
2. Both the RUN and LAP keys are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)
3. The RUN or LAP key is pressed if either is held down. (RUN and LAP functions are effective.)
4. Either the RUN or LAP key and the mask key are pressed at the same time if no other key is held down.
5. Both the RUN and LAP keys and the mask key are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)

* Simultaneous key input is referred to as two or more key inputs are sampled at the same falling edge of 1,024 Hz clock.

4.9.6 Interrupt function

10 Hz and 1 Hz interrupts

The 10 Hz and 1 Hz interrupts can be generated through the overflow of stopwatch timers SWD4–7 and SWD8–11 respectively. Also, software can set whether to separately mask the frequencies described earlier.

Figure 4.9.6.1 is the timing chart for the counters.

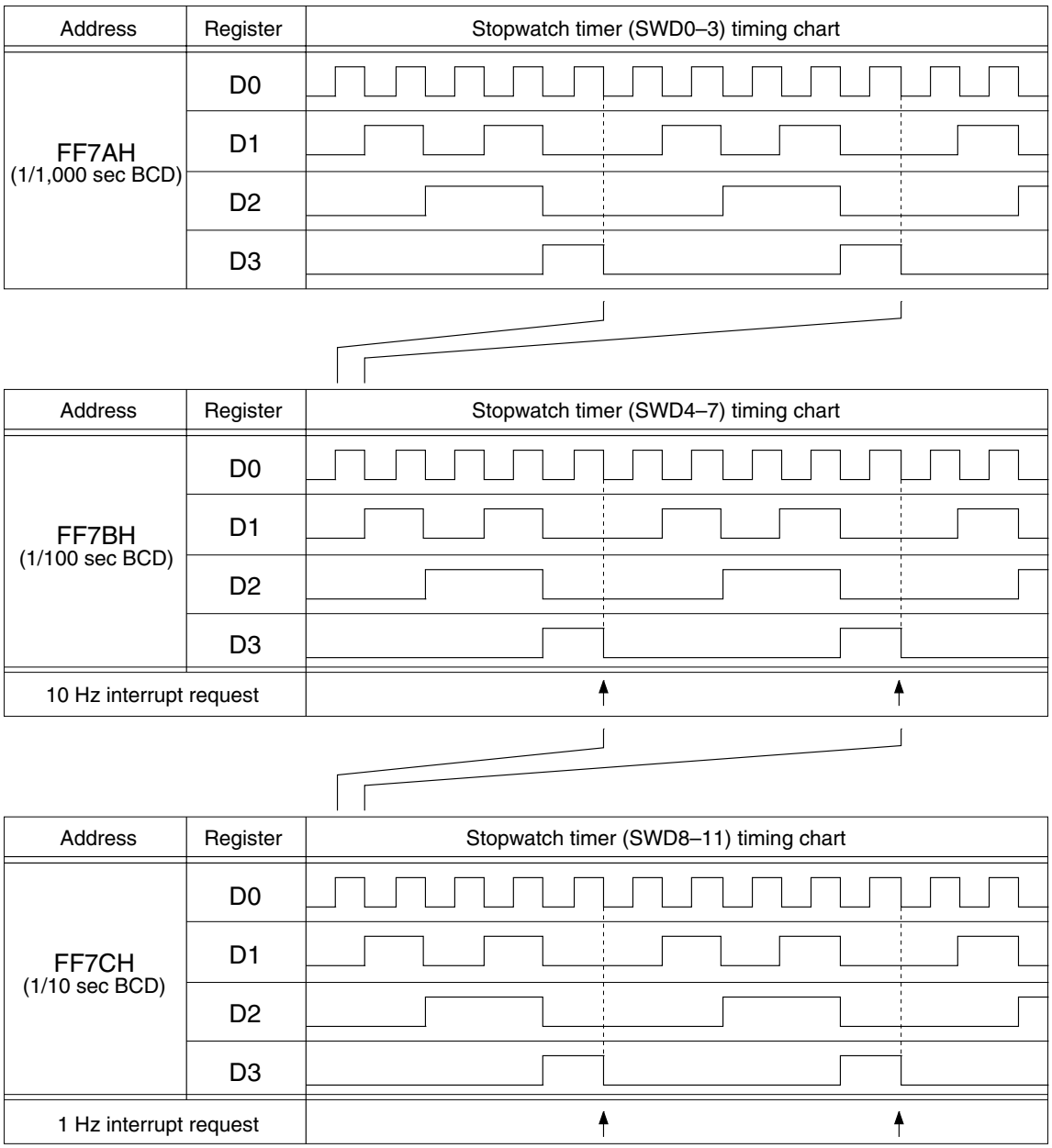


Fig. 4.9.6.1 Timing chart for counters

As shown in Figure 4.9.6.1, the interrupts are generated by the overflow of their respective counters ("9" changing to "0"). Also, at this time the corresponding interrupt factor flag (ISW10, ISW1) is set to "1". The respective interrupts can be masked separately through the interrupt mask registers (EISW10, EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

Direct RUN and direct LAP interrupts

When the direct input function is selected, the direct RUN and direct LAP interrupts can be generated. The respective interrupts occur at the rising edge of the internal signal for direct RUN and direct LAP after sampling the direct input signal in the falling edge of 1,024 Hz signal. Also, at this time the corresponding interrupt factor flag (IRUN, ILAP) is set to "1".
The respective interrupts can be masked separately through the interrupt mask registers (EIRUN, EILAP). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the inputs of the RUN and LAP.

The direct RUN and LAP functions use the K00 and K01 ports. Therefore, the direct input interrupt and the K00–K03 inputs interrupt may generate at the same time depending on the interrupt condition setting for the input port K00–K03. Consequently, when using the direct input interrupt, set the interrupt selection registers SIK00 and SIK01 to "0" so that the input interrupt does not generate by K00 and K01 inputs.

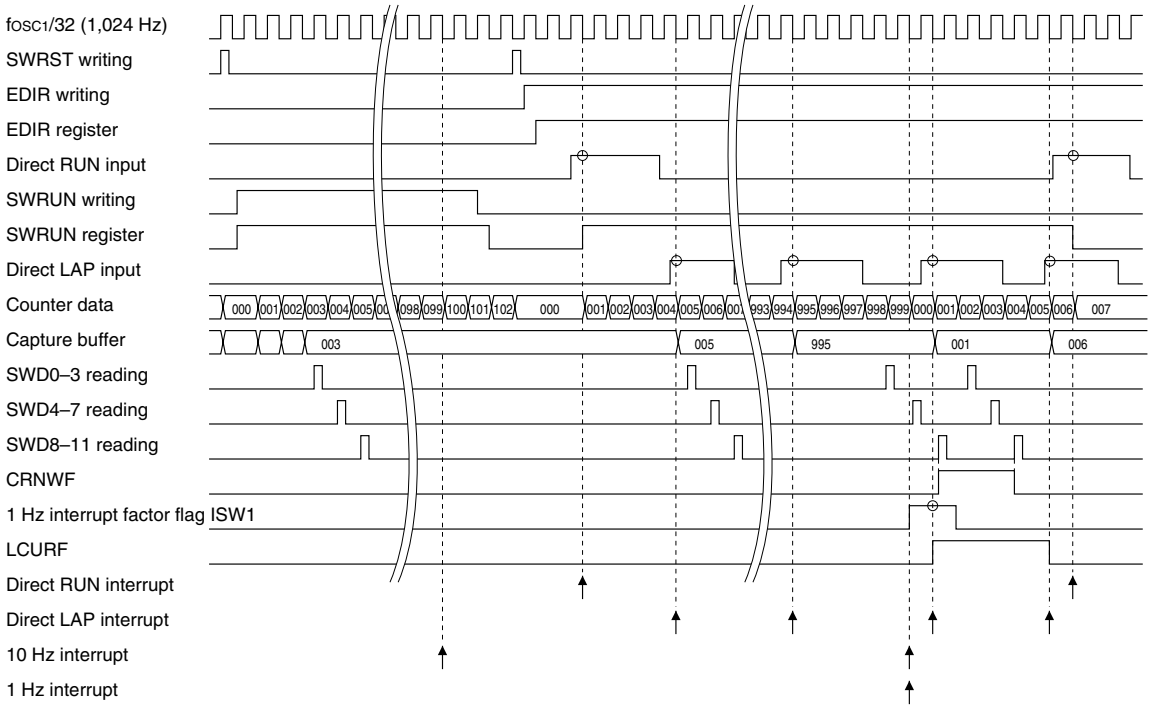


Fig. 4.9.6.2 Timing chart for stopwatch timer

4.9.7 I/O memory of stopwatch timer

Table 4.9.7.1 shows the I/O addresses and the control bits for the stopwatch timer.

Table 4.9.7.1 Control bits of stopwatch timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					SWDIR	0			Stopwatch direct input switch
									0: K00=Run/Stop, K01=Lap 1: K00=Lap, K01=Run/Stop
	R/W				FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3
					FOFQ0	0			Frequency fosc1/64 fosc1/8 fosc1 fosc3
FF78H	EDIR	DKM2	DKM1	DKM0	EDIR	0	Enable	Disable	Direct input enable
					DKM2	0			Key mask selection [DKM2, 1, 0] 0 1 2 3
	R/W				DKM1	0			Key mask None K02 K02–03 K02–03,10
					DKM0	0			[DKM2, 1, 0] 4 5 6 7
									Key mask K10 K10–11 K10–12 K10–13
FF79H	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Request	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
FF7AH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/1000 sec)
					SWD2	0			
	R				SWD1	0			
					SWD0	0			
FF7BH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/100 sec)
					SWD6	0			
	R				SWD5	0			
					SWD4	0			
FF7CH	SWD11	SWD10	SWD9	SWD8	SWD11	0			Stopwatch timer data BCD (1/10 sec)
					SWD10	0			
	R				SWD9	0			
					SWD8	0			
FFE6H	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFF6H	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SWD0–SWD3: Stopwatch timer data 1/1,000 sec (FF7AH)

Data (BCD) of the 1/1,000 sec column of the capture buffer can be read out.
The hold function of the capture buffer works by reading this data.
These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

SWD4–SWD7: Stopwatch timer data 1/100 sec (FF7BH)

Data (BCD) of the 1/100 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

SWD8–SWD11: Stopwatch timer data 1/10 sec (FF7CH)

Data (BCD) of the 1/10 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

Note: Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

EDIR: Direct input function enable register (FF78H•D3)

Enables the direct input (RUN/LAP) function.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

The direct input function is enabled by writing "1" to EDIR, and then RUN/STOP and LAP control can be done by external key input. When "0" is written, the direct input function is disabled, and the stopwatch timer is controlled by the software only.
Further the function switching is actually done by synchronizing with the falling edge of $f_{OSC1}/32$ (1,024 Hz) after the data is written to this register (after 977 µsec maximum).
At initial reset, this register is set to "0".

SWDIR: Direct input switch register (FF06H•D2)

Switches the direct-input key assignment for the K00 and K01 ports.

When "1" is written: K00 = LAP, K01 = RUN/STOP
When "0" is written: K00 = RUN/STOP, K01 = LAP
Reading: Valid

The direct-input key assignment is selected using this register. The K00 and K01 port statuses are input to the stopwatch timer as the RUN/STOP and LAP inputs according to this selection.
At initial reset, this register is set to "0".

DKM0–DKM2: Direct key mask selection register (FF78H•D0–D2)

Selects a combination of the key inputs for concurrence judgment with RUN and LAP inputs when the direct input function is set.

Table 4.9.7.2 Key mask selection

DKM2	DKM1	DKM0	Mask key combination
0	0	0	None (at initial reset)
0	0	1	K02
0	1	0	K02, K03
0	1	1	K02, K03, K10
1	0	0	K10
1	0	1	K10, K11
1	1	0	K10, K11, K12
1	1	1	K10, K11, K12, K13

When the concurrence is detected, RUN and LAP inputs cannot be accepted until the concurrence is released.
At initial reset, this register is set to "0".

SWRST: Stopwatch timer reset (FF79H•D0)

This bit resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained.
Since this reset does not affect the capture buffer, the capture buffer data in hold status is not cleared and is maintained.
This bit is write-only, and is always "0" at reading.

SWRUN: Stopwatch timer RUN/STOP (FF79H•D1)

This register controls the RUN/STOP of the stopwatch timer, and the operating status can be monitored by reading this register.

• ***When writing data***

When "1" is written: RUN
When "0" is written: STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count. RUN/STOP control with this register is valid only when the direct input function is set to disable. When the direct input function is set, it becomes invalid.

• ***When reading data***

When "1" is read: RUN
When "0" is read: STOP

Reading is always valid regardless of the direct input function setting. "1" is read when the stopwatch timer is in the RUN status, and "0" is read in the STOP status.
At initial reset, this register is set to "0".

LCURF: Lap data carry-up request flag (FF79H•D3)

This flag indicates a carry that has been generated to 1 sec-digit when the data is held. Note that this flag is invalid when the direct input function is disabled.

When "1" is read: Carry is required
When "0" is read: Carry is not required
Writing: Invalid

If the capture buffer shifts into hold status while the 1 Hz interrupt factor flag ISW1 is set to "1", LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required. When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read this flag before processing and check whether carry-up is needed or not.
This flag is renewed (set/reset) every time the capture buffer shifts into hold status.
At initial reset, this flag is set to "0".

CRNWF: Capture renewal flag (FF79H•D2)

This flag indicates that the content of the capture buffer has been renewed.

When "1" is read: Renewed
When "0" is read: Not renewed
Writing: Invalid

The content of the capture buffer is renewed if the LAP key is input when the data held into the capture buffer has not yet been read. Reading SWD8–11 in that status sets this flag to "1", and the hold status is maintained. Consequently, when data that is held by a LAP input is read, read this flag after reading the SWD8–11 and check whether the data has been renewed or not.
This flag is renewed when SWD8–11 is read.
At initial reset, this flag is set to "0".

EIRUN, EILAP, EISW1, EISW10: Interrupt mask registers (FFE6H)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers EIRUN, EILAP, EISW1 and EISW10 are used to separately select whether to mask the direct RUN, direct LAP, 1 Hz and 10 Hz interrupts.
At initial reset, these registers are set to "0".

IRUN, ILAP, ISW1, ISW10: Interrupt factor flags (FFF6H)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IRUN, ILAP, ISW1 and ISW10 correspond to the direct RUN, direct LAP, 1 Hz and 10 Hz interrupts respectively. The software can judge from these flags whether there is a stopwatch timer interrupt. However, even if the interrupt is masked, the flags are set to "1" when the timing condition is established.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.9.8 Programming notes

(1) The interrupt factor flag should be reset after resetting the stopwatch timer.

(2) Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

(3) When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWD8–11 and check whether the data has been renewed or not.

(4) When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.10 Programmable Timer

4.10.1 Configuration of programmable timer

The S1C63656 has two 8-bit programmable timer systems (timer 0 and timer 1) built-in.
The timers are composed of 8-bit presettable down counters and they can be used as 8 bits × 2 channels or 16 bits × 1 channel of programmable timers. Timer 0 also has an event counter function using the K13 input port terminal.
Figure 4.10.1.1 shows the configuration of the programmable timer.

Each timer has an 8-bit down counter and an 8-bit reload data register. The down counter counts the input clock. When the down counter underflows, the timer outputs the underflow and interrupt signals and resets the counter to its initial value. The reload data register is used to store that initial value. The underflow signal of timer 1 is used as the source clock of the serial interface, this makes it possible to program a flexible transfer rate.
Each timer has an 8-bit compare data register in addition to the above registers. This register is used to store data to be compared with the contents of the down counter. When the timer is set in the PWM mode, the timer outputs the compare match signal if the contents between the down counter and the compare data register are matched, and an interrupt occurs at the same time. Also the compare match signal is used with the underflow signal to generate a PWM waveform.
The signal generated by the programmable timer can be output from the R02 output port terminal.

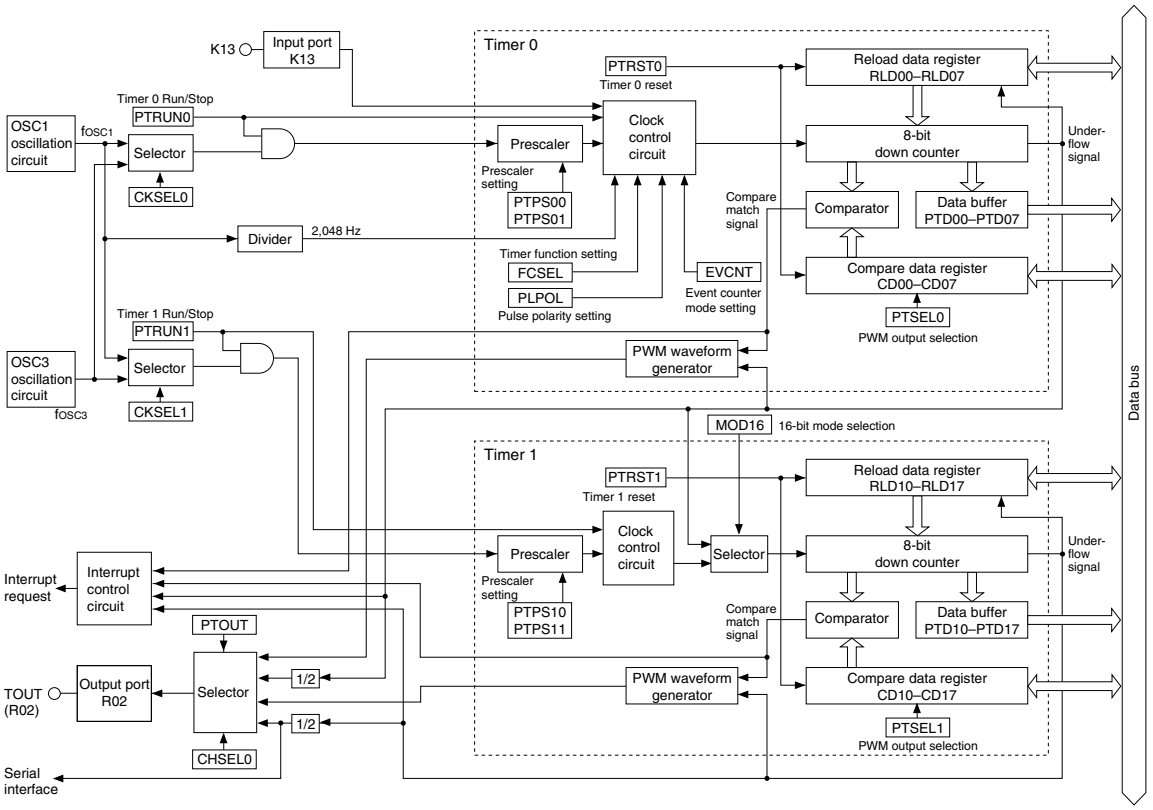


Fig. 4.10.1.1 Configuration of programmable timer

4.10.2 Basic count operation

This section explains the basic count operation when each timer is used as an individual 8-bit timer.

Each timer has an 8-bit down counter and an 8-bit reload data register.
The reload data register RLDx0–RLDx7 (x = timer number) is used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRSTx, the down counter loads the initial value set in the reload register. Therefore, down-counting is executed from the stored initial value by the input clock.
The PTRUNx register is provided to control the RUN/STOP for each timer. By writing "1" to this register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.
The counter data can be read via the data buffer PTDx0–PTDx7 in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data (PTDx4–PTDx7) when the low-order data (PTDx0–PTDx3) is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.
The counter reloads the initial value set in the reload data register when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

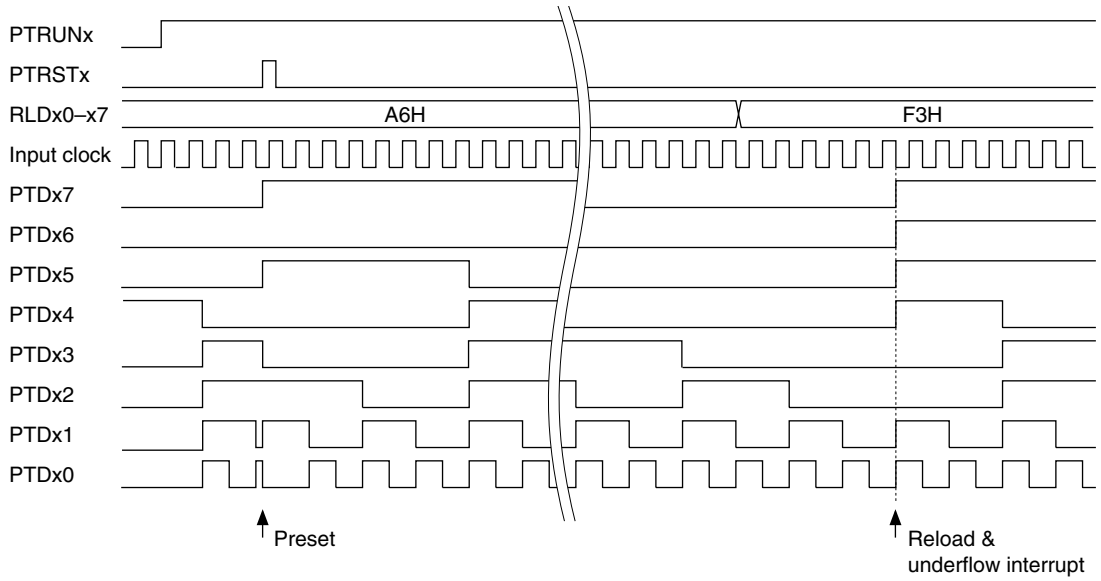


Fig. 4.10.2.1 Basic operation timing of down counter

4.10.3 Setting the input clock

A prescaler is provided for each timer. The prescaler generates the input clock for the timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit. The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software for each timer individually.
The input clock is set in the following sequence.

Selection of source clock

Select the source clock input to each prescaler from either OSC1 or OSC3. This selection is done using the source clock selection register CKSELx; when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.
When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation on, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit on until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit on to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in off state.

Note: When the mask option to disable the OSC3 oscillation circuit is selected, no source clock can be selected (fixed at OSC1). Do not set the CKSELx register to "1".

Selection of prescaler division ratio

Select the division ratio for each prescaler from among 4 types. This selection is done using the prescaler division ratio selection register PTPSx0/PTPSx1. Table 4.10.3.1 shows the correspondence between the setting value and the division ratio.

Table 4.10.3.1 Selection of prescaler division ratio

PTPSx1	PTPSx0	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the PTRUNx register, the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.10.4 Event counter mode (timer 0)

Timer 0 has an event counter function that counts an external clock input to the input port K13. This function is selected by writing "1" to timer 0 counter mode selection register EVCNT. At initial reset, EVCNT is set to "0" and timer 0 is configured as a normal timer that counts the internal clock.
In the event counter mode, the clock is supplied to timer 0 from outside the IC, therefore, the settings of the timer 0 prescaler division ratio selection register PTPS00–PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.
Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.10.4.1.

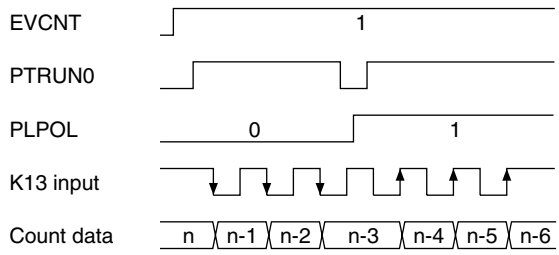


Fig. 4.10.4.1 Timing chart in event counter mode

The event counter mode also allows use of a noise reject function to eliminate noise such as chattering on the external clock (K13 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec∗ or more to count reliably. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz∗ signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec∗ or less.
(∗: f_{OSC1} = 32.768 kHz)
Figure 4.10.4.2 shows the count down timing with noise rejector.

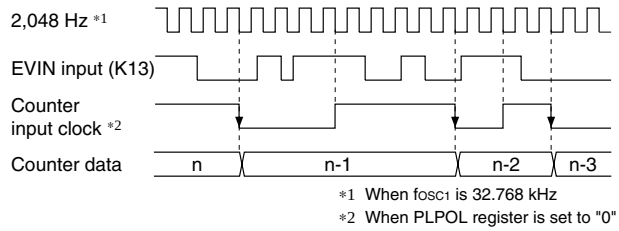


Fig. 4.10.4.2 Count down timing with noise rejector

The operation of the event counter mode is the same as the normal timer except it uses the K13 input as the clock. Refer to Section 4.10.2, "Basic count operation" for basic operation and control.

4.10.5 PWM mode (timer 0, timer 1)

Timer 0 and timer 1 can generate a PWM waveform. When using this function, write "1" to the PTSEL0 register (for timer 0) or PTSEL1 register (for timer 1) to set the timer in the PWM mode.
The compare data register CDx0–CDx7 (x represents a timer number) is provided for timers 0 and 1 to control the PWM waveform. When the timer is set in the PWM mode, the timer compares data between the down counter and the compare data register and outputs the compare match signal if their contents are matched. At the same time a compare match interrupt occurs. Furthermore, the timer output signal rises with the underflow signal and falls with the compare match signal. As shown in Figure 4.10.5.1, the cycle and duty ratio of the output signal can be controlled using the reload data register and the compare data register, respectively, to generate a PWM signal. Note, however, the following condition must be met: RLD (reload data) > CD (compare data) and CD ≠ 0. If RLD ≤ CD, the output signal is fixed at "1" after the first underflow occurs and does not fall to "0".
The generated PWM signal can be output from the R02 output port terminal (see Section 4.10.8).

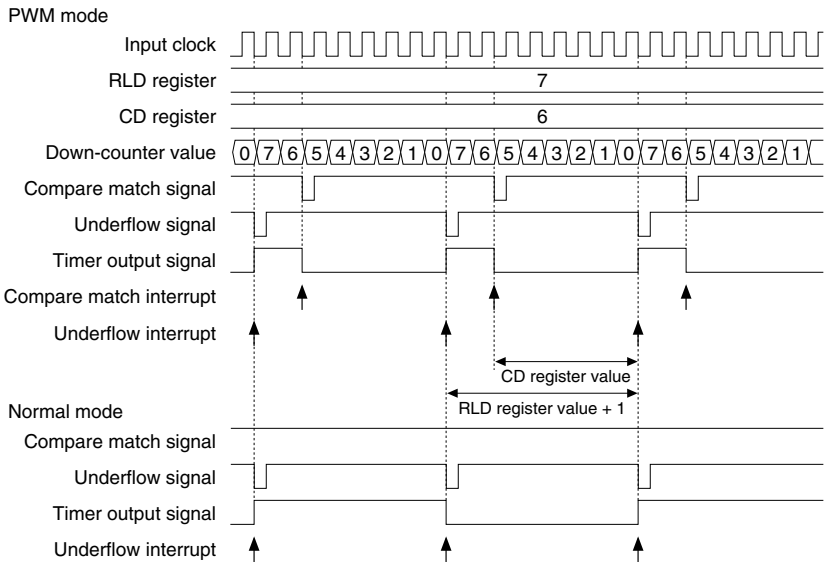


Fig. 4.10.5.1 Generating PWM waveform

4.10.6 16-bit timer (timer 0 + timer 1)

Timers 0 and 1 can be used as a 16-bit timer.
To use the 16-bit timer, write "1" to the timer 0 16-bit mode selection register MOD16.
The 16-bit timer is configured with timer 0 for low-order byte and timer 1 for high-order byte as shown in Figure 4.10.6.1.

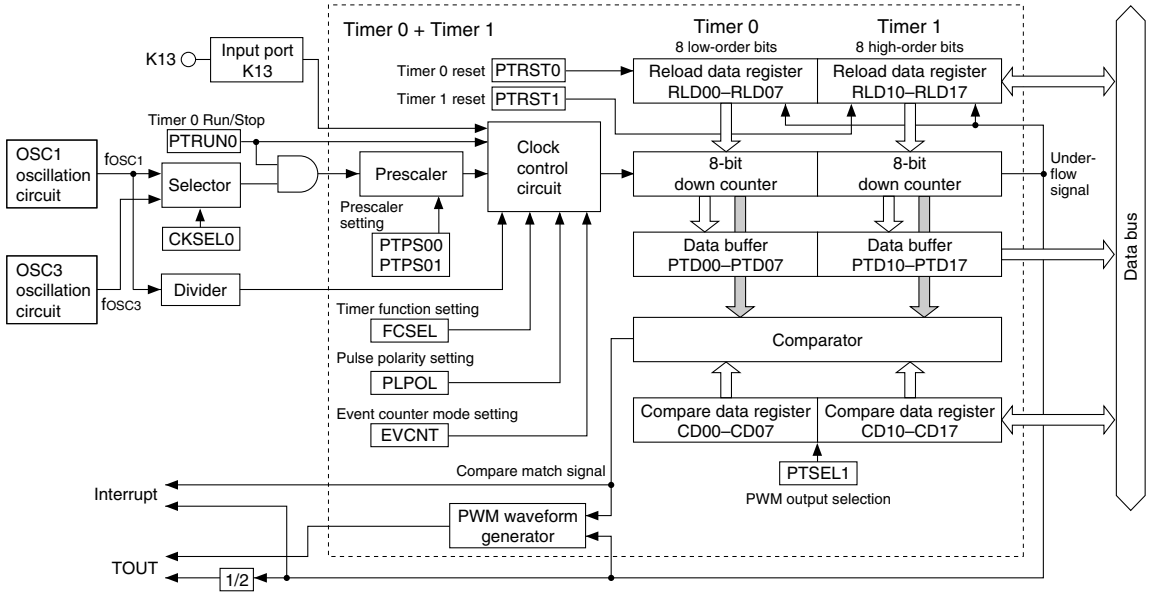


Fig. 4.10.6.1 Configuration of 16-bit timer

The registers for timer 0 are used to control the timer. The event counter and PWM output functions can also be used.
Timer 1 operates with the timer 0 underflow signal as the count clock, so the clock and RUN/STOP control registers for timer 1 become invalid. However, reload data (PTRSTx) must be preset to timers 0 and 1 separately.
The counter data in 16-bit mode must be read in the order below.
PTD00–PTD03 → PTD04–PDT07 → PTD10–PTD13 → PTD14–PTD17

4.10.7 Interrupt function

The programmable timer can generate an interrupt due to an underflow of each timer or a compare match of timers 0 and 1. See Figures 4.10.2.1 and 4.10.5.1 for the interrupt timing.

Note: The compare match interrupt can be generated only when timer 0 or 1 is set in PWM mode.

An underflow/compare match of timer x sets the corresponding interrupt factor flag IPTx/ICTCx to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPTx/ECTCx. However, the interrupt factor flag is set to "1" by an underflow/compare match of the corresponding timer regardless of the interrupt mask register setting.

When timers 0 and 1 are used as a 16-bit timer, an interrupt is generated by an underflow of timer 1. In this case, IPT0 is not set to "1" by a timer 0 underflow. The compare match interrupt uses ICTC1 of timer 1.

4.10.8 Control of TOUT output

The programmable timer can generate a TOUT signal from the timer underflow and compare match signals. The TOUT signal is generated by dividing the underflow signal by 2 in the normal mode. In the PWM mode, the PWM signal generated by timer 0/1 is output as the TOUT signal. It is possible to select which timer output is to be used by the TOUT output channel selection register CHSEL0.

Table 4.10.8.1 Selecting a timer for TOUT output

CHSEL0	TOUT output timer
1	Timer 1
0	Timer 0

Select timer 1 when generating the TOUT signal from the 16-bit timer output.

The TOUT signal can be output from the R02 output port terminal.
Figure 4.10.8.1 shows the configuration of the output port R02.

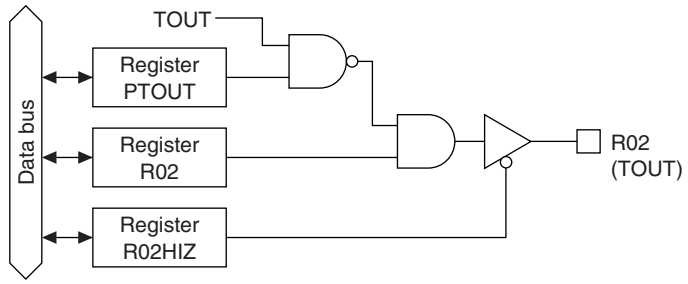


Fig. 4.10.8.1 Configuration of R02

The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R02 output port terminal and when "0" is written, the terminal goes to a high (V_{DD}) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.
Figure 4.10.8.2 shows the output waveform of the TOUT signal.

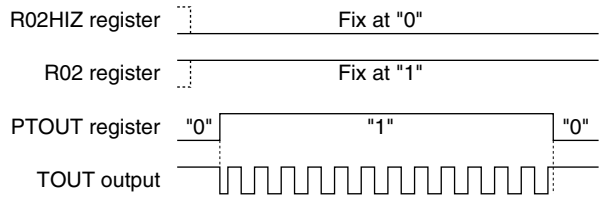


Fig. 4.10.8.2 Output waveform of the TOUT signal

4.10.9 Transfer rate setting for serial interface

The signal that is made from underflows of timer 1 by dividing them in 1/2, can be used as the clock source for the serial interface.
The programmable timer outputs the clock to the serial interface by setting timer 1 into RUN state (PTRUN1 = "1"). It is not necessary to control with the PTOUT register.

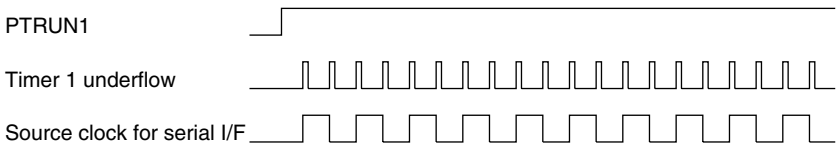


Fig. 4.10.9.1 Synchronous clock of serial interface

A setting value for the RLD1x register according to a transfer rate is calculated by the following expression:

RLD1x = fosc / (2 ∗ bps ∗ division ratio of the prescaler) - 1

fosc: Oscillation frequency (OSC1/OSC3)
bps: Transfer rate
(00H can be set to RLD1x)

Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source.

4.10.10 I/O memory of programmable timer

Table 4.10.10.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.10.10.1(a) Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFC0H	MOD16	EVCNT	FCSEL	PLPOL	MOD16	0	16 bits	8 bits	16-bit mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R/W				FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	0	0	CHSEL0	PTOUT	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		CHSEL0	0	Timer 1	Timer 0	TOUT output selection
					PTOUT	0	On	Off	TOUT output control
FFC2H	0	0	CKSEL1	CKSEL0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC3H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC4H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC6H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FFC7H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FFC8H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FFC9H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FFCCH	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFCDH	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FFCEH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCFH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FFD2H	CD03	CD02	CD01	CD00	CD03	0			MSB
					CD02	0			Programmable timer 0 compare data (low-order 4 bits)
	R/W				CD01	0			
					CD00	0			LSB

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.10.10.1(b) Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFD3H	CD07	CD06	CD05	CD04	CD07	0			MSB
					CD06	0			Programmable timer 0 compare data (high-order 4 bits)
					CD05	0			
	R/W				CD04	0			LSB
FFD4H	CD13	CD12	CD11	CD10	CD13	0			MSB
					CD12	0			Programmable timer 1 compare data (low-order 4 bits)
					CD11	0			
	R/W				CD10	0			LSB
FFD5H	CD17	CD16	CD15	CD14	CD17	0			MSB
					CD16	0			Programmable timer 1 compare data (high-order 4 bits)
					CD15	0			
	R/W				CD14	0			LSB
FFD8H	0	0	PTSEL1	PTSEL0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		PTSEL1	0	PWM	Normal	Programmable timer 1 PWM output selection
					PTSEL0	0	PWM	Normal	Programmable timer 0 PWM output selection
FFE0H	0	0	ECTC1	ECTC0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		ECTC1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 compare match)
					ECTC0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 compare match)
FFE1H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 underflow)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 underflow)
FFF0H	0	0	ICTC1	ICTC0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ICTC1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1 compare match)
					ICTC0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0 compare match)
FFF1H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1 underflow)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0 underflow)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

CKSEL0: Prescaler 0 source clock selection register (FFC2H•D0)
CKSEL1: Prescaler 1 source clock selection register (FFC2H•D1)

Selects the source clock of the prescaler.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

The source clock for the prescaler is selected from OSC1 or OSC3. When "0" is written to the CKSELx register, the OSC1 clock is selected as the input clock for the prescaler x (for timer x) and when "1" is written, the OSC3 clock is selected.
When the event counter mode is selected for timer 0, the setting of CKSEL0 becomes invalid.
When timers 0 and 1 are used as a 16-bit timer, the setting of CKSEL1 becomes invalid.
At initial reset, these registers are set to "0".

Note: When the mask option to disable the OSC3 oscillation circuit is selected, no source clock can be selected (fixed at OSC1). Do not set the CKSELx register to "1".

PTPS00, PTPS01: Timer 0 prescaler division ratio selection register (FFC3H•D2, D3)
PTPS10, PTPS11: Timer 1 prescaler division ratio selection register (FFC4H•D2, D3)
Sets the division ratio of the prescaler as shown in Table 4.10.10.2.

Table 4.10.10.2 Selection of prescaler division ratio

PTPSx1	PTPSx0	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

When the event counter mode is selected to timer 0, the setting of PTPS00 and PTPS01 becomes invalid.
When timers 0 and 1 are used as a 16-bit timer, the setting of PTPS10 and PTPS11 becomes invalid.
At initial reset, these registers are set to "0".

MOD16: 16-bit mode selection register (FFC0H•D3)
Selects whether timers 0 and 1 are used as a 16-bit timer or 2 channels of 8-bit timer.

When "1" is written: 16-bit timer
When "0" is written: 8-bit timer
Reading: Valid

When "1" is written to MOD16, a 16-bit timer is configured with timer 0 for low-order byte and timer 1 for high-order byte. Use the timer 0 registers for control. When "0" is written to MOD16, timer 0 and timer 1 are used as independent 8-bit timers.
At initial reset, this register is set to "0".

EVCNT: Timer 0 counter mode selection register (FFC0H•D2)
Selects a counter mode for timer 0.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

The counter mode for timer 0 is selected from either the event counter mode or timer mode. When "1" is written to the EVCNT register, the event counter mode is selected and when "0" is written, the timer mode is selected.
At initial reset, this register is set to "0".

FCSEL: Timer 0 function selection register (FFC0H•D1)
Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejector
When "0" is written: Without noise rejector
Reading: Valid

When "1" is written to the FCSEL register, the noise rejector is used and counting is done by an external clock (K13) with 0.98 msec* or more pulse width. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz* signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec* or less.
(*: f_{OSC1} = 32.768 kHz)
When "0" is written to the FCSEL register, the noise rejector is not used and the counting is done directly by an external clock input to the K13 input port terminal.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

PLPOL: Timer 0 pulse polarity selection register (FFC0H•D0)

Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

The count timing in the event counter mode (timer 0) is selected from either the falling edge of the external clock input to the K13 input port terminal or the rising edge. When "0" is written to the PLPOL register, the falling edge is selected and when "1" is written, the rising edge is selected.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

PTSEL0: Timer 0 PWM mode selection register (FFD8H•D0)
PTSEL1: Timer 1 PWM mode selection register (FFD8H•D1)

Sets timer 0 or 1 for PWM output.

When "1" is written: PWM output
When "0" is written: Normal output
Reading: Valid

When "1" is written to the PTSELx, the compare data register becomes valid and PWM waveform is generated using the underflow and compare match signals. When "0" is written, the timer outputs the normal clock generated from the underflow signal. When timers 0 and 1 are used as a 16-bit timer, the setting of PTSEL1 becomes invalid.
At initial reset, these registers are set to "0".

RLD00–RLD07: Timer 0 reload data register (FFC6H, FFC7H)
RLD10–RLD17: Timer 1 reload data register (FFC8H, FFC9H)

Sets the initial value for the counter.
The reload data written in this register is loaded to the respective counters. The counter counts down using the data as the initial value for counting.
Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRSTx register, or when counter underflow occurs.
At initial reset, these registers are set to "00H".

PTD00–PTD07: Timer 0 counter data (FFCCH, FFCDH)
PTD10–PTD17: Timer 1 counter data (FFCEH, FFCFH)

Count data in the programmable timer can be read from these latches.
The low-order 4 bits of the count data in timer x can be read from PTDx0–PTDx3, and the high-order data can be read from PTDx4–PTDx7. Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.
Since these latches are exclusively for reading, the writing operation is invalid.
At initial reset, these counter data are set to "00H".

CD00–CD07: Timer 0 compare data register (FFD2H, FFD3H)
CD10–CD17: Timer 1 compare data register (FFD4H, FFD5H)

Set the compare data for PWM output.
When the timer is set in the PWM mode, the compare data set in this register is compared with the counter data and outputs the compare match signal if they are matched. The compare match signal is used for generating an interrupt and controlling the duty ratio of the PWM waveform.
At initial reset, these registers are set to "00H".

PTRST0: Timer 0 reset (reload) (FFC3H•D1)
PTRST1: Timer 1 reset (reload) (FFC4H•D1)
Resets the timer and presets reload data to the counter.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PTRSTx, the reload data in the reload register RLDx0–RLDx7 is preset to the counter in timer x. When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained.
No operation results when "0" is written.
Since these bits are exclusively for writing, always set to "0" during reading.

PTRUN0: Timer 0 RUN/STOP control register (FFC3H•D0)
PTRUN1: Timer 1 RUN/STOP control register (FFC4H•D0)
Controls the RUN/STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter in timer x starts counting down by writing "1" to the PTRUNx register and stops by writing "0". In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.
At initial reset, these registers are set to "0".

CHSEL0: TOUT output channel selection register (FFC1H•D1)
Selects the channel used for TOUT signal output.

When "1" is written: Timer 1
When "0" is written: Timer 0
Reading: Valid

This register selects which timer's output (timer 0 or timer 1) is used to generate a TOUT signal. When "0" is written to the CHSEL0 register, timer 0 is selected and when "1" is written, timer 1 is selected. In the 16-bit mode (MOD16 = "1"), timer 1 is always selected regardless of this register setting.
At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D0)
Turns TOUT signal output on and off.

When "1" is written: On
When "0" is written: Off
Reading: Valid

PTOUT is the output control register for the TOUT signal. When "1" is written to the register, the TOUT signal is output from the output port terminal R02 and when "0" is written, the terminal goes to a high (V_{DD}) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).
At initial reset, this register is set to "0".

EIPT0, ECTC0: Timer 0 interrupt mask registers (FFE1H•D0, FFE0H•D0)
EIPT1, ECTC1: Timer 1 interrupt mask registers (FFE1H•D1, FFE0H•D1)

These registers are used to select whether to mask the programmable timer interrupt or not.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

EIPTx and ECTCx are the interrupt mask registers that respectively correspond to the counter underflow and compare match interrupt factors. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, these registers are set to "0".

IPT0, ICTC0: Timer 0 interrupt factor flags (FFF1H•D0, FFF0H•D0)
IPT1, ICTC1: Timer 1 interrupt factor flags (FFF1H•D1, FFF0H•D1)

These flags indicate the status of the programmable timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

IPTx and ICTCx are the interrupt factor flags that respectively correspond to the interrupts for counter underflow and compare match, and are set to "1" by generation of each factor.
The underflow interrupt factor is generated at the point where the counter underflows.
The compare match interrupt factor is generated if the counter data and the compare data are matched when the timer is set in the PWM mode.
The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by an underflow and compare match of the corresponding counter.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.10.11 Programming notes

(1) When reading counter data, be sure to read the low-order 4 bits (PTDx0–PTDx3) first. Furthermore, the high-order 4 bits (PTDx4–PTDx7) are not latched when the low-order 4 bits are read. Therefore, the high-order 4 bits should be read within 0.73 msec (when f_{OSC1} is 32.768 kHz) from reading the low-order 4 bits. When the CPU is running with the OSC1 clock and the programmable timer is running with the OSC3 clock, stop the timer before reading the counter data. The counter running with OSC3 counts down for the value listed in Table 4.10.11.1 while the CPU running with OSC1 reads the low-order 4 bits and high-order 4 bits of the counter data by two instructions.

Table 4.10.11.1 Counter change with OSC3 between readings low-order and high-order data with OSC1

Count clock	Counter change between reading
OSC3/1	0200H
OSC3/4	001AH
OSC3/32	0002H

In 16-bit mode, the counter data must be read in the order below.
PTD00–PTD03 → PTD04–PDT07 → PTD10–PTD13 → PTD14–PTD17

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.
Figure 4.10.11.1 shows the timing chart for the RUN/STOP control.

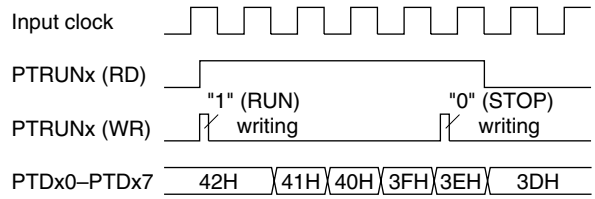


Fig. 4.10.11.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the off state.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(6) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

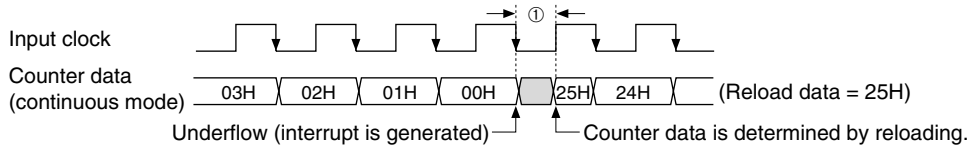


Fig. 4.10.11.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

4.11 Serial Interface (SIN, SOUT, SCLK, SRDY)

4.11.1 Configuration of serial interface

The S1C63656 has a synchronous clock type 8 bits serial interface built-in.
The configuration of the serial interface is shown in Figure 4.11.1.1.
The CPU, via the 8-bit shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8-bit shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of three types of master mode (internal clock mode: when the S1C63656 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the S1C63656 is to be the slave for serial input/output).
Also, when the serial interface is used at slave mode, SRDY signal which indicates whether or not the serial interface is available to transmit or receive can be output to the SRDY terminal.

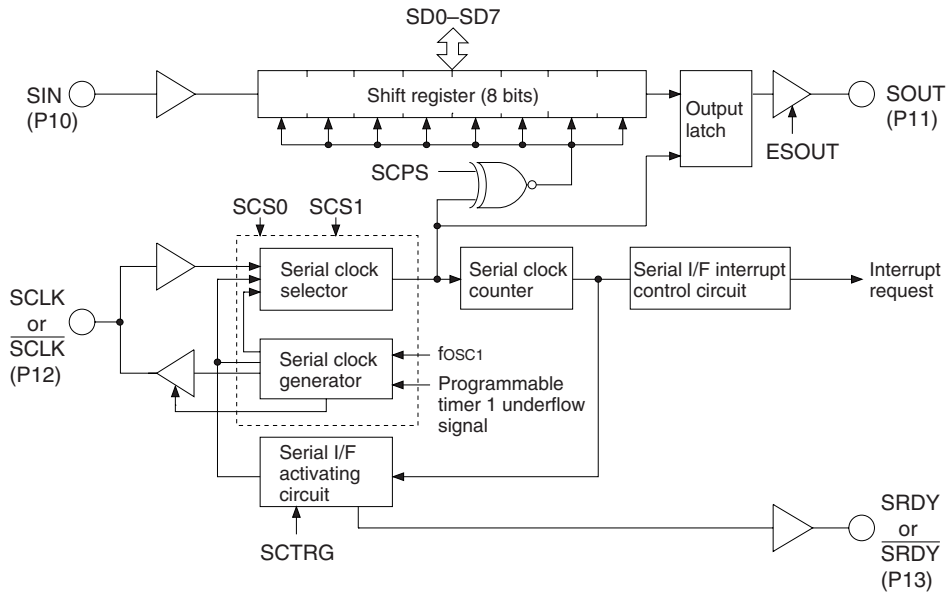


Fig. 4.11.1.1 Configuration of serial interface

The input/output ports of the serial interface are shared with the I/O ports P10–P13, and function of these ports can be selected through the software.
P10–P13 terminals and serial input/output correspondence are as follows:

Master mode	***Slave mode***
P10 = SIN (I)	P10 = SIN (I)
P11 = SOUT (O)	P11 = SOUT (O)
P12 = SCLK (O)	P12 = SCLK (I)
P13 = I/O port (I/O)	P13 = SRDY (O)

The SOUT output using the P11 port is enabled when "1" is written to the ESOUT register. If ESOUT is "0", P11 functions as a general-purpose I/O port.

Note: At initial reset, P10–P13 are set to I/O ports.
When using the serial interface, switch the function (ESIF = "1", ESOUT = "1") in the initial routine.

4.11.2 Mask option

Terminal specification

Since the input/output terminals of the serial interface is shared with the I/O ports (P10–P13), the mask option that selects the output specification for the I/O port is also applied to the serial interface. The output specification of the terminals SOUT, SCLK (during the master mode) and SRDY (during the slave mode) that are used as output in the input/output port of the serial interface is respectively selected by the mask options of P11, P12 and P13. Either complementary output or P-channel open drain output can be selected as the output specification. However, when P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the terminal.

Furthermore, the pull-down resistor for the SIN terminal and the SCLK terminal (during slave mode) that are used as input terminals can be selected by mask option. The pull-down register can be added by the mask options of P10 and P12. When "without pull-down" is selected, take care that the floating status does not occur.

Polarity of synchronous clock and ready signal

Polarity of the synchronous clock and the ready signal that is output in the slave mode can be selected from either positive polarity (high active, SCLK & SRDY) or negative polarity (low active, $\overline{\text{SCLK}}$ & $\overline{\text{SRDY}}$).
When operating the serial interface in the slave mode, the synchronous clock is input from a external device. Be aware that the terminal specification is pull-down only and a pull-up resistor cannot be built in if negative polarity is selected.
In the following explanation, it is assumed that positive polarity (SCLK, SRDY) has been selected.

4.11.3 Master mode and slave mode of serial interface

The serial interface of the S1C63656 has two types of operation mode: master mode and slave mode.
The master mode uses an internal clock as the synchronous clock for the built-in shift register, and outputs this internal clock from the SCLK (P12) terminal to control the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the SCLK (P12) terminal and it is used as the synchronous clock for the built-in shift register.
The master mode and slave mode are selected by writing data to the SCS1 and SCS0 registers.
When the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 4.11.3.1.

Table 4.11.3.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer *
0	0	Slave mode	External clock *

* The maximum clock is limited to 1 MHz.

When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 1) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.10, "Programmable Timer" for the control of the programmable timer.

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8-bit serial data, is controlled as follows:

- In the master mode, after output of 8 clocks from the SCLK (P12) terminal, clock output is automatically suspended and the SCLK (P12) terminal is fixed at low level (or high level when negative polarity is selected by mask option).
- In the slave mode, after input of 8 clocks to the SCLK (P12) terminal, subsequent clock inputs are masked.

A sample basic serial input/output portion connection is shown in Figure 4.11.3.1.

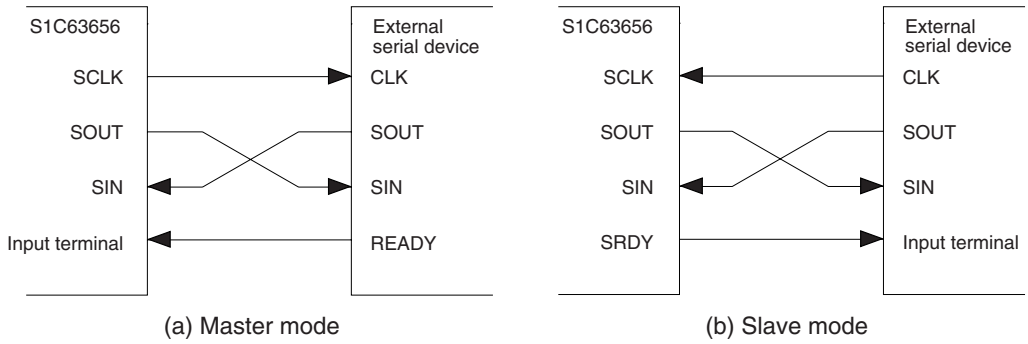


Fig. 4.11.3.1 Sample basic connection of serial input/output section

4.11.4 Data input/output and interrupt function

The serial interface of S1C63656 can input/output data via the internal 8-bit shift register. The shift register operates by synchronizing with either the synchronous clock output from the SCLK (P12) terminal (master mode), or the synchronous clock input to the SCLK (P12) terminal (slave mode).
The serial interface generates an interrupt on completion of the 8-bit serial data input/output. Detection of serial data input/output is done by counting of the synchronous clock SCLK; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates an interrupt.
The serial data input/output procedure is explained below:

Serial data output procedure and interrupt

The S1C63656 serial interface is capable of outputting parallel data as serial data, in units of 8 bits. By setting the parallel data to the data registers SD0–SD3 (FF72H) and SD4–SD7 (FF73H) and writing "1" to SCTRG bit (FF70H•D1), it synchronizes with the synchronous clock and the serial data is output to the SOUT (P11) terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK (P12) terminal while in the slave mode, external clock which is input from the SCLK (P12) terminal.
Shift timing of serial data is as follows:

- ***When positive polarity is selected for the synchronous clock (mask option):***
  The serial data output to the SOUT (P11) terminal changes at the rising edge of the clock input or output from/to the SCLK (P12) terminal. The data in the shift register is shifted at the rising edge of the SCLK signal when the SCPS register is "1" and is shifted at the falling edge of the SCLK signal when the SCPS register is "0".

- ***When negative polarity is selected for the synchronous clock (mask option):***
  The serial data output to the SOUT (P11) terminal changes at the falling edge of the clock input or output from/to the $\overline{\text{SCLK}}$ (P12) terminal. The data in the shift register is shifted at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS register (FF71H•D2) is "1" and is shifted at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "0".

  When the output of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF (FFF2H•D0) is set to "1" and an interrupt occurs. Moreover, the interrupt can be masked by the interrupt mask register EISIF (FFE2H•D0). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after output of the 8-bit data.

Serial data input procedure and interrupt

The S1C63656 serial interface is capable of inputting serial data as parallel data, in units of 8 bits. The serial data is input from the SIN (P10) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8-bit shift register. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK (P12) terminal while in the slave mode, external clock which is input from the SCLK (P12) terminal.
Shift timing of serial data is as follows:

- ***When positive polarity is selected for the synchronous clock (mask option):***
  The serial data is read into the built-in shift register at the rising edge of the SCLK signal when the SCPS register is "1" and is read at the falling edge of the SCLK signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.
- ***When negative polarity is selected for the synchronous clock (mask option):***
  The serial data is read into the built-in shift register at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "1" and is read at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.

When the input of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and an interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after input of the 8-bit data.
The data input in the shift register can be read from data registers SD0–SD7 by software.

Serial data input/output permutation

The S1C63656 allows the input/output permutation of serial data to be selected by the SDP register (FF71H•D3) as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.11.4.1. The SDP register should be set before setting data to SD0–SD7.

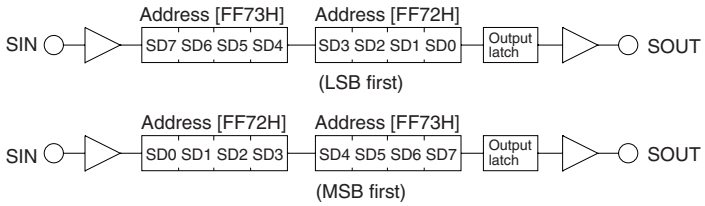


Fig. 4.11.4.1 Serial data input/output permutation

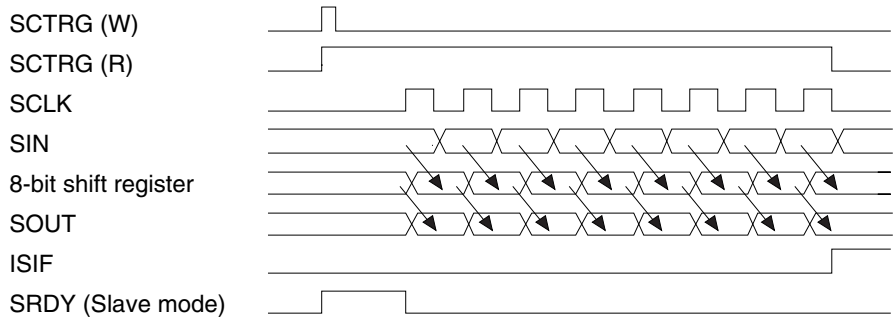
SRDY signal

When the S1C63656 serial interface is used in the slave mode (external clock mode), SRDY signal is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. SRDY signal is output from the SRDY (P13) terminal.
Output timing of SRDY signal is as follows:

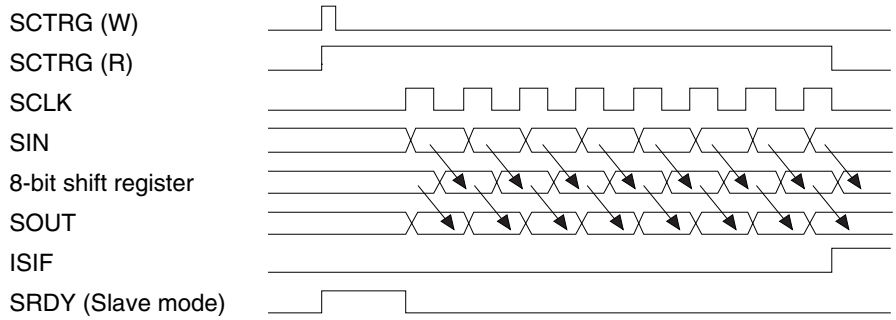
- ***When positive polarity is selected (mask option):***
  SRDY signal goes "1" (high) when the S1C63656 serial interface is available to transmit or receive data; normally, it is at "0" (low).
  SRDY signal changes from "0" to "1" immediately after "1" is written to SCTRG and returns from "1" to "0" when "1" is input to the SCLK (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the SRDY signal returns to "0".
- ***When negative polarity is selected (mask option):***
  $\overline{\text{SRDY}}$ signal goes "0" (low) when the S1C63656 serial interface is available to transmit or receive data; normally, it is at "1" (high).
  $\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to the $\overline{\text{SCLK}}$ (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".

Timing chart

The S1C63656 serial interface timing charts are shown in Figures 4.11.4.2 and 4.11.4.3.

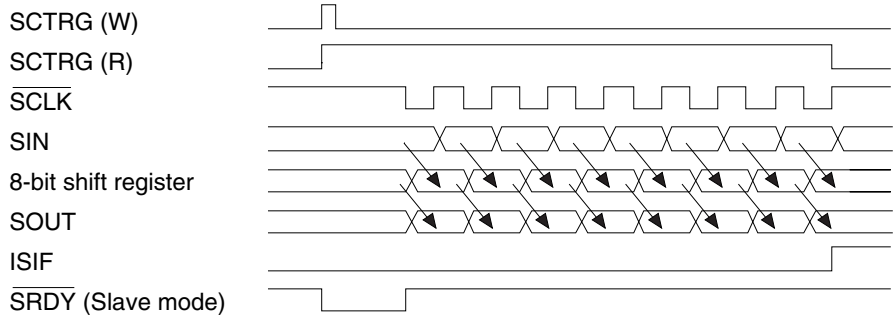


(a) When SCPS = "1"

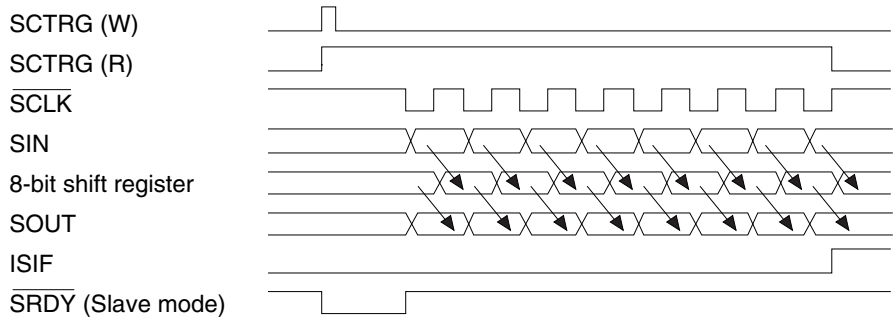


(b) When SCPS = "0"

Fig. 4.11.4.2 Serial interface timing chart (when synchronous clock is positive polarity SCLK)



(a) When SCPS = "1"



(b) When SCPS = "0"

Fig. 4.11.4.3 Serial interface timing chart (when synchronous clock is negative polarity $\overline{SCLK}$)

4.11.5 I/O memory of serial interface

Table 4.11.5.1 shows the I/O addresses and the control bits for the serial interface.

Table 4.11.5.1 Control bits of serial interface

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-down control register (ESIF=0) functions as a general-purpose register when SIF (master) is selected SCLK (I) pull-down control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-down control register (ESIF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-down control register (ESIF=0) SIN pull-down control register when SIF is selected
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R	R/W					Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
					SCPS	0	⌐	⌐	Serial I/F clock phase selection
							⌐	⌐	–Negative polarity (mask option)
							⌐	⌐	–Positive polarity (mask option)
	R/W				SCS1	0			Serial I/F clock mode selection
					SCS0	0			
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
					SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					SD1	– *2	High	Low	
	R/W				SD0	– *2	High	Low	LSB
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
					SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					SD5	– *2	High	Low	
	R/W				SD4	– *2	High	Low	LSB
FFE2H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFF2H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)

Clock mode selection:

[SCS1, 0]	0	1
Clock	Slave	PT
[SCS1, 0]	2	3
Clock	OSC1/2	OSC1

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ESIF: Serial interface enable register (P1 port function selection) (FF70H•D0)

Sets P10–P13 to the input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

When "1" is written to the ESIF register, P10, P11, P12 and P13 function as SIN, SOUT, SCLK, SRDY, respectively.
In the slave mode, the P13 terminal functions as SRDY output terminal, while in the master mode, it functions as the I/O port terminal.
At initial reset, this register is set to "0".

ESOUT: SOUT enable register (FF70H•D2)

Enables serial data output from the P11 port.

When "1" is written: Enabled (SOUT)
When "0" is written: Disabled (I/O port)
Reading: Valid

When serial data output is not used, the SOUT output can be disabled to use P11 as an I/O port. When performing serial output, write "1" to ESOUT to set P11 as the SOUT output port.
At initial reset, this register is set to "0".

PUL10: SIN (P10) pull-down control register (FF45H•D0)
PUL12: SCLK (P12) pull-down control register (FF45H•D2)

Sets the pull-down of the SIN terminal and the SCLK terminals (in the slave mode).

When "1" is written: Pull-down On
When "0" is written: Pull-down Off
Reading: Valid

Enables or disables the pull-down resistor built into the SIN (P10) and SCLK (P12) terminals. (Pull-down resistor is only built in the port selected by mask option.)
SCLK pull-down is effective only in the slave mode. In the master mode, the PUL12 register can be used as a general purpose register.
At initial reset, these registers are set to "1" and pull-down goes on.

SCS0, SCS1: Clock mode selection register (FF71H•D0, D1)

Selects the synchronous clock (SCLK) for the serial interface.

Table 4.11.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer ∗
0	0	Slave mode	External clock ∗

∗ The maximum clock is limited to 1 MHz.

Synchronous clock (SCLK) is selected from among the above 4 types: 3 types of internal clock and external clock.
When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 1) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.10, "Programmable Timer" for the control of the programmable timer.
At initial reset, external clock is selected.

SCPS: Clock phase selection register (FF71H•D2)

Selects the timing for reading in the serial data input from the SIN (P10) terminal.

• ***When positive polarity is selected:***

When "1" is written: Rising edge of SCLK
When "0" is written: Falling edge of SCLK
Reading: Valid

• ***When negative polarity is selected:***

When "1" is written: Falling edge of $\overline{\text{SCLK}}$
When "0" is written: Rising edge of $\overline{\text{SCLK}}$
Reading: Valid

Select whether the fetching for the serial input data to registers (SD0–SD7) at the rising edge or falling edge of the synchronous signal.

Pay attention to the polarity of the synchronous clock selected by the mask option because the selection content is different.
The input data fetch timing may be selected but output timing for output data is fixed at the rising edge of SCLK (when positive polarity is selected) or at the falling edge of $\overline{\text{SCLK}}$ (when negative polarity is selected).
At initial reset, this register is set to "0".

SDP: Data input/output permutation selection register (FF71H•D3)

Selects the serial data input/output permutation.

When "1" is written: MSB first
When "0" is written: LSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first.
At initial reset, this register is set to "0".

SCTRG: Clock trigger/status (FF70H•D1)

This is a trigger to start input/output of synchronous clock (SCLK).

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock (SCLK) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

• ***When reading***

When "1" is read: RUN (during input/output the synchronous clock)
When "0" is read: STOP (the synchronous clock stops)

When this bit is read, it indicates the status of serial interface clock.
After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation.
When the synchronous clock input/output is completed, this latch is reset to "0".
At initial reset, this bit is set to "0".

SD0–SD3, SD4–SD7: Serial interface data register (FF72H, FF73H)

These registers are used for writing and reading serial data.

• ***When writing***

When "1" is written: High level
When "0" is written: Low level

Write data to be output in these registers. The register data is converted into serial data and output from the SOUT (P11) terminal; data bits set at "1" are output as high (V_{DD}) level and data bits set at "0" are output as low (V_{SS}) level.

• When reading

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN (P10) terminal can be read from these registers.
The serial data input from the SIN (P10) terminal is converted into parallel data, as a high (V_{DD}) level bit into "1" and as a low (V_{SS}) level bit into "0", and is loaded to these registers. Perform data reading only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers are undefined.

EISIF: Interrupt mask register (FFE2H•D0)

Masking the interrupt of the serial interface can be selected with this register.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With this register, it is possible to select whether the serial interface interrupt is to be masked or not.
At initial reset, this register is set to "0".

ISIF: Interrupt factor flag (FFF2H•D0)

This flag indicates the occurrence of serial interface interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
This flag is set to "1" after an 8-bit data input/output even if the interrupt is masked.
This flag is reset to "0" by writing "1" to it.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, this flag is set to "0".

4.11.6 Programming notes

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source of the programmable timer or in the slave mode.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.12 Sound Generator

4.12.1 Configuration of sound generator

The S1C63656 has a built-in sound generator for generating a buzzer signal.
Hence, the generated buzzer signal can be output from the BZ terminal.
Aside permitting the respective setting of the buzzer signal frequency and sound level to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.
Figure 4.12.1.1 shows the configuration of the sound generator.

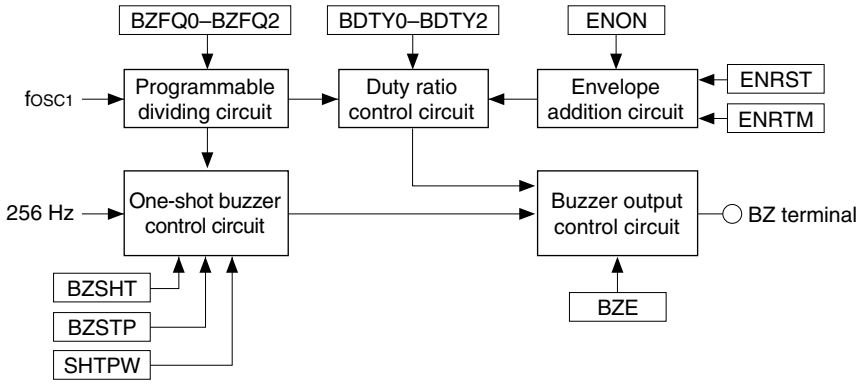


Fig. 4.12.1.1 Configuration of sound generator

4.12.2 Control of buzzer output

The BZ signal generated by the sound generator is output from the BZ terminal by setting "1" for the buzzer output enable register BZE. When "0" is set to BZE register, the BZ terminal goes low (VSS).

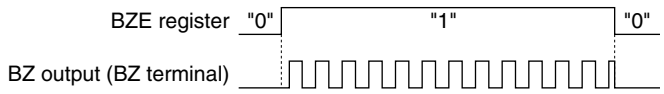


Fig. 4.12.2.1 Buzzer signal output timing chart

Note: Since it generates the buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

4.12.3 Setting of buzzer frequency and sound level

The divided signal of the OSC1 oscillation clock (32.768 kHz) is used for the buzzer signal and it is set up such that 8 types of frequencies can be selected by changing this division ratio. Frequency selection is done by setting the buzzer frequency selection registers BZFQ0–BZFQ2 as shown in Table 4.12.3.1.

Table 4.12.3.1 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer sound level is changed by controlling the duty ratio of the buzzer signal.
The duty ratio can be selected from among the 8 types shown in Table 4.12.3.2 according to the setting of the buzzer duty selection registers BDTY0–BDTY2.

Table 4.12.3.2 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0	3276.8	2730.7	2340.6
				2048.0	1638.4	1365.3	1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

When the high level output time has been made TH and when the low level output time has been made TL due to the ratio of the pulse width to the pulse synchronization, the duty ratio becomes TH/(TH+TL).
When BDTY0–BDTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when BDTY0–BDTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.
The duty ratio that can be set is different depending on the frequency that has been set, so see Table 4.12.3.2.

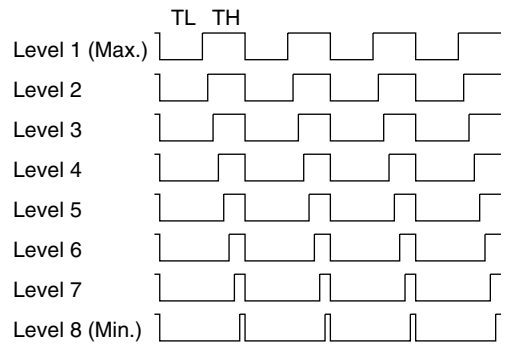


Fig. 4.12.3.1 Duty ratio of the buzzer signal waveform

Note: When a digital envelope has been added to the buzzer signal, the BDTY0–BDTY2 settings will be invalid due to the control of the duty ratio.

4.12.4 Digital envelope

A digital envelope for duty control can be added to the buzzer signal.
The envelope can be controlled by staged changing of the same duty envelope as detailed in Table 4.12.3.2 in the preceding item from level 1 (maximum) to level 8 (minimum).
The addition of an envelope to the buzzer signal can be done by writing "1" into ENON, but when "0" has been written it is not added.
When a buzzer signal output is begun (writing "1" into BZE) after setting ENON, the duty ratio shifts to level 1 (maximum) and changes in stages to level 8.
When attenuated down to level 8 (minimum), it is retained at that level. The duty ratio can be returned to maximum, by writing "1" into register ENRST during output of a envelope attached buzzer signal.
The envelope attenuation time (time for changing of the duty ratio) can be selected by the register ENRTM. The time for a 1 stage level change is 62.5 msec (16 Hz), when "0" has been written into ENRTM and 125 msec (8 Hz), when to "1" has been written. However, there is also a max. 4 msec error from envelope ON, up to the first change.
Figure 4.12.4.1 shows the timing chart of the digital envelope.

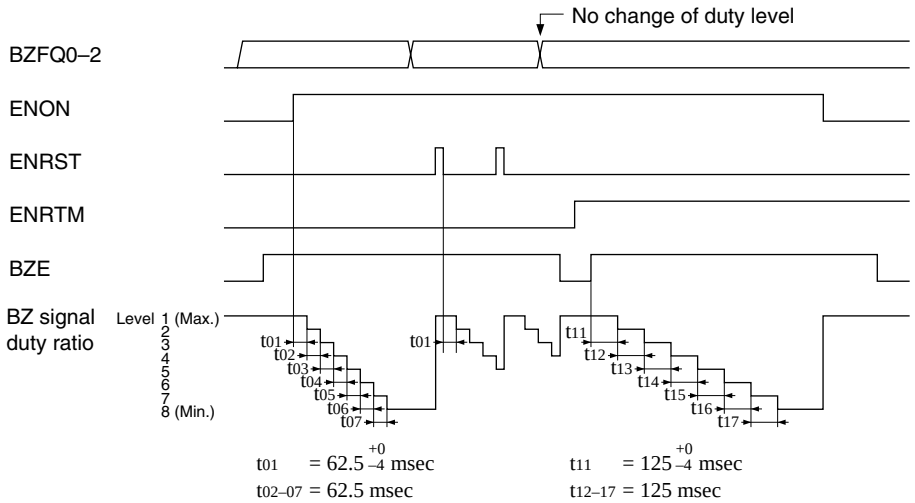


Fig. 4.12.4.1 Timing chart for digital envelope

4.12.5 One-shot output

The sound generator has a one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by SHTPW register for one-shot buzzer signal output time.
The output of the one-shot buzzer is controlled by writing "1" into the one-shot buzzer trigger BZSHT. When this trigger has been assigned, a buzzer signal in synchronization with the internal 256 Hz signal is output from the buzzer output terminal. Thereafter, when the set time has elapsed, a buzzer signal in synchronization with the 256 Hz signal goes off in the same manner as for the start of output.
The BZSHT also permits reading. When BZSHT is "1", the one-shot output circuit is in operation (during one-shot output) and when it is "0", it shows that the circuit is in the ready (outputtable) status.

In addition, it can also terminate one-shot output prior to the elapsing of the set time. This is done by writing a "1" into the one-shot buzzer stop BZSTP. In this case as well, the buzzer signal goes off in synchronization with the 256 Hz signal.

When "1" is written to BZSHT again during a one-shot output, a new one-shot output for 125 msec or 31.25 msec starts from that point (in synchronization with the 256 Hz signal).

The one-shot output cannot add an envelope for short durations. However, the sound level can be set by selecting the duty ratio, and the frequency can also be set.
One-shot output is invalid during normal buzzer output (during BZE = "1").

Figure 4.12.5.1 shows timing chart for one-shot output.

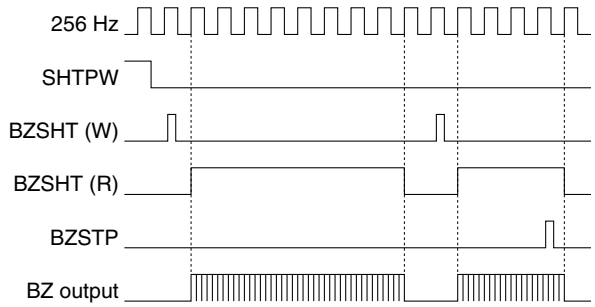


Fig. 4.12.5.1 Timing chart for one-shot output

4.12.6 I/O memory of sound generator

Table 4.12.6.1 shows the I/O addresses and the control bits for the sound generator.

Table 4.12.6.1 Control bits of sound generator

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
FF6DH	0	BZSTP	BZSHT	SHTPW	0 *3	– *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0 *3	– *2			Unused
					BZFQ2	0			Buzzer frequency selection [BZFQ2, 1, 0] 0 1 2 3 Frequency (Hz) 4096.0 3276.8 2730.7 2340.6 [BZFQ2, 1, 0] 4 5 6 7 Frequency (Hz) 2048.0 1638.4 1365.3 1170.3
	R	R/W			BZFQ1	0			
					BZFQ0	0			
FF6FH	0	BDTY2	BDTY1	BDTY0	0 *3	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
	R	R/W			BDTY1	0			
					BDTY0	0			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

BZE: Buzzer output control register (FF6CH•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output On
When "0" is written: Buzzer output Off
Reading: Valid

When "1" is written to BZE, the BZ signal is output from the BZ terminal.
When "0" is written, the BZ terminal goes to low (VSS).
At initial reset, this register is set to "0".

BZFQ0–BZFQ2: Buzzer frequency selection register (FF6EH•D0–D2)

Selects the buzzer signal frequency.

Table 4.12.6.2 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Select the buzzer frequency from among the above 8 types that have divided the oscillation clock.
At initial reset, this register is set to "0".

BDTY0–BDTY2: Duty level selection register (FF6FH•D0–D2)

Selects the duty ratio of the buzzer signal as shown in Table 4.12.6.3.

Table 4.12.6.3 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

The sound level of this buzzer can be set by selecting this duty ratio.
However, when the envelope has been set to on (ENON = "1"), this setting becomes invalid.
At initial reset, this register is set to "0".

ENRST: Envelope reset (FF6CH•D2)

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

Writing "1" into ENRST resets envelope and the duty ratio becomes maximum. If an envelope has not been added (ENON = "0") and if no buzzer signal is being output, the reset becomes invalid. Writing "0" is also invalid.
This bit is dedicated for writing, and is always "0" for reading.

ENON: Envelope On/Off control register (FF6CH•D1)

Controls the addition of an envelope onto the buzzer signal.

When "1" is written: On
When "0" is written: Off
Reading: Valid

Writing "1" into the ENON causes an envelope to be added during buzzer signal output. When a "0" has been written, an envelope is not added.
At initial reset, this register is set to "0".

ENRTM: Envelope releasing time selection register (FF6CH•D3)

Selects the envelope releasing time that is added to the buzzer signal.

When "1" is written: 1.0 sec (125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec (62.5 msec × 7 = 437.5 msec)
Reading: Valid

The releasing time of the digital envelope is determined by the time for converting the duty ratio.
When "1" has been written in ENRTM, it becomes 125 msec (8 Hz) units and when "0" has been written, it becomes 62.5 msec (16 Hz) units.
At initial reset, this register is set to "0".

SHTPW: One-shot buzzer pulse width setting register (FF6DH•D0)

Selects the output time of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

Writing "1" into SHTPW causes the one-short output time to be set at 125 msec, and writing "0" causes it to be set to 31.25 msec. It does not affect normal buzzer output.
At initial reset, this register is set to "0".

BZSHT: One-shot buzzer trigger/status (FF6DH•D1)

Controls the one-shot buzzer output.

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

Writing "1" into BZSHT causes the one-short output circuit to operate and a buzzer signal to be output. This output is automatically turned off after the time set by SHTPW has elapsed. The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

• ***When reading***

When "1" is read: BUSY
When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes off, it shifts to "0".
At initial reset, this bit is set to "0".

BZSTP: One-shot buzzer stop (FF6DH•D2)

Stops the one-shot buzzer output.

When "1" is written: Stop
When "0" is written: No operation
Reading: Always "0"

Writing "1" into BZSTP permits the one-shot buzzer output to be turned off prior to the elapsing of the time set by SHTPW. Writing "0" is invalid and writing "1" is also invalid except during one-shot output. This bit is dedicated for writing, and is always "0" for reading.

4.12.7 Programming notes

(1) Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

(2) The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

4.13 Integer Multiplier

4.13.1 Configuration of integer multiplier

The S1C63656 has a built-in unsigned-integer multiplier. This multiplier performs 8 bits × 8 bits of multiplication or 16 bits ÷ 8 bits of division and returns the results and three flag states.
Figure 4.13.1.1 shows the configuration of the integer multiplier.

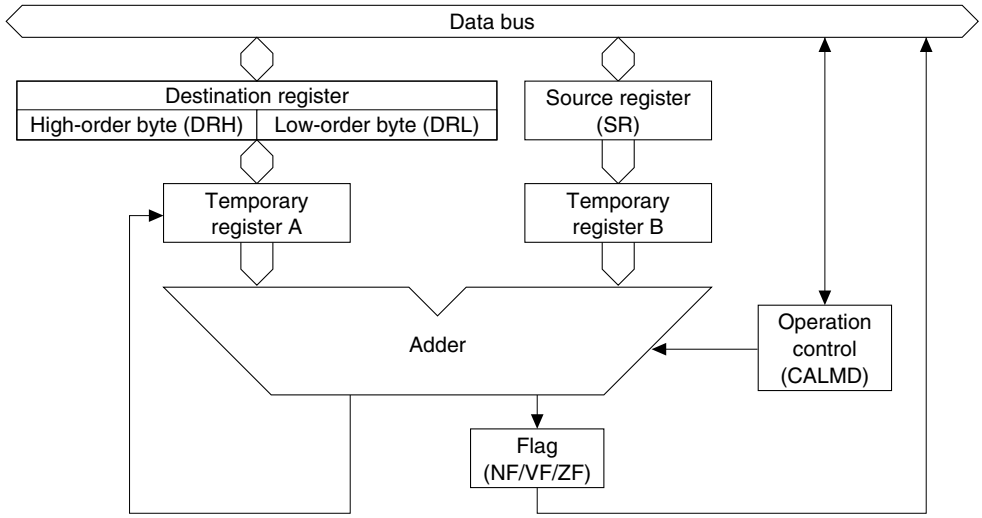


Fig. 4.13.1.1 Configuration of the integer multiplier

4.13.2 Multiplication mode

To perform a multiplication, set the multiplier to the source register (SR) and the multiplicand to the low-order 8 bits (DRL) of the destination register, then write "0" to the calculation mode selection register (CALMD). The multiplication takes 10 CPU clock cycles from writing "0" to CALMD until the 16-bit product is loaded into the destination register (DRH and DRL). At the same time the result is loaded, the operation flags (NF, VF and ZF) are updated.
The following shows the conditions that change the operation flag states and examples of multiplication.

N flag: Set when the MSB of DRH is "1" and reset when it is "0".
V flag: Always reset after a multiplication.
Z flag: Set when the 16-bit value in DRH/DRL is 0000H and reset when it is not 0000H.

<Examples of multiplication>

DRL (multiplicand)	SR (multiplier)	DRH/DRL (product)	NF	VF	ZF
00H	64H	0000H	0	0	1
64H	58H	2260H	0	0	0
C8H	58H	44C0H	0	0	0
C8H	A5H	80E8H	1	0	0

4.13.3 Division mode

To perform a division, set the divisor to the source register (SR) and the dividend to the destination register (DRH and DRL), then write "1" to the calculation mode selection register (CALMD). The division takes 10 CPU clock cycles from writing "1" to CALMD until the quotient is loaded into the low-order 8 bits (DRL) of the destination register and the remainder is loaded into the high-order 8 bits (DRH) of the destination register. At the same time the result is loaded, the operation flags (NF, VF and ZF) are updated.
However, when an overflow results (if the quotient exceeds the 8-bit range), the destination register (DRH and DRL) does not change its contents as it maintains the dividend.
The following shows the conditions that change the operation flag states and examples of division.

N flag: Set when the MSB of DRL is "1" and reset when it is "0".
V flag: Set when the quotient exceeds the 8-bit range and reset when it is within the 8-bit range.
Z flag: Set when the 8-bit value in DRL is 00H and reset when it is not 00H.

<***Examples of division***>

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
1A16H	64H	42H	4EH	0	0	0
332CH	64H	83H	00H	1	0	0
0000H	58H	00H	00H	0	0	1
2468H	13H	68H	24H	1	1	0

In the example of "2468H" ÷ "13H" shown above, DRH/DRL maintains the dividend because the quotient overflows the 8-bit. To get the correct results when an overflow has occurred, perform the division with two steps as shown below.

1. Divide the high-order 8 bits of the dividend (24H) by the divisor (13H) and then store the quotient (01H) to memory.

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
0024H	13H	01H	11H	0	0	0

2. Keep the remainder (11H) in DRH and load the low-order 8 bits of the dividend (68H) to DRL, then perform division again.

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
1168H	13H	EAH	0AH	1	0	0

The correct result is obtained as the quotient = 01EAH (the first and second results of DRL are merged) and the remainder = 0AH. However, since the operation flags (NF/VF/ZF) are changed in each step, they cannot indicate the states according to the final operation results.

Note: Make sure that the division results are correct using software as the hardware does not check.

4.13.4 Execution cycle

Both the multiplication and division take 10 CPU cycles for an operation. Therefore, before the results can be read from the destination register DRH/DRL, wait at least 5 bus cycles after writing to CALMD. The same applies to reading the operation flags NF/VF/ZF.
The following shows a sample program.

```
      ldb  %ext, src_data@h
      ldb  %xl, src_data@l      ; Set RAM address for operand
      ldb  %ext, au@h
      ldb  %yl, au@l            ; Set multiplier I/O memory address
;
      ldb  %ba, [%x]+
      ldb  [%y]+, %ba           ; Set data to SR
      ldb  %ba, [%x]+
      ldb  [%y]+, %ba           ; Set data to DRL
      ldb  %ba, [%x]+
      ldb  [%y]+, %ba           ; Set data to DRH
;
      ld   [%y], 0b0001         ; Start operation (select calculation mode)
;
      ldb  %ext, rslt_data@h
      ldb  %xl, rslt_data@l     ; Set result store address
      nop
      nop
      nop                       ; Dummy instructions to wait end of operation
;
      bit  [%y], 0b0100
      jrnz overflow             ; Jump to error routine if VF = "1"
;
      add  %y, -4               ; Set DRL again
;
      ldb  %ba, [%y]+
      ldb  [%x]+, %ba           ; Store result (quotient) into RAM
      ldb  %ba, [%y]+
      ldb  [%x]+, %ba           ; Store result (remainder) into RAM
```

4.13.5 I/O memory of integer multiplier

Table 4.13.5.1 shows the I/O addresses and the control bits for the integer multiplier.

Table 4.13.5.1 Control bits of integer multiplier

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF80H	SR3	SR2	SR1	SR0	SR3	– *2			Source register (low-order 4 bits)
					SR2	– *2			
					SR1	– *2			
	R/W				SR0	– *2			LSB
FF81H	SR7	SR6	SR5	SR4	SR7	– *2			MSB
					SR6	– *2			Source register (high-order 4 bits)
					SR5	– *2			
	R/W				SR4	– *2			
FF82H	DRL3	DRL2	DRL1	DRL0	DRL3	– *2			Low-order 8-bit destination register (low-order 4 bits)
					DRL2	– *2			
					DRL1	– *2			
	R/W				DRL0	– *2			LSB
FF83H	DRL7	DRL6	DRL5	DRL4	DRL7	– *2			MSB
					DRL6	– *2			Low-order 8-bit destination register (high-order 4 bits)
					DRL5	– *2			
	R/W				DRL4	– *2			
FF84H	DRH3	DRH2	DRH1	DRH0	DRH3	– *2			High-order 8-bit destination register (low-order 4 bits)
					DRH2	– *2			
					DRH1	– *2			
	R/W				DRH0	– *2			LSB
FF85H	DRH7	DRH6	DRH5	DRH4	DRH7	– *2			MSB
					DRH6	– *2			High-order 8-bit destination register (high-order 4 bits)
					DRH5	– *2			
	R/W				DRH4	– *2			
FF86H	NF	VF	ZF	CALMD	NF	0	Negative	Positive	Negative flag
					VF	0	Overflow	No	Overflow flag
					ZF	0	Zero	No	Zero flag
	R			R/W	CALMD	0	Run	Stop	Operation status (reading)
							Div.	Mult.	Calculation mode selection (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SR0–SR7: Source register (FF80H, FF81H)

Used to set multipliers and divisors.
Set the low-order 4 bits of data to SR0–SR3 and the high-order 4 bits to SR4–SR7.
This register maintains the latest set value until the next writing, so it is not necessary to set data for each operation if the same multiplier and divisor is used in a series of operations.
At initial reset, this register is undefined.

DRL0–DRL7: Destination register low-order 8 bits (FF82H, FF83H)

Used to set multiplicands and low-order 8 bits of dividends.
Set the low-order 4 bits of data to DRL0–DRL3 and the high-order 4 bits to DRL4–DRL7.
Data written to this register is loaded to the arithmetic circuit when an operation starts (by writing to FF86H•D0), and then a multiplication or a division is performed in 10 CPU clock cycles (5 bus cycles).
After the operation has finished, the low-order 8 bits of the product or the quotient are loaded to this register.
However, if an overflow occurs in a division process, the quotient is not loaded and the low-order 8 bits of the dividend remains.
At initial reset, this register is undefined.

DRH0–DRH7: Destination register high-order 8 bits (FF84H, FF85H)

Used to set high-order 8 bits of dividends.
Set the low-order 4 bits of data to DRH0–DRH3 and the high-order 4 bits to DRH4–DRH7.
At the start of a multiplication (by writing "0" to FF86H•D0), the contents in this register are ignored.
After 10 CPU cycles (5 bus cycles) of multiplication process has finished, the high-order 8 bits of the product are loaded in this register.
In a division process, data written to this register is loaded to the arithmetic circuit when an operation starts (by writing "1" to FF86H•D0), and then a division is performed in 10 CPU clock cycles (5 bus cycles). After the operation has finished, the remainder is loaded to this register. However, if an overflow occurs in a division process, the remainder is not loaded and the high-order 8 bits of the dividend remains.
At initial reset, this register is undefined.

NF: Negative flag (FF86H•D3)

Indicates whether the operation result is a positive value or a negative value.

When "1" is read: Negative value (MSB of the results is "1")
When "0" is read: Positive value (MSB of the results is "0")
Writing: Invalid

NF is a read-only bit, so writing operation is invalid.
At initial reset, this flag is set to "0".

VF: Overflow flag (FF86H•D2)

Indicates whether an overflow has occurred or not in a division process.

When "1" is read: Overflow occurred
When "0" is read: Overflow has not occurred
Writing: Invalid

When a multiplication process has finished, this flag is always set to "0".
VF is a read-only bit, so writing operation is invalid.
At initial reset, this flag is set to "0".

ZF: Zero flag (FF86H•D1)

Indicates whether the operation result is zero or not.

When "1" is read: Zero
When "0" is read: Not zero
Writing: Invalid

ZF is a read-only bit, so writing operation is invalid.
At initial reset, this flag is set to "0".

CALMD: Calculation mode selection register/operation status (FF86H•D0)

Selects multiplication or division mode and starts operation.

When "1" is written: Selects/starts division
When "0" is written: Selects/starts multiplication
When "1" is read: Under operating
When "0" is read: Operation has finished

Writing to this register starts the specified operation. After that, this register is set to "1" and returns to "0" when the multiplication or division process has finished.
At initial reset, this register is reset to "0".

4.13.6 Programming note

An operation process takes 10 CPU clock cycles (5 bus cycles) after writing to the calculation mode selection register CALMD until the operation result is set to the destination register DRH/DRL and the operation flags. While this operation is in process, do not read/write from/to the destination register DRH/DRL and do not read NF/VF/ZF.

4.14 R/f Converter

4.14.1 Configuration of R/f converter

The S1C63656 has a CR oscillation type R/f converter.
Two systems (channel 0 and channel 1) of CR oscillation circuit are built into this R/f converter, so it is possible to compose two types of R/f conversion circuits by connecting different sensors to each CR oscillation circuit.
Channel 0 can be used as an R/f conversion circuit using a resistive sensor such as a thermistor, and channel 1 can be used as an R/f conversion circuit same as channel 0, or an R/f conversion circuit for humidity conversion using a resistive humidity sensor.
The channel to be used and sensor type for channel 1 are selected using software.
Resistance value (relative value to external reference resistance) of the resistive sensor that has been connected to the sensor input terminal is converted into frequency by the CR oscillation circuit and the number of clocks is counted in the built-in measurement counter. By reading the value of the measurement counter, it can obtain the data after digitally-converting the value detected by the sensor.
Various sensor circuits such as temperature/humidity measurement circuits can be easily realized using this R/f converter.
The configuration of the R/f converter is shown in Figure 4.14.1.1.

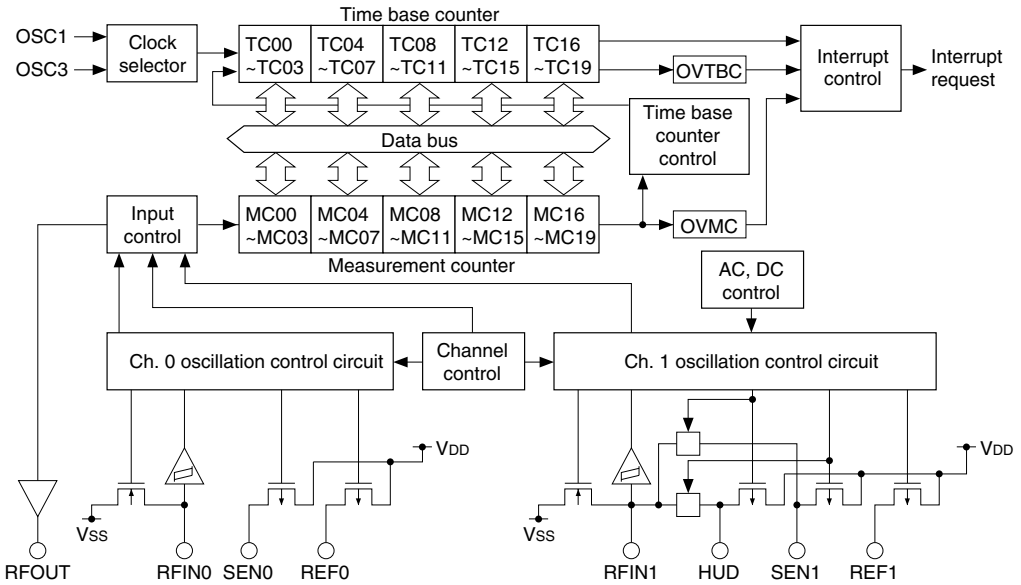


Fig. 4.14.1.1 Configuration of R/f converter

4.14.2 Connection terminals and CR oscillation circuit

Two systems of CR oscillation circuit, channel 0 and channel 1, are built into the R/f converter and perform CR oscillation with external resistor and capacitor.
The counter that is used to obtain an R/f converted value is shared with channel 0 and channel 1. Therefore, operation for two systems is realized by switching the CR oscillation circuit that performs R/f conversion. The channel selection is done using the register SENSEL. When SENSEL is set to "0", channel 0 is selected and when "1" is set, channel 1 is selected.
The sensor type to be R/f converted in the channel 1 can also be selected by the software, and it should be previously set using the register RFSEL.

Channel selection	SENSEL = "0":	Channel 0
	SENSEL = "1":	Channel 1
Sensor selection for channel 1	RFSEL = "0":	R/f conversion using a resistive sensor such as thermistor
	RFSEL = "1":	R/f conversion using a resistive humidity sensor *

* The operation of the oscillation circuit differs from the normal resistive sensor. (Refer to the following.)

(1) R/f conversion using a resistive sensor such as thermistor

Channel 0 is set only for this conversion method, and channel 1 is selected into this method by setting RFSEL to "0". This method should be selected for R/f conversion using a normal resistive sensor (DC bias), such as temperature measurement using thermistor. At initial reset, channel 1 is set into this conversion method.
Figure 4.14.2.1 shows the connection diagram of external elements.

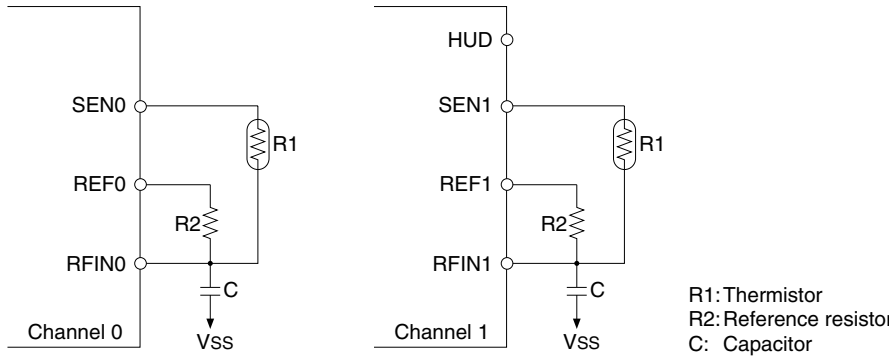


Fig. 4.14.2.1 Connection diagram in case of R/f conversion

Connect a resistive sensor (such as a thermistor) between the SEN0 (SEN1) and RFIN0 (RFIN1) terminals.
Next, set the reference value of the item to be measured (e.g. reference temperature in the case of temperature measurement) and connect the reference resistance equivalent to the sensor resistance value at the above reference value between the REF0 (REF1) and RFIN0 (RFIN1) terminals. An element that does not change due to temperature or other environmental conditions must be used as the reference resistance.
Connect an oscillating capacitor that is used for CR oscillation of both the reference resistance and the sensor between the RFIN0 (RFIN1) and VSS terminals.
The HUD terminal should be opened because it is not used in this method.

The R/f converter performs CR oscillation using each of the two resistances (sensor and reference resistance) in the same period, and counts the CR oscillation clock. Difference in counted oscillation frequency can be evaluated in terms of the difference between the respective resistance values. Measurement results can be obtained from the changes in resistance values after correcting the difference according to the program.

The CR oscillation circuit is designed so that either the reference resistance side or the sensor side can be operated independently by the oscillation control circuit.
Each circuit performs the same oscillating operation as follows:

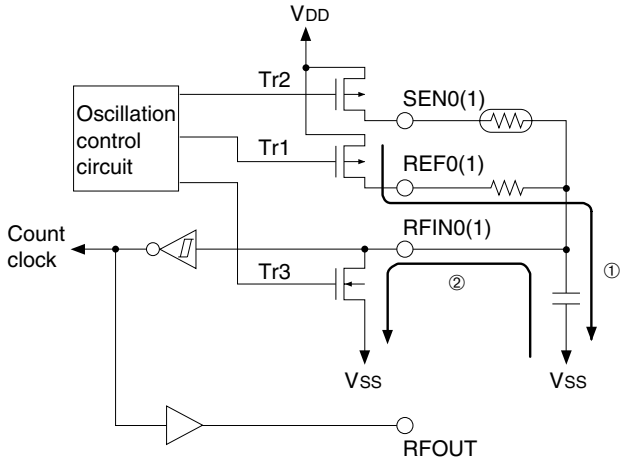


Fig. 4.14.2.2 CR oscillation circuit (DC bias)

The Tr1 (Tr2) turns on first, and the capacitor connected between the REF (SEN) and VSS terminals is charged through the reference resistance (sensor). If the voltage level of the RFIN terminal decreases, the Tr1 (Tr2) turns off and the Tr3 turns on. As a result, the capacitor becomes discharged, and oscillation is performed according to CR time constant. The time constant changes as the sensor resistance value fluctuates, producing a difference from the oscillation frequency of the reference resistance.

Oscillation waveforms are shaped by the schmitt trigger and transmitted to the measurement counter. The clock transmitted to the measurement counter is also output from the RFOUT terminal while the sensor is oscillating. As a result, oscillation frequency can be identified by the oscilloscope. Since this monitor has no effect on oscillation frequency, it can be used to adjust R/f conversion accuracy.
Oscillation waveforms and waveforms output from the RFOUT terminal are shown in Figure 4.14.2.3. The "L" pulse width of the RFOUT output must be 10 µsec or more (when V_{DD} = 3.0 V, $R_{SEN0/1}$ = 50 kΩ, C_{RF} = 1000 pF).

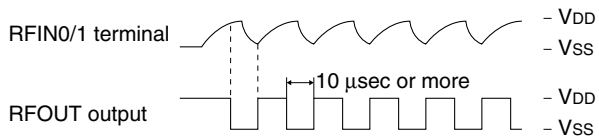


Fig. 4.14.2.3 Oscillation waveform

(2) R/f conversion using a resistive humidity sensor

This conversion is possible only in channel 1, and this method is selected by setting the RFSEL register to "1". This is basically the same as the R/f conversion described above (1), but the AC bias circuit works for the humidity sensor.
Figure 4.14.2.4 shows the connection diagram of external devices.

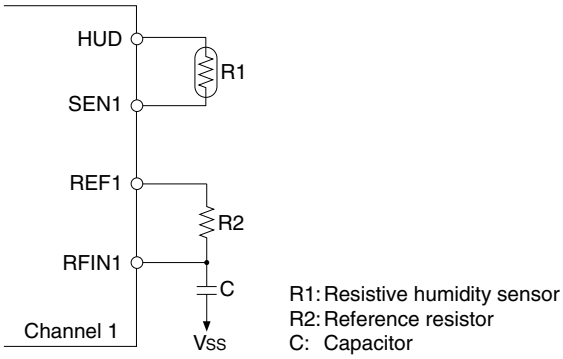


Fig. 4.14.2.4 Connection diagram of resistive humidity sensor

Connect a humidity sensor between the HUD and SEN1 terminals, and connect a reference resistance between the REF1 and RFIN1 terminals.
Connect an oscillating capacitor that is used for CR oscillation of both the reference resistance and the sensor between the RFIN1 and VSS terminals.
The oscillating operation by reference resistance is the same as the R/f conversion described above (1). The humidity sensor cannot be DC biased for a long time, therefore this method powers the HUD and SEN1 terminals alternately.

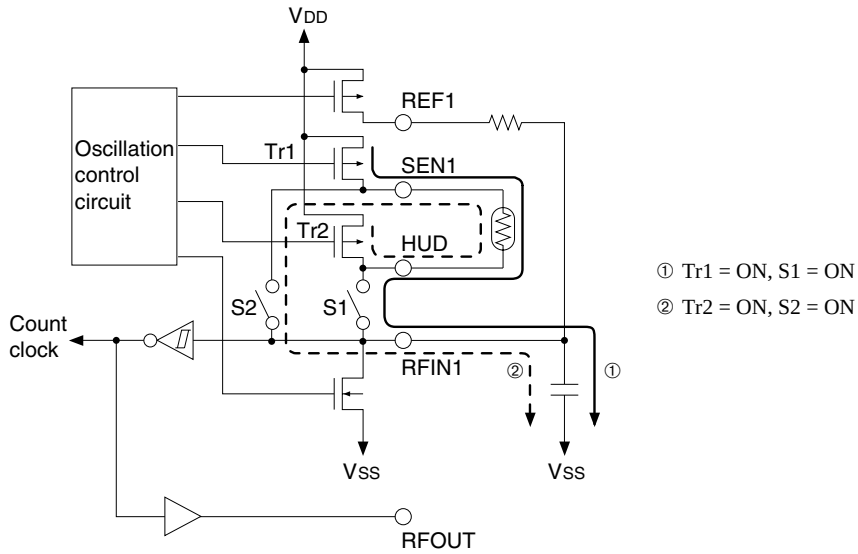


Fig. 4.14.2.5 CR oscillation circuit for resistive humidity sensor

The oscillation waveform is the same as Figure 4.14.2.3.

4.14.3 Operation of R/f conversion

Counter

The R/f converter incorporates two types of counters: measurement counter MCxx and time base counter TCxx. The measurement counter is a 20-bit up counter that counts the CR oscillation clock with the reference resistance or sensor selected by software. The time base counter is a 20-bit up/down counter to equal both oscillation times for the reference resistance and the sensor. The time base counter uses the count clock selected by the RFCLK register (OSC1 or OSC3). Each counter permits reading and writing on a 4-bit basis.

First start an R/f conversion for the reference resistance. The measurement counter starts counting up and the time base counter starts counting down. The counters stop counting when the measurement counter overflows (counter = 00000H). By resetting the time base counter to 00000H before starting an R/f conversion for the reference resistance, the reference oscillation time will be obtained from the time base counter.

Then start an R/f conversion for the sensor, the measurement counter starts counting up from 00000H and the time base counter starts counting up from the counted value. The counters stop counting when the time base counter overflows (counter = 00000H). The oscillation time in this phase is the same as that of the reference resistance.

Therefore, by converting a proper initial value for counting of the oscillation of the reference resistance into a complement (value subtracted from 00000H) and setting it into the measurement counter before starting to count, the number of counts for the sensor oscillation is obtained by reading the measurement counter after the R/f conversion. In other words, the difference between the reference resistance and sensor oscillation frequencies can be found easily. For instance, if resistance values of the reference resistance and the sensor are equivalent, the same value as the initial value before converting into a complement will be obtained as the result.

The time base counter allows reading of the counter value and presetting of data. By saving the counter value after the reference oscillation has completed into the RAM, the subsequent reference oscillation phase can be omitted. The sensor oscillation can be started after setting the saved value to the time base counter and 00000H to the measurement counter.

Note: When setting the measurement counter, always write 5 words of data continuously in order from the lower address (FF92H → FF93H → FF94H → FF95H → FF96H). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used.

R/f conversion sequence

An R/f conversion for the reference resistance starts by writing "1" to the register RFRUNR. However, an initial value must be set to the measurement counter and the time base counter must be cleared to 00000H before starting the R/f conversion.

When R/f conversion is initiated by the RFRUNR register, oscillation by the reference resistance begins, and the measurement counter starts counting up from the initial value by the oscillation clock. The time base counter also starts counting down by the OSC1 clock.

If the measurement counter becomes 00000H due to overflow, the oscillation is terminated. At the same time an interrupt occurs and the RFRUNR register is set to "0", and the R/f converter circuit stops operation completely.

The time base counter value should be saved into the RAM for R/f conversion of the sensor.

Figure 4.14.3.1 shows a timing chart for the reference oscillation.

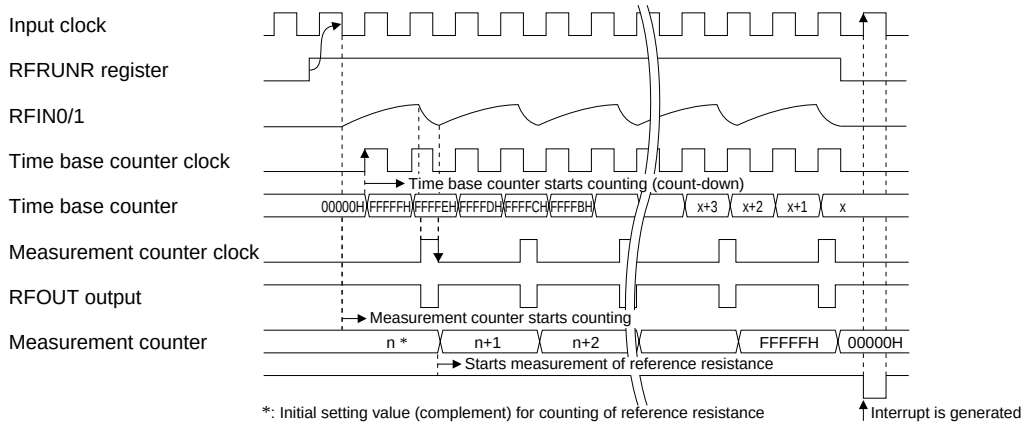


Fig. 4.14.3.1 Reference oscillation timing chart

CR oscillation starts in synchronization with the falling edge of the input clock immediately after writing "1" to the RFRUNR register. The measurement counter starts counting up at the falling edge of the first clock after CR oscillation is initiated. The time base counter is enabled at the falling edge of the first input clock. Then, it counts down by the rising edge of the input clock. The RFRUNR register is set to "0" at the falling edge of the input clock immediately after the measurement counter stops. Interrupt conditions are sampled with the OSC1 clock, so an interrupt occurs in synchronization with the rising edge of the OSC1 clock immediately after the RFRUNR register is set to "0".

An R/f conversion for the sensor starts by writing "1" to the register RFRUNS. When performing this sensor oscillation after an reference oscillation has completed, it is not necessary to set initial values to the counters. If converting the sensor resistance independently, the measurement counter must be set to 00000H and the time base counter must be set to the value measured at the time of a reference oscillation. When R/f conversion is initiated by the RFRUNS register, oscillation by the sensor begins, and the measurement counter starts counting up from 00000H by the oscillation clock. The time base counter also starts counting up by the input clock. If the time base counter becomes 00000H, the oscillation is terminated. At the same time an interrupt occurs and the RFRUNS register is set to "0", and the R/f converter circuit stops operation completely.
Figure 4.14.3.2 shows a timing chart for the sensor oscillation.

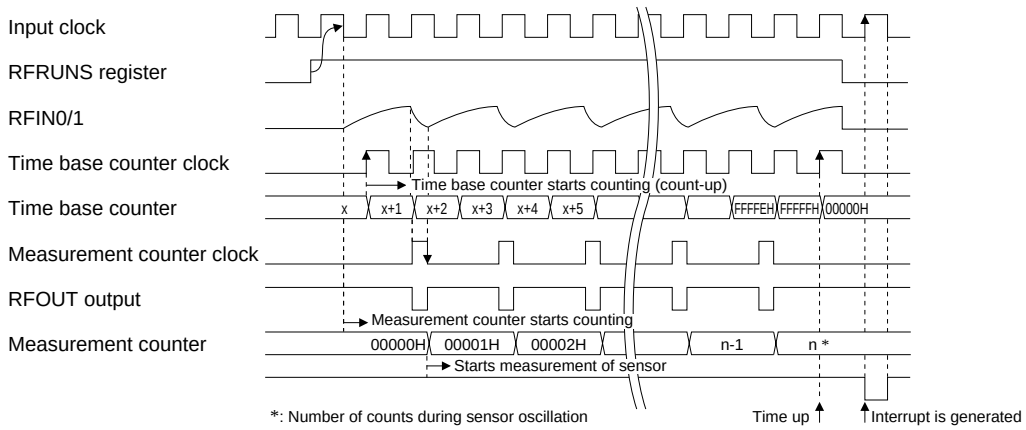


Fig. 4.14.3.2 Sensor oscillation timing chart

The sensor oscillation starts in synchronization with the falling edge of the input clock immediately after writing "1" to the RFRUNS register. The measurement counter starts counting up at the falling edge of the first clock after CR oscillation is initiated.
The time base counter is enabled at the falling edge of the first input clock. Then, it counts up by the rising edge of the input clock. Depending on the timing, the measurement counter may not count the CR oscillation clock at the time RFRUNS is set to "0".

The RFRUNS register is set to "0" at the falling edge of the input clock immediately after the time base counter reaches 00000H. Interrupt conditions are sampled with the OSC1 clock, so an interrupt occurs in synchronization with the rising edge of the OSC1 clock immediately after the RFRUNS register is set to "0".

By the above operation, the sensor is oscillated for the same period of time as the reference resistance is oscillated. Therefore, the difference in oscillation frequency can be measured from the values counted by the measurement counter.

Since the reference resistance is oscillated until the measurement counter overflows, an appropriate initial value needs to be set before R/f conversion is started. If a smaller initial value is set, a longer counting period is possible, thereby ensuring more accurate detection. However, the time base counter may overflow while counting the oscillation frequency of the reference resistance.
If an overflow occurs, CR oscillation and R/f conversion is terminated immediately. Also in such cases, an interrupt occurs. Moreover, the measurement counter may overflow while counting the sensor oscillation depending on initial value setting. If the measurement counter overflows, CR oscillation and R/f conversion is terminated at that point and an interrupt occurs.
When these overflows occur, the correct value cannot be read. Therefore, the overflow flags are provided to judge whether the read data is correct or an overflow occurs. There are two overflow flags; OVMC that indicates an measurement counter overflow and OVTBC that indicates an time base counter overflow. These flags are set to "1" if respective counter overflows. These flags are reset to "0" when R/f conversion is started or when "1" is written to the flag. When the interrupt occurs, be sure to read the overflow flags and check overflow.
The initial value to be set depends on the measurable range by the sensor or where to set the reference resistance value within that range.
The initial value must be set taking the above into consideration.

Convert the initial value into a complement (value subtracted from 00000H) before setting it on the measurement counter. Since the data output from the measurement counter after R/f conversion matches data detected by the sensor, process the difference between that value and the initial value before it is converted into a complement according to the program and calculate the target value.

The above operations are shown in Figure 4.14.3.3.

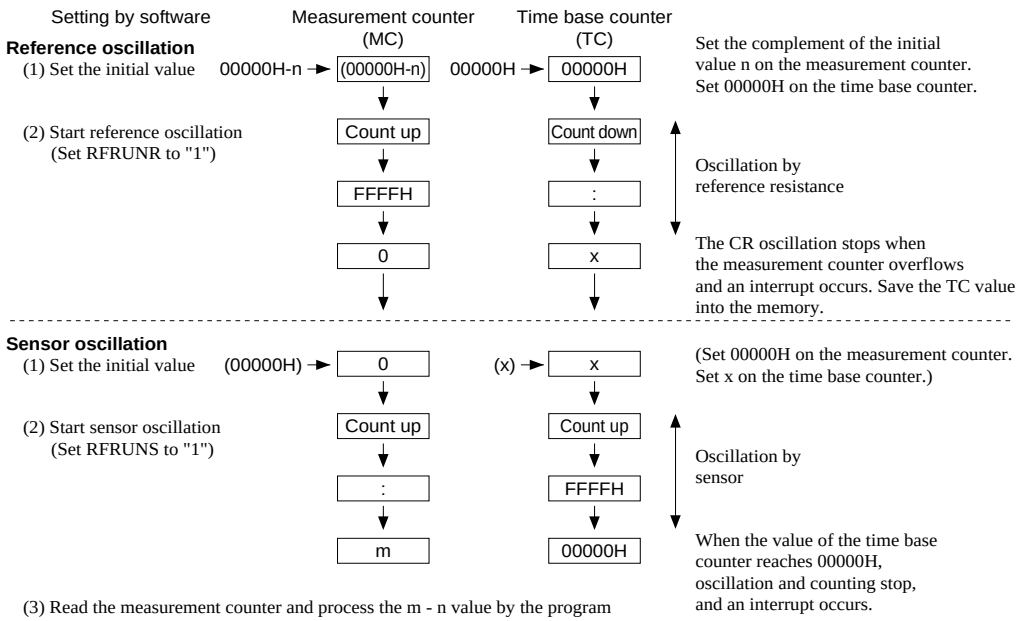


Fig. 4.14.3.3 Sequence of R/f conversion

Note: Set the initial value of the measurement counter taking into account the measurable range and the overflow of counters.

4.14.4 Interrupt function

The R/f converter has a function which allows interrupt to occur after R/f conversion.
When the measurement counter is counted up to 00000H, both counters stop counting. The interrupt factor flag IRFB is set to "1" at the rising edge of the OSC1 clock immediately after RFRUNR is set to "0" and an interrupt occurs.
When the time base counter is counted down to 00000H, both counters stop counting. The interrupt factor flag IRFM is set to "1" at the rising edge of the OSC1 clock immediately after the RFRUNS register is set to "0" and an interrupt occurs.
If the measurement counter overflows during counting of the sensor oscillation, or the time base counter overflows during counting of the reference resistance oscillation, the interrupt factor flag IRFM or IRFB is also set to "1". These interrupt factors allow masking by the interrupt mask registers EIRFM and EIRFB. When the EIRFM/EIRFB has been set at "1", an interrupt occurs in the CPU. When the EIRFM/EIRFB is set at "0", no interrupt will occur in the CPU even if the interrupt factor flag is set to "1". The interrupt factor flag is reset to "0" by writing "1".
Timing of interrupt by the R/f converter is shown in Figures 4.14.4.1 to 4.14.4.4.

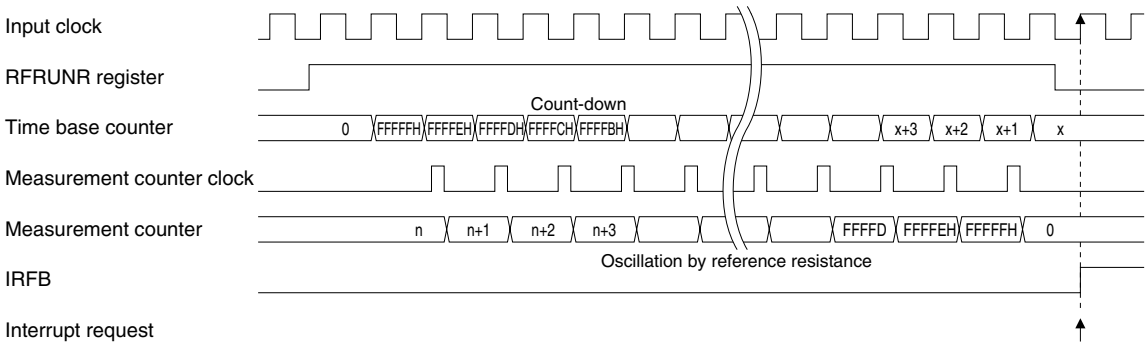


Fig. 4.14.4.1 Reference oscillate completion interrupt

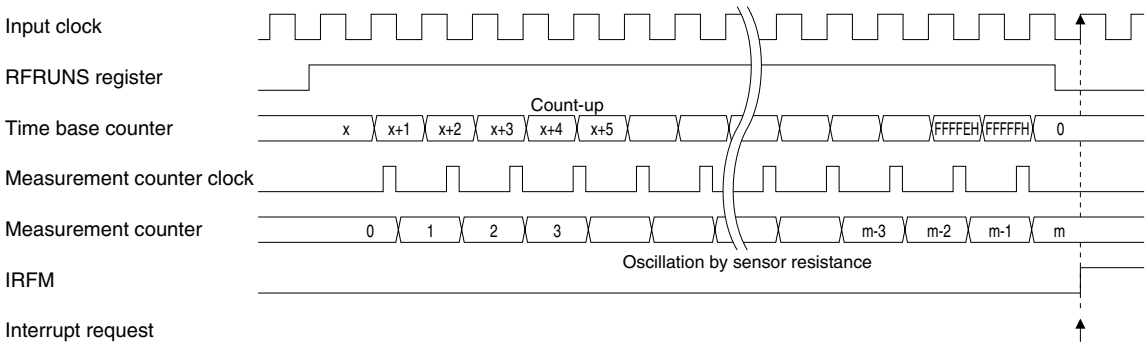


Fig. 4.14.4.2 Sensor oscillate completion interrupt

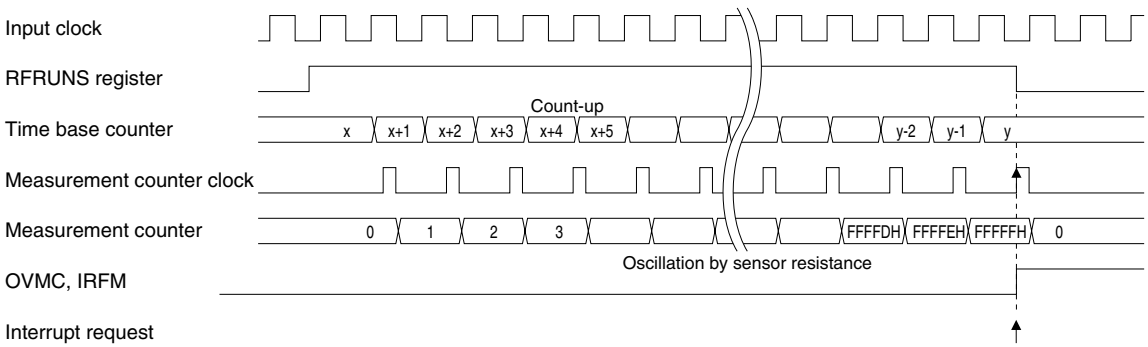


Fig. 4.14.4.3 Measurement counter overflow interrupt

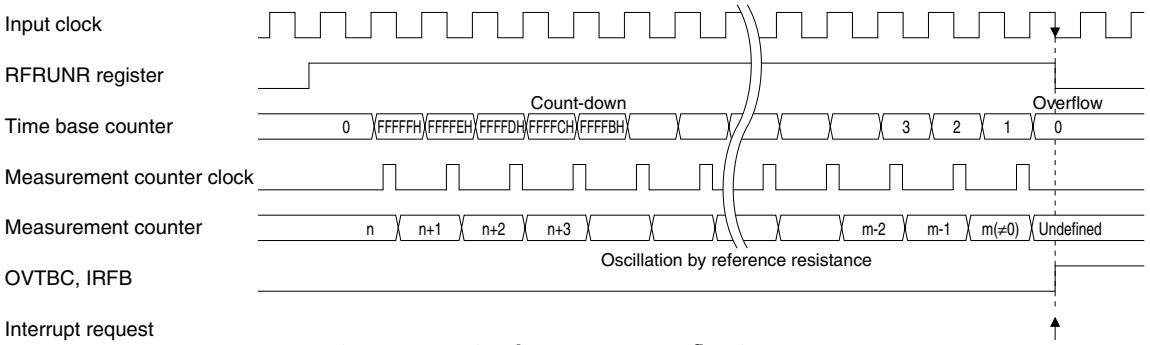


Fig. 4.14.4.4 Time base counter overflow interrupt

Note: • *When the R/f converter interrupt is generated, be sure to check whether or not the R/f conversion has completed normally by reading the overflow flags.*

• *When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/f converter interrupt occurs.*

4.14.5 I/O memory of R/f converter

Table 4.14.5.1 shows the I/O addresses and the control bits for the R/f converter.

Table 4.14.5.1 Control bits of R/f converter

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF90H	0	RFCLK	RFSEL	SENSEL	0 *3	– *2			Unused
					RFCLK	0	OSC3	OSC1	R/f conversion clock selection
	R	R/W			RFSEL	0	AC	DC	Ch. 1 sensor type selection
					SENSEL	0	Ch. 1	Ch. 0	Conversion channel selection
FF91H	OVTBC	OVMC	RFRUNR	RFRUNS	OVTBC	0	Overflow	Non-ov	Time base counter overflow flag
					OVMC	0	Overflow	Non-ov	Measurement counter overflow flag
	R/W				RFRUNR	0	Run	Stop	Reference oscillation Run control/status (writing "0" is ineffective)
					RFRUNS	0	Run	Stop	Sensor oscillation Run control/status (writing "0" is ineffective)
FF92H	MC3	MC2	MC1	MC0	MC3	– *2			Measurement counter MC0–MC3
					MC2	– *2			
	R/W				MC1	– *2			
					MC0	– *2			LSB
FF93H	MC7	MC6	MC5	MC4	MC7	– *2			Measurement counter MC4–MC7
					MC6	– *2			
	R/W				MC5	– *2			
					MC4	– *2			
FF94H	MC11	MC10	MC9	MC8	MC11	– *2			Measurement counter MC8–MC11
					MC10	– *2			
	R/W				MC9	– *2			
					MC8	– *2			
FF95H	MC15	MC14	MC13	MC12	MC15	– *2			Measurement counter MC12–MC15
					MC14	– *2			
	R/W				MC13	– *2			
					MC12	– *2			
FF96H	MC19	MC18	MC17	MC16	MC19	– *2			MSB
					MC18	– *2			Measurement counter MC16–MC19
	R/W				MC17	– *2			
					MC16	– *2			
FF97H	TC3	TC2	TC1	TC0	TC3	– *2			Time base counter TC0–TC3
					TC2	– *2			
	R/W				TC1	– *2			
					TC0	– *2			LSB
FF98H	TC7	TC6	TC5	TC4	TC7	– *2			Time base counter TC4–TC7
					TC6	– *2			
	R/W				TC5	– *2			
					TC4	– *2			
FF99H	TC11	TC10	TC9	TC8	TC11	– *2			Time base counter TC8–TC11
					TC10	– *2			
	R/W				TC9	– *2			
					TC8	– *2			
FF9AH	TC15	TC14	TC13	TC12	TC15	– *2			Time base counter TC12–TC15
					TC14	– *2			
	R/W				TC13	– *2			
					TC12	– *2			
FF9BH	TC19	TC18	TC17	TC16	TC19	– *2			MSB
					TC18	– *2			Time base counter TC16–TC19
	R/W				TC17	– *2			
					TC16	– *2			
FFE7H	0	0	EIRFB	EIRFM	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIRFB	0	Enable	Mask	Interrupt mask register (R/f converter reference oscillate completion)
					EIRFM	0	Enable	Mask	Interrupt mask register (R/f converter sensor oscillate completion)
FFF7H	0	0	IRFB	IRFM	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IRFB	0	(W)	(W)	Interrupt factor flag (R/f converter reference oscillate completion)
					IRFM	0	Reset	Invalid	Interrupt factor flag (R/f converter sensor oscillate completion)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

MC0–MC19: Measurement counter (FF92H–FF96H)

The measurement counter counts up according to the CR oscillation clock. It permits writing and reading on a 4-bit basis.
The complement of the number of clocks to be counted by the oscillation of the reference resistance must be entered in this counter prior to reference oscillation. When the counter reaches 00000H due to overflow, the oscillation of the reference resistance stops. When converting a sensor oscillation, 00000H must be set in this register (it is unnecessary when it is done immediately after a reference oscillation has completed). The sensor oscillation and measurement counter stop when the time base counter overflows. Number of clocks counted by the sensor oscillation can be evaluated from the value indicated by the counter when it stops. Calculate the target value by processing the above counted number according to the program. Measurable range and the overflow of the counter must be taken into account when setting an initial value to be entered prior to R/f conversion.
At initial reset, this counter is undefined.

TC0–TC19: Time base counter (FF97H–FF9BH)

Writing and reading is possible on a 4-bit basis by the time base counter that is used to adjust the CR oscillation time between the reference resistance and the sensor.
The time base counter counts down during oscillation of the reference resistance and counts up to 00000H during oscillation of the sensor.
00000H needs to be entered in the counter prior to a reference oscillation in order to adjust the CR oscillating time (number of clocks) of both counts. The counter value after a reference oscillation has completed should be read from this register and save it in the memory. The saved value should be set in this counter before starting a sensor oscillation.
At initial reset, this counter is undefined.

RFCLK: Input clock selection (FF90H•D2)

Selects the clock input to the time base counter.

When "1" is written: OSC3
When "0" is written: OSC1
Reading: Valid

Select the count clock for the time base counter. When "1" is written to RFCLK, the OSC3 clock is selected. When "0" is written, the OSC1 clock (Typ. 32 kHz) is selected. To select the OSC3 clock, the OSC3 oscillation frequency must be 2 MHz or less.
At initial reset, this register is set to "0".

RFSEL: Sensor selection for channel 1 (FF90H•D1)

Selects a sensor type to be used for channel 1.

When "1" is written: Resistive humidity sensor
When "0" is written: Resistive sensor
Reading: Valid

When "1" is written to RFSEL, a resistive humidity sensor is selected as the sensor for channel 1. When "0" is written, a normal resistive sensor is selected.
At initial reset, this register is set to "0".

SENSEL: Channel selection register (FF90H•D0)

Selects the channel to be converted.

When "1" is written: Channel 1
When "0" is written: Channel 0
Reading: Valid

When "1" is written to SENSEL, channel 1 is selected for R/f conversion and when "0" is written, channel 0 is selected.
At initial reset, this register is set to "0".

RFRUNR: Reference oscillation RUN control/status (FF91H•D1)
Starts R/f conversion for the reference resistance and indicates the operating (RUN/STOP) status.

When "1" is written: R/f conversion starts
When "0" is written: No operation

When "1" is read: RUN status
When "0" is read: STOP status

When "1" is written to RFRUNR, R/f conversion for the reference resistance starts. The register remains at "1" during R/f conversion and is set to "0" when R/f conversion is terminated.
Writing "0" to RFRUNR is invalid.
At initial reset, this register is set to "0".

RFRUNS: Sensor oscillation RUN control/status (FF91H•D0)
Starts R/f conversion for the sensor and indicates the operating (RUN/STOP) status.

When "1" is written: R/f conversion starts
When "0" is written: No operation

When "1" is read: RUN status
When "0" is read: STOP status

When "1" is written to RFRUNS, R/f conversion for the sensor starts. The register remains at "1" during R/f conversion and is set to "0" when R/f conversion is terminated.
Writing "0" to RFRUNS is invalid.
At initial reset, this register is set to "0".

OVMC: Measurement counter overflow flag (FF91H•D2)
Indicates whether the measurement counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred

When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the sensor, OVMC is set to "1" and the interrupt occurs at the same time.
This flag is reset by writing "1" or starting R/f conversion.
At initial reset, this flag is set to "0".

OVTBC: Time base counter overflow flag (FF91H•D3)
Indicates whether the time base counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred

When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the reference resistance, OVTBC is set to "1" and the interrupt occurs at the same time.
This flag is reset by writing "1" or starting R/f conversion.
At initial reset, this flag is set to "0".

EIRFM, EIRFB: Interrupt mask registers (FFE7H•D0, D1)

Select whether to mask interrupt with the R/f converter.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

EIRFM and EIRFB are the interrupt mask registers for the sensor oscillate completion interrupt and the reference oscillate completion interrupt. The R/f converter interrupt is permitted when "1" is written to EIRFM and EIRFB. When "0" is written, interrupt is masked.
At initial reset, these registers are set to "0".

IRFM, IRFB: Interrupt factor flags (FFF7H•D0, D1)

These flags indicate the status of the R/f converter interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

IRFB is set to "1" when an R/f conversion for the reference resistor is terminated or when the time base counter overflows while counting the oscillation of the reference resistance.
IRFM is set to "1" when an R/f conversion for the sensor is terminated or when the measurement counter overflows while counting the oscillation of the sensor.
From the status of these flags, the software can decide whether an R/f converter interrupt has occurred. Further this flag is set in the above timing regardless of the interrupt mask register setting (except for debug mode). These flags are reset to "0" by writing "1". After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
After an initial reset, these flags are set to "0".

4.14.6 Programming notes

(1) Depending on the initial value of the measurement counter (MC), the measurement counter or the time base counter may overflow while the CR oscillation clock is being counted. When setting the initial value, pay attention to CR oscillation frequency, its fluctuation range and the input clock frequency of the time base counter. If an overflow occurs, R/f conversion is terminated immediately. When the R/f conversion result (measurement counter value) is read, check the overflow flags (OVMC and OVTBC). The upper limit of the CR oscillation frequency is 500 kHz. There is no lower-limit but make sure that the time base counter does not overflow.

(2) When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/f converter interrupt occurs.

(3) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(4) When selecting OSC3 for the time base counter clock, the maximum frequency of the OSC3 clock is limited to 2 MHz.

(5) When setting the measurement counter, always write 5 words of data continuously in order from the lower address (FF92H → FF93H → FF94H → FF95H → FF96H). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used.

4.15 Stepping Motor Driver

4.15.1 Configuration of stepping motor driver

The S1C63656 has 2 channels (Ch. 1 and Ch. 2) of stepping motor drivers allowing control of two stepping motors. By configuring the timing signal with software, low-power combination clocks and watches can be implemented.
Figure 4.15.1.1 shows the configuration of the motor driver.

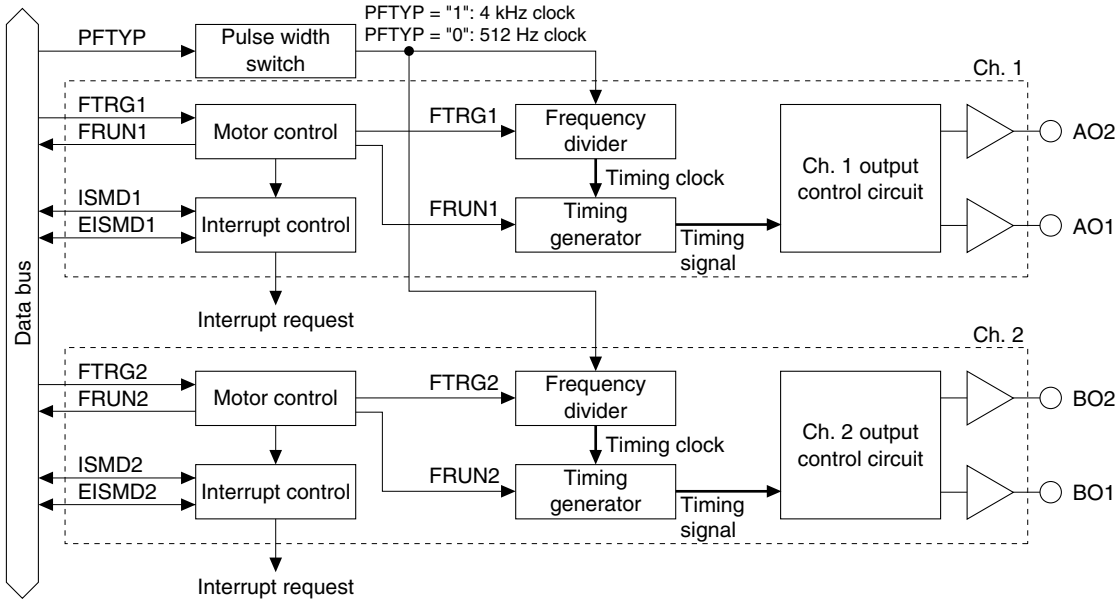


Fig. 4.15.1.1 Configuration of motor driver

4.15.2 Setting up the motor-drive pulse

This motor driver supports stepping motors for watches and clocks.
A different motor-drive pulse is required between watches and clocks since motor-drive pulses for watch motors cannot drive clock motors. Therefore, this motor driver provides two types of base pulse widths that can be selected with software.
Use the pulse width base clock select register PFTYP (FF15H•D0) for this selection.
When PFTYP is set to "0", long pulse width for clocks is selected and the motor-drive pulse will be generated from a 512-Hz source clock.
When PFTYP is set to "1", short pulse width for watches is selected and the motor-drive pulse will be generated from a 4-kHz source clock.

In addition to this setting, the pulse width select register is provided for each channel (Ch. 1: PFWA0–PFWA4, Ch. 2: PFWB0–PFWB4) to make fine adjustment of the pulse width according to the characteristics of the stepping motor to be used.
This register allows selection of 16 pulse widths from 11.72 msec to 56.64 msec in 1.953 msec increments for a clock pulse, or from 1.46 msec to 7.08 msec in 0.244 msec increments for a watch pulse.

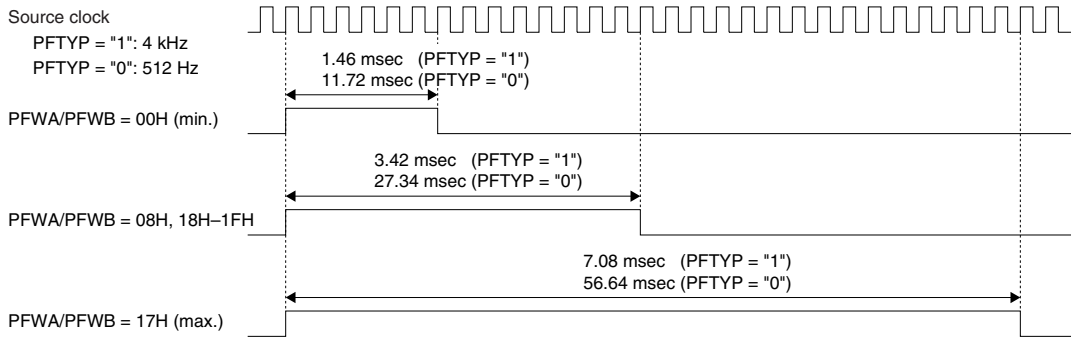


Fig. 4.15.2.1 Motor-drive pulse

Table 4.15.2.1 Setting up the motor-drive pulse

PFWA4	PFWA3	PFWA2	PFWA1	PFWA0	Pulse width	
PFWB4	PFWB3	PFWB2	PFWB1	PFWB0	PFTYP = "1"	PFTYP = "0"
0	0	0	0	0	1.46 msec	11.72 msec
0	0	0	0	1	1.71 msec	13.67 msec
0	0	0	1	0	1.95 msec	15.63 msec
0	0	0	1	1	2.20 msec	17.58 msec
0	0	1	0	0	2.44 msec	19.53 msec
0	0	1	0	1	2.69 msec	21.48 msec
0	0	1	1	0	2.93 msec	23.44 msec
0	0	1	1	1	3.17 msec	25.39 msec
0	1	0	0	0	3.42 msec	27.34 msec
0	1	0	0	1	3.66 msec	29.30 msec
0	1	0	1	0	3.91 msec	31.25 msec
0	1	0	1	1	4.15 msec	33.20 msec
0	1	1	0	0	4.40 msec	35.16 msec
0	1	1	0	1	4.64 msec	37.11 msec
0	1	1	1	0	4.88 msec	39.06 msec
0	1	1	1	1	5.13 msec	41.02 msec
1	0	0	0	0	5.37 msec	42.97 msec
1	0	0	0	1	5.62 msec	44.92 msec
1	0	0	1	0	5.86 msec	46.88 msec
1	0	0	1	1	6.10 msec	48.83 msec
1	0	1	0	0	6.35 msec	50.78 msec
1	0	1	0	1	6.59 msec	52.73 msec
1	0	1	1	0	6.84 msec	54.69 msec
1	0	1	1	1	7.08 msec	56.64 msec
1	1	X	X	X	3.42 msec	27.34 msec

Note: Make sure that the motor driver idles when selecting the source clock for generating the pulse width using PFTYP or the pulse width using PFWA0–PFWA4 or PFWB0–PFWB4.

4.15.3 Pulse output control

Ch. 1 starts outputting a pulse by writing "1" to the FTRG1 bit (FF10H•D0).
The motor driver starts executing a pulse output sequence using this writing as a trigger, and a pulse is output from the AO1 or AO2 terminal in the timing shown in the figure below. The first motor-drive pulse after an initial reset is output from the AO1 terminal. The following pulses are output from AO2 and AO1 terminals alternately every time "1" is written to FTRG1.
The FTRG1 bit used to trigger a pulse output is used as the status bit FRUN1 that indicates the motor driver status when reading. FRUN1 is set to "1" when the motor driver starts a pulse output sequence and is cleared to "0" upon completion of a pulse output for the specified width. At this time, an interrupt can be generated.
Ch. 2 can also be controlled with exactly the same method but FTRG2/FRUN2 (FF10H•D1) is used instead of FTRG1/FRUN1. The motor-drive pulses are output from the BO1 and BO2 alternately.

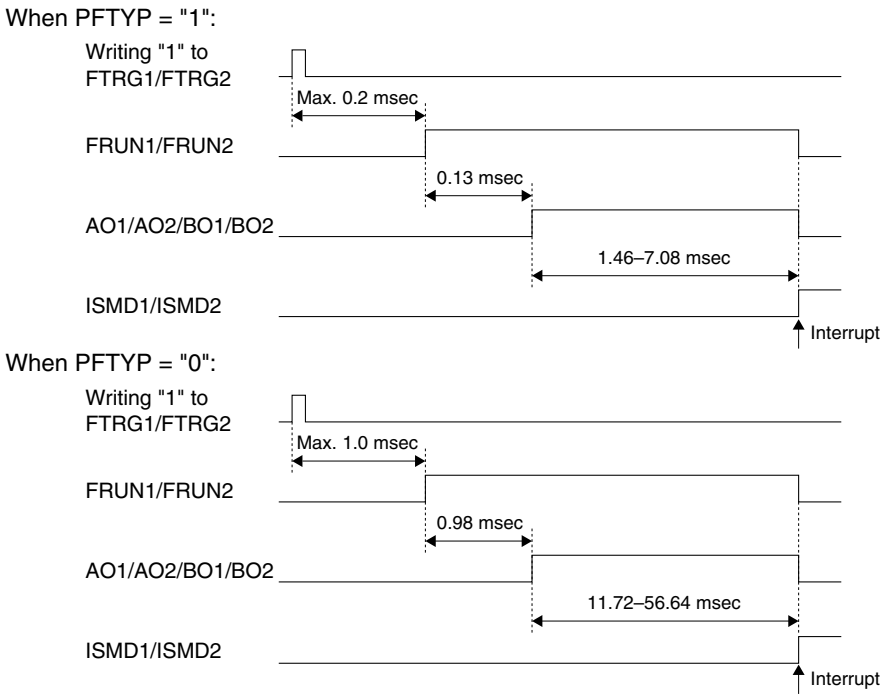


Fig. 4.15.3.1 Motor-drive pulse output timing chart

4.15.4 Interrupt function

This motor driver has an interrupt function in each channel. As shown in Figure 4.15.3.1, the interrupt factor flag ISMD1 (Ch. 1)/ISMD2 (Ch. 2) is set to "1" upon completion of a pulse output triggered by writing "1" to the FTRG1/FTRG2 bit and an interrupt is generated. The interrupt can also be masked by setting the corresponding interrupt mask register EISMD1/EISMD2. However, the interrupt factor flag is set to "1" upon completion of a pulse output from the corresponding channel regardless of the interrupt mask register setting.

4.15.5 I/O memory of stepping motor driver

Table 4.15.5.1 shows the I/O addresses and the control bits for the stepping motor driver.

Table 4.15.5.1 Control bits of stepping motor driver

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF10H	0	0	FTRG2	FTRG1	0 *3	– *2			Unused
			FRUN2	FRUN1	0 *3	– *2			Unused
					FTRG2	– *2	Trigger	Invalid	Motor driver Ch. 2 trigger (writing)
	R		W	W	FRUN2	0	Run	Stop	Motor driver Ch. 2 status (reading)
					FTRG1	– *2	Trigger	Invalid	Motor driver Ch. 1 trigger (writing)
			R	R	FRUN1	0	Run	Stop	Motor driver Ch. 1 status (reading)
FF11H	0	0	0	PFWA4	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					PFWA4	0			Motor driver Ch. 1 pulse width selection
FF12H	PFWA3	PFWA2	PFWA1	PFWA0	PFWA3	0			Motor driver Ch. 1 pulse width selection
					PFWA2	0			
	R/W				PFWA1	0			
					PFWA0	0			
FF13H	0	0	0	PFWB4	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					PFWB4	0			Motor driver Ch. 2 pulse width selection
FF14H	PFWB3	PFWB2	PFWB1	PFWB0	PFWB3	0			Motor driver Ch. 2 pulse width selection
					PFWB2	0			
	R/W				PFWB1	0			
					PFWB0	0			
FF15H	0	0	0	PFTYP	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					PFTYP	0	Short	Long	Pulse width base clock selection
FFE8H	0	0	EISMD2	EISMD1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EISMD2	0	Enable	Mask	Interrupt mask register (Motor driver Ch. 2)
					EISMD1	0	Enable	Mask	Interrupt mask register (Motor driver Ch. 1)
FFF8H	0	0	ISMD2	ISMD1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISMD2	0	(W)	(W)	Interrupt factor flag (Motor driver Ch. 2)
					ISMD1	0	Reset	Invalid	Interrupt factor flag (Motor driver Ch. 1)

[PFWA4–0] / [PFWB4–0]	Pulse width (PFTYP = "1")	Pulse width (PFTYP = "0")
00H	1.46 msec	11.72 msec
01H	1.71 msec	13.67 msec
02H	1.95 msec	15.63 msec
03H	2.20 msec	17.58 msec
04H	2.44 msec	19.53 msec
05H	2.69 msec	21.48 msec
06H	2.93 msec	23.44 msec
07H	3.17 msec	25.39 msec
08H	3.42 msec	27.34 msec
09H	3.66 msec	29.30 msec
0AH	3.91 msec	31.25 msec
0BH	4.15 msec	33.20 msec
0CH	4.40 msec	35.16 msec
0DH	4.64 msec	37.11 msec
0EH	4.88 msec	39.06 msec
0FH	5.13 msec	41.02 msec
10H	5.37 msec	42.97 msec
11H	5.62 msec	44.92 msec
12H	5.86 msec	46.88 msec
13H	6.10 msec	48.83 msec
14H	6.35 msec	50.78 msec
15H	6.59 msec	52.73 msec
16H	6.84 msec	54.69 msec
17H	7.08 msec	56.64 msec
18H–1FH	3.42 msec	27.34 msec

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

FTRG1/FRUN1: Motor driver Ch. 1 pulse output trigger/status (FF10H•D0)
FTRG2/FRUN2: Motor driver Ch. 2 pulse output trigger/status (FF10H•D1)
This is the trigger bit to start a motor-drive pulse and the status bit.

• ***When writing***

When "1" is written: Start outputting
When "0" is written: No operation

When writing has made, this bit functions as the trigger bit FTRGx (x = 1 or 2) to start outputting a motor-drive pulse.
By writing "1" to FTRGx, the motor driver starts a motor-drive pulse output sequence for Ch. x.
No operation results when "0" is written to FTRGx.

• ***When reading***

When "1" is read: RUN (during pulse output process)
When "0" is read: STOP (idle status)

When reading this bit functions as the status bit FRUNx (x = 1 or 2) that indicates the motor driver status. After "1" is written to FTRGx (this bit), the motor driver starts a motor-drive pulse output sequence within 0.2 msec when PFTYP = "1" or within 1.0 msec when PFTYP = "0". At this point FRUNx is set to "1" and is cleared to "0" upon completion of the pulse output sequence. In other words, this bit set to "1" indicates that the motor driver is in busy status for pulse output process.
Writing "1" to FTRGx for trigger is ignored while FRUNx is set to "1".
At initial reset, this bit is set to "0".

PFWA0–PFWA4: Motor driver Ch. 1 pulse width select register (FF12H, FF11H•D0)
PFWB0–PFWB4: Motor driver Ch. 2 pulse width select register (FF14H, FF13H•D0)
Selects the motor-drive pulse width. The selectable range is changed according to the selection of the pulse width base clock register PFTYP.

Table 4.15.5.2 Setting up the motor-drive pulse

PFWA4	PFWA3	PFWA2	PFWA1	PFWA0	Pulse width	
PFWB4	PFWB3	PFWB2	PFWB1	PFWB0	PFTYP = "1"	PFTYP = "0"
0	0	0	0	0	1.46 msec	11.72 msec
0	0	0	0	1	1.71 msec	13.67 msec
0	0	0	1	0	1.95 msec	15.63 msec
0	0	0	1	1	2.20 msec	17.58 msec
0	0	1	0	0	2.44 msec	19.53 msec
0	0	1	0	1	2.69 msec	21.48 msec
0	0	1	1	0	2.93 msec	23.44 msec
0	0	1	1	1	3.17 msec	25.39 msec
0	1	0	0	0	3.42 msec	27.34 msec
0	1	0	0	1	3.66 msec	29.30 msec
0	1	0	1	0	3.91 msec	31.25 msec
0	1	0	1	1	4.15 msec	33.20 msec
0	1	1	0	0	4.40 msec	35.16 msec
0	1	1	0	1	4.64 msec	37.11 msec
0	1	1	1	0	4.88 msec	39.06 msec
0	1	1	1	1	5.13 msec	41.02 msec
1	0	0	0	0	5.37 msec	42.97 msec
1	0	0	0	1	5.62 msec	44.92 msec
1	0	0	1	0	5.86 msec	46.88 msec
1	0	0	1	1	6.10 msec	48.83 msec
1	0	1	0	0	6.35 msec	50.78 msec
1	0	1	0	1	6.59 msec	52.73 msec
1	0	1	1	0	6.84 msec	54.69 msec
1	0	1	1	1	7.08 msec	56.64 msec
1	1	X	X	X	3.42 msec	27.34 msec

At initial reset, these registers are set to "00H".

PFTYP: Pulse width base clock register (FF15H•D0)

Selects the source clock to generate motor-drive pulses according to clocks or watches.

When "1" is written: Short pulse (4 kHz)
When "0" is written: Long pulse (512 Hz)
Reading: Valid

When "1" is written to PFTYP, a 4-kHz clock used to generate the short pulse for watch stepping motors is selected. When "0" is written, a 512-Hz clock used to generate the long pulse for clock stepping motors is selected. See Table 4.15.5.2 for the pulse widths generated.
At initial reset, this register is set to "0".

EISMD1: Motor driver Ch. 1 interrupt mask register (FFE8H•D0)
EISMD2: Motor driver Ch. 2 interrupt mask register (FFE8H•D1)

Masking the interrupt of the motor driver can be selected with this register.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

EISMD1 and EISMD2 are the interrupt mask registers that respectively correspond to the motor driver Ch. 1 and Ch. 2 interrupt factors. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, these registers are set to "0".

ISMD1: Motor driver Ch. 1 interrupt factor flag (FFF8H•D0)
ISMD2: Motor driver Ch. 2 interrupt factor flag (FFF8H•D1)

These flags indicate the status of the motor driver interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

ISMD1 and ISMD2 are the interrupt factor flags that respectively correspond to the motor driver Ch. 1 and Ch. 2 interrupts, and are set to "1" upon completion of a motor-drive pulse output.
The software can judge from these flags whether there is a motor driver interrupt. However, even if the interrupt is masked, the flags are set to "1" upon completion of a motor-drive pulse output from the corresponding channel.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.15.6 Programming notes

(1) Make sure that the motor driver idles when selecting the source clock for generating the pulse width using PFTYP or the pulse width using PFWA0–PFWA4 or PFWB0–PFWB4.

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.16 SVD (Supply Voltage Detection) Circuit

4.16.1 Configuration of SVD circuit

The S1C63656 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers.
Turning the SVD circuit on/off and the SVD criteria voltage setting can be done with software.
Figure 4.16.1.1 shows the configuration of the SVD circuit.

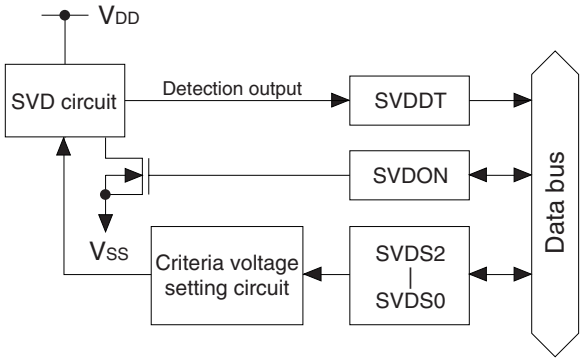


Fig. 4.16.1.1 Configuration of SVD circuit

4.16.2 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (V_{DD} terminal–V_{SS} terminal) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.

The criteria voltage can be selected using the SVDS2–SVDS0 register as shown in Table 4.16.2.1.
Not that the criteria voltage range depends on the selected OSC3 oscillation circuit option (use or not used).

Table 4.16.2.1 Criteria voltage

SVDS2	SVDS1	SVDS0	Criteria voltage (V)	
			When OSC3 is used	When OSC3 is not used
1	1	1	2.90	1.64
1	1	0	2.75	1.56
1	0	1	2.60	1.47
1	0	0	2.45	1.39
0	1	1	2.30	1.30
0	1	0	2.15	1.22
0	0	1	2.00	1.13
0	0	0	1.85	–

When the SVDON register is set to "1", source voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes off.
To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is on, the IC draws a large current, so keep the SVD circuit off unless it is.

4.16.3 I/O memory of SVD circuit

Table 4.16.3.1 shows the I/O addresses and the control bits for the SVD circuit.

Table 4.16.3.1 Control bits of SVD circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF04H	0	SVDS2	SVDS1	SVDS0	0 *3	– *2			Unused
					SVDS2	0			SVD criteria voltage setting (V1: when OSC3 is used, V2: when OSC3 is not used)
					SVDS1	0			[SVDS2–0] 0 1 2 3 4 5 6 7
	R	R/W			SVDS0	0			V1 (V) 1.85 2.00 2.15 2.30 2.45 2.60 2.75 2.90
									V2 (V) – 1.13 1.22 1.30 1.39 1.47 1.56 1.64
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SVDS2–SVDS0: SVD criteria voltage setting register (FF04H•D2–D0)

Criteria voltage for SVD is set as shown in Table 4.16.2.1.
At initial reset, this register is set to "0".

SVDON: SVD control (on/off) register (FF05H•D0)

Turns the SVD circuit on and off.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When SVDON is set to "1", a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec.
At initial reset, this register is set to "0".

SVDDT: SVD data (FF05H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

4.16.4 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned off because SVD operation increase current consumption.

4.17 Interrupt and HALT

<Interrupt types>

The S1C63656 provides the following interrupt functions.

External interrupt:	• Input interrupt	(2 systems)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Programmable timer interrupt	(5 systems)
	• Serial interface interrupt	(1 system)
	• Clock timer interrupt	(4 systems)
	• Stopwatch timer interrupt	(4 systems)
	• R/f converter interrupt	(2 systems)
	• Motor driver interrupt	(2 systems)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.17.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

<HALT>

The S1C63656 has HALT functions that considerably reduce the current consumption when it is not necessary.
The CPU enters HALT status when the HALT instruction is executed.
In HALT status, the operation of the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.

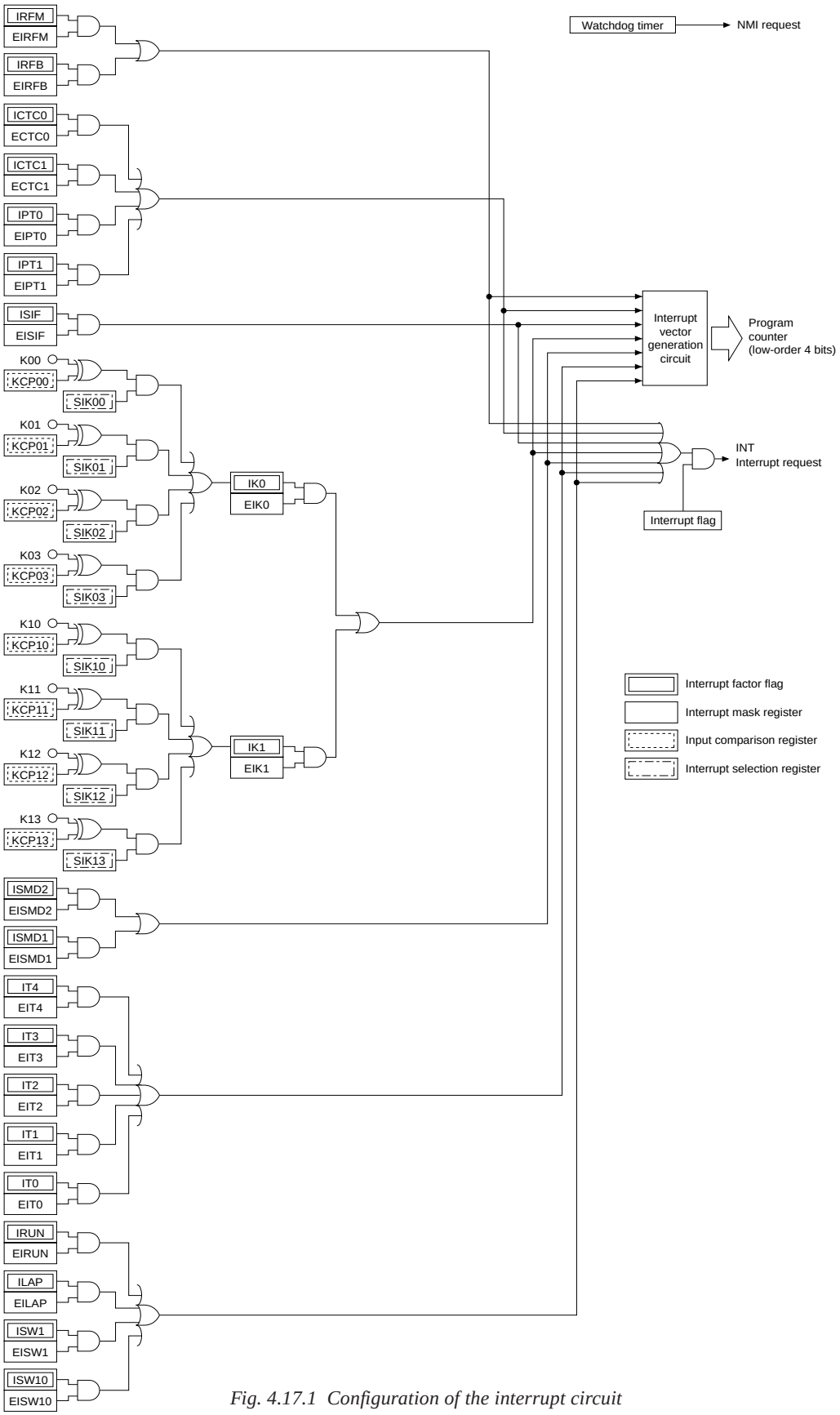


Fig. 4.17.1 Configuration of the interrupt circuit

4.17.1 Interrupt factor

Table 4.17.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.
At initial reset, the interrupt factor flags are reset to "0".

∗ Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.17.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Programmable timer 1 (compare match)	ICTC1	(FFF0H•D1)
Programmable timer 0 (compare match)	ICTC0	(FFF0H•D0)
Programmable timer 1 (underflow)	IPT1	(FFF1H•D1)
Programmable timer 0 (underflow)	IPT0	(FFF1H•D0)
Serial interface (8-bit data input/output completion)	ISIF	(FFF2H•D0)
K00–K03 input (falling edge or rising edge)	IK0	(FFF3H•D0)
K10–K13 input (falling edge or rising edge)	IK1	(FFF4H•D0)
Clock timer 16 Hz (falling edge)	IT4	(FFF9H•D0)
Clock timer 1 Hz (falling edge)	IT3	(FFF5H•D3)
Clock timer 2 Hz (falling edge)	IT2	(FFF5H•D2)
Clock timer 8 Hz (falling edge)	IT1	(FFF5H•D1)
Clock timer 32 Hz (falling edge)	IT0	(FFF5H•D0)
Stopwatch timer (Direct RUN)	IRUN	(FFF6H•D3)
Stopwatch timer (Direct LAP)	ILAP	(FFF6H•D2)
Stopwatch timer (1 Hz)	ISW1	(FFF6H•D1)
Stopwatch timer (10 Hz)	ISW10	(FFF6H•D0)
R/f converter (end of reference conversion)	IRFB	(FFF7H•D1)
R/f converter (end of sensor conversion)	IRFM	(FFF7H•D0)
Motor driver Ch. 2 (pulse output completion)	ISMD2	(FFF8H•D1)
Motor driver Ch. 1 (pulse output completion)	ISMD1	(FFF8H•D0)

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.17.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is reset to "0".
Table 4.17.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.17.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
ECTC1	(FFE0H•D1)	ICTC1	(FFF0H•D1)
ECTC0	(FFE0H•D0)	ICTC0	(FFF0H•D0)
EIPT1	(FFE1H•D1)	IPT1	(FFF1H•D1)
EIPT0	(FFE1H•D0)	IPT0	(FFF1H•D0)
EISIF	(FFE2H•D0)	ISIF	(FFF2H•D0)
EIK0	(FFE3H•D0)	IK0	(FFF3H•D0)
EIK1	(FFE4H•D0)	IK1	(FFF4H•D0)
EIT4	(FFE9H•D0)	IT4	(FFF9H•D0)
EIT3	(FFE5H•D3)	IT3	(FFF5H•D3)
EIT2	(FFE5H•D2)	IT2	(FFF5H•D2)
EIT1	(FFE5H•D1)	IT1	(FFF5H•D1)
EIT0	(FFE5H•D0)	IT0	(FFF5H•D0)
EIRUN	(FFE6H•D3)	IRUN	(FFF6H•D3)
EILAP	(FFE6H•D2)	ILAP	(FFF6H•D2)
EISW1	(FFE6H•D1)	ISW1	(FFF6H•D1)
EISW10	(FFE6H•D0)	ISW10	(FFF6H•D0)
EIRFB	(FFE7H•D1)	IRFB	(FFF7H•D1)
EIRFM	(FFE7H•D0)	IRFM	(FFF7H•D0)
EISMD2	(FFE8H•D1)	ISMD2	(FFF8H•D1)
EISMD1	(FFE8H•D0)	ISMD1	(FFF8H•D0)

4.17.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

1 The content of the flag register is evacuated, then the I flag is reset.
2 The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).
3 The interrupt request causes the value of the interrupt vector (0100H–010EH) to be set in the program counter.
4 The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.17.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.17.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High
0102H	R/f converter	↑
0104H	Programmable timer	
0106H	Serial interface	
0108H	K00–K03, K10–K13 input	
010AH	Motor driver	
010CH	Clock timer	↓
010EH	Stopwatch timer	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.17.4 I/O memory of interrupt

Tables 4.17.4.1 shows the I/O addresses and the control bits for controlling interrupts.

Table 4.17.4.1(a) Control bits of interrupt

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FFE0H	0	0	ECTC1	ECTC0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		ECTC1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 compare match)
					ECTC0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 compare match)
FFE1H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 underflow)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 underflow)
FFE2H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFE3H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE4H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE5H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE6H	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFE7H	0	0	EIRFB	EIRFM	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIRFB	0	Enable	Mask	Interrupt mask register (R/f converter reference oscillate completion)
					EIRFM	0	Enable	Mask	Interrupt mask register (R/f converter sensor oscillate completion)
FFE8H	0	0	EISMD2	EISMD1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EISMD2	0	Enable	Mask	Interrupt mask register (Motor driver Ch. 2)
					EISMD1	0	Enable	Mask	Interrupt mask register (Motor driver Ch. 1)
FFE9H	0	0	0	EIT4	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIT4	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.17.4.1(b) Control bits of interrupt

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFF0H	0	0	ICTC1	ICTC0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ICTC1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1 compare match)
					ICTC0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0 compare match)
FFF1H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1 underflow)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0 underflow)
FFF2H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)
FFF3H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF4H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF5H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF6H	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)
FFF7H	0	0	IRFB	IRFM	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IRFB	0	(W)	(W)	Interrupt factor flag (R/f converter reference oscillate completion)
					IRFM	0	Reset	Invalid	Interrupt factor flag (R/f converter sensor oscillate completion)
FFF8H	0	0	ISMD2	ISMD1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISMD2	0	(W)	(W)	Interrupt factor flag (Motor driver Ch. 2)
					ISMD1	0	Reset	Invalid	Interrupt factor flag (Motor driver Ch. 1)
FFF9H	0	0	0	IT4	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IT4	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ECTC1, ECTC0: Interrupt mask registers (FFE0H•D1, D0)
EIPT1, EIPT0: Interrupt mask registers (FFE1H•D1, D0)
ICTC1, ICTC0: Interrupt factor flags (FFF0H•D1, D0)
IPT1, IPT0: Interrupt factor flags (FFF1H•D1, D0)
Refer to Section 4.10, "Programmable Timer".

EISIF: Interrupt mask register (FFE2H•D0)
ISIF: Interrupt factor flag (FFF2H•D0)
Refer to Section 4.11, "Serial Interface".

KCP03–KCP00, KCP13–KCP10: Input comparison registers (FF22H, FF26H)
SIK03–SIK00, SIK13–SIK10: Interrupt selection registers (FF20H, FF24H)
EIK0, EIK1: Interrupt mask registers (FFE3H•D0, FFE4H•D0)
IK0, IK1: Interrupt factor flags (FFF3H•D0, FFF4H•D0)
Refer to Section 4.4, "Input Ports".

EIT4–EIT0: **Interrupt mask registers (FFE9H•D0, FFE5H)**
IT4–IT0: **Interrupt factor flags (FFF9H•D0, FFF5H)**
Refer to Section 4.8, "Clock Timer".

EIRUN, EILAP, EISW1, EISW10: **Interrupt mask registers (FFE6H)**
IRUN, ILAP, ISW1, ISW10: **Interrupt factor flags (FFF6H)**
Refer to Section 4.9, "Stopwatch Timer".

EIRFB, EIRFM: **Interrupt mask registers (FFE7H•D1, D0)**
IRFB, IRFM: **Interrupt factor flags (FFF7H•D1, D0)**
Refer to Section 4.14, "R/f Converter".

EISMD2, EISMD1: **Interrupt mask registers (FFE8H•D1, D0)**
ISMD2, ISMD1: **Interrupt factor flags (FFF8H•D1, D0)**
Refer to Section 4.15, "Stepping Motor Driver".

4.17.5 Programming notes

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The S1C63656 contains control registers for each of the circuits so that current consumption can be reduced.
These control registers reduce the current consumption through programs that operate the circuits at the minimum levels.
The following lists the circuits that can control operation and their control registers. Refer to these when programming.

Table 5.1.1 Circuits and control registers

Circuit (and item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
LCD system voltage circuit	LPWR
SVD circuit	SVDON
Motor driver	FTRG1, FTRG2

Refer to Chapter 7, "Electrical Characteristics" for current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0")
OSC3 oscillation circuit is in off status (OSCC = "0")

LCD system voltage circuit: Off status (LPWR = "0")

SVD circuit: Off status (SVDON = "0")

Motor driver: Off status (FTRG1/FRUN1 = FTRG2/FRUN2 = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

(1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Table 4.1.1 for the peripheral I/O area.

(2) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(3) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63656 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access. After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

Watchdog timer

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Oscillation circuit

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) When selecting OSC3 for the time base counter clock of the R/f converter, the maximum frequency of the OSC3 clock is limited to 2 MHz.

Input port

When input ports are changed from high to low by pull-down resistors, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time. Particular care needs to be taken of the key scan during key matrix configuration. Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$ C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

Output port

(1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

(2) A hazard may occur when the FOUT signal and the TOUT signal are turned on and off.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output. Refer to Section 4.3, "Oscillation Circuit", for the control and notes.
f_{OSC3} is available when a mask option for using the OSC3 oscillation circuit is selected. If the system uses the OSC1 oscillation circuit only, do not set the FOFQ register to "11".

I/O port

When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$ C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

LCD driver

Because at initial reset, the contents of display memory are undefined and LC3–LC0 (LCD contrast) is set to 0000B, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes off.

Clock timer

Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

Stopwatch timer

(1) The interrupt factor flag should be reset after resetting the stopwatch timer.

(2) Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

(3) When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWD8–11 and check whether the data has been renewed or not.

(4) When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

Programmable timer

(1) When reading counter data, be sure to read the low-order 4 bits (PTDx0–PTDx3) first. Furthermore, the high-order 4 bits (PTDx4–PTDx7) are not latched when the low-order 4 bits are read. Therefore, the high-order 4 bits should be read within 0.73 msec (when f_{OSC1} is 32.768 kHz) from reading the low-order 4 bits. When the CPU is running with the OSC1 clock and the programmable timer is running with the OSC3 clock, stop the timer before reading the counter data. The counter running with OSC3 counts down for the value listed in Table 5.2.1 while the CPU running with OSC1 reads the low-order 4 bits and high-order 4 bits of the counter data by two instructions.

Table 5.2.1 Counter change with OSC3 between readings low-order and high-order data with OSC1

Count clock	Counter change between reading
OSC3/1	0200H
OSC3/4	001AH
OSC3/32	0002H

In 16-bit mode, the counter data must be read in the order below.
PTD00–PTD03 → PTD04–PDT07 → PTD10–PTD13 → PTD14–PTD17

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.
Figure 5.2.1 shows the timing chart for the RUN/STOP control.

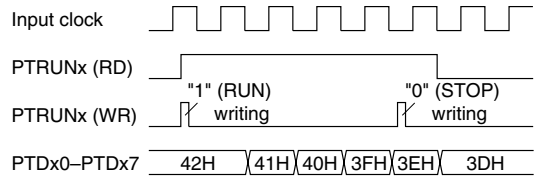


Fig. 5.2.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the off state.

(5) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

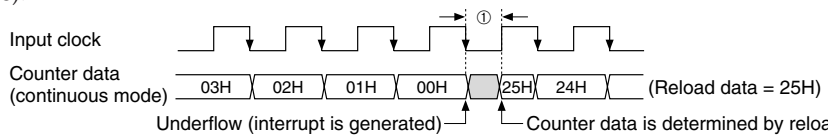


Fig. 5.2.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

Serial interface

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source of the programmable timer or in the slave mode.

Sound generator

(1) Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

(2) The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

Integer multiplier

An operation process takes 10 CPU clock cycles (5 bus cycles) after writing to the calculation mode selection register CALMD until the operation result is set to the destination register DRH/DRL and the operation flags. While this operation process, do not read/write from/to the destination register DRH/DRL and do not read NF/VF/ZF.

R/f converter

(1) Depending on the initial value of the measurement counter (MC), the measurement counter or the time base counter may overflow while the CR oscillation clock is being counted. When setting the initial value, pay attention to CR oscillation frequency, its fluctuation range and the input clock frequency of the time base counter. If an overflow occurs, R/f conversion is terminated immediately. When the R/f conversion result (measurement counter value) is read, check the overflow flags (OVMC and OVTBC). The upper limit of the CR oscillation frequency is 500 kHz. There is no lower-limit but make sure that the time base counter does not overflow.

(2) When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/f converter interrupt occurs.

(3) When selecting OSC3 for the time base counter clock, the maximum frequency of the OSC3 clock is limited to 2 MHz.

(4) When setting the measurement counter, always write 5 words of data continuously in order from the lower address (FF92H → FF93H → FF94H → FF95H → FF96H). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used.

Stepping motor driver

Make sure that the motor driver idles when selecting the source clock for generating the pulse width using PFTYP or the pulse width using PFWA0–PFWA4 or PFWB0–PFWB4.

SVD circuit

(1) To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned off because SVD operation increase current consumption.

Interrupt

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

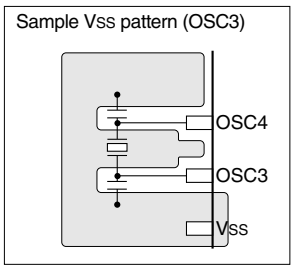
5.3 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals. Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VDD, please keep enough distance between OSC1/OSC3 and VDD or other signals on the board pattern.

<Reset Circuit>

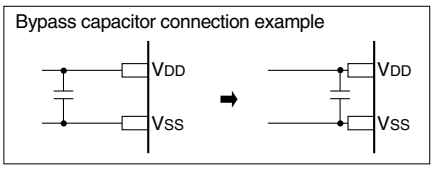
- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product. When using the built-in pull-down resistor of the RESET terminal, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD, VSS, VDDA and VSSA terminals with patterns as short and large as possible.
  In particular, the power supply for VDDA and VSSA affect R/f conversion accuracy.

  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



  (3) Components which are connected to the VD1, VOSC and VC1–VC3 terminals, such as capacitors, should be connected in the shortest line.
  In particular, the VC1–VC3 voltages affect the display quality.

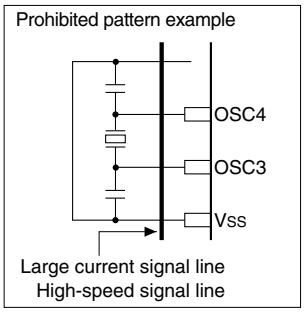
- Do not connect anything to the VC1–VC3 terminals when the LCD driver is not used.

<R/f Converter>

- The power supply terminals for the analog system should be connected as shown below even if the R/f converter is not used.
  VDDA → VDD
  VSSA → VSS

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit and analog input unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit and analog input unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

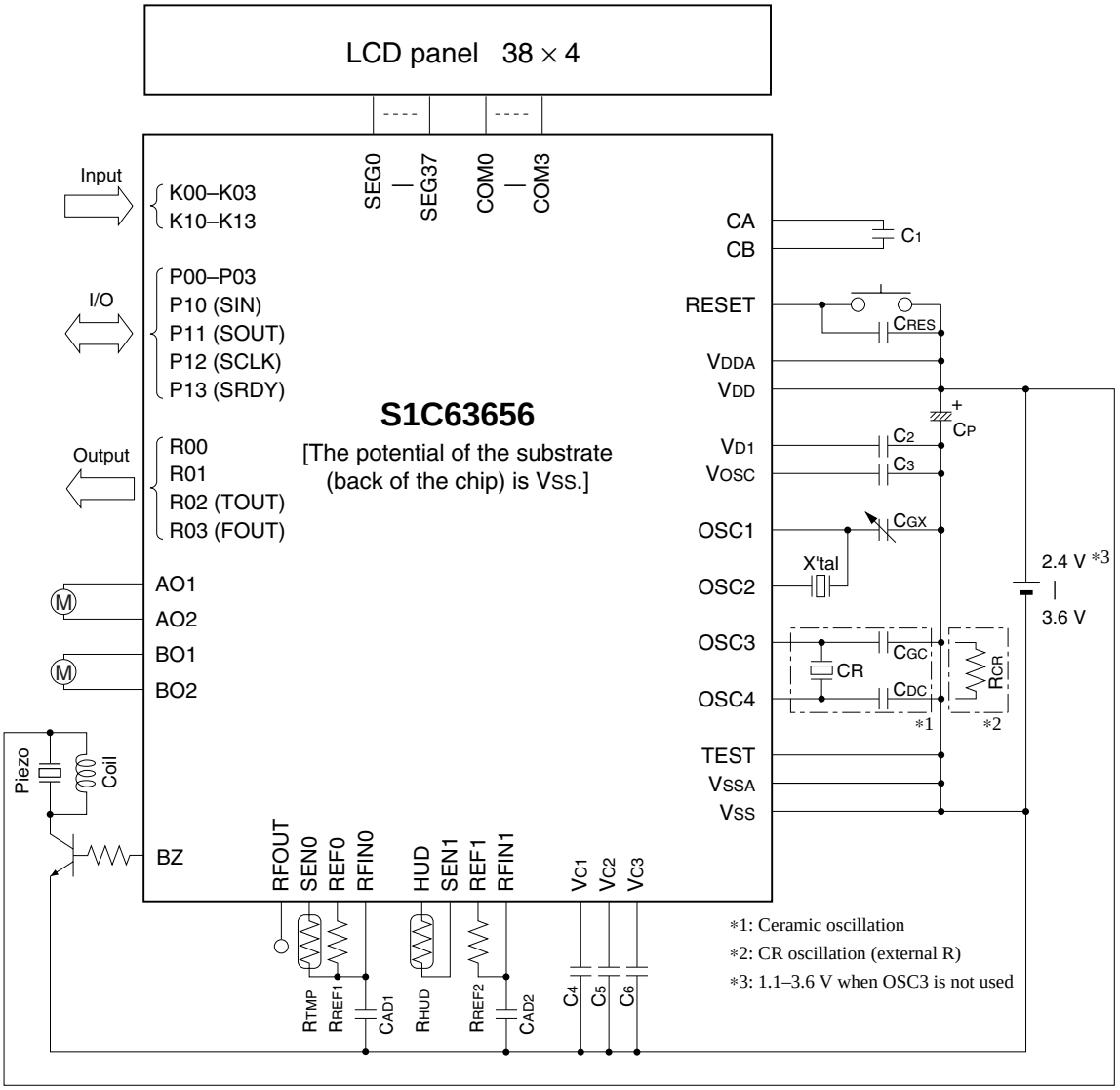
- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	30 pF
CDC	Drain capacitor	30 pF
RCR	Resistor for OSC3 CR oscillation	30 kΩ (2 MHz)
C1–C6	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{SS}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{DD}	-0.5 to 4.5	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package (QFP20-144pin).

7.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	when OSC3 is not used	1.1	3.0	3.6	V
			when OSC3 is used, 4MHz (Max.)	2.4	3.0	3.6	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
	f_{OSC3}	CR oscillation (built-in R), V_{DD}=2.4 to 3.6V		770	1,100	1,430	kHz
		CR oscillation (external R), V_{DD}=2.4 to 3.6V		200		2,000	kHz
		Ceramic oscillation, V_{DD}=2.4 to 3.6V when the R/f converter uses the OSC3 clock				2,000	kHz
		Ceramic oscillation, V_{DD}=2.4 to 3.6V when the R/f converter does not use the OSC3 clock				4,000	kHz

7.3 DC Characteristics

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_6=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, P00–03, P10–13	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, P00–03, P10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	0		0.1·V_{DD}	V
High level input current (1)	I_{IH1}	V_{IH1}=3.0V No pull down	K00–03, K10–13, P00–03, P10–13, RESET, TEST	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=3.0V With pull down	K00–03, K10–13, P00–03, P10–13, RESET, TEST	8	12	20	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull down	K00–03, K10–13, P00–03, P10–13, RESET, TEST	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull down	K00–03, K10–13, P00–03, P10–13, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, P00–03, P10–13			-0.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-0.5	mA
High level output current (3)	I_{OH3}	V_{OH3}=0.9·V_{DD}	AO1, AO2, BO1, BO2			-25	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, P00–03, P10–13	0.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	0.5			mA
Low level output current (3)	I_{OL3}	V_{OL3}=0.1·V_{DD}	AO1, AO2, BO1, BO2	25			mA
Common output current	I_{OH4}	V_{OH4}=V_{C3}-0.05V	COM0–3			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH5}	V_{OH5}=V_{C3}-0.05V	SEG0–37			-10	µA
	I_{OL5}	V_{OL5}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH6}	V_{OH6}=0.9·V_{DD}	SEG0–37			-300	µA
	I_{OL6}	V_{OL6}=0.1·V_{DD}		300			µA
R/f converter transistor ON resistance	R_{RFINTr}	V_{DS}=0.1V, V_{DD}=1.8V			20	40	Ω
	R_{REFTr}	V_{DS}=0.1V, V_{DD}=1.8V			50	100	Ω
	R_{SEN0Tr}	V_{DS}=0.1V, V_{DD}=1.8V			50	100	Ω
	R_{SEN1Tr}						

7.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_6=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)	LC0–3="0"		1.03		V
			LC0–3="1"		1.06		
			LC0–3="2"		1.09		
			LC0–3="3"		1.12		
			LC0–3="4"		1.15		
			LC0–3="5"		1.18		
			LC0–3="6"		1.20		
			LC0–3="7"	Typ.	1.23	Typ.	
			LC0–3="8"	-100mV	1.26	+100mV	
			LC0–3="9"		1.28		
			LC0–3="10"		1.30		
			LC0–3="11"		1.32		
			LC0–3="12"		1.34		
			LC0–3="13"		1.36		
			LC0–3="14"		1.38		
			LC0–3="15"		1.40		
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2·V_{C1} ×0.9		2·V_{C1}	V
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3·V_{C1} ×0.9		3·V_{C1}	V
SVD voltage (OSC3 disabled) ∗2	V_{SVD1}	SVDS0–2="0" (SVD not used)			–		V
		SVDS0–2="1"			1.13		
		SVDS0–2="2"			1.22		
		SVDS0–2="3"		Typ.	1.30	Typ.	
		SVDS0–2="4"		-100mV	1.39	+100mV	
		SVDS0–2="5"			1.47		
		SVDS0–2="6"			1.56		
		SVDS0–2="7"			1.64		
SVD voltage (OSC3 enabled) ∗3	V_{SVD2}	SVDS0–2="0"			1.85		V
		SVDS0–2="1"			2.00		
		SVDS0–2="2"			2.15		
		SVDS0–2="3"		Typ.	2.30	Typ.	
		SVDS0–2="4"		-100mV	2.45	+100mV	
		SVDS0–2="5"			2.60		
		SVDS0–2="6"			2.75		
		SVDS0–2="7"			2.90		
SVD circuit response time	t_{SVD}					500	µs
Current consumption in HALT mode (OSC3 disabled) ∗2	I_{HALT1}	32kHz crystal, LCD OFF ∗1			0.50	1.50	µA
		32kHz crystal, LCD ON (low-power) ∗1, ∗4			0.60	1.80	µA
		32kHz crystal, LCD ON (normal) ∗1			1.20	2.10	µA
Current consumption in HALT mode (OSC3 enabled) ∗3	I_{HALT2}	32kHz crystal, LCD OFF ∗1			0.90	1.80	µA
		32kHz crystal, LCD ON (normal) ∗1			1.20	2.10	µA
		32kHz crystal, LCD ON (normal) ∗1			1.40	2.80	µA
Current consumption in Run state (OSC3 disabled) ∗2	I_{EXE1}	32kHz crystal, LCD ON (low-power) ∗1, ∗4			2.5	4.5	µA
		32kHz crystal, LCD ON (normal) ∗1			4.0	6.0	µA
Current consumption in Run state (OSC3 enabled) ∗3	I_{EXE2}	2MHz ceramic, LCD ON (normal) ∗1			400	800	µA
		4MHz ceramic, LCD ON (normal) ∗1			800	1000	µA
		1.1MHz CR, LCD ON (normal) ∗1			350	600	µA
SVD circuit current	I_{SVD}	During voltage detection, V_{DD}=1.1 to 3.6V			5	10	µA
R/f converter circuit current	I_{RF}	Oscillation frequency=10kHz, V_{DD}=2.4 to 3.6V			100	150	µA

∗1 No panel load. When SVD circuit, R/f converter and motor driver are in OFF status.
∗2 When the mask option to disable OSC3 is selected.
∗3 When a mask option for using OSC3 is selected.
∗4 Without LCD contrast adjustment

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:
VDD=3.0V, VSS=0V, fOSC1=32.768kHz, CG=25pF, CD=built-in, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (VDD)	1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (VDD)	1.1			V
Built-in capacitance (drain)	CD	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	∂f/∂V	VDD=1.1 to 3.6V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂CG	CG=5 to 25pF	10	20		ppm
Harmonic oscillation start voltage	Vhho	CG=5pF (VDD)	3.6			V
Permitted leak resistance	Rleak	Between OSC1 and VSS	200			MΩ

OSC3 ceramic oscillation circuit

Unless otherwise specified:
VDD=3.0V, VSS=0V, Ceramic oscillator: 4MHz, CGC=CDC=30pF, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(VDD)	2.4			V
Oscillation start time	tsta	VDD=2.4 to 3.6V			5	ms
Oscillation stop voltage	Vstp	(VDD)	2.4			V

OSC3 CR oscillation circuit (built-in R type)

Unless otherwise specified:
VDD=3.0V, VSS=0V, RCR=Built in, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC3		-30	1,100kHz	30	%
Oscillation start voltage	Vsta	(VDD)	2.4			V
Oscillation start time	tsta	VDD=2.4 to 3.6V			3	ms
Oscillation stop voltage	Vstp	(VDD)	2.4			V

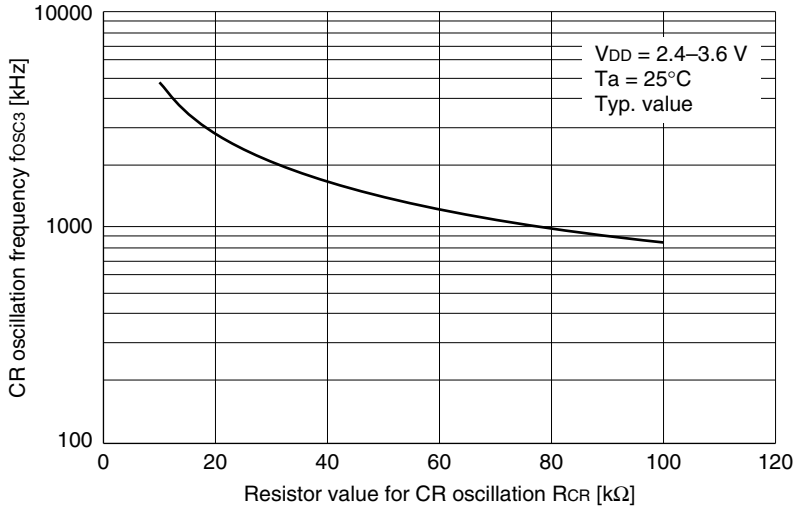
OSC3 CR oscillation circuit (external R type)

Unless otherwise specified:
VDD=3.0V, VSS=0V, RCR=30kΩ (2MHz), Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC3		-30		30	%
Oscillation start voltage	Vsta	(VDD)	2.4			V
Oscillation start time	tsta	VDD=2.4 to 3.6V			3	ms
Oscillation stop voltage	Vstp	(VDD)	2.4			V

OSC3 CR oscillation frequency-resistance characteristic (external R type)

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



7.6 Serial Interface AC Characteristics

Clock synchronous master mode

• During 32 kHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µs
Receiving data input set-up time	tsms	10			µs
Receiving data input hold time	tsmh	5			µs

• During 4 MHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	ns
Receiving data input set-up time	tsms	400			ns
Receiving data input hold time	tsmh	200			ns

Note that the maximum clock frequency is limited to 1 MHz.

Clock synchronous slave mode

• During 32 kHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µs
Receiving data input set-up time	tsss	10			µs
Receiving data input hold time	tssh	5			µs

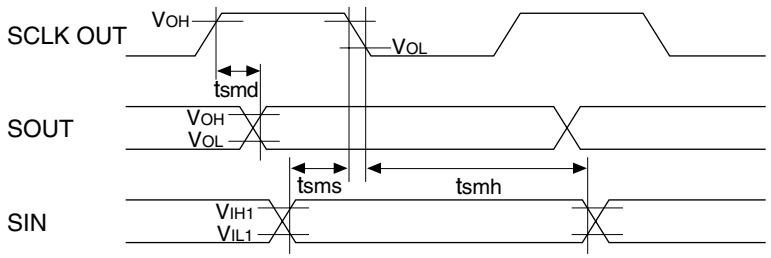
• During 4 MHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

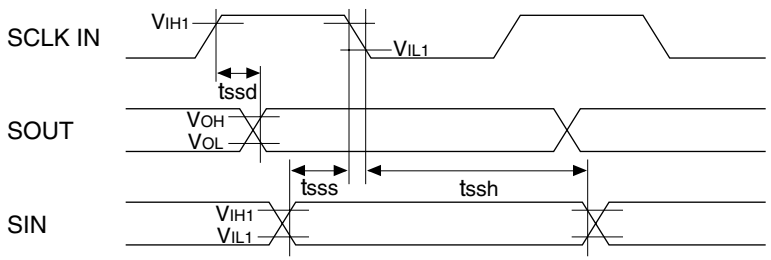
Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	ns
Receiving data input set-up time	tsss	400			ns
Receiving data input hold time	tssh	200			ns

Note that the maximum clock frequency is limited to 1 MHz.

<Master mode>

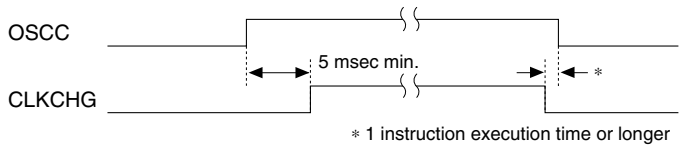


<Slave mode>



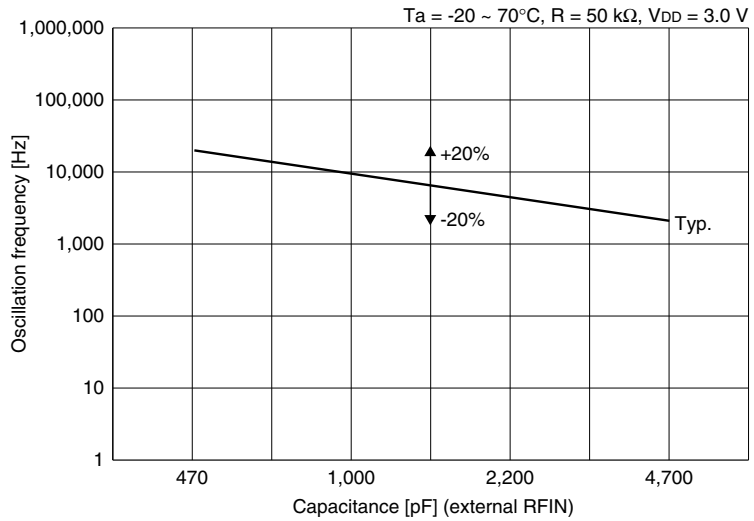
7.7 Timing Chart

System clock switching

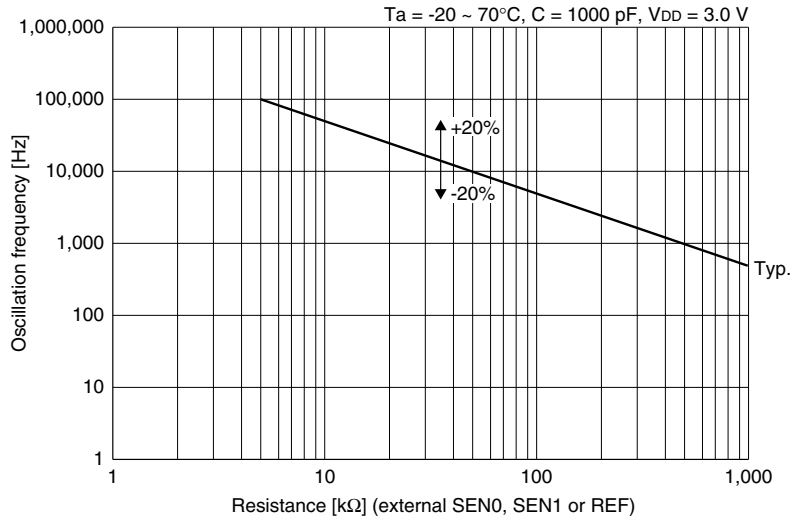


7.8 R/f Converter Characteristics

R/f converter oscillation frequency - capacitance characteristic (reference value)



R/f converter oscillation frequency - resistance characteristic (reference value)

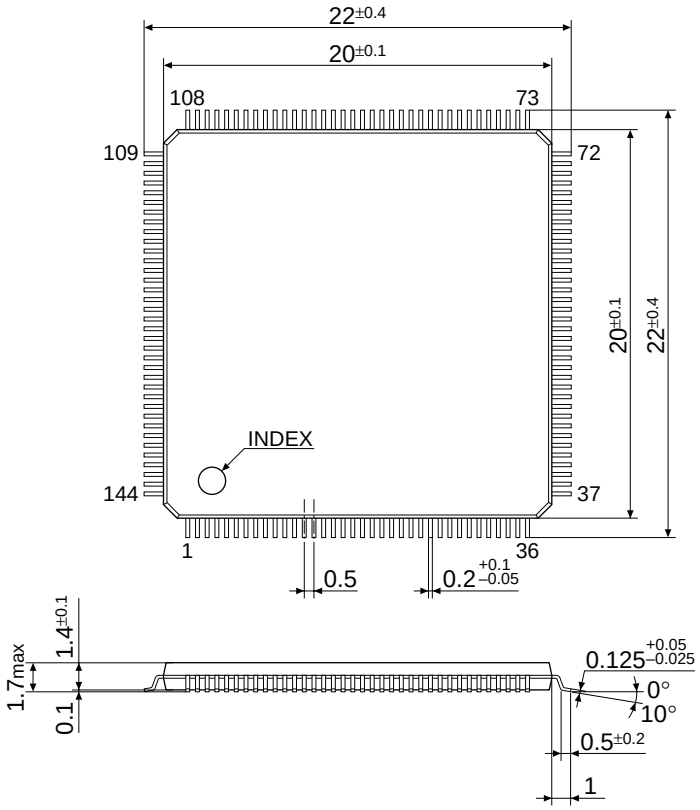


CHAPTER 8 PACKAGE

8.1 Plastic Package

QFP20-144pin

(Unit: mm)

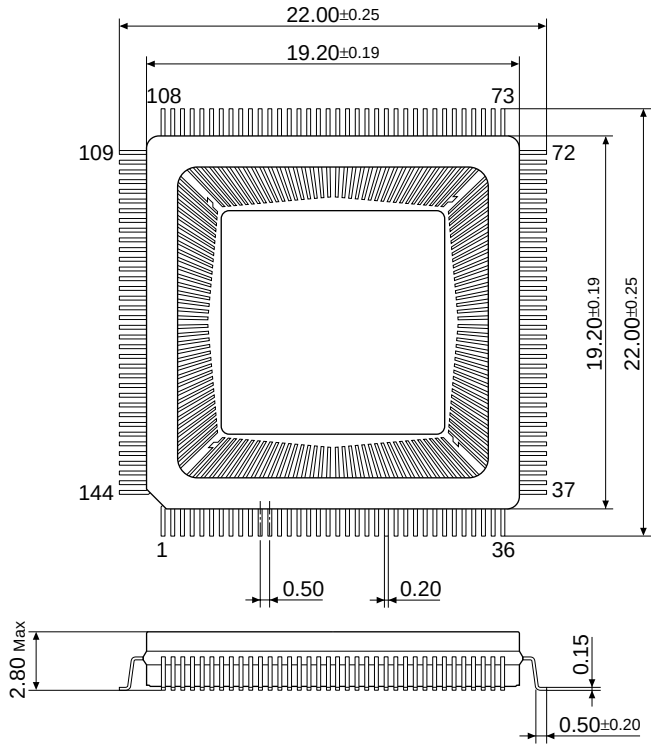


The dimensions are subject to change without notice.

8.2 Ceramic Package for Test Samples

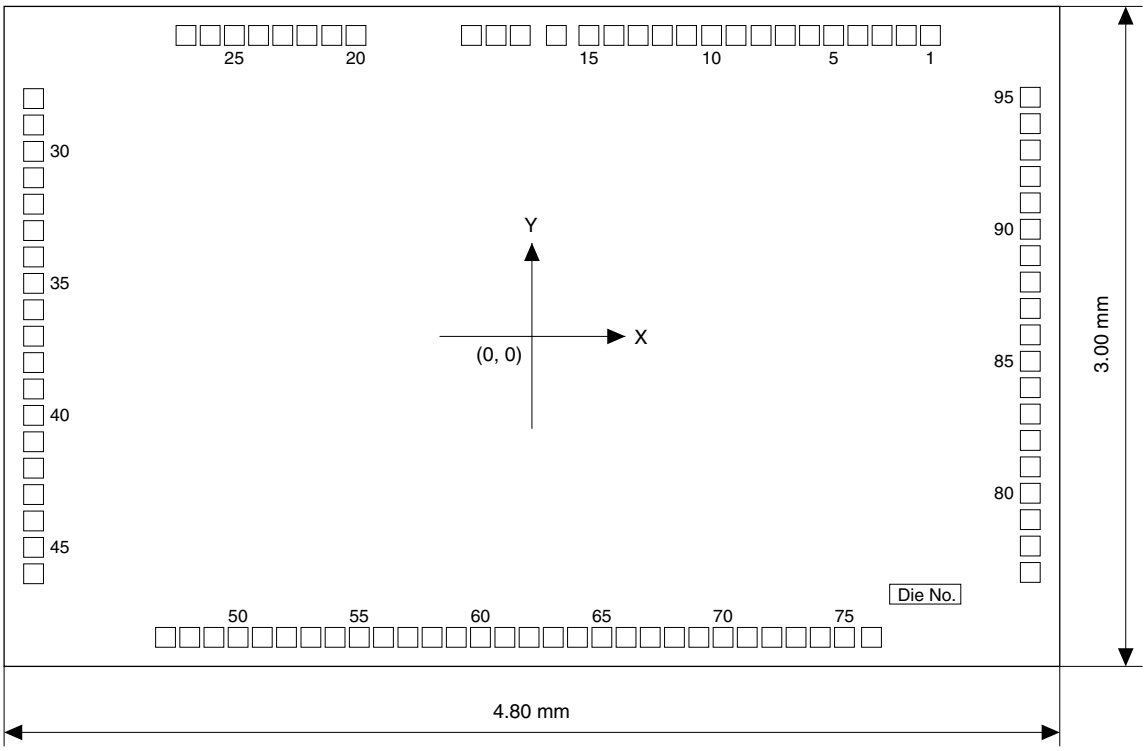
QFP17-144pin

(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 90 µm

9.2 Pad Coordinates

Unit: mm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	COM0	1.812	1.368	33	SEG24	-2.266	0.481	65	P13	0.318	-1.368
2	COM1	1.702	1.368	34	SEG25	-2.266	0.361	66	R00	0.428	-1.368
3	CA	1.592	1.368	35	SEG26	-2.266	0.241	67	R01	0.538	-1.368
4	CB	1.482	1.368	36	SEG27	-2.266	0.121	68	R02	0.648	-1.368
5	V_{C1}	1.372	1.368	37	SEG28	-2.266	0.001	69	R03	0.759	-1.368
6	V_{C2}	1.262	1.368	38	SEG29	-2.266	-0.119	70	BZ	0.869	-1.368
7	V_{C3}	1.152	1.368	39	SEG30	-2.266	-0.239	71	V_{SS}	0.979	-1.368
8	V_{SSA}	1.042	1.368	40	SEG31	-2.266	-0.359	72	AO1	1.091	-1.368
9	RFOUT	0.928	1.368	41	SEG32	-2.266	-0.479	73	AO2	1.201	-1.368
10	RFIN0	0.817	1.368	42	SEG33	-2.266	-0.599	74	BO1	1.311	-1.368
11	RFIN1	0.703	1.368	43	SEG34	-2.266	-0.719	75	BO2	1.421	-1.368
12	REF0	0.593	1.368	44	SEG35	-2.266	-0.839	76	V_{DD}	1.544	-1.368
13	SEN0	0.483	1.368	45	SEG36	-2.266	-0.959	77	SEG0	2.266	-1.073
14	REF1	0.373	1.368	46	SEG37	-2.266	-1.079	78	SEG1	2.266	-0.953
15	SEN1	0.259	1.368	47	COM2	-1.666	-1.368	79	SEG2	2.266	-0.833
16	HUD	0.111	1.368	48	COM3	-1.556	-1.368	80	SEG3	2.266	-0.713
17	V_{DDA}	-0.053	1.368	49	V_{DD}	-1.446	-1.368	81	SEG4	2.266	-0.593
18	V_{DDA}	-0.163	1.368	50	K00	-1.336	-1.368	82	SEG5	2.266	-0.473
19	V_{OSC}	-0.275	1.368	51	K01	-1.226	-1.368	83	SEG6	2.266	-0.353
20	OSC1	-0.800	1.368	52	K02	-1.116	-1.368	84	SEG7	2.266	-0.233
21	OSC2	-0.910	1.368	53	K03	-1.005	-1.368	85	SEG8	2.266	-0.113
22	V_{D1}	-1.023	1.368	54	K10	-0.895	-1.368	86	SEG9	2.266	0.007
23	OSC3	-1.133	1.368	55	K11	-0.785	-1.368	87	SEG10	2.266	0.127
24	OSC4	-1.243	1.368	56	K12	-0.675	-1.368	88	SEG11	2.266	0.247
25	V_{SS}	-1.353	1.368	57	K13	-0.564	-1.368	89	SEG12	2.266	0.367
26	TEST	-1.463	1.368	58	P00	-0.454	-1.368	90	SEG13	2.266	0.487
27	RESET	-1.573	1.368	59	P01	-0.344	-1.368	91	SEG14	2.266	0.607
28	SEG19	-2.266	1.081	60	P02	-0.234	-1.368	92	SEG15	2.266	0.727
29	SEG20	-2.266	0.961	61	P03	-0.123	-1.368	93	SEG16	2.266	0.847
30	SEG21	-2.266	0.841	62	P10	-0.013	-1.368	94	SEG17	2.266	0.967
31	SEG22	-2.266	0.721	63	P11	0.097	-1.368	95	SEG18	2.266	1.087
32	SEG23	-2.266	0.601	64	P12	0.207	-1.368	–	–	–	–

APPENDIX PERIPHERAL CIRCUIT BOARDS FOR S1C63656

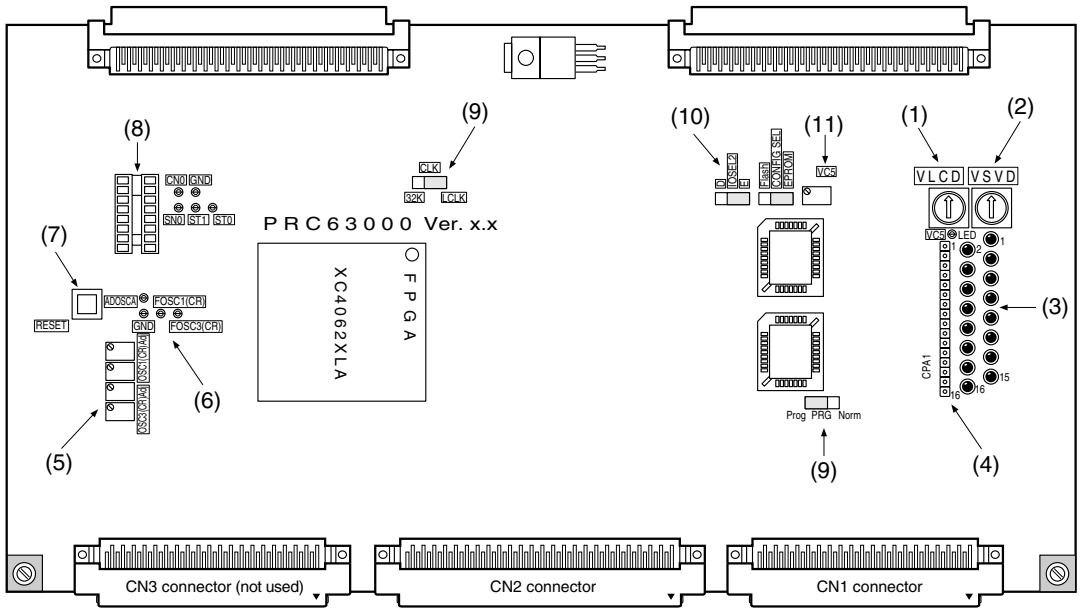
This section describes how to use the Peripheral Circuit Boards for the S1C63656 (S5U1C63000P1 and S5U1C63658P2), which provide emulation functions when mounted on the debugging tool for the S1C63 Family of 4-bit single-chip microcomputers, the ICE (S5U1C63000H1/S5U1C63000H2).

This description of the S1C63 Family Peripheral Circuit Board (S5U1C63000P1) provided in this document assumes that circuit data for the S1C63656 has already been downloaded to the board. For information on downloading various circuit data, please see Section A.3. Please refer to the user's manual provided with your ICE for detailed information on its functions and method of use.

A.1 Names and Functions of Each Part

A.1.1 S5U1C63000P1

The S5U1C63000P1 board provides peripheral circuit functions of S1C63 Family microcomputers other than the core CPU. The following explains the names and functions of each part of the S5U1C63000P1 board.



(1) VLCD

When external LCD power supply has been selected by mask option, you can turn this control to adjust the LCD drive power supply voltage.

(2) VSVD

This control allows you to vary the power supply voltage artificially in order to verify the operation of the power supply voltage detect function (SVD).

(3) Register monitor LEDs

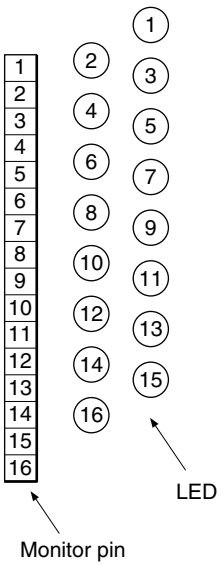
These LEDs correspond one-to-one to the registers and motor driver outputs listed below. The LED lights when the data is logic "1" and goes out when the data is logic "0".
OSCC, CLKCHG, LPWR, SVDS0–SVDS2, SVDON, AO1, AO2, BO1, BO2

(4) Register monitor pins

These pins correspond one-to-one to the registers and motor driver outputs listed below. The pin outputs a high for logic "1" and a low for logic "0".

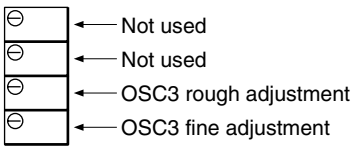
Monitor		LED	
Pin No.	Name	LED No.	Name
1	DONE *	1	DONE *
2	–	2	–
3	–	3	–
4	–	4	–
5	–	5	–
6	OSCC	6	OSCC
7	CLKCHG	7	CLKCHG
8	LPWR	8	LPWR
9	SVDS0	9	SVDS0
10	SVDS1	10	SVDS1
11	SVDS2	11	SVDS2
12	SVDON	12	SVDON
13	AO1	13	AO1
14	AO2	14	AO2
15	BO1	15	BO1
16	BO2	16	BO2

∗ DONE: The monitor pin outputs a high while the LED lights when initialization of this board completes without problems.



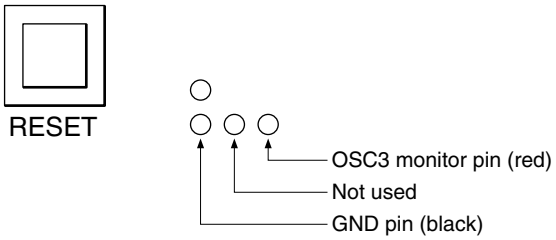
(5) CR oscillation frequency adjusting control

This control allows you to adjust the OSC3 oscillation frequency. This function is effective when ceramic oscillation is selected for the OSC3 oscillation circuit by mask option as well as when CR oscillation is selected. The oscillation frequency can be adjusted in the range of approx. 100 kHz to 8 MHz. Note that the actual IC does not operate with all of these frequencies; refer to Chapter 7, "Electrical Characteristics", to select the appropriate operating frequency.



(6) CR oscillation frequency monitor pins

These pins allow you to monitor the clock waveform from the CR oscillation circuit with an oscilloscope. Note that these pins always output a signal waveform whether or not the oscillation circuit is operating.



(7) RESET switch

This switch initializes the internal circuits of this board and feeds a reset signal to the ICE.

(8) External part connecting socket

Unused

(9) CLK and PRG switch

If power to the ICE is shut down before circuit data downloading is complete, the circuit configuration in this board will remain incomplete, and the debugger may not be able to start when you power on the ICE once again. In this case, temporarily power off the ICE and set CLK to the 32K position and the PRG switch to the Prog position, then switch on power for the ICE once again. This should allow the debugger to start up, allowing you to download circuit data. After downloading the circuit data, temporarily power off the ICE and reset CLK and PRG to the LCLK and the Norm position, respectively. Then power on the ICE once again.

(10) IOSEL2

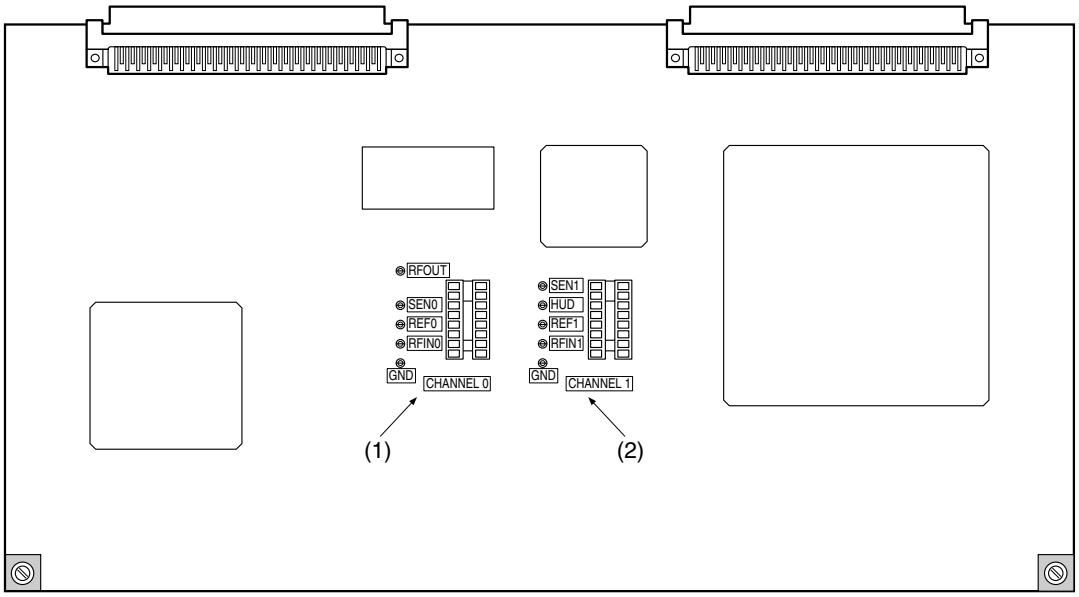
When downloading circuit data, set IOSEL2 to the "E" position. Otherwise, set to the "D" position.

(11) VC5

When the internal LCD power supply has been selected by mask option, you can turn this control to fine-adjust the LCD drive power supply voltage. Note, however, that the LCD drive power supply voltage in the actual IC is set according to the contents of the LCD contrast adjustment register.

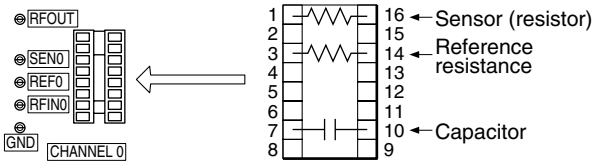
A.1.2 S5U1C63658P2

The S5U1C63658P2 board provides the R/f converter function that supports resistive sensors such as a thermistor and resistive humidity sensors.
The following explains the names and functions of each part of the S5U1C63658P2 board.



(1) R/f converter monitor pins and external part connecting socket (Channel 0)

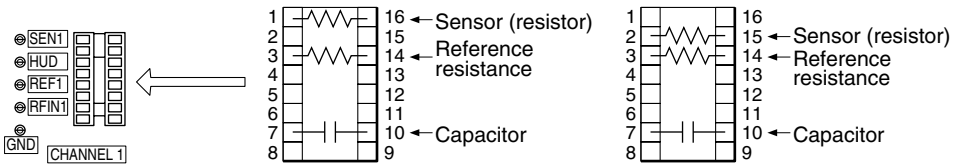
These monitor pins are used to check the operation of R/f converter channel 0. The socket is used to connect external resistors and a capacitor for R/f conversion.
Mount resistors and a capacitor on the platform attached with the S5U1C63658P2 and then connect it to the onboard socket.



Connecting a DC-bias resistive sensor (e.g. thermistor)

(2) R/f converter monitor pins and external part connecting socket (Channel 1)

These monitor pins are used to check the operation of R/f converter channel 1. The socket is used to connect external resistors and a capacitor for R/f conversion.
Mount resistors and a capacitor on the platform attached with the S5U1C63658P2 and then connect it to the onboard socket.



Connecting a AC-bias resistive humidity sensor

Connecting a DC-bias resistive sensor (e.g. thermistor)

The sensor connect position changes according to the sensor type to be used.
Do not mount an AC bias sensor and a DC bias sensor at the same time as it causes a malfunction.

A.2 Connecting to the Target System

This section explains how to connect the S5U1C63000P1 to the target system.
First insert the S5U1C63000P1 board into the second upper slot of the ICE and the S5U1C63658P2 board into the top slot.
Download the circuit data to the S5U1C63000P1 board before installing the S5U1C63658P2 board if the S5U1C63000P1 board does not include the correct circuit data. See Section A.3 for downloading circuit data.

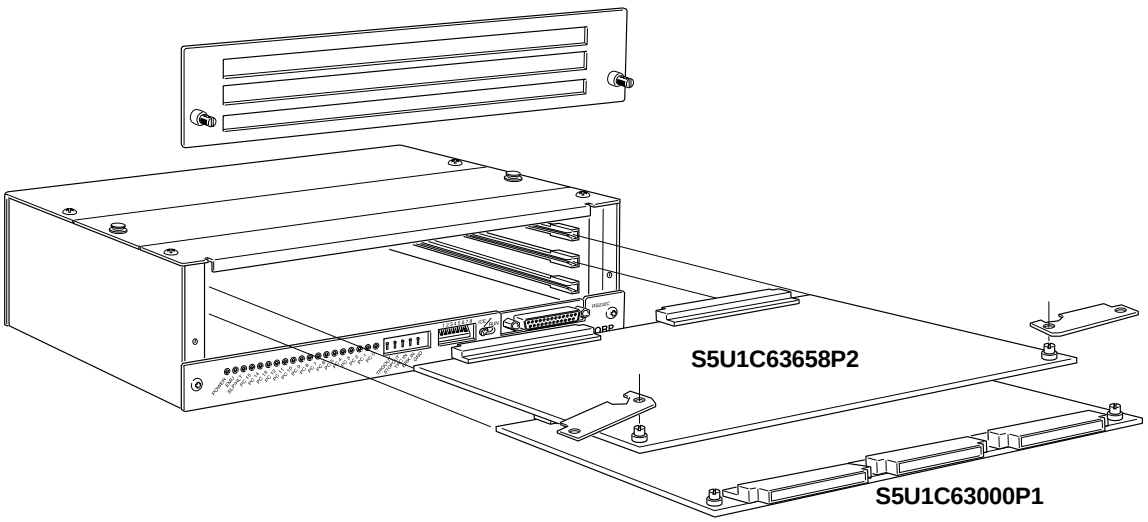


Fig. A.2.1 Installing the peripheral circuit boards to the ICE

- **Installing the S5U1C63000P1/63658P2 board**

Set the jig included with the ICE into position as shown in Figure A.2.2. Using this jig as a lever, push it toward the inside of the board evenly on the left and right sides. After confirming that the board has been firmly fitted into the internal slot of the ICE, remove the jig.

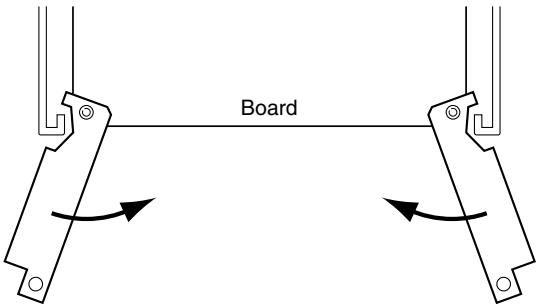


Fig. A.2.2
Installing the board

- **Dismounting the S5U1C63000P1/63658P2 board**

Set the jig included with the ICE into position as shown in Figure A.2.3. Using this jig as a lever, push it toward the outside of the board evenly on the left and right sides. After confirming that the board has been dismounted from the backboard connector, pull the board out of the ICE.

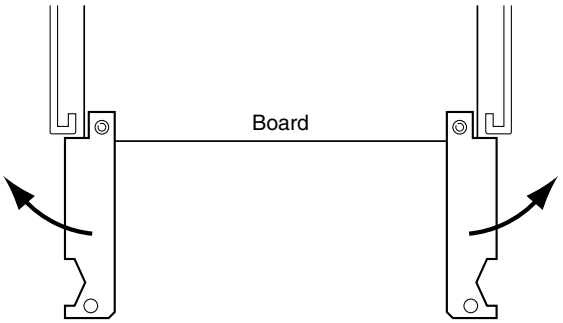


Fig. A.2.3
Dismounting the board

To connect this board (S5U1C63000P1) to the target system, use the I/O connecting cables supplied with the board (80-pin/40-pin × 2, 100-pin/50-pin × 2, flat type). Take care when handling the connectors, since they conduct electrical power (V_{DD} = +3.3 V).

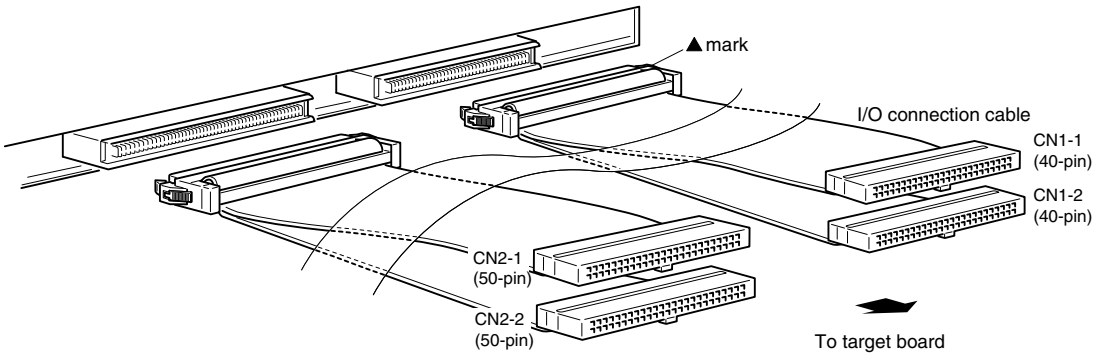


Fig. A.2.4 Connecting the S5U1C63000P1 to the target system

Table A.2.1 I/O connector pin assignment

40-pin CN1-1 connector		40-pin CN1-2 connector	
No.	Pin name	No.	Pin name
1	VDD (= 3.3 V)	1	VDD (= 3.3 V)
2	VDD (= 3.3 V)	2	VDD (= 3.3 V)
3	K00	3	R00
4	K01	4	R01
5	K02	5	R02
6	K03	6	R03
7	K10	7	Cannot be connected
8	K11	8	Cannot be connected
9	K12	9	Cannot be connected
10	K13	10	Cannot be connected
11	VSS	11	VSS
12	VSS	12	VSS
13	P00	13	BZ
14	P01	14	Cannot be connected
15	P02	15	Cannot be connected
16	P03	16	Cannot be connected
17	P10	17	Cannot be connected
18	P11	18	Cannot be connected
19	P12	19	Cannot be connected
20	P13	20	Cannot be connected
21	VDD (= 3.3 V)	21	VDD (= 3.3 V)
22	VDD (= 3.3 V)	22	VDD (= 3.3 V)
23	Cannot be connected	23	AO1
24	Cannot be connected	24	AO2
25	Cannot be connected	25	BO1
26	Cannot be connected	26	BO2
27	Cannot be connected	27	Cannot be connected
28	Cannot be connected	28	Cannot be connected
29	Cannot be connected	29	Cannot be connected
30	Cannot be connected	30	Cannot be connected
31	Vss	31	VSS
32	Vss	32	VSS
33	Cannot be connected	33	Cannot be connected
34	Cannot be connected	34	Cannot be connected
35	Cannot be connected	35	Cannot be connected
36	Cannot be connected	36	Cannot be connected
37	Cannot be connected	37	Cannot be connected
38	Cannot be connected	38	RESET
39	Vss	39	VSS
40	Vss	40	VSS

50-pin CN2-1 connector		50-pin CN2-2 connector	
No.	Pin name	No.	Pin name
1	VDD (= 3.3 V)	1	VDD (= 3.3 V)
2	VDD (= 3.3 V)	2	VDD (= 3.3 V)
3	SEG0 (DC)	3	Cannot be connected
4	SEG1 (DC)	4	Cannot be connected
5	SEG2 (DC)	5	Cannot be connected
6	SEG3 (DC)	6	Cannot be connected
7	SEG4 (DC)	7	Cannot be connected
8	SEG5 (DC)	8	Cannot be connected
9	SEG6 (DC)	9	Cannot be connected
10	SEG7 (DC)	10	Cannot be connected
11	VSS	11	VSS
12	VSS	12	VSS
13	SEG8 (DC)	13	Cannot be connected
14	SEG9 (DC)	14	Cannot be connected
15	SEG10 (DC)	15	Cannot be connected
16	SEG11 (DC)	16	Cannot be connected
17	SEG12 (DC)	17	Cannot be connected
18	SEG13 (DC)	18	Cannot be connected
19	SEG14 (DC)	19	Cannot be connected
20	SEG15 (DC)	20	Cannot be connected
21	VDD (= 3.3 V)	21	VDD (= 3.3 V)
22	VDD (= 3.3 V)	22	VDD (= 3.3 V)
23	SEG16 (DC)	23	Cannot be connected
24	SEG17 (DC)	24	Cannot be connected
25	SEG18 (DC)	25	Cannot be connected
26	SEG19 (DC)	26	Cannot be connected
27	SEG20 (DC)	27	Cannot be connected
28	SEG21 (DC)	28	Cannot be connected
29	SEG22 (DC)	29	Cannot be connected
30	SEG23 (DC)	30	Cannot be connected
31	VSS	31	VSS
32	VSS	32	VSS
33	SEG24 (DC)	33	Cannot be connected
34	SEG25 (DC)	34	Cannot be connected
35	SEG26 (DC)	35	Cannot be connected
36	SEG27 (DC)	36	Cannot be connected
37	SEG28 (DC)	37	Cannot be connected
38	SEG29 (DC)	38	Cannot be connected
39	SEG30 (DC)	39	Cannot be connected
40	SEG31 (DC)	40	Cannot be connected
41	VDD (= 3.3 V)	41	VDD (= 3.3 V)
42	VDD (= 3.3 V)	42	VDD (= 3.3 V)
43	SEG32 (DC)	43	Cannot be connected
44	SEG33 (DC)	44	Cannot be connected
45	SEG34 (DC)	45	Cannot be connected
46	SEG35 (DC)	46	Cannot be connected
47	SEG36 (DC)	47	Cannot be connected
48	SEG37 (DC)	48	Cannot be connected
49	Cannot be connected	49	Cannot be connected
50	Cannot be connected	50	Cannot be connected

∗ Connectors CN2-1 and CN2-2 are used when the SEG pins are set for DC output by mask option.

A.3 Downloading to S5U1C63000P1

A.3.1 Downloading Circuit Data 1 – when new ICE (S5U1C63000H2) is used

The S5U1C63000P1 board comes with the FPGA that contains factory inspection data, therefore the circuit data for the model to be used should be downloaded. The following explains the downloading procedure.

1) Remove the ICE top cover and then set the DIP switch "IOSEL2" on this board to the "E" position.
2) Connect the ICE to the host PC. Then turn the host PC and ICE on.
3) Invoke the debugger included in the assembler package (ver. 5 or later). For how to use the ICE and debugger, refer to the manuals supplied with the ICE and assembler package.
4) Download the circuit data file (.mot) corresponding to the model by entering the following commands in the command window.

`>XFER`	(erase all)
`>XFWR` *<file name>*	(download the specified file)*
`>XFCP` *<file name>*	(compare the specified file and downloaded data)

   * The downloading takes about 15 minutes.
5) Terminate the debugger and then turn the ICE off.
6) Set the DIP switch "IOSEL2" on this board to the "D" position.
7) Turn the ICE on and invoke the debugger again. Debugging can be started here.

A.3.2 Downloading Circuit Data 2 – when previous ICE (S5U1C63000H1) is used

The standard ICE (S5U1C63000H1, previous model) did not support the circuit data download function for this board. To use the download function, update the ICE firmware according to the following procedure.

1) Set the baud rate of the ICE to 9600 bps. Refer to the manual supplied with the ICE for setting the DIP switch.
2) Connect the ICE to the host PC and then start up the host PC in DOS. When Windows is running, restart in DOS mode.

   Note: Do not use the DOS prompt of Windows.
3) Turn the ICE on.
4) Configure the RS232C parameters for the host PC as follows:

   `C:\>MODE COM1:9600,n,8,1,p` (9600 bps, 8-bit data, 1 stop bit, no parity)
5) Copy the following files included in the assembler package (ver. 5 or later) to a directory on the hard disk.

   `tm63.exe, ice63.com, i63com.o, i63par`
6) Move to the directory in Step 5, run the TM63. TM63 enters command ready status after invocation, enter a command as follows:

```
C:\>tm63 xat↵
TM63 start on IBM PC
TM63 start V01.01
>dlf ice63.com i63com.o i63par 0b↵
                ...
>q↵
```

7) Enter "q" to terminate TM63 after the prompt mark is displayed.
8) The ICE firmware is now updated. Turn the ICE off and then download the circuit data by the procedure described in Section A.3.1.

A.4 Usage Precautions

To ensure correct use of the peripheral circuit board, please observe the following precautions.

A.4.1 Operational precautions

(1) Before inserting or removing cables, turn off power to all pieces of connected equipment.
(2) Do not turn on power or load mask option data if all of the input ports (K00–K03) are held low. Doing so may activate the multiple key entry reset function.
(3) Before debugging, always be sure to load mask option data.

A.4.2 Differences with the actual IC

(1) Differences in I/O

<Interface power supply>

S5U1C63000P1 and target system interface voltage is set to +3.3 V. To obtain the same interface voltage as in the actual IC, attach a level shifter circuit, etc. on the target system side to accommodate the required interface voltage.

<Each output port's drive capability>

The drive capability of each output port on S5U1C63000P1 is higher than that of the actual IC. When designing application system and software, refer to Chapter 7, "Electrical Characteristics", to confirm each output port's drive capability.

<Each port's protective diode>

All I/O ports incorporate a protective diode for VDD and VSS, and the interface signals between S5U1C63000P1 and the target system are set to +3.3 V. Therefore, S5U1C63000P1 and the target system cannot be interfaced with voltages exceeding VDD by setting the output ports for open-drain mode.

<Pull-down resistance value>

The pull-down resistance values on S5U1C63000P1 are set to 220 kΩ which differ from those for the actual IC. For the resistance values on the actual IC, refer to Chapter 7, "Electrical Characteristics". Note that when using pull-down resistors to pull the input pins low, the input pins may require a certain period to reach a valid low level. Exercise caution if a key matrix circuit is configured using a combination of output and input ports, since fall delay times on these input ports differ from those of the actual IC.

(2) Differences in current consumption

The amount of current consumed by the peripheral circuit boards differ significantly from that of the actual IC. Inspecting the LEDs on S5U1C63000P1 may help you keep track of approximate current consumption. The following factors/components greatly affect device current consumption:

<Those which can be verified by LEDs and monitor pins>

a) Run and Halt execution ratio (verified by LEDs and monitor pins on the ICE)
b) OSC3 oscillation on/off circuit (OSCC)
c) CPU clock select circuit (CLKCHG)
d) SVD circuit on/off circuit (SVDON)
e) LCD power supply on/off circuit (LPWR)
f) R/f converter oscillation on/off circuit (RFOUT)
g) Motor drive pulse outputs (AO1, AO2, BO1, BO2)

<Those that can only be counteracted by system or software>

h) Current consumed by the internal pull-down resistors
i) Input ports in a floating state

(3) Functional precautions

<LCD power supply circuit>

There is a finite delay time from the point at which the LCD power supply circuit (LPWR) turns on until an LCD drive waveform is output. On S5U1C63000P1, this delay is set to approx. 100 msec, which differs from that of the actual IC.

<Differences in LCD drive waveform>

This board is capable of static waveform output even if the internal LCD power supply is used. However, select 1/2-bias external power supply by mask option when driving the LCD with the static waveform.

<SVD circuit>

- The SVD function is realized by artificially varying the power supply voltage using the VSVD control on S5U1C63000P1.
- There is a finite delay time from when the power to the SVD circuit turns on until actual detection of the voltage. On S5U1C63000P1, this delay is set to approx. 500 µsec, which differs from that of the actual IC. Refer to Chapter 7, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.

<Oscillation circuit>

- A wait time is required before oscillation stabilizes after the OSC3 oscillation control circuit (OSCC) is turned on. On S5U1C63000P1, even when OSC3 oscillation is changed (CLKCHG) without a wait time, OSC3 will function normally. Refer to Chapter 7, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.
- Use separate instructions to switch the clock from OSC3 to OSC1 and to turn off the OSC3 oscillation circuit. If executed simultaneously with a single instruction, these operations, although good with S5U1C63000P1, may not function properly well with the actual IC.
- Because the logic level of the oscillation circuit is high, the timing at which the oscillation starts on S5U1C63000P1 differs from that of the actual IC.
- S5U1C63000P1 contains oscillation circuits for OSC1 and OSC3. Keep in mind that even though the actual IC may not have a resonator connected to its OSC3, its emulator can operate with the OSC3 circuit.
- S5U1C63000P1 generates the OSC3 clock using the onboard CR oscillation circuit even if ceramic oscillation is selected for the OSC3 oscillation circuit by mask option.

<Access to undefined address space>

If any undefined space in the S1C63656's internal ROM/RAM or I/O is accessed for data read or write operations, the read/written value is indeterminate. Additionally, it is important to remain aware that indeterminate state differs between S5U1C63000P1 and the actual IC. Note that the ICE (S5U1C63000H1/S5U1C63000H2) incorporates the program break function caused by accessing to an undefined address space.

<Reset circuit>

Keep in mind that the operation sequence from when the ICE and the peripheral circuit boards are powered on until the time at which the program starts running differs from the sequence from when the actual IC is powered on till the program starts running. This is because S5U1C63000P1 becomes capable of operating as a debugging system after the user program and optional data are down-loaded. When operating the ICE after placing it in free-running mode, always apply a system reset. A system reset can be performed by pressing the reset switch on S5U1C63000P1, by a reset pin input, or by holding the input ports high simultaneously.

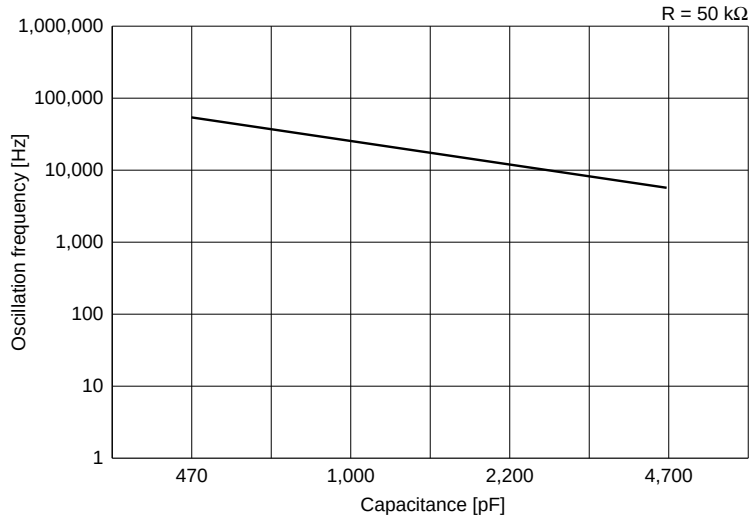
<Internal power supply circuit>

The LCD drive voltage on this board is different from that on the actual IC.

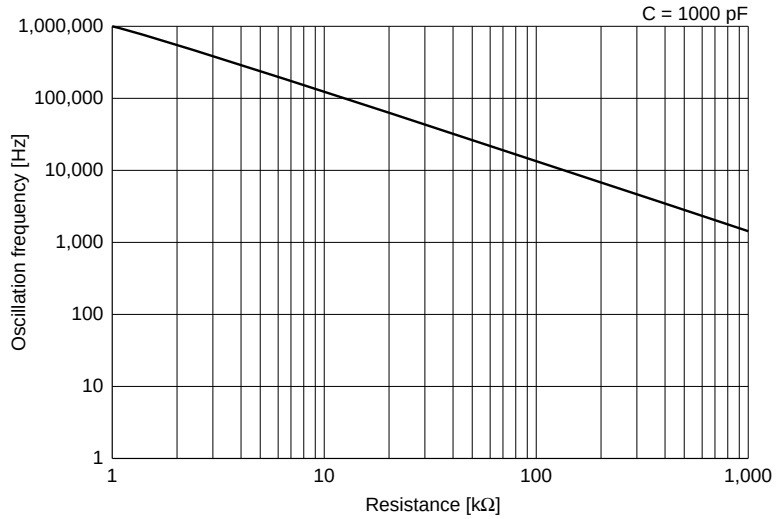
<R/f converter>

- If the debugger breaks executing of the target program while the R/f converter is counting the oscillation, the R/f converter stops counting. Note that the R/f converter will not able to load a proper result if the count operation is resumed from that point.
- The signal polarity of the R/f converter oscillation frequency output (RFOUT) is inverted. RFOUT of the S5U1C63658P2 is active High and that of the actual IC is active Low. Pay attention when using the output signal for a purpose other than measurement of the oscillation frequency.
- The following shows the oscillation characteristics (reference value) of the R/f converter on the S5U1C63658P2:

R/f converter oscillation frequency - capacitance characteristic (reference value)



R/f converter oscillation frequency - resistance characteristic (reference value)



A.5 Product Specifications

A.5.1 Specifications of S5U1C63000P1

S5U1C63000P1

Dimension:	254 mm (wide) × 144.8 mm (depth) × 13 mm (height) (including screws)
Weight:	Approx. 300 g
Power supply:	DC 5 V ± 5%, less than 1 A (supplied from ICE main unit)

I/O connection cable (80-pin)

S5U1C63000P1 connector:	KEL8830E-080-170L	
Cable connector (80-pin):	KEL8822E-080-171	
Cable connector (40-pin):	3M7940-6500SC	1 pair
Cable:	40-pin flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

I/O connection cable (100-pin)

S5U1C63000P1 connector:	KEL8830E-100-170L	
Cable connector (100-pin):	KEL8822E-100-171	
Cable connector (50-pin):	3M7950-6500SC	1 pair
Cable:	50-pin flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

Accessories

40-pin connector for connecting to target system:
3M3432-6002LCSC × 2
50-pin connector for connecting to target system:
3M3433-6002LCSC × 2

A.5.2 Specifications of S5U1C63658P2

S5U1C63658P2

Dimension:	254 mm (width) × 144.8 mm (depth) × 13 mm (height) (including screws)
Weight:	Approx. 130 g
Power supply:	DC 5 V ± 5%, less than 10 mA (supplied from ICE main unit and converted into 3.3 V by the onboard regulator)

Accessory

Discreet platform (for mounting external resistors and capacitors of the R/f converter):
DIS12-016-403 (KEL) × 2

EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
214 Devcon Drive,
San Jose, CA 95112, USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-8522-1199 FAX: +86-10-8522-1125

SHANGHAI BRANCH
7F, Block B, Hi-Tech Bldg., 900 Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5577 FAX: +86-21-5423-4677

SHENZHEN BRANCH
12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.
Unit 715-723, 7/F Trade Square, 681 Cheung Sha Wan Road,
Kowloon, Hong Kong.
Phone: +852-2585-4600 FAX: +852-2827-4346

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.
KOREA OFFICE
5F, KLI 63 Bldg., 60 Yoido-dong,
Youngdeungpo-Ku, Seoul 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.
MICRODEVICES OPERATIONS DIVISION

IC Sales & Marketing Department
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

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