EPSON
EXCEED YOUR VISION

S1S60000
Application Note

No.2 Ping reply method

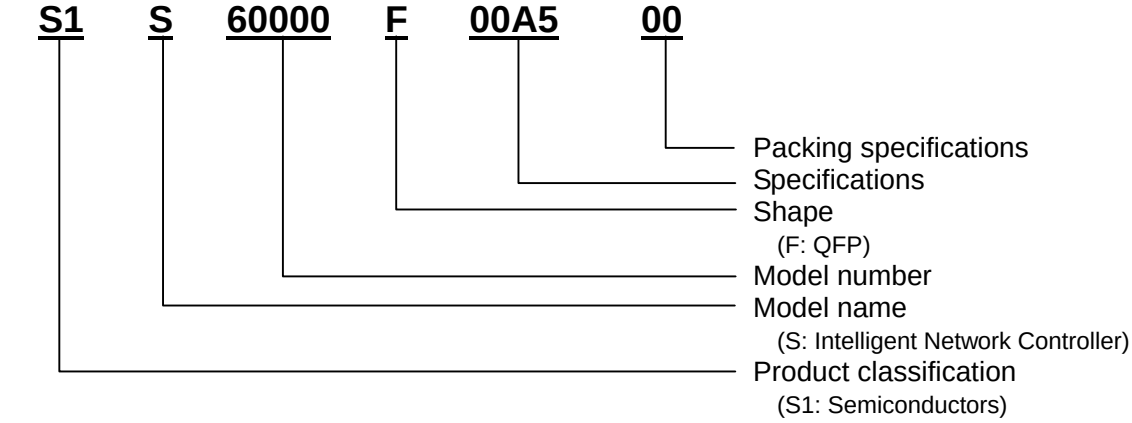
SEIKO EPSON CORPORATION

Rev.1.1

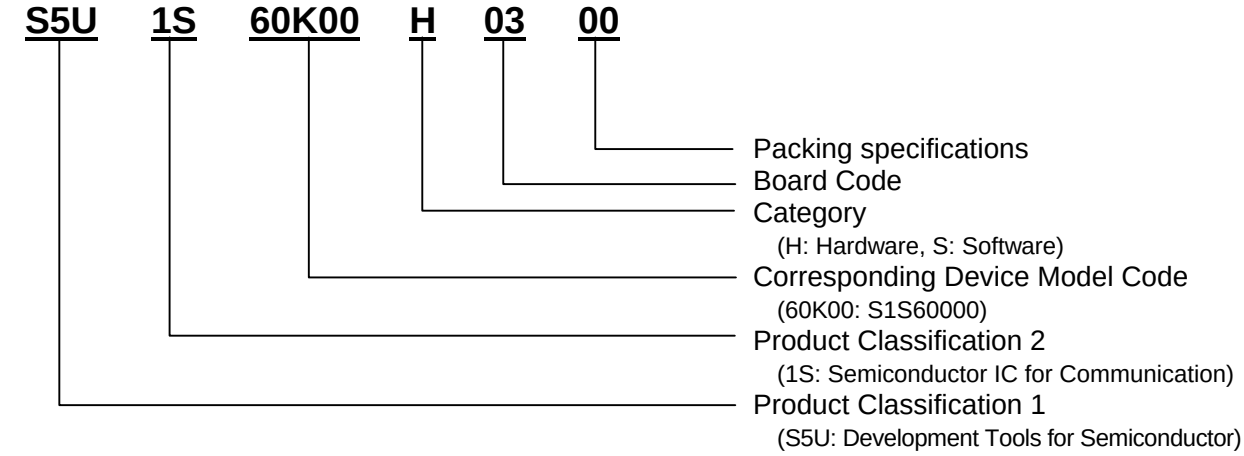
NOTICE

Configuration of product number

●DEVICES



●Evaluation Board



CONTENTS

1. DESCRIPTION

To allow S1S60000 to reply to ping, a MAC address and IP address must be set. The MAC address can be set by writing it to the S1S60000 internal register. The IP address can be set by opening the SYSTEM communication end point. Completing these two settings causes S1S60000 to reply (ICMP Echo reply) to ping (ICMP Echo request) sent through the network.

To perform this processing, the host CPU must read statuses and parameters and write commands and parameters through the host interface of S1S60000.
This document describes the procedure for enabling S1S60000 to reply to pings while explaining how to use the host interface.
To perform the procedure, the host interface of S1S60000 will be allocated to the address of the host CPU to create the program of the host CPU. Alternatively, you can operate the address allocated to S1S60000 using the debugger of host CPU.

The procedure is as follows.

① **Confirm that S1S60000 is booted.**
Read the boot status.

② **Confirm the status of S1S60000.**
Read the event status and option parameters.

③ **Set a MAC address.**
Write the send command and option parameters.

④ **Set an IP address.**
Write the open command and option parameters.

⑤ **Confirm ping reply (ICMP Echo reply).**
Transmit ping from the PC to S1S60000.

* See description of host interface port in 4.1 and 4.2 in “S1S60000 Technical Manual” before reading the following chapter.
The description of command port/status port, data port, and flag port is provided.

2. CONFIRMATION OF S1S60000 BOOT

S1S60000 issues the boot status when it is booted. The host CPU reads the boot status to confirm that it has been booted. This chapter describes how to read statuses through reading the boot status.

2.1 Confirming the host interface status

When the status or data is set in host interface port, the HINT pin changes. Connecting the HINT pin to the interrupt pin of the host CPU allows interrupt control for reading the status and data. Setting the HINTPOL pin to LOW enables Low active, and setting it to HIGH enables High active. Please set the interrupt input trigger mode of the host CPU to level trigger mode.
The flag port indicates the host interface processing status for commands, statuses, or data. When accessing the host interface, be sure to confirm the flag port. When not performing interrupt control, control the status by polling of the flag port.

2.2 Reading the status

When the status is set in status port, the HINT pin becomes active. Also, bit0 of the flag port is set to "1". Perform polling of the flag port when not performing interrupt control.
The HINT pin becomes active when bit0 or bit1 of the flag port is set; therefore, confirm that bit0 of the flag port is set to "1" and read the status.
The status form read from the status port is as follows.

Table 2.1 Status form

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA	Sequence number								Communication end point number				Status number			

For information on numbers corresponding to status types, refer to the "S1S60000 Series Host Interface Manual - 2.1.1.4 Status number".

2.3 Reading the boot status

In the same manner as the procedure in 2.2, read the "boot" status. Turn on the power of S1S60000 or input the reset signal and S1S60000 outputs the "boot" status (0x000b).

Table 2.2 Read value of boot status for each host CPU type

Host CPU type	boot status
8-bit connection Little Endian	LSB port: 0x0b MSB port: 0x00
8-bit connection Big Endian	LSB port: 0x00 MSB port: 0x0b
16-bit connection Little Endian	0x000b
16-bit connection Big Endian	0x000b

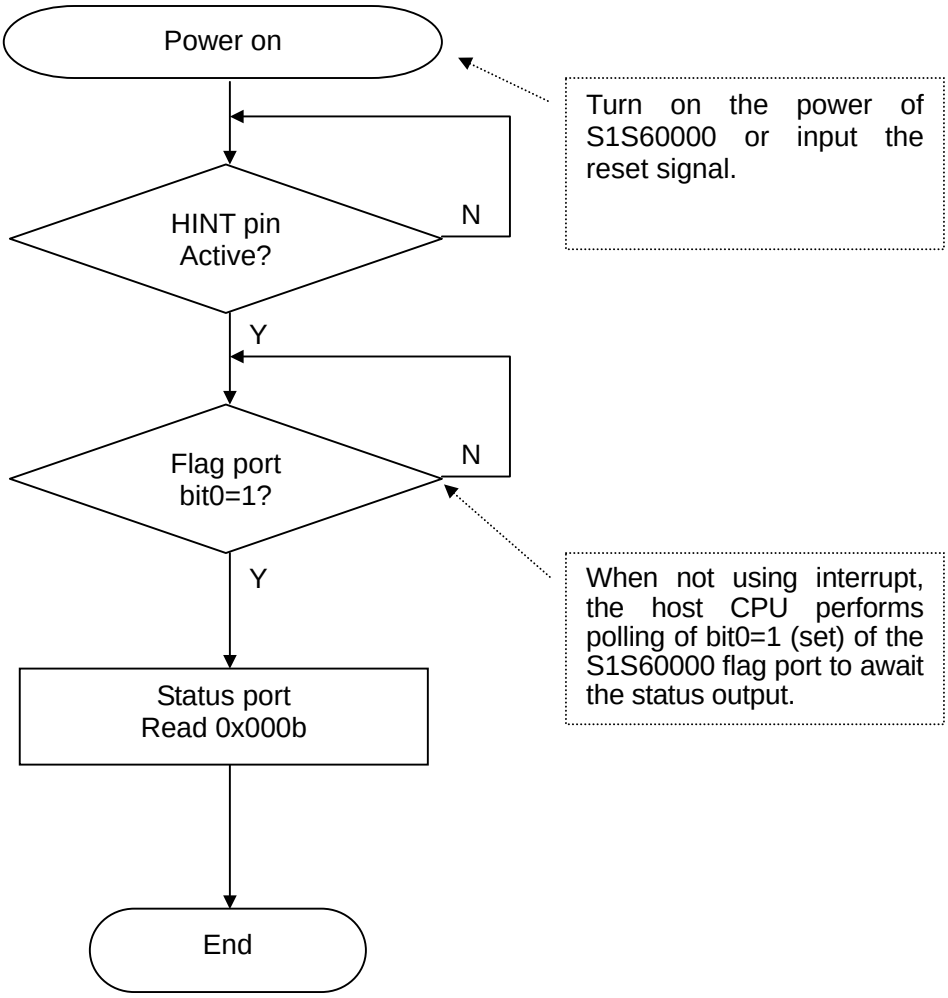


Fig.2.1 Boot status read flow

3. CONFIRMATION OF S1S60000 STATUS

S1S60000 may issue the event status to inform the host CPU of IC status. The host CPU reads the event status and option parameters to confirm which event has been informed. This chapter describes how to read the status option parameters through reading the event status and option parameters by generating a cable disconnection event and connection recovery event by disconnecting and connecting the Ethernet cable.

3.1 Reading the status option parameters

The status option parameters are data added to the status. After reading the status, read them from the data port. When the status option parameters are set, the HINT pin becomes active and bit1 of the flag port is set to “1”. Please confirm that bit1 of the flag port is set to “1” without fail before reading the data row.

3.2 Reading the cable disconnection event

In the same manner as the procedure in 3.1, read the “cable disconnection” of the “event” status by actually disconnecting the LAN cable.
When you disconnect the LAN cable, the “event” status is issued. Read the status in the same manner as “2. CONFIRMATION OF S1S60000 BOOT”. Then, the “event” status (0x000a) can be read. The “event” status is provided with 16-byte status option parameters; read them from the data port. When S1S60000 and the host CPU is 8-bit connected, the parameters are read 16 times, and when 16-bit connected, they are read eight times.
For more information about the “event” status, refer to the “S1S60000 Series Host Interface Manual - 3.11 event status”.
In the case of “cable disconnection” with the LAN cable disconnected, the following data row can be read.

Table 3.1 Cable disconnection event option parameters

BYTE	Read data	Contents	Comment
0	0x00	Fixed value	
1	0x00		
2	0x00	Flag	Reserved (0)
3	0x00	Fixed value	
4	0x00	Event type	0: Cable
5	0x00	Detail of event	0: Cable disconnection
6	0x00		In the case of cable event, 0 for all
7	0x00		
8	0x00		
9	0x00		
10	0x00		
11	0x00		
12	0x00		
13	0x00		
14	0x00		
15	0x00		

When the option parameters are stored in the memory, BYTE0 in Table 3.1 is set to the low-order address of the memory.
Read data row for each host CPU type are as follows.

Table 3.2 Data row for each host CPU type

Host CPU type	Data row
8-bit connection LittleEndian	0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00
8-bit connection BigEndian	0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00
16-bit connection LittleEndian	0x0000,0x0000,0x0000,0x0000,0x0000,0x0000,0x0000,0x0000
16-bit connection BigEndian	0x0000,0x0000,0x0000,0x0000,0x0000,0x0000,0x0000,0x0000

* Access sequence in the case of 8-bit connection: low-order port → high-order port

3. CONFIRMATION OF S1S60000 STATUS

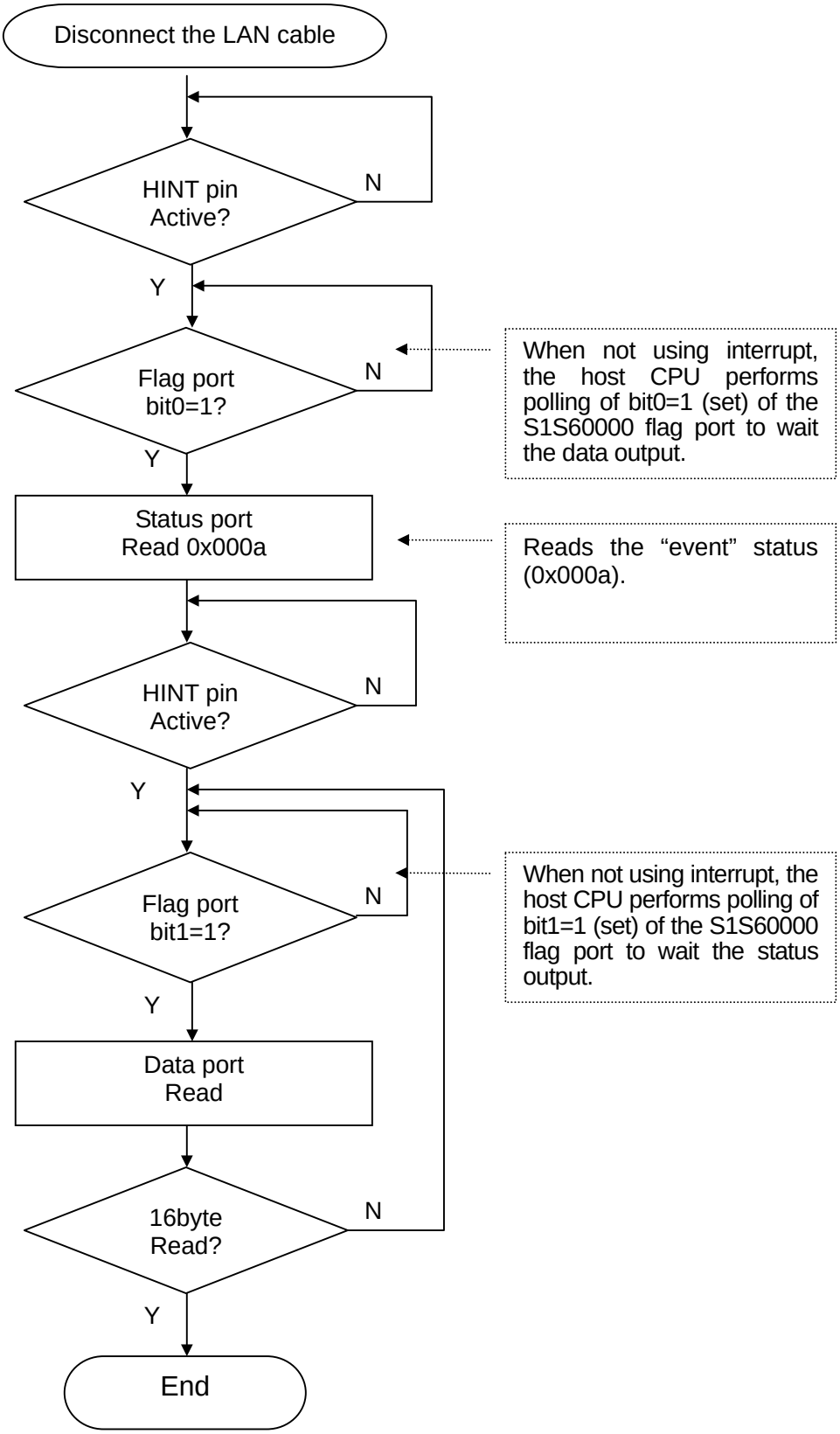


Fig.3.1 Cable disconnection event read flow

3.3 Reading cable connection recovery event

As the next step, connect the disconnected LAN cable to read the "event" status "cable connection recovery". The read method is the same as "3.2 Reading the cable disconnection event". In the case of "cable connection recovery", the following byte column can be read. The difference from "cable disconnection" is Detail of "event" of the option parameter BYTE 5: cable connection recovery=1 (the shadow area of the table).

Table 3.3 Cable connection recovery event option parameters

BYTE	Read data	Contents	Comment
0	0x00	Fixed value	
1	0x00		
2	0x00	Flag	Reserved (0)
3	0x00	Fixed value	
4	0x00	Event type	0: Cable
5	0x01	Detail of event	1: Cable connection recovery
6	0x00		In the case of cable event, 0 for all
7	0x00		
8	0x00		
9	0x00		
10	0x00		
11	0x00		
12	0x00		
13	0x00		
14	0x00		
15	0x00		

When the option parameters are stored in the memory, BYTE0 in Table 3.3 is set to the low-order address of the memory.
Read data row for each host CPU type are as follows.

Table 3.4 Data row for each host CPU type

Host CPU type	Data row
8-bit connection LittleEndian	0x00,0x00,0x00,0x00,0x00,0x01, 0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00
8-bit connection BigEndian	0x00,0x00,0x00,0x00,0x00,0x01,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00
16-bit connection LittleEndian	0x0000,0x0000,0x0100,0x0000,0x0000,0x0000,0x0000,0x0000
16-bit connection BigEndian	0x0000,0x0000,0x0001,0x0000,0x0000,0x0000,0x0000,0x0000

* Access sequence in the case of 8-bit connection: low-order port → high-order port

4. MAC ADDRESS SETTING

To make network communication, a 48-bit MAC address must be set. Set a MAC address in the internal register of S1S60000. This chapter describes how to write a command and option parameters through setting a MAC address.

4.1 Writing a command

When the host CPU writes a command in S1S60000, it confirms that bit2 of the flag port is "0" and writes it to the command port.
The command form to be written to the command port is as follows.

Table 4.1 Command form

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA	Sequence number								Communication end point number				Command number			

The sequence number is given by the host CPU. The host CPU can give any number. When the command is written, the status corresponding to the command is returned. The status corresponding to the command with the sequence number 1 is returned with the sequence number 1. The sequence number shows you to which command the returned status corresponds.
For information on numbers corresponding to command types, refer to the "S1S60000 Series Host Interface Manual - 2.1.1.3 Command number".

4.2 Writing option parameters

After reading the status corresponding to the command, confirm that bit3 of the flag port is "0" and bit4 is "1", and then write option parameters. When the option parameters are written, the status corresponding to the parameters are returned; read them in the same manner as the procedure in "2.2 Reading the status".

4.3 Setting a MAC Address

In the same manner as 4.1 and 4.2, actually write commands and option parameters here.

Although a method to store the MAC address by connecting an EEPROM is alternatively available, set it from the host CPU here. Set **00_00_48_14_01_23** (Note) for MAC address. Set the MAC address at the offset addresses 01h to 03h of the internal register of S1S60000. Set it at three offset addresses; perform the setting operation three times.
Note: Set the MAC address acquired on a customer basis. In the case of the S5U1S60K00H0300 board mounted S1S60000, the MAC address set on the EEPROM can be used.

The host CPU sets "0x0000" at the beginning of the MAC address at the offset address 01h of the internal register. The internal register to set the MAC address will be the communication end point 0 (SYSTEM communication end point). For information on the communication end point type, refer to the "S1S60000 Series Host Interface Manual - 2.1.1.2 Communication end point number".

Write the "send" command (0x0201: sequence number 02, communication end point number 0=SYSTEM, command number 1=send) to the command port. For information on the "send" command, refer to the "S1S60000 Series Host Interface Manual - 3.2 send command".

Table 4.2 Write value of send command (0x0201) for each host CPU type

Host CPU type	send command
8-bit connection Little Endian	LSB port: 0x01 MSB port: 0x02
8-bit connection Big Endian	LSB port: 0x02 MSB port: 0x01
16-bit connection Little Endian	0x0201
16-bit connection Big Endian	0x0201

S1S60000 returns the "write" status (0x0201: sequence number 02, communication end point number 0=SYSTEM, status number 1=write).

Next, write the option parameters of the "send" command. Write the following data row at the data port.

Table 4.3 send command option parameters

BYTE	Write data	Contents	Comment
0	0x00	Transmission data	In the case of internal register, there is no data following the command options.
1	0x00		
2	0x00	Flag	0 when the SYSTEM communication end point is accessed.
3	0x00	Fixed value	
4	0x01	Operation	Write (Write to the internal register)
5	0x04	Object	Internal register of S1S60000
6	0x00	Offset	Internal register/offset address 0x0001
7	0x01		
8	0x00	Fixed value	Fixed value 0 when the internal register is accessed
9	0x00		
10	0x00		
11	0x00		
12	0xff	Bit mask	Specify 1 as the operation object bit.
13	0xff		
14	0x00	Bit pattern	Write value (0x0000 at the beginning of the MAC address)
15	0x00		

When the option parameters are stored in the memory, BYTE0 in Table 4.3 is set to the low-order address of the memory.

Write data row for each host CPU type are as follows.

Table 4.4 Data row for each host CPU type

Host CPU type	Data row
8-bit connection LittleEndian	0x00,0x00,0x00,0x00,0x01,0x04,0x00,0x01,0x00,0x00,0x00,0x00,0xff,0xff,0x00,0x00
8-bit connection BigEndian	0x00,0x00,0x00,0x00,0x01,0x04,0x00,0x01,0x00,0x00,0x00,0x00,0xff,0xff,0x00,0x00
16-bit connection LittleEndian	0x0000,0x0000,0x0401,0x0100,0x0000,0x0000,0xffff,0x0000
16-bit connection BigEndian	0x0000,0x0000,0x0104,0x0001,0x0000,0x0000,0xffff,0x0000

* Access sequence in the case of 8-bit connection: low-order port → high-order port

S1S60000 returns the “ok” status (0x0203: sequence number 02, communication end point number 0=SYSTEM, status number 3=ok). Setting “0x0000” at 0bit to 15bit at the beginning of the MAC address is complete.

Next, write the subsequent “0x4814” of the MAC address to the offset address 02h of the internal register. In the same manner as the beginning of the MAC address, write the “send” command (0x0301), read the “write” status (0x0301), and write the option parameters. The sequence number has been set to number 3 in increment by 1. Write the following data row to the data port. The difference from the first setting is the offset addresses of internal register at BYTE 6 and 7 and the MAC address at BYTE 14 and 15 (the hatched areas of the table).

Table 4.5 Send command option parameters

BYTE	Write data	Contents	Comment
0	0x00	Transmission data	In the case of internal register, there is no data following the command options.
1	0x00		
2	0x00	Flag	0 when the SYSTEM communication end point is accessed.
3	0x00	Fixed value	
4	0x01	Operation	Write (Write to the internal register)
5	0x04	Object	Internal register of S1S60000
6	0x00	Offset	Internal register/offset address 0x0002
7	0x02		
8	0x00	Fixed value	Fixed value 0 when the internal register is accessed
9	0x00		
10	0x00		
11	0x00		
12	0xff	Bit mask	Specify 1 as the operation object bit.
13	0xff		
14	0x14	Bit pattern	Write value (the subsequent MAC address 4814)
15	0x48		

When the option parameters are stored in the memory, BYTE0 in Table 4.5 is set to the low-order address of the memory.

Written data row for each host CPU type are as follows.

Table 4.6 Data row for each host CPU type

Host CPU type	Data row
8-bit connection LittleEndian	0x00,0x00,0x00,0x00,0x01,0x04,0x00,0x02,0x00,0x00,0x00,0x00,0x00,0xff,0xff,0x14,0x48
8-bit connection BigEndian	0x00,0x00,0x00,0x00,0x01,0x04,0x00,0x02,0x00,0x00,0x00,0x00,0x00,0xff,0xff,0x14,0x48
16-bit connection LittleEndian	0x0000,0x0000,0x0401,0x0200,0x0000,0x0000,0xffff,0x4814
16-bit connection BigEndian	0x0000,0x0000,0x0104,0x0002,0x0000,0x0000,0xffff,0x1448

* Access sequence in the case of 8-bit connection: low-order port → high-order port

S1S60000 returns the "ok" status (0x0303). Setting at the "0x4814" part of 16-bit to 31-bit of the MAC address is complete.

At last, write the remaining "0x0123" of the MAC address at the offset address 03h of the internal register. In the same manner, write the "send" command (0x0401), read the "write" status (0x0401), and write the option parameters. The sequence number has been set to 4 in increment by 1.
Write the following data row to the data port. The difference from the second setting is the offset addresses of internal register at BYTE 6 and 7 and the MAC address at BYTE 14 and 15 (the hatched areas of the table).

Table 4.7 Send command option parameters

BYTE	Write data	Contents	Comment
0	0x00	Transmission data	In the case of internal register, there is no data following the command options.
1	0x00		
2	0x00	Flag	0 when the SYSTEM communication end point is accessed.
3	0x00	Fixed value	
4	0x01	Operation	Write (Write to the internal register)
5	0x04	Object	Internal register of S1S60000
6	0x00	Offset	Internal register/offset address 0x0003
7	0x03		
8	0x00	Fixed value	Fixed value 0 when the internal register is accessed
9	0x00		
10	0x00		
11	0x00		
12	0xff	Bit mask	Specify 1 as the operation object bit.
13	0xff		
14	0x23	Bit pattern	Write value (the subsequent MAC address 0123)
15	0x01		

When the option parameters are stored in the memory, BYTE0 in Table 4.7 is set to the low-order address of the memory.
Write data row for each host CPU type are as follows.

Table 4.8 Data row for each host CPU type

Host CPU type	Data row
8-bit connection LittleEndian	0x00,0x00,0x00,0x00,0x01,0x04,0x00,0x03,0x00,0x00,0x00,0x00,0x00,0xff,0xff,0x23,0x01
8-bit connection BigEndian	0x00,0x00,0x00,0x00,0x01,0x04,0x00,0x03,0x00,0x00,0x00,0x00,0x00,0xff,0xff,0x23,0x01
16-bit connection LittleEndian	0x0000,0x0000,0x0401,0x0300,0x0000,0x0000,0xffff,0x0123
16-bit connection BigEndian	0x0000,0x0000,0x0104,0x0003,0x0000,0x0000,0xffff,0x2301

* Access sequence in the case of 8-bit connection: low-order port → high-order port

S1S60000 returns the “ok” status (0x0403). Setting at the 48bit of the MAC address is complete.

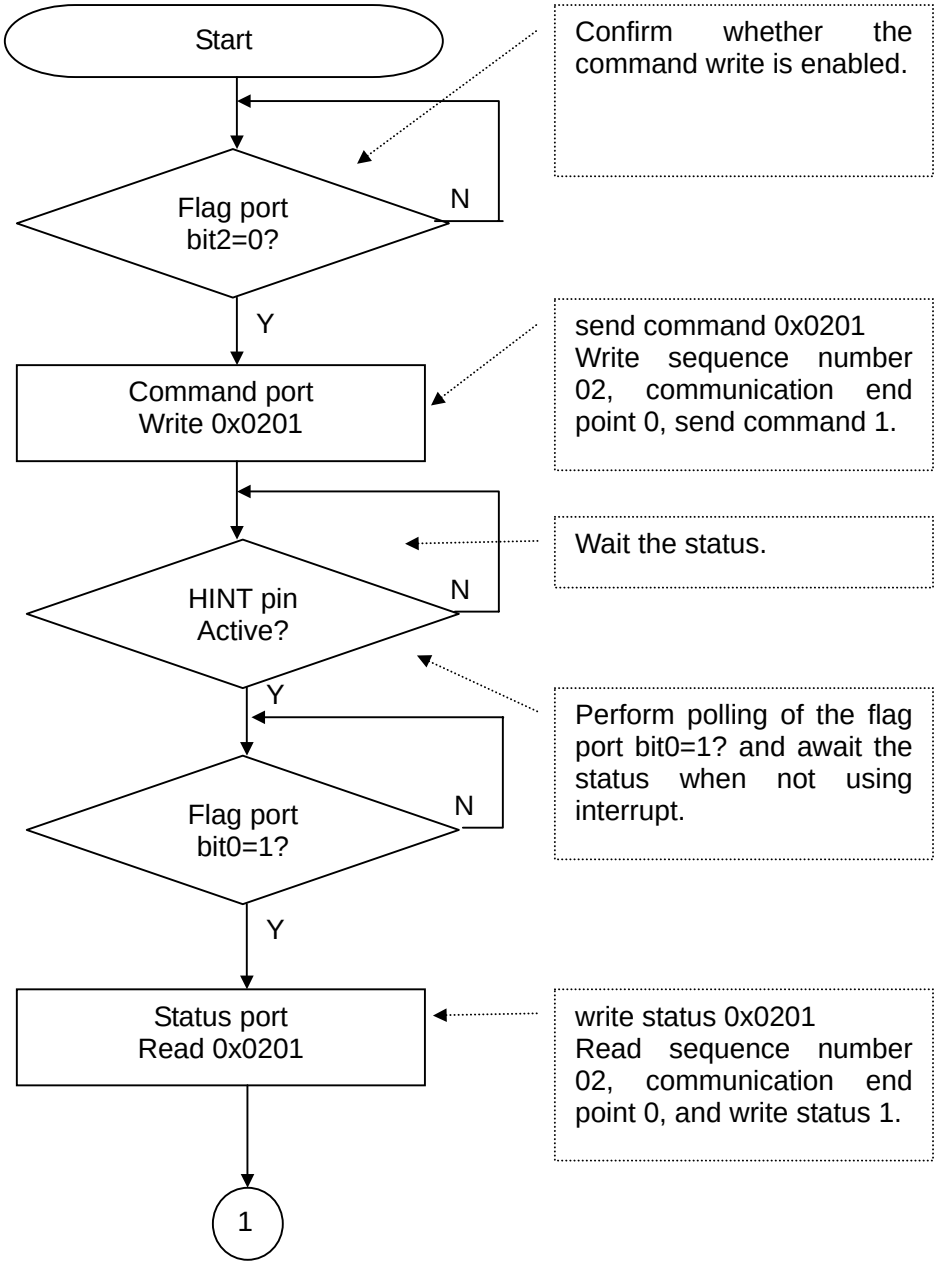


Fig.4.1 MAC address setting flow

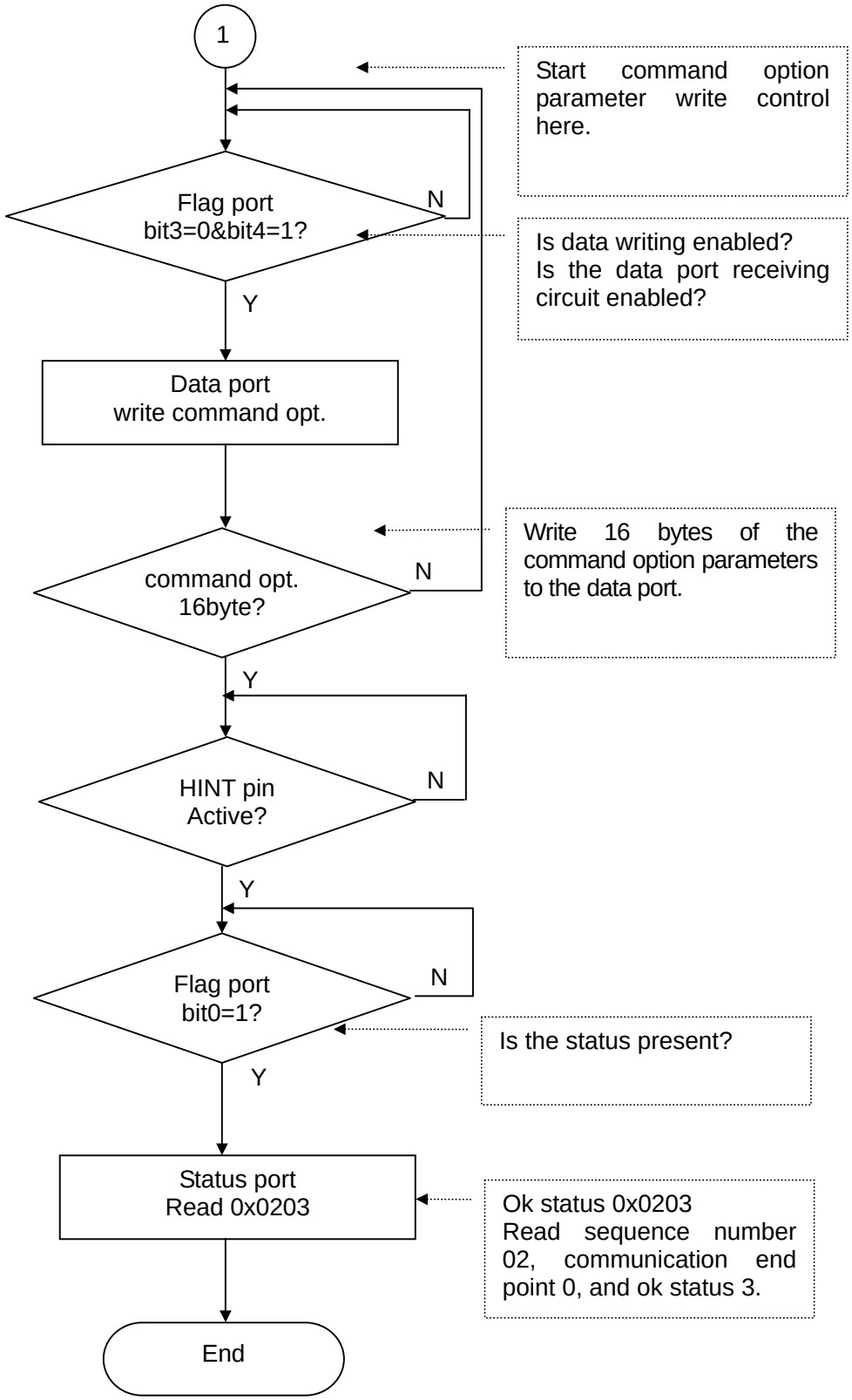


Fig.4.2 MAC address setting flow

* The above flow is an example of setting the MAC address (0 to 15 bits) in the internal register of the offset address 01h.
Then, setting in the internal registers of the offset address 02h and 03 in the same manner is required.

5. IP ADDRESS SETTING AND PING REPLY

To set an IP address in S1S60000, it is necessary to open the SYSTEM communication end point (communication end point 0). Opening the SYSTEM communication end point enables S1S60000 to reply to pings. At the SYSTEM communication end point, write the open command, read the write status, write the command option parameters, and read the ok status sequentially. This is the same procedure as that for the send command when setting the MAC address.
This chapter describes how to open the SYSTEM communication end point by specifying an IP address by the host CPU, and how to set an IP address from the DHCP server.
These are exclusive methods. If you perform one method and then perform the other method, reset S1S60000 once before starting the latter.

5.1 Specifying an IP address to open the SYSTEM communication end point

This section describes how to open the SYSTEM communication end point at the IP address 192.168.0.2, subnet mask 255.255.255.0, and gateway 192.168.0.1 of S1S60000.
Write the "open" command (0x0500: sequence number 05, communication end point number 0=SYSTEM, command number 0=open) to the command port. The sequence number has been used to 4 for setting the MAC address, use number 5 in increment by 1. S1S60000 returns the write status 0x0501.
For information on the "open" command, refer to the "S1S60000 Series Host Interface Manual - 3.1 open command".

Write the option parameters of the "open" command. Write the following data row to the data port.

Table 5.1 open command option parameters

BYTE	Write data	Contents	Comment
0	0x00	Fixed value	
1	0x00		
2	0x70	Flag	Bit7 (DATALINK layer is used)=0, Bit6 (local IP address is enabled)=1, Bit5 (subnet mask is enabled)=1, Bit4 (default gateway is enabled)=1, Bit0 (SOPAR is not used)=0
3	0x00	Fixed value	
4	0xc0	Local IP address	192.168.0.2 (0xc0.0xa8.0x00.0x02)
5	0xa8		
6	0x00		
7	0x02		
8	0xff	Subnet mask	255.255.255.0 (0xff.0xff.0xff.0x00)
9	0xff		
10	0xff		
11	0x00		
12	0xc0	Default gateway	192.168.0.1 (0xc0.0xa8.0x00.0x01)
13	0xa8		
14	0x00		
15	0x01		

When the option parameters are stored in the memory, BYTE0 in Table 5.1 is set to the low-order address of the memory.
Write data row for each host CPU type are as follows.

Table 5.2 Data row for each host CPU type

Host CPU type	Data row
8-bit connection LittleEndian	0x00,0x00,0x70,0x00,0xc0,0xa8,0x00,0x02,0xff,0xff,0xff,0x00,0xc0,0xa8,0x00,0x01
8-bit connection BigEndian	0x00,0x00,0x70,0x00,0xc0,0xa8,0x00,0x02,0xff,0xff,0xff,0x00,0xc0,0xa8,0x00,0x01
16-bit connection LittleEndian	0x0000,0x0070,0xa8c0,0x0200,0xffff,0x00ff,0xa8c0,0x0100
16-bit connection BigEndian	0x0000,0x0700,0xc0a8,0x0002,0xffff,0xff00,0xc0a8,0x0001

* Access sequence in the case of 8-bit connection: low-order port → high-order port

S1S60000 returns the “ok” status (0x0503). The flow of the “open” command at the SYSTEM communication end point is the same as the “send” command described in “MAC Address Setting”.

S1S60000 has been enabled to reply to pings. When the PC issues ping (ICMP ECHO request), S1S60000 replies to pings (ICMP ECHO reply). To confirm whether S1S60000 correctly replies to pings, use the command prompt of Windows. Start the Windows command prompt and input the following command to the IP address of S1S60000.
Note: The IP address of S1S60000 has been set at 192.168.0.2; set the IP address of PC to 192.168.0.xxx.

ping<space>192.168.0.2<enter>

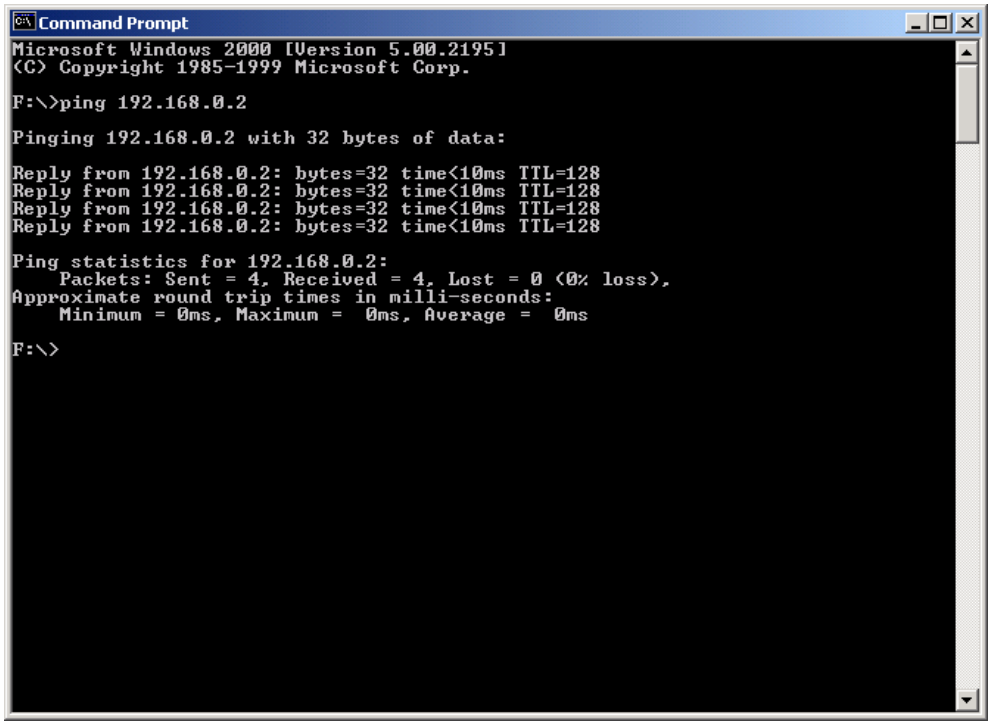


Fig.5.1 Transmission of pings from the PC to S1S60000 and reply to pings

5.2 Setting an IP address by the DHCP server to open the SYSTEM communication end point

This section describes how to open the SYSTEM communication end point by making setting so that the IP address of S1S60000 can be received from the DHCP server. Prepare a PC with the DHCP server function or broadband router with the DHCP function.
Write the send "open" (0x0500: sequence number 05, communication end point number 0=SYSTEM, command number 0=open) to the command port. The sequence number has been used for to 4 setting the MAC address; using the number 5 in increment by 1. S1S60000 returns the "write" status (0x0501).
Next, write the "open" command options. Write the following data row to the data port.

Table 5.3 open command option parameters

BYTE	Write data	Contents	Comment
0	0x00	Fixed value	
1	0x00		
2	0x00	Flag	Bit7 (DATALINK layer is used)=0, Bit6 (local IP address is enabled)=0 When the setting is made as above, setting of IP address, subnet mask, and default gateway is tried using the DHCP.
3	0x00	Fixed value	
4	0x00	Local IP address	Set by the DHCP server. No specification required.
5	0x00		
6	0x00		
7	0x00		
8	0x00	Subnet mask	
9	0x00		
10	0x00		
11	0x00		
12	0x00	Default gateway	
13	0x00		
14	0x00		
15	0x00		

S1S60000 returns the "ok" status (0x0503).

The processing to open the SYSTEM communication end point using the DHCP is complete. The DHCP server automatically sets an IP address after S1S60000 issues the ok status, and therefore the IP address has not yet been set at this point (when the "ok" status is returned to the host CPU). When the IP address is enabled by the DHCP, S1S60000 issues the "event" status (0x000a: sequence number 00, communication end point number 0=SYSTEM, status number 10=event). It is not the status corresponding to the command of the host CPU, and therefore, its sequence number becomes 0.

The “event” status is provided with 16-byte option parameters. Read the 16-byte option parameters to determine which “event” has occurred. In this case, the contents of “IP address is enabled” can be read. Reading the status and option parameters here is performed in the same process as reading the cable connection event described in “3. CONFIRMATION OF S1S60000 STATUS”.
When the IP address is enabled by the DHCP, the following data row can be read. The difference from the cable connection event is Detail of event of BYTE 4 and 5 (the shadow area of the table).

Table 5.4 Event status option parameters

BYTE	Read data	Contents	Comment
0	0x00	Fixed value	
1	0x00		
2	0x00	Flag	Reserved (0)
3	0x00	Fixed value	
4	0x01	Event type	1: IP address
5	0x04	Detail of event	4: IP address is enabled
6	0x00		In the case of IP address event, 0 for all
7	0x00		
8	0x00		
9	0x00		
10	0x00		
11	0x00		
12	0x00		
13	0x00		
14	0x00		
15	0x00		

When the option parameters are stored in the memory, BYTE0 in Table 5.4 is set to the low-order address of the memory.
Read data row for each host CPU type are as follows.

Table 5.5 Data row for each host CPU type

Host CPU type	Data row
8-bit connection LittleEndian	0x00,0x00,0x00,0x00,0x01,0x04,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00
8-bit connection BigEndian	0x00,0x00,0x00,0x00,0x01,0x04,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00
16-bit connection LittleEndian	0x0000,0x0000,0x0401,0x0000,0x0000,0x0000,0x0000,0x0000
16-bit connection BigEndian	0x0000,0x0000,0x0104,0x0000,0x0000,0x0000,0x0000,0x0000

* Access sequence in the case of 8-bit connection: low-order port → high-order port

Now, the IP address of S1S60000 is enabled. To allow S1S60000 to reply to pings from the PC, it is necessary to obtain to what value the IP address has been set. To obtain the IP address, subnet mask, and default gateway set by the DHCP, follow the procedure on the next page.

5.3 Confirming the IP address

Write the “status” command (0x0607: sequence number 06, communication end point number 0=SYSTEM, command number 7=status) to the command port. The sequence number has been used to 5 when opening the SYSTEM communication end point, and therefore use the one larger number 6.
S1S60000 returns the “read” status (0x0602: sequence number 06, communication end point number 0=SYSTEM, status number 2=read).
The “read” status is provided with 16-byte option parameters. Read the 16-byte option parameters to confirm the IP address, subnet mask, and default gateway set by the DHCP.
Reading the “read” status and option parameters is performed in the same process as reading the cable connection event described in “3. CONFIRMATION OF S1S60000 STATUS”.
When the IP address 192.168.0.03, subnet mask 255.255.255.0, and default gateway 192.168.0.1 are set by the DHCP, the following data row can be read.

Table 5.6 read status option parameters

BYTE	Read data	Contents	Comment
0	0x00	Fixed value	
1	0x00		
2	0x70	Flag	Bit7 (DATALINK layer is used)=0, Bit6 (local IP address is enabled)=1, Bit5 (subnet mask is enabled)=1, Bit4 (default gateway is enabled)=1, Bit0 (cable connection is completed)=0
3	0x00	Fixed value	
4	0xc0	Local IP address	192.168.0.3 (0xc0.0xa8.0x00.0x03)
5	0xa8		
6	0x00		
7	0x03		
8	0xff	Subnet mask	255.255.255.0 (0xff.0xff.0xff.0x00)
9	0xff		
10	0xff		
11	0x00		
12	0xc0	Default gateway	192.168.0.1 (0xc0.0xa8.0x00.0x01)
13	0xa8		
14	0x00		
15	0x01		

When the option parameters are stored in the memory, BYTE0 in Table 5.6 is set to the low-order address of the memory.

Read data row for each host CPU type are as follows.

Table 5.7 Data row for each host CPU type

Host CPU type	Data row
8-bit connection LittleEndian	0x00,0x00,0x70,0x00,0xc0,0xa8,0x00,0x03,0xff,0xff,0xff,0x00,0xc0,0xa8,0x00,0x01
8-bit connection BigEndian	0x00,0x00,0x70,0x00,0xc0,0xa8,0x00,0x03,0xff,0xff,0xff,0x00,0xc0,0xa8,0x00,0x01
16-bit connection LittleEndian	0x0000,0x0070,0xa8c0,0x0300,0xffff,0x00ff,0xa8c0,0x0100
16-bit connection BigEndian	0x0000,0x0700,0xc0a8,0x0003,0xffff,0xff00,0xc0a8,0x0001

* Access sequence in the case of 8-bit connection: low-order port → high-order port

In the same manner as “5.1 Specifying an IP address to open the SYSTEM communication end point”, pings are transmitted from the PC (ICMP ECHO request) and S1S60000 replies to pings (ICMP ECHO reply).

6. NOTES ON PROGRAMMING

This application note is designed as the first step guide for S1S60000. When creating a program for the host CPU to be incorporated in an actual product, carry out processing according to the received status.
For example, the procedure for transmitting data or processing the “send” command to write data onto a device is: write the “send” command, read the “write” status, write the option parameters, and read the “ok” status. S1S60000, however, performs the command processing asynchronously, and therefore a different status may be inserted in this procedure.
The status of the “send” command the host CPU expects is the “write” status. However, other statuses such as the “arrival” status can be read depending on circumstances. When data has been received through the network when the “send” command is written to send data, the “arrival” status can be read. The internal buffer is consumed if the received data is held in S1S60000; therefore, the host CPU needs to read the received data using the “receive” command.
In addition, the “busy” status can be read instead of the “write” status according to conditions. It is the insufficient internal buffer; for example, when the received data is not read using the “receive” command after the “arrival” status is read, or when data which must be transmitted after carrying out “send” command processing many times in a short interval, that is accumulated in the buffer of S1S60000.
The operation of the host CPU to S1S60000 and data received from the network are performed asynchronously. For this reason, we recommend that you create an event-type program based on the received status, instead of continuing to wait for the expected status.

EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
HEADQUARTERS
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-800-228-3964 FAX: +1-408-922-0238

SALES OFFICES

West
1960 E.Grand Avenue Flr 2
El Segundo, CA 90245, U.S.A.
Phone: +1-800-249-7730 FAX: +1-310-955-5400

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-800-853-3588 FAX: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 210
Wakefield, MA 01880, U.S.A.
Phone: +1-800-922-7667 FAX: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-332-0020 FAX: +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH
HEADQUARTERS
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

DÜSSELDORF BRANCH OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-2171-5045-0 FAX: +49-2171-5045-10

FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-1-64862350 FAX: +33-1-64862355

BARCELONA BRANCH OFFICE
Barcelona Design Center
Edificio Testa, C/Alcalde Barnils 64-68, Modulo C 2a planta
E-08190 Sant Cugat del Vallès, SPAIN
Phone: +34-93-544-2490 FAX: +34-93-544-2491

UK & IRELAND BRANCH OFFICE
8 The Square, Stockley Park, Uxbridge
Middx UB11 1FW, UNITED KINGDOM
Phone: +44-1295-750-216/+44-1342-824451
FAX: +44-89-14005 446/447

Scotland Design Center
Integration House, The Alba Campus
Livingston West Lothian, EH54 7EG, SCOTLAND
Phone: +44-1506-605040 FAX: +44-1506-605041

ASIA

EPSON (CHINA) CO., LTD.
23F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON Electronic Technology Development (Shenzhen) LTD.
12/F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110
Phone: +886-2-8786-6688 FAX: +886-2-8786-6677

HSINCHU OFFICE
No. 99, Jiangong Road,
Hsinchu City 300
Phone: +886-3-573-9900 FAX: +886-3-573-9169

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

GUMI OFFICE
2F, Grand B/D, 457-4 Songjeong-dong,
Gumi-City, KOREA
Phone: +82-54-454-6027 FAX: +82-54-454-6093

SEIKO EPSON CORPORATION
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC Marketing Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

Document Code: 410503000
First Issue January 2006
Printed in JAPAN (H)