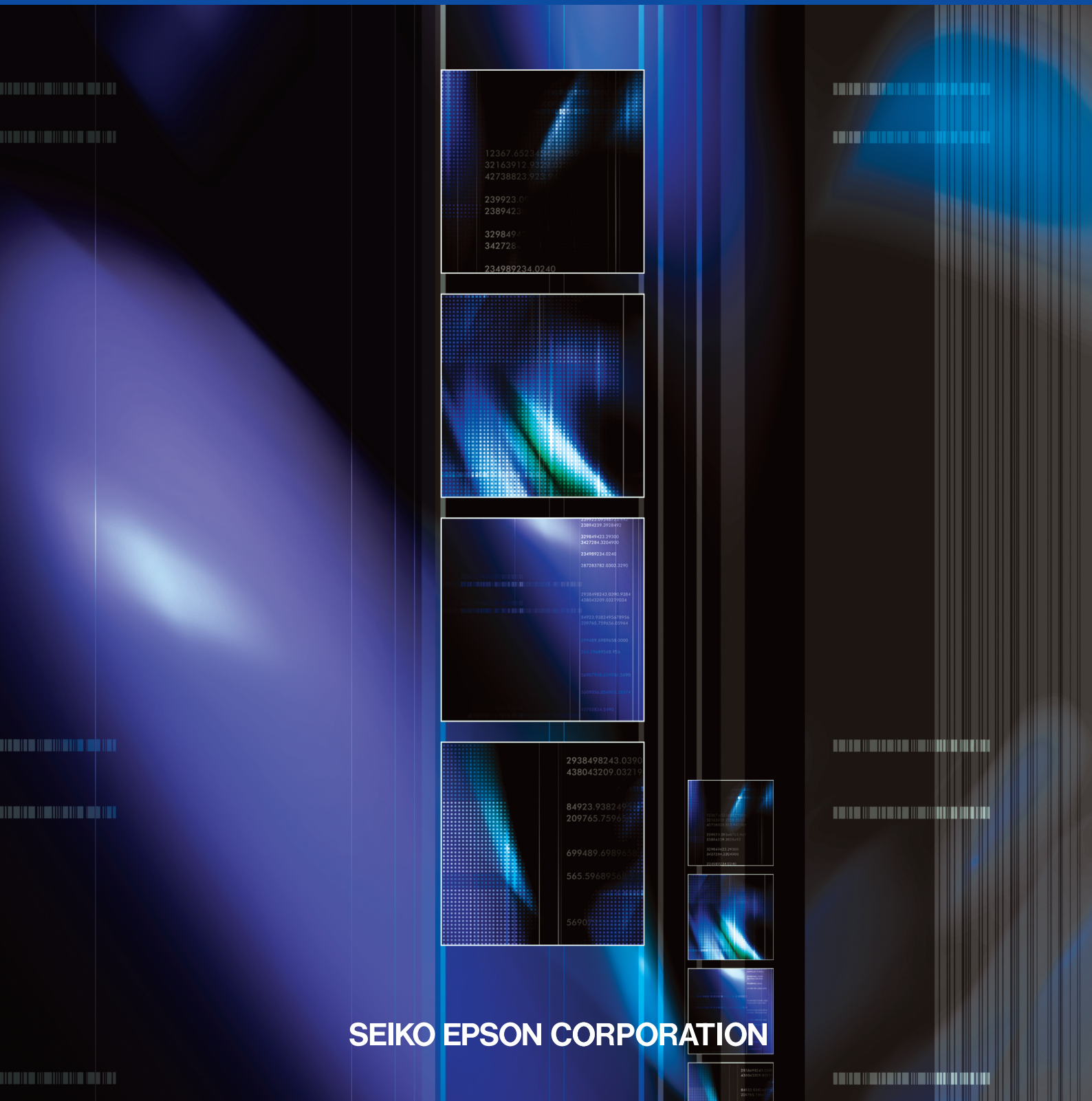
EPSON

ASICs

Gate Arrays / Embedded Arrays / Standard Cells

2025



SEIKO EPSON CORPORATION

Business Concept

The widespread of smartphones and tablets make improvements of broadband and wireless communications, then the advanced information and telecommunications network society has become a reality. In particular, semiconductors for use in portable devices, information terminals, in-vehicle devices and FA devices are expected to provide higher performance in terms of thinner structure, lighter weight, and longer operation with limited power supply. We have been focusing on the creation of compact, low-power semiconductors since we started the development of CMOS LSI for watches in 1969. Since then, we have steadily built up our expertise in energy-saving, space-saving, and time-saving designs. This has enabled us to quickly obtain the semiconductor development technology needed to meet the demands of the new era of the advanced information and telecommunications network society. Our concept is to develop "saving technologies" to reduce power consumption, development times, and implementation space. Our goal is to be a true partner for you, providing you with strategic advantages, enhancing your customer value based on our "saving technologies" and mixed analog/digital technologies that we have cultivated, as well as our design capabilities, manufacturing capabilities and stable supply that can satisfy your detailed requirements.

Environmental Responsibility

Epson semiconductor technology provides environmental value to customers by creating and manufacturing eco-friendly products.

1) We Epson's products are surely complying with the Eu-RoHS (2011/65/EU) Directive.
2) We are releasing information about the containing chemical substances of products at web-site.
   Product of QFP & BGA are described in the following URL.
   global.epson.com/products_and_drivers/semicon/information/package_lineup.html *Some products are excluded.

Environmental management system third party certification status
ISO14001

Type of certification : ISO 14001: 2015, JIS Q 14001: 2015
Awarded to : TOHOKU EPSON CORPORATION,
SEIKO EPSON CORPORATION (Fujimi Plant, Suwa Minami Plant)
Certified by : Bureau Veritas Certification
Date of certification : April 3, 1999

Type of certification : ISO 14001: 2015
Awarded to : Singapore Epson Industrial Pte. Ltd.
Certified by : SGS
Date of certification : Jan 12, 1999

Epson's Quality Policy

Keeping the customer in mind at all times, we make the quality of our products and services our highest priority. In oder to continue to creating products and services that please our customers and earn their trust. Epson's Semiconductor Business has acquired ISO9001 and IATF16949 certification with its IC, module and their application products.

Quality Management system third party certification status
ISO9001

Type of Certification : ISO9001: 2015 , JIS Q 9001: 2015
Awarded to : TOHOKU EPSON CORPORATION,
SEIKO EPSON CORPORATION (Fujimi Plant, Suwa Minami Plant, Tokyo Office, Hirooka Office)
Certified by : Bureau Veritas Certification
Initial Date of Certification : October 10, 1993

Type of Certification : ISO9001: 2015
Awarded to : Singapore Epson Industrial Pte. Ltd.
Certified by : SGS
Initial Date of Certification : February 4, 2003

IATF16949

Type of Certification : IATF16949:2016
Awarded to : TOHOKU EPSON CORPORATION, SEIKO EPSON CORPORATION
(Fujimi Plant, Tokyo Office, Hirooka Office)
Epson Europe Electronics GmbH, Epson America Inc.,
Epson Canada Ltd. (Vancouver Design Center),
Epson (China) Co., Ltd., Epson Hong Kong Ltd.
Certified by : Bureau Veritas Certification
Initial Date of Certification : Dec 9, 2017

Type of Certification : IATF16949:2016
Awarded to : Singapore Epson Industrial Pte. Ltd.
Certified by : SGS
Initial Date of Certification : May 2, 2018

ASICs

Product number explanation

●Device

S1L60173F00A000

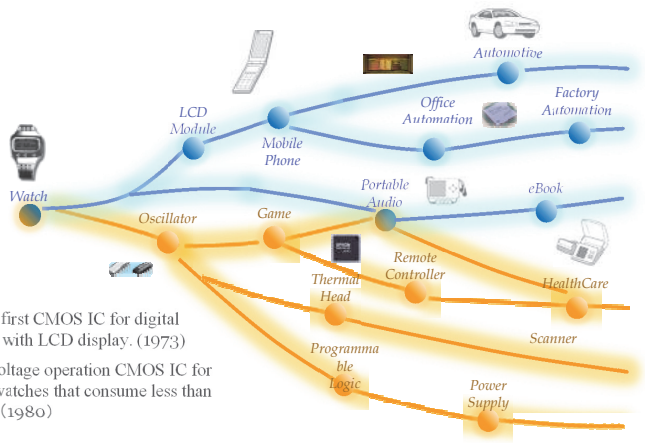
- **Packing specification**
- **Specifications**
- **Shape**
  (B : BGA, WCSP, F : PlasticQFP)
- **Model number**
- **Model name**
  (K : Stadard Cells, L : Gate Arrays, X : Embedded Arrays)
- **Product classification**
  (S1/S2/S7 : Semiconductor)

C O N T E N T S

History of Epson semiconductor

History of Epson Semiconductor's Technology

As the semiconductor division of "worldwide watch maker Seiko", semiconductor business has expanded into LCD Drivers, ASICs and MCUs from IC for Watches. These businesses are all based on Epson's energy-saving technology.

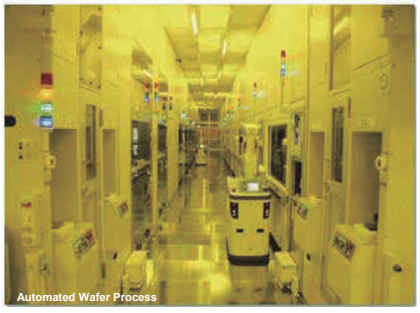


- World first CMOS IC for digital watches with LCD display. (1973)
- Low voltage operation CMOS IC for analog watches that consume less than 200nA. (1980)

LCD Driver
LCD Controller
ASSP
Microcontroller
ASIC (G/A, E/A, S/C)
Custom IC (Analog)
Silicon Foundry

Energy-Saving Technology ; Technology that reduces power consumption from both sides of process and circuit have been nurtured by Epson over 40 years since division was founded.

Epson Semiconductor's History



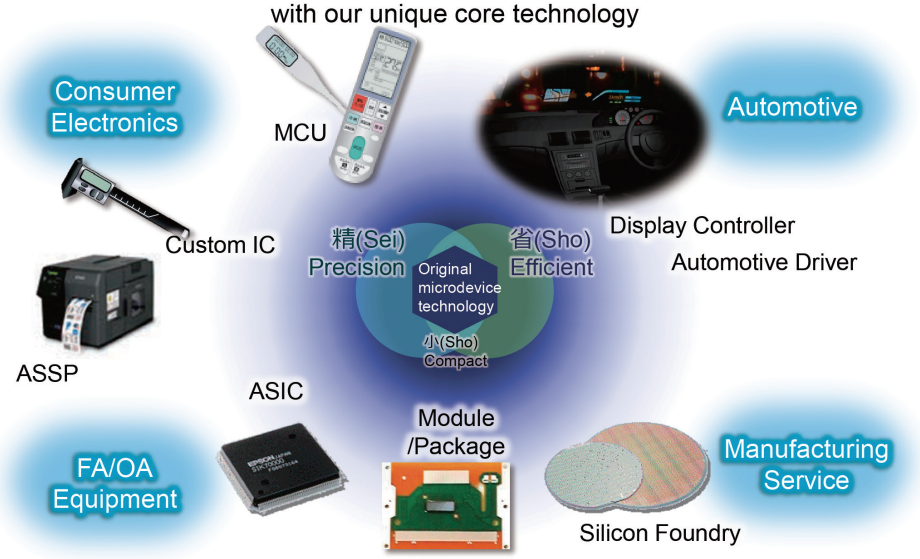
1969	Development of CMOS IC for watches started
1973	CMOS IC production started in Headquarter
1980	Fujimi plant (B-wing, 4 inch) operation started
1984	A-wing (5 inch) operation started
1985	D-wing (6 inch) operation started

1991	Sakata plant (S-wing,6 inch) operation started
1993	ISO9000 series certified
1994	Singapore assembly plant (SEP) operation started
1997	T-wing (8 inch, Sakata) operation started
	ISO14001 certified
2001	T-wing manufacturing line expanded
2006	ISO/TS16949 certified
2010	Microdevices Operations Division started
2017	IATF16949 certified

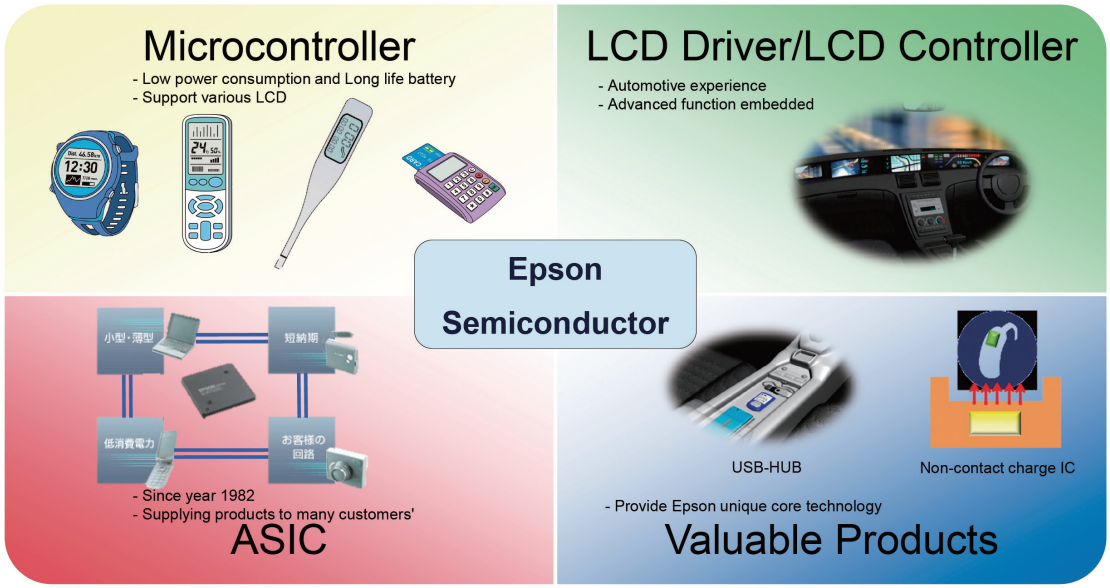
History of Epson semiconductor

Vision and Target Application

Epson aspires to be a device maker that contributes customers' business by valuable products with our unique core technology



Epson Product Line-up



ASIC Product Lineup

Epson's ASIC offerings aim to provide the best overall solution thus enabling our customers to get products to market successfully. Epson ASIC products include gate arrays that address the need for fast turnaround, at low IC development costs; Standard Cells, that make system solutions possible at the lowest unit price, and embedded arrays that combine the fast turnaround time of gate arrays with the ability to implement system level functionality on chips available with standard cells.

- Abundant supporting achievements ever since 1982
- Entire operation of design and manufacture in our own factory
- ISO9001 & IATF16949 certificated

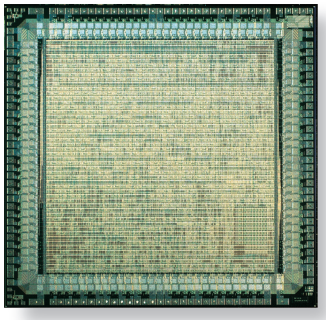
Epson ASIC

Gate Arrays

S1L60000	0.25µm	Core 1.8V, 2.0V, 2.5V 3.3V interface
S1L50000	0.35µm	Core 2.0V, 2.5V, 3.3V 5V interface
S1L5V000	0.35µm	Core 3.3V, 5.0V 5V single power supply

The gate array is a member of the ASIC family that offers quick turnaround time during the development cycle at the lowest development cost. This is achieved by Epson stocking pre-fabricating Base/Bulk wafers that have transistors arranged in the form of an array. Our customers design the "wiring", that connects the transistors, that bring specific functionality to the design of the ASICs.

Base arrays are prefabricated with different numbers of transistors giving customers a wide range of choices to implement their circuits. This offers flexibility to customers by giving them the choice of adding or subtracting functionality from the design.



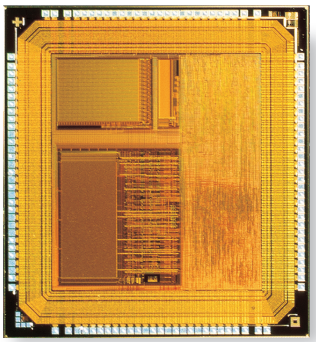
ASIC Product Lineup

Embedded Arrays

S1X80000	0.15µm	Core 1.8V 3.3V single power supply with LDO
S1X60000	0.25µm	Core 1.8V, 2.0V, 2.5V 5V interface
S1X50000	0.35µm	Core 2.0V, 2.5V, 3.3V 5V interface
S1X5V000	0.35µm	Core 3.3V, 5.0V 5V single power supply

The embedded array combines the fast turnaround time of gate arrays with the ability to implement system level functionality available in standard cells. The fast turnaround is accomplished by starting some of the wafer fabrication processes in parallel with the embedded array design process. In selecting an embedded array approach, the designer trades off the ability to change the base array in the last minute, possible with a gate array, with the need to implement system level functionality, with gate array like turnaround.

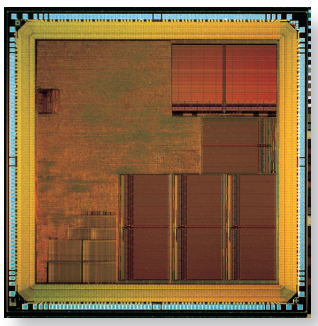
By offering gate arrays, standard cells, and embedded arrays; Epson offers a choice to meet the individual needs of our customers.



Standard Cells

S1K80000	0.15µm	Core 1.8V 3.3V single power supply with LDO

Standard cells (cell-based ASICs) are semi-custom ICs that enable optimally designed internal logic cells, memories such as ROM and RAM, CPU, and analog circuits to be implemented all on the same chip. As such, standard cells enable more design flexibility than gate arrays, offer more advanced functionality and higher integration, and can be developed as system LSI optimized for the customer's needs. Such optimization enables the achieving of ever more advanced functionality and lower power consumption.



ASICs Gate Arrays

Epson's Gate Array is a suitable solution for replacing existing devices because this Gate Array option gives flexibility to adapt the power supply and layouts of other various signals. Furthermore Epson has invested on the new Gate Array series called "S1L5V000" which supports 5V single power supply with 0.35µm process. Since it is a new series, it is also suitable for long life time applications.

S1L50000 Series

Core	I/O
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V
3.3V	3.3V
	5.0V

Series		S1L50000 Series													
Features		• Ultra large scale integration (0.35µm CMOS, using 2-, 3- or 4-layer interconnect process) • High-speed operation (0.14ns delay at 3.3V, with 2-input power NAND Typ.) • Low power consumption (Internal cell: 0.7µW/MHz/gate at 3.3V) • Drivability (I_{OL} = 0.1, 1, 3, 8, 12, 24mA, PCI at 5.0 V, I_{OL} = 0.1, 1, 2, 6, 12mA, PCI at 3.3V, I_{OL} = 0.1, 0.5, 1, 3, 6mA at 2.5V, I_{OL} = 0.05, 0.3, 0.6, 2, 4mA at 2.0V)													
Model	Double layer	S1L50062	S1L50122	S1L50282	S1L50552	S1L50752	S1L50992	S1L51252	S1L51772	S1L52502	S1L53352	S1L54422	S1L55062	S1L56682	S1L58152
	Triple layer	S1L50063	S1L50123	S1L50283	S1L50553	S1L50753	S1L50993	S1L51253	S1L51773	S1L52503	S1L53353	S1L54423	S1L55063	S1L56683	S1L58153
	Quadruple layer	S1L50064	S1L50124	S1L50284	S1L50554	S1L50754	S1L50994	S1L51254	S1L51774	S1L52504	S1L53354	S1L54424	S1L55064	S1L56684	S1L58154
Total BC (Row gates)		5.8k	12.0k	28.8k	55.5k	75.8k	99.2k	125.8k	177.1k	250.2k	335.9k	442.2k	506.7k	668.6k	815.5k
Usable gates	Double layer	2.9k	6.0k	14.4k	26.1k	35.7k	46.7k	56.6k	79.7k	112.6k	144.5k	176.9k	202.7k	267.5k	326.2k
	Triple layer	5.1k	10.6k	25.3k	47.2k	64.4k	84.4k	100.7k	132.8k	187.7k	251.9k	309.5k	354.7k	468.0k	570.9k
	Quadruple layer	5.5k	11.4k	27.3k	52.8k	72.0k	94.3k	119.5k	168.2k	237.7k	319.1k	397.9k	456.1k	601.7k	734.0k
Total Lead Count	80µm	–	56	88	124	144	168	188	224	264	308	352	376	432	480
	70µm	48	64	104	144	168	192	216	–	–	–	–	–	–	–
Delay Time	Internal gates	t_{pd} = 0.14ns (3.3V, F/O 2, typical wire load), 0.21ns (2.0V, F/O 2, typical wire load)													
	Input buffer	t_{pd} = 0.38ns (5.0V, F/O 2, typical wire load) Level shifter: 0.4ns (3.3V, F/O 2, typical wire load), 1.3ns (2.0V, F/O 2, typical wire load)													
	Output buffer	t_{pd} = 2.12ns (5.0V) Level shifter: 2.02ns (3.3V), 3.9ns (2.0V) CL = 15pF													
I/O level		CMOS, LVTTL, PCI-5V, PCI-3.3V													
Input modes		LVTTL, CMOS, Pull-up/Pull-down, Schmitt, Fail-safe, Gated													
Output m odes		Normal, Open drain, 3-state, Bidirectional, Fail-safe, Gated													

Note: Figures shown for usable gates are approximations. The actual number of usable gates varies according to the implemented circuitry.

S1L5V000 Series

Core	I/O
5.0V	5.0V
3.3V	3.3V

Series		S1L5V000 series							
Features		• Large scale integration (0.35µm CMOS, using 2-, 3-, 4-layer interconnect process) • High speed operation (internal gate delay: 0.19ns at 5V, 0.29ns at 3.3V, 2-input power NAND Typ.) • Low power consumption (Internal cell: 5V 1.3µW/MHz/BC, 3.3V 0.54µW/MHz/BC) • Drive capacity (I_{OL} = 0.1, 1, 3, 8, 12mA at 5.0V, I_{OL} = 0.1, 1, 2, 6, 10mA at 3.3V)							
Model	Double layer	S1L5V012	S1L5V042	–	S1L5V112	–	S1L5V252	–	S1L5V482
	Triple layer	S1L5V013	S1L5V043	S1X5V513*	S1L5V113	S1X5V523*	S1L5V253	S1X5V533*	S1L5V483
	Quadruple layer	S1L5V014	S1L5V044	S1X5V514*	S1L5V114	S1X5V524*	S1L5V254	S1X5V534*	S1L5V484
Total BC (Row gates)		8.8k	42.0k	26.0k	109.2k	90.3k	254.3k	235.0k	479.9k
Usable gates	Double layer	2.6k	12.6k	–	32.7k	–	63.5k	–	119.9k
	Triple layer	5.3k	25.2k	14.3k	65.5k	49.7k	139.8k	129.3k	239.9k
	Quadruple layer	6.1k	29.4k	16.9k	76.4k	58.7k	165.3k	152.8k	287.9k
Total Lead Count		48	104		168		256		308
Delay Time	Internal Gates	t_{pd} = 0.19ns (5.0V operation, F/O 2, typical wiring load), t_{pd} = 0.29ns (3.3V operation, F/O 2, typical wiring load)							
	Input Buffer	t_{pd} = 0.45 ns (5.0V operation, F/O 2, typical wiring load), t_{pd} = 0.55ns (3.3V operation, F/O 2, typical wiring load)							
	Output Buffer	t_{pd} = 2.07ns (5.0V operation, CL = 15pF), t_{pd} = 2.95ns (3.3V operation, CL = 15pF)							
I/O level		CMOS, TTL, LVTTL							
Input modes		TTL, LVTTL, CMOS, Pull-up/Pull-down, Schmitt, Fail-safe, Gated							
Output m odes		Normal, Open-drain, 3-state, Bidirectional, Fail safe, Gated							

Note: Figures shown for usable gates are approximations. The actual number of usable gates varies according to the implemented circuitry.

*: Analog PLL built in master

S1L60000 Series

Core	I/O
1.8V	1.8V
	3.3V
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V

Series		S1L60000 Series									
Features		• Ultra large scale integration (0.25µm CMOS, using 3-, 4-layer interconnect process) • High-speed operation (107ps internal gate delay at 2.5V, with 2-input NAND Typ.) • Low power consumption (Internal cell: 0.18µW/MHz/gate at 2.5V, with 2-input NAND Typ.) • Drivability (I_{OL} = 0.1, 1, 3, 6, 12, 24mA at 3.3V, I_{OL} = 0.1, 1, 3, 6, 9,18mA at 2.5V, I_{OL} = 0.05, 0.3, 1, 2, 3, 6mA at 2.0V, I_{OL} = 0.045, 0.27, 0.9, 1.8, 2.7, 5.4mA at 1.8V)									
Model	Triple layer	S1L60093	S1L60173	S1L60283	S1L60403	S1L60593	S1L60833	S1L61233	S1L61583	S1L61903	S1L62513
	Quadruple layer	S1L60094	S1L60174	S1L60284	S1L60404	S1L60594	S1L60834	S1L61234	S1L61584	S1L61904	S1L62514
Total BC (Row gates)		99.2k	171.8k	284.4k	400.3k	595.4k	831.6k	1,234.9k	1,587.8k	1,903.0k	2,519.6k
Usable gates	Triple layer	59.6k	103.1k	142.2k	200.2k	297.7k	332.7k	494.0k	635.1k	761.2k	1,007.9k
	Quadruple layer	69.5k	120.2k	184.9k	260.2k	387.0k	415.8k	617.5k	793.9k	951.5k	1,259.8k
Total Lead Count	80µm	–	–	–	–	–	284	344	388	424	488
	70µm	112	148	188	224	272	–	–	–	–	–
Delay Time	Internal gates	t_{pd} = 107ps (2.5V, F/O 1, typical wire load)									
	Input buffer	t_{pd} = 270ps (2.5V, F/O 2, typical wire load)									
	Output buffer	t_{pd} = 1600ps (2.5V, CL = 15pF)									
I/O levels		CMOS, LVTTL, PCI-3.3V									
Input modes		CMOS, LVTTL, Pull-up/Pull-down, Schmitt, Level shifter, Fail-safe, Gated									
Output modes		Normal, Open drain, 3-state, Bidirectional, Level shifter, Fail-safe, Gated									

Note: Figures shown for usable gates are approximations. The actual number of usable gates varies according to the implemented circuitry.

S1L80000 Series (Under development)

Core	I/O
1.8V	3.3V
LDO	3.3V

Series		S1L80000 Series			
Features		• Based on 0.15µm CMOS process technology using 4-, 5-layer interconnect process • Internal gate delay: 34.5ps/1.8V, 2-input NAND Typ. • Low power consumption (Internal cell: 0.063µW/MHz/gate 2-input NAND Typ.) • Drive performance (I_{OL} = 2, 4, 8, 12mA at 3.3V)			
Model	4-layer metal	S1L80104	S1L80154	S1L80204	S1L80304
	5-layer metal	S1L80105	S1L80155	S1L80205	S1L80305
Usable gates	4-layer metal	120k	230k	315k	650k
	5-layer metal	135k	255k	350k	720k
Total Lead Count		100	180	256	280
LDO (Requires external capacitors)		1	–	–	–
PLL		1	2	2	2
LVDS IO		–	Tx 4 pairs/Rx 4 pairs	Tx 8 pairs/Rx 8 pairs	Tx 8 pairs/Rx 8 pairs
Dual Port SRAM (2R+2W)		–	–	256w x 16b x 4pcs	256w x 16b x 4pcs
Status		Under development	Under development	Under development	Under development

Note: Figures shown for usable gates are approximations. The actual number of usable gates varies according to the implemented circuitry.

Embedded Arrays

Creating hard macros for cells that are highly integrated and have advanced functionality enables development of system-on-a-chip designs, and utilization of the sea-of-gates structure in the logic means that the development period subsequent to the interconnection process is roughly equivalent to that for gate array chips.
In addition, the base array for LSI can be reused allowing only the logic block to be modified in development lead time equivalent to that for gate array chips.
Embedded array technology also facilitates circuit design changes and thereby helps avoid the risks associated with product modifications.

S1X5V000 Series

Series	S1X5V000 Series
Features	• High-density integration (0.35µm CMOS process technology and 2/3/4-layer interconnect process) • High-speed operation (Internal gate delay: 0.19ns ps/5.0 V, 0.29ns/3.3 V, 2-input power NAND Typ.) • Low power consumption (Internal cell: 1.3µW/MHz/gate, 5.0V, 0.54µW/MHz/gate, 3.3V, 2-input NAND Typ.) • Drivability (I_{OL} = 0.1, 1, 3, 8, 12 mA at 5.0 V, 0.1, 1, 2, 6, 10 mA at 3.3 V

Core	I/O
3.3V	3.3V
5.0V	5.0V

S1X50000 Series

Series	S1X50000 Series
Features	• High-density integration (0.35µm CMOS process technology and 3/4-layer interconnect process) • High-speed operation (Internal gate delay: 150 ps/3.3 V, 2-input power NAND Typ.) • Low power consumption (Internal cell: 0.37µW/MHz/gate, 3.3V, Typ.) • Drivability (I_{OL} = 0.1, 1, 3, 8, 12, 24mA at 5.0V, I_{OL}=0.1, 1, 2, 6, 12mA at 3.3V, I_{OL} = 0.1, 0.5, 1, 3, 6mA at 2.5V, I_{OL}=0.05, 0.3, 0.6, 2, 4mA at 2.0V)

Core	I/O
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V
3.3V	3.3V
	5.0V

S1X60000 Series

Series	S1X60000 Series
Features	• High-density integration (0.25µm CMOS process technology and 3/4/5-layer interconnect process, number of raw gates: 2,500,000 Max.) • High-speed operation (Internal gate delay: 107 ps/2.5 V, 2-input power NAND Typ.) • Low power consumption (Internal cell: 0.18µW/MHz/gate, 2.5V, Typ.) • Drivability (I_{OL} = 0.1, 1, 3, 6, 12, 24mA at 3.3V, I_{OL} = 0.1, 1, 3, 6, 12, 24mA at 2.5V, I_{OL} = 0.05, 0.3, 1, 2, 4, 8mA at 2.0V)

Core	I/O
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V

S1X80000 Series

Series	S1X80000 Series
Features	• Based on 0.15µm CMOS process technology using 4/5-layer interconnect process • Internal gate delay: 34.5ps/1.8V, 2-input NAND Typ. • Low power consumption (Internal cell: 0.063µW /MHz/gate 2-input NAND Typ.) • Drive performance (I_{OL} = 2, 4, 8, 12mA at 3.3V)

Core	I/O
1.8V	3.3V
1.8V	5.0V
LDO	3.3V

Standard Cells

Standard cells (cell-based ASICs) are semi-custom ICs that enable optimally designed internal logic cells, memories such as ROM and RAM, CPU peripherals, and analog circuits to be implemented all on the same chip. As such, standard cells enable more design flexibility than do gate arrays, offer more advanced functionality and higher integration, and can be developed as a system-on-a-chip optimized for the customer's needs.
Such optimization leads to ever more compact, power-conserving devices.

S1K80000 Series

Core	I/O
1.8V	3.3V
1.8V	5.0V
LDO	3.3V

Series	S1K80000 Series
Features	• Based on 0.15µm CMOS process technology using 4/5-layer interconnect process • Internal gate delay: 42.9ps/1.8V, 2-input NAND Typ. • Low power consumption (Internal cell: 0.039µW /MHz/gate 2-input NAND Typ.) • Drive performance (I_{OL} = 2, 4, 8, 12mA at 3.3V)

Macro Cells

1. PLL

Series	S1X5V000	S1X50000	
Macro Type	A35M	A35K	A35M
Operation Voltage	4.5 to 5.5V	3.0 to 3.6V	
Input Frequency	5MHz to 40MHz	32kHz	5MHz to 40MHz
Multiplication Ratio	x2 to x26	x610 to x4096	x2 to x26
Output Frequency	20MHz to 135MHz	20MHz to 135MHz	
Period Jitter	±3%	±3%	±2%
Output Duty	50%±10%	50%±10%	
Lock Up Time	100µs	100msec	100µs
Low Pass Filter	On chip	On chip	
Temperature Range	-40 to 110°C	-40 to 85°C	
Layer	3	3	

Series	S1X60000		S1X80000/S1K80000	
Macro Type	A25K	A25M	A15K	A15M
Operation Voltage	2.3 to 2.7V		1.65 to 1.95V	
Input Frequency	32kHz	5MHz to 150MHz	32kHz	5MHz to 150MHz
Multiplication Ratio	Max. 16000	x1 to x16	x571 to x6667	x1 to x16
Output Frequency	20MHz to 200MHz		20MHz to 200MHz	
Period Jitter	±2%	±200ps	POUT≤100MHz ±2% POUT>100MHz ±200ps	
Output Duty	50%±5%		50%±400ps	
Lock Up Time	100msec	100µs	100msec	200µs
Low Pass Filter	On chip		On chip	
Temperature Range	-40 to 85°C		-40 to 110°C	
Layer	3		4	

2. ROM

Series	S1X50000	S1X60000	S1X80000/S1K80000
Macro Type	Standard	Standard	Standard
Memory Size/Module	1k to 256K-bit	1k to 256K-bit	1k to 512K-bit
Data Bus Width	x1 to x64 1-bit step	x1 to x64 1-bit step	x1 to x64 1-bit step
Operate Voltage	2.0V, 2.5V, 3.0V, 3.3V	2.0V, 2.5V	1.8V
Operate Frequensy (Max.)	50MHz	66MHz	56MHz
Layer	3	3	3

3. SRAM

Series	S1X5V000	
Macro Type	Standard	
Port	1-port	2-port (1R+1W)
Memory Size/Module	128 to 16K-bit	
Data Bus Width (bit)	x1 to x32 1-bit step	
Operating Voltage	3.3V, 5.0V	
Operation Frequency (Max.)	50MHz/5.0V	
Layer	3	

Series	S1X50000					
Macro Type	Standard		High-Density	High Speed		
Port	1-port	Dual port (2R+2W)	1-port	1-port	2-port (1R+1W)	Dual port (2R+2W)
Memory Size/Module	128 to 64K-bit	1K to 64K-bit	32K to 512K-bit	32K to 72K-bit		
Data Bus Width (bit)	x1 to x32 1-bit step	x8, x16, x24, x32	x8, x16, x32	x1 to x144 1-bit step		
Write Option	Byte Write		–	Byte Write		
Operating Voltage	2.0V, 2.5V, 3.0V, 3.3V		2.0V, 3.0V, 3.3V	3.3V		
Operation Frequency (Max.)	71MHz		76MHz	125MHz	110MHz	
Layer	3		3	3		

Series	S1X60000				
Macro Type	Standard		High-Density	High Speed	
Port	1-port	Dual port (2R+2W)	1-port	1-port	2-port (1R+1W)
Memory Size/Module	128 to 64K-bit	1K to 64K-bit	32K to 512K-bit	128 to 64K-bit	
Data Bus Width (bit)	x1 to x32 1-bit step	x8, x16, x24, x32	x8, x16, x32	x4 to x64 1-bit step	
Write Option	Byte Write		Byte Write	Byte Write	
Operating Voltage	2.0V, 2.5V		2.0V, 2.5V	2.5V	
Operation Frequency (Max.)	125MHz	119MHz	71MHz	179MHz	
Layer	3		3	3	

Series	S1X80000/S1K80000			
Macro Type	Standard			Large Scale
Port	1-port	2-port (1R+1W)	Dual port (2R+2W)	1-port
Memory Size/Module	128 to 64K-bit	64 to 16K-bit	1K to 32K-bit	128K to 1M-bit
Data Bus Width (bit)	x1 to x32 1-bit step	x1 to x32 1-bit step	x8, x16, x24, x32	x8, x16, x32
Write Option	Byte Write	–	Byte Write	1-bit Write
Operating Voltage	1.8V			1.8V
Operation Frequency (Max.)	125MHz	119MHz	116MHz	74MHz
Layer	3	4	3	3

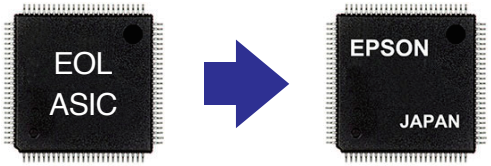
Ask our sales department regarding Gate Array SRAM.

Epson Originals

Epson Originals -1- Replacement of existing devices

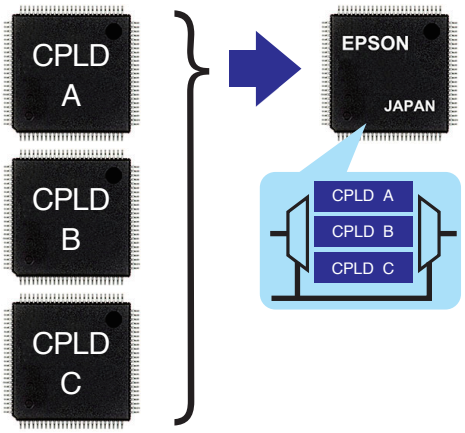
Discontinued devices

To keep power supply, pin-assignment, function compatible

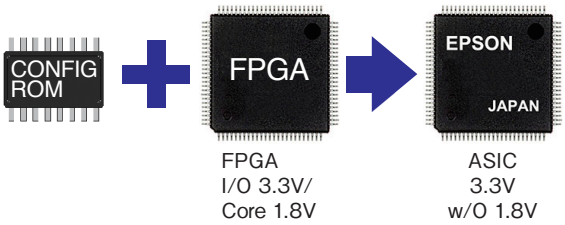


PLDs

Integration multiple PLDs into ASICs



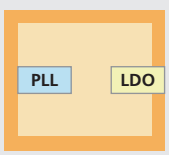
FPGA2ASIC



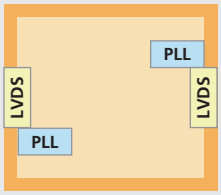
PLL built-in gate array

S1L80000 series under development

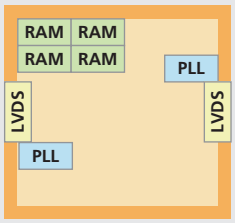
S1L8010	
Power supply	Pad counts
Core 1.8V I/O 3.3V	100
3.3V single power supply with LDO	
LDO requires external capacitors	



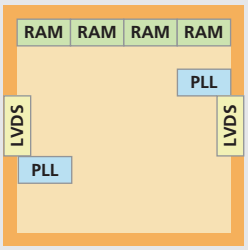
S1L8015	
Power supply	Pad counts
Core 1.8V I/O 3.3V	180



S1L8020	
Power supply	Pad counts
Core 1.8V I/O 3.3V	256



S1L8030	
Power supply	Pad counts
Core 1.8V I/O 3.3V	280



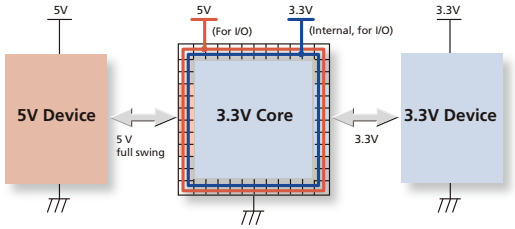
Epson Originals -2- Power System Interface

Development of low-voltage system power supplies continues as part of the trend toward reducing power consumption. However, in cases where not all system components can run on a single low-voltage power supply, multiple power supplies are used for the same system. Consequently, many of today's portable electronic devices include dual (5 V/3.3 V) power supplies, each with its own signals.

5 V/3.3 V Dual Power Supply System

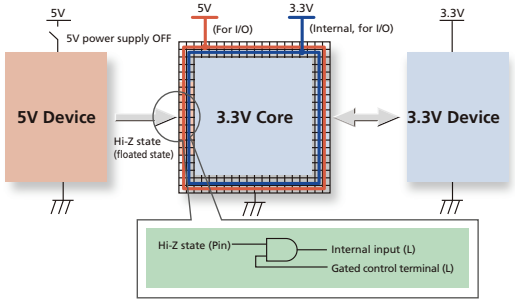
Level Shifter

Since it is often the case with ASICs that several ICs are connected in the same system, such systems are typically required to handle two types of level signals for 5 V and 3.3 V power. In S1L50000 and S1X50000 series products, the inclusion of two power supplies (such as 5 V and 3.3 V power supplies) enables the implementation of a bilevel (5 V, 3.3 V) signal interface for each I/O buffer. Such an interface is best suited for applications that include high-speed signal processing and high drive current capacity.



Gated I/O buffer

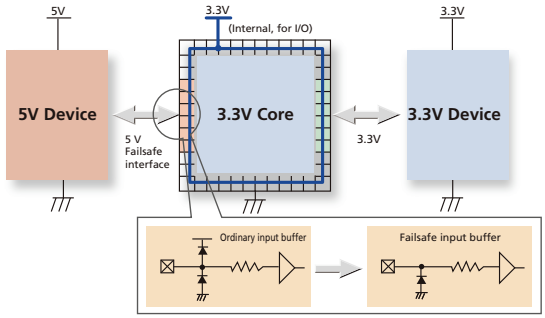
The use of the gated input buffer enables input in the Hi-Z state, which has not usually been possible using a buffer. In a system using dual-line power supply, the high-voltage power supply may be cut off. Using this function allows hot-plugging a PC card and achieving lower power consumption in the backup mode of PDA.



3.3 V Single Power Supply System

Failsafe I/O Buffer

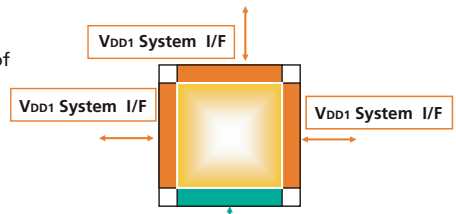
Even when system constraints preclude the implementation of a dual power supply system, it is still possible to provide an interface between a 3.3 V single power supply chip and a 5 V chip by implementing an input buffer that does not include a forward diode (in the V_{DD} direction), which also provides failsafe support for output.



Power separation suitable for low voltage power supply and low power consumption

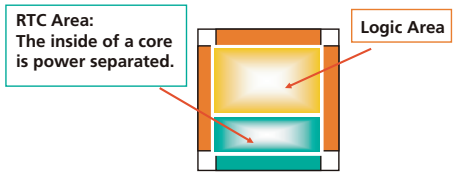
IO Power Separation

- Interface with the devices of other power systems can be possible by power separation of I/O cell area.



Core Power Separation

- When mounted with RTC, power separation between RTC area and Logic area can be possible.
  Power OFF can be possible in the non RTC area.



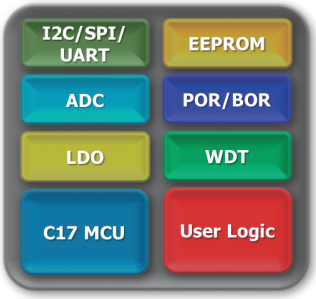
Epson Originals

Epson Originals -3- Macro examples for embedded use

Epson ASICs can utilize various macros from Epson ASSPs or MCUs.
Ask our sales department for details.

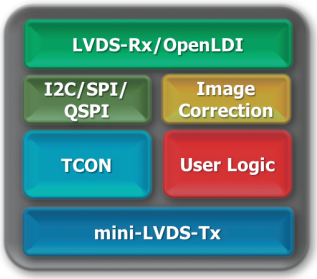
MCU Macro examples

LDO
POR/BOR
ADC
WDT
I²C/SPI/UART
EEPROM



Display controller Macro examples

LVDS-Rx
LVDS-Tx
OpenLDI-Rx
OpenLDI-Tx
mini-LVDS-Tx



Epson Originals -4- EMI countermeasures

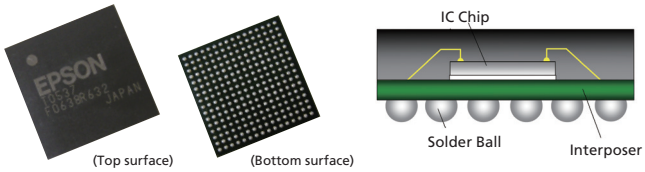
EMI countermeasures

Epson ASICs will take the following countermeasures to meet requests received from many customers to reduce EMI:

✓	Clock gating	✓	Power separation
✓	SS (Spread Spectrum)	✓	Optimization of drive capacity
✓	Multiphase delay clock	✓	Optimization of PIN arrangement
✓	Adoption of input Schmidt circuit	✓	Housing of bypass condenser
✓	Slew rate control	✓	Low noise F/F

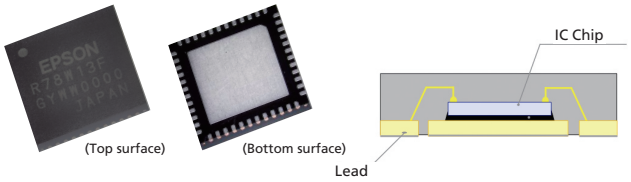
Package Lineup

Plastic Ball Grid Array (PBGA)



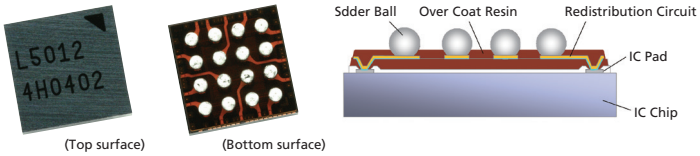
PKG Type (JEITA PKG Name)	Body Size (mm)	Ball Pitch (mm)
PBGA1UE256 (P-LBGA-0256-1717-1.00)	17 X 17 X 1.7	1.0

Quad Flat Non-leaded Package (QFN)



PKG Type (JEITA PKG Name)	Body Size (mm)	Lead Pitch (mm)
SQFN4-24 (P-VQFN024-0404-0.50)	4 X 4 X 1.0	0.5
SQFN5-32 (P-VQFN032-0505-0.50)	5 X 5 X 1.0	0.5
SQFN7-48 (P-VQFN048-0707-0.50)	7 X 7 X 1.0	0.5
SQFN9-64 (P-VQFN064-0909-0.50)	9 X 9 X 1.0	0.5

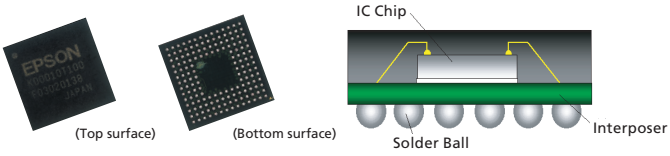
WL-CSP



PKG Type	Pin	Body Size (mm)	Ball Pitch (mm)
WL-CSP (S1L5012)	16	2.4 X 2.4 X 0.8	0.5
WL-CSP (S1L5028)	25	3.0 X 3.0 X 0.8	0.5
WL-CSP (S1L5075)	49	4.2 X 4.2 X 0.8	0.5
WL-CSP (S1L5125)	81	5.0 X 5.0 X 0.8	0.5
WL-CSP (S1L60093)	49	3.0 X 3.0 X 0.8	0.4

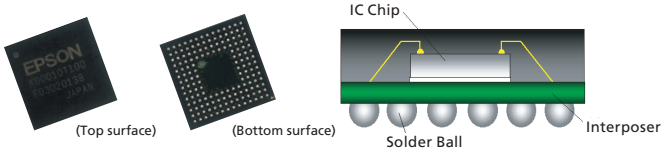
Package Lineup

Plastic Fine-pitch Ball Grid Array (PFBGA)



PKG Type (JEITA PKG Name	Body Size (mm)	Ball Pitch (mm)
PFBGA5U-60 (P-TFBGA-060-0505-0.50)	5 X 5 X 1.2	0.5
PFBGA6U-96 (P-TFBGA-096-0606-0.50)	6 X 6 X 1.2	0.5
PFBGA7U-144 (P-TFBGA-144-0707-0.50)	7 X 7 X 1.2	0.5
PFBGA8U-161 (P-TFBGA-161-0808-0.50)	8 X 8 X 1.2	0.5
PFBGA8U-181 (P-TFBGA-181-0808-0.50)	8 X 8 X 1.2	0.5
PFBGA7U-100 (P-TFBGA-100-0707-0.65)	7 X 7 X 1.2	0.65
PFBGA8U-112 (P-TFBGA-112-0808-0.65)	8 X 8 X 1.2	0.65
PFBGA8U-121 (P-TFBGA-121-0808-0.65)	8 X 8 X 1.2	0.65
PFBGA10U-160 (P-TFBGA-160-1010-0.65)	10 X 10 X 1.2	0.65
PFBGA10U-180 (P-TFBGA-180-1010-0.65)	10 X 10 X 1.2	0.65
PFBGA12U-208 (P-TFBGA-208-1212-0.65)	12 X 12 X 1.2	0.65
PFBGA7U-48 (P-TFBGA-048-0707-0.80)	7 X 7 X 1.2	0.8
PFBGA8U-81 (P-TFBGA-081-0808-0.80)	8 X 8 X 1.2	0.8
PFBGA10U-121 (P-TFBGA-121-1010-0.80)	10 X 10 X 1.2	0.8
PFBGA10U-144 (P-TFBGA-144-1010-0.80)	10 X 10 X 1.2	0.8
PFBGA12U-180 (P-TFBGA-180-1212-0.80)	12 X 12 X 1.2	0.8
PFBGA14U-220 (P-TFBGA-220-1414-0.80)	14 X 14 X 1.2	0.8
PFBGA14U-256 (P-TFBGA-256-1414-0.80)	14 X 14 X 1.2	0.8
PFBGA16U-280 (P-TFBGA-280-1616-0.80)	16 X 16 X 1.2	0.8

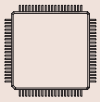
Very Thin Fine-pitch Ball Grid Array (VFBGA)



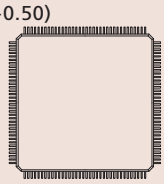
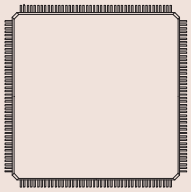
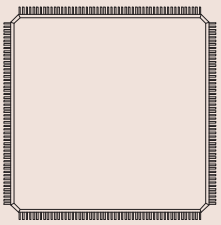
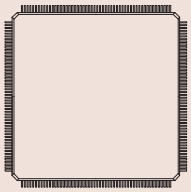
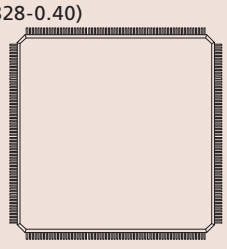
PKG Type (JEITA PKG Name	Body Size (mm)	Ball Pitch (mm)
VFBGA4H-49 (P-VFBGA-049-0404-0.50)	4 X 4 X 1.0	0.5
VFBGA5H-81 (P-VFBGA-081-0505-0.50)	5 X 5 X 1.0	0.5
VFBGA6H-96 (P-VFBGA-096-0606-0.50)	6 X 6 X 1.0	0.5
VFBGA6H-121 (P-VFBGA-121-0606-0.50)	6 X 6 X 1.0	0.5
VFBGA7H-144 (P-VFBGA-144-0707-0.50)	7 X 7 X 1.0	0.5
VFBGA7H-161 (P-VFBGA-161-0707-0.50)	7 X 7 X 1.0	0.5
VFBGA8H-181 (P-VFBGA-181-0808-0.50)	8 X 8 X 1.0	0.5
VFBGA10H-240 (P-VFBGA-240-1010-0.50)	10 X 10 X 1.0	0.5
VFBGA10H-121 (P-VFBGA-121-1010-0.80)	10 X 10 X 1.0	0.8
VFBGA10H-144 (P-VFBGA-144-1010-0.80)	10 X 10 X 1.0	0.8

Package Lineup

QFP & TQFP

PKG Type (JEITA PKG Name)	Body Size (mm)	Lead Pitch (mm)
TQFP12-48 (P-TQFP048-0707-0.50) 	7 X 7 X 1.2	0.5
* QFP12-48 (P-LQFP048-0707-0.50) 	7 X 7 X 1.7	0.5
TQFP13-64 (P-TQFP064-1010-0.50) 	10 X 10 X 1.2	0.5
* QFP13-64 (P-LQFP064-1010-0.50) 	10 X 10 X 1.7	0.5
* QFP14-80 (P-LQFP080-1212-0.50) 	12 X 12 X 1.7	0.5
* TQFP15-100 (P-TQFP100-1414-0.50) 	14 X 14 X 1.2	0.5
* QFP15-100 (P-LQFP100-1414-0.50) 	14 X 14 X 1.7	0.5
* TQFP15-128 (P-TQFP128-1414-0.40) 	14 X 14 X 1.2	0.4
* QFP15-128 (P-LQFP128-1414-0.40) 	14 X 14 X 1.7	0.4

* Can be on automobile

PKG Type (JEITA PKG Name)	Body Size (mm)	Lead Pitch (mm)
* QFP20-144 (P-LQFP144-2020-0.50) 	20 X 20 X 1.7	0.5
* QFP21-176 (P-LQFP176-2424-0.50) 	24 X 24 X 1.7	0.5
* QFP22-208 (P-LQFP208-2828-0.50) 	28 X 28 X 1.7	0.5
QFP21-216 (P-LQFP216-2424-0.40) 	24 X 24 X 1.7	0.4
QFP22-256 (P-LQFP256-2828-0.40) 	28 X 28 X 1.7	0.4

Gate Array Package List

Epson's Gate Array Series offers various packages for each base array.
Please select the most suitable package, based on the circuit specifications and number of input/output terminals.

Gate Array Package List is subject to change due to the preparation condition of the lead frame and the improvement of production efficiency. Please consult Epson sales office when you are choosing packages.

S1L5V000 Series

AL2-Series			S1L5V012	S1L5V042	–	S1L5V112	–	S1L5V252	–	S1L5V482
AL3-Series			S1L5V013	S1L5V043	S1X5V513*	S1L5V113	S1X5V523*	S1L5V253	S1X5V533*	S1L5V483
AL4-Series			S1L5V014	S1L5V044	S1X5V514*	S1L5V114	S1X5V524*	S1L5V254	S1X5V534*	S1L5V484
Raw Gates			8.9k	42.0k	26.0k	109.3k	90.3k	254.4k	235.0k	479.9k
AL2-Usable Gates			2.7k	12.6k	–	32.8k	–	63.6k	–	119.9k
AL3-Usable Gates			5.4k	25.2k	14.3k	65.6k	49.7k	139.9k	129.3k	239.9k
AL4-Usable Gates			6.2k	29.4k	16.9k	76.5k	58.7k	165.4k	152.8k	287.9k
Pads			48	104		168		256		308
PKG	Pin	PKG Type								
TQFP	48	TQFP12-48	A	A		A				
QFP	48	QFP12-48	A	A		A				
TQFP	64	TQFP13-64		A		A		A		N
QFP	64	QFP13-64		A		A		A		N
QFP	80	QFP14-80		A		A		A		A
TQFP	100	TQFP15-100		A		A		A		LQ
QFP	100	QFP15-100		A		A		A		A
TQFP	128	TQFP15-128		A (104)		A		A		A
QFP	128	QFP15-128		A (104)		A		A		A
QFP	144	QFP20-144				A		A		A
QFP	176	QFP21-176	N	N		A (168)		A		A
QFP	208	QFP22-208	N	N		N		A		A
QFP	216	QFP21-216	N	N		N		A		A
QFP	256	QFP22-256	N	N		N		LQ		A
QFN	24	SQFN4-24	A	N		N		N		N
QFN	32	SQFN5-32	A	A		N		N		N
QFN	48	SQFN7-48	N	A		A		N		N
QFN	64	SQFN9-64	N	A		A		A		N

A: Available for mass production
LQ: Quality assurance required (Lead frame required to be developed)
N: Not available A( ): Usable up to the numbers of pins in the parenthesis
*: Analog PLL built in master

Gate Array Package List

S1L50000 Series

		AL2-Series	S1L50062	S1L50122		S1L50282		S1L50552		S1L50752		S1L50992		S1L51252		S1L51772	S1L52502	S1L53352	S1L54422	S1L55062	S1L56682	S1L58152
		AL3-Series	S1L50063	S1L50123		S1L50283		S1L50553		S1L50753		S1L50993		S1L51253		S1L51773	S1L52503	S1L53353	S1L54423	S1L55063	S1L56683	S1L58153
		AL4-Series	S1L50064	S1L50124		S1L50284		S1L50554		S1L50754		S1L50994		S1L51254		S1L51774	S1L52504	S1L53354	S1L54424	S1L55064	S1L56684	S1L58154
		Raw Gates	5.8k	12.0k		28.8k		55.5k		75.8k		99.2k		125.8k		177.1k	250.2k	335.9k	442.2k	506.7k	668.6k	815.5k
		AL2-Usable Gates	2.9k	6.0k		14.4k		26.1k		35.7k		46.7k		56.6k		79.7k	112.6k	144.5k	176.9k	202.7k	267.5k	326.2k
		AL3-Usable Gates	5.1k	10.6k		25.3k		47.2k		64.4k		84.4k		100.7k		132.8k	187.7k	251.9k	309.5k	354.7k	468.0k	570.9k
		AL4-Usable Gates	5.5k	11.4k		27.3k		52.8k		72.0k		94.3k		119.5k		168.2k	237.7k	319.1k	397.9k	456.1k	601.7k	734.0k
		Pads	48	64	56	104	88	144	124	168	144	192	168	216	188	224	264	308	352	376	432	480
		Pad Pitch	70µ	70µ	80µ	70µ	80µ	70µ	80µ	70µ	80µ	70µ	80µ	70µ	80µ	80µ	80µ	80µ	80µ	80µ	80µ	80µ
PKG	Pin	PKG Type																				
TQFP	48	TQFP12-48	A	A	A		A		A		A		A	N	N	N	N	N	N	N	N	N
QFP	48	QFP12-48	A	A	A		A		A		A		A	N	N	N	N	N	N	N	N	N
TQFP	64	TQFP13-64		A	A(56)		A	A	A		A		A		A	A	A	N	N	N	N	N
QFP	64	QFP13-64		A	A(56)		A	A	A		A		A		A	A	A	N	N	N	N	N
QFP	80	QFP14-80				A	A	A	A		A		A		A	A	A	A	N	N	N	N
TQFP	100	TQFP15-100				A		A	A		A		A		A	A	A	LQ	LQ	N	N	N
QFP	100	QFP15-100				A		A	A		A		A		A	A	A	A	A	N	N	N
TQFP	128	TQFP15-128						A			A		A		A	A	A	A	LQ	N	N	N
QFP	128	QFP15-128						A			A		A		A	A	A	A	A	N	N	N
QFP	144	QFP20-144						A			A		A		A	A	A	A	A	A	LQ	N
QFP	176	QFP21-176	N	N	N	N	N	N		A(168)		A			A	A	A	A	A	A	A	N
QFP	208	QFP22-208	N	N	N	N	N	N		N		N	N	N		A	A	A	A	N	N	N
QFP	216	QFP21-216	N	N	N	N	N	N		N	N	N	N	A		A	A	A	LQ	N	N	N
QFP	256	QFP22-256	N	N	N	N	N	N		N	N	N	N				A	A	A	LQ	LQ	N
QFN	24	SQFN4-24	A	A	A	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
QFN	32	SQFN5-32	A	A	A	A	A	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
QFN	48	SQFN7-48	A	A	A	A	A	A	A	A	A	A	A	A	A	N	N	N	N	N	N	N
QFN	64	SQFN9-64		A		A	A	A	A	A	A	A	A	A	A	A	N	N	N	N	N	N

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Gate Array Package List

S1L60000 Series

		AL3-Series	S1L60093	S1L60173	S1L60283	S1L60403	S1L60593	S1L60833	S1L61233	S1L61583	S1L61903	S1L62513
		AL4-Series	S1L60094	S1L60174	S1L60284	S1L60404	S1L60594	S1L60834	S1L61234	S1L61584	S1L61904	S1L62514
		Raw Gates	99.2k	171.8k	284.4k	400.3k	595.4k	831.6k	1,234.9k	1,587.8k	1,903.0k	2,519.6k
		AL3-Usable Gates	59.6k	103.1k	142.2k	200.2k	297.7k	332.7k	494.0k	635.1k	761.2k	1,007.9k
		AL4-Usable Gates	69.5k	120.2k	184.9k	260.2k	387.0k	415.8k	617.5k	793.9k	951.5k	1,259.8k
		70µm Pads	112	148	188	224	272	-	-	-	-	-
		80µm Pads	-	-	-	-	-	284	344	388	424	488
PKG	Pin	PKG Type										
TQFP	48	TQFP12-48	A	A	A	N	N	N	N	N	N	N
QFP	48	QFP12-48	A	A	A	N	N	N	N	N	N	N
TQFP	64	TQFP13-64	A	A	A	A	A	A	N	N	N	N
QFP	64	QFP13-64	A	A	A	A	A	A	N	N	N	N
QFP	80	QFP14-80	A	A	A	A	A	A	A	N	N	N
TQFP	100	TQFP15-100	A	A	A	A	A	LQ	LQ	N	N	N
QFP	100	QFP15-100	A	A	A	A	A	A	A	N	N	N
TQFP	128	TQFP15-128	A(112)	A	A	A	A	A	A	N	N	N
QFP	128	QFP15-128	A(112)	A	A	A	A	A	A	N	N	N
QFP	144	QFP20-144	N	A	A	A	A	A	A	A	N	N
QFP	176	QFP21-176	N	A	A	A	A	A	A	A	A	LQ
QFP	208	QFP22-208	N	N	A	A	A	A	A	LQ	LQ	N
QFP	216	QFP21-216	N	N	N	A	A	A	LQ	LQ	LQ	N
QFP	256	QFP22-256	N	N	N	N	A	A	A	LQ	LQ	N
QFN	24	SQFN4-24	N	N	N	N	N	N	N	N	N	N
QFN	32	SQFN5-32	A	N	N	N	N	N	N	N	N	N
QFN	48	SQFN7-48	A	A	A	A	N	N	N	N	N	N
QFN	64	SQFN9-64	A	A	A	A	A	N	N	N	N	N

A: Available for mass production
LQ: Quality assurance required (Lead frame required to be developed)
N: Not available A( ): Usable up to the numbers of pins in the parenthesis

Package's Thermal Resistance

Among LSIs, chip temperatures (T_j) rise as power consumption increases. The chip temperature of a packaged IC can be calculated based on the ambient temperature T_a, the package's thermal resistance $\theta_{j\text{-}a}$, and the power dissipation P_D as shown below.

Chip temperature (T_j) = T_a + (P_D x $\theta_{j\text{-}a}$) (°C)

As a general rule, the chip temperature(T_j) should be kept under 125°C. Note also that the package's thermal resistance varies widely depending on the chip size and substrates, the mounting method, the forced cooling.

QFP

Package Type	$\theta_{j\text{-}a}$ (°C/W)		
	0m/sec	1m/sec	2m/sec
QFP12	51	46	44
QFP13	48	45	43
QFP14	44	41	39
QFP15	41	39	37
QFP20	36	33	31
QFP21	34	31	29
QFP22	27	24	23
TQFP12	53	47	45
TQFP13	47	44	42
TQFP15	42	36	34

SQFN

Package Type	$\theta_{j\text{-}a}$ (°C/W)		
	0m/sec	1m/sec	2m/sec
SQFN4	42	39	37
SQFN5	40	37	35
SQFN7	31	28	25
SQFN9	26	23	21

PFBGA

Package Type	$\theta_{j\text{-}a}$ (°C/W)		
	0m/sec	1m/sec	2m/sec
PFBGA5	60	55	54
PFBGA6	54	49	48
PFBGA7	49	44	43
PFBGA8	44	39	38
PFBGA10	37	32	30
PFBGA12	33	29	27
PFBGA13	30	26	24
PFBGA14	24	20	19
PFBGA16	21	18	17

VFBGA

Package Type	$\theta_{j\text{-}a}$ (°C/W)		
	0m/sec	1m/sec	2m/sec
VFBGA4	66	61	60
VFBGA5	60	55	54
VFBGA6	54	49	48
VFBGA7	49	44	43
VFBGA8	44	39	38
VFBGA10	37	32	30

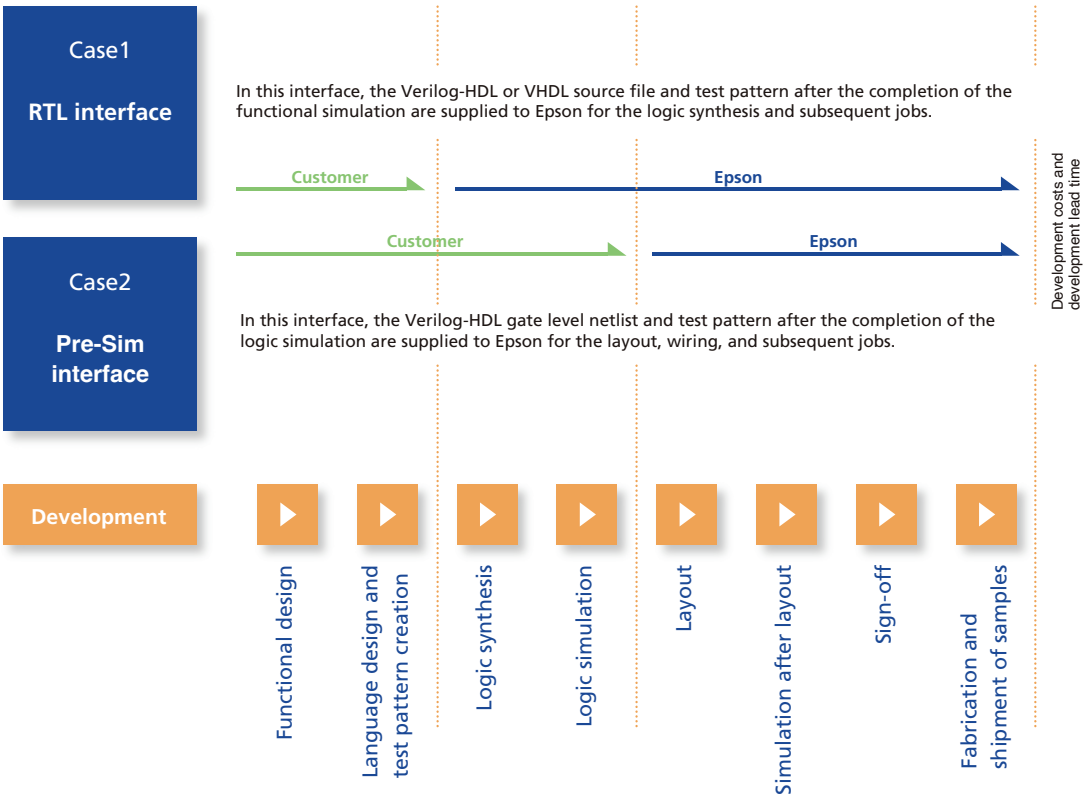
PBGA

Package Type	$\theta_{j\text{-}a}$ (°C/W)		
	0m/sec	1m/sec	2m/sec
PBGA1U	24	21	20

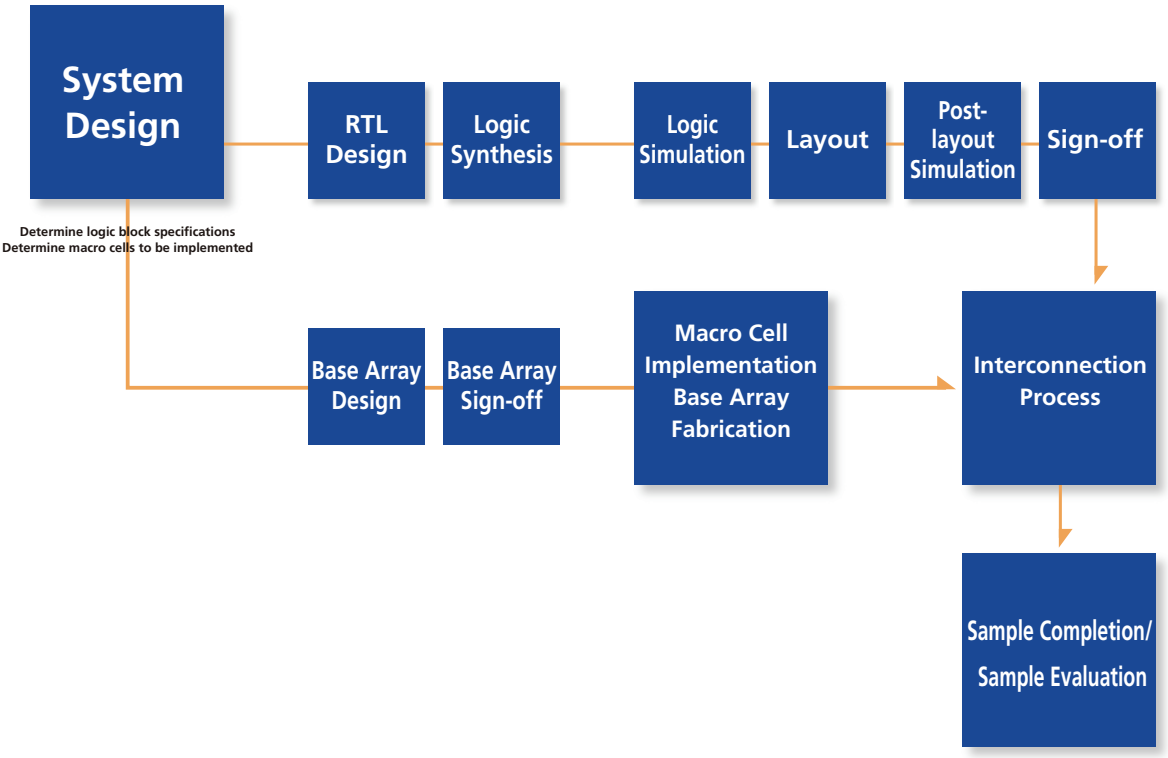
Values listed above are typical values using following evaluation boards, but the thermal resistance can easily vary depending on conditions.
- QFP, SQFN, PBGA : JEDEC STD board (114.3x76.2x1.6mm 4layer)
- PFBGA, VFBGA : JEDEC STD board (114.5x101.5x1.6mm 4layer)

User Interface

In order to flexibly comply with the customer's design stages, Epson offers two types of user interfaces. The development lead time and development costs are determined by the interface of your choice.

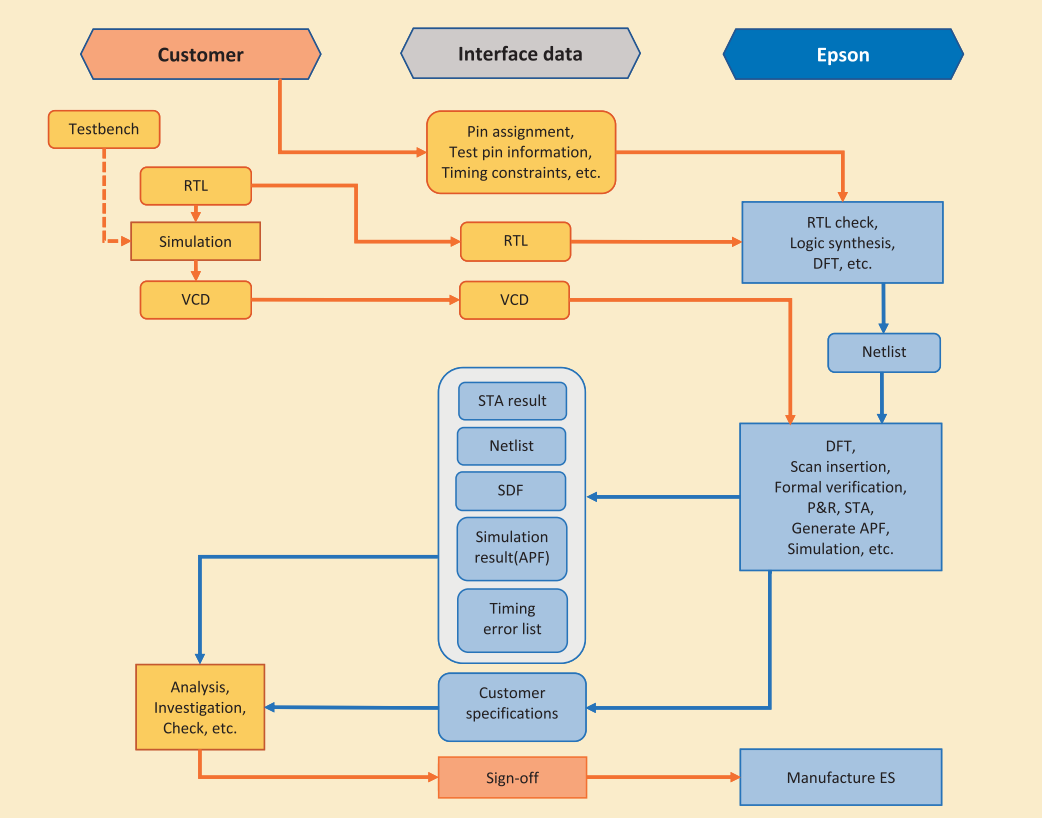


Design of Embedded Array Chips



Development Flow

Interface Flow



Library Pack

Supported series

Technology	0.35µm	0.25µm	0.15µm
Gate Array	S1L50000 S1L5V000	S1L60000	-
Embedded Array	S1X5V000 S1X50000	S1X60000	S1X80000
Standard cell	-	-	S1K80000

Supported tools

Category	Tool name
Synthesis	Design Compiler
Formal verification	Formality
RTL check	SpyGlass
Static timing analysis	Primetime
Simulation	Verilog-XL, NC-Verilog, ModelSim(Verilog), ModelSim(VHDL)*

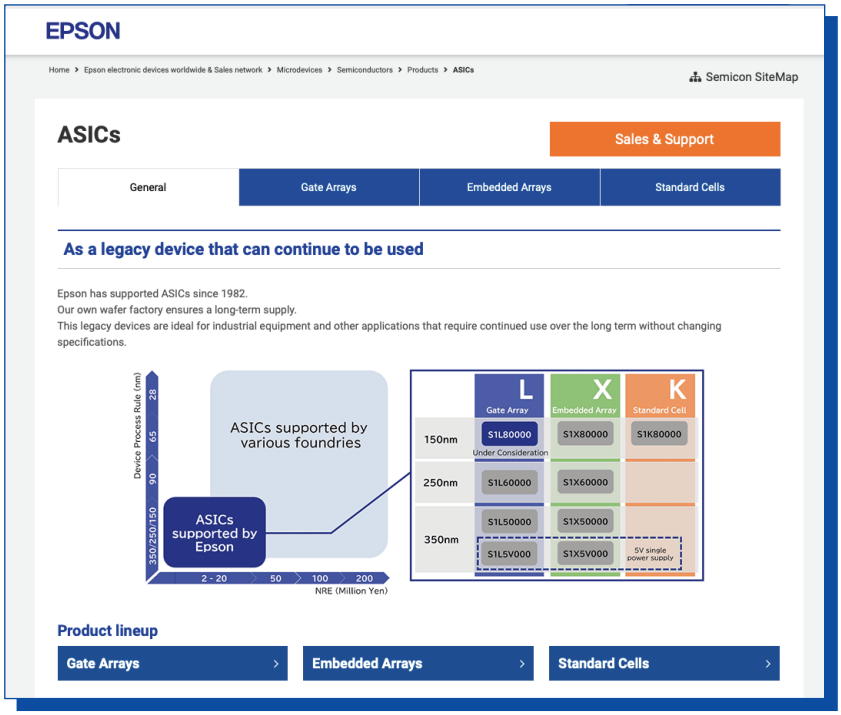
*: Not available for S1L5V000, S1X5V000, S1X80000, S1K80000 series

Epson ASIC Website

■Epson Website Presents ASIC product information

<global.epson.com/products_and_drivers/semicon/products/asic/>

<ASIC HP>



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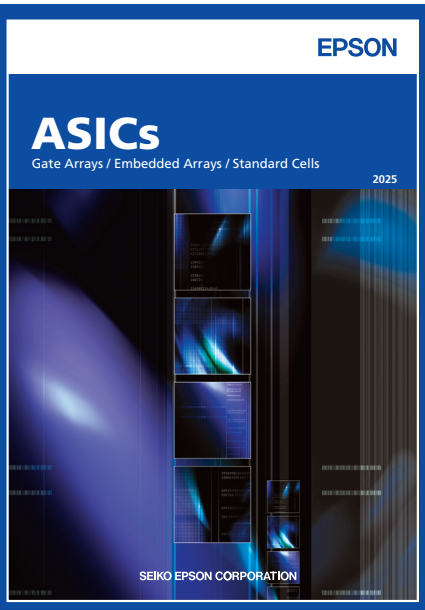
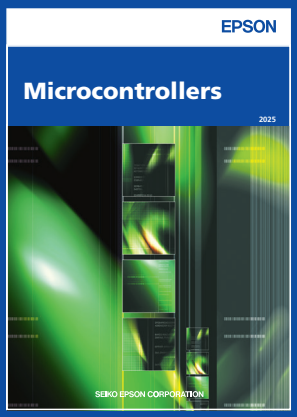
ASICs

Gate Arrays / Embedded Arrays / Standard Cells
2025





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