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CMOS 4-BIT SINGLE CHIP MICROCONTROLLER

S1C60N16
Technical Manual

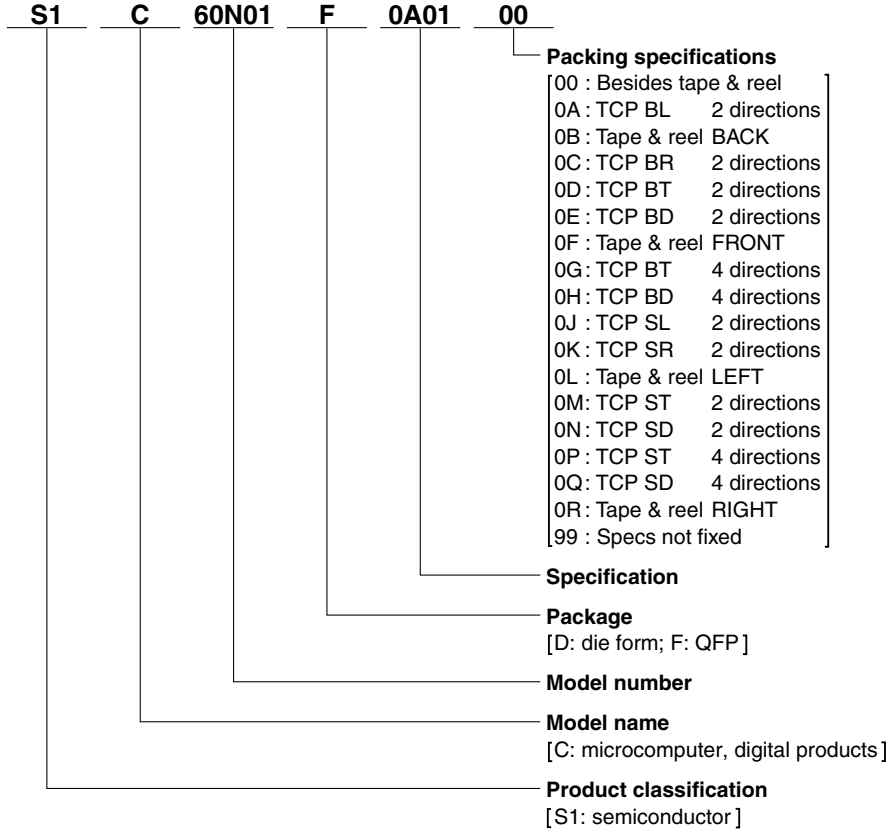
SEIKO EPSON CORPORATION

Rev.1.3

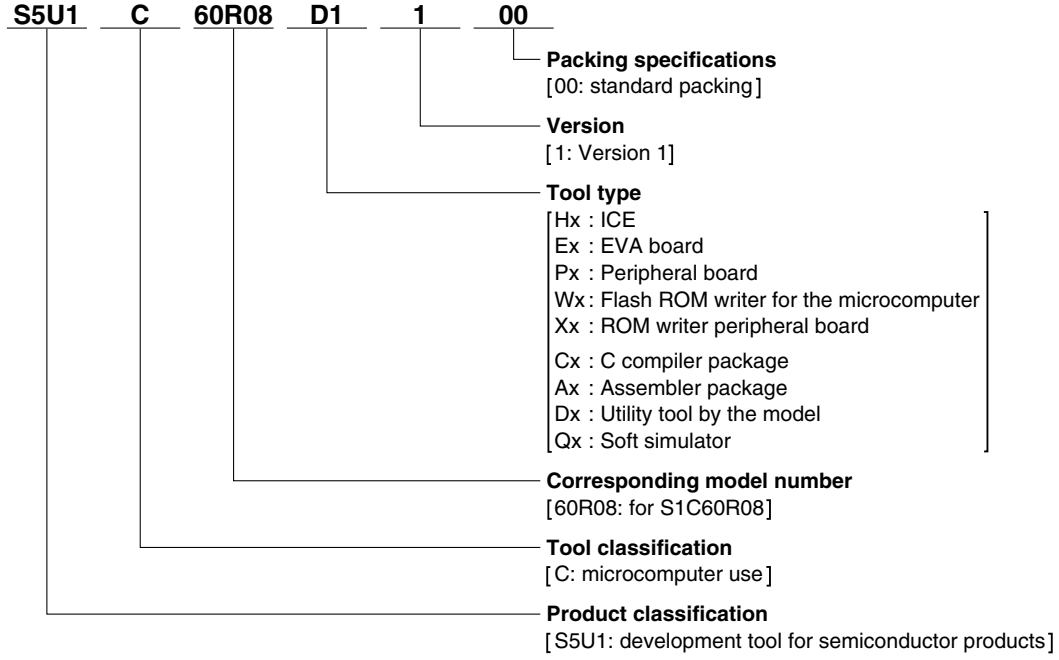
NOTICE

Configuration of product number

Devices



Development tools



CONTENTS

CHAPTER 1 OVERVIEW

The S1C60N16 Series is a single-chip microcomputer made up of the 4-bit core CPU S1C6200C, ROM (4,096 words × 12 bits), RAM (256 words × 4 bits), LCD driver, analog comparator, event counter, watch-dog timer, and two types of time base counter. Because of its low-voltage operation and low power consumption, this series is ideal for a wide range of battery-driven applications. It is especially suitable for various controller applications such as a clock, game and pager.

1.1 Configuration

The S1C60N16 Series is configured as follows, depending on supply voltage and oscillation circuits.

Table 1.1.1 Model configuration

Model	**S1C60N16**	**S1C60L16**	**S1C60A16**
Supply voltage	3.0 V	1.5 V	3.0 V
Oscillation circuit	OSC1 only (Single clock)		OSC1 and OSC3 (Twin clock)
LCD power supply	Supports 3.0 V LCD panels		

1.2 Features

Table 1.2.1 Features

Model		**S1C60N16**	**S1C60L16**	**S1C60A16**
OSC1 oscillation circuit		Crystal oscillation circuit 32.768 kHz (Typ.)		
OSC3 oscillation circuit		–		CR or ceramic oscillation circuit (selected by mask option) 1 MHz (Typ.)
Instruction set		108 types		
Instruction execution time (differs depending on instruction) (CLK: CPU operation frequency)		153 µsec, 214 µsec, 366 µsec (CLK = 32.768 kHz)		
		–		5 µsec, 7 µsec, 12 µsec (CLK = 1 MHz)
ROM capacity		4,096 words × 12 bits		
RAM capacity		256 words × 4 bits		
Input ports		5 bits (pull-down resistor can be added by mask option)		
Output ports		8 bits (BZ, $\overline{BZ}$, FOUT and SIOF outputs are available by mask option)		
I/O ports		8 bits (pull-down resistor is added during input data read-out) (3 bits can be configured as serial I/O ports by mask option)		
Serial interface		1 port (8-bit clock synchronous system)		
LCD driver		38 segments × 4, 3, or 2 commons (selected by mask option) V-3 V 1/4, 1/3 or 1/2 duty (voltage regulator and booster circuits built-in)		
Time base counter		Two types (timer and stopwatch)		
Watchdog timer		Built-in (can be disabled by mask option)		
Event counter		Two 8-bit inputs (dial input evaluation or independent)		
Sound generator		Programmable in 8 sounds (8 frequencies) Digital envelope built-in (can be disabled by mask option)		
Analog comparator		Inverted input × 1, non-inverted input × 1		
Supply voltage detection (SVD)		2.2 V	1.2 V	2.2 V
Heavy load protection function		Not implemented		Implemented
External interrupt		Input interrupt: 2 systems		
Internal interrupt		Time base counter interrupt: 2 systems Serial interface interrupt: 1 system		
Supply voltage		3.0 V (2.2–3.6 V)	1.5 V (1.2–1.8 V)	3.0 V (2.2–3.6 V)
Current consumption (Typ. value)	CLK= 32.768 kHz (when halted)	0.7 µA	0.7 µA	1.5 µA (Normal operation mode)
	CLK= 32.768 kHz (when executed)	1.4 µA	1.4 µA	2.4 µA (Normal operation mode)
	CLK= 1 MHz (ceramic) (when executed)	–	–	50 µA (Normal operation mode)
	CLK= 1 MHz (CR) (when executed)	–	–	85 µA (Normal operation mode)
Form when shipped		QFP14-80pin or chip		

1.3 Block Diagram

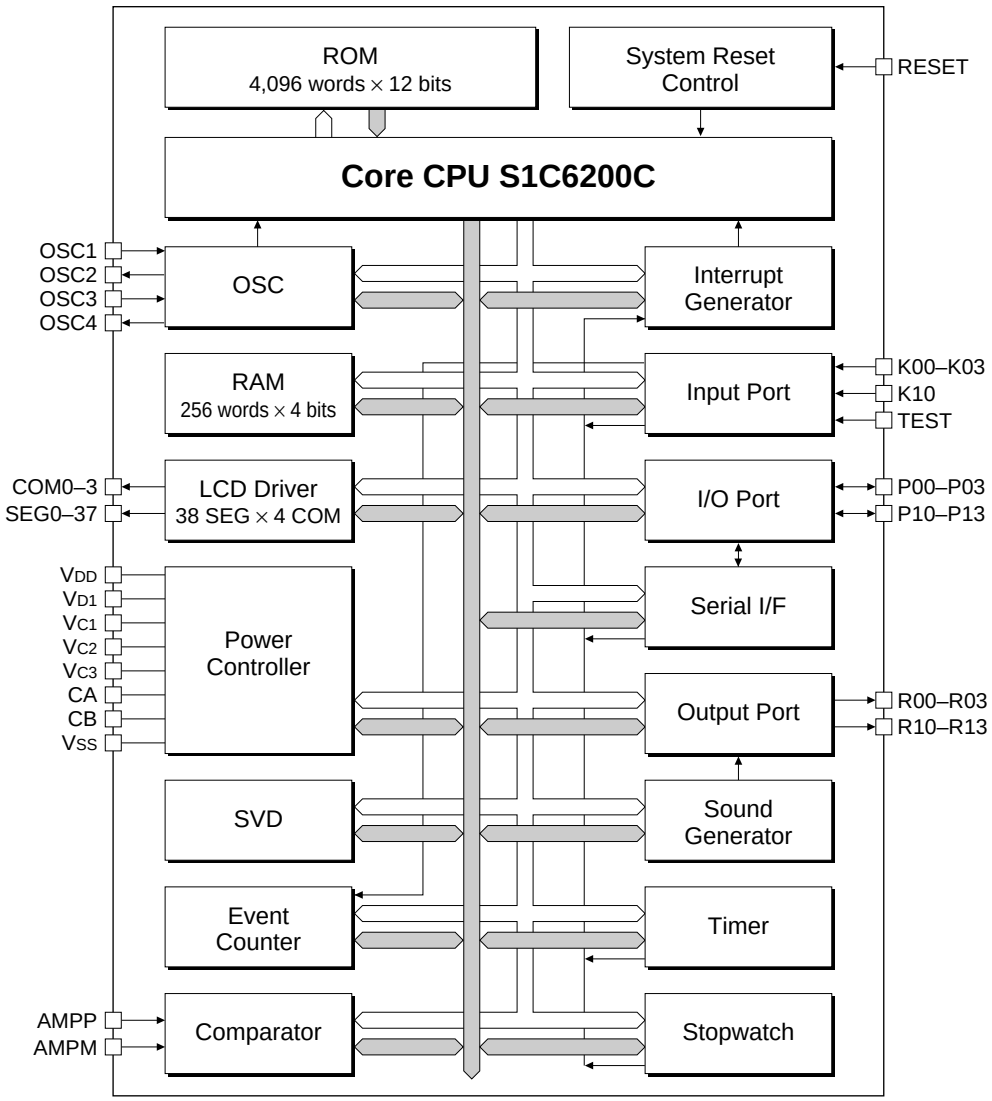
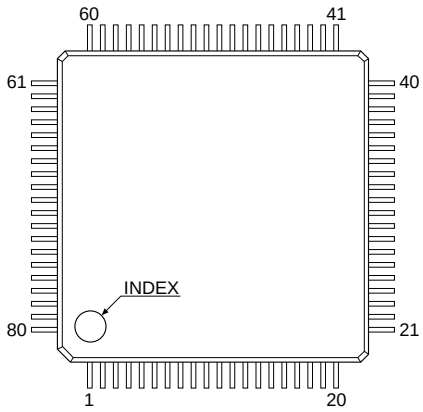


Fig. 1.3.1 Block diagram

1.4 Pin Layout Diagram

QFP14-80pin



No.	Name	No.	Name	No.	Name	No.	Name
1	P13	21	K10	41	SEG37	61	SEG17
2	P12	22	V_{SS}	42	SEG36	62	SEG16
3	P11	23	AMPM	43	SEG35	63	SEG15
4	P10	24	AMPP	44	SEG34	64	SEG14
5	P03	25	OSC1	45	SEG33	65	SEG13
6	P02	26	OSC2	46	SEG32	66	SEG12
7	P01	27	V_{D1}	47	SEG31	67	SEG11
8	P00	28	OSC3	48	SEG30	68	SEG10
9	R13	29	OSC4	49	SEG29	69	SEG9
10	R12	30	V_{DD}	50	SEG28	70	SEG8
11	R11	31	V_{C3}	51	SEG27	71	SEG7
12	R10	32	V_{C2}	52	SEG26	72	SEG6
13	R03	33	V_{C1}	53	SEG25	73	SEG5
14	R02	34	CB	54	SEG24	74	SEG4
15	R01	35	N.C.	55	SEG23	75	SEG3
16	R00	36	CA	56	SEG22	76	SEG2
17	K00	37	COM3	57	SEG21	77	SEG1
18	K01	38	COM2	58	SEG20	78	SEG0
19	K02	39	COM1	59	SEG19	79	RESET
20	K03	40	COM0	60	SEG18	80	TEST

N.C. : No Connection

Fig. 1.4.1 Pin layout

1.5 Pin Description

Table 1.5.1 Pin description

Pin name	Pin No.	I/O	Function
V_{DD}	30	(I)	Power supply pin (+)
V_{SS}	22	(I)	Power supply pin (-)
V_{D1}	27	–	Oscillation and internal logic system voltage output pin
V_{C1}	33	–	LCD drive voltage output pin (approx. 0.98 V)
V_{C2}	32	–	LCD drive voltage output pin (2·V_{C1})
V_{C3}	31	–	LCD drive voltage output pin (3·V_{C1})
CA, CB	36, 34	–	Boost capacitor connecting pin
OSC1	25	I	Crystal oscillation input pin
OSC2	26	O	Crystal oscillation output pin
OSC3	28	I	CR or ceramic oscillation input pin * (N.C. for S1C60N16 and S1C60L16)
OSC4	29	O	CR or ceramic oscillation output pin * (N.C. for S1C60N16 and S1C60L16)
K00–K03	17–20	I	Input port pin
K10	21	I	Input port pin
P00–P03	8–5	I/O	I/O port pin
P10	4	I/O	I/O port pin or serial interface data input pin *
P11	3	I/O	I/O port pin or serial interface data output pin *
P12	2	I/O	I/O port pin or serial interface clock input/output pin *
P13	1	I/O	I/O port pin
R00–R03	16–13	O	Output port pin
R10	12	O	Output port pin or BZ output pin *
R13	11	O	Output port pin or $\overline{BZ}$ output pin *
R11	10	O	Output port pin or SIOF output pin *
R12	9	O	Output port pin or FOUT output pin *
AMPP	24	I	Analog comparator non-inverted input pin
AMPM	23	I	Analog comparator inverted input pin
SEG0–37	78–41	O	LCD segment output pin or DC output pin *
COM0–3	40–37	O	LCD common output pin (1/2, 1/3 or 1/4 duty are selectable *)
RESET	79	I	Initial reset input pin
TEST	80	I	Test input pin

* Can be selected by mask option

1.6 Option List

The following function and segment options are provided for the S1C60N16 Series.
Multiple specifications are available in each option item as indicated in the Option List. Select the specifications that meet the target system using the function option generator winfog and the segment option generator winsog. Be sure to record the specifications for unused ports too, according to the instructions provided.
Refer to the "S1C60/62 Family Development Tool Manual" for winfog and winsog.

<FUNCTION OPTION>

1. DEVICE TYPE

- DEVICE TYPE ..... ☐ 1. S1C60N16 (Normal Type)
  ☐ 2. S1C60L16 (Low Power Type)
  ☐ 3. S1C60A16 (Twin Clock Type)

2. OSC3 SYSTEM CLOCK (only for S1C60A16)

☐ 1. Ceramic ☐ 2. CR

3. MULTIPLE KEY ENTRY RESET

- COMBINATION ..... ☐ 1. Not Use
  ☐ 2. Use K00, K01
  ☐ 3. Use K00, K01, K02
  ☐ 4. Use K00, K01, K02, K03
- TIME AUTHORIZE ..... ☐ 1. Not Use ☐ 2. Use

4. WATCHDOG TIMER

☐ 1. Use ☐ 2. Not Use

5. I/P INTERRUPT NOISE REJECTOR

- K00–K03 ..... ☐ 1. Use ☐ 2. Not Use
- K10 ..... ☐ 1. Use ☐ 2. Not Use

6. SIO FUNCTION

- SIO FUNCTION ..... ☐ 1. Not Use ☐ 2. Use
- SIO SCLK LOGIC ..... ☐ 1. Positive ☐ 2. Negative
- SIO DATA PERMUTATION ..... ☐ 1. MSB First ☐ 2. LSB First

7. I/P PULL DOWN RESISTOR

- K00 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K01 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K02 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K03 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K10 ..... ☐ 1. With Resistor ☐ 2. Gate Direct

8. O/P OUTPUT SPECIFICATION (R00–R03)

- R00 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- R01 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- R02 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- R03 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain

9. R10 TERMINAL SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. Buzzer Output

10. R11 TERMINAL SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. SIO Flag

11. R12 TERMINAL SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output
  ☐ 2. FOUT 32768 [Hz]
  ☐ 3. FOUT 16384 [Hz]
  ☐ 4. FOUT 8192 [Hz]
  ☐ 5. FOUT 4096 [Hz]
  ☐ 6. FOUT 2048 [Hz]
  ☐ 7. FOUT 1024 [Hz]
  ☐ 8. FOUT 512 [Hz]
  ☐ 9. FOUT 256 [Hz]

12. R13 TERMINAL SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output
  ☐ 2. Buzzer Inverted Output (R13 Control)
  ☐ 3. Buzzer Inverted Output (R10 Control)

13. I/O PORT SPECIFICATION (P00–P03)

- P00 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P01 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P02 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P03 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain

14. I/O PORT SPECIFICATION (P10–P13)

- P10 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P11 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P12 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P13 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain

15. EVENT COUNTER NOISE REJECTOR

☐ 1. 2048 [Hz] ☐ 2. 256 [Hz]

16. LCD DRIVER DUTY

- DUTY SELECTION ..... ☐ 1. 1/4 Duty
  ☐ 2. 1/3 Duty
  ☐ 3. 1/2 Duty

17. LCD BIAS & POWER SOURCE

- BIAS & POWER SOURCE SELECTION
  S1C60N16 ..... ☐ 1. 1/3 Bias, Regulator Used, LCD 3 V
  S1C60L16 ..... ☐ 1. 1/3 Bias, Regulator Used, LCD 3 V
  S1C60A16 ..... ☐ 1. 1/3 Bias, Regulator Used, LCD 3 V
  ☐ 2. 1/3 Bias, Regulator Not Used, LCD 3 V
  ☐ 3. 1/2 Bias, Regulator Not Used, LCD 3 V

18. SEGMENT MEMORY ADDRESS

☐ 1. 2 Page (240–265) ☐ 2. 0 Page (040–065)

<SEGMENT OPTION>

TERMINAL NAME	ADDRESS												OUTPUT SPECIFICATION
	COM0			COM1			COM2			COM3			
	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0													SEG output ☐
SEG1													DC output ☐ C ☐ P
SEG2													SEG output ☐
SEG3													DC output ☐ C ☐ P
SEG4													SEG output ☐
SEG5													DC output ☐ C ☐ P
SEG6													SEG output ☐
SEG7													DC output ☐ C ☐ P
SEG8													SEG output ☐
SEG9													DC output ☐ C ☐ P
SEG10													SEG output ☐
SEG11													DC output ☐ C ☐ P
SEG12													SEG output ☐
SEG13													DC output ☐ C ☐ P
SEG14													SEG output ☐
SEG15													DC output ☐ C ☐ P
SEG16													SEG output ☐
SEG17													DC output ☐ C ☐ P
SEG18													SEG output ☐
SEG19													DC output ☐ C ☐ P
SEG20													SEG output ☐
SEG21													DC output ☐ C ☐ P
SEG22													SEG output ☐
SEG23													DC output ☐ C ☐ P
SEG24													SEG output ☐
SEG25													DC output ☐ C ☐ P
SEG26													SEG output ☐
SEG27													DC output ☐ C ☐ P
SEG28													SEG output ☐
SEG29													DC output ☐ C ☐ P
SEG30													SEG output ☐
SEG31													DC output ☐ C ☐ P
SEG32													SEG output ☐
SEG33													DC output ☐ C ☐ P
SEG34													SEG output ☐
SEG35													DC output ☐ C ☐ P
SEG36													SEG output ☐
SEG37													DC output ☐ C ☐ P

Legend: <ADDRESS>
H: High order address (4–6)
L: Low order address (0–F)
D: Data bit (0–3)

<OUTPUT SPECIFICATION>
C: Complementary output
P: Pch open drain output

Note: When setting H (high order address) to 6, L (low order address) must be within 0 to 5.

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (*1) supplied to VDD through VSS, the S1C60N16 Series generates the necessary internal voltage with the voltage regulator circuit (<VD1> for oscillators, <VC1> for LCD) and the voltage booster circuit (<VC2 and VC3> for LCD).

*1 Supply voltage: S1C60N16/60A16 .. 3 V, S1C60L16 .. 1.5 V

Figure 2.1.1 shows the power supply configuration.
The voltage <VD1> for the internal circuit is generated by the internal system voltage regulator.

The S1C60N16 Series generates <VC1> with the voltage regulator and <VC2, VC3> with the voltage booster.

Notes: • *External loads cannot be driven by the output voltage of the voltage regulator and voltage booster.*
• *See Chapter 7, "Electrical Characteristics", for voltage values.*

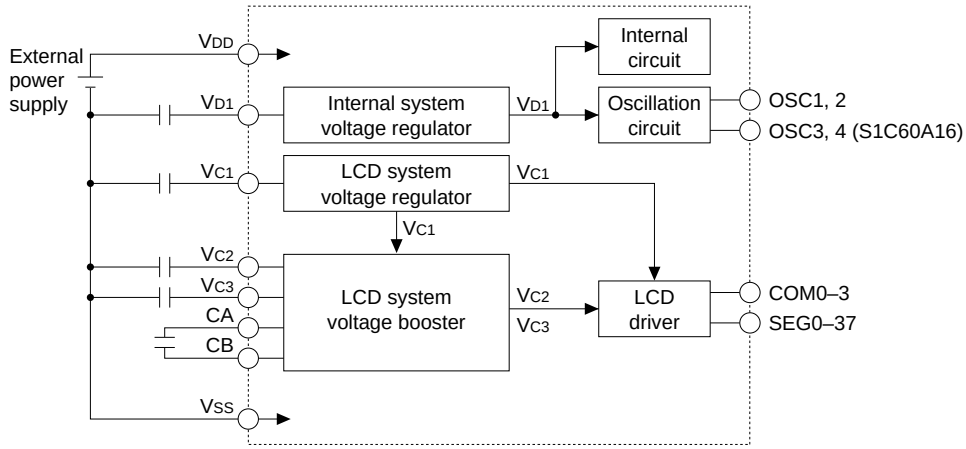


Fig. 2.1.1 Power supply configuration

The LCD system voltage regulator in the S1C60A16 can be disabled by mask option. In this case, external elements can be minimized because the external capacitors for the LCD system voltage regulator are not necessary. However when the LCD system voltage regulator is not used, the display quality of the LCD panel, when the supply voltage fluctuates (drops), is inferior to when the LCD system voltage regulator is used. Figure 2.1.2 shows the external element configuration when the LCD system voltage regulator is not used.

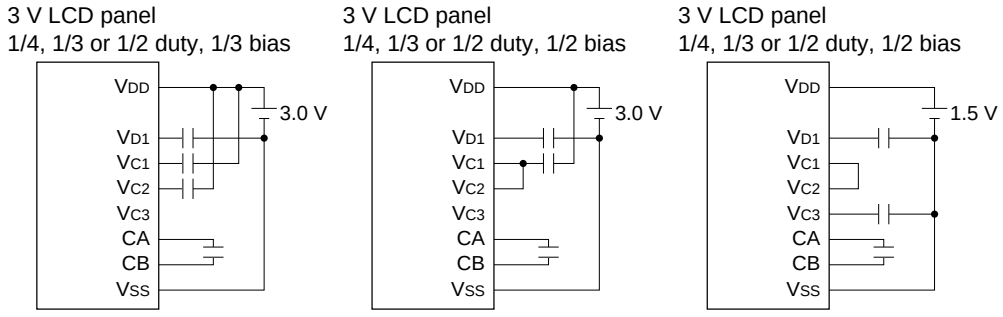


Fig. 2.1.2 External elements when LCD system voltage regulator is not used (S1C60A16)

2.2 Initial Reset

To initialize the S1C60N16 Series circuits, initial reset must be executed. There are four ways of doing this.
(1) Initial reset by the power on reset circuit
(2) External initial reset by the RESET terminal
(3) External initial reset by simultaneous high input to terminals K00–K03
(4) Initial reset by the watchdog timer

Figure 2.2.1 shows the configuration of the initial reset circuit.

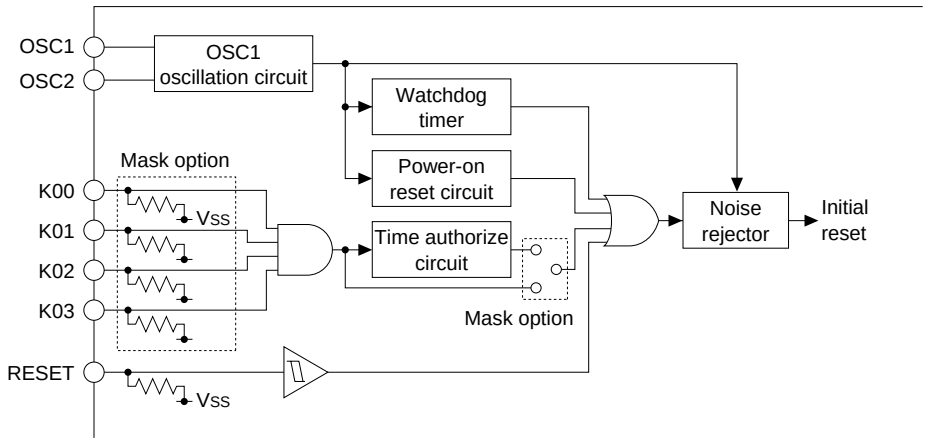


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Power-on reset circuit

The power-on reset circuit outputs the initial reset signal at power-on until the oscillation circuit starts oscillating.

Note: The power-on reset circuit may not work properly due to unstable or lower voltage input. The following two initial reset method are recommended to generate the initial reset signal.

2.2.2 RESET terminal

Initial reset can be executed externally by setting the reset terminal to the high level. This high level must be maintained for at least 5 msec (when oscillating frequency is f_{OSC1} = 32 kHz), because the initial reset circuit contains a noise rejector. When the reset terminal goes low the CPU begins to operate.

2.2.3 Simultaneous high input to input ports (K00–K03)

Another way of executing initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option. The specified input port terminals must be kept high for at least 5 msec (when oscillating frequency is f_{OSC1} = 32 kHz), because the initial reset circuit contains a noise rejector. Table 2.2.3.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.3.1 Input port combination

Selection	Combination
A	Not used
B	K00∗K01
C	K00∗K01∗K02
D	K00∗K01∗K02∗K03

When, for instance, mask option D (K00*K01*K02*K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time.

Further, the time authorize circuit can be selected with the mask option. The time authorize circuit performs initial reset, when the input time of the simultaneous high input is authorized and found to be the same or more than the defined time (1 to 3 sec).

If you use this function, make sure that the specified ports do not go high at the same time during ordinary operation.

2.2.4 Watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See Section 4.2, "Resetting Watchdog Timer", for details.

2.2.5 Internal register at initial reset

Initial reset initializes the CPU as shown in the table below.

Table 2.2.5.1 Initial values

CPU Core			
Name	Symbol	Bit size	Initial value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register X	X	10	Undefined
Index register Y	Y	10	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral Circuits		
Name	Bit size	Initial value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	4	*

* See Section 4.1, "Memory Map".

2.3 Test Terminal (TEST)

This terminal is used when the IC load is being detected. During ordinary operation be certain to connect this terminal to Vss.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C60N16 Series employs the core CPU S1C6200C for the CPU, so that register configuration, instructions and so forth are virtually identical to those in other family processors using the S1C6200 / 6200A / 6200B / 6200C.
Refer to the "S1C6200 / 6200A Core CPU Manual" for details about the core CPU.
Note the following points with regard to the S1C60N16 Series:

(1) The SLEEP operation is not assumed, so the SLP instruction cannot be used.

(2) Because the ROM capacity is 4,096 words, bank bits are unnecessary and PCB and NBP are not used.

(3) Data memory is set up to two pages, so only the two low-order bits are valid for the page portion (XP, YP) of the index register that specifies addresses. (The two high-order bits are ignored.)

3.2 ROM

The built-in ROM, a mask ROM for loading the program, has a capacity of 4,096 steps, 12 bits each. The program area is 16 pages (0–15), each of 256 steps (00H–FFH). After initial reset, the program start address is page 1, step 00H. The interrupt vector is allocated to page 1, steps 01H–0FH.

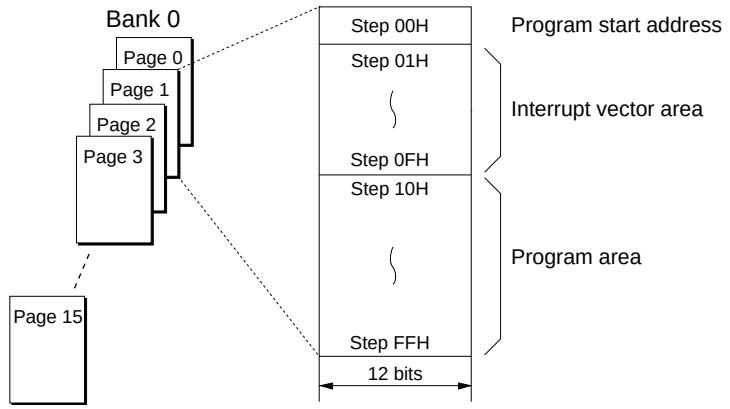


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory for storing a variety of data, has a capacity of 256 words, 4-bit words. When programming, keep the following points in mind:

(1) Part of the data memory is used as stack area when saving subroutine return addresses and registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words on the stack.

(3) Data memory 000H–00FH is the memory area pointed by the register pointer (RP).

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the S1C60N16 Series are memory mapped. Thus, all the peripheral circuits can be controlled by using memory operations to access the I/O memory. The following sections describe how the peripheral circuits operate.

4.1 Memory Map

The data memory of the S1C60N16 Series has an address space of 287 words (325 words when display memory is laid out in Page 2), of which 38 words are allocated to display memory and 31 words, to I/O memory. Figure 4.1.1 shows the overall memory map for the S1C60N16 Series, and Tables 4.1.1(a)–(c), the memory maps for the peripheral circuits (I/O space).

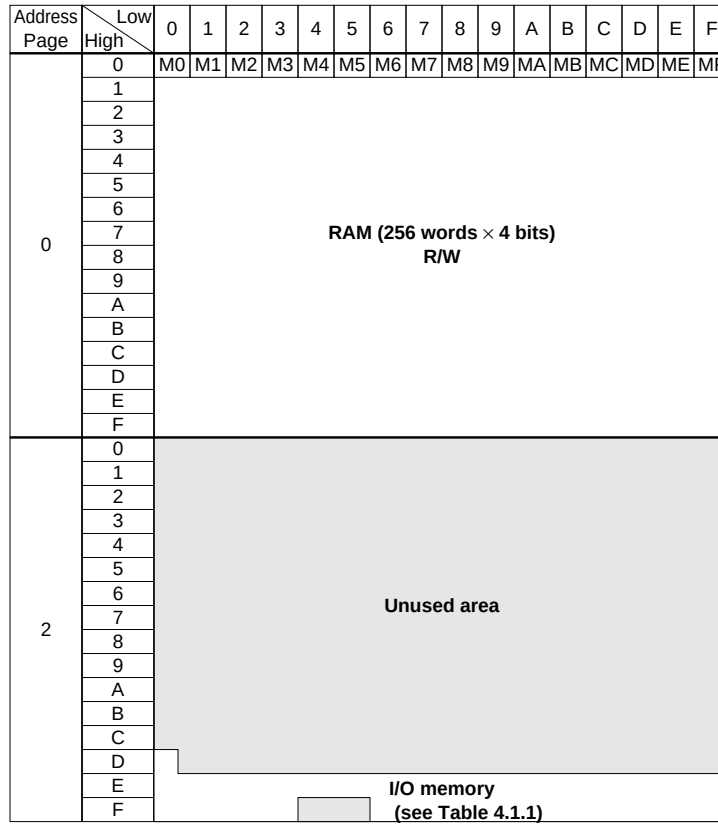


Fig. 4.1.1 Memory map

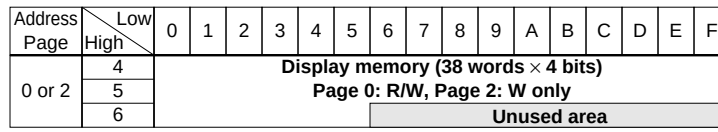


Fig. 4.1.2 Display memory map

Notes:
- *The display memory area can be selected from between Page 0 (040H–065H) and Page 2 (240H–265H) by mask option. When Page 0 (040H–065H) is selected, the display memory is assigned in the RAM area. So read/write operation is allowed. When Page 2 (240H–265H) is selected, the display memory is assigned as a write-only memory.*
- *Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

Table 4.1.1(a) I/O memory map (2D0H, 2E0H–2ECH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2D0H	0	0	0	CSDC2	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R			R/W	0 *3	– *2	–	–	Unused
					CSDC2	1	Normal	All off	LCD all off control
2E0H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (2 Hz)
					TM2	0			Clock timer data (4 Hz)
	R				TM1	0			Clock timer data (8 Hz)
					TM0	0			Clock timer data (16 Hz)
2E1H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer 1/100 sec data (BCD)
	R				SWL1	0			
					SWL0	0			LSB
2E2H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer 1/10 sec data (BCD)
	R				SWH1	0			
					SWH0	0			LSB
2E3H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
	R/W				EIK01	0	Enable	Mask	
					EIK00	0	Enable	Mask	
2E6H	HLMOD	0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register (S1C60A16)
					0 *3	– *2	–	–	Unused
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial I/F clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2E8H	CSDC1	ETI2	ETI8	ETI32	CSDC1	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2EBH	R03	R02	R01	R00	R03	0	High	Low	Output port (R03)
					R02	0	High	Low	Output port (R02)
	R/W				R01	0	High	Low	Output port (R01)
					R00	0	High	Low	Output port (R00)
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
	R/W		R/W / R	R/W	R11	0	High	Low	Output port (R11)
					SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

Table 4.1.1(b) I/O memory map (2EDH–2F3H, 2F6H–2FCH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2EDH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data (P00–P03)
					P02	– *2	High	Low	
					P01	– *2	High	Low	Output latch is reset at initial reset
	R/W				P00	– *2	High	Low	
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)
2EFH	WDRST	WD2	WD1	WD0	WDRST*3	Reset	Reset	–	Watchdog timer reset
					WD2	0			Timer data (watchdog timer) 1/4 Hz
	W	R			WD1	0			Timer data (watchdog timer) 1/2 Hz
					WD0	0			Timer data (watchdog timer) 1 Hz
2F0H	SD3	SD2	SD1	SD0	SD3	× *5			Serial I/F data register (low-order 4 bits)
					SD2	× *5			
	R/W				SD1	× *5			
					SD0	× *5			
2F1H	SD7	SD6	SD5	SD4	SD7	× *5			Serial I/F data register (high-order 4 bits)
					SD6	× *5			
	R/W				SD5	× *5			
					SD4	× *5			
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			Serial I/F clock mode selection [SCS1, 0]: 0 Clock, 1 CLK, 2 CLK/2, 3 CLK/4, Slave
					SCS0	1			
	R/W				SE2	0	↑	↓	Serial I/F clock edge selection
					EISIO	0	Enable	Mask	Interrupt mask register (serial I/F)
2F3H	0	0	0	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				0 *3	– *2	–	–	Unused
					ISIO *4	0	Yes	No	Interrupt factor flag (serial I/F)
2F6H	BZFQ2	BZFQ1	BZFQ0	ENVRST	BZFQ2	0			Buzzer frequency selection [BZFQ2–0]: 0 fOSC1/8, 1 fOSC1/10, 2 fOSC1/12, 3 fOSC1/14, 4 fOSC1/16, 5 fOSC1/20, 6 fOSC1/24, 7 fOSC1/28
					BZFQ1	0			
	R/W			W	BZFQ0	0			
					ENVRST*3	Reset	Reset	–	Envelope reset
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off
2F8H	EV03	EV02	EV01	EV00	EV03	0			Event counter 0 (low-order 4 bits)
					EV02	0			
	R				EV01	0			
					EV00	0			
2F9H	EV07	EV06	EV05	EV04	EV07	0			Event counter 0 (high-order 4 bits)
					EV06	0			
	R				EV05	0			
					EV04	0			
2FAH	EV13	EV12	EV11	EV10	EV13	0			Event counter 1 (low-order 4 bits)
					EV12	0			
	R				EV11	0			
					EV10	0			
2FBH	EV17	EV16	EV15	EV14	EV17	0			Event counter 1 (high-order 4 bits)
					EV16	0			
	R				EV15	0			
					EV14	0			
2FCH	EVSEL	ENRUN	EV1RST	EV0RST	EVSEL	0	Separate	Phase	Event counter mode selection
					EVRUN	0	Run	Stop	Event counter Run/Stop
	R/W		W		EV1RST*3	Reset	Reset	–	Event counter 1 reset
					EV0RST*3	Reset	Reset	–	Event counter 0 reset

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

Table 4.1.1(c) I/O memory map (2FDH–2FFH)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2FDH	P13	P12	P11	P10	P13	– *2	High	Low	I/O port data (P10–P13) Output latch is reset at initial reset
					P12	– *2	High	Low	
					P11	– *2	High	Low	
	R/W				P10	– *2	High	Low	
2FEH	0	CLKCHG	OSCC	IOC1	0 *3	– *2	–	–	Unused
					CLKCHG	0	OSC3	OSC1	CPU clock switch
	R	R/W			OSCC	0	On	Off	OSC3 oscillation On/Off
					IOC1	0	Output	Input	I/O control register (P10–P13)
2FFH	SVDDT	0	0	0	SVDDT	0	Low	Normal	SVD evaluation data
	SVDON				SVDON	0	On	Off	SVD On/Off
	R	R			0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	W				0 *3	– *2	–	–	Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

4.2 Resetting Watchdog Timer

4.2.1 Configuration of watchdog timer

The S1C60N16 Series incorporates a watchdog timer as the source oscillator for OSC1 (clock timer 2 Hz signal). The watchdog timer must be reset cyclically by the software. If reset is not executed in at least 3 or 4 seconds, the initial reset signal is output automatically for the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

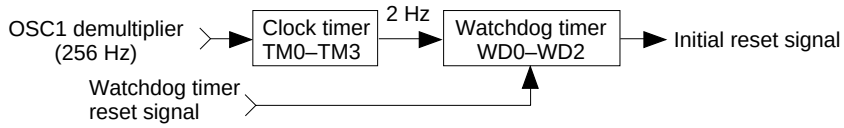


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer, configured of a three-bit binary counter (WD0–WD2), generates the initial reset signal internally by overflow of the MSB.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the halt mode. If the halt status continues for 3 or 4 seconds, the initial reset signal restarts operation.

4.2.2 Mask option

You can select whether or not to use the watchdog timer with the mask option. When "Not use" is chosen, there is no need to reset the watchdog timer.

4.2.3 Control of watchdog timer

Table 4.2.3.1 lists the watchdog timer's control bits and their addresses.

Table 4.2.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2EFH	WDRST	WD2	WD1	WD0	WDRST*3	Reset	Reset	–	Watchdog timer reset
					WD2	0			Timer data (watchdog timer) 1/4 Hz
	W	R			WD1	0			Timer data (watchdog timer) 1/2 Hz
					WD0	0			Timer data (watchdog timer) 1 Hz

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

WDRST: Watchdog timer reset (2EFH•D3)
This is the bit for resetting the watchdog timer.

When "1" is written : Watchdog timer is reset
When "0" is written : No operation
Read-out : Always "0"

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written to WDRST, no operation results.
This bit is dedicated for writing, and is always "0" for read-out.

4.2.4 Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles, and timer data (WD0–WD2) cannot be used for timer applications.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The S1C60N16 and S1C60L16 have one oscillation circuit (OSC1), and the S1C60A16 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or ceramic oscillation circuit. When processing with the S1C60A16 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3. Figure 4.3.1.1 is the block diagram of this oscillation system.

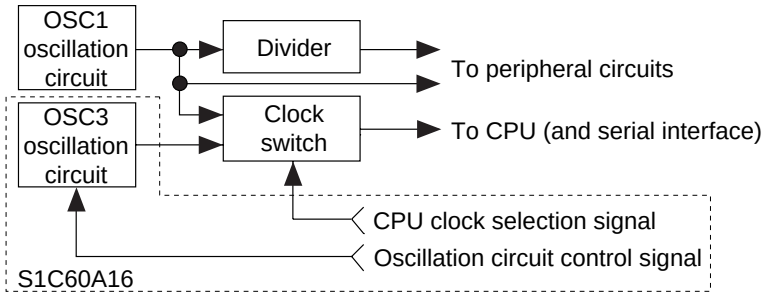


Fig. 4.3.1.1 Oscillation system

4.3.2 OSC1 oscillation circuit

The OSC1 oscillation circuit generates the main clock for the CPU and the peripheral circuits. The oscillator type is a crystal oscillation circuit and the oscillation frequency is 32.768 kHz (Typ.).
Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

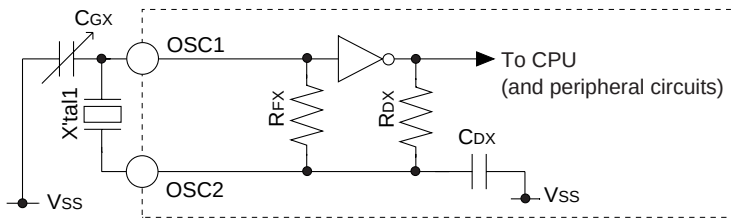
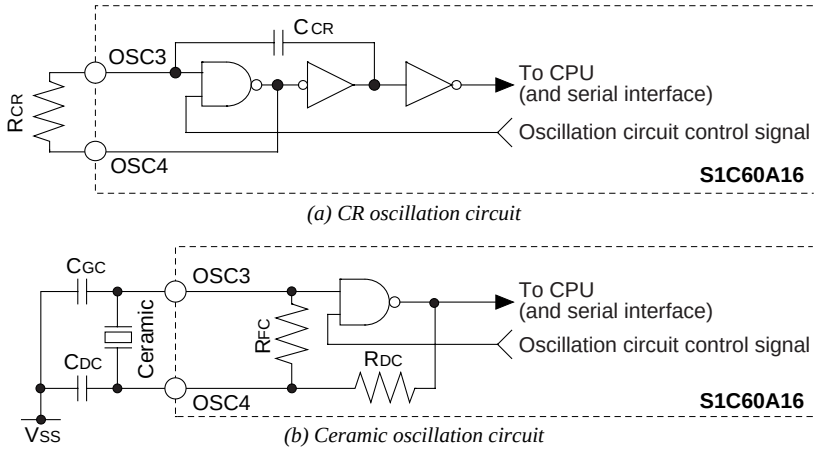


Fig. 4.3.2.1 OSC1 oscillation circuit

As shown in Figure 4.3.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal1) of 32.768 kHz (Typ.) between the OSC1 and OSC2 terminals and the trimmer capacitor (C_{GX}) between the OSC1 and V_{SS} terminals.

4.3.3 OSC3 oscillation circuit (S1C60A16)

The S1C60A16 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Typ. 1 MHz) for high speed operation and the source clock for the serial interface. The mask option enables selection of CR or ceramic oscillation circuit.
Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.



(a) CR oscillation circuit

(b) Ceramic oscillation circuit

Fig. 4.3.3.1 OSC3 oscillation circuit

As shown in Figure 4.3.3.1, the CR oscillation circuit can be configured simply by connecting the resistor RCR between the OSC3 and OSC4 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics", for resistance value of RCR.
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Typ. 1 MHz) between the OSC3 and OSC4 terminals, capacitor CGC between the OSC3 and OSC4 terminals, and capacitor CDC between the OSC4 and VSS terminals. See Chapter 7, "Electrical Characteristics", for capacitor values of CGC and CDC. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

For the S1C60N16 and S1C60L16 (single clock model), do not connect anything to terminals OSC3 and OSC4.

4.3.4 Switching the system clock (S1C60A16)

In the S1C60A16, the CPU system clock is switched to OSC1 or OSC3 by the software (CLKCHG register). When OSC3 is to be used as the CPU clock, it should be done as the following procedure using the software: turn the OSC3 oscillation ON and wait at least 5 msec for oscillation stabilization, then switch the CPU clock after waiting 5 msec or more.
When switching from OSC3 to OSC1, switch the CPU clock, then turn the OSC3 oscillation circuit off.

OSC1 → OSC3

1. Set OSCC to "1" (OSC3 oscillation ON).
2. Maintain 5 msec or more.
3. Set CLKCHG to "1" (OSC1 → OSC3).

OSC3 → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1).
2. Set OSCC to "0" (OSC3 oscillation OFF).

4.3.5 Control of oscillation circuit (S1C60A16)

Table 4.3.5.1 lists the control bits and their addresses for the oscillation circuit.

Table 4.3.5.1 Control bits of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2FEH	0	CLKCHG	OSCC	IOC1	0 *3	– *2	–	–	Unused
					CLKCHG	0	OSC3	OSC1	CPU clock switch
	R	R/W			OSCC	0	On	Off	OSC3 oscillation On/Off
					IOC1	0	Output	Input	I/O control register (P10–P13)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

OSCC: OSC3 oscillation control (2FEH•D1)

Controls oscillation ON / OFF for the OSC3 oscillation circuit. (S1C60A16 only.)

When "1" is written : The OSC3 oscillation ON
When "0" is written : The OSC3 oscillation OFF
Read-out : Valid

When it is necessary to operate the CPU of the S1C60A16 at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption.
For S1C60N16 and S1C60L16, keep OSCC set to "0".
At initial reset, OSCC is set to "0".

CLKCHG: CPU clock switch (2FEH•D2)

The CPU's operation clock is selected with this register. (S1C60A16 only.)

When "1" is written : OSC3 clock is selected
When "0" is written : OSC1 clock is selected
Read-out : Valid

When the S1C60A16's CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0". This register cannot be controlled for S1C60N16 and S1C60L16, so that OSC1 is selected no matter what the set value.
At initial reset, CLKCHG is set to "0".

4.3.6 Programming notes (S1C60A16)

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

4.4 Input Ports (K00–K03, K10)

4.4.1 Configuration of input ports

The S1C60N16 Series has five bits (4 bits + 1 bit) of general-purpose input ports. Each of the input port terminals (K00–K03, K10) provides internal pull-down resistor. Pull-down resistor can be selected for each bit with the mask option.
Figure 4.4.1.1 shows the configuration of input port.

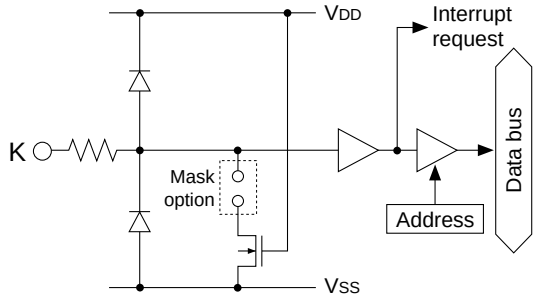


Fig. 4.4.1.1 Configuration of input port

Selection of "With pull-down resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

Further, The input port terminal K02 and K03 are used as the input terminals for the event counter. (See Section 4.12, "Event Counter", for details.)

4.4.2 Input comparison registers and interrupt function

All five bits of the input ports (K00–K03, K10) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected individually for all five bits by the software.
Figure 4.4.2.1 shows the configuration of the input interrupt circuit.

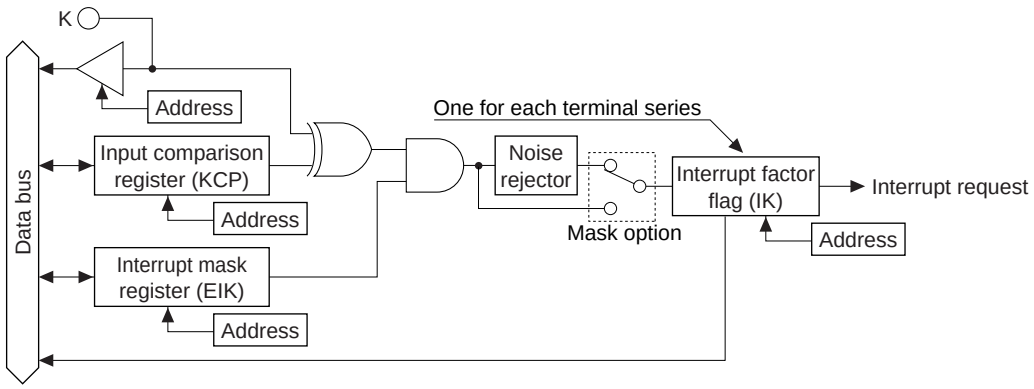


Fig. 4.4.2.1 Input interrupt circuit configuration

The input interrupt timing for K00–K03 and K10 depends on the value set for the input comparison registers (KCP00–KCP03 and KCP10). Interrupt can be selected to occur at the rising or falling edge of the input.
The interrupt mask registers (EIK00–EIK03, EIK10) enables the interrupt mask to be selected individually for K00–K03 and K10. However, whereas the interrupt function is enabled inside K00–K03, the interrupt occurs when the contents change from matching those of the input comparison register to non-matching contents. Interrupt for K10 can be generated by setting the same conditions individually.
When the interrupt is generated, the interrupt factor flag (IK0 and IK1) is set to "1".
Figure 4.4.2.2 shows an example of an interrupt for K00–K03.

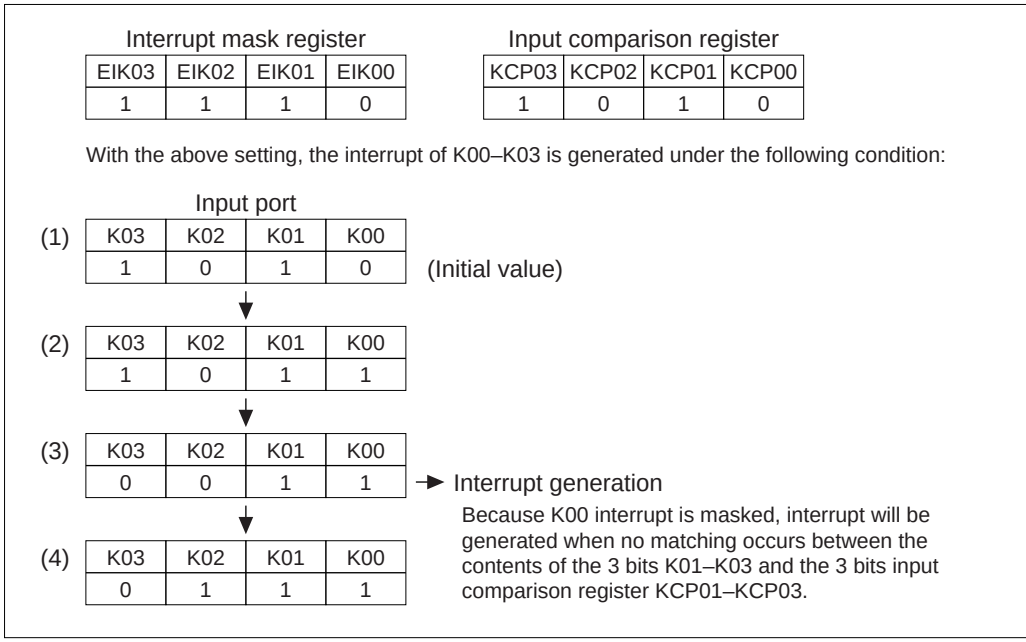


Fig. 4.4.2.2 Example of interrupt of K00–K03

K00 is masked by the interrupt mask register (EIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminal that is interrupt enabled no longer matches the data of the input comparison register, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison register from matching to nonmatching. Hence, in (4), when the nonmatching status changes to another nonmatching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.4.3 Mask option

The contents that can be selected with the input port mask option are as follows:

(1) Internal pull-down resistor can be selected for each of the five bits of the input ports (K00–K03, K10). When you have selected "Gate direct", take care that the floating status does not occur for the input. Select "With pull-down resistor" for input ports that are not being used.

(2) The input interrupt circuit contains a noise rejector for preventing interrupt occurring through noise. The mask option enables selection of whether to use the noise rejector for each separate terminal series.
When "Use" is selected, a maximum delay of 1 msec occurs from the time interrupt condition is established until the interrupt factor flag (IK) is set to "1".

4.4.4 Control of input ports

Table 4.4.4.1 lists the input ports control bits and their addresses.

Table 4.4.4.1 Input port control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E3H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
	R/W				EIK01	0	Enable	Mask	
					EIK00	0	Enable	Mask	
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial I/F clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

K00–K03, K10: Input port data (2E3H, 2E7H•D0)

Input data of the input port terminals can be read out with these registers.

When "1" is read out : High level
When "0" is read out : Low level
Writing : Invalid

The read-out is "1" when the terminal voltage of the five bits of the input ports (K00–K03, K10) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for read-out, so writing cannot be done.

KCP00–KCP03, KCP10: Input comparison registers (2E4H, 2E7H•D1)

Interrupt conditions for terminals K00–K03 and K10 can be set with these registers.

When "1" is written : Falling edge
When "0" is written : Rising edge
Read-out : Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the five bits (K00–K03 and K10), through the input comparison registers (KCP00–KCP03 and KCP10).
At initial reset, these registers are set to "0".

EIK00–EIK03, EIK10: Interrupt mask registers (2E5H, 2E7H•D2)

Masking the interrupt of the input port terminals can be selected with these registers.

When "1" is written : Enable
When "0" is written : Mask
Read-out : Valid

With these registers, masking of the input port bits can be selected for each of the five bits.
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are all set to "0".

IK0, IK1: Interrupt factor flags (2EAH•D2 and D3)

These flags indicate the occurrence of input interrupt.

When "1" is read out : Interrupt has occurred
When "0" is read out : Interrupt has not occurred
Writing : Invalid

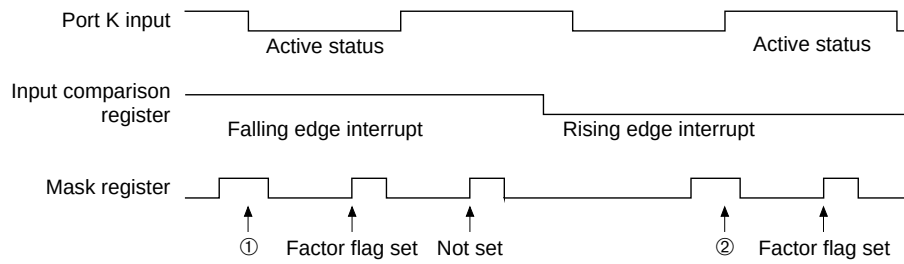
The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
These flags are reset when the software reads them. Read-out can be done only in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

4.4.5 Programming notes

(1) When input ports are changed from high to low by pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When "Use" is selected with the noise rejector mask option, a maximum delay of 1 msec occurs from time the interrupt conditions are established until the interrupt factor flag (IK) is set to "1" (until the interrupt is actually generated). Hence, pay attention to the timing when reading out (resetting) the interrupt factor flag. For example, when performing a key scan with the key matrix, the key scan changes the input status to set the interrupt factor flag, so it has to be read out to reset it. However, if the interrupt factor flag is read out immediately after key scanning, the delay will cause the flag to be set after read-out, so that it will not be reset.

(3) Input interrupt programming related precautions



When the content of the mask register is rewritten while the port K input is in the active status, the input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 4.4.5.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set.
Therefore, when using the input interrupt, the active status of the input terminal implies
input terminal = low status, when the falling edge interrupt is effected and
input terminal = high status, when the rising edge interrupt is effected.
When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 4.4.5.1. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 4.4.5.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the low status.
In addition, when the mask register = "1" and the content of the input comparison register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input comparison register in the mask register = "0" status.

(4) Read out the interrupt factor flag (IK) only in the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

(5) Write the interrupt mask register (EIK) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.5 Output Ports (R00–R03, R10–R13)

4.5.1 Configuration of output ports

The S1C60N16 Series has eight bits (4 bits × 2) of general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and Pch open drain output.
Further, the mask option enables the output ports R10–R13 to be used as special output ports.
Figure 4.5.1.1 shows the configuration of the output ports.

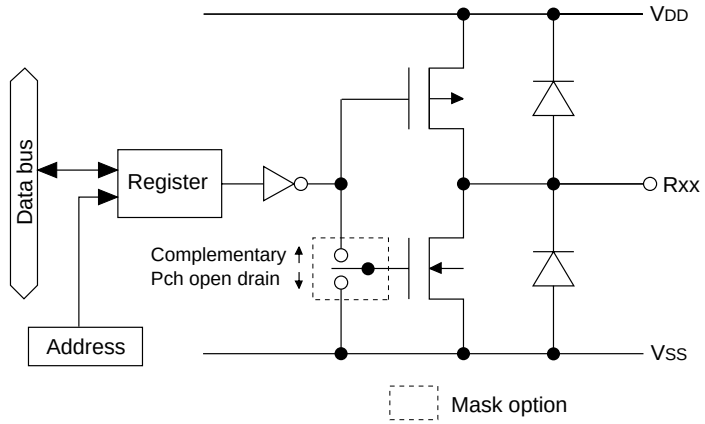


Fig. 4.5.1.1 Configuration of output ports

4.5.2 Mask option

The mask option enables the following output port selection.

(1) Output specifications of output ports

Output specifications for the output ports (R00–R03, R10–R13) enable selection of either complementary output or Pch open drain output for each of the eight bits.
However, even when Pch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.

(2) Special output

In addition to the regular DC output, special output can be selected for the output ports R10–R13 as shown in Table 4.5.2.1. Figure 4.5.2.1 shows the structure of the output ports R10–R13.

Table 4.5.2.1 Special output

Output port	Special output
R10	BZ output
R13	$\overline{BZ}$ output (selectable only when R10 is used as BZ output)
R11	SIOF output
R12	FOUT output

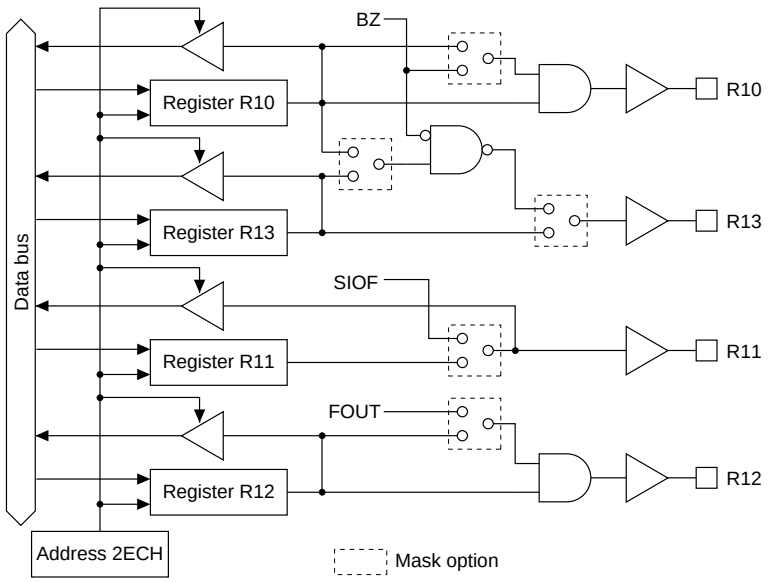


Fig. 4.5.2.1 Structure of output port R10–R13

BZ, $\overline{BZ}$ (R10, R13)

BZ and $\overline{BZ}$ are the buzzer signal output for driving the piezoelectric buzzer. The buzzer signal is generated by demultiplicaion of fOSC1. The buzzer signal frequency can be selected by software. Also, a digital envelope can be added to the buzzer signal. See Section 4.11, "Sound Generator", for details.

Notes: • When the BZ and $\overline{BZ}$ output signals are turned ON or OFF, a hazard can result.
• When DC output is set for the output port R10, the output port R13 cannot be set for $\overline{BZ}$ output.

Figure 4.5.2.2 shows the output waveform for BZ and $\overline{BZ}$.

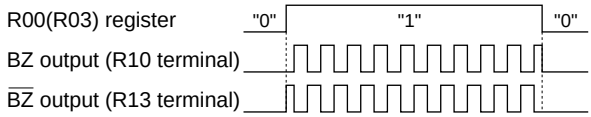


Fig. 4.5.2.2 Output waveform of BZ and $\overline{BZ}$

SIOF (R11)

When the output port R11 is set for SIOF output, it outputs the signal indicating the running status (RUN / STOP) of the serial interface. See Section 4.7, "Serial Interface", for details.

FOUT (R12)

When the output port R12 is set for FOUT output, it outputs the clock of fOSC1 or the demultiplied fOSC1. The clock frequency is selectable with the mask options, from the frequencies listed in Table 4.5.2.2.

Table 4.5.2.2 FOUT clock frequency

Setting value	Clock frequency (Hz) *
fOSC1 / 1	32,768
fOSC1 / 2	16,384
fOSC1 / 4	8,192
fOSC1 / 8	4,096
fOSC1 / 16	2,048
fOSC1 / 32	1,024
fOSC1 / 64	512
fOSC1 / 128	256

∗ When fOSC1 = 32.768 kHz

Note: A hazard may occur when the FOUT signal is turned ON or OFF.

4.5.3 Control of output ports

Table 4.5.3.1 lists the output ports' control bits and their addresses.

Table 4.5.3.1 Control bits of output ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2EBH	R03	R02	R01	R00	R03	0	High	Low	Output port (R03)
					R02	0	High	Low	Output port (R02)
	R/W				R01	0	High	Low	Output port (R01)
					R00	0	High	Low	Output port (R00)
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
					R11	0	High	Low	Output port (R11)
	R/W		R/W / R	R/W	SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

R00–R03, R10–R13 (when DC output): Output port data (2EBH, 2ECH)

Sets the output data for the output ports.

When "1" is written : High output
When "0" is written : Low output
Read-out : Valid

The output port terminals output the data written in the corresponding registers (R00–R03, R10–R13) without changing it. When "1" is written in the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
At initial reset, all registers are set to "0".

R10, R13 (when BZ and $\overline{BZ}$ output is selected): Buzzer output control (2ECH•D0 and D3)

These bits control the output of the buzzer signals (BZ, $\overline{BZ}$).

When "1" is written : Buzzer signal is output
When "0" is written : Low level (DC) is output
Read-out : Valid

$\overline{BZ}$ is output from terminal R13. With the mask option, selection can be made perform this output control by R13, or to perform output control simultaneously with BZ by R10.

- ***When R13 controls $\overline{BZ}$ output***

  BZ output and $\overline{BZ}$ output can be controlled independently. BZ output is controlled by writing data to R10, and $\overline{BZ}$ output is controlled by writing data to R13.

- ***When R10 controls $\overline{BZ}$ output***

  BZ output and $\overline{BZ}$ output can be controlled simultaneously by writing data to R10 only. For this case, R13 can be used as a one-bit general register having both read and write functions, and data of this register exerts no affect on $\overline{BZ}$ output (output from the R13 pin).

At initial reset, registers R10 and R13 are set to "0".

R11 (when SIOF output is selected): Serial interface status (2ECH•D1)

Indicates the running status of the serial interface.

When "1" is read out : RUN
When "0" is read out : STOP
Writing : Valid

See Section 4.7, "Serial Interface", for details of SIOF.
This bit is exclusively for reading out, so data cannot be written to it.

R12 (when FOUT is selected): FOUT output control (2ECH•D2)
Controls the FOUT (clock) output.

When "1" is written : Clock output
When "0" is written : Low level (DC) output
Read-out : Valid

FOUT output can be controlled by writing data to R12.
At initial reset, this register is set to "0".

4.5.4 Programming note

When BZ, $\overline{BZ}$ and FOUT are selected with the mask option, a hazard may be observed in the output waveform when the data of the output register changes.

4.6 I/O Ports (P00–P03, P10–P13)

4.6.1 Configuration of I/O ports

The S1C60N16 Series has eight bits (4 bits × 2) of general-purpose I/O ports. Figure 4.6.1.1 shows the configuration of the I/O ports.
The four bits of each of the I/O ports P00–P03 and P10–P13 can be set to either input mode or output mode. Modes can be set by writing data to the I/O control register.

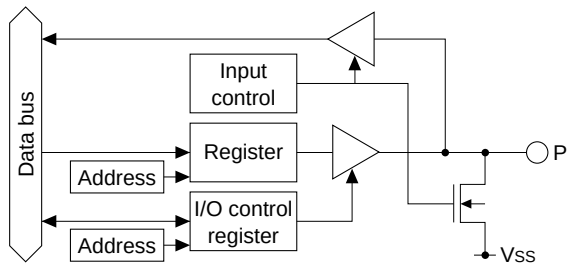


Fig. 4.6.1.1 Configuration of I/O port

The P10–P12 I/O port terminals are shared with the serial interface input/output terminals and the serial interface is enabled by mask option.

4.6.2 Mask option

(1) Output specification

The output specification during output mode (IOC = "1") of these I/O ports can be set with the mask option for either complementary output or Pch open drain output. This setting can be performed for each bit of each port.
However, when Pch open drain output has been selected, voltage in excess of the power voltage must not be applied to the port.

(2) Serial interface

The serial interface can be enabled by mask option. When the serial interface is enabled, the P10, P11 and P12 terminals are used as the serial I/O port.

4.6.3 I/O control register and I/O mode

Input or output mode can be set for the four bits of I/O port P00–P03 and I/O port P10–P13 by writing data into the corresponding I/O control register IOC0 and IOC1.

To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, the input line is pulled down when input data is read.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high signal (V_{DD}) when the port output data is "1", and a low signal (V_{SS}) when the port output data is "0".

At initial reset, the I/O control registers are set to "0", and the I/O port enters the input mode.

When the serial interface is used, the IOC1 register controls only the P13 port.

4.6.4 Control of I/O ports

Table 4.6.4.1 lists the I/O ports' control bits and their addresses.

Table 4.6.4.1 I/O port control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2EDH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data (P00–P03)
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	Output latch is reset at initial reset
					P00	– *2	High	Low	
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)
2FDH	P13	P12	P11	P10	P13	– *2	High	Low	I/O port data (P10–P13)
					P12	– *2	High	Low	
	R/W				P11	– *2	High	Low	Output latch is reset at initial reset
					P10	– *2	High	Low	
2FEH	0	CLKCHG	OSCC	IOC1	0 *3	– *2	–	–	Unused
					CLKCHG	0	OSC3	OSC1	CPU clock switch
	R	R/W			OSCC	0	On	Off	OSC3 oscillation On/Off
					IOC1	0	Output	Input	I/O control register (P10–P13)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

P00–P03, P10–P13: I/O port data (2EDH, 2FDH)

I/O port data can be read and output data can be set through these ports.

When writing data

When "1" is written : High level
When "0" is written : Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}).
Port data can be written also in the input mode.

When reading data out

When "1" is read out : High level
When "0" is read out : Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the output voltage level can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
Further, the built-in pull-down resistance goes ON during read-out, so that the I/O port terminal is pulled down.

The data registers of the ports (P10–P12) that are set as input/output for the serial interface can be used as general purpose registers that do not affect the input/output.

Notes: • *When the I/O port is set to the output mode and a low-impedance load is connected to the port terminal, the data written to the register may differ from the data read out.*

• *When the I/O port is set to the input mode and a low-level voltage (V_{SS}) is input, erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-down resistance load is greater than the read-out time. When the input data is being read out, the time that the input line is pulled down is equivalent to 1.5 cycles of the CPU system clock. However, the electric potential of the terminals must be settled within 0.5 cycles. If this condition cannot be fulfilled, some measure must be devised such as arranging pull-down resistance externally, or performing multiple read-outs.*

IOC0, IOC1: I/O control registers (2EEH•D0, 2FEH•D0)

The input and output modes of the I/O ports can be set with these registers.

When "1" is written : Output mode
When "0" is written : Input mode
Read-out : Valid

The input and output modes of the I/O ports are set in units of four bits. IOC0 sets the mode for P00–P03, and IOC1 sets the mode for P10–P13.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these two registers are set to "0", so the I/O ports are in the input mode.
When the serial interface is used, the IOC1 register controls only the P13 port.

4.6.5 Programming notes

(1) When input data are changed from high to low by built-in pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Consequently, if data is read out while the CPU is running in the OSC3 oscillation circuit, data must be read out continuously for about 500 µsec.

(2) When the I/O port is set to the output mode and the data register has been read, the terminal data instead of the register data can be read out. Because of this, if a low-impedance load is connected and read-out performed, the value of the register and the read-out result may differ.

4.7 Serial Interface

4.7.1 Configuration of serial interface

The S1C60N16 Series has a built-in synchronous clock type 8 bits serial interface that can be enabled by mask option. The configuration of the serial interface is shown in Figure 4.7.1.1.
The CPU, via the 8 bits shift register, can read the serial input data from the SIN (P10) terminal. Moreover, via the same 8 bits shift register, it can convert parallel data to serial data and output it to the SOUT (P11) terminal. The synchronous clock for serial data input/output may be set by selecting by software any one of 3 types of master mode (internal clock mode: when the S1C60N16 Series is to be the master for serial input/output) and a type of slave mode (external clock mode: when the S1C60N16 Series is to be the slave for serial input/output).
Furthermore, the R11 output port can be configured to output the SIOF signal, which indicates whether the serial interface in master or slave mode is ready to transmit/receive or not, by mask option. Also this option enables the SIOF (2ECH•D1) bit that indicates the serial interface operating status.

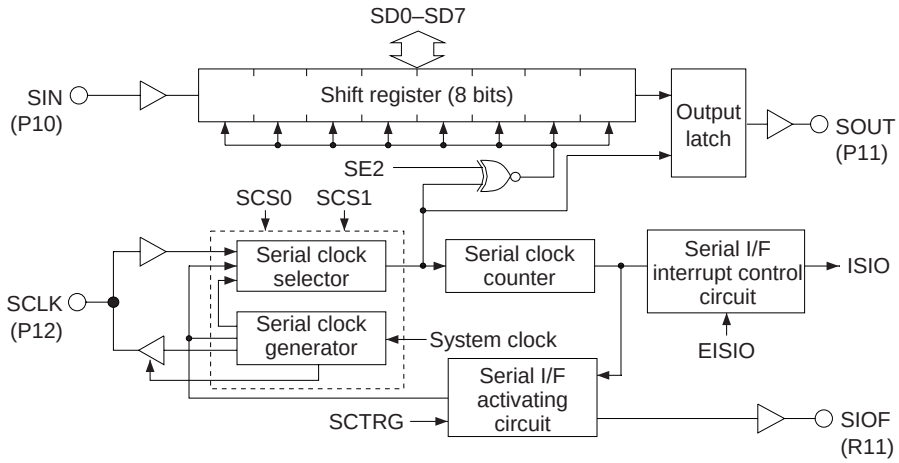


Fig. 4.7.1.1 Configuration of serial interface

The SIN (P10) and SCLK (P12) terminals have a pull-down resistor. However, the SCLK (P12) terminal is pulled down to low in external clock mode and the pull-down resistor is disabled in internal clock mode.

4.7.2 Mask option

The serial interface may be selected for the following by mask option.

(1) Whether the serial interface is used or not may be selected. When "use" is selected, the following I/O port terminals are configured as the serial I/O terminals.
P10 → SIN (data input)
P11 → SOUT (data output)
P12 → SCLK (clock input/output)

(2) Either complementary output or Pch open drain as output specification for the SOUT (P11) terminal may be selected. However, even if Pch open drain has been selected, application of voltage exceeding power source voltage to the SOUT (P11) terminal will be prohibited.

(3) As output specification during output mode, either complementary output or Pch open drain output may be selected for the SCLK (P12) terminal.

(4) Positive or negative logic can be selected for the signal logic of the SIO function. However, keep in mind that only pull-down resistance can be set for the input mode (pull-up resistance is not built-in).

(5) LSB first or MSB first as input/output permutation of serial data may be selected in the SIO function.

(6) The output port R11 (see Section 4.5, "Output Ports") can be configured as the SIOF signal output port to notify the external serial device whether the internal serial interface is ready to transmit/receive data or not. Also this option switches the function of the R11 output port data bit (2ECH•D1) to indicate the SIOF signal. When this option is selected, the R11 terminal cannot be used as a general-purpose output port and the R11 port data bit (2ECH•D1) cannot be used for setting the output signal.

4.7.3 Master mode and slave mode of serial interface

The serial interface of the S1C60N16 Series has two types of operation mode: master mode and slave mode.
In the master mode, it uses an internal clock as synchronous clock of the built-in shift register, generates this internal clock at the SCLK (P12) terminal and controls the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the SCLK (P12) terminal and uses it as the synchronous clock to the built-in shift register.
The master mode and slave mode are selected by writing data to registers SCS1 and SCS0 (address 2F2H•D2, D3).
When the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 4.7.3.1.

Table 4.7.3.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
0	0	Master mode	CLK
0	1		CLK/2
1	0		CLK/4
1	1	Slave mode	External clock

CLK: CPU system clock

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8 bits serial data, is controlled as follows:

- At master mode, after output of 8 clocks from the SCLK (P12) terminal, clock output is automatically suspended and SCLK (P12) terminal is fixed at low level.
- At slave mode, after input of 8 clocks to the SCLK (P12) terminal, subsequent clock inputs are masked.

Note: When using the serial interface in the master mode, CPU system clock is used as the synchronous clock. Accordingly, when the serial interface is operating, system clock switching ($f_{OSC1} \leftrightarrow f_{OSC3}$) should not be performed.

A sample basic serial input/output portion connection is shown in Figure 4.7.3.1.

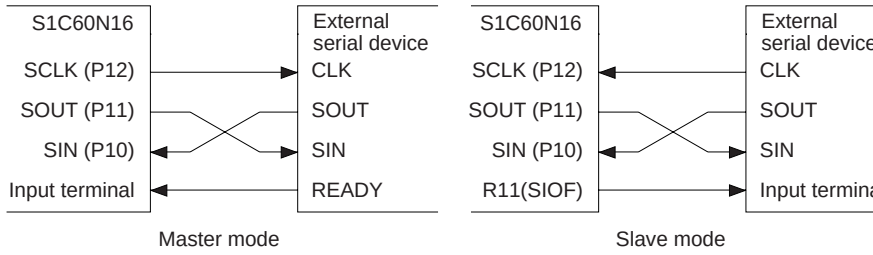


Fig. 4.7.3.1 Sample basic connection

4.7.4 Data input/output and interrupt function

The serial interface can input / output data via the internal 8 bits shift register. The shift register operates by synchronizing with either the synchronous clock output from SCLK (P12) terminal (master mode), or the synchronous clock input to SCLK (P12) (slave mode).
The serial interface generates interrupt on completion of the 8 bits serial data input / output. Detection of serial data input / output is done by the counting of the synchronous clock (SCLK); the clock completes input / output operation when 8 counts (equivalent to 8 cycles) have been made and then generates interrupt.
The serial data input / output procedure data is explained below:

(1) Serial data output procedure and interrupt

The serial interface is capable of outputting parallel data as serial data, in units of 8 bits.
By setting the parallel data to 4 bits registers SD0–SD3 (address 2F0H) and SD4–SD7 (address 2F1H) individually and writing "1" to SCTRG bit (address 2E7H·D3), it synchronizes with the synchronous clock and serial data is output at the SOUT (P11) terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK (P12) terminal while in the slave mode, external clock which is input from the SCLK (P12) terminal. The serial output of the SOUT (P11) terminal changes with the rising edge of the clock that is input or output from the SCLK (P12) terminal.
The serial data to the built-in shift register is shifted with the rising edge of the SCLK signal when SE2 bit (address 2F2H • D1) is "1" and is shifted with the falling edge of the SCLK signal when SE2 bit (address 2F2H • D1) is "0".
When the output of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO (address 2F3H • D0) is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO (address 2F2H • D0).

(2) Serial data input procedure and interrupt

The serial interface is capable of inputting serial data as parallel data, in units of 8 bits.
The serial data is input from the SIN (P10) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8 bits shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK (P12) terminal while in the slave mode, external clock which is input from the SCLK (P12) terminal.
The serial data to the built-in shift register is read with the rising edge of the SCLK signal when SE2 bit is "1" and is read with the falling edge of the SCLK signal when SE2 bit is "0". Moreover, the shift register is sequentially shifted as the data is fetched.
When the input of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after input of the 8 bits data.
The data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

The S1C60N16 Series allows the input / output permutation of serial data to be selected by mask option as to either LSB first or MSB first. The block diagram showing input / output permutation in case of LSB first and MSB first is provided in Figure 4.7.4.1.

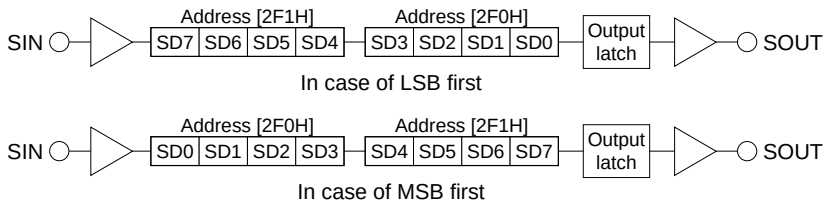


Fig. 4.7.4.1 Serial data input/output permutation

(4) SIOF signal

The SIOF signal can be output from the R11 terminal regardless of the set mode, master or slave, by mask option.

For example, when the serial interface is used in slave mode (external clock mode), the SIOF signal is used to notify the master (external) serial device whether the internal serial interface is ready to transmit / receive data or not. In master mode, the serial interface operating status can be checked by reading the status bit SIOF (2ECH • D1).

The SIOF signal and the SIOF bit (2ECH • D1) go "1" (high) when the S1C60N16 serial interface becomes ready to transmit / receive data; normally they are "0" (low).

The SIOF signal and the SIOF bit (2ECH • D1) change from "0" to "1" immediately after "1" is written to the SCTRG bit and return from "1" to "0" when eight synchronous clocks (eight cycles) have been counted.

(5) Timing chart

The serial interface timing chart is shown in Figure 4.7.4.2.

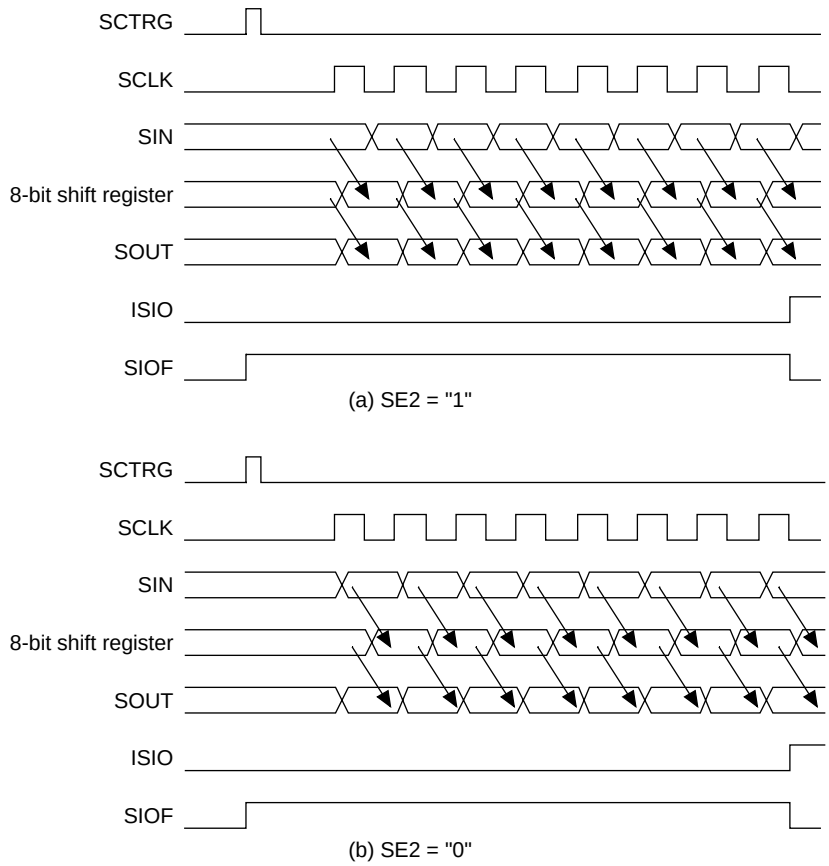


Fig. 4.7.4.2 Serial interface timing chart

4.7.5 Control of serial interface

The control registers for the serial interface are explained below.

Table 4.7.5.1 Control bits of serial interface

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E7H	SCTRG	IK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial I/F clock trigger
					EIK0	0	Enable	Mask	Interrupt mask register (K10)
					KCP10	0	↓	↑	Input comparison register (K10)
	W	R/W		R	K10	– *2	High	Low	Input port data (K10)
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
					R11	0	High	Low	Output port (R11)
	R/W		R/W / R	R/W	SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/On	Output port (R10)/BZ output control
2F0H	SD3	SD2	SD1	SD0	SD3	× *5			Serial I/F data register (low-order 4 bits)
					SD2	× *5			
					SD1	× *5			
	R/W				SD0	× *5			
2F1H	SD7	SD6	SD5	SD4	SD7	× *5			Serial I/F data register (high-order 4 bits)
					SD6	× *5			
					SD5	× *5			
	R/W				SD4	× *5			
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			Serial I/F clock mode selection [SCS1, 0]: 0 Clock, 1 CLK, 2 CLK/2, 3 CLK/4, Slave
					SCS0	1			
					SE2	0	↑	↓	Serial I/F clock edge selection
	R/W				EISIO	0	Enable	Mask	Interrupt mask register (serial I/F)
2F3H	0	0	0	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				ISIO *4	0	Yes	No	Interrupt factor flag (serial I/F)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

SD0–SD3, SD4–SD7: Serial interface data registers (2F0H, 2F1H)

These registers are used for writing and reading serial data.

During writing operation

When "1" is written : High level
When "0" is written : Low level

Writes serial data will be output to SOUT (P11) terminal. From the SOUT (P11) terminal, the data converted to serial data as high (V_{DD}) level bit for bits set at "1" and as low (V_{SS}) level bit for bits set at "0".

During reading operation

When "1" is read out : High level
When "0" is read out : Low level

The serial data input from the SIN (P10) terminal can be read by this register.
The data converted to parallel data, as high (V_{DD}) level bit "1" and as low (V_{SS}) level bit "0" input from SIN (P10) terminal. Perform data reading only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers will be undefined.

SCS1, SCS0: Clock mode selection register (2F2H•D3, D2)

Selects the synchronous clock for the serial interface (SCLK).

Table 4.7.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
0	0	Master mode	CLK
0	1		CLK/2
1	0		CLK/4
1	1	Slave mode	External clock

CLK: CPU system clock

Synchronous clock (SCLK) is selected from among the above 4 types: 3 types of internal clock and external clock.
At initial reset, external clock is selected.

SE2: Clock edge selection register (2F2H•D1)

Selects the timing for reading in the serial data input.

When "1" is written : Rising edge of SCLK
When "0" is written : Falling edge of SCLK
Read-out : Valid

Selects whether the fetching for the serial input data to registers (SD0–SD7) at the rising edge (at "1" writing) or falling edge (at "0" writing) of the SCLK signal.
Pay attention if the synchronous clock goes into reverse phase (SCLK → $\overline{\text{SCLK}}$) through the mask option.

SCLK rising = $\overline{\text{SCLK}}$ falling, SCLK falling = $\overline{\text{SCLK}}$ rising

When the internal clock is selected as the synchronous clock (SCLK), a hazard occurs in the synchronous clock (SCLK) when data is written to register SE2.
The input data fetching timing may be selected but output timing for output data is fixed at SCLK rising edge.
At initial reset, falling edge of SCLK (SE2 = "0") is selected.

EISIO: Interrupt mask register (2F2H•D0)

This is the interrupt mask register of the serial interface.

When "1" is written : Enabled
When "0" is written : Masked
Read-out : Valid

At initial reset, this register is set to "0" (mask).

ISIO: Interrupt factor flag (2F3H•D0)

This is the interrupt factor flag of the serial interface.

When "1" is read out : Interrupt has occurred
When "0" is read out : Interrupt has not occurred
Writing : Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
The interrupt factor flag is reset when it has been read out.
Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8 bits data input/output.
Be sure that the interrupt factor flag reading is done with the interrupt in the DI status (interrupt flag = "0").
At initial reset, this flag is set to "0".

SCTRG: Clock trigger (2E7H•D3)

This is a trigger to start input / output of synchronous clock.

When "1" is written : Trigger
When "0" is written : No operation
Read-out : Always "0"

When this trigger is supplied to the serial interface activating circuit, the synchronous clock (SCLK) input / output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing / reading on data registers SD0–SD7.)
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

SIOF (R11): Serial interface status (2ECH•D1)

Indicates the running status of the serial interface.

When "1" is read out : RUN status
When "0" is read out : STOP status
Writing : Invalid

The RUN status is indicated from immediately after "1" is written to SCTRG bit through to the end of serial data input / output.
The SIOF read only bit can be used only when the R11 port is configured for SIOF output by mask option.

4.7.6 Programming notes

(1) If the bit data of SE2 changes while the serial interface is in the master mode, a hazard will be output to the SCLK (P12) terminal. If this poses a problem for the system, be sure to set the SCLK to the external clock if the bit data of SE2 is to be changed.

(2) Be sure that read-out of the interrupt factor flag (ISIO) is done only when the serial port is in the STOP status (SIOF = "0") and the DI status (interrupt flag = "0"). If read-out is performed while the serial data is in the RUN status (during input or output), the data input or output will be suspended and the initial status resumed. Read-out during the EI status (interrupt flag = "1") causes malfunctioning.

(3) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(4) Perform data writing / reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(5) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing / reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(6) Be sure that writing to the interrupt mask register is done only in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause malfunction.

4.8 LCD Driver (COM0–COM3, SEG0–SEG37)

4.8.1 Configuration of LCD driver

The S1C60N16 Series has four common terminals and 38 (SEG0–SEG37) segment terminals, so that an LCD with a maximum of 152 (38 × 4) segments can be driven. The power for driving the LCD is generated by the internal circuit, so there is no need to supply power externally.
The driving method is 1/4 duty (or 1/3, 1/2 duty is selectable by mask option) dynamic drive, adopting the four types of potential (1/3 bias), V_{SS}, V_{C1}, V_{C2} and V_{C3}. In the S1C60A16, the 1/2 bias dynamic drive that uses three types of potential, V_{SS}, V_{C1} = V_{C2} and V_{C3}, can be selected by setting the mask option (drive duty can also be selected from 1/4, 1/3 or 1/2).
1/2 bias drive is effective when the LCD system voltage regulator is not used. The V_{C1} terminal and the V_{C2} terminal should be connected outside the IC.
The frame frequency is 32 Hz for 1/4 duty and 1/2 duty, and 42.7 Hz for 1/3 duty (in the case of f_{OSC1} = 32.768 kHz).
Figures 4.8.1.1 to 4.8.1.6 show the drive waveform for each duty and bias.

Note: "f_{OSC1}" indicates the oscillation frequency of the oscillation circuit.

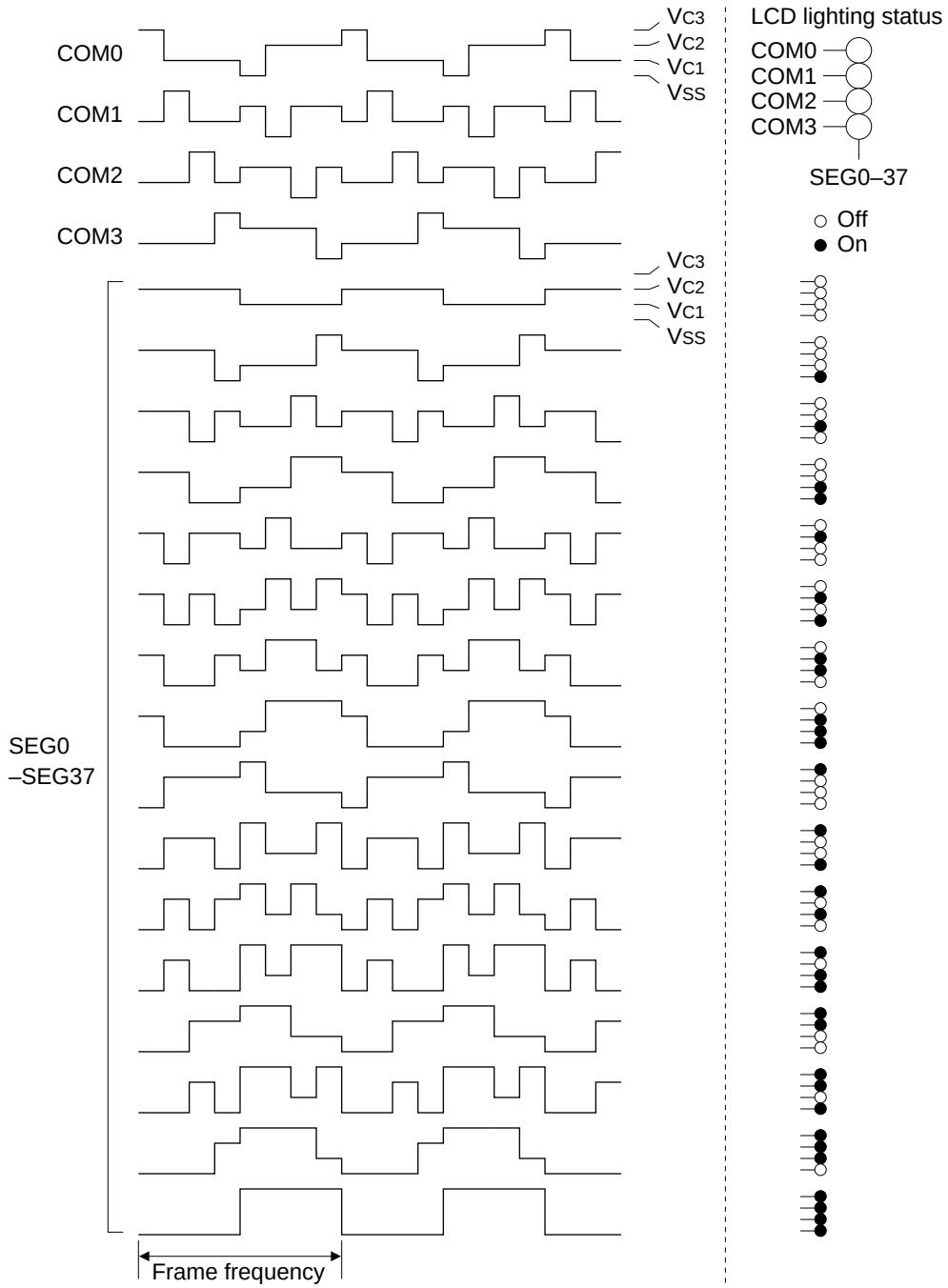


Fig. 4.8.1.1 Drive waveform for 1/4 duty (1/3 bias)

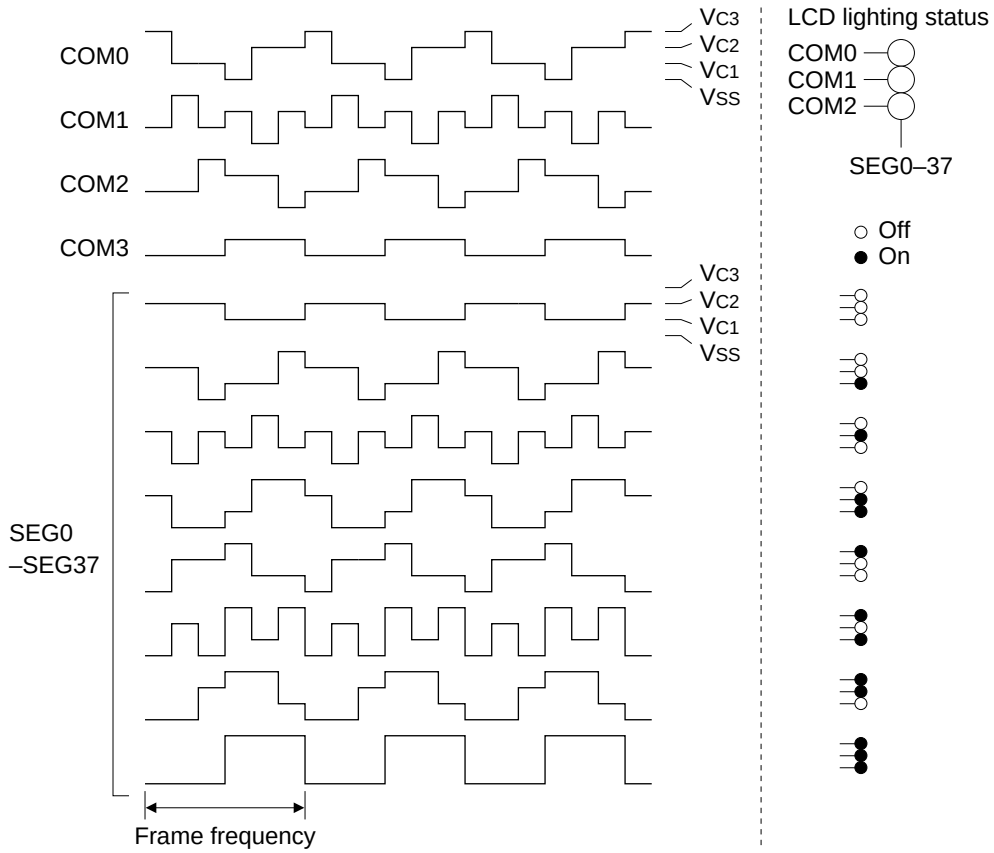


Fig. 4.8.1.2 Drive waveform for 1/3 duty (1/3 bias)

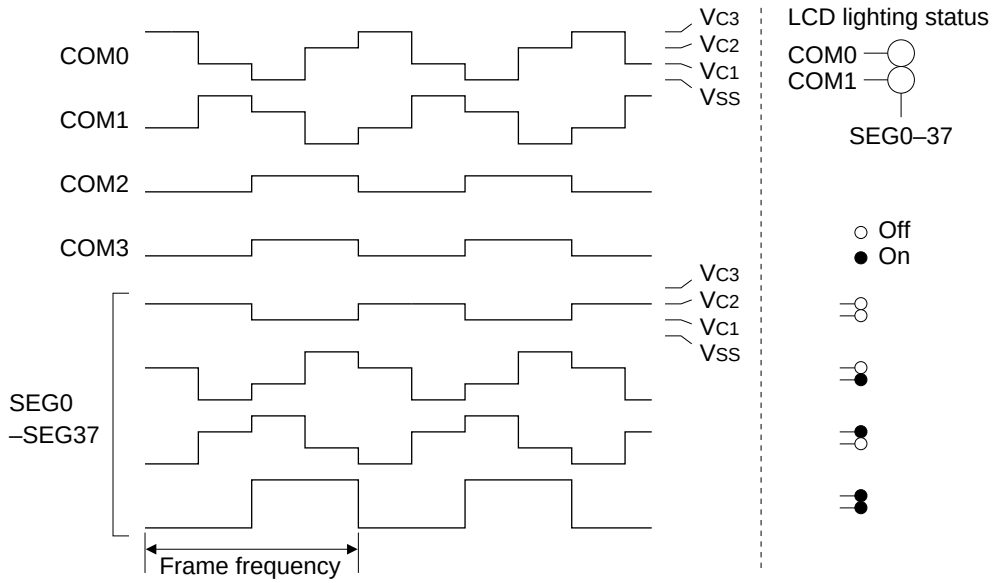


Fig. 4.8.1.3 Drive waveform for 1/2 duty (1/3 bias)

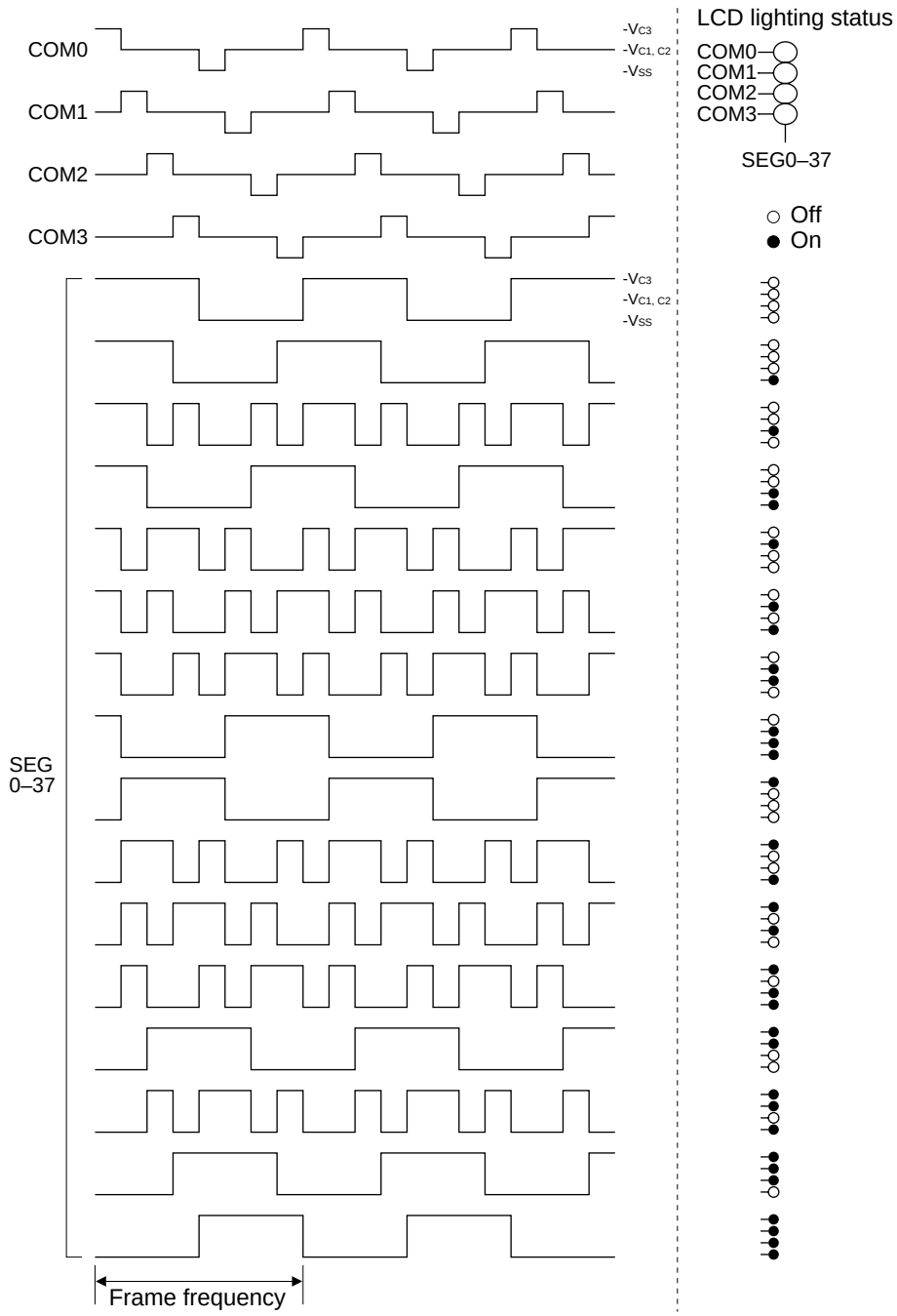


Fig. 4.8.1.4 Drive waveform for 1/4 duty (1/2 bias)

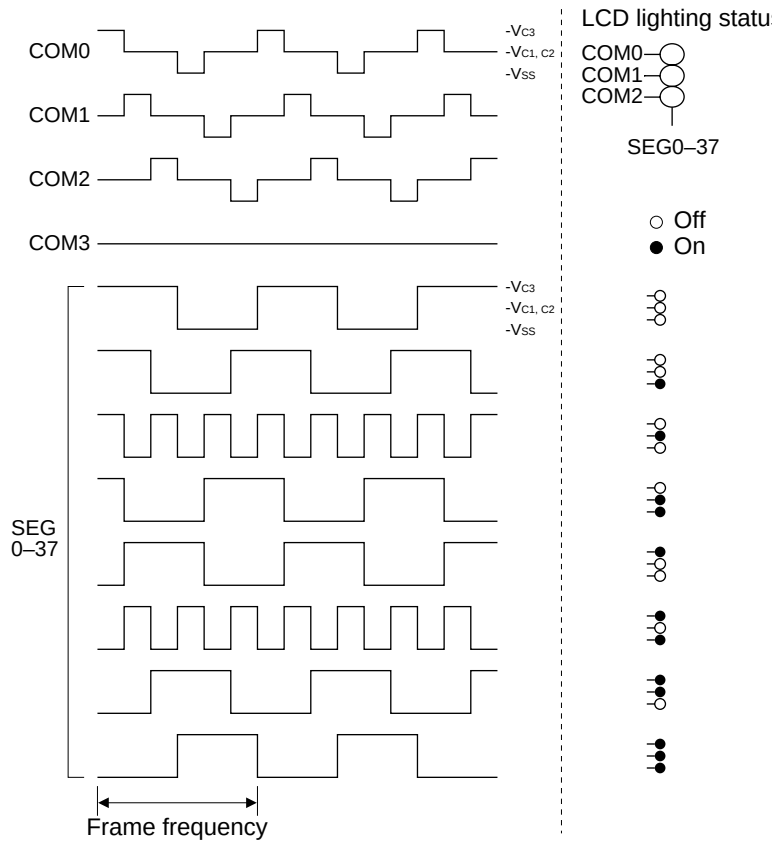


Fig. 4.8.1.5 Drive waveform for 1/3 duty (1/2 bias)

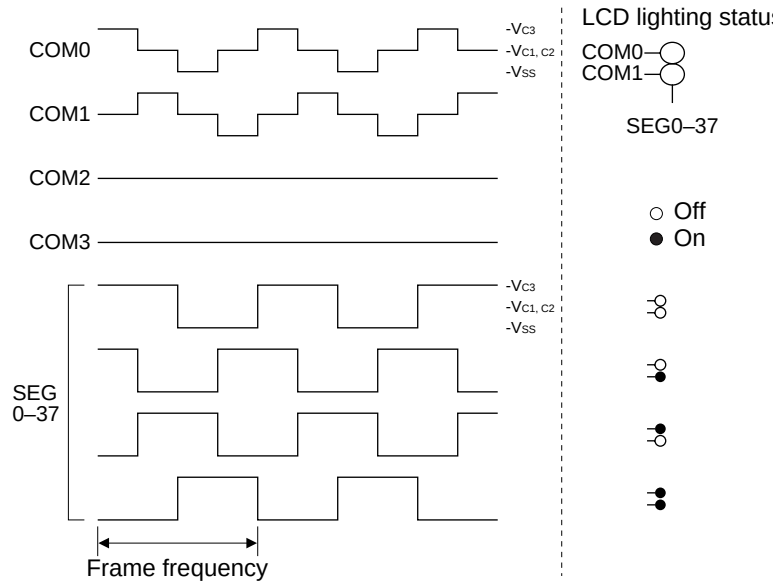


Fig. 4.8.1.6 Drive waveform for 1/2 duty (1/2 bias)

4.8.2 Cadence adjustment of oscillation frequency

In the S1C60N16 Series, the LCD drive duty can be set to 1/1 duty by software. This function enables easy adjustment (cadence adjustment) of the oscillation frequency of the oscillation circuit.
The procedure to set to 1/1 duty drive is as follows:

① Write "1" to the CSDC1 register at address 2E8H • D3.

② Write the same value to all registers corresponding to COMs 0 through 3 of the display memory.

The frame frequency is 32 Hz (f_{OSC1} / 1,024, when f_{OSC1} = 32.768 kHz).

Notes: • *Even when l/3 or 1/2 duty is selected by the mask option, the display data corresponding to all COM are valid during 1/1 duty driving. Hence, for 1/1 duty drive, set the same value for all display memory corresponding to COMs 0 through 3.*

• *For cadence adjustment, set the display data corresponding to COMs 0 through 3, so that all the LCD segments go on.*

Figures 4.8.2.1 and 4.8.2.2 show the 1/1 duty drive waveform in 1/3 bias and 1/2 bias driving.

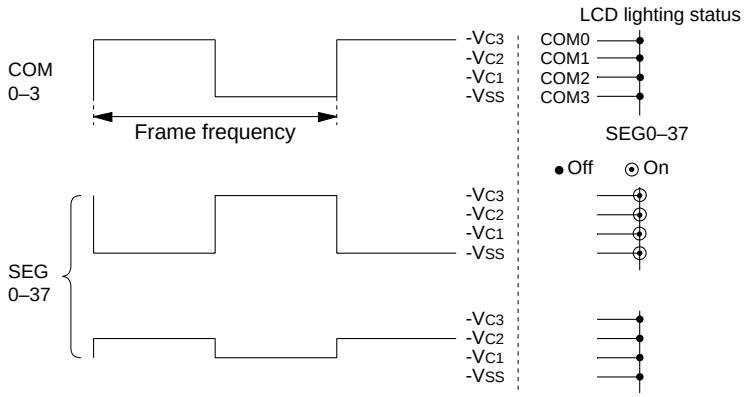


Fig. 4.8.2.1 Drive waveform for 1/1 duty (1/3 bias)

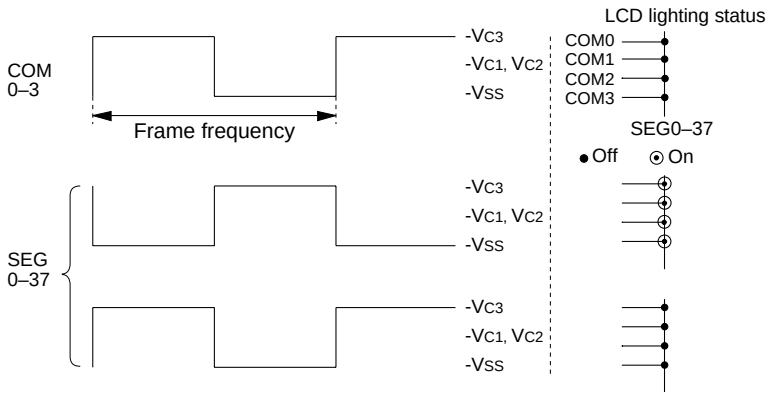


Fig. 4.8.2.2 Drive waveform for 1/1 duty (1/2 bias)

4.8.3 Mask option (segment allocation)

(1) Segment allocation

As shown in Figure 4.1.2, segment data of the S1C60N16 Series is decided depending on display data written to the display memory at address 040H–065H (Page 0) or 240H–265H (Page 2).

- The mask option enables the display memory to be allocated entirely to either Page 0 or Page 2.
- The address and bits of the display memory can be made to correspond to the segment terminals (SEG0–SEG37) in any form through the mask option. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.8.3.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory (when page 0 is selected) for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
09AH	d	c	b	a
09BH	p	g	f	e
09CH	d'	c'	b'	a'
09DH	p'	g'	f'	e'

Display data memory allocation

	Common 0	Common 1	Common 2
SEG10	9A, D0 (a)	9B, D1 (f)	9B, D0 (e)
SEG11	9A, D1 (b)	9B, D2 (g)	9A, D3 (d)
SEG12	9D, D1 (f')	9A, D2 (c)	9B, D3 (p)

Pin address allocation

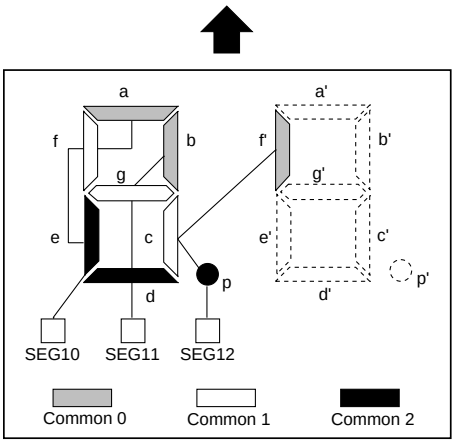


Fig. 4.8.3.1 Segment allocation

(2) Drive duty

According to the mask option, either 1/4, 1/3 or 1/2 duty can be selected as the LCD drive duty. Table 4.8.3.1 shows the differences in the number of segments according to the selected duty.

Table 4.8.3.1 Differences according to selected duty

Duty	COM used	Max. number of segments	Frame frequency *
1/4	COM0–COM3	152 (38 × 4)	f_{OSC1}/1,024 (32 Hz)
1/3	COM0–COM2	114 (38 × 3)	f_{OSC1}/768 (42.7 Hz)
1/2	COM0–COM1	76 (38 × 2)	f_{OSC1}/1,024 (32 Hz)

∗ When f_{OSC1} = 32 kHz

(3) Output specification

- The segment terminals (SEG0–SEG37) are selected by mask option in pairs for either segment signal output or DC output (V_{DD} and V_{SS} binary output). When DC output is selected, the data corresponding to COM0 of each segment terminal is output.
- When DC output is selected, either complementary output or Pch open drain output can be selected for each terminal by mask option.

*Note: The terminal pairs are the combination of SEG (2*n) and SEG (2*n + 1) (where n is an integer from 0 to 18).*

(4) Drive bias

For the drive bias of the S1C60A16, either 1/3 bias or 1/2 bias can be selected by the mask option. When using the LCD system voltage regulator, it is fixed at 1/3 bias.

4.8.4 Control of LCD driver

Table 4.8.4.1 shows the LCD driver's control bits and their addresses. Figure 4.8.4.1 shows the display memory map.

Table 4.8.4.1 Control bits of LCD driver

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2D0H	0	0	0	CSDC2	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R			R/W	0 *3	– *2	–	–	Unused
					CSDC2	1	Normal	All off	LCD all off control
2E8H	CSDC1	ETI2	ETI8	ETI32	CSDC1	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 or 2	4	**Display memory (38 words × 4 bits)**															
	5	**Page 0: R/W, Page 2: W only**															
	6							**Unused area**									

Fig. 4.8.4.1 Display memory map

CSDC2: LCD all Off control (2D0H•D0)

Controls the LCD display.

When "1" is written : LCD displayed
When "0" is written : LCD is all off
Read-out : Valid

By writing "0" to the CSDC2 register, all the LCD dots goes off, and when "1" is written, it returns to normal display.
Writing "0" outputs an off waveform to the SEG terminals, and does not affect the content of the display memory.
After an initial reset, CSDC2 is set to "1".

CSDC1: LCD drive switch (2E8H•D3)

The LCD drive format can be selected with this switch.

When "1" is written : Static drive
When "0" is written : Dynamic drive
Read-out : Valid

At initial reset, dynamic drive (CSDC1 = "0") is selected.

Display memory (040H–065H or 240H–265H)

The LCD segments are lit or turned off depending on this data.

When "1" is written : Lit
When "0" is written : Not lit
Read-out : Valid for Page 0
Undefined Page 2

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.
At initial reset, the contents of the display memory are undefined.

4.8.5 Programming notes

(1) When Page 0 is selected for the display memory, the memory data and the display will not match until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When Page 2 is selected for the display memory, that area becomes write-only. Consequently, data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

4.9 Clock Timer

4.9.1 Configuration of clock timer

The S1C60N16 Series has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of a seven-bit binary counter that serves as the input clock, a 256 Hz signal output by the divider. Data of the four high-order bits (16 Hz–2 Hz) can be read out by the software.
Figure 4.9.1.1 is the block diagram for the clock timer.

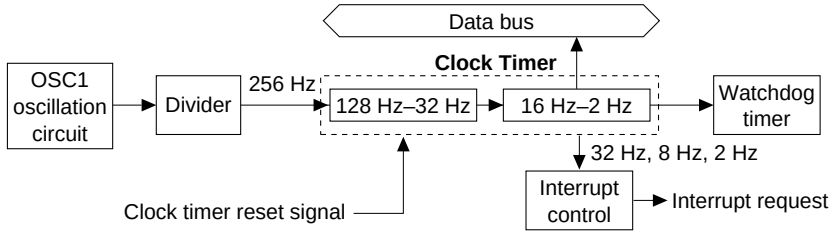


Fig. 4.9.1.1 Clock timer block diagram

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

4.9.2 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz and 2 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.9.2.1 is the timing chart of the clock timer.

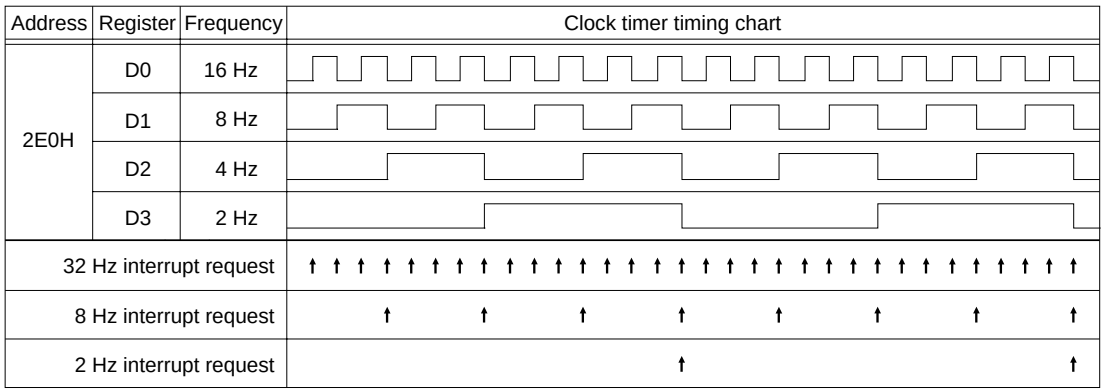


Fig. 4.9.2.1 Clock timer timing chart

As shown in Figure 4.9.2.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz , 2 Hz). At this time, the corresponding interrupt factor flag (TI32, TI8, TI2) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (ETI32, ETI8, ETI2). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.9.3 Control of clock timer

Table 4.9.3.1 shows the clock timer control bits and their addresses.

Table 4.9.3.1 Control bits of clock timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E0H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (2 Hz)
					TM2	0			Clock timer data (4 Hz)
	R				TM1	0			Clock timer data (8 Hz)
					TM0	0			Clock timer data (16 Hz)
2E8H	CSDC1	ETI2	ETI8	ETI32	CSDC1	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

TM0–TM3: Timer data (2E0H)

The 16 Hz–2 Hz timer data of the clock timer can be read out with this register. These four bits are read-out only, and writing operations are invalid.
At initial reset, the timer data is initialized to "0H".

ETI32, ETI8, ETI2: Interrupt mask registers (2E8H•D0–D2)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written : Enabled
When "0" is written : Masked
Read-out : Valid

The interrupt mask registers (ETI32, ETI8, ETI2) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz).
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are all set to "0".

TI32, TI8, TI2: Interrupt factor flags (2E9H•D0–D2)

These flags indicate the status of the clock timer interrupt.

When "1" is read out : Interrupt has occurred
When "0" is read out : Interrupt has not occurred
Writing : Invalid

The interrupt factor flags (TI32, TI8, TI2) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags can be reset through being read out by the software. Also, the flags can be read out only in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

TMRST: Clock timer reset (2EEH•D3)

This bit resets the clock timer.

When "1" is written : Clock timer reset
When "0" is written : No operation
Read-out : Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer starts immediately after this. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" at read-out.

4.9.4 Programming notes

(1) When the clock timer has been reset, the interrupt factor flag (TI) may sometimes be set to "1". Consequently, perform flag read-out (reset the flag) as necessary at reset.

(2) The input clock of the watchdog timer is the 2 Hz signal of the clock timer, so that the watchdog timer may be counted up at timer reset.

(3) Read-out the interrupt factor flag (TI) only during the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

4.10 Stopwatch Timer

4.10.1 Configuration of stopwatch timer

The S1C60N16 Series incorporates a 1/100 sec and 1/10 sec stopwatch timer. The stopwatch timer is configured of a two-stage, four-bit BCD counter serving as the input clock of an approximately 100 Hz signal (signal obtained by approximately demultiplying the 256 Hz signal output by the divider). Data can be read out four bits at a time by the software.
Figure 4.10.1.1 is the block diagram of the stopwatch timer.

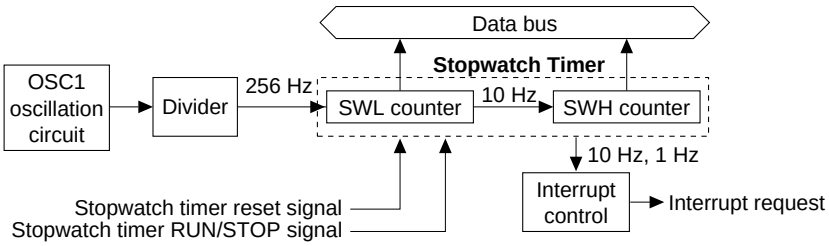


Fig. 4.10.1.1 Stopwatch timer block diagram

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

4.10.2 Count-up pattern

The stopwatch timer is configured of four-bit BCD counters SWL and SWH.
The counter SWL, at the stage preceding the stopwatch timer, has an approximated 100 Hz signal for the input clock. It counts up every 1/100 sec, and generates an approximated 10 Hz signal. The counter SWH has an approximated 10 Hz signal generated by the counter SWL for the input clock. It count-up every 1/10 sec, and generated 1 Hz signal.
Figure 4.10.2.1 shows the count-up pattern of the stopwatch timer.

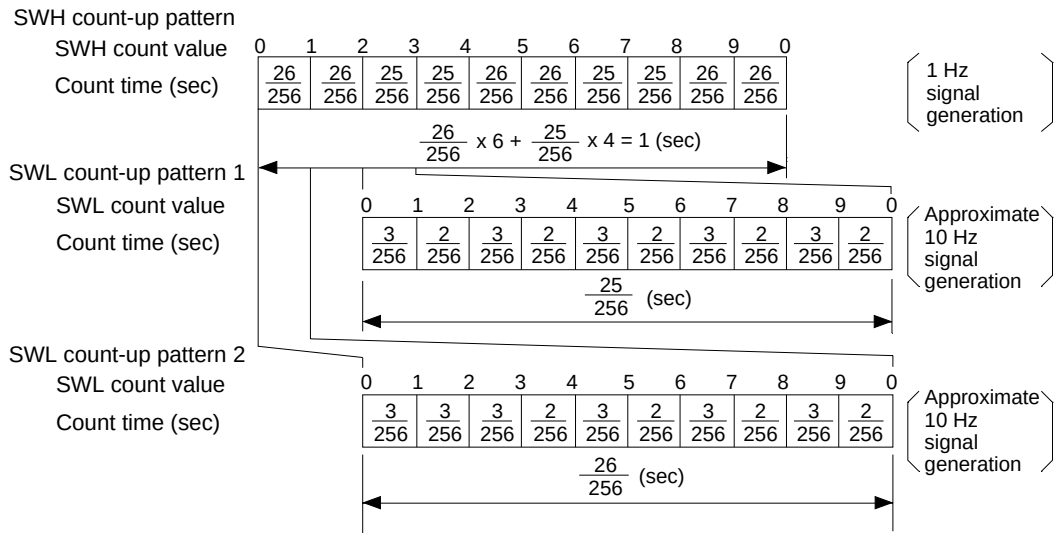


Fig. 4.10.2.1 Count-up pattern of stopwatch timer

SWL generates an approximated 10 Hz signal from the basic 256 Hz signal. The count-up intervals are 2/256 sec and 3/256 sec, so that finally two patterns are generated: 25/256 sec and 26/256 sec intervals. Consequently, these patterns do not amount to an accurate 1/100 sec.
SWH counts the approximated 10 Hz signals generated by the 25/256 sec and 26/256 sec intervals in the ratio of 4:6, to generate a 1 Hz signal. The count-up intervals are 25/256 sec and 26/256 sec, which do not amount to an accurate 1/10 sec.

4.10.3 Interrupt function

The 10 Hz (approximate 10 Hz) and 1 Hz interrupts can be generated through the overflow of stopwatch timers SWL and SWH respectively. Also, software can set whether to separately mask the frequencies described earlier.
Figure 4.10.3.1 is the timing chart for the stopwatch timer.

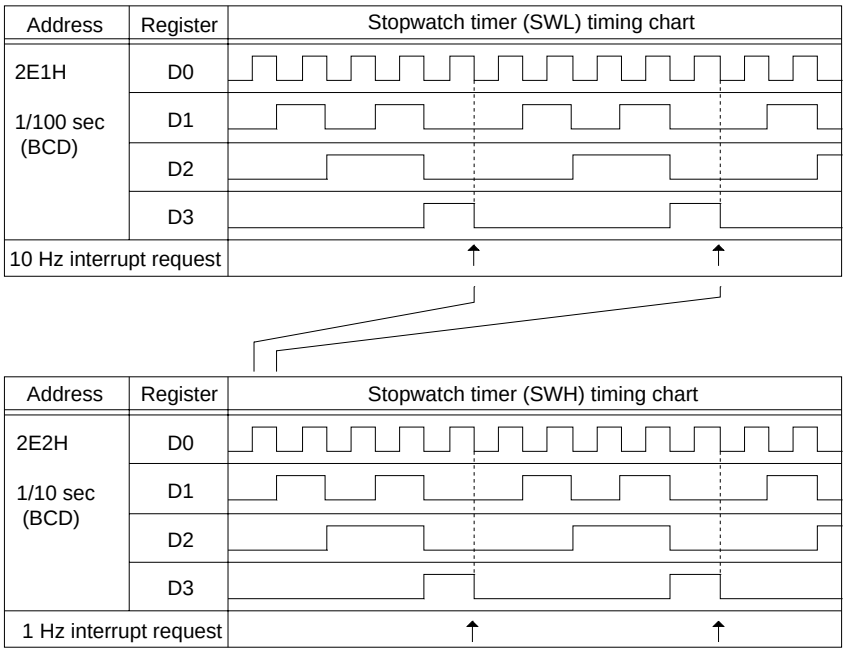


Fig. 4.10.3.1 Stopwatch timer timing chart

As shown in Figure 4.10.3.1, the interrupts are generated by the overflow of their respective counters ("9" changing to "0"). Also, at this time the corresponding interrupt factor flags (SWIT0, SWIT1) are set to "1". The respective interrupts can be masked separately through the interrupt mask registers (EISWIT0, EISWIT1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

4.10.4 Control of stopwatch timer

Table 4.10.4.1 list the stopwatch timer control bits and their addresses.

Table 4.10.4.1 Control bits of stopwatch timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E1H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer 1/100 sec data (BCD)
	R				SWL1	0			
					SWL0	0			LSB
2E2H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer 1/10 sec data (BCD)
	R				SWH1	0			
					SWH0	0			LSB
2E6H	HLMOD	0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register (S1C60A16)
					0 *3	– *2	–	–	Unused
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

SWL0–SWL3: Stopwatch timer 1/100 sec (2E1H)

Data (BCD) of the 1/100 sec column of the stopwatch timer can be read out. These four bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0H".

SWH0–SWH3: Stopwatch timer 1/10 sec (2E2H)

Data (BCD) of the 1/10 sec column of the stopwatch timer can be read out. These four bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0H".

EISWIT0, EISWIT1: Interrupt mask registers (2E6H•D0 and D1)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written : Enabled
When "0" is written : Masked
Read-out : Valid

The interrupt mask registers (EISWIT0, EISWIT1) are used to separately select whether to mask the 10 Hz and 1 Hz interrupts.
At initial reset, these registers are both set to "0".

SWIT0, SWIT1: Interrupt factor flags (2EAH•D0 and D1)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read out : Interrupt has occurred
When "0" is read out : Interrupt has not occurred
Writing : Invalid

The interrupt factor flags (SWIT0, SWIT1) correspond to the 10 Hz and 1 Hz interrupts respectively. With these flags, the software can judge whether a stopwatch timer interrupt has occurred. However, regardless of the interrupt mask register setting, these flags are set to "1" by the counter overflow.
These flags are reset when read out by the software. Also, read-out is only possible in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

SWRST: Stopwatch timer reset (2EEH•D1)

This bit resets the stopwatch timer.

When "1" is written : Stopwatch timer reset
When "0" is written : No operation
Read-out : Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained.
This bit is write-only, and is always "0" at read-out.

SWRUN: Stopwatch timer RUN/STOP (2EEH•D2)

This bit controls RUN / STOP of the stopwatch timer.

When "1" is written : RUN
When "0" is written : STOP
Read-out : Valid

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
When the timer data is read out in the RUN status, correct read-out may be impossible because of the carry from the low-order bit (SWL) to the high-order bit (SWH). This occurs when read-out has extended over the SWL and SWH bits when the carry occurs. To prevent this, perform read out after entering the STOP status, and then return to the RUN status. Also, the duration of the STOP status must be within 976 µsec (256 Hz 1 / 4 cycle).
At initial reset, this register is set to "0".

4.10.5 Programming notes

(1) If timer data is read out in the RUN status, the timer must be made into the STOP status, and after data is read out the RUN status can be restored. If data is read out when a carry occurs, the data cannot be read correctly.
Also, the processing above must be performed within the STOP interval of 976 µsec (256 Hz 1 / 4 cycle).

(2) Read-out of the interrupt factor flag (SWIT) must be done only in the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

4.11 Sound Generator

4.11.1 Configuration of sound generator

The S1C60N16 Series outputs buzzer signals (BZ, $\overline{BZ}$) to drive the piezoelectric buzzer.
The frequency of the buzzer signal is software-selectable from eight kinds of demultiplied fOSC1. Further, a digital envelope can be added to the buzzer signal through duty ratio control.
Figure 4.11.1.1 shows the sound generator configuration. Figure 4.11.1.2 shows the sound generator timing chart.

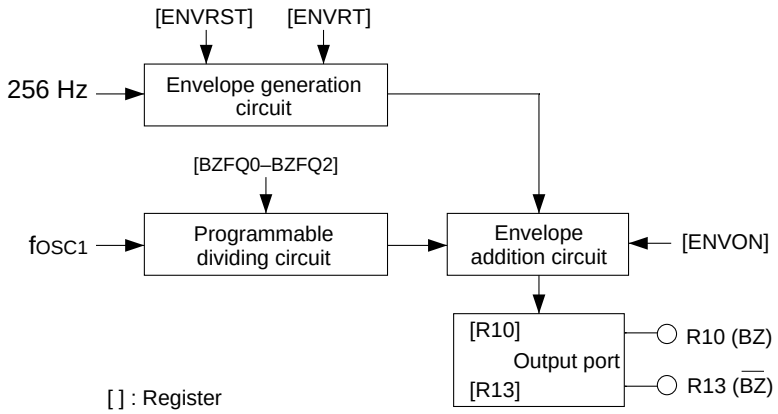


Fig. 4.11.1.1 Configuration of sound generator

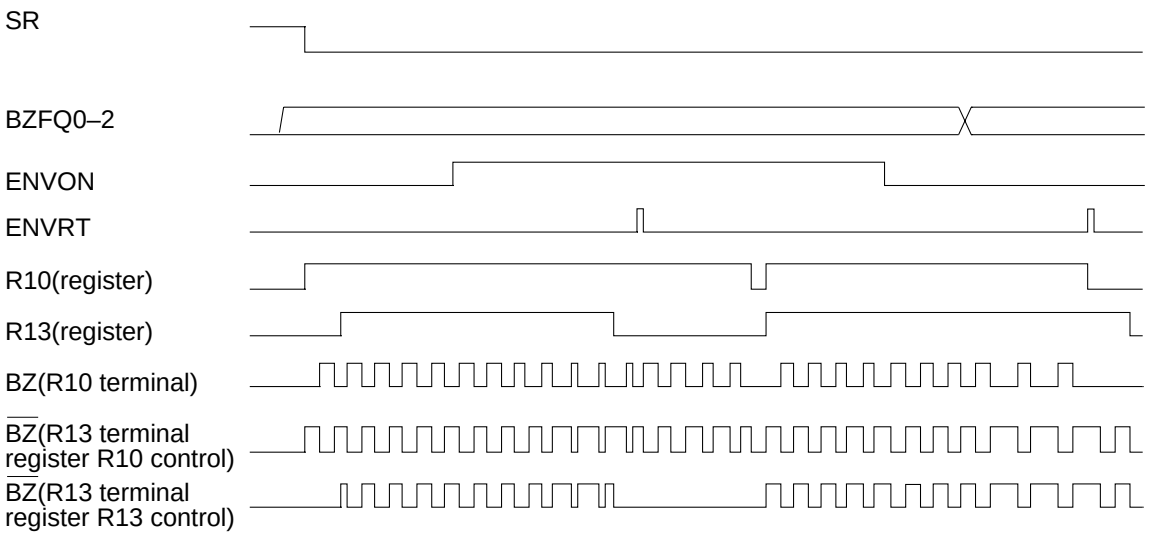


Fig. 4.11.1.2 Timing chart of sound generator

4.11.2 Frequency setting

The frequencies of the buzzer signals (BZ, $\overline{BZ}$) are set by writing data to registers BZFQ0–BZFQ2. Table 4.11.2.1 lists the register setting values and the frequencies that can be set.

Table 4.11.2.1 Setting of frequencies of buzzer signals

BZFQ			Buzzer frequency (Hz)	
2	1	0	Demultiplier ratio	When f_{OSC1} = 32 kHz
0	0	0	f_{OSC1}/8	4,096.0
0	0	1	f_{OSC1}/10	3,276.8
0	1	0	f_{OSC1}/12	2,730.7
0	1	1	f_{OSC1}/14	2,340.6
1	0	0	f_{OSC1}/16	2,048.0
1	0	1	f_{OSC1}/20	1,638.4
1	1	0	f_{OSC1}/24	1,365.3
1	1	1	f_{OSC1}/28	1,170.3

Note: A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the buzzer frequency selection registers (BZFQ0–BZFQ2) changes.

4.11.3 Digital envelope

A duty ratio control data envelope (with duty ratio change in eight stages) can be added to the buzzer signal (BZ, $\overline{BZ}$).
The duty ratio is the ratio of the pulse width compared with the pulse cycle. The BZ output is TH / (TH+TL) when the high level output is TH and the low level output is TL. The $\overline{BZ}$ output (BZ inverted output) is TL / (TH+TL). Also, care must be taken because the duty ratio differs depending on the buzzer frequency.
The envelope is added by writing "1" to register ENVON. If "0" is written the duty ratio is fixed to the maximum. Also, if the envelope is added, the duty ratio is reverted to the maximum by writing "1" in register ENVRST, and the duty ratio also becomes the maximum at the start of the buzzer signal output.
The decay time of the envelope (time for the duty ratio to change) can be selected with the register ENVRT. This time is 62.5 msec (16 Hz) when "0" is written, and 125 msec (8 Hz) when "1" is written. However, a maximum difference of 4 msec is taken from envelope-ON until the first change.
Table 4.11.3.1 lists the duty rates and buzzer frequencies. Figure 4.11.3.1 shows the digital envelope timing chart.

Table 4.11.3.1 Duty rates and buzzer frequencies

BZFQ (register) / Duty rate	2	0	1	0	1	0	1	0	1
	1	0	0	0	0	1	1	1	1
	0	0	0	1	1	0	0	1	1
Level 1 (max.)		8/16		8/20		12/24		12/28	
Level 2		7/16		7/20		11/24		11/28	
Level 3		6/16		6/20		10/24		10/28	
Level 4		5/16		5/20		9/24		9/28	
Level 5		4/16		4/20		8/24		8/28	
Level 6		3/16		3/20		7/24		7/28	
Level 7		2/16		2/20		6/24		6/28	
Level 8 (min.)		1/16		1/20		5/24		5/28	

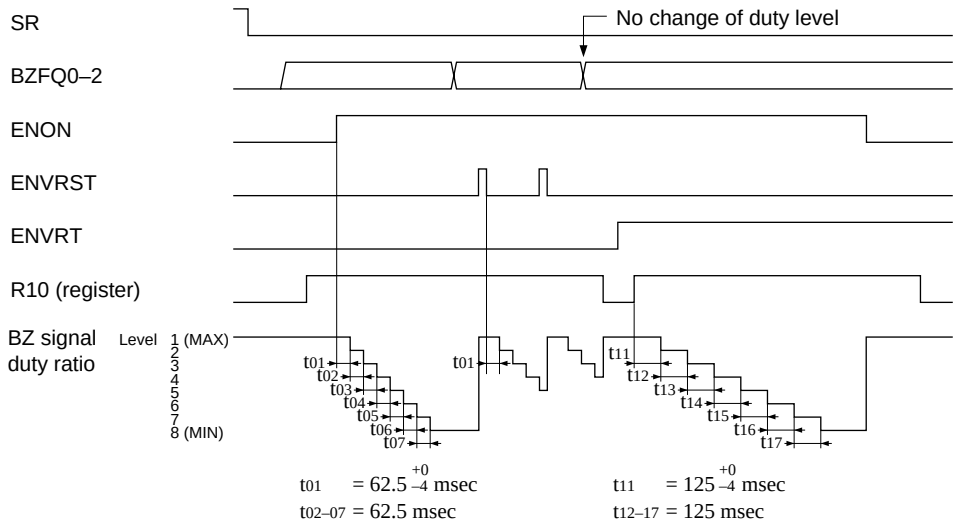


Fig. 4.11.3.1 Digital envelope timing chart

4.11.4 Mask option

(1) Selection can be made whether to output the BZ signal from the R10 terminal.

(2) Selection can be made whether to output the $\overline{BZ}$ signal from the R13 terminal. However, if the BZ signal is not output the $\overline{BZ}$ signal cannot be output.

(3) Selection can be made to perform the $\overline{BZ}$ signal output control through the R10 register or the R13 register.

See Section 4.5, "Output Ports" for details of the above mask option.

4.11.5 Control of sound generator

Table 4.11.5.1 lists the sound generator's control bits and their addresses.

Table 4.11.5.1 Control bits of sound generator

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
					R11	0	High	Low	Output port (R11)
	R/W		R/W / R	R/W	SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control
2F6H	BZFQ2	BZFQ1	BZFQ0	ENVRST	BZFQ2	0			Buzzer frequency selection [BZFQ2–0]: 0 / 1 / 2 / 3 → Frequency: fOSC1/8 / fOSC1/10 / fOSC1/12 / fOSC1/14; [BZFQ2–0]: 4 / 5 / 6 / 7 → Frequency: fOSC1/16 / fOSC1/20 / fOSC1/24 / fOSC1/28
					BZFQ1	0			
	R/W			W	BZFQ0	0			
					ENVRST*3	Reset	Reset	–	Envelope reset
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

BZFQ0–BZFQ2: Buzzer frequency selection register (2F6H•D1–D3)

This is used to select the frequency of the buzzer signal.

Table 4.11.5.2 Buzzer frequency

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	fOSC1/8
0	0	1	fOSC1/10
0	1	0	fOSC1/12
0	1	1	fOSC1/14
1	0	0	fOSC1/16
1	0	1	fOSC1/20
1	1	0	fOSC1/24
1	1	1	fOSC1/28

Buzzer frequency is selected from the above eight types that have been divided by fOSC1 (oscillation frequency of the OSC1 oscillation circuit).
At initial reset, fOSC1 / 8 (Hz) is selected.

ENVRST: Envelope reset (2F6H•D0)

This is the reset input to make the duty ratio of the buzzer signal the maximum.

When "1" is written : Reset input
When "0" is written : No operation
Read-out : Always "0"

When the envelope is added to the buzzer signal, the duty ratio is made maximum through this reset input. When the envelope is not added or when the buzzer signal is not output, the reset input is invalid.

ENVON: Envelope ON/OFF (2F7H•D3)

This controls adding the envelope to the buzzer signal.

When "1" is written : Envelope added (ON)
When "0" is written : No envelope (OFF)
Read-out : Valid

The envelope is the digital envelope based on duty ratio control. When there is no envelope, the duty ratio is fixed to the maximum.
At initial reset, no envelope (OFF) is selected.

ENVRT: Envelope decay time (2F7H•D2)

This input selects the decay time of the envelope added to the buzzer signal.

When "1" is written : 1.0 sec (125 msec × 7 = 875 msec)
When "0" is written : 0.5 sec (62.5 msec × 7 = 437.5 msec)
Read-out : Valid

The decay time of the digital envelope is decided by the time taken for the duty ratio to change. When "1" is written to ENVRT the time is 125 msec (8 Hz) units, and when "0" is written it is 62.5 msec (16 Hz) units.
At initial reset, 0.5 sec (437.5 msec) is selected.

R10, R13 (at BZ, $\overline{BZ}$ output selection): Special output port data (2ECH•D0, D3)

These control output of the buzzer signals (BZ, $\overline{BZ}$).

When "1" is written : Buzzer signal output
When "0" is written : Low level (DC) output
Read-out : Valid

- ***$\overline{BZ}$ output under R13 control***

  BZ output and $\overline{BZ}$ output can be controlled independently. BZ output is controlled by writing data to register R10. $\overline{BZ}$ output is controlled by writing data to register R13.

- ***$\overline{BZ}$ output under R10 control***

  By writing data to register R10 only, BZ output and $\overline{BZ}$ output can be controlled simultaneously. In this case, register R13 can be used as a read / write one-bit general register. This register does not affect $\overline{BZ}$ output (output to pin R13).

At initial reset, R10 and R13 are set to "0".

4.11.6 Programming note

A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the output registers (R10, R13) and the buzzer frequency selection registers (BZFQ0–BZFQ2) changes.

4.12 Event Counter

4.12.1 Configuration of event counter

The S1C60N16 Series has an event counter that counts the clock signals input from outside.
The event counter is configured of a pair of eight-bit binary counters (UP counters). The clock pulses are input through terminals K02 and K03 of the input port.
The clock signals input from the terminals are input to the event counter via the noise rejector.
The event counter detects the phases of the two clock signals. Software selection provides for two modes, the phase detection mode in which one of the counters can be chosen to input the clock signal, and the separate mode in which each clock signal is input to different counters.
Figure 4.12.1.1 shows the configuration of the event counter.

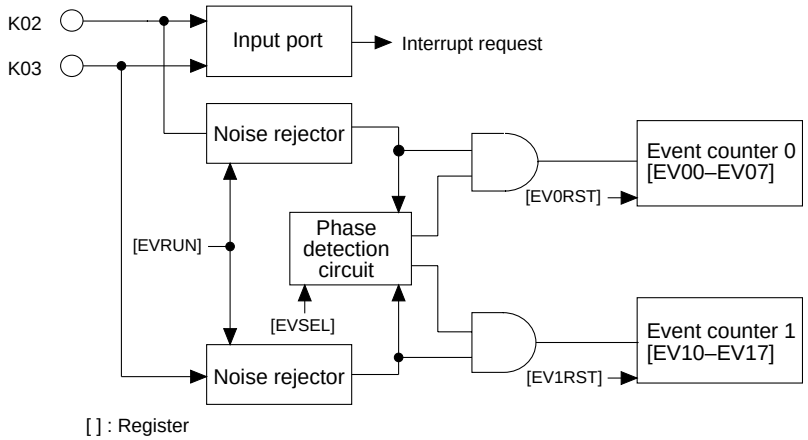


Fig. 4.12.1.1 Configuration of event counter

4.12.2 Switching count mode

The event counter detects the phases of the two clock signals. Software selection provides for two modes, the phase detection mode in which one of the counters can be chosen to input the clock signal, and the separate mode in which each clock signal is input to different counters.
Selection can be made by writing data to the EVSEL register. When "0" is written the phase detection mode is enabled, and when "1" is written the separate mode is enabled.
In the phase detection mode, the clock signals having different phases must be input simultaneously to terminals K02 and K03. When the input from terminal K02 is fast the clock signal is input to event counter 1, and when the input from terminal K03 is fast the clock signal is input to event counter 0.
In the separate mode, input from terminal K02 is made to event counter 0, and input from terminal K03 is made to event counter 1.
Figure 4.12.2.1 is the timing chart for the event counter.

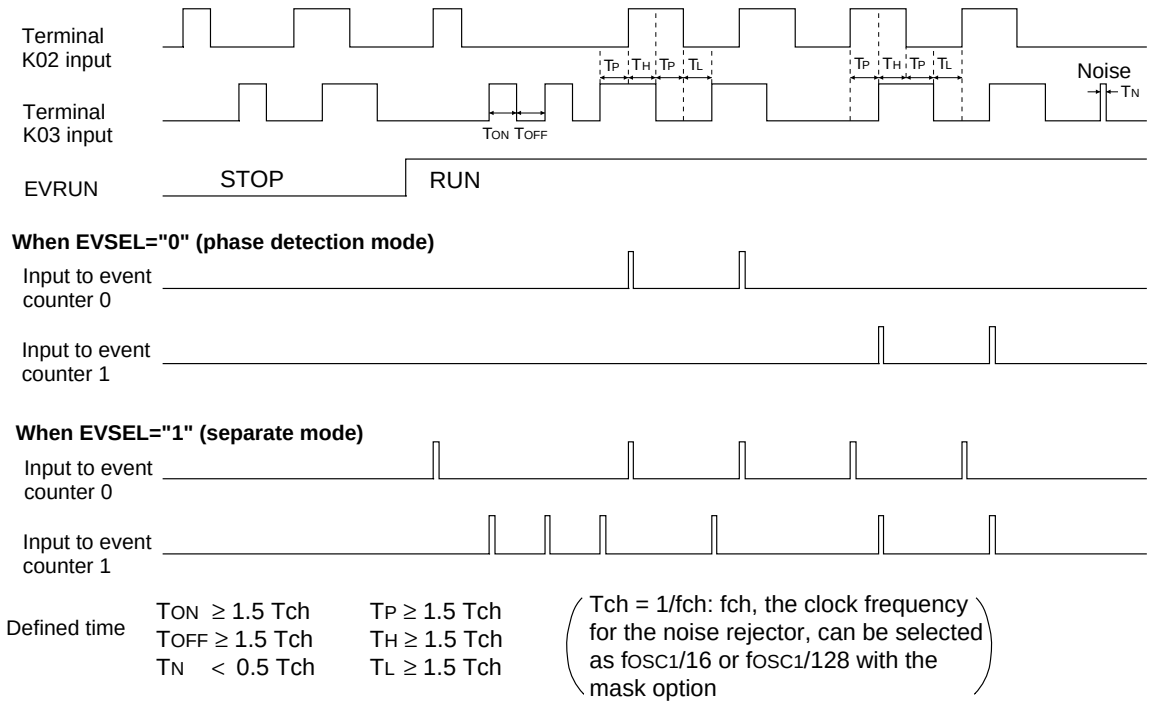


Fig. 4.12.2.1 Event counter timing chart

4.12.3 Mask option

The clock frequency of the noise rejector can be selected as f_{OSC1} / 16 or f_{OSC1} / 128. Table 4.12.3.1 lists the defined time depending on the frequency selected.

Table 4.12.3.1 Defined time depending on frequency selected

Selection	When f_{OSC1} = 32.768 kHz	
	f_{OSC1}/16	f_{OSC1}/128
T_N	0.24	1.95
T_{ON}	0.74	5.86
T_{OFF}	0.74	5.86
T_P	0.74	5.86
T_H	0.74	5.86
T_L	0.74	5.86

T_N : Max value (Unit: msec)
Others : Min value

4.12.4 Control of event counter

Table 4.12.4.1 shows the event counter control bits and their addresses.

Table 4.12.4.1 Control bits of event counter

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2F8H	EV03	EV02	EV01	EV00	EV03	0			Event counter 0 (low-order 4 bits)
					EV02	0			
	R				EV01	0			
					EV00	0			
2F9H	EV07	EV06	EV05	EV04	EV07	0			Event counter 0 (high-order 4 bits)
					EV06	0			
	R				EV05	0			
					EV04	0			
2FAH	EV13	EV12	EV11	EV10	EV13	0			Event counter 1 (low-order 4 bits)
					EV12	0			
	R				EV11	0			
					EV10	0			
2FBH	EV17	EV16	EV15	EV14	EV17	0			Event counter 1 (high-order 4 bits)
					EV16	0			
	R				EV15	0			
					EV14	0			
2FCH	EVSEL	ENRUN	EV1RST	EV0RST	EVSEL	0	Separate	Phase	Event counter mode selection
					EVRUN	0	Run	Stop	Event counter Run/Stop
	R/W		W		EV1RST*3	Reset	Reset	–	Event counter 1 reset
					EV0RST*3	Reset	Reset	–	Event counter 0 reset

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

EV00–EV03: Event counter 0 low-order data (2F8H)

The four low-order data bits of event counter 0 are read out.
These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 0 is set to "00H".

EV04–EV07: Event counter 0 high-order data (2F9H)

The four high-order data bits of event counter 0 are read out.
These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 0 is set to "00H".

EV10–EV13: Event counter 1 low-order data (2FAH)

The four low-order data bits of event counter 1 are read out.
These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 1 is set to "00H".

EV14–EV17: Event counter 1 high-order data (2FBH)

The four high-order data bits of event counter 1 are read out.
These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 1 is set to "00H".

EV0RST: Event counter 0 reset (2FCH•D0)

This is the register for resetting event counter 0.

When "1" is written : Event counter 0 reset
When "0" is written : No operation
Read-out : Always "0"

When "1" is written, event counter 0 is reset and the data becomes "00H". When "0" is written, no operation is executed.
This is a write-only bit, and is always "0" at read-out.

EV1RST: Event counter 1 reset (2FCH•D1)

This is the register for resetting event counter 1.

When "1" is written : Event counter 1 reset
When "0" is written : No operation
Read-out : Always "0"

When "1" is written, event counter 1 is reset and the data becomes "00H". When "0" is written, no operation is executed.
This is a write-only bit, and is always "0" at read-out.

EVRUN: Event counter RUN/STOP (2FCH•D2)

This register controls the event counter RUN / STOP status.

When "1" is written : RUN
When "0" is written : STOP
Read-out : Valid

When "1" is written, the event counter enters the RUN status and starts receiving the clock signal input. When "0" is written, the event counter enters the STOP status and the clock signal input is ignored. (However, input to the input port is valid.)
At initial reset, this register is set to "0".

EVSEL: Event counter mode (2FCH•D3)

This register control the count mode of the event counter.

When "1" is written : Separate
When "0" is written : Phase detection
Read-out : Valid

When "0" is written, the phases of the two clock signals are detected, and the phase detection mode is selected, in which one of the counters is chosen to input the clock signal. When "1" is written, the separate mode is selected, in which each clock signal is input to different counters.
At initial reset, this register is set to "0".

4.12.5 Programming notes

(1) After the event counter has written data to the EVRUN register, it operates or stops in synchronization with the falling edge of the noise rejector clock or stops. Hence, attention must be paid to the above timing when input signals (input to K02 and K03) are being received.

(2) To prevent erroneous reading of the event counter data, read out the counter data several times, compare it, and use the matching data as the result.

4.13 Analog Comparator

4.13.1 Configuration of analog comparator

The S1C60N16 Series incorporates an MOS input analog comparator. This analog comparator, which has two differential input terminals (inverted input terminal AMPM, non-inverted input terminal AMPP), can be used for general purposes.
Figure 4.13.1.1 shows the configuration of the analog comparator.

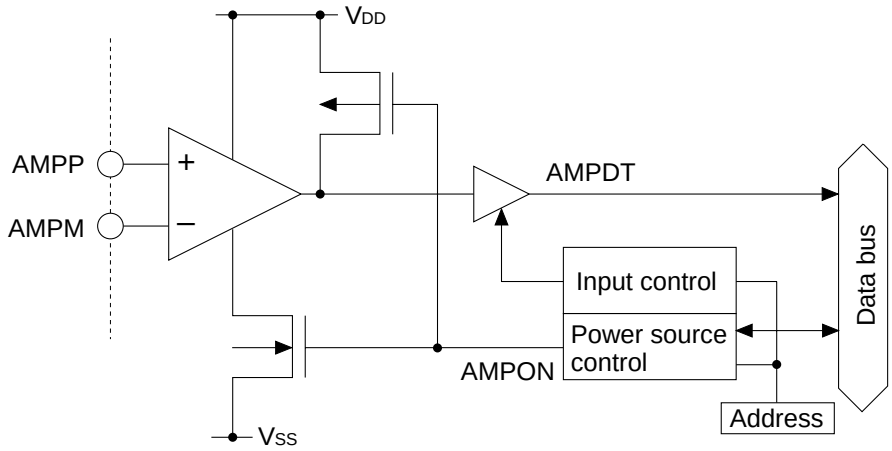


Fig. 4.13.1.1 Configuration of analog comparator

4.13.2 Operation of analog comparator

The analog comparator is ON when the AMPON register is "1", and compares the input levels of the AMPP and AMPM terminals. The result of the comparison is read from the AMPDT register. It is "1" when AMPP (+) > AMPM (-) and "0" when AMPP (+) < AMPM (-).

After the analog comparator goes ON it takes a maximum of 3 msec until the output stabilizes.

4.13.3 Control of analog comparator

Table 4.13.3.1 lists the analog comparator control bits and their addresses.

Table 4.13.3.1 Control bits of analog comparator

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

AMPON: Analog comparator ON/OFF (2F7H•D0)

Switches the analog comparator ON and OFF.

When "1" is written : The analog comparator goes ON
When "0" is written : The analog comparator goes OFF
Read-out : Valid

The analog comparator goes ON when "1" is written to AMPON, and OFF when "0" is written.
At initial reset, AMPON is set to "0".

AMPDT: Analog comparator data (2F7H•D1)

Reads out the output from the analog comparator.

When "1" is read out : AMPP (+) > AMPM (-)
When "0" is read out : AMPP (+) < AMPM (-)
Writing : Invalid

AMPDT is "0" when the input level of the inverted input terminal (AMPM) is greater than the input level of the noninverted input terminal (AMPP); and "1" when smaller.
At initial reset, AMPDT is set to "1".

4.13.4 Programming notes

(1) To reduce current consumption, set the analog comparator to OFF when it is not necessary.

(2) After setting AMPON to "1", wait at least 3 msec for the operation of the analog comparator to stabilize before reading the output data of the analog comparator from AMPDT.

4.14 Supply Voltage Detection (SVD) Circuit

4.14.1 Configuration of SVD circuit

The S1C60N16 Series has a built-in supply voltage detection (SVD) circuit, so that the software can find when the source voltage lowers. The configuration of the SVD circuit is shown in Figure 4.14.1.1.
Turning the SVD operation ON / OFF is controlled through the software (SVDON).
Because the power current consumption of the IC increases when the SVD operation is turned ON, set the SVD operation to OFF unless otherwise necessary.

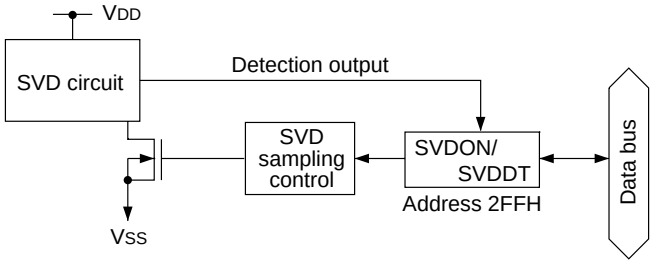


Fig. 4.14.1.1 Configuration of SVD circuit

In the S1C60N16 Series, the evaluation voltage is set as follows:

S1C60N16: 2.2 V
S1C60L16: 1.2 V
S1C60A16: 2.2 V

See Chapter 7, "Electrical Characteristics", for the evaluation voltage accuracy.

4.14.2 Detection timing of SVD circuit

This section explains the timing for when the SVD circuit writes the result of the supply voltage detection to the SVD latch.
Turning the SVD operation ON / OFF is controlled through the software (SVDON).
The result of the source voltage detection is written to the SVD latch by the SVD circuit, and this data can be read out by the software to find the status of the source voltage.

When SVDON is set to "1", SVD detection is executed. As soon as SVDON is reset to "0" the detection result is loaded to the SVD latch. To obtain a stable SVD detection result, the SVD circuit must be set to ON with at least 100 µsec. Hence, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain at 100 µsec minimum
3. Set SVDON to "0"
4. Read out SVDDT

However, when a crystal oscillation clock (f_{OSC1}) is selected for the CPU system clock in the S1C60N16, S1C60L16, and S1C60A16, the instruction cycles are long enough, so that there is no need for concern about maintaining 100 µsec for the SVDON = "1" with the software.

4.14.3 Control of SVD circuit

Table 4.14.3.1 shows the SVD circuit's control bits and their addresses.

Table 4.14.3.1 Control bits of SVD circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2FFH	SVDDT	0	0	0	SVDDT	0	Low	Normal	SVD evaluation data
	SVDON				SVDON	0	On	Off	SVD On/Off
	R	R			0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	W				0 *3	– *2	–	–	Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

SVDON/SVDDT: SVD control/SVD data (2FFH•D3)

Controls the SVD operation.

When "0" is written : SVD OFF
When "1" is written : SVD ON
When "0" is read out : Supply voltage (V_{DD}–V_{SS}) ≥ 2.2 V (S1C60N16 / 60A16) / 1.2 V (S1C60L16)
When "1" is read out : Supply voltage (V_{DD}–V_{SS}) < 2.2 V (S1C60N16 / 60A16) / 1.2 V (S1C60L16)

Note that the function of this bit when written is different to when read out.
When this bit is written to, ON / OFF of the SVD detection operation is controlled; when this bit is read out, the result of the SVD detection (contents of SVD latch) is obtained. Appreciable current is consumed during operation of SVD detection, so keep SVD detection OFF except when necessary.

When SVDON is set to "1", SVD detection is executed. As soon as SVDON is reset to "0" the detection result is loaded to the SVD latch. To obtain a stable detection result, the SVD circuit must be set to ON with at least 100 µsec. Hence, to obtain the detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain at 100 µsec minimum
3. Set SVDON to "0"
4. Read out SVDDT

However, when a crystal oscillation clock (f_{OSC1}) is selected for the CPU system clock in the S1C60N16, S1C60L16, and S1C60A16, the instruction cycles are long enough, so that there is no need for concern about maintaining 100 µsec for the SVDON = "1" with the software.

4.14.4 Programming notes

(1) The SVD circuit takes 100 µsec from the time it goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:
After writing "1" on SVDON, write "0" after at least 100 µsec has elapsed (possible with the next instruction when the OSC1 clock is used as the CPU clock) and then read the SVDDT.

(2) SVDON resides in the same bit at the same address as SVDDT, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for SVDON control.

4.15 Heavy Load Protection Function (S1C60A16)

4.15.1 Outline of heavy load protection function

The S1C60A16 has the heavy load protection function for when the battery load becomes heavy and the source voltage changes, such as when an external buzzer sounds or an external lamp lights. The state where the heavy load protection function is in effect is called the heavy load protection mode. Compared with the normal operation mode, this mode can reduce the output voltage variation of the constant voltage.
The normal mode changes to the heavy load protection mode in the following case:

- When the software changes the mode to the heavy load protection mode (HLMOD = "1")

The heavy load protection mode switches the voltage regulator circuit to the high-stability mode from the low current consumption mode. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

Note: The S1C60N16 and S1C60L16 do not support the heavy load protection function.

4.15.2 Control of heavy load protection function

Table 4.15.2.1 shows the control bits and their addresses for the heavy load protection function.

Table 4.15.2.1 Control bits of heavy load protection function

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2E6H	HLMOD	0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register (S1C60A16)
					0 *3	– *2	–	–	Unused
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

HLMOD: Heavy load protection mode (2E6H•D3)

Sets the IC in heavy load protection mode.

When "1" is written : Heavy load protection mode is set
When "0" is written : Heavy load protection mode is released
Read-out : Valid

When HLMOD is set to "1", the IC enters the heavy load protection mode.
In the S1C60N16 and S1C60L16, HLMOD can be used as a general-purpose R/W register.

4.15.3 Programming notes

(1) More current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) The heavy load protection function is available only in the S1C60A16.
The S1C60N16 and S1C60L16 do not support this function and HLMOD can be used as a general-purpose R/W register that does not affect the IC's operations.

4.16 Interrupt and HALT

The S1C60N16 Series provides the following interrupt settings, each of which is maskable.

External interrupt: Input interrupt (two)
Internal interrupt: Timer interrupt (three)
Stopwatch interrupt (two)
Serial interface interrupt (one)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.
When a HALT instruction is input the CPU operating clock stops, and the CPU enters the HALT status. The CPU is reactivated from the HALT status when an interrupt request occurs.
If reactivation is not caused by an interrupt request, initial reset by the watchdog timer causes reactivates the CPU (when the watchdog timer is enabled).
Figure 4.16.1 shows the configuration of the interrupt circuit.

Interrupt vector map

Table 4.16.1 Interrupt vector map

Page	Step	Interrupt vector
1	00H	Initial reset
	01H	Serial interface interrupt
	02H	Input port interrupt
	03H	Serial interface + Input port interrupt
	04H	Clock timer interrupt
	05H	Serial interface + Clock timer interrupt
	06H	Input port + Clock timer interrupt
	07H	Serial interface + Input port + Clock timer interrupt
	08H	Stopwatch timer interrupt
	09H	Serial interface + Stopwatch timer interrupt
	0AH	Input port + Stopwatch timer interrupt
	0BH	Serial interface + Input port + Stopwatch timer interrupt
	0CH	Clock timer + Stopwatch timer interrupt
	0DH	Serial interface + Clock timer + Stopwatch timer interrupt
	0EH	Input port + Clock timer + Stopwatch timer interrupt
	0FH	All interrupts

The interrupt service routine start address should be written to each interrupt vector address.

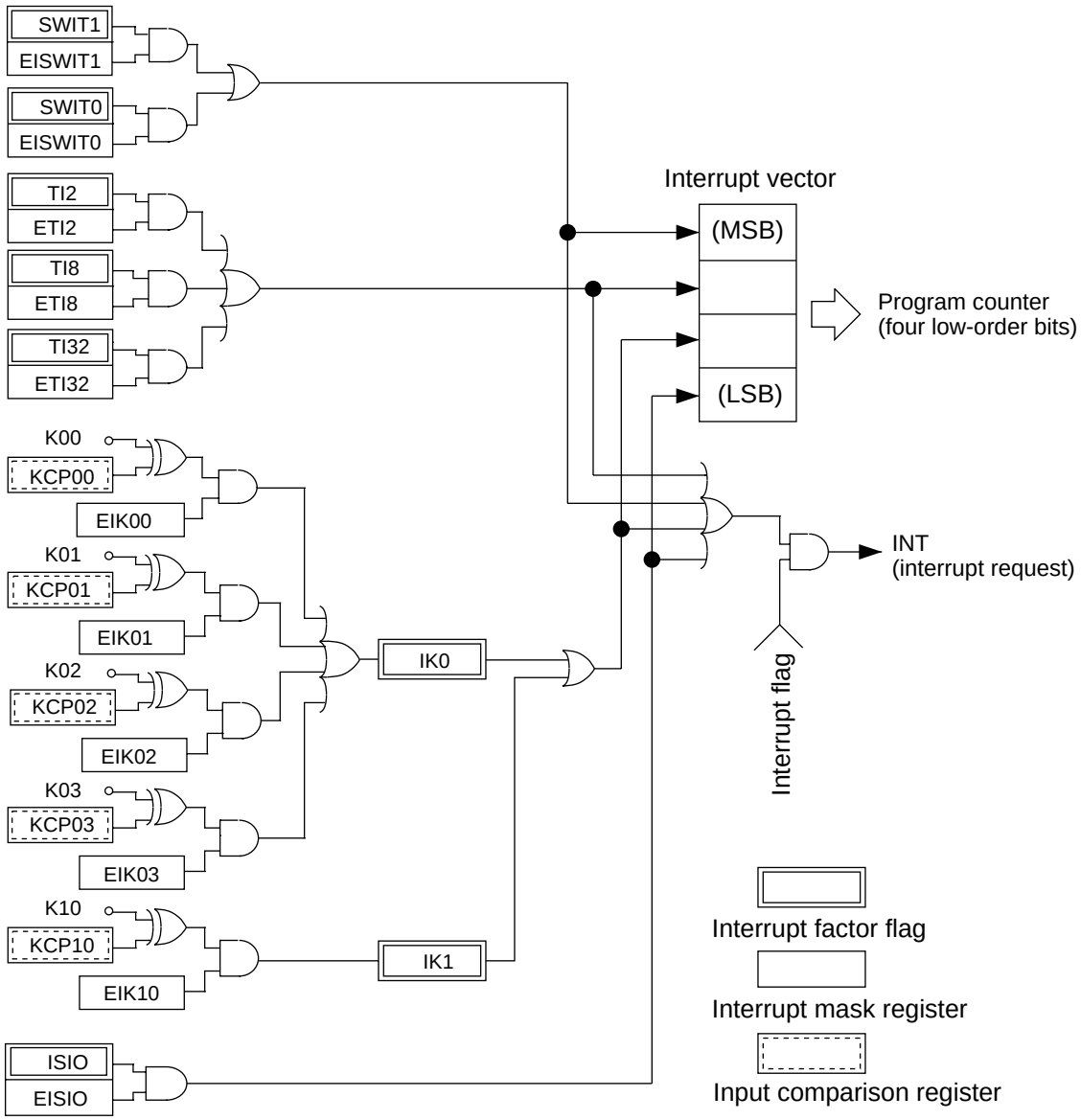


Fig. 4.16.1 Configuration of interrupt circuit

4.16.1 Interrupt factors

Table 4.16.1.1 shows the factors for generating interrupt requests.
The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when any of the conditions below set an interrupt factor flag to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read out.
At initial reset, the interrupt factor flags are reset to "0".

Note: Read the interrupt factor flags only in the DI status (interrupt flag = "0"). A malfunction could result from read-out during the EI status (interrupt flag = "1").

Table 4.16.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag
Clock timer 2 Hz falling edge	TI2 (2E9H•D2)
Clock timer 8 Hz falling edge	TI8 (2E9H•D1)
Clock timer 32 Hz falling edge	TI32 (2E9H•D0)
Stopwatch timer 1 Hz falling edge	SWIT1 (2EAH•D1)
Stopwatch timer 10 Hz falling edge	SWIT0 (2EAH•D0)
Serial interface When 8-bit data input/output has completed	ISIO (2F3H•D0)
Input (K00–K03) port rising/falling edge	IK0 (2EAH•D2)
Input (K10) port rising/falling edge	IK1 (2EAH•D3)

4.16.2 Specific masks and factor flags for interrupt

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read / write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.16.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.16.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
ETI2	(2E8H•D2)	TI2	(2E9H•D2)
ETI8	(2E8H•D1)	TI8	(2E9H•D1)
ETI32	(2E8H•D0)	TI32	(2E9H•D0)
EISWIT1	(2E6H•D1)	SWIT1	(2EAH•D1)
EISWIT0	(2E6H•D0)	SWIT0	(2EAH•D0)
EISIO	(2F2H•D0)	ISIO	(2F3H•D0)
EIK03*	(2E5H•D3)	IK0	(2EAH•D2)
EIK02*	(2E5H•D2)		
EIK01*	(2E5H•D1)		
EIK00*	(2E5H•D0)		
EIK10*	(2E7H•D2)	IK1	(2EAH•D3)

* There is an interrupt mask register for each pin of the input ports.

4.16.3 Interrupt vectors

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 01H–0FH) to be set in the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.16.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Note: The processing in ① and ② above take 12 cycles of the CPU system clock.

Table 4.16.3.1 Interrupt request and interrupt vectors

PC	Value	Interrupt request	
PCS3	1	Stopwatch timer interrupt	Enabled
	0		Masked
PCS2	1	Clock timer interrupt	Enabled
	0		Masked
PCS1	1	Input port interrupt	Enabled
	0		Masked
PCS0	1	Serial interface interrupt	Enabled
	0		Masked

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.16.4 Control of interrupt and HALT

Table 4.16.4.1 shows the interrupt control bits and their addresses.

Table 4.16.4.1 Interrupt control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
	R/W				EIK01	0	Enable	Mask	
					EIK00	0	Enable	Mask	
2E6H	HLMOD	0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register (S1C60A16)
					0 *3	– *2	–	–	Unused
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial I/F clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2E8H	CSDC1	ETI2	ETI8	ETI32	CSDC1	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			Serial I/F clock mode selection [SCS1, 0] 0 1 2 3 / Clock CLK CLK/2 CLK/4 Slave
					SCS0	1			
	R/W				SE2	0	↑	↓	Serial I/F clock edge selection
					EISIO	0	Enable	Mask	Interrupt mask register (serial I/F)
2F3H	0	0	0	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				0 *3	– *2	–	–	Unused
					ISIO *4	0	Yes	No	Interrupt factor flag (serial I/F)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

ETI32, ETI8, ETI2: Interrupt mask registers (2E8H•D0–D2)
TI32, TI8, TI2: Interrupt factor flags (2E9H•D0–D2)
See Section 4.9, "Clock Timer".

EISWIT0, EISWIT1: Interrupt mask registers (2E6H•D0–D1)
SWIT0, SWIT1: Interrupt factor flags (2EAH•D0–D1)
See Section 4.10, "Stopwatch Timer".

EISIO: Interrupt mask register (2F2H•D0)
ISIO: Interrupt factor flag (2F3H•D0)
See Section 4.7, "Serial Interface".

KCP00–KCP03: Input comparison registers (2E4H)
EIK00–EIK03: Interrupt mask registers (2E5H)
IK0: Interrupt factor flag (2EAH•D2)
See Section 4.4, "Input Ports".

KCP10: Input comparison register (2E7H•D1)
EIK10: Interrupt mask register (2E7H•D2)
IK1: Interrupt factor flag (2EAH•D3)
See Section 4.4, "Input Ports".

4.16.5 Programming notes

(1) When the interrupt mask register (EIK) is set to "0", the interrupt factor flag (IK) of the input port cannot be set even though the terminal status of the input port has changed.

(2) The interrupt factor flags of the clock timer, stopwatch timer and serial interface (TI, SWIT, ISIO) are set when the timing condition is established, even if the interrupt mask registers (ETI, EISWIT, EISIO) are set to "0".

(3) Read out the interrupt factor flags only in the DI status (interrupt flag = "0"). If read-out is performed in the EI status (interrupt flag = "1") a malfunction will result.

(4) Writing to the interrupt mask register only in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause malfunction.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The S1C60N16 Series contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 5.1.1 Circuits and control register

Circuit (and item)	Control register	Order of consumed current
CPU	HALT instruction	See Electrical Characteristics (Chapter 7)
CPU operating frequency (S1C60A16)	CLKCHG, OSCC	See Electrical Characteristics (Chapter 7)
Heavy load protection mode (S1C60A16)	HLMOD	See Electrical Characteristics (Chapter 7)
SVD circuit	SVDON	Several tens µA
Analog comparator	AMPON	Several tens µA

Below are the circuit statuses at initial reset.

CPU: Operating status
CPU operating frequency (S1C60A16): Low speed side (CLKCHG = "0"),
OSC3 oscillation circuit stop status (OSCC = "0")
Heavy load protection mode (S1C60A16): Normal operating mode (HLMOD = "0")
SVD circuit: OFF status (SVDON = "0")
Analog comparator: OFF status (AMPON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Watchdog timer

When the watchdog timer is being used, the software must reset it within 3-second cycles, and timer data (WD0–WD2) cannot be used for timer applications.

Oscillation circuit (S1C60A16)

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

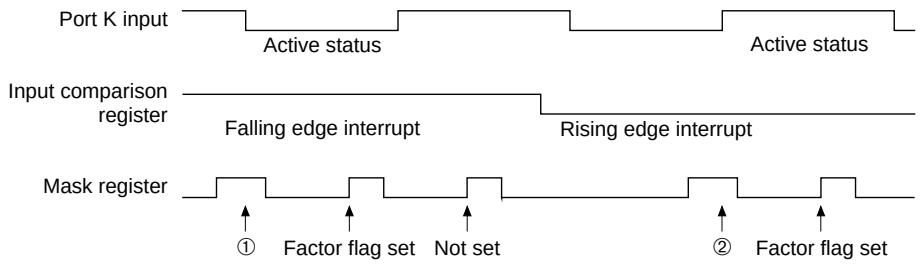
(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

Input port

(1) When input ports are changed from high to low by pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When "Use" is selected with the noise rejector mask option, a maximum delay of 1 msec occurs from time the interrupt conditions are established until the interrupt factor flag (IK) is set to "1" (until the interrupt is actually generated). Hence, pay attention to the timing when reading out (resetting) the interrupt factor flag. For example, when performing a key scan with the key matrix, the key scan changes the input status to set the interrupt factor flag, so it has to be read out to reset it. However, if the interrupt factor flag is read out immediately after key scanning, the delay will cause the flag to be set after read-out, so that it will not be reset.

(3) Input interrupt programming related precautions



When the content of the mask register is rewritten while the port K input is in the active status, the input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 5.2.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set.
Therefore, when using the input interrupt, the active status of the input terminal implies
input terminal = low status, when the falling edge interrupt is effected and
input terminal = high status, when the rising edge interrupt is effected.
When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 5.2.1. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 5.2.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the low status.
In addition, when the mask register = "1" and the content of the input comparison register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input comparison register in the mask register = "0" status.

Output port

When BZ, $\overline{BZ}$ and FOUT are selected with the mask option, a hazard may be observed in the output waveform when the data of the output register changes.

I/O port

(1) When input data are changed from high to low by built-in pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Consequently, if data is read out while the CPU is running in the OSC3 oscillation circuit, data must be read out continuously for about 500 µsec.

(2) When the I/O port is set to the output mode and the data register has been read, the terminal data instead of the register data can be read out. Because of this, if a low-impedance load is connected and read-out performed, the value of the register and the read-out result may differ.

Serial interface

(1) If the bit data of SE2 changes while SCLK is in the master mode, a hazard will be output to the SCLK pin. If this poses a problem for the system, be sure to set the SCLK to the external clock if the bit data of SE2 is to be changed.

(2) Be sure that read-out of the interrupt factor flag (ISIO) is done only when the serial port is in the STOP status (SIOF = "0") and the DI status (interrupt flag = "0"). If read-out is performed while the serial data is in the RUN status (during input or output), the data input or output will be suspended and the initial status resumed. Read-out during the EI status (interrupt flag = "1") causes malfunctioning.

(3) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(4) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(5) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

LCD driver

(1) When Page 0 is selected for the display memory, the memory data and the display will not match until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When Page 2 is selected for the display memory, that area becomes write-only. Consequently, data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

Clock timer

(1) When the clock timer has been reset, the interrupt factor flag (TI) may sometimes be set to "1". Consequently, perform flag read-out (reset the flag) as necessary at reset.

(2) The input clock of the watchdog timer is the 2 Hz signal of the clock timer, so that the watchdog timer may be counted up at timer reset.

Stopwatch timer

If timer data is read out in the RUN status, the timer must be made into the STOP status, and after data is read out the RUN status can be restored. If data is read out when a carry occurs, the data cannot be read correctly.
Also, the processing above must be performed within the STOP interval of 976 µsec (256 Hz 1/4 cycle).

Sound generator

A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the output registers (R10, R13) and the buzzer frequency selection registers (BZFQ0–BZFQ2) changes.

Event counter

(1) After the event counter has written data to the EVRUN register, it operates or stops in synchronization with the falling edge of the noise rejector clock or stops. Hence, attention must be paid to the above timing when input signals (input to K02 and K03) are being received.

(2) To prevent erroneous reading of the event counter data, read out the counter data several times, compare it, and use the matching data as the result.

Analog comparator

(1) To reduce current consumption, set the analog comparator to OFF when it is not necessary.

(2) After setting AMPON to "1", wait at least 3 msec for the operation of the analog comparator to stabilize before reading the output data of the analog comparator from AMPDT.

Supply voltage detection (SVD) circuit

(1) The SVD circuit takes 100 µsec from the time it goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:
After writing "1" on SVDON, write "0" after at least 100 µsec has elapsed (possible with the next instruction when the OSC1 clock is used as the CPU clock) and then read the SVDDT.

(2) SVDON resides in the same bit at the same address as SVDDT, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for SVDON control.

Heavy load protection function (S1C60A16)

(1) More current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) The heavy load protection function is available only in the S1C60A16.
The S1C60N16 and S1C60L16 do not support this function and HLMOD can be used as a general-purpose R/W register that does not affect IC's operations.

Interrupt and HALT

(1) When the interrupt mask register (EIK) is set to "0", the interrupt factor flag (IK) of the input port cannot be set even though the terminal status of the input port has changed.

(2) The interrupt factor flags of the clock timer, stopwatch timer and serial interface (TI, SWIT, ISIO) are set when the timing condition is established, even if the interrupt mask registers (ETI, EISWIT, EISIO) are set to "0".

(3) Read out the interrupt factor flags only in the DI status (interrupt flag = "0"). If read-out is performed in the EI status (interrupt flag = "1") a malfunction will result.

(4) Writing to the interrupt mask register only in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause malfunction.

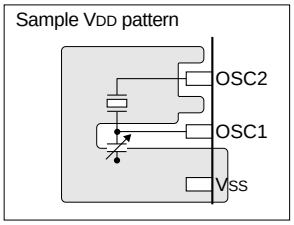
5.3 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when using a crystal oscillator, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1/OSC3 and OSC2/OSC4 terminals and the components connected to these terminals. Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VDD, please keep enough distance between OSC1/OSC3 and VDD or other signals on the board pattern.

<Reset Circuit>

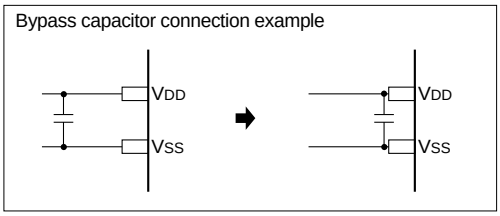
- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-down resistor is added to the RESET terminal by mask option, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD and VSS terminal with patterns as short and large as possible.

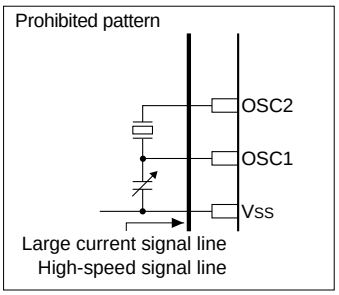
  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



  (3) Components which are connected to the VD1, VC1, VC2, VC3 terminals, such as a capacitor, should be connected in the shortest line.

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

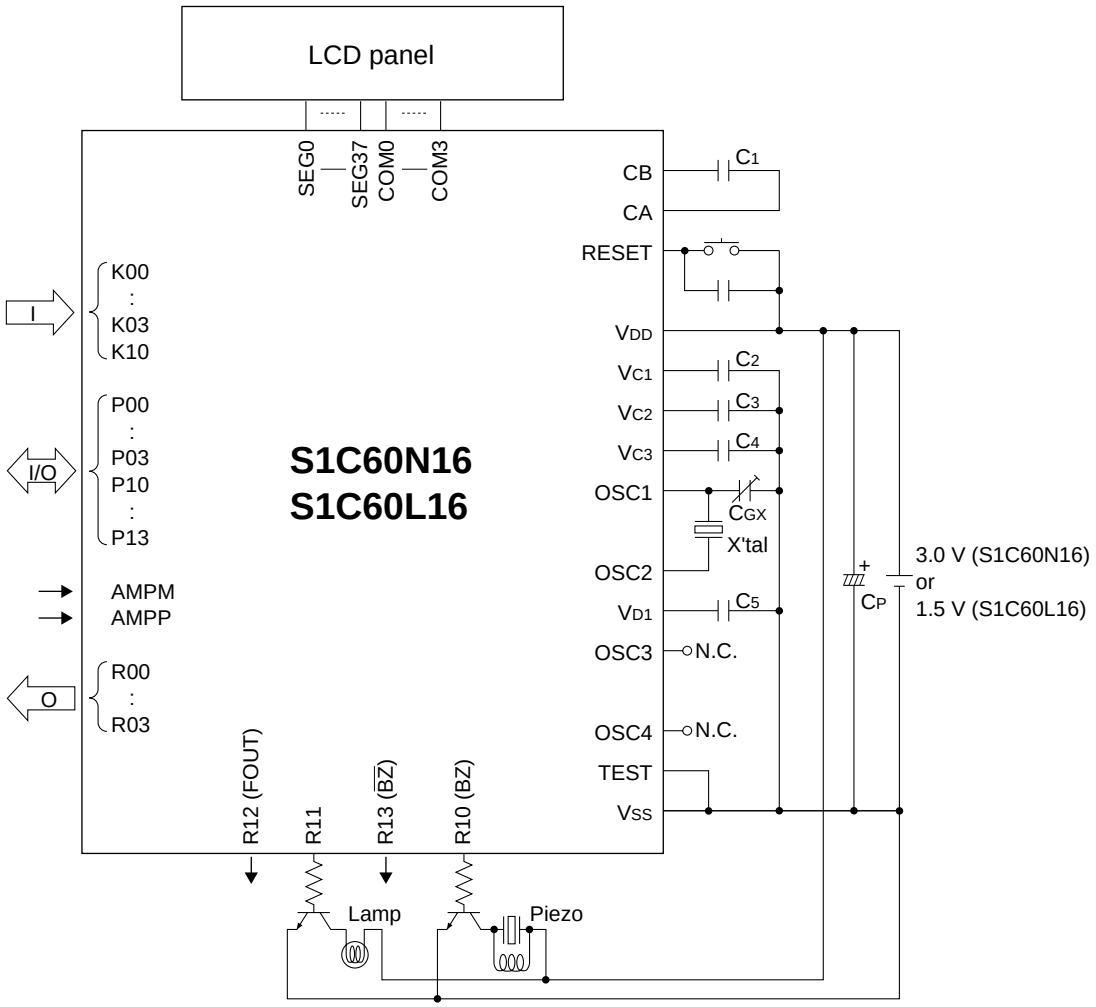
  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

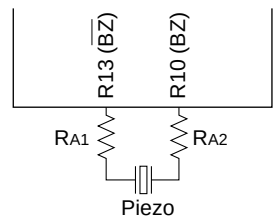
  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM

S1C60N16 and S1C60L16



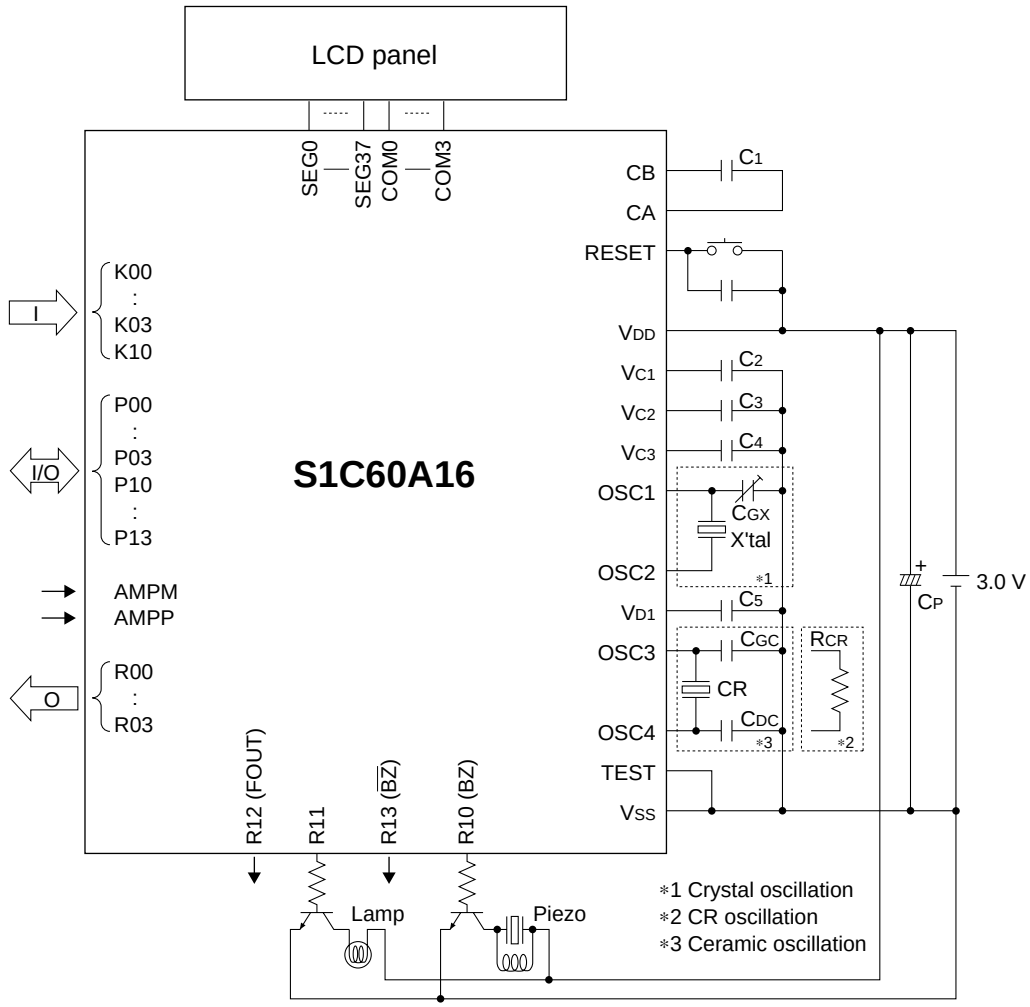
X'tal	Crystal oscillator	32.768 kHz, C_I = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_5	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω



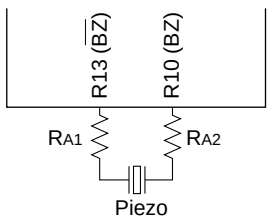
When the piezoelectric buzzer is driven directly

Note: The above table is simply an example, and is not guaranteed to work.

S1C60A16



X'tal	Crystal oscillator	32.768 kHz, C_I = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	1 MHz
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
R_{CR}	Resistor for CR oscillation	40 kΩ (1 MHz)
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_5	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω



When the piezoelectric buzzer is driven directly

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

S1C60N16 and S1C60A16

(V_{SS}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{DD}	-0.5 to 4.5	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package.

S1C60L16

(V_{SS}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{DD}	0.5 to 2.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package.

7.2 Recommended Operating Conditions

S1C60N16

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	2.2	3.0	3.6	V
Oscillation frequency	f_{OSC1}	Crystal oscillation	–	32.768	–	kHz

S1C60L16

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	1.2	1.5	1.8	V
Oscillation frequency	f_{OSC1}	Crystal oscillation	–	32.768	–	kHz

S1C60A16

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	2.2	3.0	3.6	V
Oscillation frequency (1)	f_{OSC1}	Crystal oscillation	–	32.768	–	kHz
Oscillation frequency (2)	f_{OSC3}	duty 50±5%	50	1000	1200	kHz

7.3 DC Characteristics

S1C60N16 and S1C60A16

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, P00–03, P10–13	0.8·V_{DD}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.9·V_{DD}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, P00–03, P10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	0		0.1·V_{DD}	V
High level input current (1)	I_{IH1}	V_{IH1}=3.0V No pull-down	K00–03, K10, P00–03, P10–13 AMPP, AMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=3.0V With pull-down	K00–03, K10	3		10	µA
High level input current (3)	I_{IH3}	V_{IH3}=3.0V With pull-down	P00–03, P10–13, RESET, TEST	3		10	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, K10, P00–03, P10–13 AMPP, AMPM, RESET, TEST	-0.5		0	µA
High level output current	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, P00–03, P10–13			-0.9	mA
Low level output current	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, P00–03, P10–13	3.0			mA
Common output current	I_{OH2}	V_{OH2}=V_{C3}-0.05V	COM0–3			-3	µA
	I_{OL2}	V_{OL2}=V_{SS}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH3}	V_{OH3}=V_{C3}-0.05V	SEG0–37			-3	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		3			µA
Segment output current (during DC output)	I_{OH4}	V_{OH4}=0.9·V_{DD}	SEG0–37			-200	µA
	I_{OL4}	V_{OL4}=0.1·V_{DD}		200			µA

S1C60L16

Unless otherwise specified:

V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, P00–03, P10–13	0.8·V_{DD}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.9·V_{DD}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, P00–03, P10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	0		0.1·V_{DD}	V
High level input current (1)	I_{IH1}	V_{IH1}=1.5V No pull-down	K00–03, K10, P00–03, P10–13 AMPP, AMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=1.5V With pull-down	K00–03, K10	1.5		5	µA
High level input current (3)	I_{IH3}	V_{IH3}=1.5V With pull-down	P00–03, P10–13, RESET, TEST	1.5		5	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, K10, P00–03, P10–13 AMPP, AMPM, RESET, TEST	-0.5		0	µA
High level output current	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, P00–03, P10–13			-150	µA
Low level output current	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, P00–03, P10–13	700			µA
Common output current	I_{OH2}	V_{OH2}=V_{C3}-0.05V	COM0–3			-3	µA
	I_{OL2}	V_{OL2}=V_{SS}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH3}	V_{OH3}=V_{C3}-0.05V	SEG0–37			-3	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		3			µA
Segment output current (during DC output)	I_{OH4}	V_{OH4}=0.9·V_{DD}	SEG0–37			-100	µA
	I_{OL4}	V_{OL4}=0.1·V_{DD}		100			µA

7.4 Analog Circuit Characteristics and Current Consumption

S1C60N16

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		0.90	0.98	1.06	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2·V_{C1} ×0.9		2·V_{C1} +0.1	V
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3·V_{C1} ×0.9		3·V_{C1} +0.1	V
SVD voltage	V_{SVD}			2.05	2.20	2.35	V
SVD circuit response time	t_{SVD}					100	µs
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=1.5V V_{IM}=V_{IP}±15mV				3	ms
Current consumption	I_{OP}	During HALT	Without panel load		0.7	1.0	µA
		During operation *1			1.4	2.0	µA

*1 The SVD circuit and analog comparator are in the OFF status.

S1C60L16

Unless otherwise specified:

V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		0.90	0.98	1.06	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2·V_{C1} ×0.9		2·V_{C1} +0.1	V
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3·V_{C1} ×0.9		3·V_{C1} +0.1	V
SVD voltage	V_{SVD}			1.10	1.20	1.30	V
SVD circuit response time	t_{SVD}					100	µs
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=1.1V V_{IM}=V_{IP}±30mV				3	ms
Current consumption	I_{OP}	During HALT	Without panel load		0.7	1.0	µA
		During operation *1			1.4	2.0	µA

*1 The SVD circuit and analog comparator are in the OFF status.

S1C60A16

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		0.90	0.98	1.06	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2·V_{C1} ×0.9		2·V_{C1} +0.1	V
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3·V_{C1} ×0.9		3·V_{C1} +0.1	V
SVD voltage	V_{SVD}			2.05	2.20	2.35	V
SVD circuit response time	t_{SVD}					100	µs
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=1.5V V_{IM}=V_{IP}±15mV				3	ms
Current consumption (normal operation mode)	I_{OP1}	During HALT, OSC3: OFF	Without panel load		1.5	2.5	µA
		During operation *1, OSC3: OFF			2.4	4.0	µA
		During operation at 1MHz *1, OSC3 (Ceramic): ON			50	80	µA
		During operation at 1MHz *1, OSC3 (CR): ON			85	130	µA
Current consumption (heavy load protection mode)	I_{OP2}	During HALT, OSC3: OFF	Without panel load		10.5	15.0	µA
		During operation *1, OSC3: OFF			11.5	17.0	µA
		During operation at 1MHz *1, OSC3 (Ceramic): ON			60	95	µA
		During operation at 1MHz *1, OSC3 (CR): ON			95	145	µA

*1 The SVD circuit and analog comparator are in the OFF status.

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

S1C60N16 and S1C60A16 (OSC1 crystal oscillation circuit)

Unless otherwise specified:
VDD=3.0V, VSS=0V, Crystal: Q13MC146, CG=25pF, CD=built-in, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (VDD)	2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (VDD)	2.2			V
Built-in capacitance (drain)	CD	Including the parasitic capacitance inside the IC		15		pF
Frequency/voltage deviation	Δf/ΔV	VDD=2.2 to 3.6V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔCG	CG=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	Vhho	(VDD)			3.6	V
Permitted leak resistance	Rleak	Between OSC1 and VDD	200			MΩ

S1C60L16 (OSC1 crystal oscillation circuit)

Unless otherwise specified:
VDD=1.5V, VSS=0V, Crystal: Q13MC146, CG=25pF, CD=built-in, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (VDD)	1.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (VDD)	1.2			V
Built-in capacitance (drain)	CD	Including the parasitic capacitance inside the IC		15		pF
Frequency/voltage deviation	Δf/ΔV	VDD=1.2 to 1.8V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔCG	CG=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	Vhho	(VDD)			1.8	V
Permitted leak resistance	Rleak	Between OSC1 and VDD	200			MΩ

S1C60A16 (OSC3 CR oscillation circuit)

Unless otherwise specified:
VDD=3.0V, VSS=0V, RCR=40kΩ, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC3		-30	1MHz	30	%
Oscillation start voltage	Vsta	(VDD)	2.2			V
Oscillation start time	tsta	VDD=2.2 to 3.6V			3	ms
Oscillation stop voltage	Vstp	(VDD)	2.2			V

S1C60A16 (OSC3 ceramic oscillation circuit)

Unless otherwise specified:
VDD=3.0V, VSS=0V, Ceramic oscillator: 1MHz, CGC=CDC=100pF, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(VDD)	2.2			V
Oscillation start time	tsta	VDD=2.2 to 3.6V			5	ms
Oscillation stop voltage	Vstp	(VDD)	2.2			V

7.6 Serial Interface AC Characteristics

Clock synchronous master mode

• ***During 32 kHz operation***

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µs
Receiving data input set-up time	tsms	10			µs
Receiving data input hold time	tsmh	5			µs

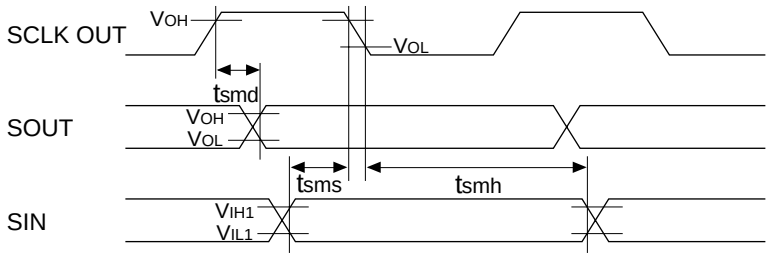
Clock synchronous slave mode

• ***During 32 kHz operation***

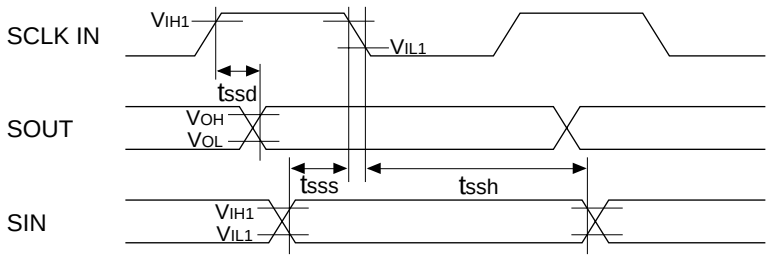
Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µs
Receiving data input set-up time	tsss	10			µs
Receiving data input hold time	tssh	5			µs

<Master mode>



<Slave mode>

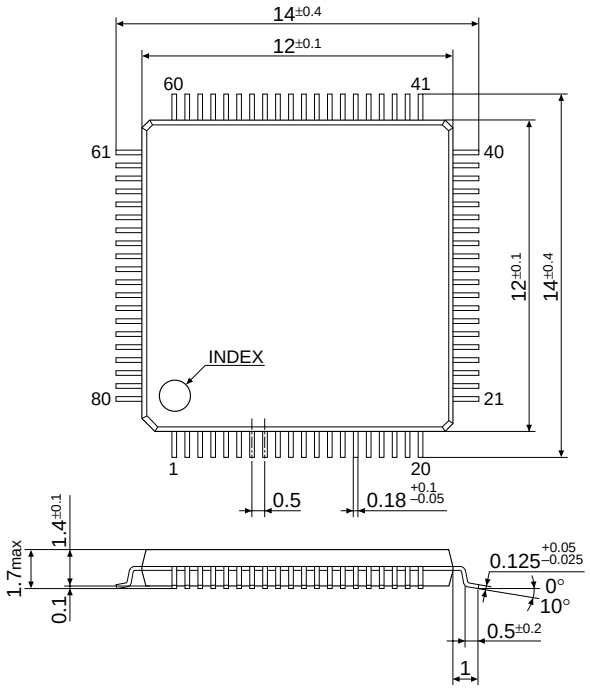


CHAPTER 8 PACKAGE

8.1 Plastic Package

QFP14-80pin

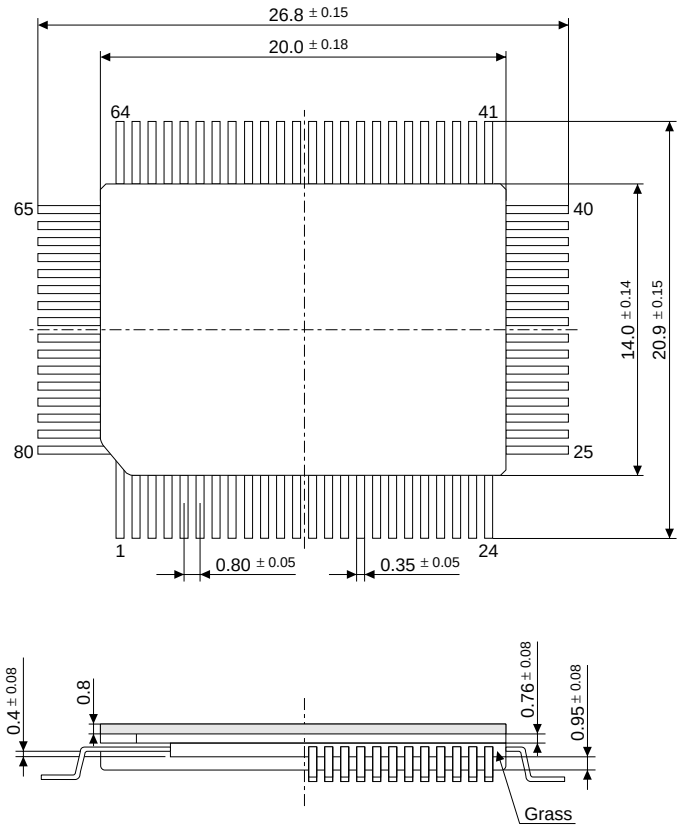
(Unit: mm)



8.2 Ceramic Package for Test Samples

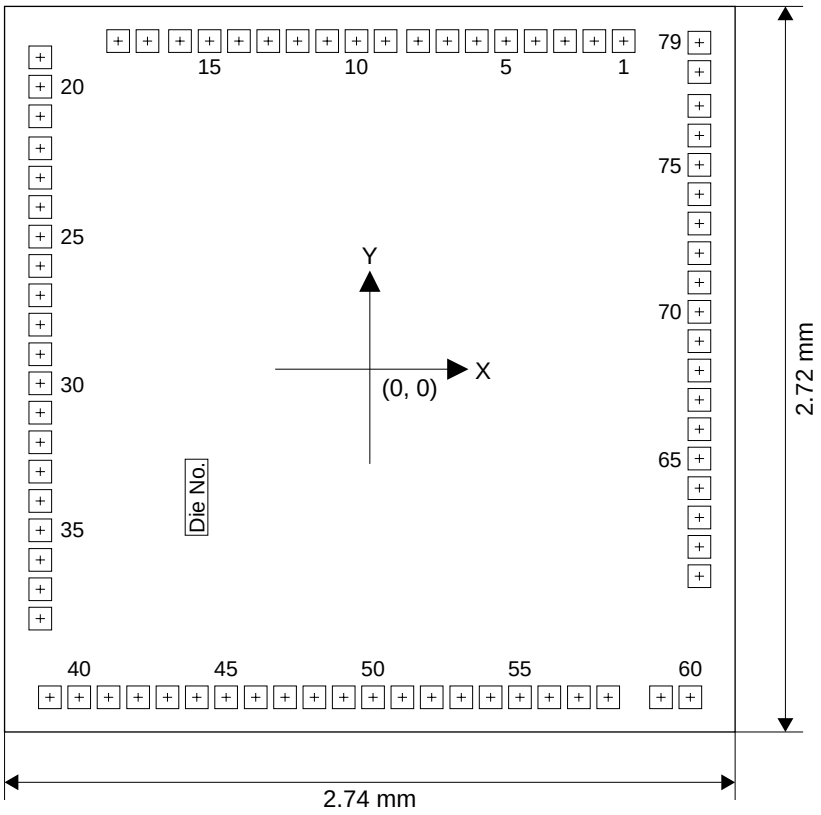
QFP5-80pin

(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400µm
Pad opening: 85µm

9.2 Pad Coordinates

(Unit: µm)

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	P13	952	1,230	28	OSC3	-1,236	167	55	SEG22	563	-1,230
2	P12	842	1,230	29	OSC4	-1,236	56	56	SEG21	673	-1,230
3	P11	732	1,230	30	V_{DD}	-1,236	-53	57	SEG20	784	-1,230
4	P10	622	1,230	31	V_{C3}	-1,236	-163	58	SEG19	894	-1,230
5	P03	511	1,230	32	V_{C2}	-1,236	-274	59	SEG18	1,092	-1,230
6	P02	401	1,230	33	V_{C1}	-1,236	-384	60	SEG17	1,202	-1,230
7	P01	291	1,230	34	CB	-1,236	-494	61	SEG16	1,236	-776
8	P00	181	1,230	35	CA	-1,236	-604	62	SEG15	1,236	-666
9	R13	59	1,230	36	COM3	-1,236	-715	63	SEG14	1,236	-556
10	R12	-50	1,230	37	COM2	-1,236	-825	64	SEG13	1,236	-446
11	R11	-160	1,230	38	COM1	-1,236	-935	65	SEG12	1,236	-335
12	R10	-271	1,230	39	COM0	-1,200	-1,230	66	SEG11	1,236	-225
13	R03	-381	1,230	40	SEG37	-1,090	-1,230	67	SEG10	1,236	-115
14	R02	-491	1,230	41	SEG36	-980	-1,230	68	SEG9	1,236	-5
15	R01	-601	1,230	42	SEG35	-869	-1,230	69	SEG8	1,236	105
16	R00	-712	1,230	43	SEG34	-759	-1,230	70	SEG7	1,236	215
17	K00	-834	1,230	44	SEG33	-649	-1,230	71	SEG6	1,236	325
18	K01	-944	1,230	45	SEG32	-539	-1,230	72	SEG5	1,236	435
19	K02	-1,236	1,169	46	SEG31	-428	-1,230	73	SEG4	1,236	546
20	K03	-1,236	1,059	47	SEG30	-318	-1,230	74	SEG3	1,236	656
21	K10	-1,236	948	48	SEG29	-208	-1,230	75	SEG2	1,236	766
22	V_{SS}	-1,236	828	49	SEG28	-98	-1,230	76	SEG1	1,236	876
23	AMPM	-1,236	718	50	SEG27	12	-1,230	77	SEG0	1,236	987
24	AMPP	-1,236	608	51	SEG26	122	-1,230	78	RESET	1,236	1,114
25	OSC1	-1,236	497	52	SEG25	232	-1,230	79	TEST	1,236	1,224
26	OSC2	-1,236	387	53	SEG24	343	-1,230	–			
27	V_{D1}	-1,236	277	54	SEG23	453	-1,230	–			

Revision History

Code No.	Page	Contents
404539503	1, 3, 4, 90	Package Deleted QFP5-80pin(S2)
	5	Option List: 3. MULTIPLE KEY ENTRY RESET (Old) TIME AUTHORIZE ..... ☐ 1. Use ☐ 2. Not Use (New) TIME AUTHORIZE ..... ☐ 1. Not Use ☐ 2. Use
	6	Option List: 17. LCD BIAS & POWER SOURCE (Old) S1C60N16 ..... ☐ 1. 1/3 Bias, Regulator Used, LCD 3 V ☐ 2. 1/3 Bias, Regulator Not Used, LCD 3 V ☐ 3. 1/2 Bias, Regulator Not Used, LCD 3 V S1C60L16 ..... ☐ 1. 1/3 Bias, Regulator Used, LCD 3 V ☐ 2. 1/2 Bias, Regulator Not Used, LCD 3 V (New) S1C60N16 ..... ☐ 1. 1/3 Bias, Regulator Used, LCD 3 V S1C60L16 ..... ☐ 1. 1/3 Bias, Regulator Used, LCD 3 V
	8	Power Supply (Old) The LCD system voltage regulator can be disabled by mask option. ... Fig. 2.1.2 External elements when LCD system voltage regulator is not used (New) The LCD system voltage regulator in the S1C60A16 can be disabled by mask option. ... Fig. 2.1.2 External elements when LCD system voltage regulator is not used (S1C60A16)
	9	Initial Reset: Configuration of initial reset circuit Modified Figure 2.2.1
	39	LCD Driver: Configuration of LCD driver (Old) Moreover, the 1/2 bias dynamic drive that uses three types of potential, V_{SS}, V_{C1} = V_{C2} and V_{C3}, can be selected by setting the mask option (drive duty can also be selected from 1/4, 1/3 or 1/2). (New) In the S1C60A16, the 1/2 bias dynamic drive that uses three types of potential, V_{SS}, V_{C1} = V_{C2} and V_{C3}, can be selected by setting the mask option (drive duty can also be selected from 1/4, 1/3 or 1/2).
	46	LCD Driver: Drive bias (Old) For the drive bias of the S1C60N16 or the S1C60L16, either 1/3 bias or 1/2 bias can be selected by the mask option. (New) For the drive bias of the S1C60A16, either 1/3 bias or 1/2 bias can be selected by the mask option.

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Document Code: 404539503
First Issue October 2002
Revised March 2011 in JAPAN Ⓛ