EPSON
EXCEED YOUR VISION

# S1C63709

## 4-bit Single Chip Microcomputer

- **High Performance 4-bit Core CPU S1C63000**
- **LCD Driver (64 SEG × 8 COM)**
- **Motor Driver**
- **Solar Charge-Control Circuit**
- **Low Current Consumption (0.15 µA/HALT)**
- **Low Voltage Operation**

## ■ DESCRIPTIONS

The S1C63709 is a microcomputer which consists of a high-performance 4-bit CPU S1C63000 as the core CPU, ROM (12,288 words × 13 bits), RAM (2,048 words × 4 bits), serial interface, 2-channel motor driver, solar charging circuit, an LCD driver that can drive a maximum 64 segments × 8 commons, sound generator and time base counters. The S1C63709 features low current consumption, this makes it suitable for solar-powered radio-controlled watches.

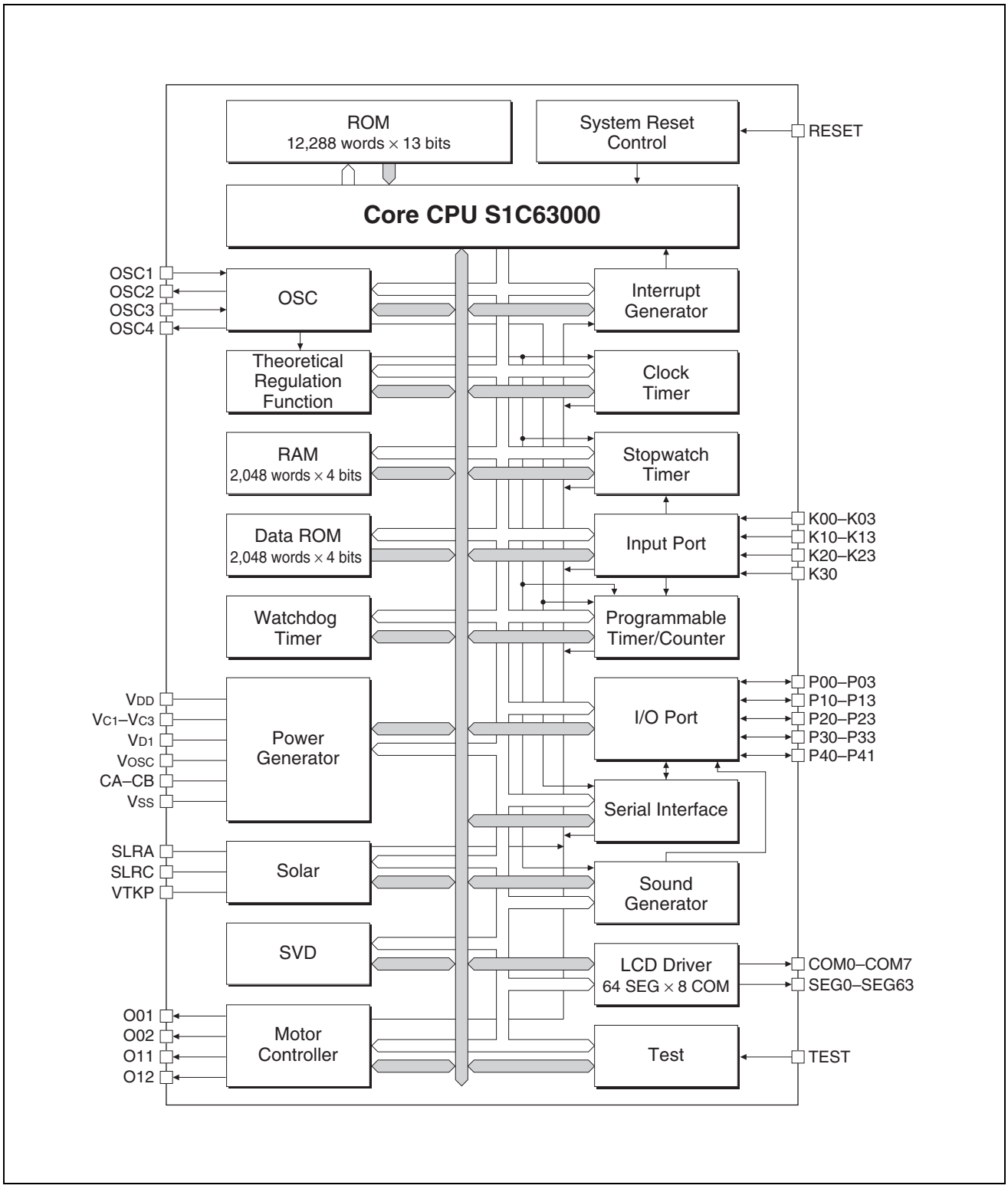
## ■ FEATURES

- Core CPU ..... 4-bit CMOS core CPU S1C63000
- OSC1 oscillation circuit ..... 32.768 kHz (Typ.) crystal oscillation circuit
- OSC3 oscillation circuit ..... 4 MHz (Typ.) ceramic, 1.1 MHz (Typ.) CR (external R)
  or 200 kHz (Typ.) CR (built-in R) oscillation circuit (∗1)
- Instruction set ..... Basic instruction: 47 types (411 instructions with all)
  Addressing mode: 8 types
- Instruction execution time ..... During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec
  During operation at 4 MHz: 0.5 µsec 1.0 µsec 1.5 µsec
- ROM capacity ..... Code ROM: 12,288 words × 13 bits
  Data ROM: 2,048 words × 4 bits
- RAM capacity ..... Data memory: 2,048 words × 4 bits
  Display memory: 160 words × 4 bits
- Input port ..... 4 bits for general-purpose input ports
  4 bits for crown switches
  5 bits for theoretical regulation
  (pull-down resistors may be supplemented ∗1)
- I/O port ..... 18 bits (usable as special output and serial I/F ports ∗2)
- Serial interface ..... 1 port (8-bit clock synchronous system)
- LCD driver ..... 64 segments × 4, 5 or 8 commons (∗2)
- Time base counter ..... Clock timer
  Stopwatch timer (1/1000 sec, with direct key input function)
- Programmable timer ..... 8 bits × 3 ch. or 16 bits × 1 ch. + 8 bits × 1 ch. (∗2)
- Watchdog timer ..... Built-in
- Sound generator ..... With envelope and 1-shot output functions
- Motor driver ..... 2 channels
- Solar charge-control circuit ..... Built in
- Supply voltage detection (SVD) circuit ... 24 detection voltage values are configurable (∗2)
- External interrupt ..... Input port interrupt: 2 systems
- Internal interrupt ..... Clock timer interrupt: 7 systems
  Stopwatch timer interrupt: 4 systems
  Programmable timer interrupt: 3 systems
  Serial interface interrupt: 1 system
  Motor driver interrupt: 2 systems
  Solar interrupt: 1 system
- Power supply voltage ..... 1.0 to 3.6 V (when CR (built-in R) oscillation circuit is selected)
  2.1 to 3.6 V (when CR (external R) or ceramic oscillation circuit is selected)

- Operating temperature range ..... -20 to 70ºC
- Current consumption (Typ.) ..... 32 kHz HALT state (3.0 V, LCD off) 0.15 µA
  32 kHz run state (3.0 V, LCD on) 3.50 µA
- Shipping form ..... QFP20-144pin (plastic) or chip

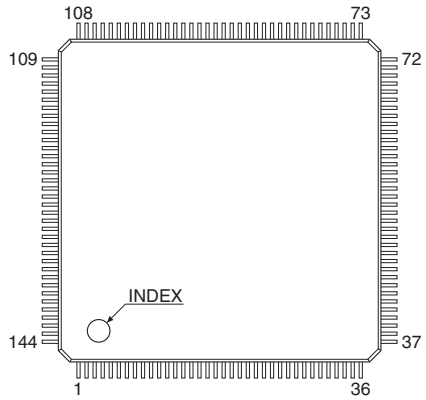
∗1: Can be selected with mask option ∗2: Can be selected with software

## ■ BLOCK DIAGRAM



## ■ PIN LAYOUT DIAGRAM

QFP20-144pin




| No. | Pin name | No. | Pin name | No. | Pin name | No. | Pin name |
|---|---|---|---|---|---|---|---|
| 1 | N.C. | 37 | COM0 | 73 | N.C. | 109 | N.C. |
| 2 | N.C. | 38 | COM1 | 74 | N.C. | 110 | N.C. |
| 3 | SEG0 | 39 | COM2 | 75 | SEG32 | 111 | COM4 |
| 4 | SEG1 | 40 | COM3 | 76 | SEG33 | 112 | COM5 |
| 5 | SEG2 | 41 | CA | 77 | SEG34 | 113 | COM6 |
| 6 | SEG3 | 42 | CB | 78 | SEG35 | 114 | COM7 |
| 7 | SEG4 | 43 | $V_{C1}$ | 79 | SEG36 | 115 | P41 |
| 8 | SEG5 | 44 | $V_{C2}$ | 80 | SEG37 | 116 | P40 |
| 9 | SEG6 | 45 | $V_{C3}$ | 81 | SEG38 | 117 | P33 |
| 10 | SEG7 | 46 | $V_{DD}$ | 82 | SEG39 | 118 | P32 |
| 11 | SEG8 | 47 | $V_{OSC}$ | 83 | SEG40 | 119 | P31 |
| 12 | SEG9 | 48 | N.C. | 84 | SEG41 | 120 | P30 |
| 13 | SEG10 | 49 | OSC1 | 85 | SEG42 | 121 | P23 |
| 14 | SEG11 | 50 | OSC2 | 86 | SEG43 | 122 | P22 |
| 15 | SEG12 | 51 | N.C. | 87 | SEG44 | 123 | P21 |
| 16 | SEG13 | 52 | $V_{D1}$ | 88 | SEG45 | 124 | P20 |
| 17 | SEG14 | 53 | OSC3 | 89 | SEG46 | 125 | $V_{DD}$ |
| 18 | SEG15 | 54 | OSC4 | 90 | SEG47 | 126 | SLRA |
| 19 | SEG16 | 55 | N.C. | 91 | SEG48 | 127 | VTKP |
| 20 | SEG17 | 56 | $V_{SS}$ | 92 | SEG49 | 128 | SLRC |
| 21 | SEG18 | 57 | TEST | 93 | SEG50 | 129 | $V_{SS}$ |
| 22 | SEG19 | 58 | RESET | 94 | SEG51 | 130 | $V_{DD}$ |
| 23 | SEG20 | 59 | K00 | 95 | SEG52 | 131 | O01 |
| 24 | SEG21 | 60 | K01 | 96 | SEG53 | 132 | N.C. |
| 25 | SEG22 | 61 | K02 | 97 | SEG54 | 133 | O02 |
| 26 | SEG23 | 62 | K03 | 98 | SEG55 | 134 | O11 |
| 27 | SEG24 | 63 | K10 | 99 | SEG56 | 135 | O12 |
| 28 | SEG25 | 64 | K11 | 100 | SEG57 | 136 | $V_{SS}$ |
| 29 | SEG26 | 65 | K12 | 101 | SEG58 | 137 | P13 |
| 30 | SEG27 | 66 | K13 | 102 | SEG59 | 138 | P12 |
| 31 | SEG28 | 67 | K20 | 103 | SEG60 | 139 | P11 |
| 32 | SEG29 | 68 | K21 | 104 | SEG61 | 140 | P10 |
| 33 | SEG30 | 69 | K22 | 105 | SEG62 | 141 | P03 |
| 34 | SEG31 | 70 | K23 | 106 | SEG63 | 142 | P02 |
| 35 | N.C. | 71 | K30 | 107 | N.C. | 143 | P01 |
| 36 | N.C. | 72 | N.C. | 108 | N.C. | 144 | P00 |

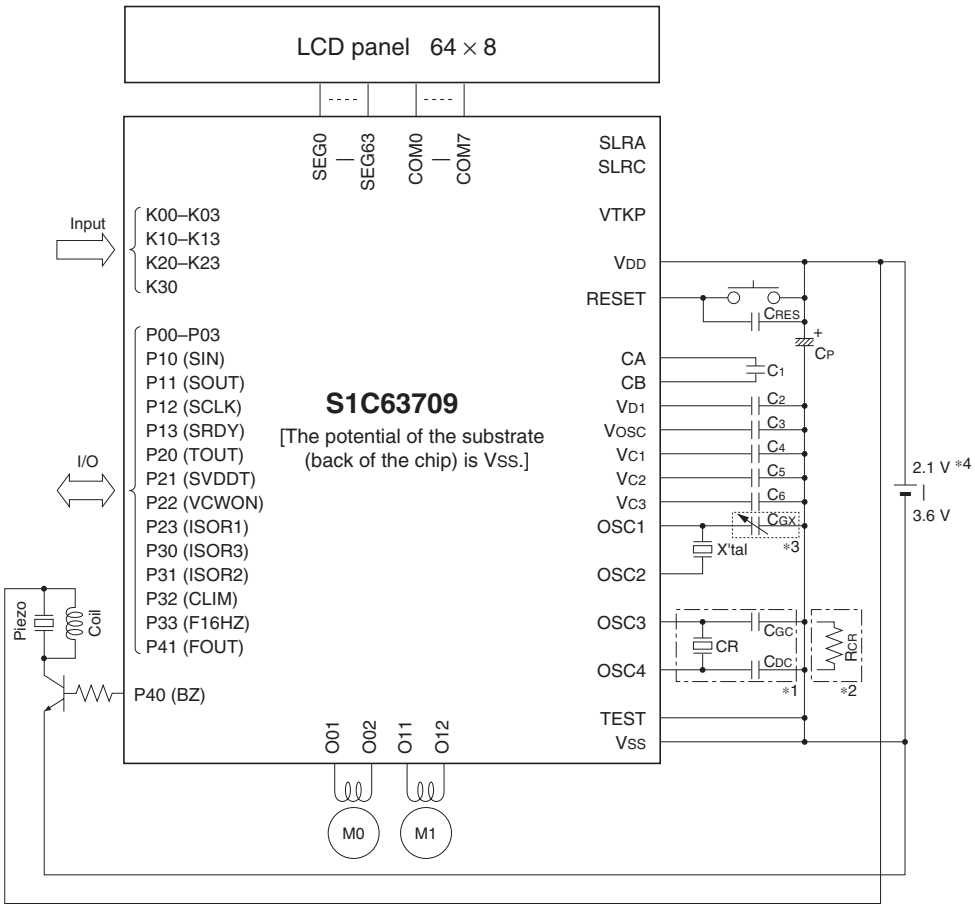
N.C. : No Connection

## ■ PIN DESCRIPTION

| Pin name | Pin No. | I/O | Function |
|---|---|---|---|
| $V_{DD}$ | 46, 125, 130 | – | Power (+) supply pin |
| $V_{SS}$ | 56, 129, 136 | – | Power (–) supply pin |
| $V_{D1}$ | 52 | – | Internal logic system regulated voltage output pin |
| $V_{OSC}$ | 47 | – | OSC1 oscillation system regulated voltage output pin |
| $V_{C1}$–$V_{C3}$ | 43–45 | – | LCD system power supply pins |
| CA, CB | 41, 42 | – | LCD system voltage boosting/halving capacitor connecting pins |
| OSC1 | 49 | I | Crystal oscillation input pin |
| OSC2 | 50 | O | Crystal oscillation output pin |
| OSC3 | 53 | I | Ceramic or CR oscillation input pin (selectable by mask option) |
| OSC4 | 54 | O | Ceramic or CR oscillation output pin (selectable by mask option) |
| K00–K03 | 59–62 | I | Input port pins |
| K10–K13 | 63–66 | I | Input port pins |
| K20–K23 | 67–70 | I | Input port pins |
| K30 | 71 | I | Input port pin |
| P00–P03 | 144–141 | I/O | I/O port pins |
| P10/SIN | 140 | I/O | I/O port or serial I/F data input pin (selected by software) |
| P11/SOUT | 139 | I/O | I/O port or serial I/F data output pin (selected by software) |
| P12/SCLK | 138 | I/O | I/O port or serial I/F clock I/O pin (selected by software) |
| P13/SRDY | 137 | I/O | I/O port or serial I/F ready signal output pin (selected by software) |
| P20/TOUT | 124 | I/O | I/O port or TOUT clock output pin (selected by software) |
| P21/SVDDT | 123 | I/O | I/O port or SVDDT signal monitor output pin (selected by software) |
| P22/VCWON | 122 | I/O | I/O port or VCWON signal monitor output pin (selected by software) |
| P23/ISOR1 | 121 | I/O | I/O port or ISOR1 signal monitor output pin (selected by software) |
| P30/ISOR3 | 120 | I/O | I/O port or ISOR3 signal monitor output pin (selected by software) |
| P31/ISOR2 | 119 | I/O | I/O port or ISOR2 signal monitor output pin (selected by software) |
| P32/CLIM | 118 | I/O | I/O port or CLIM signal monitor output pin (selected by software) |
| P33/F16HZ | 117 | I/O | I/O port or 16 Hz clock output pin (selected by software) |
| P40/BZ | 116 | I/O | I/O port or buzzer output pin (selected by software) |
| P41/FOUT | 115 | I/O | I/O port or FOUT clock output pin (selected by software) |
| COM0–COM7 | 37–40, 111–114 | O | LCD common output pins (1/4, 1/5 or 1/8 duty is selectable by software) |
| SEG0–SEG63 | 3–34, 75–106 | O | LCD segment output pins |
| O01, O02 | 131, 133 | O | Motor 0 drive pulse output pins |
| O11, O12 | 134, 135 | O | Motor 1 drive pulse output pins |
| SLRA | 126 | – | Solar cell anode connecting pin |
| SLRC | 128 | – | Solar cell cathode connecting pin |
| VTKP | 127 | – | Solar voltage detection pin |
| RESET | 58 | I | Initial reset input pin |
| TEST | 57 | I | Testing input pin |

## ■ BASIC EXTERNAL CONNECTION DIAGRAM

● When a primary cell is used

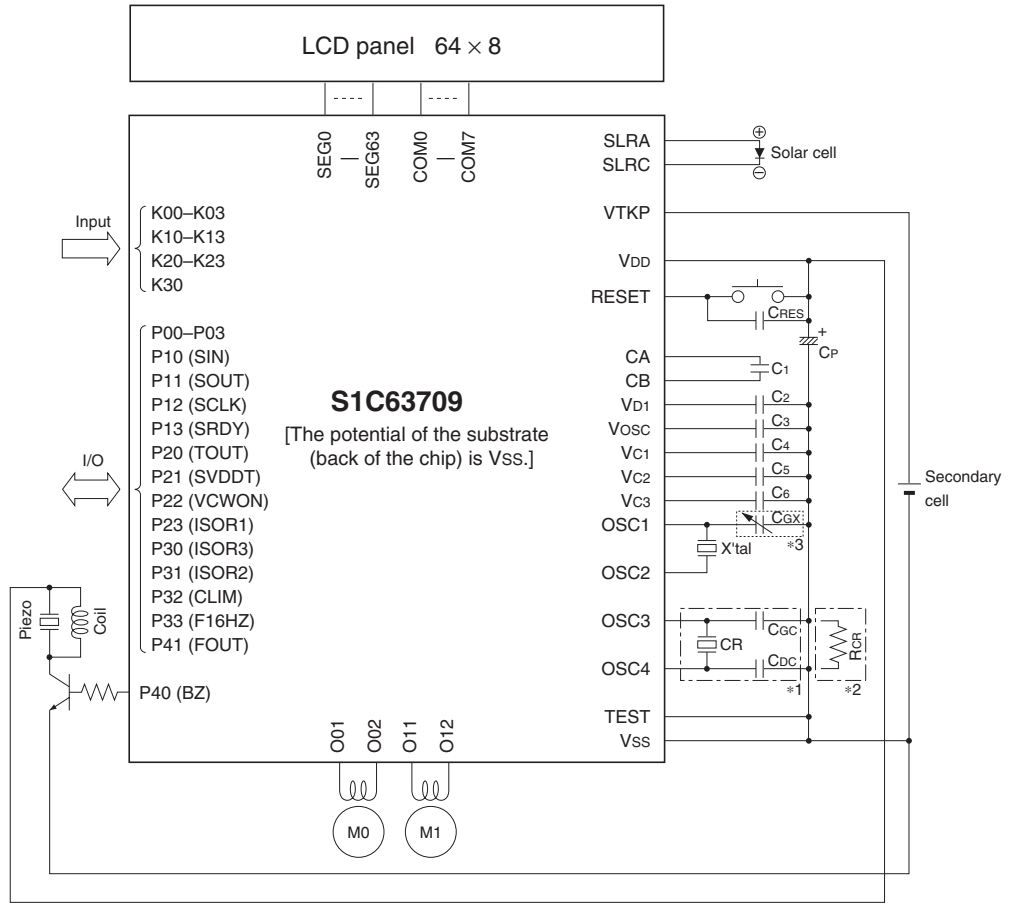



| | | |
|---|---|---|
| X'tal | Crystal oscillator | 32.768 kHz, CI(Max.) = 35 kΩ, CL(Typ.) = 6 pF |
| CGX | Trimmer capacitor | 0–20 pF |
| CR | Ceramic oscillator | 4 MHz (3.0 V) |
| CGC | Gate capacitor | 30 pF |
| CDC | Drain capacitor | 30 pF |
| RCR | Resistor for OSC3 CR oscillation | 75 kΩ (1.1 MHz) |
| C1–C6 | Capacitor | 0.2 µF |
| CP | Capacitor | 3.3 µF |
| CRES | RESET terminal capacitor | 0.1 µF |

Note: The above table is simply an example, and is not guaranteed to work.

*1: Ceramic oscillation
*2: CR oscillation (external R)
*3: CG regulation
*4: 1.0–3.6 V when OSC3 is not used or OSC3 CR oscillation (built-in R) is used

● When a solar cell is used




| | | |
|---|---|---|
| X'tal | Crystal oscillator | 32.768 kHz, CI(Max.) = 35 kΩ, CL(Typ.) = 6 pF |
| CGX | Trimmer capacitor | 0–20 pF |
| CR | Ceramic oscillator | 4 MHz (3.0 V) |
| CGC | Gate capacitor | 30 pF |
| CDC | Drain capacitor | 30 pF |
| RCR | Resistor for OSC3 CR oscillation | 75 kΩ (1.1 MHz) |
| C1–C6 | Capacitor | 0.2 µF |
| CP | Capacitor | 4.7 µF |
| CRES | RESET terminal capacitor | 0.1 µF |

*1: Ceramic oscillation
*2: CR oscillation (external R)
*3: CG regulation

Note: The above table is simply an example, and is not guaranteed to work.



**SEIKO EPSON CORPORATION**
SEMICONDUCTOR OPERATIONS DIVISION

■ EPSON Electronic Devices Website
**http://www.epson.jp/device/semicon_e**

**IC Sales Dept.**
**IC International Sales Group**
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

Document code: 410776901
Issue August, 2007
Printed in Japan Ⓛ