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S1C63632
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.0

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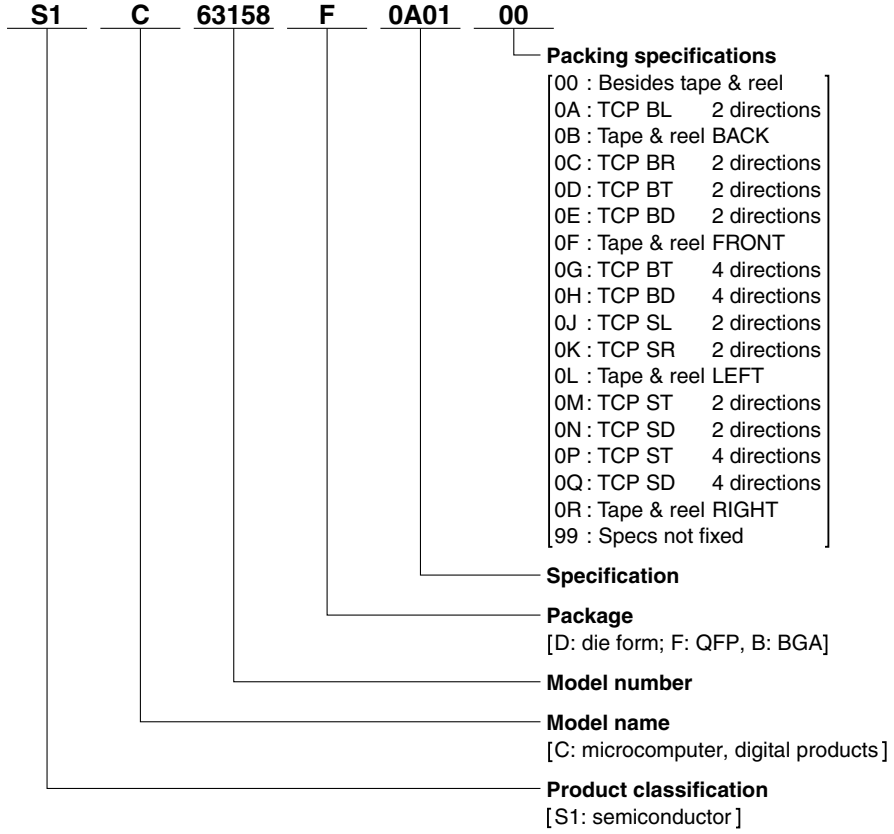
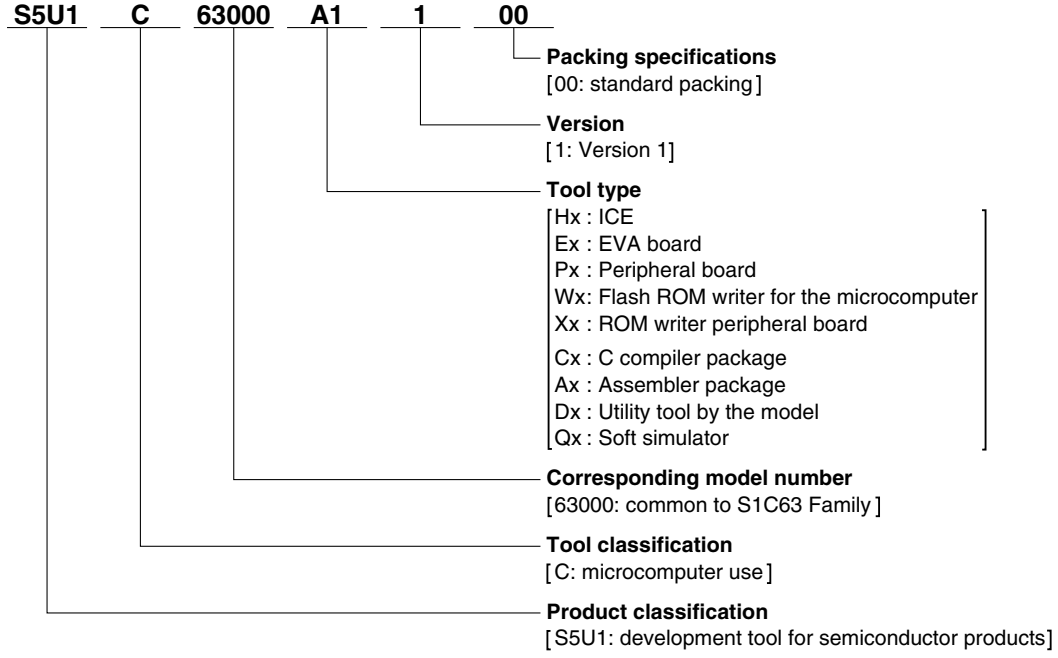


Development tools



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CHAPTER 1 OUTLINE

The S1C63632 is a microcomputer which has a 4-bit CPU S1C63000 as the core CPU, ROM (31,744 words × 13 bits), RAM (8,192 words × 4 bits), multiply-divide circuit, serial interface, watchdog timer, programmable timer, time base counters (2 systems), a dot matrix LCD driver that can drive a maximum 1,536 dots of LCD panel, and an R/f converter that can measure temperature and humidity using sensors such as a thermistor. The S1C63632 features low current consumption, this makes it suitable for battery driven clocks and watches with temperature and humidity measurement functions.

1.1 Features

OSC1 oscillation circuit	32.768 kHz (Typ.) crystal oscillation circuit
OSC3 oscillation circuit	4.2 MHz (Max.) ceramic or 1.8 MHz (Typ.) CR oscillation circuit (*1)
Instruction set	Basic instruction: 47 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time	During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec During operation at 4 MHz: 0.5 µsec 1 µsec 1.5 µsec
ROM capacity	Code ROM: 31,744 words × 13 bits Data ROM: 4,096 words × 4 bits
RAM capacity	Data memory: 8,192 words × 4 bits Display memory: 2,048 bits
I/O port	24 bits (pull-down resistors may be incorporated*1 Shared with 4 serial I/F I/O pins, 4 R/f converter I/O pins, and 6 special output pins *2)
Serial interface	1 port (8-bit clock synchronous system)
LCD driver	48 segments × 32 commons, 56 segments × 24 commons, or 64 segments × 16 commons (*2)
Time base counter	Clock timer Stopwatch timer (1/1000 sec, with direct key input function)
Programmable timer	16-bit timer × 4 ch. (each 16-bit timer is configurable to two 8-bit timer channels *2)
Watchdog timer	Built-in
Sound generator	With envelope and 1-shot output functions
R/f converter	2 ch., CR oscillation type, 20-bit counter Supports resistive humidity sensors
Multiply-divide circuit	8-bit accumulator × 1 ch. Multiplication: 8 bits × 8 bits → 16-bit product Division: 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder
Supply voltage detection (SVD) circuit	Programmable 16 detection voltage levels (*2)
External interrupt	Key input interrupt: 8 systems
Internal interrupt	Clock timer interrupt: 8 systems Stopwatch timer interrupt: 4 systems Programmable timer interrupt: 16 systems Serial interface interrupt: 1 system R/f converter interrupt: 3 systems
Power supply voltage	1.6 to 5.5 V
Operating temperature range	-40 to 85°C
Current consumption (Typ.)	During SLEEP (32 kHz) 0.08 µA During HALT (32 kHz) 0.6 µA During running (32 kHz) 2.5 µA During running (4 MHz) 320 µA
Shipment form	QFP20-144pin, VFBGA10H-144 or die form

*1: Can be selected with mask option *2: Can be selected with software

1.2 Block Diagram

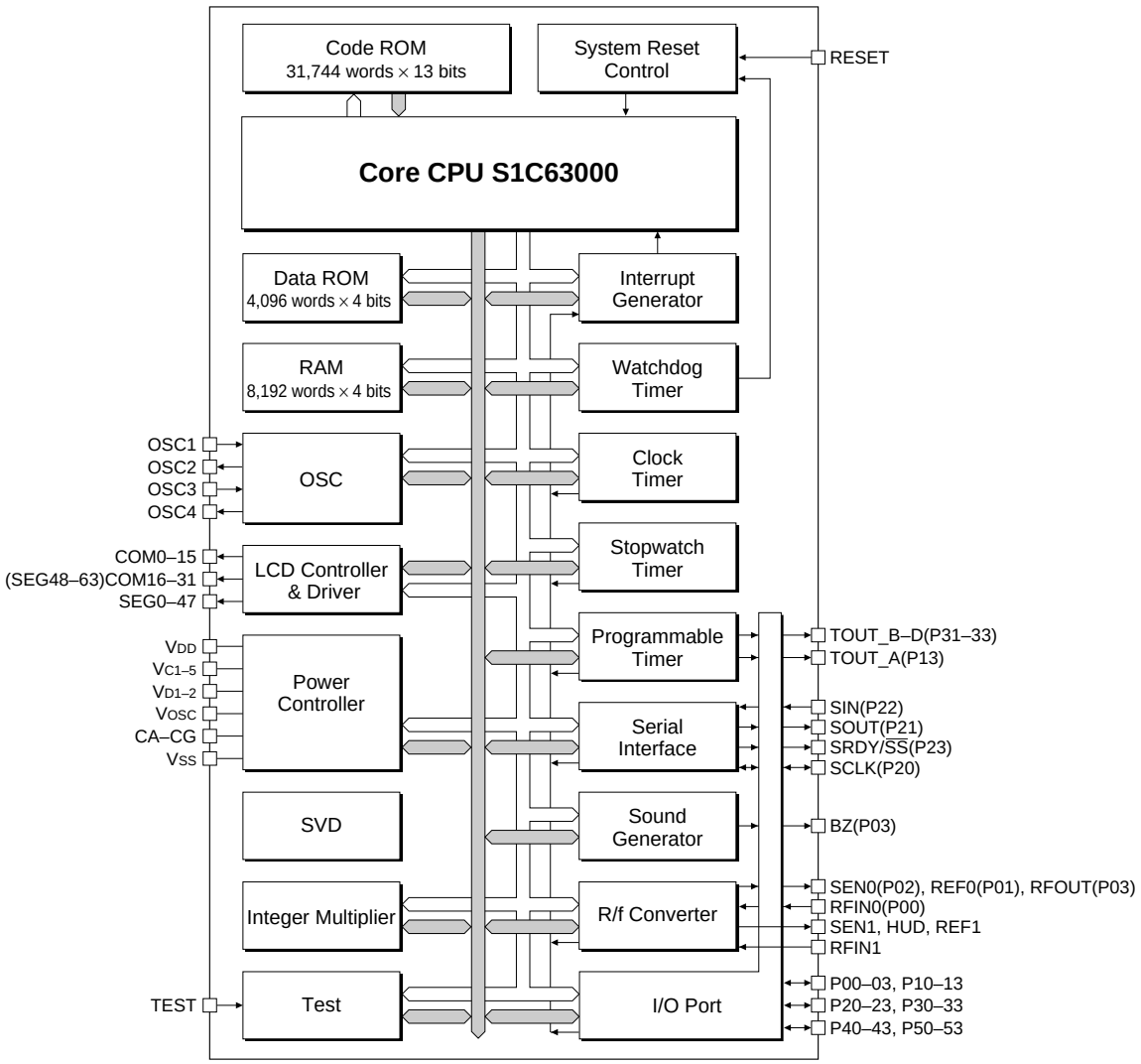


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP20-144pin

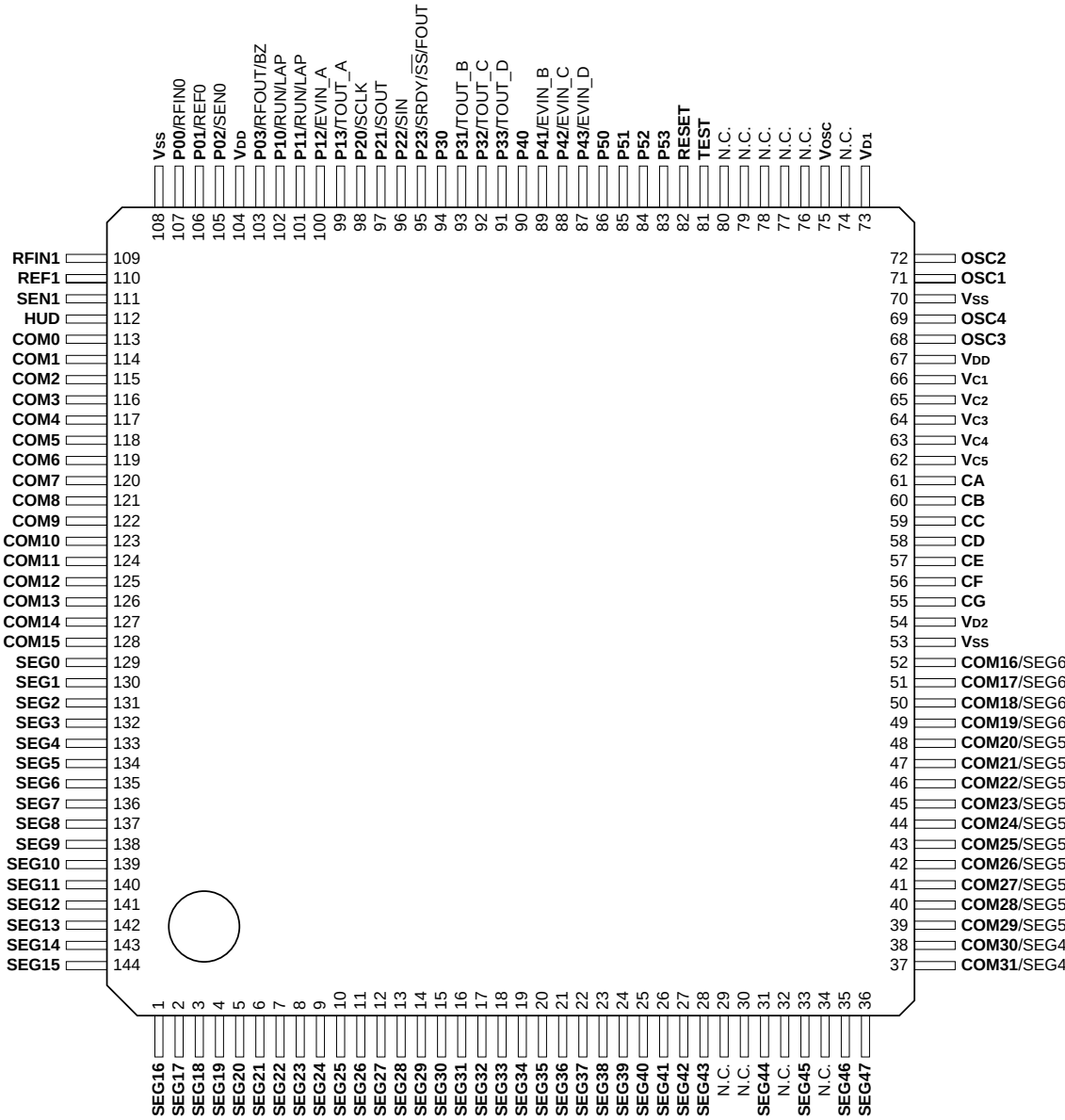
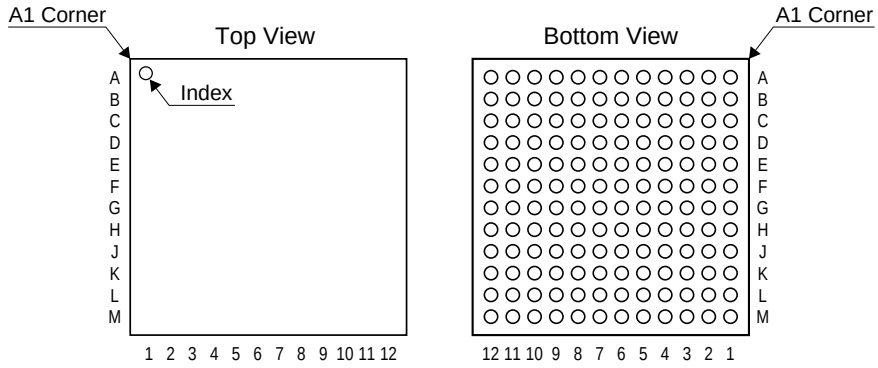


Fig. 1.3.1 Pin layout diagram (QFP20-144pin)

VFBGA10H-144



	1	2	3	4	5	6	7	8	9	10	11	12	
A	N.C.	**SEG12**	**SEG9**	**SEG5**	**SEG1**	**COM11**	**COM6**	**COM2**	**HUD**	**SEN1**	**RFIN1**	N.C.	A
B	**SEG15**	**SEG14**	**SEG11**	**SEG6**	**SEG2**	**COM12**	**COM7**	**COM3**	**COM1**	**REF1**	**P00** RFIN0	**P01** REF0	B
C	**SEG16**	**SEG13**	**SEG10**	**SEG8**	**SEG4**	**COM13**	**COM8**	**COM4**	**COM0**	**VSS**	**P02** SEN0	**VDD**	C
D	**SEG18**	**SEG17**	**SEG21**	**SEG7**	**SEG3**	**COM14**	**COM9**	**COM5**	**P12** EVIN_A	**P11** RUN LAP	**P10** RUN LAP	**P03** RFOUT BZ	D
E	**SEG20**	**SEG19**	**SEG22**	**SEG26**	**SEG0**	**COM15**	**COM10**	**P13** TOUT_A	**P20** SCLK	**P21** SOUT	**P22** SIN	**P23** SRDY $\overline{SS}$ FOUT	E
F	**SEG23**	**SEG24**	**SEG25**	**SEG27**	**SEG30**	**SEG31**	**P30**	**P31** TOUT_B	**P41** EVIN_B	**P40**	**P32** TOUT_C	**P33** TOUT_D	F
G	**SEG28**	**SEG29**	**SEG32**	**SEG35**	**SEG36**	**SEG39**	**VSS**	**P52**	**P51**	**P42** EVIN_C	**P50**	**P43** EVIN_D	G
H	**SEG33**	**SEG34**	**SEG40**	**SEG42**	**COM20** SEG59	**COM16** SEG63	**CG**	**VC3**	N.C.	**P53**	**RESET**	**TEST**	H
J	**SEG37**	**SEG38**	**SEG43**	**COM28** SEG51	**COM21** SEG58	**COM17** SEG62	**CF**	**VC4**	N.C.	N.C.	N.C.	N.C.	J
K	**SEG41**	**SEG44**	**SEG45**	**COM27** SEG52	**COM22** SEG57	**COM18** SEG61	**CE**	**VC5**	**VC2**	**VSS**	**VOSC**	N.C.	K
L	**SEG46**	**SEG47**	**COM29** SEG50	**COM26** SEG53	**COM24** SEG55	**COM19** SEG60	**CD**	**CA**	**VC1**	**OSC4**	**OSC2**	**VD1**	L
M	N.C.	**COM31** SEG48	**COM30** SEG49	**COM25** SEG54	**COM23** SEG56	**VD2**	**CC**	**CB**	**VDD**	**OSC3**	**OSC1**	N.C.	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Top View

Fig. 1.3.2 Pin layout diagram (VFBGA10H-144)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.			I/O	Function
	Die	QFP	VFBGA		
V_{DD}	63, 94	67, 104	C12, M9	–	Power (+) supply pins
V_{SS}	49, 66, 98	53, 70, 108	C10, G7, K10	–	Power (–) supply pins
V_{D1}	69	73	L12	–	Internal logic voltage regulator output pin
V_{OSC}	70	75	K11	–	Crystal oscillation circuit operating voltage output pin
V_{D2}	50	54	M6	–	Power supply voltage booster/halver output pin
V_{C1}–V_{C5}	62–58	66–62	L9, K9, H8, J8, K8	–	LCD drive voltage output pins
CA–CE	57–53	61–57	L8, M8, M7, L7, K7	–	LCD system voltage boost capacitor connecting pins
CF, CG	52, 51	56, 55	J7, H7	–	Power supply voltage boost/halving capacitor connecting pins
OSC1	67	71	M11	I	Crystal oscillation input pin
OSC2	68	72	L11	O	Crystal oscillation output pin
OSC3	64	68	M10	I	Ceramic or CR oscillation input pin (mask option)
OSC4	65	69	L10	O	Ceramic or CR oscillation output pin (mask option)
P00/RFIN0	97	107	B11	I	I/O port or R/f converter Ch.0 CR oscillation input pin (software switch)
P01/REF0	96	106	B12	I/O	I/O port or R/f converter Ch.0 reference oscillation output pin (software switch)
P02/SEN0	95	105	C11	I/O	I/O port or R/f converter Ch.0 CR oscillation output pin (software switch)
P03/RFOUT/BZ	93	103	D12	I/O	I/O port, R/f converter oscillation frequency output pin, or sound output pin (software switch)
P10/RUN/LAP	92	102	D11	I/O	I/O port or stopwatch Run/Lap input pin (software switch)
P11/RUN/LAP	91	101	D10	I/O	I/O port or stopwatch Run/Lap input pin (software switch)
P12/EVIN_A	90	100	D9	I/O	I/O port or event counter input pin (software switch)
P13/TOUT_A	89	99	E8	I/O	I/O port or programmable timer output pin (software switch)
P20/SCLK	88	98	E9	I/O	I/O port or serial I/F clock I/O pin (software switch)
P21/SOUT	87	97	E10	I/O	I/O port or serial I/F data output pin (software switch)
P22/SIN	86	96	E11	I/O	I/O port or serial I/F data input pin (software switch)
P23/SRDY/$\overline{SS}$ /FOUT	85	95	E12	I/O	I/O port, serial I/F ready signal output, $\overline{SS}$ signal input or FOUT clock output pin (software switch)
P30	84	94	F7	I/O	I/O port pin
P31/TOUT_B	83	93	F8	I/O	I/O port or programmable timer output pin (software switch)
P32/TOUT_C	82	92	F11	I/O	I/O port or programmable timer output pin (software switch)
P33/TOUT_D	81	91	F12	I/O	I/O port or programmable timer output pin (software switch)
P40	80	90	F10	I/O	I/O port pin
P41/EVIN_B	79	89	F9	I/O	I/O port or event counter input pin (software switch)
P42/EVIN_C	78	88	G10	I/O	I/O port or event counter input pin (software switch)
P43/EVIN_D	77	87	G12	I/O	I/O port or event counter input pin (software switch)
P50–P53	76–73	86–83	G11, G9, G8, H10	I/O	I/O port pins
COM0–COM15	103–118	113–128	∗1	O	LCD common output pins
COM16–COM31 /SEG63–SEG48	48–33	52–37	∗2	O	LCD common output or segment output pins (software switch)
SEG0–SEG47	119–134, 1–32	129–144, 1–28, 31, 33, 35, 36	∗3	O	LCD segment output pins
RFIN1	99	109	A11	I	R/f converter Ch.1 CR oscillation input pin
REF1	100	110	B10	O	R/f converter Ch.1 reference oscillation output pin
SEN1	101	111	A10	O	R/f converter Ch.1 CR oscillation output pin
HUD	102	112	A9	O	R/f converter AC-bias oscillation output pin for humidity sensor
RESET	72	82	H11	I	Initial reset input pin
TEST	71	81	H12	I	Test input pin

∗1 COM0–COM15: C9, B9, A8, B8, C8, D8, A7, B7, C7, D7, E7, A6, B6, C6, D6, E6
∗2 COM16/SEG63–COM31/SEG48: H6, J6, K6, L6, H5, J5, K5, M5, L5, M4, L4, K4, J4, L3, M3, M2
∗3 SEG0–SEG47: E5, A5, B5, D5, C5, A4, B4, D4, C4, A3, C3, B3, A2, C2, B2, B1, C1, D2, D1, E2, E1, D3, E3, F1, F2, F3, E4, F4, G1, G2, F5, F6, G3, H1, H2, G4, G5, J1, J2, G6, H3, K1, H4, J3, K2, K3, L1, L2

1.5 Mask Option

Mask options shown below are provided for the S1C63632. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator winfog, that has been prepared as the development software tool of S1C63632, is used for this selection. Mask pattern of the IC is finally generated based on the data created by the winfog. Refer to the "S5U1C63000A Manual" for the winfog.

<Outline of the mask option>

(1) OSC1 oscillation circuit

The OSC1 oscillator type is fixed at crystal oscillation. Refer to Section 4.4.3, "OSC1 oscillation circuit", for details.

(2) OSC3 oscillation circuit

The OSC3 oscillator type can be selected from ceramic oscillation or CR oscillation (external R). Refer to Section 4.4.4, "OSC3 oscillation circuit", for details.

(3) RESET terminal pull-down resistor

This option is used to select whether an internal pull-down resistor is incorporated into the RESET input port. Refer to Section 2.2.1, "Reset terminal (RESET)", for details.

(4) I/O port pull-down resistor

This option is used to select whether an internal pull-down resistor that will be enabled in input mode is incorporated into each I/O port (P00–P03, P10–P13, P20–P23, P30–P33, P40–P43, P50–P53). Refer to Section 4.5.2, "Mask option", for details.

(5) Output specification of the I/O port

This option is used to select either complementary output or P-channel open drain output as the output cell type of each I/O port (P00–P03, P10–P13, P20–P23, P30–P33, P40–P43, P50–P53). Refer to Section 4.5.2, "Mask option", for details.

(6) Multiple key entry reset function (by simultaneous high input to the P1x ports)

This option is used to select whether the function to reset the IC by pressing multiple keys simultaneously is implemented or not. A combination of the P1x ports (P10–P13) to be used for this function can also be selected. Refer to Section 2.2.2, "Simultaneous high input to P1x ports (P10–P13)", for details.

(7) Time authorize circuit for the multiple key entry reset function

When the multiple key entry reset option (option (6)) is selected, the time authorize circuit can also be incorporated. The time authorize circuit measures the high pulse width of the simultaneous input signals and asserts the reset signal if it is longer than the predetermined time. This option is not available when the multiple key entry reset option is not selected. Refer to Section 2.2.2, "Simultaneous high input to P1x ports (P10–P13)", for details.

(8) LCD drive power supply

This option is used to select the LCD drive bias from 1/5 bias (with V_{C2} reference voltage), 1/4 bias (with V_{C2} reference voltage) and 1/4 bias (with V_{C1} reference voltage). Refer to Section 4.6.2, "Power supply for LCD driving", for details.

<Option List>

The following is the option list for the S1C63632.
Multiple selections are available in each option item as indicated in the option list. Select the specifications that meet the target system and check the appropriate box. Be sure to record the specifications for unused functions too, according to the instructions provided.

1. OSC1 SYSTEM CLOCK

☐ 1. Crystal

2. OSC3 SYSTEM CLOCK

☐ 1. CR (external R)
☐ 2. Ceramic (4.2 MHz)

3. RESET PORT PULL DOWN RESISTOR

- RESET ☐ 1. Use ☐ 2. Not Use

4. I/O PORT PULL DOWN RESISTOR

- P00 ☐ 1. Use ☐ 2. Not Use
- P01 ☐ 1. Use ☐ 2. Not Use
- P02 ☐ 1. Use ☐ 2. Not Use
- P03 ☐ 1. Use ☐ 2. Not Use
- P10 ☐ 1. Use ☐ 2. Not Use
- P11 ☐ 1. Use ☐ 2. Not Use
- P12 ☐ 1. Use ☐ 2. Not Use
- P13 ☐ 1. Use ☐ 2. Not Use
- P20 ☐ 1. Use ☐ 2. Not Use
- P21 ☐ 1. Use ☐ 2. Not Use
- P22 ☐ 1. Use ☐ 2. Not Use
- P23 ☐ 1. Use ☐ 2. Not Use
- P30 ☐ 1. Use ☐ 2. Not Use
- P31 ☐ 1. Use ☐ 2. Not Use
- P32 ☐ 1. Use ☐ 2. Not Use
- P33 ☐ 1. Use ☐ 2. Not Use
- P40 ☐ 1. Use ☐ 2. Not Use
- P41 ☐ 1. Use ☐ 2. Not Use
- P42 ☐ 1. Use ☐ 2. Not Use
- P43 ☐ 1. Use ☐ 2. Not Use
- P50 ☐ 1. Use ☐ 2. Not Use
- P51 ☐ 1. Use ☐ 2. Not Use
- P52 ☐ 1. Use ☐ 2. Not Use
- P53 ☐ 1. Use ☐ 2. Not Use

5. I/O PORT OUTPUT SPECIFICATION

- P00 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P01 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P02 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P03 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P10 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P11 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P12 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P13 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P20 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P21 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P22 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P23 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P30 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P31 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P32 ☐ 1. Complementary ☐ 2. Pch Open Drain
- P33 ☐ 1. Complementary ☐ 2. Pch Open Drain

• P40	☐ 1. Complementary	☐ 2. Pch Open Drain
• P41	☐ 1. Complementary	☐ 2. Pch Open Drain
• P42	☐ 1. Complementary	☐ 2. Pch Open Drain
• P43	☐ 1. Complementary	☐ 2. Pch Open Drain
• P50	☐ 1. Complementary	☐ 2. Pch Open Drain
• P51	☐ 1. Complementary	☐ 2. Pch Open Drain
• P52	☐ 1. Complementary	☐ 2. Pch Open Drain
• P53	☐ 1. Complementary	☐ 2. Pch Open Drain

6. MULTIPLE KEY ENTRY RESET COMBINATION

☐ 1. Not Use
☐ 2. Use <P10, P11>
☐ 3. Use <P10, P11, P12>
☐ 4. Use <P10, P11, P12, P13>

7. MULTIPLE KEY ENTRY RESET TIME AUTHORIZE

☐ 1. Not Use
☐ 2. Use

8. LCD DRIVING POWER

☐ 1. 1/5 Bias, V_{C2} Reference
☐ 2. 1/4 Bias, V_{C2} Reference
☐ 3. 1/4 Bias, V_{C1} Reference

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

This section explains the operating voltage and the configuration of the internal power supply circuit of the S1C63632.

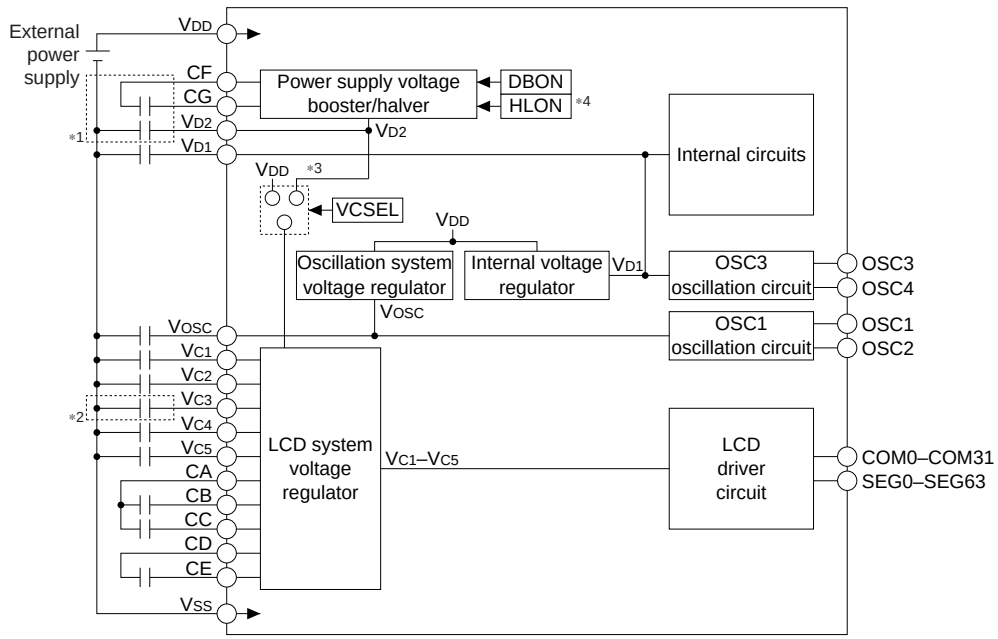
2.1.1 Operating voltage

The S1C63632 operating power voltage is as follows:

1.6 V to 5.5 V

2.1.2 Internal power supply circuit

The S1C63632 incorporates the power supply circuit shown in Figure 2.1.2.1. When voltage within the range described above is supplied to VDD (+) and VSS (GND), all the voltages needed for the internal circuits are generated internally in the IC.



*1 Leave these terminals open when the power supply voltage booster/halver is not used.
*2 Connect when the 1/5 bias LCD drive power is used. (Leave the terminal open when the 1/4 bias LCD drive power is used.)
*3 Can be selected as the power source for the LCD system voltage regulator when the power supply voltage booster/halver operates in boost mode.
*4 HLON is prohibited from use.

Fig. 2.1.2.1 Configuration of power supply circuit

The power supply circuit is broadly divided into four blocks.

Table 2.1.2.1 Power supply circuit

Circuit	Power supply circuit	Output voltage
Internal and oscillation system voltage regulators	Power supply voltage (VDD)	—
Internal circuits and OSC3 oscillation circuit	Internal voltage regulator	VD1
OSC1 oscillation circuit	Oscillation system voltage regulator	VOSC
LCD system voltage regulator	Power supply voltage booster/halver (halving mode)	VDD or VD2
LCD driver	LCD system voltage regulator	VC1—VC5

Note: The supply voltage booster/halver circuit can perform either boosting or halving the supply voltage at a time. The boosting and halving operations cannot be performed simultaneously.

Power supply voltage booster/halver circuit

The S1C63632 supports a wide supply voltage (V_{DD}) range that exceeds the operating voltage range of the voltage regulator (LCD system voltage regulator). The power supply voltage booster/halver circuit generates the V_{D2} voltage to drive the voltage regulators when the supply voltage V_{DD} is out of the operating voltage range of the voltage regulators.

Table 2.1.2.2 Relationship between supply voltage V_{DD} and voltage regulator operating voltage

Power supply voltage V_{DD}	Power source for LCD system voltage regulator
1.6 to 2.5 V	V_{D2} ($\approx V_{DD} \times 2$)
2.5 to 5.5 V	V_{DD}

When a V_{C2} reference voltage option for the LCD drive power supply is selected, the LCD system voltage regulator must be driven with a 2.5 V or more operating voltage. Therefore, the LCD system voltage regulator can be driven with V_{DD} if 2.5 V or more supply voltage V_{DD} is used. When the supply voltage V_{DD} is less than 2.5 V, drive the power supply voltage booster/halver in boost mode to generate V_{D2} and use it to drive the LCD system voltage regulator. The V_{D2} voltage generated in boost mode is about double the V_{DD} voltage level.

The V_{D2} voltage is not required when the power supply voltage (V_{DD}) is within the range from 2.5 V to 5.5 V (1.6 V to 5.5 V when the V_{C1} reference LCD drive power option is selected). In this case the power supply voltage booster/halver can be turned off.
The S1C63632 allows software to control the power supply voltage booster/halver and to select the power source of the voltage regulator. Refer to Section 4.2, "Power Control", for details.

Internal voltage regulator

The internal voltage regulator generates the operating voltage V_{D1} for driving the internal logic circuits and the OSC3 oscillation circuit.

Oscillation system voltage regulator

The oscillation system voltage regulator generates the V_{OSC} voltage for driving the OSC1 oscillation circuit and is provided separately with the internal voltage regulator to stabilize the oscillation and to reduce power consumption.

LCD system voltage regulator

The LCD system voltage regulator generates the LCD drive voltages V_{C1} to V_{C5}. See Chapter 7, "Electrical Characteristics" for the voltage values.
In the S1C63632, the LCD drive voltage is supplied to the built-in LCD driver which drives the LCD panel connected to the SEG and COM terminals.

Notes:
- *Be sure not to use the V_{D1}, V_{D2}, V_{OSC} and V_{C1} to V_{C5} terminal output voltages to drive external circuits.*
- *If V_{DD} equal to or less than 2.5 V is used as the power source for the LCD system voltage regulator, the V_{C1} to V_{C5} voltages cannot be generated within specifications (when a V_{C2} reference voltage option is selected).*
- *HLON is prohibited from use. Always be sure to set to "0".*

2.2 Initial Reset

The S1C63632 should be reset to initialize the internal circuits. There are two ways of doing this.

(1) External initial reset by the RESET terminal
(2) External initial reset by simultaneous high input to P10–P13 ports (mask option)

The circuits are initialized by either (1) or (2). When the power is turned on, be sure to initialize using the reset function. It is not guaranteed that the circuits are initialized by only turning the power on.

Figure 2.2.1 shows the configuration of the initial reset circuit.

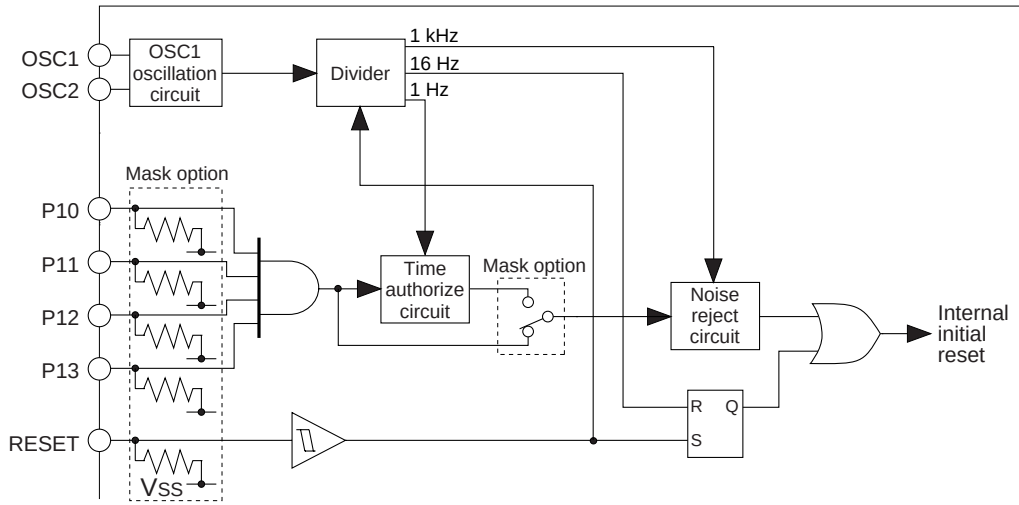


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a high level (V_{DD}). After that the initial reset is released by setting the reset terminal to a low level (V_{SS}) and the CPU starts operating.
The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 16 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 16,396/f_{OSC1} seconds (500 msec when f_{OSC1} = 32.768 kHz) is needed until the internal initial reset is released after the reset terminal goes to low level. Be sure to maintain a reset input of 0.1 msec or more. However, when turning the power on, the reset terminal should be set at a high level as in the timing shown in Figure 2.2.1.1.
Note that a reset pulse shorter than 100 nsec is rejected as noise.

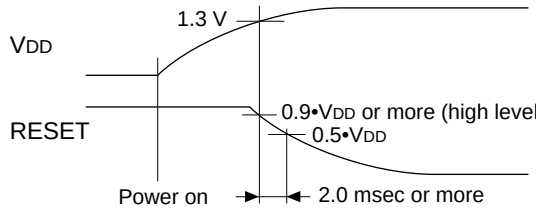


Fig. 2.2.1.1 Initial reset at power on

The reset terminal should be set to 0.9•V_{DD} or more (high level) until the supply voltage becomes 1.3 V or more.
After that, a level of 0.5•V_{DD} or more should be maintained more than 2.0 msec.

The reset terminal incorporates a pull-down resistor and a mask option is provided to select whether the resistor is used or not.

2.2.2 Simultaneous high input to P1x ports (P10–P13)

Another way of executing initial reset externally is to input high level signals simultaneously to the P1x ports (P10–P13) selected by a mask option.
Since this initial reset passes through the noise reject circuit, maintain the specified input port terminals at high level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) during normal operation. The noise reject circuit does not operate immediately after turning the power on until the oscillation circuit starts oscillating. Therefore, maintain the specified input port terminals at high level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) after oscillation starts.
Table 2.2.2.1 shows the combinations of P1x ports (P10–P13) that can be selected by a mask option.

Table 2.2.2.1 Combinations of P1x ports

1	Not use
2	P10∗P11
3	P10∗P11∗P12
4	P10∗P11∗P12∗P13

When, for instance, mask option 4 (P10∗P11∗P12∗P13) is selected, initial reset is executed when the signals input to the four ports P10–P13 are all high at the same time. When 2 or 3 is selected, the initial reset is done when a key entry including a combination of selected input ports is made.
Further, the time authorize circuit mask option is selected when this reset function is selected. The time authorize circuit checks the input time of the simultaneous high input and performs initial reset if that time is the defined time (1 to 2 sec) or more.
If using this function, make sure that the specified ports do not go high at the same time during ordinary operation.

2.2.3 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.3.1.
The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.
In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.
When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.
Refer to the "S1C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.3.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	–	∗

∗ See Section 4.1, "Memory Map".

2.2.4 Terminal settings at initial resetting

The I/O port (P) terminals are shared with special output terminals and input/output terminals of the serial interface, R/f converter, stopwatch timer and programmable timer (event counter). These functions are selected by the software. At initial reset, these terminals are configured to the general purpose I/O port terminals. Set them according to the system in the initial routine.
Table 2.2.4.1 shows the list of the shared terminal settings.

Table 2.2.4.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	When special outputs/peripheral functions are used (selected by software)							
		Special output			Serial I/F		R/f converter	Stopwatch direct input	Event counter
		TOUT	FOUT	BZ	Master	Slave			
P00	P00 (Input & pulled down*)						RFIN0		
P01	P01 (Input & pulled down*)						REF0		
P02	P02 (Input & pulled down*)						SEN0		
P03	P03 (Input & pulled down*)			BZ			RFOUT		
P10	P10 (Input & pulled down*)							RUN/LAP	
P11	P11 (Input & pulled down*)							RUN/LAP	
P12	P12 (Input & pulled down*)								EVIN_A
P13	P13 (Input & pulled down*)	TOUT_A							
P20	P20 (Input & pulled down*)				SCLK(O)	SCLK(I)			
P21	P21 (Input & pulled down*)				SOUT(O)	SOUT(O)			
P22	P22 (Input & pulled down*)				SIN(I)	SIN(I)			
P23	P23 (Input & pulled down*)		FOUT			SRDY(O)/$\overline{SS}$(I)			
P30	P30 (Input & pulled down*)								
P31	P31 (Input & pulled down*)	TOUT_B							
P32	P32 (Input & pulled down*)	TOUT_C							
P33	P33 (Input & pulled down*)	TOUT_D							
P40	P40 (Input & pulled down*)								
P41	P41 (Input & pulled down*)								EVIN_B
P42	P42 (Input & pulled down*)								EVIN_C
P43	P43 (Input & pulled down*)								EVIN_D
P50–P53	P50–P53 (Input & pulled down*)								

* When "With Pull-Down" is selected by mask option (high impedance when "Gate Direct" is selected)

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal (TEST)

This is the terminal used for the factory inspection of the IC. During normal operation, connect the TEST terminal to VSS.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C63632 has a 4-bit core CPU S1C63000 built-in as its CPU part.
Refer to the "S1C63000 Core CPU Manual" for the S1C63000.

3.2 Code ROM

The built-in code ROM is a mask ROM for loading programs, and has a capacity of 31,744 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the S1C63632 is step 0000H to step 7BFFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0101H–010FH, respectively.

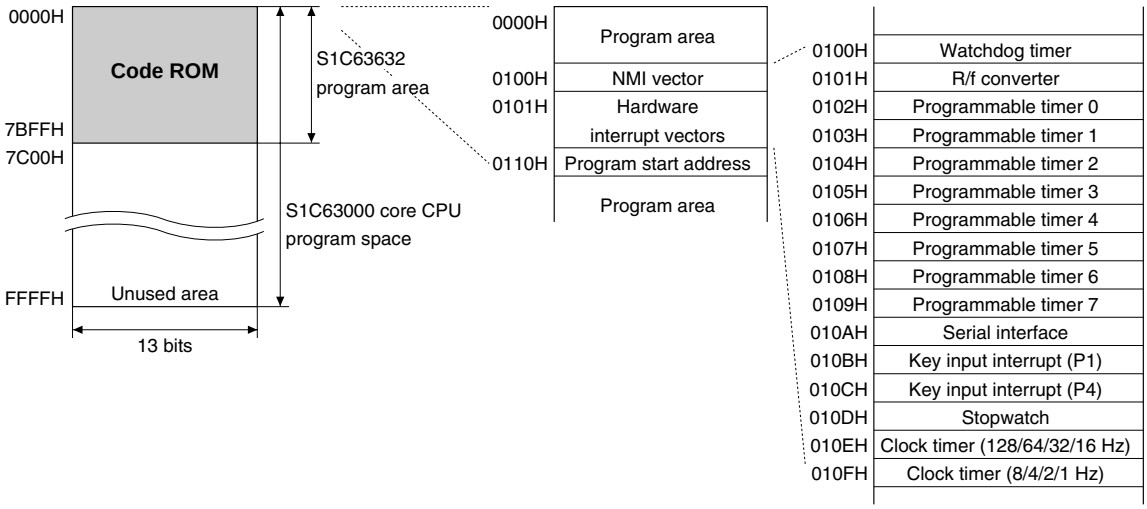


Fig. 3.2.1 Configuration of code ROM

3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 8,192 words × 4 bits. The RAM area is assigned to addresses 0000H to 1FFFH on the data memory map. Addresses 0100H to 01FFH are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data. When programming, keep the following points in mind.

(1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(2) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 1FFFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63632 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

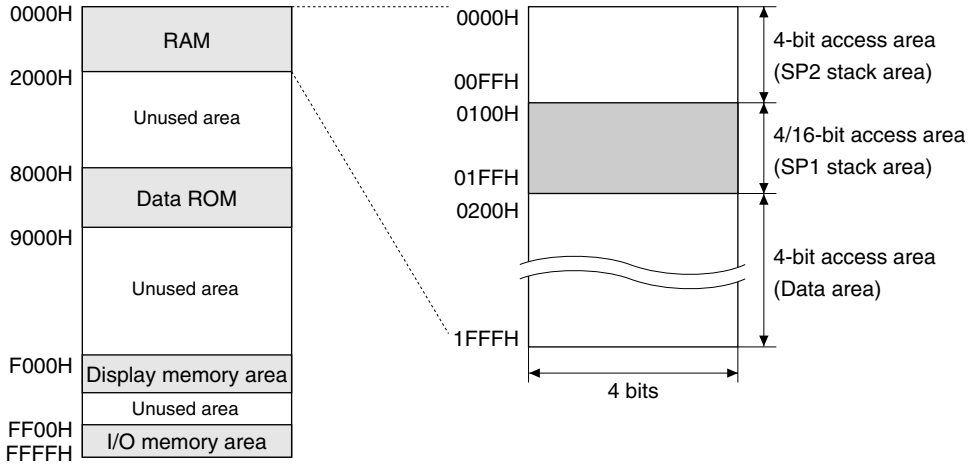


Fig. 3.3.1 Configuration of data RAM

3.4 Data ROM

The data ROM is a mask ROM for loading various static data such as a character generator, and has a capacity of 4,096 words × 4 bits. The data ROM is assigned to addresses 8000H to 8FFFH on the data memory map, and the data can be read using the same data memory access instructions as the RAM.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of S1C63632 (timer, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions. The following sections explain the detailed operation of each peripheral circuit.

4.1 Memory Map

The S1C63632 data memory consists of 8,192-word RAM, 4,096-word mask ROM, 2,048-bit display memory and 178-word peripheral I/O memory. Figure 4.1.1 shows the overall memory map of the S1C63632, and Table 4.1.1 the peripheral circuits' (I/O space) memory maps.

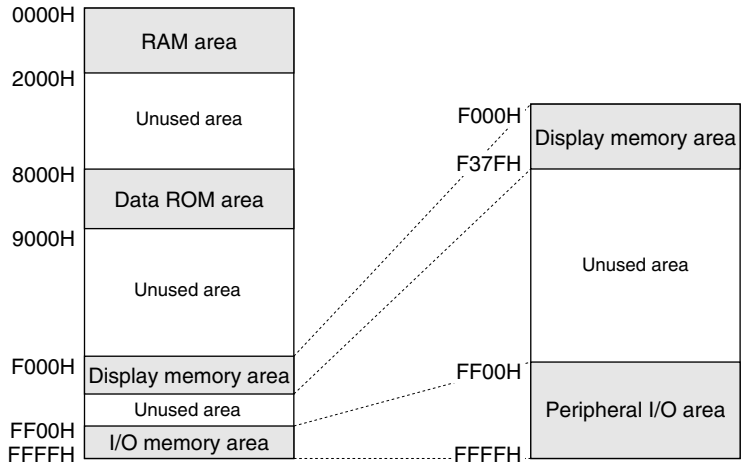


Fig. 4.1.1 Memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Table 4.1.1 for the peripheral I/O area.

Table 4.1.1 (a) I/O memory map (FF00H–FF16H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF00H	CLKCHG	OSCC	0	0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused
FF01H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)
FF02H	VDSEL	VCSEL	HLON	DBON	VDSEL	0	1	0	General-purpose register
					VCSEL	0	V_{D2}	V_{DD}	Power source select for LCD system voltage regulator
	R/W				HLON	0	On	Off	Power voltage booster/halver halving mode On/Off
					DBON	0	On	Off	Power voltage booster/halver boost mode On/Off
FF03H	VCHLMOD	VDHLMOD	General	LPWR	VCHLMOD	0	On	Off	Heavy load protection mode On/Off for LCD system voltage regulator
					VDHLMOD	0	On	Off	Heavy load protection mode On/Off for internal voltage regulator
	R/W				General	0	1	0	General-purpose register
					LPWR	0	On	Off	LCD system voltage regulator On/Off
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting
					SVDS2	0			[SVDS3–0] 0 1 2 3 4 5 6 7
	R/W				SVDS1	0			Voltage (V) 1.6 1.8 1.9 2.0 2.1 2.2 2.3 2.4
					SVDS0	0			[SVDS3–0] 8 9 10 11 12 13 14 15
									Voltage (V) 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF10H	FOUT3	FOUT2	FOUT1	FOUT0	FOUT3	0			FOUT frequency selection
					FOUT2	0			[FOUT3–0] 0 1 2 3 4 5
	R/W				FOUT1	0			Frequency Off f_{OSC1}/256 f_{OSC1}/64 f_{OSC1}/32 f_{OSC1}/16 f_{OSC1}/4
					FOUT0	0			[FOUT3–0] 6 7 8 9 10
									Frequency f_{OSC1}/2 f_{OSC1} f_{OSC3}/256 f_{OSC3}/64 f_{OSC3}/32
									[FOUT3–0] 11 12 13 14 15
									Frequency f_{OSC3}/16 f_{OSC3}/8 f_{OSC3}/4 f_{OSC3}/2 f_{OSC3}
FF11H	NRSP11	NRSP10	NRSP01	NRSP00	NRSP11	0			Key input interrupt noise reject frequency selection
					NRSP10	0			[NRSP11, 10] (P40–P43) 0 1 2 3
	R/W				NRSP01	0			Frequency Off f_{OSC1}/16 f_{OSC1}/64 f_{OSC1}/256
					NRSP00	0			[NRSP01, 00] (P10–P13) 0 1 2 3
									Frequency Off f_{OSC1}/16 f_{OSC1}/64 f_{OSC1}/256
FF12H	FLCKS1	FLCKS0	VCCKS1	VCCKS0	FLCKS1	0			Frame frequency selection [FLCKS1, 0] 0 1 2 3
					FLCKS0	0			Frequency 32 Hz 24 Hz 16 Hz 8 Hz
	R/W				VCCKS1	0			VC boost frequency selection [VCCKS1, 0] 0 1 2, 3
					VCCKS0	0			Frequency Off 2 kHz Prohibited
FF14H	0	SIFCKS2	SIFCKS1	SIFCKS0	0 *3	– *2			Unused
					SIFCKS2	0			Serial I/F clock frequency selection [SIFCKS2–0] 0 1 2 3
	R	R/W			SIFCKS1	0			Frequency Off/External f_{OSC1} f_{OSC1}/2 f_{OSC1}/4
					SIFCKS0	0			[SIFCKS2–0] 4 5 6 7
									Frequency PT1 f_{OSC3} f_{OSC3}/2 f_{OSC3}/4
FF15H	0	RFCKS2	RFCKS1	RFCKS0	0 *3	– *2			Unused
					RFCKS2	0			R/f converter clock frequency selection [RFCKS2–0] 0 1 2 3
	R	R/W			RFCKS1	0			Frequency Off f_{OSC1} f_{OSC1}/2 f_{OSC1}/4
					RFCKS0	0			[RFCKS2–0] 4 5 6 7
									Frequency PT1 f_{OSC3} f_{OSC3}/2 f_{OSC3}/4
FF16H	MDCKE	SGCKE	SWCKE	RTCKE	MDCKE	0	Enable	Disable	Integer multiplier clock enable
					SGCKE	0	Enable	Disable	Sound generator clock enable
	R/W				SWCKE	0	Enable	Disable	Stopwatch timer clock enable
					RTCKE	0	Enable	Disable	Clock timer clock enable

Remarks

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF18H–FF20H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF18H	PTPS03	PTPS02	PTPS01	PTPS00	PTPS03	0			Programmable timer 0 count clock frequency selection [PTPS03–00] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS03–00] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS03–00] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS02	0			
	R/W				PTPS01	0			
					PTPS00	0			
FF19H	PTPS13	PTPS12	PTPS11	PTPS10	PTPS13	0			Programmable timer 1 count clock frequency selection [PTPS13–10] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS13–10] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS13–10] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS12	0			
	R/W				PTPS11	0			
					PTPS10	0			
FF1AH	PTPS23	PTPS22	PTPS21	PTPS20	PTPS23	0			Programmable timer 2 count clock frequency selection [PTPS23–20] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS23–20] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS23–20] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS22	0			
	R/W				PTPS21	0			
					PTPS20	0			
FF1BH	PTPS33	PTPS32	PTPS31	PTPS30	PTPS33	0			Programmable timer 3 count clock frequency selection [PTPS33–30] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS33–30] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS33–30] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS32	0			
	R/W				PTPS31	0			
					PTPS30	0			
FF1CH	PTPS43	PTPS42	PTPS41	PTPS40	PTPS43	0			Programmable timer 4 count clock frequency selection [PTPS43–40] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS43–40] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS43–40] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS42	0			
	R/W				PTPS41	0			
					PTPS40	0			
FF1DH	PTPS53	PTPS52	PTPS51	PTPS50	PTPS53	0			Programmable timer 5 count clock frequency selection [PTPS53–50] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS53–50] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS53–50] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS52	0			
	R/W				PTPS51	0			
					PTPS50	0			
FF1EH	PTPS63	PTPS62	PTPS61	PTPS60	PTPS63	0			Programmable timer 6 count clock frequency selection [PTPS63–60] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS63–60] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS63–60] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS62	0			
	R/W				PTPS61	0			
					PTPS60	0			
FF1FH	PTPS73	PTPS72	PTPS71	PTPS70	PTPS73	0			Programmable timer 7 count clock frequency selection [PTPS73–70] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS73–70] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS73–70] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS72	0			
	R/W				PTPS71	0			
					PTPS70	0			
FF20H	P03 (RFOUT/ BZ)	P02 (SEN0)	P01 (REF0)	P00 (RFIN0)	P03	1	High	Low	P03 I/O port data functions as a general-purpose register when R/f or BZ is used
					P02	1	High	Low	P02 I/O port data functions as a general-purpose register when R/f is used
	R/W				P01	1	High	Low	P01 I/O port data functions as a general-purpose register when R/f is used
					P00	1	High	Low	P00 I/O port data functions as a general-purpose register when R/f is used

Table 4.1.1 (c) I/O memory map (FF21H–FF28H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF21H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P03 I/O control register functions as a general-purpose register when R/f or BZ is used
					IOC02	0	Output	Input	P02 I/O control register functions as a general-purpose register when R/f is used
	R/W				IOC01	0	Output	Input	P01 I/O control register functions as a general-purpose register when R/f is used
					IOC00	0	Output	Input	P00 I/O control register functions as a general-purpose register when R/f is used
FF22H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P03 pull-down control register functions as a general-purpose register when R/f or BZ is used
					PUL02	1	On	Off	P02 pull-down control register functions as a general-purpose register when R/f is used
	R/W				PUL01	1	On	Off	P01 pull-down control register functions as a general-purpose register when R/f is used
					PUL00	1	On	Off	P00 pull-down control register functions as a general-purpose register when R/f is used
FF23H	SMT03	SMT02	SMT01	SMT00	SMT03	1	Schmitt	CMOS	P03 input interface level select register functions as a general-purpose register when R/f or BZ is used
					SMT02	1	Schmitt	CMOS	P02 input interface level select register functions as a general-purpose register when R/f is used
	R/W				SMT01	1	Schmitt	CMOS	P01 input interface level select register functions as a general-purpose register when R/f is used
					SMT00	1	Schmitt	CMOS	P00 input interface level select register functions as a general-purpose register when R/f is used
FF24H	P13 (TOUT_A)	P12	P11	P10	P13	1	High	Low	P13 I/O port data functions as a general-purpose register when TOUT_A is used
	R/W				P12	1	High	Low	P12 I/O port data
					P11	1	High	Low	P11 I/O port data
					P10	1	High	Low	P10 I/O port data
FF25H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when TOUT_A is used
	R/W				IOC12	0	Output	Input	P12 I/O control register
					IOC11	0	Output	Input	P11 I/O control register
					IOC10	0	Output	Input	P10 I/O control register
FF26H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when TOUT_A is used
	R/W				PUL12	1	On	Off	P12 pull-down control register
					PUL11	1	On	Off	P11 pull-down control register
					PUL10	1	On	Off	P10 pull-down control register
FF27H	SMT13	SMT12	SMT11	SMT10	SMT13	1	Schmitt	CMOS	P13 input interface level select register functions as a general-purpose register when TOUT_A is used
	R/W				SMT12	1	Schmitt	CMOS	P12 input interface level select register
					SMT11	1	Schmitt	CMOS	P11 input interface level select register
					SMT10	1	Schmitt	CMOS	P10 input interface level select register
FF28H	P23 ($\overline{SS}$/ SRDY/ FOUT)	P22 (SIN)	P21 (SOUT)	P20 (SCLK)	P23	1	High	Low	P23 I/O port data functions as a general-purpose register when SIF (slave, SRDY) or FOUT is used
	R/W				P22	1	High	Low	P22 I/O port data
					P21	1	High	Low	P21 I/O port data functions as a general-purpose register when SIF is used
					P20	1	High	Low	P20 I/O port data functions as a general-purpose register when SIF (master) is used

Table 4.1.1 (d) I/O memory map (FF29H–FF2FH)

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF29H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register functions as a general-purpose register when SIF or FOUT is used
					IOC22	0	Output	Input	P22 I/O control register functions as a general-purpose register when SIF is used
	R/W				IOC21	0	Output	Input	P21 I/O control register functions as a general-purpose register when SIF is used
					IOC20	0	Output	Input	P20 I/O control register functions as a general-purpose register when SIF is used
FF2AH	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-down control register $\overline{SS}$ pull-down control register when SIF (slave, $\overline{SS}$) is used functions as a general-purpose register when SIF (slave, SRDY) or FOUT is used
					PUL22	1	On	Off	P22 pull-down control register SIN pull-down control register when SIF is used
	R/W				PUL21	1	On	Off	P21 pull-down control register functions as a general-purpose register when SIF (SOUT) is used
					PUL20	1	On	Off	P20 pull-down control register SCLK (I) pull-down control register when SIF (slave) is used functions as a general-purpose register when SIF (master) is used
FF2BH	SMT23	SMT22	SMT21	SMT20	SMT23	1	Schmitt	CMOS	P23 input interface level select register $\overline{SS}$ input I/F level select register when SIF (slave, $\overline{SS}$) is used functions as a general-purpose register when SIF (slave, SRDY) or FOUT is used
					SMT22	1	Schmitt	CMOS	P22 input interface level select register SIN input interface level select register when SIF is used
	R/W				SMT21	1	Schmitt	CMOS	P21 input interface level select register functions as a general-purpose register when SIF (SOUT) is used
					SMT20	1	Schmitt	CMOS	P20 input interface level select register SCLK (I) input I/F level select register when SIF (slave) is used functions as a general-purpose register when SIF (master) is used
FF2CH	P33 (TOUT_D)	P32 (TOUT_C)	P31 (TOUT_B)	P30	P33	1	High	Low	P33 I/O port data functions as a general-purpose register TOUT_D is used
					P32	1	High	Low	P32 I/O port data functions as a general-purpose register TOUT_C is used
	R/W				P31	1	High	Low	P31 I/O port data functions as a general-purpose register TOUT_B is used
					P30	1	High	Low	P30 I/O port data
FF2DH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P33 I/O control register functions as a general-purpose register TOUT_D is used
					IOC32	0	Output	Input	P32 I/O control register functions as a general-purpose register TOUT_C is used
	R/W				IOC31	0	Output	Input	P31 I/O control register functions as a general-purpose register TOUT_B is used
					IOC30	0	Output	Input	P30 I/O control register
FF2EH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P33 pull-down control register functions as a general-purpose register TOUT_D is used
					PUL32	1	On	Off	P32 pull-down control register functions as a general-purpose register TOUT_C is used
	R/W				PUL31	1	On	Off	P31 pull-down control register functions as a general-purpose register TOUT_B is used
					PUL30	1	On	Off	P30 pull-down control register
FF2FH	SMT33	SMT32	SMT31	SMT30	SMT33	1	Schmitt	CMOS	P33 input interface level select register functions as a general-purpose register TOUT_D is used
					SMT32	1	Schmitt	CMOS	P32 input interface level select register functions as a general-purpose register TOUT_C is used
	R/W				SMT31	1	Schmitt	CMOS	P31 input interface level select register functions as a general-purpose register TOUT_B is used
					SMT30	1	Schmitt	CMOS	P30 input interface level select register

Table 4.1.1 (e) I/O memory map (FF30H–FF41H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF30H	P43	P42	P41	P40	P43	1	High	Low	P40–P43 I/O port data
					P42	1	High	Low	
	R/W				P41	1	High	Low	
					P40	1	High	Low	
FF31H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P40–P43 I/O control register
					IOC42	0	Output	Input	
	R/W				IOC41	0	Output	Input	
					IOC40	0	Output	Input	
FF32H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P40–P43 pull-down control register
					PUL42	1	On	Off	
	R/W				PUL41	1	On	Off	
					PUL40	1	On	Off	
FF33H	SMT43	SMT42	SMT41	SMT40	SMT43	1	Schmitt	CMOS	P40–P43 input interface level select register
					SMT42	1	Schmitt	CMOS	
	R/W				SMT41	1	Schmitt	CMOS	
					SMT40	1	Schmitt	CMOS	
FF34H	P53	P52	P51	P50	P53	1	High	Low	P50–P53 I/O port data
					P52	1	High	Low	
	R/W				P51	1	High	Low	
					P50	1	High	Low	
FF35H	IOC53	IOC52	IOC51	IOC50	IOC53	0	Output	Input	P50–P53 I/O control register
					IOC52	0	Output	Input	
	R/W				IOC51	0	Output	Input	
					IOC50	0	Output	Input	
FF36H	PUL53	PUL52	PUL51	PUL50	PUL53	1	On	Off	P50–P53 pull-down control register
					PUL52	1	On	Off	
	R/W				PUL51	1	On	Off	
					PUL50	1	On	Off	
FF37H	SMT53	SMT52	SMT51	SMT50	SMT53	1	Schmitt	CMOS	P50–P53 input interface level select register
					SMT52	1	Schmitt	CMOS	
	R/W				SMT51	1	Schmitt	CMOS	
					SMT50	1	Schmitt	CMOS	
FF3CH	SIP03	SIP02	SIP01	SIP00	SIP03	0	Enable	Disable	P10–P13 interrupt select register
					SIP02	0	Enable	Disable	
	R/W				SIP01	0	Enable	Disable	
					SIP00	0	Enable	Disable	
FF3DH	PCP03	PCP02	PCP01	PCP00	PCP03	1			P10–P13 interrupt polarity select register
					PCP02	1			
	R/W				PCP01	1			
					PCP00	1			
FF3EH	SIP13	SIP12	SIP11	SIP10	SIP13	0	Enable	Disable	P40–P43 interrupt select register
					SIP12	0	Enable	Disable	
	R/W				SIP11	0	Enable	Disable	
					SIP10	0	Enable	Disable	
FF3FH	PCP13	PCP12	PCP11	PCP10	PCP13	1			P40–P43 interrupt polarity select register
					PCP12	1			
	R/W				PCP11	1			
					PCP10	1			
FF40H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF41H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)

Table 4.1.1 (f) I/O memory map (FF42H–FF51H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF42H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
					TM5	0			Clock timer data (4 Hz)
	R				TM4	0			Clock timer data (8 Hz)
FF44H	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
FF45H	0	BZSTP	BZSHT	SHTPW	0 *3	– *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FF46H	0	BZFQ2	BZFQ1	BZFQ0	0 *3	– *2			Unused
					BZFQ2	0			Buzzer frequency selection [BZFQ2–0] 0 1 2 3 / Frequency (Hz) 4096.0 3276.8 2730.7 2340.6 / [BZFQ2–0] 4 5 6 7 / Frequency (Hz) 2048.0 1638.4 1365.3 1170.3
					BZFQ1	0			
	R	R/W			BZFQ0	0			
FF47H	0	BDTY2	BDTY1	BDTY0	0 *3	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
					BDTY1	0			
	R	R/W			BDTY0	0			
FF48H	0	0	SWDIR	EDIR	0 *3	– *2			Unused
					0 *3	– *2			Unused
					SWDIR	0			Stopwatch direct input switch 0: P10=Run/Stop, P11=Lap 1: P10=Lap, P11=Run/Stop
	R		R/W						
					EDIR	0	Enable	Disable	Direct input enable
FF49H	0	DKM2	DKM1	DKM0	0 *3	– *2			Unused
					DKM2	0			Key mask selection [DKM2–0] 0 1 2 3 / Key mask None P12 P12–13 P12–13,40 / [DKM2–0] 4 5 6 7 / Key mask P40 P40–41 P40–42 P40–43
					DKM1	0			
	R	R/W			DKM0	0			
FF4AH	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Request	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
FF4BH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/1000 sec)
					SWD2	0			
					SWD1	0			
	R				SWD0	0			
FF4CH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/100 sec)
					SWD6	0			
					SWD5	0			
	R				SWD4	0			
FF4DH	SWD11	SWD10	SWD9	SWD8	SWD11	0			Stopwatch timer data BCD (1/10 sec)
					SWD10	0			
					SWD9	0			
	R				SWD8	0			
FF50H	General	LPAGE	DSPC1	DSPC0	General	0	1	0	General-purpose register
					LPAGE	0	F200-F37F	F000-F17F	Display memory area (when 1/16 duty is selected) functions as a general-purpose register when 1/24 or 1/32 is selected
	R/W				DSPC1	0			LCD display mode selection [DSPC1, 0] 0 1 2 3 / Display mode Normal Reverse All lit All off
					DSPC0	0			
FF51H	General	LDUTY2	LDUTY1	LDUTY0	General	0	1	0	General-purpose register
					LDUTY2	0			LCD drive duty selection [LDUTY2–0] 0 1 2 / Duty 1/32 (32 Hz) Prohibited 1/24 (42 Hz) / [LDUTY2–0] 3 4 5–7 / Duty 1/24 (21 Hz) 1/16 (32 Hz) Prohibited
					LDUTY1	0			
	R/W				LDUTY0	0			

Table 4.1.1 (g) I/O memory map (FF52H–FF67H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF52H	LC3	LC2	LC1	LC0	LC3	0			LCD contrast adjustment [LC3–0] 0 – 15; Contrast Light – Dark
	R/W				LC2	0			
					LC1	0			
					LC0	0			
FF58H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R	R/W					Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P2 port function selection)
FF59H	SCPS1	SCPS0	SDP	SMOD	SCPS1	0			Serial I/F clock format selection [SCPS1, 0] 0: P, 1: P, 2: N, 3: N (Polarity phase)
					SCPS0	0	↓	↑	
	R/W				SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
					SMOD	0	Master	Slave	Serial I/F mode selection
FF5AH	0	0	ESREADY	ENCS	0 *3	– *2			Unused
					0 *3	– *2			Unused
					ESREADY	0	SRDY	$\overline{SS}$	P23 port function selection: ESREADY=x, ENCS=0 → P23 I/O (Slave & Master); ESREADY=0, ENCS=1 → P23 $\overline{SS}$ I/O (Slave & Master); ESREADY=1, ENCS=1 → P23 SRDY (Slave), P23 Prohibited (Master)
	R		R/W		ENCS	0	SIF	I/O	Serial I/F enable (P23 function selection)
FF5BH	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
					SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					SD1	– *2	High	Low	
	R/W				SD0	– *2	High	Low	LSB
FF5CH	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
					SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					SD5	– *2	High	Low	
	R/W				SD4	– *2	High	Low	LSB
FF60H	RFCNT	RFOUT	ERF1	ERF0	RFCNT	0	Continue	Normal	Continuous oscillation enable
					RFOUT	0	Enable	Disable	RFOUT enable
	R/W				ERF1	0			R/f conversion selection [ERF1, 0] 0: R/f conversion I/O, 1: Ch.0 DC, 2: Ch.1 AC, 3: Ch.1 DC
					ERF0	0			
FF61H	OVTC	OVMC	RFRUNR	RFRUNS	OVTC	0	Overflow	Non-ov	Time base counter overflow flag
					OVMC	0	Overflow	Non-ov	Measurement counter overflow flag
	R/W				RFRUNR	0	Run	Stop	Reference oscillation Run control/status
					RFRUNS	0	Run	Stop	Sensor oscillation Run control/status
FF62H	MC3	MC2	MC1	MC0	MC3	– *2			Measurement counter MC0–MC3
					MC2	– *2			
	R/W				MC1	– *2			
					MC0	– *2			LSB
FF63H	MC7	MC6	MC5	MC4	MC7	– *2			Measurement counter MC4–MC7
					MC6	– *2			
	R/W				MC5	– *2			
					MC4	– *2			
FF64H	MC11	MC10	MC9	MC8	MC11	– *2			Measurement counter MC8–MC11
					MC10	– *2			
	R/W				MC9	– *2			
					MC8	– *2			
FF65H	MC15	MC14	MC13	MC12	MC15	– *2			Measurement counter MC12–MC15
					MC14	– *2			
	R/W				MC13	– *2			
					MC12	– *2			
FF66H	MC19	MC18	MC17	MC16	MC19	– *2			MSB
					MC18	– *2			Measurement counter MC16–MC19
	R/W				MC17	– *2			
					MC16	– *2			
FF67H	TC3	TC2	TC1	TC0	TC3	– *2			Time base counter TC0–TC3
					TC2	– *2			
	R/W				TC1	– *2			
					TC0	– *2			

Table 4.1.1 (h) I/O memory map (FF68H–FF82H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF68H	TC7	TC6	TC5	TC4	TC7	– *2			Time base counter TC4–TC7
					TC6	– *2			
	R/W				TC5	– *2			
					TC4	– *2			
FF69H	TC11	TC10	TC9	TC8	TC11	– *2			Time base counter TC8–TC11
					TC10	– *2			
	R/W				TC9	– *2			
					TC8	– *2			
FF6AH	TC15	TC14	TC13	TC12	TC15	– *2			Time base counter TC12–TC15
					TC14	– *2			
	R/W				TC13	– *2			
					TC12	– *2			
FF6BH	TC19	TC18	TC17	TC16	TC19	– *2			MSB Time base counter TC16–TC19
					TC18	– *2			
	R/W				TC17	– *2			
					TC16	– *2			
FF70H	SR3	SR2	SR1	SR0	SR3	– *2			Source register (low-order 4 bits) LSB
					SR2	– *2			
	R/W				SR1	– *2			
					SR0	– *2			
FF71H	SR7	SR6	SR5	SR4	SR7	– *2			MSB Source register (high-order 4 bits)
					SR6	– *2			
	R/W				SR5	– *2			
					SR4	– *2			
FF72H	DRL3	DRL2	DRL1	DRL0	DRL3	– *2			Low-order 8-bit destination register (low-order 4 bits) LSB
					DRL2	– *2			
	R/W				DRL1	– *2			
					DRL0	– *2			
FF73H	DRL7	DRL6	DRL5	DRL4	DRL7	– *2			MSB Low-order 8-bit destination register (high-order 4 bits)
					DRL6	– *2			
	R/W				DRL5	– *2			
					DRL4	– *2			
FF74H	DRH3	DRH2	DRH1	DRH0	DRH3	– *2			High-order 8-bit destination register (low-order 4 bits) LSB
					DRH2	– *2			
	R/W				DRH1	– *2			
					DRH0	– *2			
FF75H	DRH7	DRH6	DRH5	DRH4	DRH7	– *2			MSB High-order 8-bit destination register (high-order 4 bits)
					DRH6	– *2			
	R/W				DRH5	– *2			
					DRH4	– *2			
FF76H	NF	VF	ZF	CALMD	NF	0	Negative	Positive	Negative flag
					VF	0	Overflow	No	Overflow flag
	R			R/W	ZF	0	Zero	No	Zero flag
					CALMD	0	Run	Stop	Operation status (reading)
							Div.	Mult.	Calculation mode selection (writing)
FF80H	MOD16_A	EVCNT_A	FCSEL_A	PLPUL_A	MOD16_A	0	16 bits	8 bits	PTM0–1 16-bit mode selection
					EVCNT_A	0	Event ct.	Timer	PTM0 counter mode selection
	R/W				FCSEL_A	0	With NR	No NR	PTM0 function selection (for event counter mode)
					PLPUL_A	0	↑	↓	PTM0 pulse polarity selection (for event counter mode)
FF81H	PTSEL1	PTSEL0	CHSEL_A	PTOUT_A	PTSEL1	0	PWM	Normal	Programmable timer 1 PWM output selection
					PTSEL0	0	PWM	Normal	Programmable timer 0 PWM output selection
	R/W				CHSEL_A	0	Timer 1	Timer 0	PTM0–1 TOUT_A output selection
					PTOUT_A	0	On	Off	PTM0–1 TOUT_A output control
FF82H	PTRST1	PTRUN1	PTRST0	PTRUN0	PTRST1*3	– *2	Reset	Invalid	Programmable timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Programmable timer 1 Run/Stop
	W	R/W	W	R/W	PTRST0*3	– *2	Reset	Invalid	Programmable timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Programmable timer 0 Run/Stop

Table 4.1.1 (i) I/O memory map (FF84H–FF91H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF84H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FF85H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FF86H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FF87H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FF88H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FF89H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FF8AH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FF8BH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FF8CH	CD03	CD02	CD01	CD00	CD03	0			MSB
					CD02	0			Programmable timer 0 compare data (low-order 4 bits)
	R/W				CD01	0			
					CD00	0			LSB
FF8DH	CD07	CD06	CD05	CD04	CD07	0			MSB
					CD06	0			Programmable timer 0 compare data (high-order 4 bits)
	R/W				CD05	0			
					CD04	0			LSB
FF8EH	CD13	CD12	CD11	CD10	CD13	0			MSB
					CD12	0			Programmable timer 1 compare data (low-order 4 bits)
	R/W				CD11	0			
					CD10	0			LSB
FF8FH	CD17	CD16	CD15	CD14	CD17	0			MSB
					CD16	0			Programmable timer 1 compare data (high-order 4 bits)
	R/W				CD15	0			
					CD14	0			LSB
FF90H	MOD16_B	EVCNT_B	FCSEL_B	PLPUL_B	MOD16_B	0	16 bits	8 bits	PTM2–3 16-bit mode selection
					EVCNT_B	0	Event ct.	Timer	PTM2 counter mode selection
	R/W				FCSEL_B	0	With NR	No NR	PTM2 function selection (for event counter mode)
					PLPUL_B	0	↑	↓	PTM2 pulse polarity selection (for event counter mode)
FF91H	PTSEL3	PTSEL2	CHSEL_B	PTOUT_B	PTSEL3	0	PWM	Normal	Programmable timer 3 PWM output selection
					PTSEL2	0	PWM	Normal	Programmable timer 2 PWM output selection
	R/W				CHSEL_B	0	Timer 3	Timer 2	PTM2–3 TOUT_B output selection
					PTOUT_B	0	On	Off	PTM2–3 TOUT_B output control

Table 4.1.1 (j) I/O memory map (FF92H–FFA0H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF92H	PTRST3	PTRUN3	PTRST2	PTRUN2	PTRST3*3	– *2	Reset	Invalid	Programmable timer 3 reset (reload)
					PTRUN3	0	Run	Stop	Programmable timer 3 Run/Stop
	W	R/W	W	R/W	PTRST2*3	– *2	Reset	Invalid	Programmable timer 2 reset (reload)
					PTRUN2	0	Run	Stop	Programmable timer 2 Run/Stop
FF94H	RLD23	RLD22	RLD21	RLD20	RLD23	0			MSB
					RLD22	0			Programmable timer 2 reload data (low-order 4 bits)
	R/W				RLD21	0			
					RLD20	0			LSB
FF95H	RLD27	RLD26	RLD25	RLD24	RLD27	0			MSB
					RLD26	0			Programmable timer 2 reload data (high-order 4 bits)
	R/W				RLD25	0			
					RLD24	0			LSB
FF96H	RLD33	RLD32	RLD31	RLD30	RLD33	0			MSB
					RLD32	0			Programmable timer 3 reload data (low-order 4 bits)
	R/W				RLD31	0			
					RLD30	0			LSB
FF97H	RLD37	RLD36	RLD35	RLD34	RLD37	0			MSB
					RLD36	0			Programmable timer 3 reload data (high-order 4 bits)
	R/W				RLD35	0			
					RLD34	0			LSB
FF98H	PTD23	PTD22	PTD21	PTD20	PTD23	0			MSB
					PTD22	0			Programmable timer 2 data (low-order 4 bits)
	R				PTD21	0			
					PTD20	0			LSB
FF99H	PTD27	PTD26	PTD25	PTD24	PTD27	0			MSB
					PTD26	0			Programmable timer 2 data (high-order 4 bits)
	R				PTD25	0			
					PTD24	0			LSB
FF9AH	PTD33	PTD32	PTD31	PTD30	PTD33	0			MSB
					PTD32	0			Programmable timer 3 data (low-order 4 bits)
	R				PTD31	0			
					PTD30	0			LSB
FF9BH	PTD37	PTD36	PTD35	PTD34	PTD37	0			MSB
					PTD36	0			Programmable timer 3 data (high-order 4 bits)
	R				PTD35	0			
					PTD34	0			LSB
FF9CH	CD23	CD22	CD21	CD20	CD23	0			MSB
					CD22	0			Programmable timer 2 compare data (low-order 4 bits)
	R/W				CD21	0			
					CD20	0			LSB
FF9DH	CD27	CD26	CD25	CD24	CD27	0			MSB
					CD26	0			Programmable timer 2 compare data (high-order 4 bits)
	R/W				CD25	0			
					CD24	0			LSB
FF9EH	CD33	CD32	CD31	CD30	CD33	0			MSB
					CD32	0			Programmable timer 3 compare data (low-order 4 bits)
	R/W				CD31	0			
					CD30	0			LSB
FF9FH	CD37	CD36	CD35	CD34	CD37	0			MSB
					CD36	0			Programmable timer 3 compare data (high-order 4 bits)
	R/W				CD35	0			
					CD34	0			LSB
FFA0H	MOD16_C	EVCNT_C	FCSEL_C	PLPUL_C	MOD16_C	0	16 bits	8 bits	PTM4–5 16-bit mode selection
					EVCNT_C	0	Event ct.	Timer	PTM4 counter mode selection
	R/W				FCSEL_C	0	With NR	No NR	PTM4 function selection (for event counter mode)
					PLPUL_C	0	↑	↓	PTM4 pulse polarity selection (for event counter mode)

Table 4.1.1 (k) I/O memory map (FFA1H–FFAFH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFA1H	PTSEL5	PTSEL4	CHSEL_C	PTOUT_C	PTSEL5	0	PWM	Normal	Programmable timer 5 PWM output selection
					PTSEL4	0	PWM	Normal	Programmable timer 4 PWM output selection
	R/W				CHSEL_C	0	Timer 5	Timer 4	PTM4–5 TOUT_C output selection
					PTOUT_C	0	On	Off	PTM4–5 TOUT_C output control
FFA2H	PTRST5	PTRUN5	PTRST4	PTRUN4	PTRST5*3	– *2	Reset	Invalid	Programmable timer 5 reset (reload)
					PTRUN5	0	Run	Stop	Programmable timer 5 Run/Stop
	W	R/W	W	R/W	PTRST4*3	– *2	Reset	Invalid	Programmable timer 4 reset (reload)
					PTRUN4	0	Run	Stop	Programmable timer 4 Run/Stop
FFA4H	RLD43	RLD42	RLD41	RLD40	RLD43	0			MSB
					RLD42	0			Programmable timer 4 reload data (low-order 4 bits)
	R/W				RLD41	0			
					RLD40	0			LSB
FFA5H	RLD47	RLD46	RLD45	RLD44	RLD47	0			MSB
					RLD46	0			Programmable timer 4 reload data (high-order 4 bits)
	R/W				RLD45	0			
					RLD44	0			LSB
FFA6H	RLD53	RLD52	RLD51	RLD50	RLD53	0			MSB
					RLD52	0			Programmable timer 5 reload data (low-order 4 bits)
	R/W				RLD51	0			
					RLD50	0			LSB
FFA7H	RLD57	RLD56	RLD55	RLD54	RLD57	0			MSB
					RLD56	0			Programmable timer 5 reload data (high-order 4 bits)
	R/W				RLD55	0			
					RLD54	0			LSB
FFA8H	PTD43	PTD42	PTD41	PTD40	PTD43	0			MSB
					PTD42	0			Programmable timer 4 data (low-order 4 bits)
	R				PTD41	0			
					PTD40	0			LSB
FFA9H	PTD47	PTD46	PTD45	PTD44	PTD47	0			MSB
					PTD46	0			Programmable timer 4 data (high-order 4 bits)
	R				PTD45	0			
					PTD44	0			LSB
FFAAH	PTD53	PTD52	PTD51	PTD50	PTD53	0			MSB
					PTD52	0			Programmable timer 5 data (low-order 4 bits)
	R				PTD51	0			
					PTD50	0			LSB
FFABH	PTD57	PTD56	PTD55	PTD54	PTD57	0			MSB
					PTD56	0			Programmable timer 5 data (high-order 4 bits)
	R				PTD55	0			
					PTD54	0			LSB
FFACH	CD43	CD42	CD41	CD40	CD43	0			MSB
					CD42	0			Programmable timer 4 compare data (low-order 4 bits)
	R/W				CD41	0			
					CD40	0			LSB
FFADH	CD47	CD46	CD45	CD44	CD47	0			MSB
					CD46	0			Programmable timer 4 compare data (high-order 4 bits)
	R/W				CD45	0			
					CD44	0			LSB
FFAEH	CD53	CD52	CD51	CD50	CD53	0			MSB
					CD52	0			Programmable timer 5 compare data (low-order 4 bits)
	R/W				CD51	0			
					CD50	0			LSB
FFAFH	CD57	CD56	CD55	CD54	CD57	0			MSB
					CD56	0			Programmable timer 5 compare data (high-order 4 bits)
	R/W				CD55	0			
					CD54	0			LSB

Table 4.1.1 (l) I/O memory map (FFB0H–FFBEH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFB0H	MOD16_D	EVCNT_D	FCSEL_D	PLPUL_D	MOD16_D	0	16 bits	8 bits	PTM6–7 16-bit mode selection
					EVCNT_D	0	Event ct.	Timer	PTM6 counter mode selection
					FCSEL_D	0	With NR	No NR	PTM6 function selection (for event counter mode)
	R/W				PLPUL_D	0	↑	↓	PTM6 pulse polarity selection (for event counter mode)
FFB1H	PTSEL7	PTSEL6	CHSEL_D	PTOUT_D	PTSEL7	0	PWM	Normal	Programmable timer 7 PWM output selection
					PTSEL6	0	PWM	Normal	Programmable timer 6 PWM output selection
					CHSEL_D	0	Timer 7	Timer 6	PTM6–7 TOUT_D output selection
	R/W				PTOUT_D	0	On	Off	PTM6–7 TOUT_D output control
FFB2H	PTRST7	PTRUN7	PTRST6	PTRUN6	PTRST7*3	– *2	Reset	Invalid	Programmable timer 7 reset (reload)
					PTRUN7	0	Run	Stop	Programmable timer 7 Run/Stop
	W	R/W	W	R/W	PTRST6*3	– *2	Reset	Invalid	Programmable timer 6 reset (reload)
					PTRUN6	0	Run	Stop	Programmable timer 6 Run/Stop
FFB4H	RLD63	RLD62	RLD61	RLD60	RLD63	0			MSB
					RLD62	0			Programmable timer 6 reload data (low-order 4 bits)
	R/W				RLD61	0			
					RLD60	0			LSB
FFB5H	RLD67	RLD66	RLD65	RLD64	RLD67	0			MSB
					RLD66	0			Programmable timer 6 reload data (high-order 4 bits)
	R/W				RLD65	0			
					RLD64	0			LSB
FFB6H	RLD73	RLD72	RLD71	RLD70	RLD73	0			MSB
					RLD72	0			Programmable timer 7 reload data (low-order 4 bits)
	R/W				RLD71	0			
					RLD70	0			LSB
FFB7H	RLD77	RLD76	RLD75	RLD74	RLD77	0			MSB
					RLD76	0			Programmable timer 7 reload data (high-order 4 bits)
	R/W				RLD75	0			
					RLD74	0			LSB
FFB8H	PTD63	PTD62	PTD61	PTD60	PTD63	0			MSB
					PTD62	0			Programmable timer 6 data (low-order 4 bits)
	R				PTD61	0			
					PTD60	0			LSB
FFB9H	PTD67	PTD66	PTD65	PTD64	PTD67	0			MSB
					PTD66	0			Programmable timer 6 data (high-order 4 bits)
	R				PTD65	0			
					PTD64	0			LSB
FFBAH	PTD73	PTD72	PTD71	PTD70	PTD73	0			MSB
					PTD72	0			Programmable timer 7 data (low-order 4 bits)
	R				PTD71	0			
					PTD70	0			LSB
FFBBH	PTD77	PTD76	PTD75	PTD74	PTD77	0			MSB
					PTD76	0			Programmable timer 7 data (high-order 4 bits)
	R				PTD75	0			
					PTD74	0			LSB
FFBCH	CD63	CD62	CD61	CD60	CD63	0			MSB
					CD62	0			Programmable timer 6 compare data (low-order 4 bits)
	R/W				CD61	0			
					CD60	0			LSB
FFBDH	CD67	CD66	CD65	CD64	CD67	0			MSB
					CD66	0			Programmable timer 6 compare data (high-order 4 bits)
	R/W				CD65	0			
					CD64	0			LSB
FFBEH	CD73	CD72	CD71	CD70	CD73	0			MSB
					CD72	0			Programmable timer 7 compare data (low-order 4 bits)
	R/W				CD71	0			
					CD70	0			LSB

Table 4.1.1 (m) I/O memory map (FFBFH–FFEDH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFBFH	CD77	CD76	CD75	CD74	CD77	0			MSB
					CD76	0			Programmable timer 7 compare data (high-order 4 bits)
					CD75	0			
	R/W				CD74	0			LSB
FFE1H	General	EIRFE	EIRFR	EIRFS	General	0	1	0	General-purpose register
					EIRFE	0	Enable	Mask	Interrupt mask register (R/f converter error)
					EIRFR	0	Enable	Mask	Interrupt mask register (R/f converter reference oscillate completion)
	R/W				EIRFS	0	Enable	Mask	Interrupt mask register (R/f converter sensor oscillate completion)
FFE2H	General	General	EIPT0	EICTC0	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 underflow)
	R/W				EICTC0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 compare match)
FFE3H	General	General	EIPT1	EICTC1	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
					EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 underflow)
	R/W				EICTC1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 compare match)
FFE4H	General	General	EIPT2	EICTC2	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
					EIPT2	0	Enable	Mask	Interrupt mask register (Programmable timer 2 underflow)
	R/W				EICTC2	0	Enable	Mask	Interrupt mask register (Programmable timer 2 compare match)
FFE5H	General	General	EIPT3	EICTC3	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
					EIPT3	0	Enable	Mask	Interrupt mask register (Programmable timer 3 underflow)
	R/W				EICTC3	0	Enable	Mask	Interrupt mask register (Programmable timer 3 compare match)
FFE6H	General	General	EIPT4	EICTC4	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
					EIPT4	0	Enable	Mask	Interrupt mask register (Programmable timer 4 underflow)
	R/W				EICTC4	0	Enable	Mask	Interrupt mask register (Programmable timer 4 compare match)
FFE7H	General	General	EIPT5	EICTC5	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
					EIPT5	0	Enable	Mask	Interrupt mask register (Programmable timer 5 underflow)
	R/W				EICTC5	0	Enable	Mask	Interrupt mask register (Programmable timer 5 compare match)
FFE8H	General	General	EIPT6	EICTC6	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
					EIPT6	0	Enable	Mask	Interrupt mask register (Programmable timer 6 underflow)
	R/W				EICTC6	0	Enable	Mask	Interrupt mask register (Programmable timer 6 compare match)
FFE9H	General	General	EIPT7	EICTC7	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
					EIPT7	0	Enable	Mask	Interrupt mask register (Programmable timer 7 underflow)
	R/W				EICTC7	0	Enable	Mask	Interrupt mask register (Programmable timer 7 compare match)
FFEAH	General	General	General	EISIF	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
FFEBH	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (Key input interrupt 3 <P13>)
					EIK02	0	Enable	Mask	Interrupt mask register (Key input interrupt 2 <P12>)
					EIK01	0	Enable	Mask	Interrupt mask register (Key input interrupt 1 <P11>)
	R/W				EIK00	0	Enable	Mask	Interrupt mask register (Key input interrupt 0 <P10>)
FFECH	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (Key input interrupt 7 <P43>)
					EIK12	0	Enable	Mask	Interrupt mask register (Key input interrupt 6 <P42>)
					EIK11	0	Enable	Mask	Interrupt mask register (Key input interrupt 5 <P41>)
	R/W				EIK10	0	Enable	Mask	Interrupt mask register (Key input interrupt 4 <P40>)
FFEDH	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
					EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
	R/W				EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)

Table 4.1.1 (n) I/O memory map (FFEEH–FFFCH)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFEEH	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 64 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 128 Hz)
FFEFH	EIT7	EIT6	EIT5	EIT4	EIT7	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT6	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT5	0	Enable	Mask	Interrupt mask register (Clock timer 4 Hz)
					EIT4	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
FFF1H	General	IRFE	IRFR	IRFS	General	0	(R)	(R)	General-purpose register
					IRFE	0	Yes	No	Interrupt factor flag (R/f converter error)
	R/W				IRFR	0	(W)	(W)	Interrupt factor flag (R/f converter reference oscillate completion)
					IRFS	0	Reset	Invalid	Interrupt factor flag (R/f converter sensor oscillate completion)
FFF2H	General	General	IPT0	ICTC0	General	0	(R)	(R)	General-purpose register
					General	0	Yes	No	General-purpose register
	R/W				IPT0	0	(W)	(W)	Interrupt factor flag (Programmable timer 0 underflow)
					ICTC0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0 compare match)
FFF3H	General	General	IPT1	ICTC1	General	0	(R)	(R)	General-purpose register
					General	0	Yes	No	General-purpose register
	R/W				IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1 underflow)
					ICTC1	0	Reset	Invalid	Interrupt factor flag (Programmable timer 1 compare match)
FFF4H	General	General	IPT2	ICTC2	General	0	(R)	(R)	General-purpose register
					General	0	Yes	No	General-purpose register
	R/W				IPT2	0	(W)	(W)	Interrupt factor flag (Programmable timer 2 underflow)
					ICTC2	0	Reset	Invalid	Interrupt factor flag (Programmable timer 2 compare match)
FFF5H	General	General	IPT3	ICTC3	General	0	(R)	(R)	General-purpose register
					General	0	Yes	No	General-purpose register
	R/W				IPT3	0	(W)	(W)	Interrupt factor flag (Programmable timer 3 underflow)
					ICTC3	0	Reset	Invalid	Interrupt factor flag (Programmable timer 3 compare match)
FFF6H	General	General	IPT4	ICTC4	General	0	(R)	(R)	General-purpose register
					General	0	Yes	No	General-purpose register
	R/W				IPT4	0	(W)	(W)	Interrupt factor flag (Programmable timer 4 underflow)
					ICTC4	0	Reset	Invalid	Interrupt factor flag (Programmable timer 4 compare match)
FFF7H	General	General	IPT5	ICTC5	General	0	(R)	(R)	General-purpose register
					General	0	Yes	No	General-purpose register
	R/W				IPT5	0	(W)	(W)	Interrupt factor flag (Programmable timer 5 underflow)
					ICTC5	0	Reset	Invalid	Interrupt factor flag (Programmable timer 5 compare match)
FFF8H	General	General	IPT6	ICTC6	General	0	(R)	(R)	General-purpose register
					General	0	Yes	No	General-purpose register
	R/W				IPT6	0	(W)	(W)	Interrupt factor flag (Programmable timer 6 underflow)
					ICTC6	0	Reset	Invalid	Interrupt factor flag (Programmable timer 6 compare match)
FFF9H	General	General	IPT7	ICTC7	General	0	(R)	(R)	General-purpose register
					General	0	Yes	No	General-purpose register
	R/W				IPT7	0	(W)	(W)	Interrupt factor flag (Programmable timer 7 underflow)
					ICTC7	0	Reset	Invalid	Interrupt factor flag (Programmable timer 7 compare match)
FFFAH	General	General	General	ISIF	General	0	(R)	(R)	General-purpose register
					General	0	Yes	No	General-purpose register
	R/W				General	0	(W)	(W)	General-purpose register
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial interface)
FFFBH	IK03	IK02	IK01	IK00	IK03	0	(R)	(R)	Interrupt factor flag (Key input interrupt 3 <P13>)
					IK02	0	Yes	No	Interrupt factor flag (Key input interrupt 2 <P12>)
	R/W				IK01	0	(W)	(W)	Interrupt factor flag (Key input interrupt 1 <P11>)
					IK00	0	Reset	Invalid	Interrupt factor flag (Key input interrupt 0 <P10>)
FFFCH	IK13	IK12	IK11	IK10	IK13	0	(R)	(R)	Interrupt factor flag (Key input interrupt 7 <P43>)
					IK12	0	Yes	No	Interrupt factor flag (Key input interrupt 6 <P42>)
	R/W				IK11	0	(W)	(W)	Interrupt factor flag (Key input interrupt 5 <P41>)
					IK10	0	Reset	Invalid	Interrupt factor flag (Key input interrupt 4 <P40>)

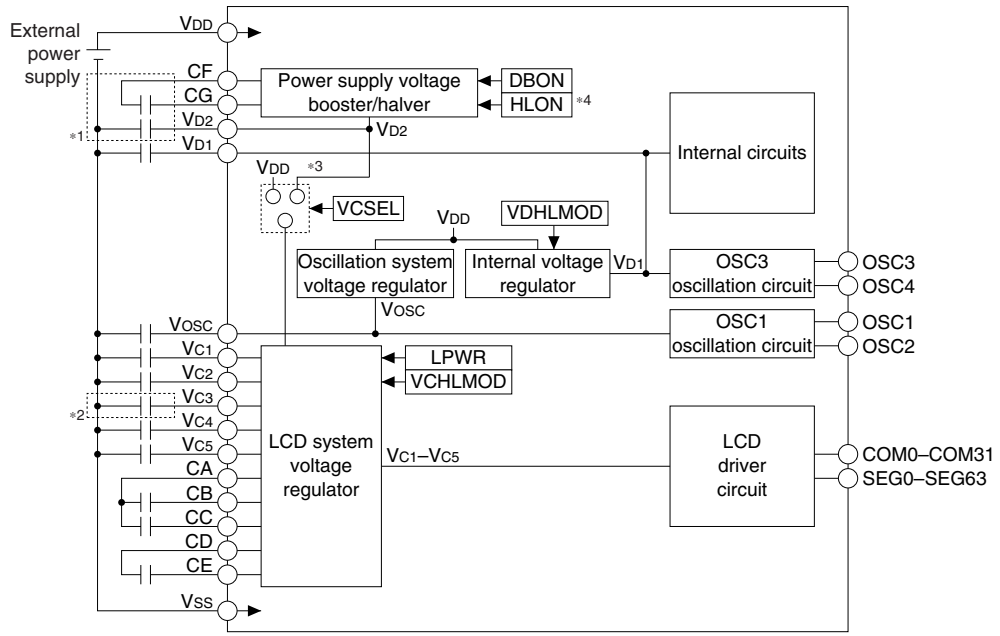
Table 4.1.1 (o) I/O memory map (FFFDH–FFFFH)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFFDH	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)
FFFEH	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 16 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 64 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 128 Hz)
FFFFH	IT7	IT6	IT5	IT4	IT7	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT6	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT5	0	(W)	(W)	Interrupt factor flag (Clock timer 4 Hz)
					IT4	0	Reset	Invalid	Interrupt factor flag (Clock timer 8 Hz)

4.2 Power Control

4.2.1 Configuration of power supply circuit

The S1C63632 has built-in power supply circuits shown in Figure 4.2.1.1 so the voltages to drive the CPU, internal logic circuits, oscillation circuits and LCD driver can be generated on the chip.



*1 Leave these terminals open when the power supply voltage booster/halver is not used.
*2 Connect when the 1/5 bias LCD drive power is used. (Leave the terminal open when the 1/4 bias LCD drive power is used.)
*3 Can be selected as the power source for the LCD system voltage regulator when the power supply voltage booster/halver operates in boost mode.
*4 HLON is prohibited from use.

Fig. 4.2.1.1 Built-in power supply circuit

Power supply voltage booster/halver

The power supply voltage booster/halver generates the operating voltage V_{D2} for the voltage regulator (LCD system voltage regulator). The S1C63632 allows software to control the power supply voltage booster/halver and to select the power source of the voltage regulator.

Internal voltage regulator

This voltage regulator always operates to generate the V_{D1} operating voltage for the internal logic circuits and OSC3 oscillation circuit.

Oscillation system voltage regulator

This voltage regulator always operates to generate the V_{OSC} voltage for driving the OSC1 oscillation circuit.

LCD system voltage regulator

The LCD system voltage regulator generates the LCD drive voltages V_{C1} to V_{C5}. See Chapter 7, "Electrical Characteristics" for the voltage values. In the S1C63632, the LCD drive voltage is supplied to the built-in LCD driver which drives the LCD panel connected to the SEG and COM terminals.

Note: Be sure not to use the V_{D1}, V_{D2}, V_{OSC} and V_{C1} to V_{C5} terminal output voltages to drive external circuits.

4.2.2 Controlling the power supply voltage booster/halver and voltage regulators

Controlling the power supply voltage booster/halver

The power supply voltage booster/halver generates the operating voltage V_{D2} for driving the voltage regulator (LCD system voltage regulator) when the supply voltage V_{DD} is out of their operating voltage range.
The power supply voltage booster/halver has two operating modes, boost mode and halving mode, that can be selected using the DBON and HLON registers according to the V_{DD} value being supplied.
The power supply voltage booster/halver enters boost mode by setting DBON to "1" and boosts the supply voltage V_{DD} to generate V_{D2} (about double V_{DD}). The power supply voltage booster/halver should be placed in boost mode only when V_{D2} is required for driving the LCD system voltage regulator (see "Controlling the LCD system voltage regulator" described below).
HLON is prohibited from use. Always be sure to set to "0".
Setting both DBON and HLON to "0" turns the power supply voltage booster/halver off. The V_{D2} voltage is not required when the supply voltage V_{DD} is within the range from 2.5 V to 5.5 V (1.6 V to 5.5 V when the V_{C1} reference LCD drive power option is selected). In this case the power supply voltage booster/halver should be turned off to reduce current consumption.
At initial reset, DBON and HLON are both set to "0" and the power supply voltage booster/halver does not activate.

Controlling the LCD system voltage regulator

When the V_{C2} reference LCD drive power option is selected, the LCD system voltage regulator must be driven with a 2.5 V or more power voltage. Therefore, they can be driven with V_{DD} if the supply voltage V_{DD} is 2.5 V or more. When the supply voltage V_{DD} less than 2.5 V is used, drive the power supply voltage booster/halver in boost mode to generate V_{D2} and use it to drive the LCD system voltage regulator.
Use VCSEL to select the power source voltage (V_{DD} or V_{D2}) for the LCD system voltage regulator. It is driven with V_{DD} by setting VCSEL to "0" or V_{D2} by setting VCSEL to "1".
At initial reset, VCSEL is set to "0" so that V_{DD} is selected as the power source for the LCD system voltage regulator.

To generate the LCD drive voltages by the LCD system voltage regulator (to start LCD display), turn the LCD system voltage regulator on using the LPWR register. When "1" is written to LPWR, the LCD system voltage regulator goes on and generates the LCD drive voltages. At initial reset, LPWR is set to "0" (Off). When LCD display is not necessary, turn the LCD system voltage regulator off to reduce power consumption.

Notes:
- *When driving the LCD system voltage regulator with V_{D2}, be sure to write "1" to DBON to place the power supply voltage booster/halver in boost mode before setting VCSEL to "1". Furthermore, do not switch the power source to V_{D2} for about 1 msec until the V_{D2} voltage has stabilized after the power supply voltage booster/halver is turned on.*
- *Do not set DBON to "1" (boost mode) and VCSEL to "1" (driving with V_{D2}) if the supply voltage V_{DD} exceeds 2.5 V, as it may cause damage of the IC.*
- *If V_{DD} less than 2.5 V is used as the power source for the LCD system voltage regulator, the V_{C1} to V_{C5} voltages cannot be generated within specifications (when a V_{C2} reference voltage option is selected).*

Table 4.2.2.1 lists settings of the above registers according to the supply voltage V_{DD}.

Table 4.2.2.1 Power control register settings according to supply voltage V_{DD}

When V_{C2} reference LCD drive power option is selected

Power supply voltage V_{DD}	DBON	HLON	VDSEL	VCSEL	Power source for internal and oscillation system voltage regulators	Power source for LCD system voltage regulator (V_{C2} reference)
1.6 to 2.5 V	1	0	0	1	V_{DD}	V_{D2} ($\approx V_{DD} \times 2$)
2.5 to 5.5 V	0	0	0	0	V_{DD}	V_{DD}

When V_{C1} reference LCD drive power option is selected

Power supply voltage V_{DD}	DBON	HLON	VDSEL	VCSEL	Power source for internal and oscillation system voltage regulators	Power source for LCD system voltage regulator (V_{C1} reference)
1.6 to 5.5 V	0	0	0	0	V_{DD}	V_{DD}

4.2.3 Heavy load protection function

In order to ensure a stable circuit behavior and LCD display quality even if the power supply voltage fluctuates due to driving an external load, the internal operating voltage regulator and the LCD system voltage regulator have a heavy load protection function.
The internal operating voltage regulator enters heavy load protection mode by writing "1" to the VDHLMOD register and it ensures stable V_{D1} output. Use the heavy load protection function when a heavy load such as a lamp or buzzer is driven with a port output.

The LCD system voltage regulator enters heavy load protection mode by writing "1" to the VCHLMOD register and it ensures stable V_{C1}–V_{C5} outputs. Use the heavy load protection function when the LCD display has inconsistencies in density.

Note: Current consumption increases in heavy load protection mode, therefore do not set heavy load protection mode with software if unnecessary.

4.2.4 I/O memory for power control

Table 4.2.4.1 shows the I/O address and the control bits for power control.

Table 4.2.4.1 Power control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF02H	VDSEL	VCSEL	HLON	DBON	VDSEL	0	1	0	General-purpose register
					VCSEL	0	V_{D2}	V_{DD}	Power source select for LCD system voltage regulator
	R/W				HLON	0	On	Off	Power voltage booster/halver halving mode On/Off
					DBON	0	On	Off	Power voltage booster/halver boost mode On/Off
FF03H	VCHLMOD	VDHLMOD	General	LPWR	VCHLMOD	0	On	Off	Heavy load protection mode On/Off for LCD system voltage regulator
					VDHLMOD	0	On	Off	Heavy load protection mode On/Off for internal voltage regulator
	R/W				General	0	1	0	General-purpose register
					LPWR	0	On	Off	LCD system voltage regulator On/Off

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

DBON: Power supply voltage booster/halver boost mode On/Off register (FF02H•D0)
Activates the power supply voltage booster/halver in boost mode.

When "1" is written: Booster On
When "0" is written: Booster Off
Reading: Valid

When "1" is written to DBON, the power supply voltage booster/halver activates in boost mode and almost doubles the V_{DD} voltage to generate the V_{D2} voltage. Turn the power supply voltage booster/halver on when driving the LCD system voltage regulator with V_{D2} (V_{C2} reference voltage, V_{DD} = 1.6 to 2.5 V). When "0" is written to DBON, the voltage boost operation is deactivated. Be sure to set DBON to "0" (Off) when driving the LCD system voltage regulator with V_{DD}. Furthermore, do not set both DBON and HLON to "1".
At initial reset, this register is set to "0".

HLON: Power supply voltage booster/halver halving mode On/Off register (FF02H•D1)
Activates the power supply voltage booster/halver in halving mode.

When "1" is written: Halver On
When "0" is written: Halver Off
Reading: Valid

HLON is prohibited from use. Always be sure to set to "0".
At initial reset, this register is set to "0".

VCSEL: LCD system voltage regulator power source switch register (FF02H•D2)
Selects the power voltage for the LCD system voltage regulator.

When "1" is written: V_{D2}
When "0" is written: V_{DD}
Reading: Valid

When "1" is written to VCSEL, the LCD system voltage regulator is driven with V_{D2} generated by the power supply voltage booster/halver. Before this setting is made, it is necessary to write "1" to DBON to activate the power supply voltage booster (boost mode). Furthermore, do not switch the power voltage to V_{D2} for at least 1 msec after the power supply voltage booster/halver is turned on to allow V_{D2} to stabilize. When "0" is written to VCSEL, the LCD system voltage regulator is driven with V_{DD}.
At initial reset, this register is set to "0".

Note: Do not set DBON to "1" (boost mode) and VCSEL to "1" (driving with V_{D2}) if the supply voltage V_{DD} exceeds 2.5 V, as it may cause damage of the IC.

LPWR: LCD system voltage regulator On/Off register (FF03H•D0)
Turns the LCD system voltage regulator on and off.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to LPWR, the LCD system voltage regulator goes on and generates the LCD drive voltages. When "0" is written, all the LCD drive voltages go to V_{SS} level.
It takes about 100 msec for the LCD drive voltages to stabilize after starting up the LCD system voltage regulator by writing "1" to LPWR.
At initial reset, this register is set to "0".

VDHLMOD: Internal operating voltage regulator heavy load protection On/Off register (FF03H•D2)
Enables heavy load protection function for the internal operating voltage regulator.

When "1" is written: On
When "0" is written: Off
Reading: Valid

By writing "1" to VDHLMOD, the internal operating voltage regulator enters heavy load protection mode and it ensures stable V_{D1} output. The heavy load protection function is effective when the buzzer/FOUT signal is being output. However, heavy load protection mode increases current consumption compared with normal operation mode. Therefore, do not set heavy load protection mode unless it is necessary.
At initial reset, this register is set to "0".

VCHLMOD: LCD system voltage regulator heavy load protection On/Off register (FF03H•D3)

Enables heavy load protection function for the LCD system voltage regulator.

When "1" is written: On
When "0" is written: Off
Reading: Valid

By writing "1" to VCHLMOD, the LCD system voltage regulator enters heavy load protection mode to minimize degradation in display quality when fluctuations in the supply voltage occurs due to driving a heavy load. The heavy load protection function is effective when the OSC3 clock is used or the buzzer/FOUT signal is being output. However, heavy load protection mode increases current consumption compared with normal operation mode. Therefore, do not set heavy load protection mode unless it is necessary.
At initial reset, this register is set to "0".

4.2.5 Programming notes

(1) When the power supply voltage booster/halver is turned on, the V_{D2} output voltage requires about 1 msec to stabilize. Do not switch the power source for the voltage regulator (LCD system voltage regulator) to V_{D2} until the stabilization time has elapsed.

(2) HLON is prohibited from use, as it may cause malfunctions. Always be sure to set to "0".

(3) Do not set DBON to "1" (boost mode) and VCSEL to "1" (driving with V_{D2}) if the supply voltage V_{DD} exceeds 2.5 V, as it may cause damage of the IC.

(4) Current consumption increases in heavy load protection mode, therefore do not set heavy load protection mode with software if unnecessary.

4.3 Watchdog Timer

4.3.1 Configuration of watchdog timer

The S1C63632 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.
Figure 4.3.1.1 is the block diagram of the watchdog timer.

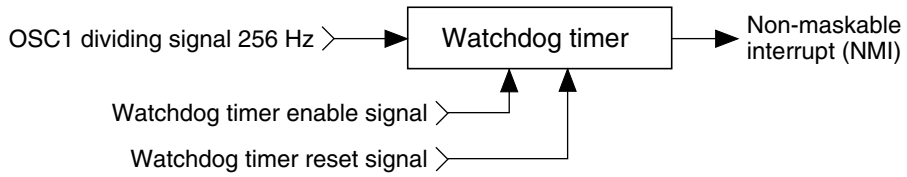


Fig. 4.3.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

4.3.2 Interrupt function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "0"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

4.3.3 I/O memory of watchdog timer

Table 4.3.3.1 shows the I/O address and control bits for the watchdog timer.

Table 4.3.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF01H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

WDRST: Watchdog timer reset (FF01H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

WDEN: Watchdog timer enable register (FF01H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI).
At initial reset, this register is set to "1".

4.3.4 Programming notes

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

4.4 Oscillation Circuit

4.4.1 Configuration of oscillation circuit

The S1C63632 is configured as a twin clock system with two internal oscillation circuits (OSC1 and OSC3). The OSC1 oscillation circuit generates the main-clock (Typ. 32.768 kHz) for low-power operation and the OSC3 oscillation circuit generates the sub-clock (Max. 4.2 MHz) to run the CPU and some peripheral circuits in high speed.
Figure 4.4.1.1 shows the configuration of the oscillation circuit.

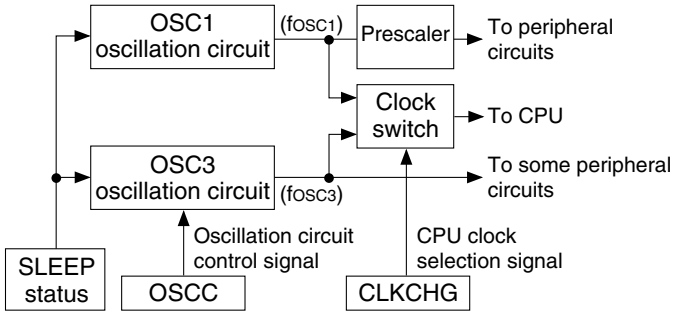


Fig. 4.4.1.1 Oscillation system block diagram

At initial reset, OSC1 oscillation circuit is selected as the CPU operating clock source. The S1C63632 allows the software to turn the OSC3 oscillation circuit on and off, and to switch the system clock between OSC3 and OSC1. The OSC3 oscillation circuit is used when the CPU and some peripheral circuits need high speed operation. Otherwise, use the OSC1 oscillation circuit to generate the operating clock and stop the OSC3 oscillation circuit to reduce current consumption.

Note: The S1C63632 supports the SLEEP function and both the OSC1 and OSC3 oscillation circuits stop oscillating when the CPU enters SLEEP mode. To prevent the CPU from a malfunction when it resumes operating from SLEEP mode, switch the CPU clock to OSC1 before placing the CPU into SLEEP mode.

4.4.2 Mask option

The OSC1 oscillator type is fixed at crystal.
For the OSC3 oscillator type, either ceramic or CR (external R) can be selected.

4.4.3 OSC1 oscillation circuit

The OSC1 oscillation circuit generates the 32.768 kHz (Typ.) system clock which is used during low speed (low power) operation of the CPU and peripheral circuits. Furthermore, even when OSC3 is used as the system clock, OSC1 continues to generate the source clock for the clock timer and stopwatch timer. This oscillation circuit stops when the SLP instruction is executed.
Figure 4.4.3.1 shows the configuration of the OSC1 oscillation circuit.

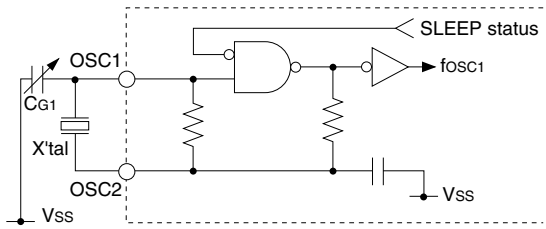
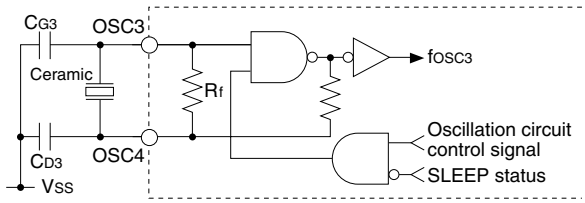


Fig. 4.4.3.1 OSC1 oscillation circuit (crystal oscillation)

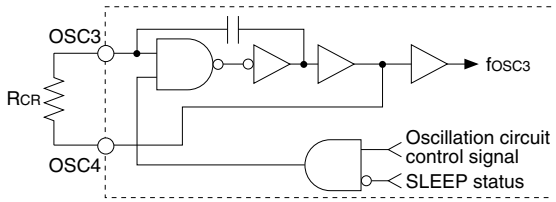
A crystal oscillation circuit can be configured simply by connecting a crystal oscillator X'tal (Typ. 32.768 kHz) between the OSC1 and OSC2 terminals along with a trimmer capacitor C_{G1} (0–25 pF) between the OSC1 terminal and V_{SS}.

4.4.4 OSC3 oscillation circuit

The OSC3 oscillation circuit generates the system clock to run the CPU and some peripheral circuits at high speed. This oscillation circuit stops when the SLP instruction is executed or the OSCC register is set to "0".
The oscillator type can be selected from ceramic or CR by mask option.
Figure 4.4.4.1 shows the configuration of the OSC3 oscillation circuit.



(1) Ceramic oscillation circuit



(2) CR oscillation circuit

Fig. 4.4.4.1 OSC3 oscillation circuit

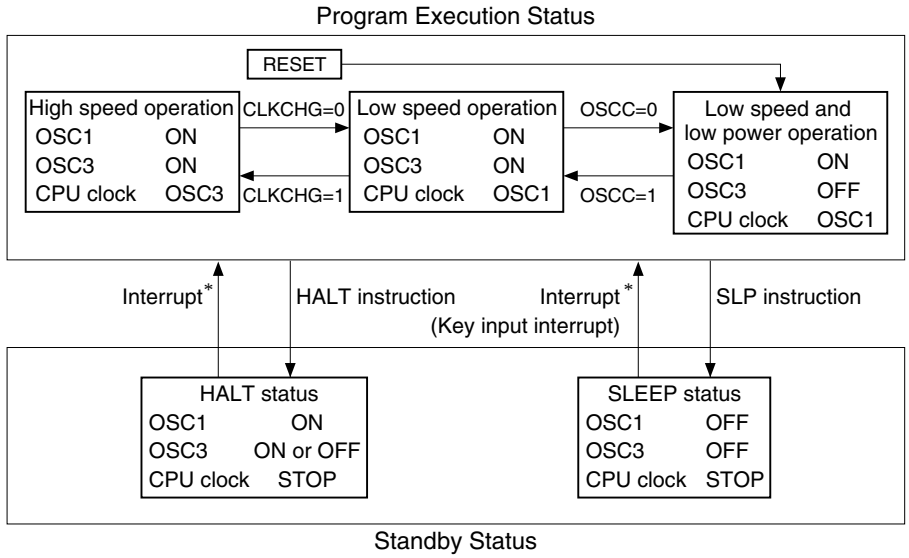
When ceramic oscillation circuit (Max. 4.2 MHz) is selected, connect a ceramic oscillator (Ceramic) between the OSC3 and OSC4 terminals and connecting two capacitors (C_{G3}, C_{D3}) between the OSC3 terminal and V_{SS}, and between the OSC4 terminal and V_{SS}, respectively.

When CR oscillation (Max. 2 MHz) is selected, connect a resistor (R_{CR}) between the OSC3 and OSC4 terminals.

4.4.5 Switching the CPU clock

Either the OSC1 clock or the OSC3 clock can be selected as the CPU system clock using the CLKCHG register.
The OSC3 oscillation circuit can be turned off (OSCC = "0") to save power while the CPU is operating with the OSC1 clock (CLKCHG = "0").
If the system needs high speed operation, turn the OSC3 oscillation circuit on (OSCC = "1") and switch over the system clock to OSC3 (CLKCHG = "0" → "1").
In this case, since 1 msec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit on, you should switch over the clock after the stabilization time has elapsed. For the oscillation start time, refer to Chapter 8, "Electrical Characteristics".
After the clock is switched from OSC3 to OSC1, the OSC3 oscillation circuit can be turned off immediately.
When switching the clock from OSC3 to OSC1 (CLKCHG = "1" → "0"), be sure to switch OSC3 oscillation off with separate instructions. Using a single instruction to process simultaneously can cause a malfunction of the CPU.

Figure 4.4.5.1 indicates the status transition diagram for the clock changeover.



* The return destination from the standby status becomes the program execution status prior to shifting to the standby status.

Fig. 4.4.5.1 Status transition diagram for the clock changeover

4.4.6 I/O memory of oscillation circuit

Table 4.4.6.1 shows the I/O address and the control bits for the oscillation circuit.

Note: The control bits for the oscillation circuit described below are effective only when the OSC3 oscillation circuit is used. If the system uses the OSC1 oscillation circuit only, do not change the default settings.

Table 4.4.6.1 Control bits of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF00H	CLKCHG	OSCC	0	0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

OSCC: OSC3 oscillation control register (FF00H•D2)

Turns the OSC3 oscillation circuit on and off.

When "1" is written: OSC3 oscillation On
When "0" is written: OSC3 oscillation Off
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption.
At initial reset, this register is set to "0".

CLKCHG: CPU system clock switching register (FF00H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
At initial reset, this register is set to "0".

4.4.7 Programming notes

(1) When the high speed CPU operation is not necessary, you should operate the peripheral circuits according to the setting outline indicate below.
- CPU operating clock: OSC1
- OSC3 oscillation circuit: Off

(When the OSC3 clock is not necessary for some peripheral circuits.)

(2) Since 1 msec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit on. Consequently, you should switch the CPU operating clock (OSC1 → OSC3) after allowing for a sufficient waiting time once the OSC3 oscillation goes on. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "Electrical Characteristics".)

(3) When switching the clock from OSC3 to OSC1, be sure to switch OSC3 oscillation off with separate instructions. Using a single instruction to process simultaneously can cause a malfunction of the CPU.

(4) The S1C63632 supports the SLEEP function and both the OSC1 and OSC3 oscillation circuits stop oscillating when the CPU enters SLEEP mode. To prevent the CPU from a malfunction when it resumes operating from SLEEP mode, switch the CPU clock to OSC1 before placing the CPU into SLEEP mode.

4.5 I/O Ports *(P00–P03, P10–P13, P20–P23, P30–P33, P40–P43 and P50–P53)*

4.5.1 Configuration of I/O ports

The S1C63632 is equipped with 24 bits of I/O ports (P00–P03, P10–P13, P20–P23, P30–P33, P40–P43, and P50–P53) in which the input/output direction can be switched with software.
Figure 4.5.1.1 shows the structure of an I/O port.

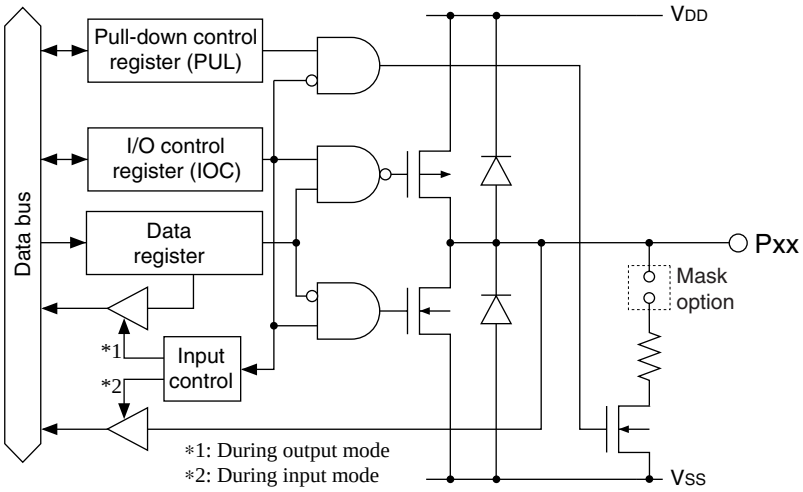


Fig. 4.5.1.1 Structure of I/O port

Note: If an output terminal (including a special output terminal) of this IC is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.

Each I/O port terminal provides an internal pull-down resistor. The mask option allows selection of the pull-down resistor to be connected or disconnected in 1-bit units.
When "Use" is selected by mask option, the port suits input from the push switch, key matrix, and so forth. When "Not use" is selected, the port can be used for slide switch input and interfacing with other LSIs.

The P10 and P11 I/O ports can also be used as the Run/Stop and Lap direct inputs for the stopwatch timer. The P12 and P41–P43 ports can also be used as the event counter inputs for the programmable timer.

The I/O port terminals P00–P03, P13, P20–P23, P31–P33 are shared with the R/f converter input/output terminals, serial interface input/output terminals and special output (BZ, FOUT, TOUT_A–TOUT_D) terminals. The software can select the function to be used.
At initial reset, these terminals are all set to the I/O port.
Table 4.5.1.1 shows the setting of the input/output terminals by function selection.

Table 4.5.1.1 Function setting of input/output terminals

Terminal name	Terminal status at initial reset	When special outputs/peripheral functions are used (selected by software)							
		Special output			Serial I/F		R/f converter	Stopwatch direct input	Event counter
		TOUT	FOUT	BZ	Master	Slave			
P00	P00 (Input & pulled down*)						RFIN0		
P01	P01 (Input & pulled down*)						REF0		
P02	P02 (Input & pulled down*)						SEN0		
P03	P03 (Input & pulled down*)			BZ			RFOUT		
P10	P10 (Input & pulled down*)							RUN/LAP	
P11	P11 (Input & pulled down*)							RUN/LAP	
P12	P12 (Input & pulled down*)								EVIN_A
P13	P13 (Input & pulled down*)	TOUT_A							
P20	P20 (Input & pulled down*)				SCLK(O)	SCLK(I)			
P21	P21 (Input & pulled down*)				SOUT(O)	SOUT(O)			
P22	P22 (Input & pulled down*)				SIN(I)	SIN(I)			
P23	P23 (Input & pulled down*)		FOUT			SRDY(O)/$\overline{SS}$(I)			
P30	P30 (Input & pulled down*)								
P31	P31 (Input & pulled down*)	TOUT_B							
P32	P32 (Input & pulled down*)	TOUT_C							
P33	P33 (Input & pulled down*)	TOUT_D							
P40	P40 (Input & pulled down*)								
P41	P41 (Input & pulled down*)								EVIN_B
P42	P42 (Input & pulled down*)								EVIN_C
P43	P43 (Input & pulled down*)								EVIN_D
P50–P53	P50–P53 (Input & pulled down*)								

* When "With Pull-Down" is selected by mask option (high impedance when "Gate Direct" is selected)

When these ports are used as I/O ports, the ports can be set to either input mode or output mode individually (in 1-bit units). The mode can be set by writing data to the I/O control registers.

When the special output or peripheral function is used, the input/output direction of the port is automatically configured by switching the terminal function. For controlling the serial interface, R/f converter, BZ output, stopwatch timer, and event counter, refer to "4.10 Serial Interface", "4.13 R/f Converter", "4.11 Sound Generator", "4.8 Stopwatch Timer", and "4.9 Programmable Timer".

Note: Before the port function is configured, the circuit that uses the port (e.g. input interrupt, multiple key entry reset, serial interface, event counter input, direct RUN/LAP input for stopwatch) must be disabled.

4.5.2 Mask option

The output specification of each I/O port during output mode can be selected from either complementary output or P-channel open drain output by mask option. This selection can be done in 1-bit units. When P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the port.

The mask option also allows selection of whether the pull-down resistor is used or not during input mode. This selection can be done in 1-bit units. When "Not use" is selected, take care that the floating status does not occur during input mode.

The pull-down resistor for input mode and output specification (complementary output or P-channel open drain output) selected by mask option are effective even when I/O ports are used for input/output of the serial interface and R/f converter.

4.5.3 I/O control registers and input/output mode

The I/O ports can be placed into input or output mode by writing data to the corresponding I/O control registers IOCxx.

To set a port to input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull-down explained in Section 4.5.5 has been enabled by software, the input line is pulled down only during this input mode.

To set a port to output mode, write "1" to the I/O control register. When an I/O port is set to output mode, it works as an output port. The port outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0". The I/O ports allow software to read data even in output mode. In this case, the data register value is read out.
At initial reset, the I/O control registers are set to "0", and the I/O ports enter input mode.

When the peripheral input/output or special output function is selected (see Table 4.5.1.1), the input/output direction is controlled by the hardware. In this case, the I/O control register of the port can be used as a general purpose register that does not affect the I/O control.

4.5.4 Input interface level

The I/O ports allow software to select an input interface level. When the input interface level select register SMTxx is set to "0", the corresponding port is configured with a CMOS level input interface. When SMTxx is set to "1", the port is configured with a CMOS Schmitt level input interface. At initial reset, all the ports are configured with a CMOS Schmitt level interface.

The input interface level select register of the port that is set for a peripheral output , R/f converter input/output or special output (see Table 4.5.1.1) can be used as a general-purpose register.
The input interface level select register of the port that is set for a peripheral input (except for the R/f converter) functions the same as the I/O port.

4.5.5 Pull-down during input mode

A pull-down resistor that activates during the input mode can be built into the I/O ports of the S1C63632. The pull-down resistor becomes effective by writing "1" to the pull-down control register PULxx that corresponds to each port, and the input line is pulled down during input mode. When "0" is written to PULxx or in output mode, the port will not be pulled down.
At initial reset, the pull-down control registers are set to "1".

The pull-down control registers of the ports in which the pull-down resistor is disconnected by mask option can be used as general purpose registers.
Even if the pull-down resistor has been connected, the pull-down control register of the port that is set for a peripheral output, R/f converter input/output or output special output (see Table 4.5.1.1) can be used as a general purpose register that does not affect the pull-down control. The pull-down control register of the port that is set for a peripheral input (except for the R/f converter) functions the same as the I/O port.

4.5.6 Special output

Besides general purpose DC input/output, the I/O ports P03, P13, P23 and P31–P33 can also be assigned special output functions in software as shown in Table 4.5.6.1.

Table 4.5.6.1 Special output ports

Port	Special output	Special output control register
P03	BZ	BZE, BZSHT
P13	TOUT_A	PTOUT_A
P23	FOUT	FOUT0–FOUT3
P31	TOUT_B	PTOUT_B
P32	TOUT_C	PTOUT_C
P33	TOUT_D	PTOUT_D

When a special output function is enabled using the special output control register, the corresponding I/O port is automatically configured for output. The data register, I/O control register, pull-down control register and input interface level select register of the special output port can be used as general-purpose registers that do not affect the output status.

TOUT output (P13, P31–P33)

In order for the S1C63632 to provide clock signals to external devices, the P13 and P31–P33 terminals can be used to output the TOUT_A–TOUT_D signals (clocks output by the programmable timer).

The TOUT_x signal (x = A–D) is enabled to output by the PTOUT_x register. When PTOUT_x is set to "1", the TOUT_x signal is output from the corresponding port terminal. The I/O control register (IOC13, IOC31, IOC32 or IOC33), pull-down control register (PUL13, PUL31, PUL32 or PUL33) and data register (P13, P31, P32 or P33) settings are ineffective while the TOUT_x signal is being output. When PTOUT_x is set to "0", the port is configured as a general-purpose DC input/output port.

The TOUT_x signal is generated from the underflow and compare-match signals of a programmable timer. Refer to Section 4.9, "Programmable Timer", for controlling the clock output and frequency. Since the TOUT_x signal is generated asynchronously from the PTOUT_x register, a hazard of a 1/2 cycle or less is generated when the signal is turned on or off by setting the register.
Figure 4.5.6.1 shows the output waveform of the TOUT_x signal.

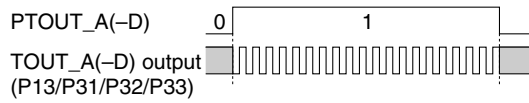


Fig. 4.5.6.1 Output waveform of TOUT_x signal

FOUT output (P23)

In order for the S1C63632 to provide a clock signal to an external device, the FOUT signal (f_{OSC1}, f_{OSC3} or a divided clock) can be output from the P23 port terminal.

The FOUT signal is enabled to output by the FOUT0–FOUT3 registers. When the output clock frequency is selected using FOUT0–FOUT3, the FOUT signal is output from the P23 port terminal. The I/O control register (IOC23), pull-down control register (PUL23) and data register (P23) settings are ineffective while the FOUT signal is being output.
When FOUT0–FOUT3 are set to "0", the P23 port is configured as a general-purpose DC input/output port.

The frequency of the FOUT signal can be selected from among 15 settings as shown in Table 4.5.6.2.

Table 4.5.6.2 FOUT frequency selection

FOUT3	FOUT2	FOUT1	FOUT0	FOUT frequency
1	1	1	1	f_{OSC3}
1	1	1	0	f_{OSC3} / 2
1	1	0	1	f_{OSC3} / 4
1	1	0	0	f_{OSC3} / 8
1	0	1	1	f_{OSC3} / 16
1	0	1	0	f_{OSC3} / 32
1	0	0	1	f_{OSC3} / 64
1	0	0	0	f_{OSC3} / 256
0	1	1	1	f_{OSC1} (32 kHz)
0	1	1	0	f_{OSC1} / 2 (16 kHz)
0	1	0	1	f_{OSC1} / 4 (8 kHz)
0	1	0	0	f_{OSC1} / 16 (2 kHz)
0	0	1	1	f_{OSC1} / 32 (1 kHz)
0	0	1	0	f_{OSC1} / 64 (512 Hz)
0	0	0	1	f_{OSC1} / 256 (128 Hz)
0	0	0	0	Off

f_{OSC1}: OSC1 oscillation frequency. ( ) indicates the clock frequency when f_{OSC1} = 32 kHz.
f_{OSC3}: OSC3 oscillation frequency

When the FOUT frequency is set to "f_{OSC3}/n", the OSC3 oscillation circuit must be turned on before outputting the FOUT signal. A time interval of several tens of µsec to several tens of msec, from turning the OSC3 oscillation circuit on until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning the OSC3 oscillation on, before starting FOUT output. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "Electrical Characteristics".)
Since the FOUT signal is generated asynchronously from the FOUT0–FOUT3 registers, a hazard of a 1/2 cycle or less is generated when the signal is turned on or off by setting the registers.
Figure 4.5.6.2 shows the output waveform of the FOUT signal.

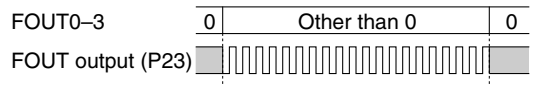


Fig. 4.5.6.2 Output waveform of FOUT signal

Note: The P23 terminal used for FOUT output is also shared with the SRDY output or $\overline{SS}$ input for the serial interface. When the P23 port is configured for the serial interface, the FOUT0–FOUT3 registers become ineffective.

BZ (P03)

The P03 terminal can output the BZ signal.
The BZ signal is the buzzer signal generated by the sound generator.
Use the BZE or BZSHT register for controlling (On/Off) the BZ signal output.
Refer to Section 4.11, "Sound Generator", for details of the buzzer signal and controlling method.

Note: The P03 terminal used for BZ output is also shared with the RFOUT output for the R/f converter. Do not enable the RFOUT and BZ signals to output simultaneously.

4.5.7 Key input interrupt function

Eight bits of the I/O ports (P10–P13, P40–P43) provide the interrupt function. The conditions for generating an interrupt can be set with software. Further, whether to mask the interrupt function can be selected with software. Figure 4.5.7.1 shows the configuration of the key input interrupt circuit.

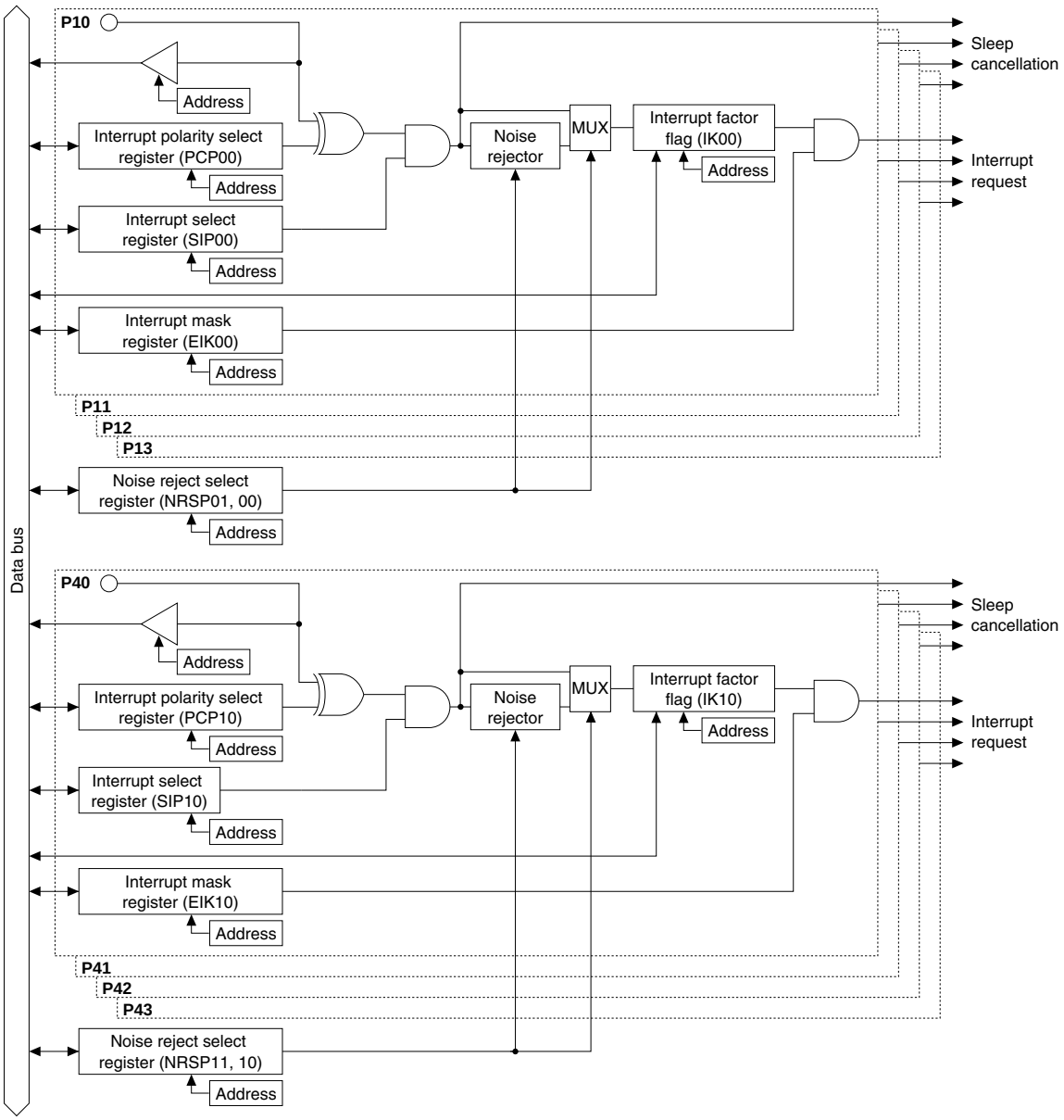


Fig. 4.5.7.1 Key input interrupt circuit configuration

The interrupt select registers (SIP00–SIP03, SIP10–SIP13) and interrupt polarity select registers (PCP00–PCP03, PCP10–PCP13) are individually provided for the I/O ports P10–P13 and P40–P43.

The interrupt select registers (SIPxx) select the ports to be used for generating interrupts or canceling SLEEP mode. Writing "1" to an interrupt select register incorporates that port into the interrupt generation conditions. Changing the port where the interrupt select register has been set to "0" does not affect the generation of the interrupt.

The input interrupt timing can be selected using the interrupt polarity select registers (PCPxx) so that an interrupt will be generated at the rising edge or falling edge of the input.

By setting these two conditions, an interrupt request signal and a SLEEP cancellation signal are generated at the rising or falling edge (selected by PCPxx) of the signal input to the port (selected by SIPxx).

When an interrupt factor occurs, the interrupt factor flag (IK00–IK03, IK10–IK13) is set to "1". At the same time, an interrupt request is generated to the CPU if the corresponding interrupt mask register (EIK00–EIK03, EIK10–EIK13) is set to "1".
When the interrupt mask register (EIKxx) is set to "0", the interrupt request is masked and no interrupt is generated to the CPU. However, SLEEP mode can be cancelled regardless of the interrupt mask register setting.

The key input interrupt circuit has a noise rejector to avoid unnecessary interrupt generation due to noise or chattering. This noise rejector allows selection of a noise-reject frequency from among three types shown in Table 4.5.7.1. Use the NRSP01 and NRSP00 registers for P10–P13 ports or NRSP11 and NRSP10 registers for P40–P43 ports to select a noise-reject frequency. If a pulse shorter than the selected width is input to the port, an interrupt is not generated. When high speed response is required, turns the noise rejecter off (bypassed).

Table 4.5.7.1 Setting up noise rejector

NRSP01 NRSP11	NRSP00 NRSP10	Noise reject frequency	Reject pulse width
1	1	f_{OSC1} / 256 (128 Hz)	7.8 msec
1	0	f_{OSC1} / 64 (512 Hz)	2.0 msec
0	1	f_{OSC1} / 16 (2 kHz)	0.5 msec
0	0	OFF (bypassed)	–

Notes:
- *Be sure to turn the noise rejector off before executing the SLP instruction.*
- *Reactivating from SLEEP status can only be done by generation of a key input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt select register (SIPxx = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction. Furthermore, enable the key input interrupt using the corresponding interrupt mask register (EIKxx = "1") before executing the SLP instruction to run key input interrupt handler routine after SLEEP status is released.*

4.5.8 I/O memory of I/O ports

Table 4.5.8.1 shows the I/O addresses and the control bits for the I/O ports.

Table 4.5.8.1(a) Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF10H	FOUT3	FOUT2	FOUT1	FOUT0	FOUT3	0			FOUT frequency selection [FOUT3–0] 0 1 2 3 4 5 Frequency Off fOSC1/256 fOSC1/64 fOSC1/32 fOSC1/16 fOSC1/4 [FOUT3–0] 6 7 8 9 10 Frequency fOSC1/2 fOSC1 fOSC3/256 fOSC3/64 fOSC3/32 [FOUT3–0] 11 12 13 14 15 Frequency fOSC3/16 fOSC3/8 fOSC3/4 fOSC3/2 fOSC3
					FOUT2	0			
	R/W				FOUT1	0			
					FOUT0	0			
FF11H	NRSP11	NRSP10	NRSP01	NRSP00	NRSP11	0			Key input interrupt noise reject frequency selection [NRSP11, 10] (P40–P43) 0 1 2 3 Frequency Off fOSC1/16 fOSC1/64 fOSC1/256 [NRSP01, 00] (P10–P13) 0 1 2 3 Frequency Off fOSC1/16 fOSC1/64 fOSC1/256
					NRSP10	0			
	R/W				NRSP01	0			
					NRSP00	0			
FF20H	P03 (RFOUT/ BZ)	P02 (SEN0)	P01 (REF0)	P00 (RFIN0)	P03	1	High	Low	P03 I/O port data functions as a general-purpose register when R/f or BZ is used
					P02	1	High	Low	P02 I/O port data functions as a general-purpose register when R/f is used
	R/W				P01	1	High	Low	P01 I/O port data functions as a general-purpose register when R/f is used
					P00	1	High	Low	P00 I/O port data functions as a general-purpose register when R/f is used
FF21H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P03 I/O control register functions as a general-purpose register when R/f or BZ is used
					IOC02	0	Output	Input	P02 I/O control register functions as a general-purpose register when R/f is used
	R/W				IOC01	0	Output	Input	P01 I/O control register functions as a general-purpose register when R/f is used
					IOC00	0	Output	Input	P00 I/O control register functions as a general-purpose register when R/f is used
FF22H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P03 pull-down control register functions as a general-purpose register when R/f or BZ is used
					PUL02	1	On	Off	P02 pull-down control register functions as a general-purpose register when R/f is used
	R/W				PUL01	1	On	Off	P01 pull-down control register functions as a general-purpose register when R/f is used
					PUL00	1	On	Off	P00 pull-down control register functions as a general-purpose register when R/f is used
FF23H	SMT03	SMT02	SMT01	SMT00	SMT03	1	Schmitt	CMOS	P03 input interface level select register functions as a general-purpose register when R/f or BZ is used
					SMT02	1	Schmitt	CMOS	P02 input interface level select register functions as a general-purpose register when R/f is used
	R/W				SMT01	1	Schmitt	CMOS	P01 input interface level select register functions as a general-purpose register when R/f is used
					SMT00	1	Schmitt	CMOS	P00 input interface level select register functions as a general-purpose register when R/f is used
FF24H	P13 (TOUT_A)	P12	P11	P10	P13	1	High	Low	P13 I/O port data functions as a general-purpose register when TOUT_A is used
					P12	1	High	Low	P12 I/O port data
	R/W				P11	1	High	Low	P11 I/O port data
					P10	1	High	Low	P10 I/O port data
FF25H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when TOUT_A is used
					IOC12	0	Output	Input	P12 I/O control register
	R/W				IOC11	0	Output	Input	P11 I/O control register
					IOC10	0	Output	Input	P10 I/O control register

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.5.8.1(b) Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF26H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when TOUT_A is used
					PUL12	1	On	Off	P12 pull-down control register
	R/W				PUL11	1	On	Off	P11 pull-down control register
					PUL10	1	On	Off	P10 pull-down control register
FF27H	SMT13	SMT12	SMT11	SMT10	SMT13	1	Schmitt	CMOS	P13 input interface level select register functions as a general-purpose register when TOUT_A is used
					SMT12	1	Schmitt	CMOS	P12 input interface level select register
	R/W				SMT11	1	Schmitt	CMOS	P11 input interface level select register
					SMT10	1	Schmitt	CMOS	P10 input interface level select register
FF28H	P23 ($\overline{SS}$/ SRDY/ FOUT)	P22 (SIN)	P21 (SOUT)	P20 (SCLK)	P23	1	High	Low	P23 I/O port data functions as a general-purpose register when SIF (slave, SRDY) or FOUT is used
					P22	1	High	Low	P22 I/O port data
	R/W				P21	1	High	Low	P21 I/O port data functions as a general-purpose register when SIF is used
					P20	1	High	Low	P20 I/O port data functions as a general-purpose register when SIF (master) is used
FF29H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register functions as a general-purpose register when SIF or FOUT is used
					IOC22	0	Output	Input	P22 I/O control register functions as a general-purpose register when SIF is used
	R/W				IOC21	0	Output	Input	P21 I/O control register functions as a general-purpose register when SIF is used
					IOC20	0	Output	Input	P20 I/O control register functions as a general-purpose register when SIF is used
FF2AH	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-down control register $\overline{SS}$ pull-down control register when SIF (slave, $\overline{SS}$) is used functions as a general-purpose register when SIF (slave, SRDY) or FOUT is used
					PUL22	1	On	Off	P22 pull-down control register SIN pull-down control register when SIF is used
	R/W				PUL21	1	On	Off	P21 pull-down control register functions as a general-purpose register when SIF (SOUT) is used
					PUL20	1	On	Off	P20 pull-down control register SCLK (I) pull-down control register when SIF (slave) is used functions as a general-purpose register when SIF (master) is used
FF2BH	SMT23	SMT22	SMT21	SMT20	SMT23	1	Schmitt	CMOS	P23 input interface level select register $\overline{SS}$ input I/F level select register when SIF (slave, $\overline{SS}$) is used functions as a general-purpose register when SIF (slave, SRDY) or FOUT is used
					SMT22	1	Schmitt	CMOS	P22 input interface level select register SIN input interface level select register when SIF is used
	R/W				SMT21	1	Schmitt	CMOS	P21 input interface level select register functions as a general-purpose register when SIF (SOUT) is used
					SMT20	1	Schmitt	CMOS	P20 input interface level select register SCLK (I) input I/F level select register when SIF (slave) is used functions as a general-purpose register when SIF (master) is used
FF2CH	P33 (TOUT_D)	P32 (TOUT_C)	P31 (TOUT_B)	P30	P33	1	High	Low	P33 I/O port data functions as a general-purpose register TOUT_D is used
					P32	1	High	Low	P32 I/O port data functions as a general-purpose register TOUT_C is used
	R/W				P31	1	High	Low	P31 I/O port data functions as a general-purpose register TOUT_B is used
					P30	1	High	Low	P30 I/O port data

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.5.8.1(c) Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF2DH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P33 I/O control register functions as a general-purpose register TOUT_D is used
					IOC32	0	Output	Input	P32 I/O control register functions as a general-purpose register TOUT_C is used
	R/W				IOC31	0	Output	Input	P31 I/O control register functions as a general-purpose register TOUT_B is used
					IOC30	0	Output	Input	P30 I/O control register
FF2EH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P33 pull-down control register functions as a general-purpose register TOUT_D is used
					PUL32	1	On	Off	P32 pull-down control register functions as a general-purpose register TOUT_C is used
	R/W				PUL31	1	On	Off	P31 pull-down control register functions as a general-purpose register TOUT_B is used
					PUL30	1	On	Off	P30 pull-down control register
FF2FH	SMT33	SMT32	SMT31	SMT30	SMT33	1	Schmitt	CMOS	P33 input interface level select register functions as a general-purpose register TOUT_D is used
					SMT32	1	Schmitt	CMOS	P32 input interface level select register functions as a general-purpose register TOUT_C is used
	R/W				SMT31	1	Schmitt	CMOS	P31 input interface level select register functions as a general-purpose register TOUT_B is used
					SMT30	1	Schmitt	CMOS	P30 input interface level select register
FF30H	P43	P42	P41	P40	P43	1	High	Low	P40–P43 I/O port data
					P42	1	High	Low	
	R/W				P41	1	High	Low	
					P40	1	High	Low	
FF31H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P40–P43 I/O control register
					IOC42	0	Output	Input	
	R/W				IOC41	0	Output	Input	
					IOC40	0	Output	Input	
FF32H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P40–P43 pull-down control register
					PUL42	1	On	Off	
	R/W				PUL41	1	On	Off	
					PUL40	1	On	Off	
FF33H	SMT43	SMT42	SMT41	SMT40	SMT43	1	Schmitt	CMOS	P40–P43 input interface level select register
					SMT42	1	Schmitt	CMOS	
	R/W				SMT41	1	Schmitt	CMOS	
					SMT40	1	Schmitt	CMOS	
FF34H	P53	P52	P51	P50	P53	1	High	Low	P50–P53 I/O port data
					P52	1	High	Low	
	R/W				P51	1	High	Low	
					P50	1	High	Low	
FF35H	IOC53	IOC52	IOC51	IOC50	IOC53	0	Output	Input	P50–P53 I/O control register
					IOC52	0	Output	Input	
	R/W				IOC51	0	Output	Input	
					IOC50	0	Output	Input	
FF36H	PUL53	PUL52	PUL51	PUL50	PUL53	1	On	Off	P50–P53 pull-down control register
					PUL52	1	On	Off	
	R/W				PUL51	1	On	Off	
					PUL50	1	On	Off	
FF37H	SMT53	SMT52	SMT51	SMT50	SMT53	1	Schmitt	CMOS	P50–P53 input interface level select register
					SMT52	1	Schmitt	CMOS	
	R/W				SMT51	1	Schmitt	CMOS	
					SMT50	1	Schmitt	CMOS	
FF3CH	SIP03	SIP02	SIP01	SIP00	SIP03	0	Enable	Disable	P10–P13 interrupt select register
					SIP02	0	Enable	Disable	
	R/W				SIP01	0	Enable	Disable	
					SIP00	0	Enable	Disable	

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.5.8.1(d) Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF3DH	PCP03	PCP02	PCP01	PCP00	PCP03	1	↓	↑	P10–P13 interrupt polarity select register
					PCP02	1	↓	↑	
					PCP01	1	↓	↑	
	R/W				PCP00	1	↓	↑	
FF3EH	SIP13	SIP12	SIP11	SIP10	SIP13	0	Enable	Disable	P40–P43 interrupt select register
					SIP12	0	Enable	Disable	
					SIP11	0	Enable	Disable	
	R/W				SIP10	0	Enable	Disable	
FF3FH	PCP13	PCP12	PCP11	PCP10	PCP13	1	↓	↑	P40–P43 interrupt polarity select register
					PCP12	1	↓	↑	
					PCP11	1	↓	↑	
	R/W				PCP10	1	↓	↑	
FF44H	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
FF45H	0	BZSTP	BZSHT	SHTPW	0 *3	– *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FF48H	0	0	SWDIR	EDIR	0 *3	– *2			Unused
					0 *3	– *2			Unused
					SWDIR	0			Stopwatch direct input switch 0: P10=Run/Stop, P11=Lap 1: P10=Lap, P11=Run/Stop
	R		R/W		EDIR	0	Enable	Disable	Direct input enable
FF58H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R	R/W					Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P2 port function selection)
FF5AH	0	0	ESREADY	ENCS	0 *3	– *2			Unused
					0 *3	– *2			Unused
					ESREADY	0	SRDY	$\overline{SS}$	P23 port function selection: ESREADY=x, ENCS=0 → Slave (SMOD=0) P23 = I/O, Master (SMOD=1) P23 = I/O
	R		R/W		ENCS	0	SIF	I/O	Serial I/F enable (P23 function selection): ESREADY=0, ENCS=1 → Slave P23 = $\overline{SS}$, Master P23 = I/O; ESREADY=1, ENCS=1 → Slave P23 = SRDY, Master P23 = Prohibited
FF60H	RFCNT	RFOUT	ERF1	ERF0	RFCNT	0	Continue	Normal	Continuous oscillation enable
					RFOUT	0	Enable	Disable	RFOUT enable
	R/W				ERF1 ERF0	0 0			R/f conversion selection: [ERF1, 0] 0 → R/f conversion I/O; 1 → Ch.0 DC; 2 → Ch.1 AC; 3 → Ch.1 DC
FF80H	MOD16_A	EVCNT_A	FCSEL_A	PLPUL_A	MOD16_A	0	16 bits	8 bits	PTM0–1 16-bit mode selection
					EVCNT_A	0	Event ct.	Timer	PTM0 counter mode selection
					FCSEL_A	0	With NR	No NR	PTM0 function selection (for event counter mode)
	R/W				PLPUL_A	0	↑	↓	PTM0 pulse polarity selection (for event counter mode)
FF81H	PTSEL1	PTSEL0	CHSEL_A	PTOUT_A	PTSEL1	0	PWM	Normal	Programmable timer 1 PWM output selection
					PTSEL0	0	PWM	Normal	Programmable timer 0 PWM output selection
					CHSEL_A	0	Timer 1	Timer 0	PTM0–1 TOUT_A output selection
	R/W				PTOUT_A	0	On	Off	PTM0–1 TOUT_A output control
FF90H	MOD16_B	EVCNT_B	FCSEL_B	PLPUL_B	MOD16_B	0	16 bits	8 bits	PTM2–3 16-bit mode selection
					EVCNT_B	0	Event ct.	Timer	PTM2 counter mode selection
					FCSEL_B	0	With NR	No NR	PTM2 function selection (for event counter mode)
	R/W				PLPUL_B	0	↑	↓	PTM2 pulse polarity selection (for event counter mode)
FF91H	PTSEL3	PTSEL2	CHSEL_B	PTOUT_B	PTSEL3	0	PWM	Normal	Programmable timer 3 PWM output selection
					PTSEL2	0	PWM	Normal	Programmable timer 2 PWM output selection
					CHSEL_B	0	Timer 3	Timer 2	PTM2–3 TOUT_B output selection
	R/W				PTOUT_B	0	On	Off	PTM2–3 TOUT_B output control
FFA0H	MOD16_C	EVCNT_C	FCSEL_C	PLPUL_C	MOD16_C	0	16 bits	8 bits	PTM4–5 16-bit mode selection
					EVCNT_C	0	Event ct.	Timer	PTM4 counter mode selection
					FCSEL_C	0	With NR	No NR	PTM4 function selection (for event counter mode)
	R/W				PLPUL_C	0	↑	↓	PTM4 pulse polarity selection (for event counter mode)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.5.8.1(e) Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFA1H	PTSEL5	PTSEL4	CHSEL_C	PTOUT_C	PTSEL5	0	PWM	Normal	Programmable timer 5 PWM output selection
					PTSEL4	0	PWM	Normal	Programmable timer 4 PWM output selection
	R/W				CHSEL_C	0	Timer 5	Timer 4	PTM4–5 TOUT_C output selection
					PTOUT_C	0	On	Off	PTM4–5 TOUT_C output control
FFB0H	MOD16_D	EVCNT_D	FCSEL_D	PLPUL_D	MOD16_D	0	16 bits	8 bits	PTM6–7 16-bit mode selection
					EVCNT_D	0	Event ct.	Timer	PTM6 counter mode selection
	R/W				FCSEL_D	0	With NR	No NR	PTM6 function selection (for event counter mode)
					PLPUL_D	0	↑	↓	PTM6 pulse polarity selection (for event counter mode)
FFB1H	PTSEL7	PTSEL6	CHSEL_D	PTOUT_D	PTSEL7	0	PWM	Normal	Programmable timer 7 PWM output selection
					PTSEL6	0	PWM	Normal	Programmable timer 6 PWM output selection
	R/W				CHSEL_D	0	Timer 7	Timer 6	PTM6–7 TOUT_D output selection
					PTOUT_D	0	On	Off	PTM6–7 TOUT_D output control
FFEBH	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (Key input interrupt 3 <P13>)
					EIK02	0	Enable	Mask	Interrupt mask register (Key input interrupt 2 <P12>)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (Key input interrupt 1 <P11>)
					EIK00	0	Enable	Mask	Interrupt mask register (Key input interrupt 0 <P10>)
FFECH	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (Key input interrupt 7 <P43>)
					EIK12	0	Enable	Mask	Interrupt mask register (Key input interrupt 6 <P42>)
	R/W				EIK11	0	Enable	Mask	Interrupt mask register (Key input interrupt 5 <P41>)
					EIK10	0	Enable	Mask	Interrupt mask register (Key input interrupt 4 <P40>)
FFFBH	IK03	IK02	IK01	IK00	IK03	0	(R)	(R)	Interrupt factor flag (Key input interrupt 3 <P13>)
					IK02	0	Yes	No	Interrupt factor flag (Key input interrupt 2 <P12>)
	R/W				IK01	0	(W)	(W)	Interrupt factor flag (Key input interrupt 1 <P11>)
					IK00	0	Reset	Invalid	Interrupt factor flag (Key input interrupt 0 <P10>)
FFFCH	IK13	IK12	IK11	IK10	IK13	0	(R)	(R)	Interrupt factor flag (Key input interrupt 7 <P43>)
					IK12	0	Yes	No	Interrupt factor flag (Key input interrupt 6 <P42>)
	R/W				IK11	0	(W)	(W)	Interrupt factor flag (Key input interrupt 5 <P41>)
					IK10	0	Reset	Invalid	Interrupt factor flag (Key input interrupt 4 <P40>)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

(1) Selecting port functions

ESIF: Serial interface enable (P2 port function select) register (FF58H•D0)

Selects the function for P20–P23.

When "1" is written: Serial interface input/output port
When "0" is written: I/O port
Reading: Valid

When using the serial interface, write "1" to this register and when P20–P23 are used as I/O ports, write "0". The configuration of the terminals within P20–P23 that are used for the serial interface depends on master or slave mode set by the SMOD register (see Section 4.10). In slave mode, all the P20–P23 ports are set to the serial interface input/output port. In master mode, P20–P22 are set to the serial interface input/output port and P23 can be used as an I/O port. Furthermore, when the SOUT terminal is disabled (ESOUT = "0"), P21 can be used as an I/O port.
At initial reset, this register is set to "0".

ENCS: Serial interface enable (P23 port function select) register (FF5AH•D0)

Selects the function for P23.

When "1" is written: Serial interface input/output port (SRDY or $\overline{SS}$)
When "0" is written: I/O port
Reading: Valid

Set this register to "0" to use P23 as an I/O port if SRDY output or $\overline{SS}$ input is not used in slave mode.
At initial reset, this register is set to "0".

ERF1, ERF0: R/f conversion select register (FF60H•D1, D0)
Selects the function for P00–P03.
When using the R/f converter, write "01B–11B" to this register and when P00–P03 are used as I/O ports, write "00B". Furthermore, when the RFOUT terminal is disabled (RFOUT = "0"), P03 can be used as an I/O port even if the R/f converter is used.
At initial reset, this register is set to "0".

EDIR: Direct input function enable register (FF48H•D0)
Enables the direct input (RUN/LAP) function.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

The direct input function of the stopwatch timer is enabled by writing "1" to EDIR, and the P10 and P11 ports are set for the RUN/STOP and LAP key input ports. When "0" is written to EDIR, the direct input function is disabled, and P10 and P11 can be used as I/O ports.
At initial reset, this register is set to "0".

EVCNT_A: PTM0 counter mode select register (FF80H•D2)
EVCNT_B: PTM2 counter mode select register (FF90H•D2)
EVCNT_C: PTM4 counter mode select register (FFA0H•D2)
EVCNT_D: PTM6 counter mode select register (FFB0H•D2)
Selects a counter mode for programmable timer 0/2/4/6.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

When "1" is written to the EVCNT_A/B/C/D register, programmable timer 0/2/4/6 is placed into event counter mode. In this mode, P12/P41/P42/P43 is used as an external clock input port for the event counter. When "0" is written to EVCNT_A/B/C/D, P12/P41/P42/P43 can be used as an I/O port.
At initial reset, these registers are set to "0".

(2) I/O port control

P00–P03: P0 I/O port data register (FF20H)
P10–P13: P1 I/O port data register (FF24H)
P20–P23: P2 I/O port data register (FF28H)
P30–P33: P3 I/O port data register (FF2CH)
P40–P43: P4 I/O port data register (FF30H)
P50–P53: P5 I/O port data register (FF34H)
I/O port data can be read and output data can be set through these registers.

• ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is placed into output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as port data, the port terminal goes high (V_{DD}), and when "0" is written, the terminal goes low (V_{SS}).
Port data can be written also in the input mode.

• When reading data

When "1" is read: High level
When "0" is read: Low level

When the I/O port is placed into input mode, the voltage level being input to the port terminal can be read out. When the terminal voltage is high (V_{DD}), the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the read data is "0".
When the pull-down resistor option has been selected and the PULxx register is set to "1", the built-in pull-down resistor goes on during input mode, so that the I/O port terminal is pulled down.

When the I/O port is placed into output mode, the register value is read. Therefore, when using the data register of a port that is not used for signal input/output as a general-purpose register, set the port to output mode.
At initial reset, these registers are set to "1".
The data register of the port, which is set for an input/output of the serial interface or R/f converter or a special output, becomes a general-purpose register that does not affect the input/output status.

Note: When I/O ports set in input mode is changed from high to low by the pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input data, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

IOC00–IOC03: P0 port I/O control register (FF21H)
IOC10–IOC13: P1 port I/O control register (FF25H)
IOC20–IOC23: P2 port I/O control register (FF29H)
IOC30–IOC33: P3 port I/O control register (FF2DH)
IOC40–IOC43: P4 port I/O control register (FF31H)
IOC50–IOC53: P5 port I/O control register (FF35H)
Sets the I/O ports to input or output mode.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input/output mode of the I/O ports are set in 1-bit units.
Writing "1" to the I/O control register places the corresponding I/O port into output mode, and writing "0" sets input mode.
At initial reset, these registers are all set to "0", so the I/O ports are placed in input mode.

The I/O control register of the port, which is set for an input/output of the serial interface or R/f converter or a special output, becomes a general-purpose register that does not affect the input/output status.

PUL00–PUL03: P0 port pull-down control register (FF22H)
PUL10–PUL13: P1 port pull-down control register (FF26H)
PUL20–PUL23: P2 port pull-down control register (FF2AH)
PUL30–PUL33: P3 port pull-down control register (FF2EH)
PUL40–PUL43: P4 port pull-down control register (FF32H)
PUL50–PUL53: P5 port pull-down control register (FF36H)
Enables the pull-down during input mode.

When "1" is written: Pull-down On
When "0" is written: Pull-down Off
Reading: Valid

These registers enable the built-in pull-down resistor to be effective during input mode in 1-bit units. (The pull-down resistor is included into the ports selected by mask option.)
By writing "1" to the pull-down control register, the corresponding I/O ports are pulled down during input mode, while writing "0" or output mode disables the pull-down function.
At initial reset, these registers are all set to "1", so the pull-down function is enabled.

The pull-down control register of the port in which the pull-down resistor is not included becomes a general-purpose register. The register of the port that is set as output for the serial interface, input/output for the R/f converter or a special output can also be used as a general-purpose register that does not affect the pull-down control.
The pull-down control register of the port that is set as input for the serial interface functions the same as the I/O port.

SMT00–SMT03: P0 port input interface level select register (FF23H)
SMT10–SMT13: P1 port input interface level select register (FF27H)
SMT20–SMT23: P2 port input interface level select register (FF2BH)
SMT30–SMT33: P3 port input interface level select register (FF2FH)
SMT40–SMT43: P4 port input interface level select register (FF33H)
SMT50–SMT53: P5 port input interface level select register (FF37H)
Selects an input interface level.

When "1" is written: CMOS Schmitt level
When "0" is written: CMOS level
Reading: Valid

These registers select the input interface level of the I/O ports in 1-bit units.
When "1" is written to SMTxx, the corresponding I/O port Pxx is configured with a CMOS Schmitt level input interface. When "0" is written, the port is configured with a CMOS level input interface.
At initial reset, these registers are set to "1".

SIP00–SIP03: P1 port interrupt select register (FF3CH)
SIP10–SIP13: P4 port interrupt select register (FF3EH)
Selects the ports used for the key input interrupt from P10–P13 and P40–P43.

When "1" is written: Interrupt enable
When "0" is written: Interrupt disable
Reading: Valid

By writing "1" to an interrupt select register (SIP00–SIP03, SIP10–SIP13), the corresponding I/O port (P10–P13, P40–P43) is enabled to generate interrupts. When "0" is written, the I/O port does not affect the interrupt generation.
Reactivating from SLEEP status can only be done by generation of a key input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt select register (SIPxx = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction.
At initial reset, these registers are set to "0".

PCP00–PCP03: P1 port interrupt polarity select register (FF3DH)
PCP10–PCP13: P4 port interrupt polarity select register (FF3FH)
Sets the interrupt conditions.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

When "1" is written to an interrupt polarity select register (PCP00–PCP03, PCP10–PCP13), the corresponding I/O port (P10–P13, P40–P43) generates an interrupt at the falling edge of the input signal.
When "0" is written, the I/O port generates an interrupt at the rising edge of the input signal.
At initial reset, these registers are set to "1".

NRSP01, NRSP00: Key input interrupt 0–3 noise reject frequency select register (FF11H•D1, D0)
NRSP11, NRSP10: Key input interrupt 4–7 noise reject frequency select register (FF11H•D3, D2)
Selects the noise reject frequency for the key input interrupts.

Table 4.5.8.2 Setting up noise rejector

NRSP01 NRSP11	NRSP00 NRSP10	Noise reject frequency	Reject pulse width
1	1	fOSC1 / 256 (128 Hz)	7.8 msec
1	0	fOSC1 / 64 (512 Hz)	2.0 msec
0	1	fOSC1 / 16 (2 kHz)	0.5 msec
0	0	OFF (bypassed)	–

NRSP0x and NRSP1x are the noise reject frequency select registers that correspond to the key input interrupts 0–3 (P10–P13) and the key input interrupts 4–7 (P40–P43), respectively.
At initial reset, these registers are set to "00B".

EIK00–EIK03: Key input interrupt 0–3 mask register (FFEBH)
EIK10–EIK13: Key input interrupt 4–7 mask register (FFECH)
Enable/disable the key input interrupts.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

EIK0x and EIK1x are the interrupt mask registers that correspond to the key input interrupts 0–3 (P10–P13) and the key input interrupts 4–7 (P40–P43), respectively.
Setting EIKxx to "1" enables the interrupt and setting EIKxx to "0" disables the interrupt.
The SLEEP cancellation signal will be generated even if this register is set to "0". However, enable the key input interrupt using the corresponding interrupt mask register before executing the SLP instruction to execute the key input interrupt handler routine after SLEEP status is released.
At initial reset, these registers are set to "0".

IK00–IK03: Key input interrupt 0–3 factor flag (FFFBH)
IK10–IK13: Key input interrupt 4–7 factor flag (FFFCH)
These flags indicate the occurrence of key input interrupts.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IK00–IK03 and IK10–IK13 are associated with the key input interrupts 0–3 (P10–P13) and the key input interrupts 4–7 (P40–P43), respectively. From the status of these flags, the software can decide whether an key input interrupt has occurred.
The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

(3) Special output control

FOUT0–FOUT3: FOUT frequency select register (FF10H)

Selects the frequency of the FOUT signal and controls the FOUT output.

Table 4.5.8.3 FOUT clock frequency

FOUT3	FOUT2	FOUT1	FOUT0	FOUT frequency
1	1	1	1	f_{OSC3}
1	1	1	0	f_{OSC3} / 2
1	1	0	1	f_{OSC3} / 4
1	1	0	0	f_{OSC3} / 8
1	0	1	1	f_{OSC3} / 16
1	0	1	0	f_{OSC3} / 32
1	0	0	1	f_{OSC3} / 64
1	0	0	0	f_{OSC3} / 256
0	1	1	1	f_{OSC1} (32 kHz)
0	1	1	0	f_{OSC1} / 2 (16 kHz)
0	1	0	1	f_{OSC1} / 4 (8 kHz)
0	1	0	0	f_{OSC1} / 16 (2 kHz)
0	0	1	1	f_{OSC1} / 32 (1 kHz)
0	0	1	0	f_{OSC1} / 64 (512 Hz)
0	0	0	1	f_{OSC1} / 256 (128 Hz)
0	0	0	0	Off

f_{OSC1}: OSC1 oscillation frequency. ( ) indicates the clock frequency when f_{OSC1} = 32 kHz.
f_{OSC3}: OSC3 oscillation frequency

Selecting an FOUT frequency (writing 1–15 to this register) outputs the FOUT signal from the P23 terminal. Set FOUT0–FOUT3 to "0" to use P23 as a general-purpose DC input/output port.
At initial reset, these registers are set to "0".

BZE: Buzzer output control register (FF44H•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output On
When "0" is written: Buzzer output Off
Reading: Valid

When "1" is written to BZE, the BZ signal is output from the P03 terminal. When "0" is written, P03 is used as a general-purpose DC input/output port.
At initial reset, this register is set to "0".

BZSHT: One-shot buzzer trigger/status (FF45H•D1)

Controls the one-shot buzzer output.

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

Writing "1" into BZSHT causes the one-short output circuit to operate and a buzzer signal to be output from the P03 terminal. This output is automatically turned off after the time set by SHTPW has elapsed. The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

• ***When reading***

When "1" is read: BUSY
When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes off, it shifts to "0".

At initial reset, this register is set to "0".

PTOUT_A: TOUT_A output control register (FF81H•D0)
PTOUT_B: TOUT_B output control register (FF91H•D0)
PTOUT_C: TOUT_C output control register (FFA1H•D0)
PTOUT_D: TOUT_D output control register (FFB1H•D0)
Controls the TOUT_A–TOUT_D outputs.

When "1" is written: TOUT output On
When "0" is written: TOUT output Off
Reading: Valid

By writing "1" to the PTOUT_A/B/C/D register, the TOUT_A/B/C/D signal is output from the P13/P31/P32/P33 terminal. When "0" is written, the corresponding terminal is used as a general-purpose DC input/output port.
At initial reset, these registers are set to "0".

4.5.9 Programming notes

(1) When an I/O ports in input mode is changed from high to low by the pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input data, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

(2) Be sure to turn the noise rejector off before executing the SLP instruction.

(3) Reactivating from SLEEP status can only be done by generation of a key input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt select register (SIPxx = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction. Furthermore, enable the key input interrupt using the corresponding interrupt mask register (EIKxx = "1") before executing the SLP instruction to run key input interrupt handler routine after SLEEP status is released.

(4) A hazard may occur when the TOUT_A–TOUT_D and FOUT signals are turned on and off.

(5) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output. Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

(6) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(7) Before the port function is configured, the circuit that uses the port (e.g. input interrupt, multiple key entry reset, serial interface, event counter input, direct RUN/LAP input for stopwatch) must be disabled.

4.6 LCD Driver

4.6.1 Configuration of LCD driver

The S1C63632 has a built-in dot matrix LCD driver that can drive an LCD panel with a maximum of 1,536 dots (48 segments × 32 commons). Figures 4.6.1.1 to 4.6.1.3 show the configuration of the LCD driver and the drive power supply.

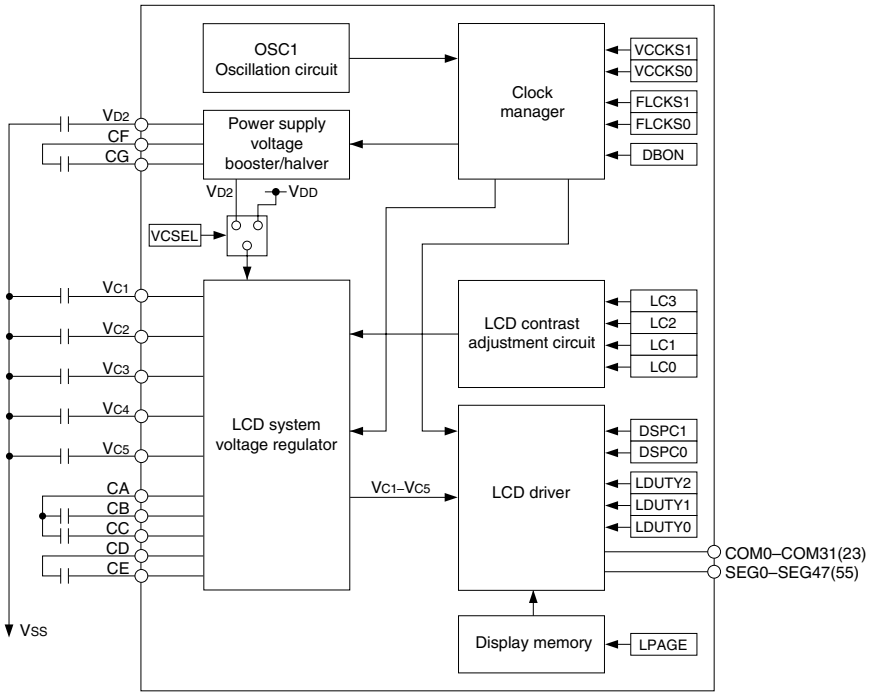


Fig. 4.6.1.1 Configuration of LCD driver and drive power supply (V_{C2} reference, 1/5 bias)

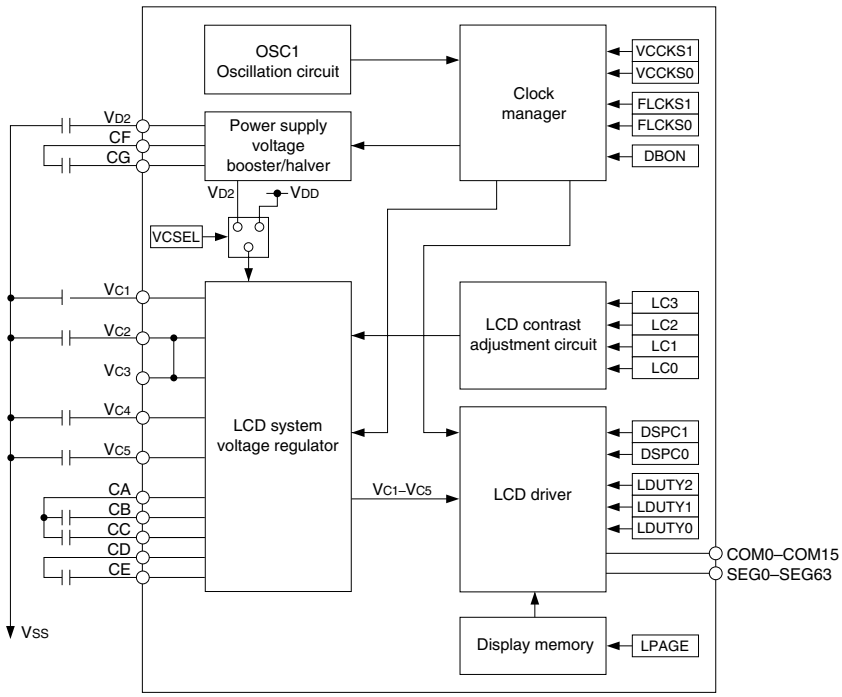


Fig. 4.6.1.2 Configuration of LCD driver and drive power supply (V_{C2} reference, 1/4 bias)

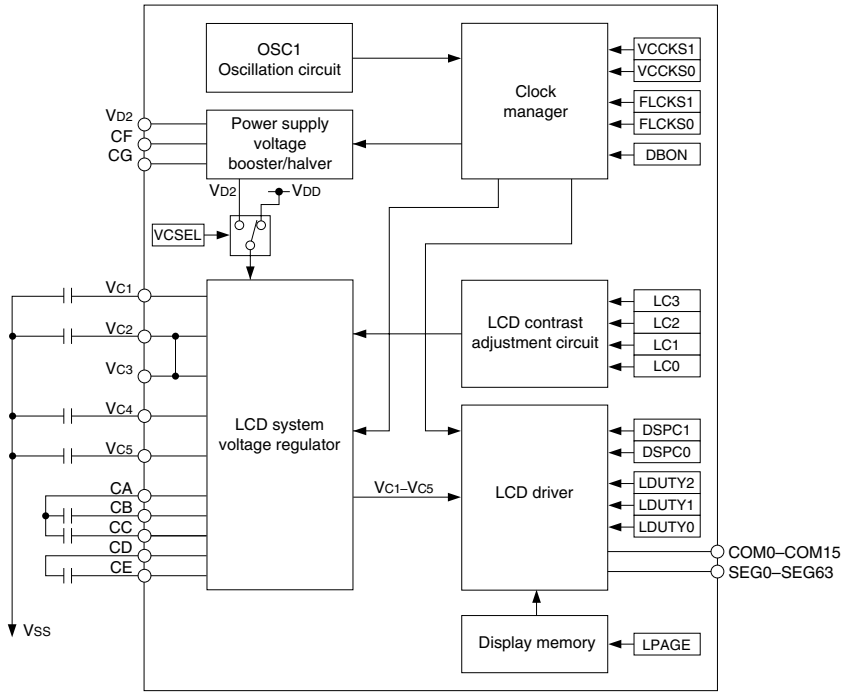


Fig. 4.6.1.3 Configuration of LCD driver and drive power supply (V_{C1} reference, 1/4 bias)

4.6.2 Power supply for LCD driving

(1) Mask option

The S1C63632 provides three options to configure the internal LCD power supply for generating the LCD drive voltages V_{C1}–V_{C5}.

TYPE 1 V_{C2} reference, 1/5 bias
V_{DD} = 1.6 to 2.5 V (power supply voltage booster/halver is used)
V_{DD} = 2.5 to 5.5 V (power supply voltage booster/halver is not used)

TYPE 2 V_{C2} reference, 1/4 bias
V_{DD} = 1.6 to 2.5 V (power supply voltage booster/halver is used)
V_{DD} = 2.5 to 5.5 V (power supply voltage booster/halver is not used)

TYPE 3 V_{C1} reference, 1/4 bias
V_{DD} = 1.6 to 5.5 V (power supply voltage booster/halver is not used)

Select one from three types according to the supply voltage and the LCD panel characteristics.

The LCD drive voltages are generated by boosting/halving the V_{C1} or V_{C2} reference voltage output from the voltage regulator.
Table 4.6.2.1 lists the V_{C1}, V_{C2}, V_{C3}, V_{C4} and V_{C5} voltage values and boosting/halving status. Note that the number of externally attached parts differs according to the selected bias (1/5 or 1/4). (See Figures 4.6.1.1 to 4.6.1.3.)

Table 4.6.2.1 LCD drive voltage

LCD drive voltage	TYPE 1	[V]	TYPE 2	[V]	TYPE 3	[V]
V_{C1}	$V_{C2} \times 0.5$	1.10	$V_{C2} \times 0.5$	1.13	V_{C1} (reference)	1.13
V_{C2}	V_{C2} (reference)	2.20	V_{C2} (reference)	2.25	$V_{C1} \times 2$	2.25
V_{C3}	$V_{C2} \times 1.5$	3.30	= V_{C2}	2.25	= V_{C2}	2.25
V_{C4}	$V_{C2} \times 2$	4.40	$V_{C2} \times 1.5$	3.38	$V_{C1} \times 3$	3.38
V_{C5}	$V_{C2} \times 2.5$	5.50	$V_{C2} \times 2$	4.50	$V_{C1} \times 4$	4.50

Note: Each LCD drive voltage varies depending on the contrast adjustment register (LCx) setting.

(2) Controlling the LCD system voltage regulator

To start LCD display, turn the LCD system voltage regulator on using the LPWR register. When "1" is written to LPWR, the LCD system voltage regulator goes on and generates the LCD drive voltages listed in Table 4.6.2.1. At initial reset, LPWR is set to "0" (Off).
When LCD display is not necessary, turn the LCD system voltage regulator off to reduce power consumption.

To generate stable LCD drive voltages, the LCD system voltage regulator must be driven with a source voltage higher than the reference voltage V_{C2} or V_{C1}. When a V_{C2} reference voltage option (TYPE 1 or TYPE 2) is selected, the LCD system voltage regulator can be driven with the V_{D2} voltage generated by the power supply voltage booster/halver (boost mode) if the supply voltage V_{DD} is less than 2.5 V. The V_{D2} voltage is generated by approximately doubling the V_{DD} voltage. Use the VCSEL register to select V_{DD} or V_{D2} to drive the LCD system voltage regulator. V_{DD} is selected when VCSEL is "0" and V_{D2} is selected when VCSEL is "1". When using V_{D2}, the power supply voltage booster/halver must be turned on by writing "1" to the DBON register before switching to V_{D2}.
When the V_{C1} reference voltage option (TYPE 3) is selected, this control is not required. In this case, VCSEL and DBON should be set to "0".

Furthermore, the LCD system voltage regulator uses the boost clock supplied from the clock manager for boosting/halving the voltage. The clock supply is controlled by the VCCKS0–VCCKS1 register. Set VCCKS to "01B" before writing "1" to LPWR. When LCD display is not necessary, stop the clock supply by setting VCCKS to "00B" to reduce power consumption.

Table 4.6.2.2 Controlling boost clock

VCCKS1	VCCKS0	Boost clock control
1	*	Prohibited
0	1	On (2 kHz)
0	0	Off

Note: The oscillation circuit stops oscillating in SLEEP mode set by the SLP instruction of the CPU. Therefore, the power supply voltage booster/halver cannot generate V_{D2} in SLEEP mode. Before executing the SLP instruction, configure the LCD system voltage regulator (VCSEL="0", DBON="0") so that it will be driven with V_{DD}.

(3) Heavy load protection mode for LCD system voltage regulator

The LCD system voltage regulator has a heavy load protection function that can be activated with software to stabilize display on the LCD as much as possible (to minimize degradation in display quality) even if fluctuations in the supply voltage occur due to driving an external load. By writing "1" to the VCHLMOD register, the LCD system voltage regulator enters heavy load protection mode to stabilize the V_{C1} to V_{C5} outputs. Use the heavy load protection function if the LCD display has inconsistencies in density when a heavy load such as a lamp or buzzer is driven with a port output. At initial reset, VCHLMOD is set to "0" (Off).

Note: The heavy load protection mode increases current consumption compared with normal operation mode. Therefore, do not set heavy load protection mode unless it is necessary.

4.6.3 Controlling LCD display

(1) Selecting display mode

In addition to the LPWR register for turning the display on and off, the DSPC0–DSPC1 register is provided to select a display mode. There are four display modes available as shown in Table 4.6.3.1.

Table 4.6.3.1 Display mode

DSPC1	DSPC0	Display mode
1	1	All white mode
1	0	All black mode
0	1	Reverse mode
0	0	Normal mode

Normal mode: The screen image written in the display RAM is output without being processed. (default)

Reverse mode: The screen image written in the display RAM is output in reverse video. The contents in the display RAM are not modified.

All black mode: Turns all the LCD pixels on (black when normal white LCD is used) in static drive. The contents in the display RAM are not modified.

All white mode: Turns all the LCD pixels off (white when normal white LCD is used) in dynamic drive. The contents in the display RAM are not modified.

(2) Drive duty and frame frequency

The S1C63632 supports three types of LCD drive duty settings, 1/32, 1/24 and 1/16, and can be switched using the LDUTY2–LDUTY0 register as shown in Table 4.6.3.2. Select an appropriate drive duty according to the LCD panel to be used.

The frame frequency is determined by the selected duty and the clock supplied from the clock manager. The clock to be supplied (8 Hz to 32 Hz) can be selected using the FLCKS0–FLCKS1 register. Selecting a low frame frequency can reduce current consumption.

Note: The frame frequency affects the display quality, therefore, it should be determined after the display quality is evaluated using the actual LCD panel.

Table 4.6.3.2 Combination of frame frequency and duty

LDUTY2	LDUTY1	LDUTY0	Duty	Frame frequency				Drive bias (mask option)
				FLCKS = 11B	FLCKS = 10B	FLCKS = 01B	FLCKS = 00B	
1	1	1	Prohibited	–	–	–	–	–
1	1	0	Prohibited	–	–	–	–	–
1	0	1	Prohibited	–	–	–	–	–
1	0	0	1/16	8 Hz	16 Hz	21.333 Hz	32 Hz	1/4 bias
0	1	1	1/24	5.333 Hz	10.666 Hz	14.22 Hz	21.333 Hz	1/5 bias
0	1	0	1/24	10.666 Hz	21.333 Hz	28.44 Hz	42.666 Hz	1/5 bias
0	0	1	Prohibited	–	–	–	–	–
0	0	0	1/32	8 Hz	16 Hz	21.333 Hz	32 Hz	1/5 bias

Table 4.6.3.3 shows the relationship of the drive duty setting, available SEG/COM terminals and the maximum number of pixels.

Table 4.6.3.3 Drive duty setting, SEG/COM terminals and the maximum number of pixels

Terminal / Duty	SEG0–SEG47	COM31–COM24	COM23–COM16	COM15–COM0	Number of pixels
1/32	SEG0–SEG47	COM31–COM24	COM23–COM16	COM15–COM0	1,536
1/24	SEG0–SEG47	SEG48–SEG55	COM23–COM16	COM15–COM0	1,344
1/16	SEG0–SEG47	SEG48–SEG55	SEG56–SEG63	COM15–COM0	1,024

The respective drive waveforms are shown in Figures 4.6.3.1 to 4.6.3.3.

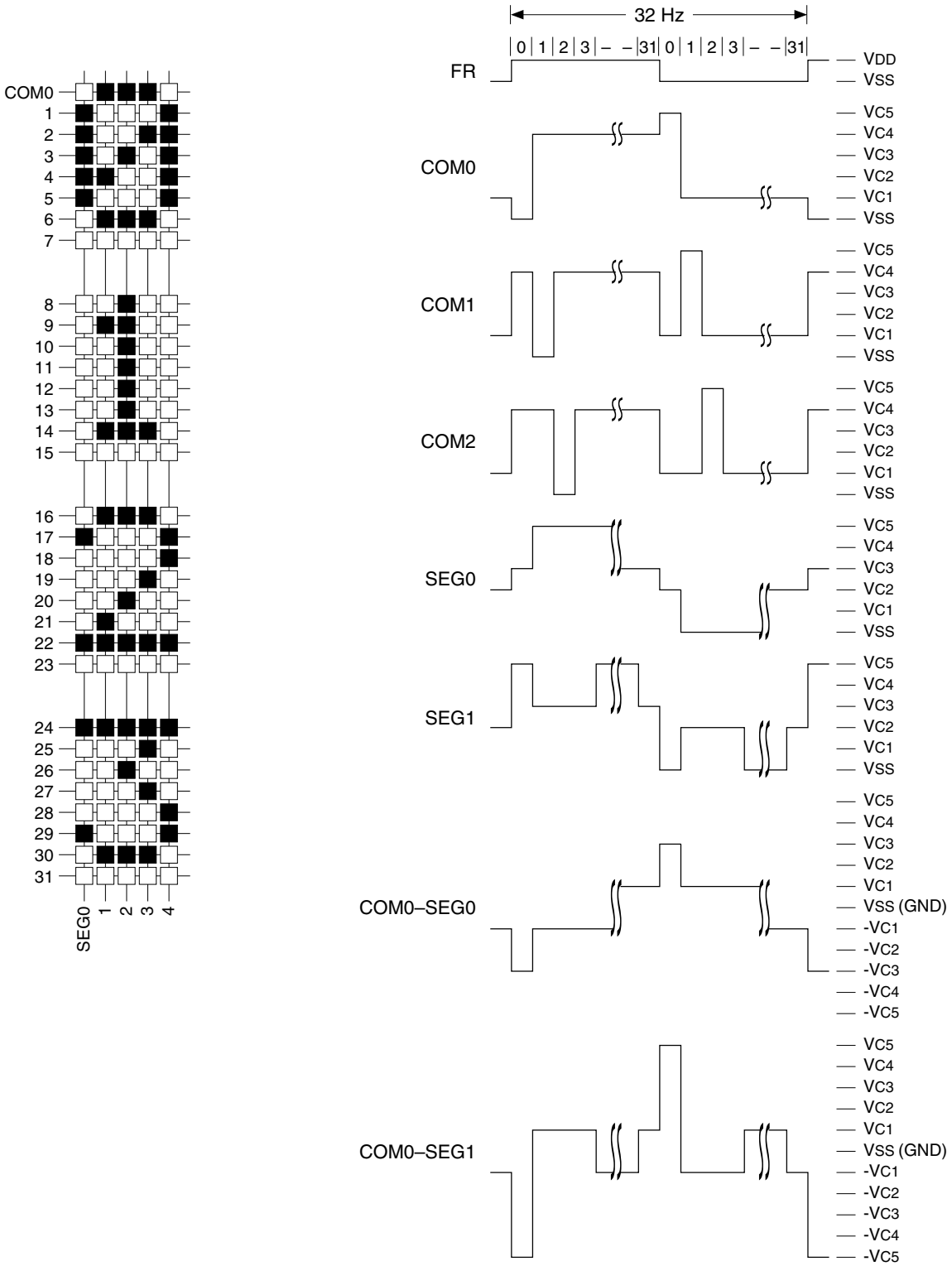


Fig. 4.6.3.1 Drive waveform for 1/32 duty (FLCKS = "00B")

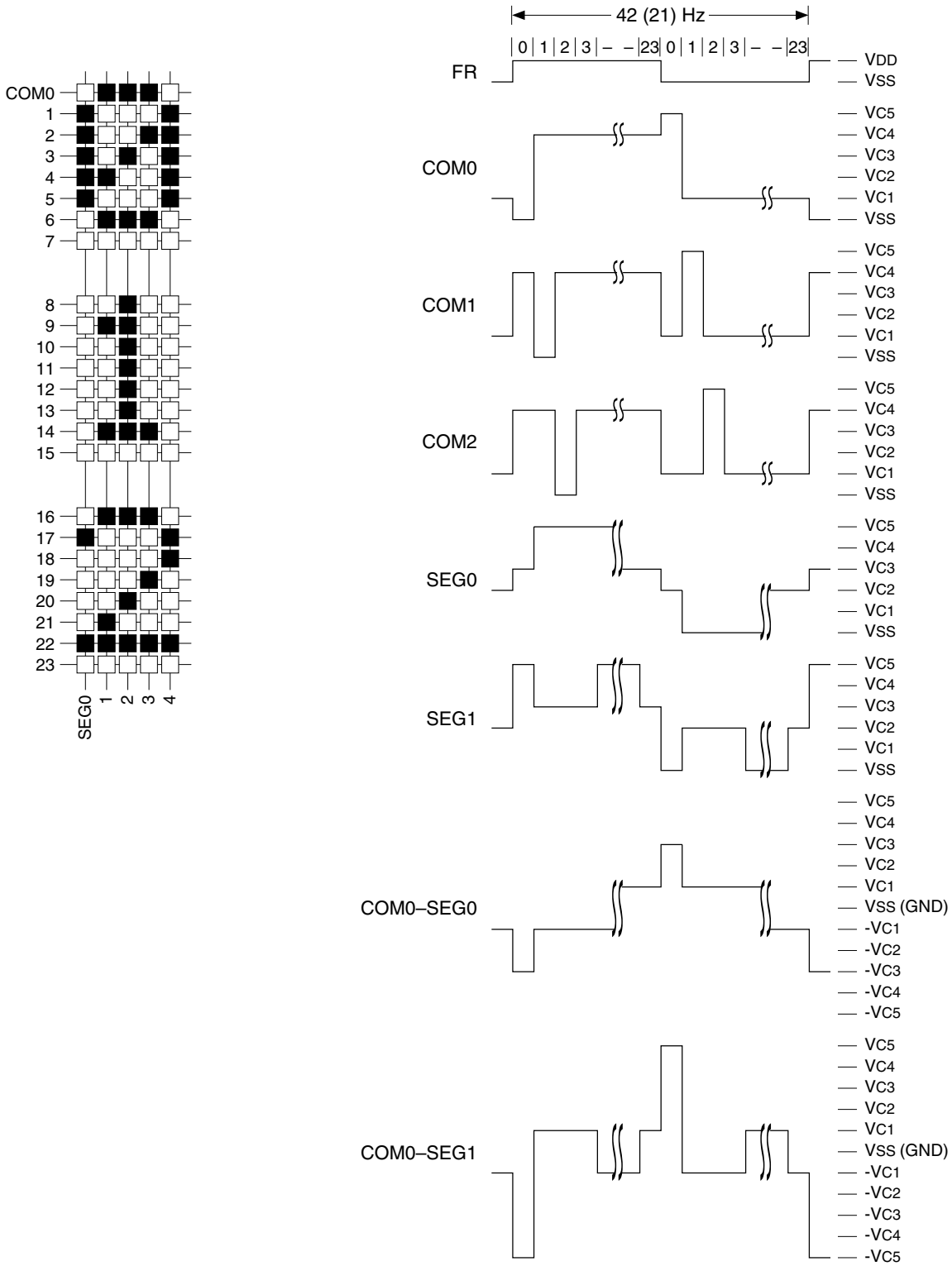


Fig. 4.6.3.2 Drive waveform for 1/24 duty (FLCKS = "00B")

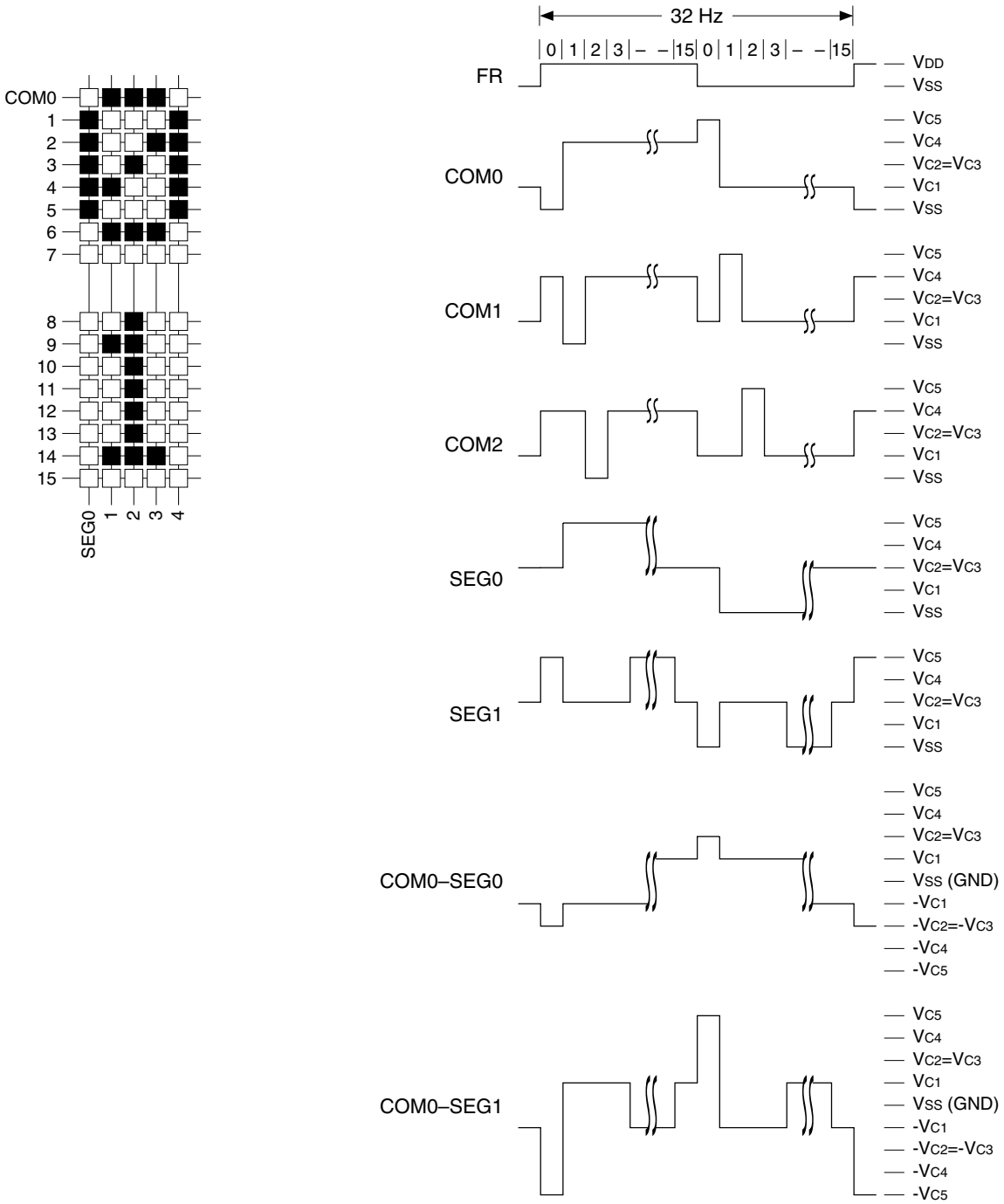


Fig. 4.6.3.3 Drive waveform for 1/16 duty (FLCKS = "00B")

4.6.4 Display memory

The display memory is allocated to F000H–F37FH in the data memory area and the addresses and the data bits correspond to COM and SEG outputs as shown in Figures 4.6.4.1 to 4.6.4.3.

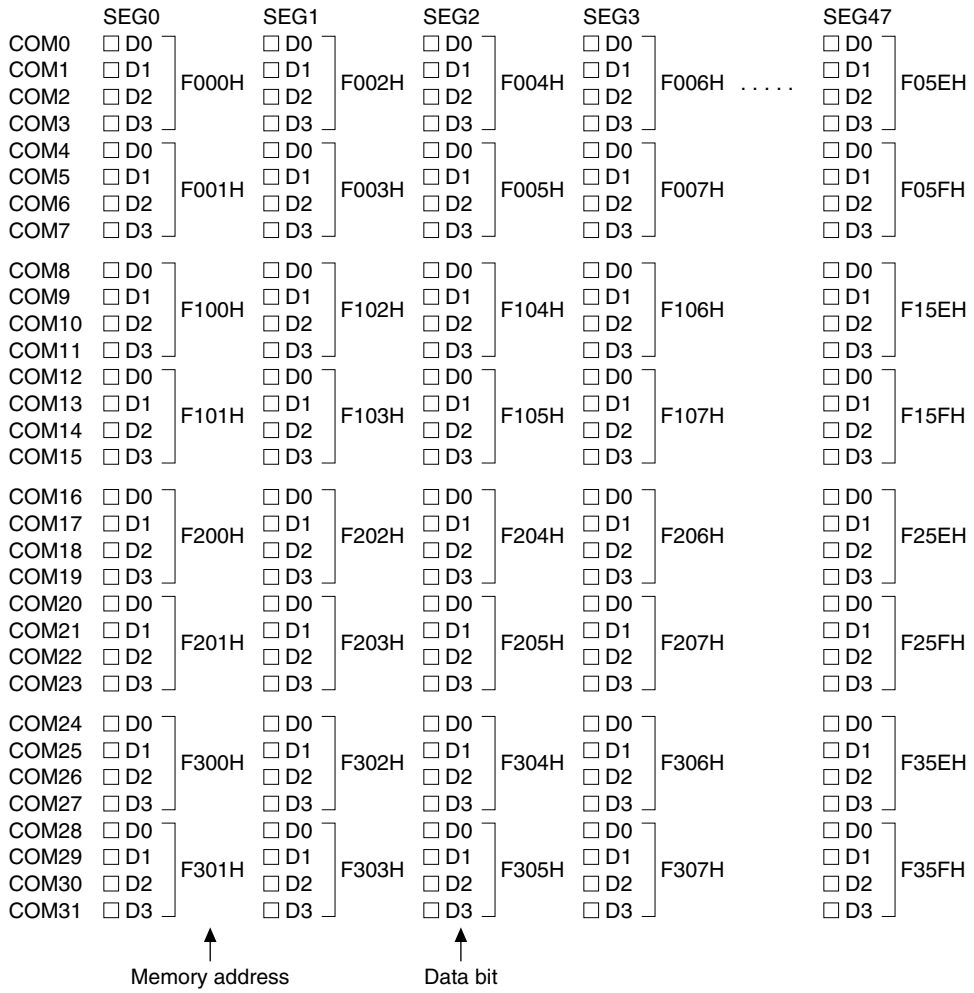


Fig. 4.6.4.1 Correspondence between display memory and LCD dot matrix (1/32 duty)

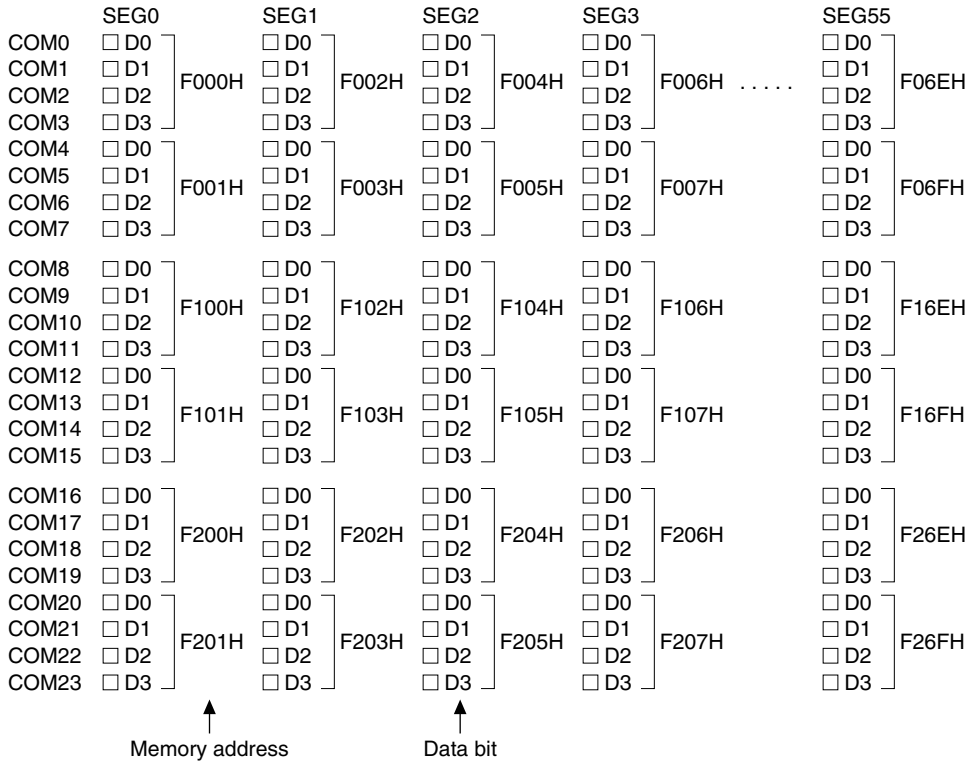


Fig. 4.6.4.2 Correspondence between display memory and LCD dot matrix (1/24 duty)

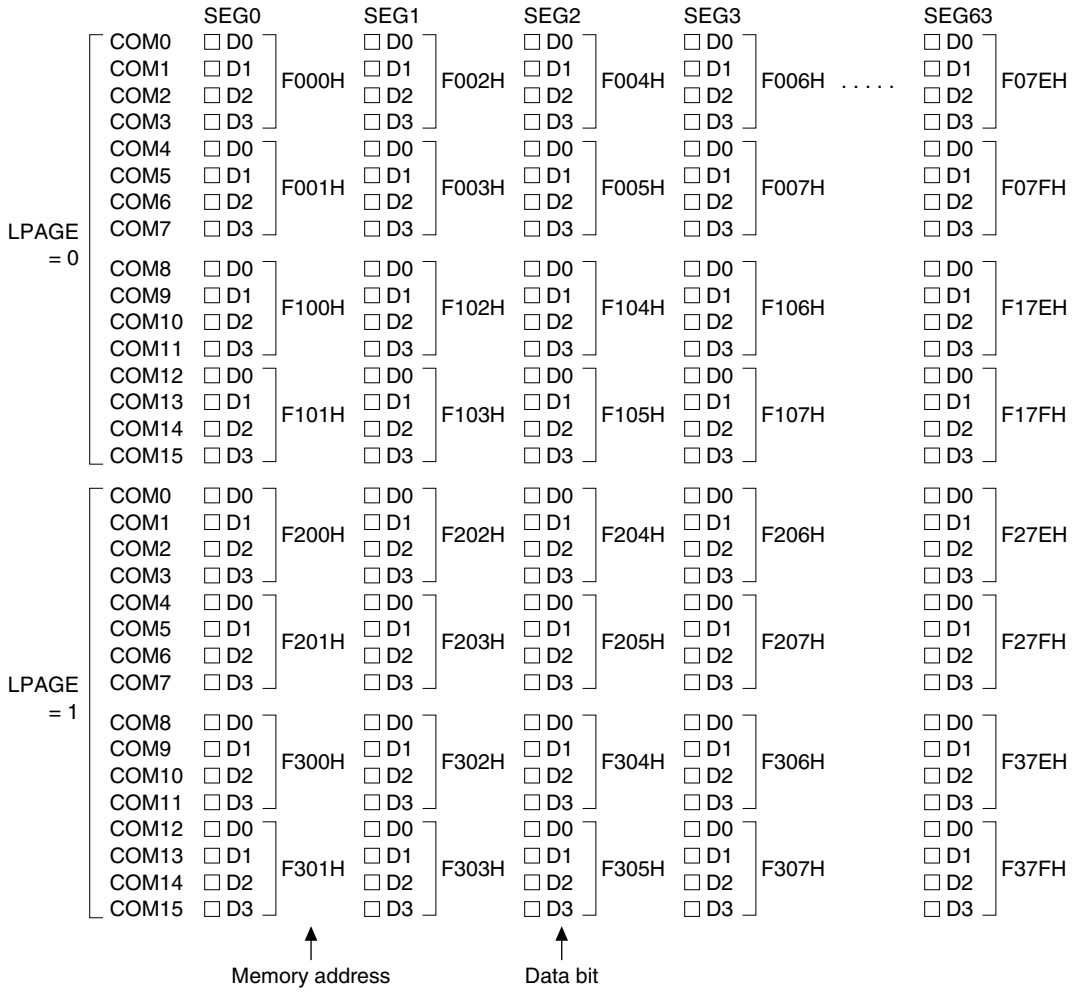


Fig. 4.6.4.3 Correspondence between display memory and LCD dot matrix (1/16 duty)

When a bit in the display memory is set to "1", the corresponding LCD pixel goes on, and when it is set to "0", the pixel goes off.

When 1/16 duty is selected, the display memory area can be used for two screen images. Select either F000H–F17FH or F200H–F37FH for the area to be displayed using the LPAGE register. This allows the software to switch the screen in an instant.

At initial reset, the data memory contents become undefined hence, there is need to initialize using the software. The display memory has read/write capability, and the addresses that have not been used for LCD display can be used as general purpose registers.

Note: When a program that access no memory implemented area (F080H–F0FFH, F180H–F1FFH, F280H–F2FFH, F380H–F3FFH) is made, the operation is not guaranteed.

4.6.5 LCD contrast adjustment

The LCD driver allows the software to adjust the LCD contrast.
It is realized by controlling the voltages V_{C1}–V_{C5} output from the LCD system voltage regulator. The contrast can be adjusted to 16 levels using the LC3–LC0 register.

Table 4.6.5.1 LCD contrast

No.	LC3	LC2	LC1	LC0	Contrast
0	0	0	0	0	Light
1	0	0	0	1	↑
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	↓
15	1	1	1	1	Dark

At initial reset, the LC3–LC0 register is set to 0000B. The software should initialize the register to get the desired contrast.

4.6.6 I/O memory of LCD driver

Table 4.6.6.1 shows the I/O addresses and the control bits for the LCD driver. Figure 4.6.6.1 shows the display memory map.

Table 4.6.6.1 Control bits of LCD driver

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF02H	VDSEL	VCSEL	HLON	DBON	VDSEL	0	1	0	General-purpose register
					VCSEL	0	V_{D2}	V_{DD}	Power source select for LCD system voltage regulator
	R/W				HLON	0	On	Off	Power voltage booster/halver halving mode On/Off
					DBON	0	On	Off	Power voltage booster/halver boost mode On/Off
FF03H	VCHLMOD	VDHLMOD	General	LPWR	VCHLMOD	0	On	Off	Heavy load protection mode On/Off for LCD system voltage regulator
					VDHLMOD	0	On	Off	Heavy load protection mode On/Off for internal voltage regulator
	R/W				General	0	1	0	General-purpose register
					LPWR	0	On	Off	LCD system voltage regulator On/Off
FF12H	FLCKS1	FLCKS0	VCCKS1	VCCKS0	FLCKS1	0			Frame frequency selection: [FLCKS1, 0] 0: 32 Hz; 1: 24 Hz; 2: 16 Hz; 3: 8 Hz
					FLCKS0	0			
	R/W				VCCKS1	0			VC boost frequency selection: [VCCKS1, 0] 0: Off; 1: 2 kHz; 2, 3: Prohibited
					VCCKS0	0			
FF50H	General	LPAGE	DSPC1	DSPC0	General	0	1	0	General-purpose register
					LPAGE	0	F200-F37F	F000-F17F	Display memory area (when 1/16 duty is selected); functions as a general-purpose register when 1/24 or 1/32 is selected
	R/W				DSPC1	0			LCD display mode selection: [DSPC1, 0] 0: Normal; 1: Reverse; 2: All lit; 3: All off
					DSPC0	0			
FF51H	General	LDUTY2	LDUTY1	LDUTY0	General	0	1	0	General-purpose register
					LDUTY2	0			LCD drive duty selection: [LDUTY2—0] 0: 1/32 (32 Hz); 1: Prohibited; 2: 1/24 (42 Hz); 3: 1/24 (21 Hz); 4: 1/16 (32 Hz); 5—7: Prohibited
	R/W				LDUTY1	0			
					LDUTY0	0			
FF52H	LC3	LC2	LC1	LC0	LC3	0			LCD contrast adjustment: [LC3—0] 0: Light — 15: Dark
					LC2	0			
	R/W				LC1	0			
					LC0	0			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

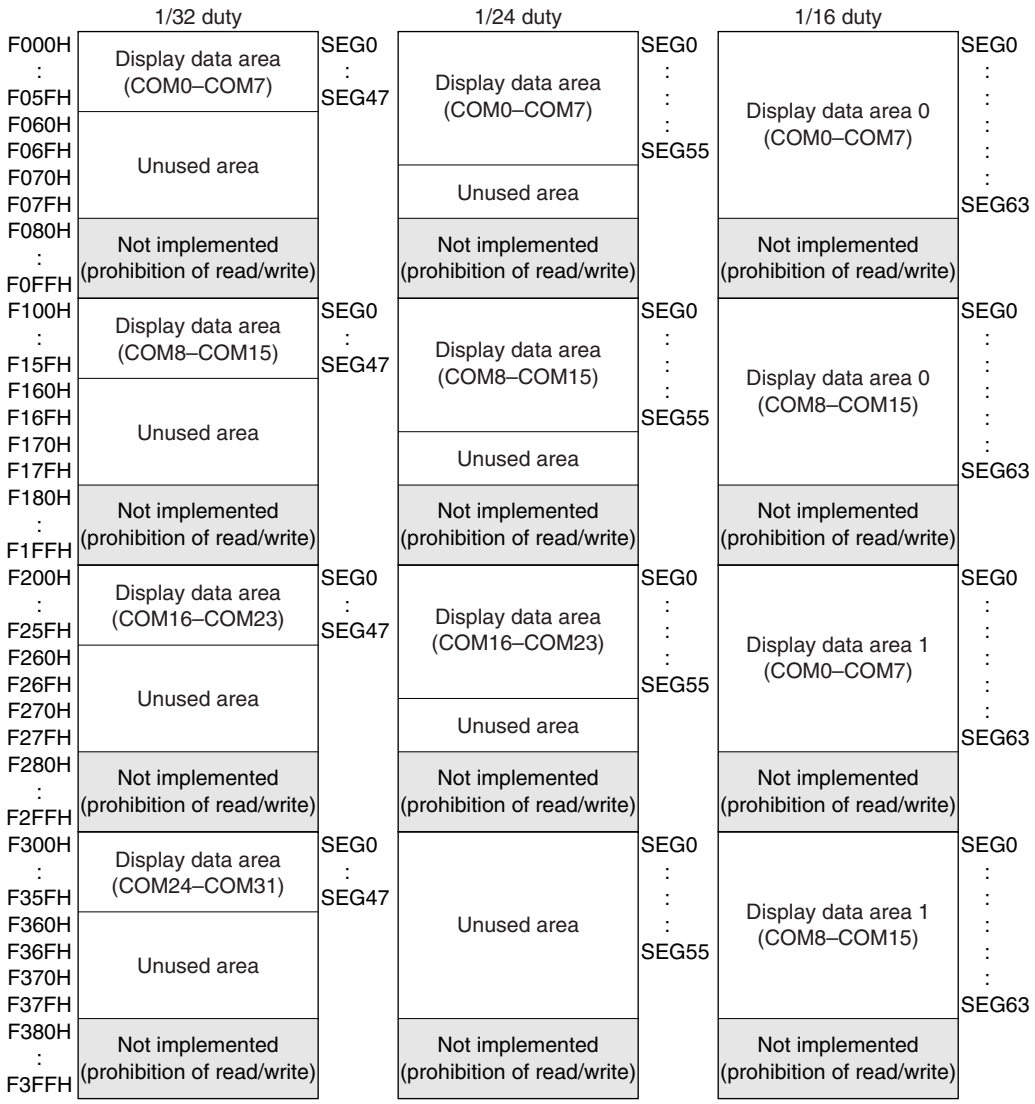


Fig. 4.6.6.1 Display memory map

DBON: Power supply voltage booster/halver boost mode On/Off register (FF02H•D0)
Activates the power supply voltage booster/halver in boost mode.

When "1" is written: Booster On
When "0" is written: Booster Off
Reading: Valid

When "1" is written to DBON, the power supply voltage booster/halver activates in boost mode and almost doubles the V_{DD} voltage to generate the V_{D2} voltage. Turn the power supply voltage booster/halver on when driving the LCD system voltage regulator with V_{D2} (V_{C2} reference voltage, V_{DD} = 1.6 to 2.5 V). When "0" is written to DBON, the voltage boost operation is deactivated. Be sure to set DBON to "0" (Off) when driving the LCD system voltage regulator with V_{DD}. Furthermore, do not set both DBON and HLON to "1".
At initial reset, this register is set to "0".

VCSEL: LCD system voltage regulator power source switch register (FF02H•D2)
Selects the power voltage for the LCD system voltage regulator.

When "1" is written: V_{D2}
When "0" is written: V_{DD}
Reading: Valid

When "1" is written to VCSEL, the LCD system voltage regulator is driven with V_{D2} generated by the power supply voltage booster/halver. Before this setting is made, it is necessary to write "1" to DBON to activate the power supply voltage booster (boost mode). Furthermore, do not switch the power voltage to V_{D2} for at least 1 msec after the power supply voltage booster/halver is turned on to allow V_{D2} to stabilize. When "0" is written to VCSEL, the LCD system voltage regulator is driven with V_{DD}.
At initial reset, this register is set to "0".

Note: Do not set DBON to "1" (boost mode) and VCSEL to "1" (driving with V_{D2}) if the supply voltage V_{DD} exceeds 2.5 V, as it may cause damage of the IC.

LPWR: LCD system voltage regulator On/Off register (FF03H•D0)
Turns the LCD system voltage regulator on and off.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to LPWR, the LCD system voltage regulator goes on and generates the LCD drive voltages. When "0" is written, all the LCD drive voltages go to V_{SS} level.
It takes about 100 msec for the LCD drive voltages to stabilize after starting up the LCD system voltage regulator by writing "1" to LPWR.
At initial reset, this register is set to "0".

VCHLMOD: LCD system voltage regulator heavy load protection On/Off register (FF03H•D3)
Enables heavy load protection function for the LCD system voltage regulator.

When "1" is written: On
When "0" is written: Off
Reading: Valid

By writing "1" to VCHLMOD, the LCD system voltage regulator enters heavy load protection mode to minimize degradation in display quality when fluctuations in the supply voltage occurs due to driving a heavy load. The heavy load protection function is effective when the OSC3 clock is used or the buzzer/FOUT signal is being output. However, heavy load protection mode increases current consumption compared with normal operation mode. Therefore, do not set heavy load protection mode unless it is necessary.
At initial reset, this register is set to "0".

VCCKS0, VCCKS1: VC boost frequency select register (FF12H•D0, D1)

Controls the boost clock supply to the LCD system voltage regulator.

Table 4.6.6.2 Controlling boost clock

VCCKS1	VCCKS0	Boost clock control
1	*	Prohibited
0	1	On (2 kHz)
0	0	Off

The LCD system voltage regulator uses the boost clock supplied from the clock manager for boosting/reducing the voltage. Use this register to control the clock supply. Set VCCKS to "01B" before writing "1" to LPWR. When LCD display is not necessary, stop the clock supply by setting VCCKS to "00B" to reduce power consumption.
At initial reset, this register is set to "00B".

FLCKS0, FLCKS1: Frame frequency select register (FF12H•D2, D3)

Selects the frequency of the frame clock supplied from the clock manager.

Table 4.6.6.3 Selecting frame frequency

FLCKS1	FLCKS0	Frame frequency
1	1	8 Hz
1	0	16 Hz
0	1	24 Hz
0	0	32 Hz

(When f_{OSC1} = 32.768 Hz)

See Table 4.6.6.5 for the frame frequency when 1/24 duty is selected by the LDUTY0–LDUTY2 register.
At initial reset, this register is set to "00B".

DSPC0, DSPC1: Display mode select register (FF50H•D0, D1)

Sets the display mode.

Table 4.6.6.4 Display mode

DSPC1	DSPC0	Display mode
1	1	All white mode
1	0	All black mode
0	1	Reverse mode
0	0	Normal mode

In normal mode, the screen image written in the display RAM is output without being processed.
In reverse mode, the screen image written in the display RAM is output in reverse video.
All black mode turns all the LCD pixels on (black when normal white LCD is used) in static drive.
All white mode turns all the LCD pixels off (white when normal white LCD is used) in dynamic drive.
The contents in the display RAM are not modified by setting this register.
At initial reset, this register is set to "00B".

LPAGE: LCD display memory area select register (FF50H•D2)

Selects the display memory area at 1/16 duty drive.

When "1" is written: F200H–F37FH
When "0" is written: F000H–F17FH
Reading: Valid

By writing "1" to the LPAGE register, the data set in F200H–F37FH (the second half of the display memory) is displayed, and when "0" is written, the data set in F000H–F17FH (the first half of the display memory) is displayed.
This function is valid only when 1/16 duty is selected, and when 1/24 or 1/32 duty is selected, this register can be used as a general purpose register.
At initial reset, this register is set to "0".

LDUTY0–LDUTY2: LCD drive duty switching register (FF51H•D0–D2)

Selects the LCD drive duty.

Table 4.6.6.5 Drive duty setting

LDUTY2	LDUTY1	LDUTY0	Duty	Frame frequency				Drive bias (mask option)
				FLCKS = 11B	FLCKS = 10B	FLCKS = 01B	FLCKS = 00B	
1	1	1	Prohibited	–	–	–	–	–
1	1	0	Prohibited	–	–	–	–	–
1	0	1	Prohibited	–	–	–	–	–
1	0	0	1/16	8 Hz	16 Hz	21.333 Hz	32 Hz	1/4 bias
0	1	1	1/24	5.333 Hz	10.666 Hz	14.22 Hz	21.333 Hz	1/5 bias
0	1	0	1/24	10.666 Hz	21.333 Hz	28.44 Hz	42.666 Hz	1/5 bias
0	0	1	Prohibited	–	–	–	–	–
0	0	0	1/32	8 Hz	16 Hz	21.333 Hz	32 Hz	1/5 bias

At initial reset, this register is set to "000B".

LC3–LC0: LCD contrast adjustment register (FF52H)

Adjusts the LCD contrast.

Table 4.6.6.6 LCD contrast

No.	LC3	LC2	LC1	LC0	Contrast
0	0	0	0	0	Light
1	0	0	0	1	↑
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	↓
15	1	1	1	1	Dark

Setting this register changes the V_{C1}–V_{C5} LCD drive voltages.
At initial reset, this register is set to "0000B".

4.6.7 Programming notes

(1) When a program that access no memory implemented area (F080H–F0FFH, F180H–F1FFH, F280H–F2FFH, F380H–F3FFH) is made, the operation is not guaranteed.

(2) When driving the LCD system voltage regulator with V_{D2}, wait at least 1 msec for stabilization of the voltage before switching the power voltage for the LCD system voltage regulator to V_{D2} using VCSEL after the power supply voltage booster/halver is turned on.

4.7 Clock Timer

4.7.1 Configuration of clock timer

The S1C63632 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of an 8-bit binary counter that serves as the input clock, fOSC1 divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.7.1.1 is the block diagram for the clock timer.

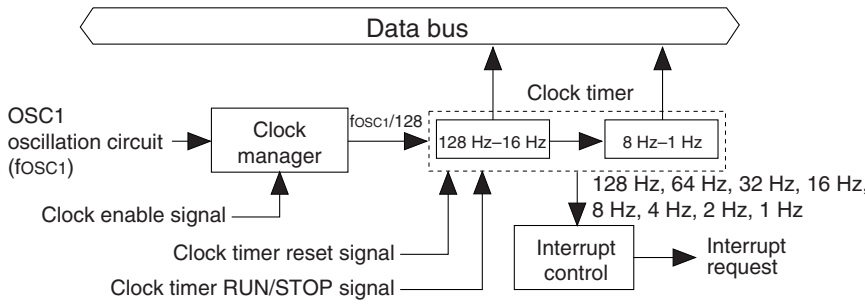


Fig. 4.7.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

4.7.2 Controlling clock manager

The clock manager generates the clock timer operating clock by dividing the OSC1 clock by 128. Before the clock timer can be run, write "1" to the RTCKE register to supply the operating clock to the clock timer.

Table 4.7.2.1 Controlling clock timer operating clock

RTCKE	Clock timer operating clock
1	fOSC1 / 128 (256 Hz)
0	Off

If it is not necessary to run the clock timer, stop the clock supply by setting RTCKE to "0" to reduce current consumption.

4.7.3 Data reading and hold function

The 8 bits timer data are allocated to the address FF41H and FF42H.

<FF41H>	D0: TM0 = 128 Hz	D1: TM1 = 64 Hz	D2: TM2 = 32 Hz	D3: TM3 = 16 Hz
<FF42H>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

Since two addresses are allocated for the clock timer data, a carry is generated from the low-order data (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz) during counting. If this carry is generated between readings of the low-order data and the high-order data, the combined data does not represent the correct value (if a carry occurs after the low-order data is read as FFH, the incremented (+1) value is read as the high-order data). To avoid this problem, the clock timer is designed to latch the high-order data at the time the low-order data is read. The latched high-order data will be maintained until the next reading of the low-order data.

Note: The latched value, not the current value, is always read as the high-order data. Therefore, be sure to read the low-order data first.

4.7.4 Interrupt function

The clock timer can generate an interrupt at the falling edge of 128 Hz, 64 Hz, 32 Hz, 16 Hz, 8 Hz, 4 Hz, 2 Hz and 1 Hz signals. Software can enable or mask any of these frequencies to generate interrupts.
Figure 4.7.4.1 is the timing chart of the clock timer.

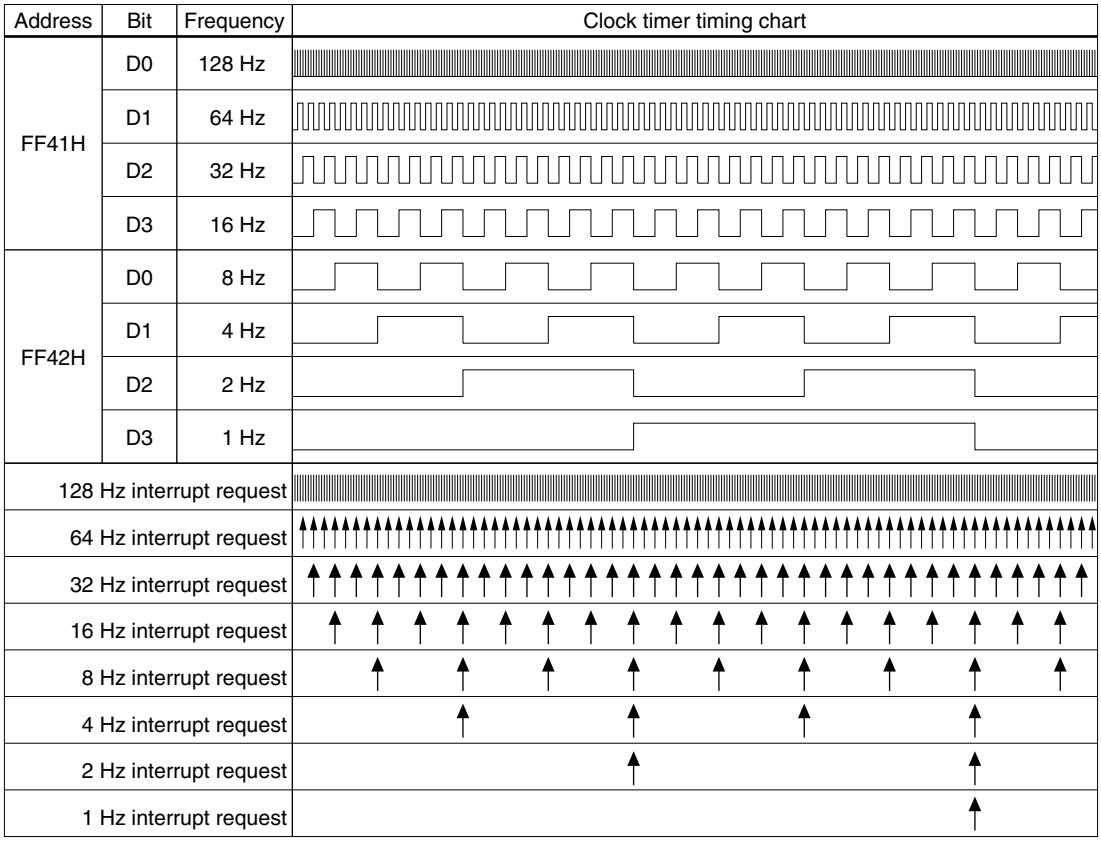


Fig. 4.7.4.1 Timing chart of clock timer

As shown in Figure 4.7.4.1, an interrupt is generated at the falling edge of each frequency signal (128 Hz, 64 Hz, 32 Hz, 16 Hz, 8 Hz, 4 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3, IT4, IT5, IT6, IT7) is set to "1". The interrupt mask registers (EIT0, EIT1, EIT2, EIT3, EIT4, EIT5, EIT6, EIT7) are used to enable or mask each interrupt factor. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.7.5 I/O memory of clock timer

Table 4.7.5.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.7.5.1 Control bits of clock timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF16H	MDCKE	SGCKE	SWCKE	RTCKE	MDCKE	0	Enable	Disable	Integer multiplier clock enable
					SGCKE	0	Enable	Disable	Sound generator clock enable
	R/W				SWCKE	0	Enable	Disable	Stopwatch timer clock enable
					RTCKE	0	Enable	Disable	Clock timer clock enable
FF40H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF41H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF42H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFEEH	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 64 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 128 Hz)
FFEFH	EIT7	EIT6	EIT5	EIT4	EIT7	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT6	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT5	0	Enable	Mask	Interrupt mask register (Clock timer 4 Hz)
					EIT4	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
FFFEH	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 16 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 64 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 128 Hz)
FFFFH	IT7	IT6	IT5	IT4	IT7	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT6	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT5	0	(W)	(W)	Interrupt factor flag (Clock timer 4 Hz)
					IT4	0	Reset	Invalid	Interrupt factor flag (Clock timer 8 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

RTCKE: Clock timer clock enable register (FF16H•D0)

Controls the operating clock supply to the clock timer.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to RTCKE, the clock timer operating clock is supplied from the clock manager. If it is not necessary to run the clock timer, stop the clock supply by setting RTCKE to "0" to reduce current consumption.
At initial reset, this register is set to "0".

TMRUN: Clock timer Run/Stop control register (FF40H•D0)

Controls run/stop of the clock timer.

When "1" is written: Run
When "0" is written: Stop
Reading: Valid

The clock timer starts running when "1" is written to the TMRUN register, and stops when "0" is written. In stop status, the timer data is maintained until the next run status or the timer is reset. Also, when stop status changes to run status, the data that is maintained can be used for resuming the count.
At initial reset, this register is set to "0".

TMRST: Clock timer reset (FF40H•D1)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in run status, counting restarts immediately. Also, in stop status the reset data is maintained. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" at reading.

TM0–TM7: Timer data (FF41H, FF42H)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.
By reading the low-order data (FF41H), the high-order data (FF42H) is latched. The latched value, not the current value, is always read as the high-order data. Therefore, be sure to read the low-order data first.
At initial reset, the timer data is initialized to "00H".

EIT0: 128 Hz interrupt mask register (FFEEH•D0)
EIT1: 64 Hz interrupt mask register (FFEEH•D1)
EIT2: 32 Hz interrupt mask register (FFEEH•D2)
EIT3: 16 Hz interrupt mask register (FFEEH•D3)
EIT4: 8 Hz interrupt mask register (FFEFH•D0)
EIT5: 4 Hz interrupt mask register (FFEFH•D1)
EIT6: 2 Hz interrupt mask register (FFEFH•D2)
EIT7: 1 Hz interrupt mask register (FFEFH•D3)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3, EIT4, EIT5, EIT6, EIT7) are used to select whether to mask the interrupt to the separate frequencies (128 Hz, 64 Hz, 32 Hz, 16 Hz, 8 Hz, 4 Hz, 2 Hz, 1 Hz).
At initial reset, these registers are set to "0".

IT0: 128 Hz interrupt factor flag (FFFEH•D0)
IT1: 64 Hz interrupt factor flag (FFFEH•D1)
IT2: 32 Hz interrupt factor flag (FFFEH•D2)
IT3: 16 Hz interrupt factor flag (FFFEH•D3)
IT4: 8 Hz interrupt factor flag (FFFFH•D0)
IT5: 4 Hz interrupt factor flag (FFFFH•D1)
IT6: 2 Hz interrupt factor flag (FFFFH•D2)
IT7: 1 Hz interrupt factor flag (FFFFH•D3)

These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3, IT4, IT5, IT6, IT7) correspond to the clock timer interrupts of the respective frequencies (128 Hz, 64 Hz, 32 Hz, 16 Hz, 8 Hz, 4 Hz, 2 Hz, 1 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.7.6 Programming notes

(1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) The clock timer count clock does not synch with the CPU clock. Therefore, the correct value may not be obtained depending on the count data read and count-up timings. To avoid this problem, the clock timer count data should be read by one of the procedures shown below.

- Read the count data twice and verify if there is any difference between them.
- Temporarily stop the clock timer when the counter data is read to obtain proper data.

(3) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.8 Stopwatch Timer

4.8.1 Configuration of stopwatch timer

The S1C63632 has a 1/1,000 sec stopwatch timer. The stopwatch timer is configured of a 3-stage, 4-bit BCD counter serving as the input clock of a 1,000 Hz signal output from the prescaler. Data can be read out four bits (1/1,000 sec, 1/100 sec and 1/10 sec) at a time by the software.
In addition it has a direct input function that controls the stopwatch timer RUN/STOP and LAP using the input ports P10 and P11.
Figure 4.8.1.1 is the block diagram of the stopwatch timer.

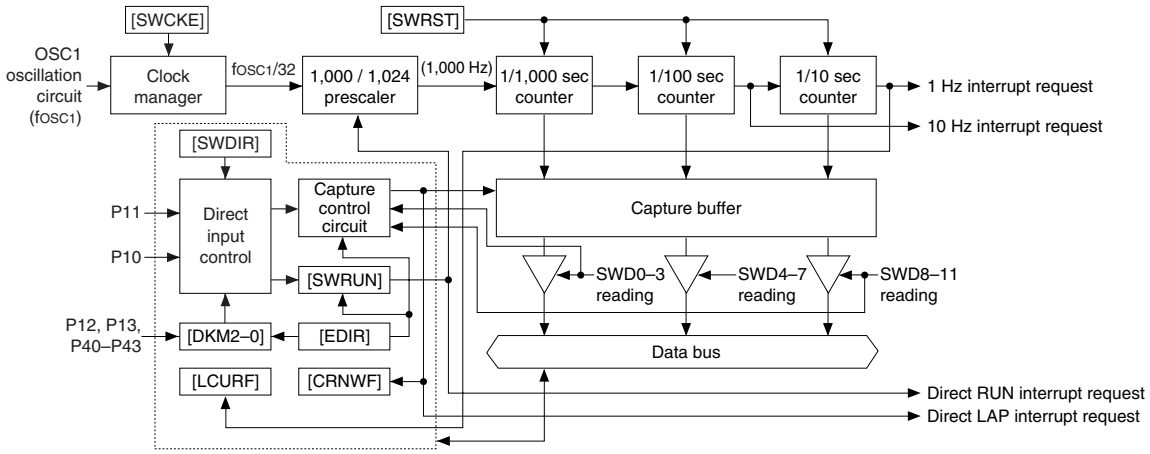


Fig. 4.8.1.1 Block diagram of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

4.8.2 Controlling clock manager

The clock manager generates the stopwatch timer operating clock by dividing the OSC1 clock by 32. Before the stopwatch timer can be run, write "1" to the SWCKE register to supply the operating clock to the stopwatch timer.

Table 4.8.2.1 Controlling stopwatch timer operating clock

SWCKE	Stopwatch timer clock
1	fOSC1 / 32 (1 kHz)
0	Off

If it is not necessary to run the stopwatch timer, stop the clock supply by setting SWCKE to "0" to reduce current consumption.

4.8.3 Counter and prescaler

The stopwatch timer is configured of four-bit BCD counters SWD0–3, SWD4–7 and SWD8–11.
The counter SWD0–3, at the stage preceding the stopwatch timer, has a 1,000 Hz signal generated by the prescaler for the input clock. It counts up every 1/1,000 sec, and generates 100 Hz signal. The counter SWD4–7 has a 100 Hz signal generated by the counter SWD0–3 for the input clock. It count-up every 1/100 sec, and generated 10 Hz signal. The counter SWD8–11 has an approximated 10 Hz signal generated by the counter SWD4–7 for the input clock. It count-up every 1/10 sec, and generated 1 Hz signal.
The prescaler inputs a 1,024 Hz clock dividing f_{OSC1} (output from the OSC1 oscillation circuit), and outputs 1,000 Hz counting clock for SWD0–3. To generate a 1,000 Hz clock from 1,024 Hz, 24 pulses from 1,024 pulses that are input to the prescaler every second are taken out.
When the counter becomes the value indicated below, one pulse (1,024 Hz) that is input immediately after to the prescaler will be pulled out.

<Counter value (msec) in which the pulse correction is performed>
39, 79, 139, 179, 219, 259, 299, 319, 359, 399, 439, 479, 539, 579, 619, 659, 699, 719, 759, 799, 839, 879, 939, 979

Figure 4.8.3.1 shows the operation of the prescaler.

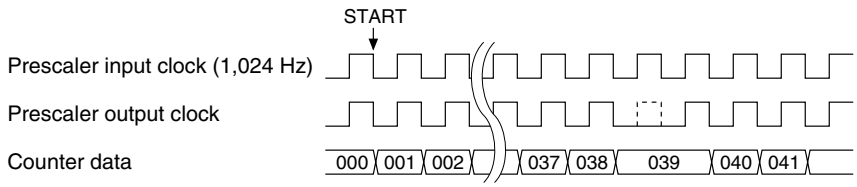


Fig. 4.8.3.1 Timing of the prescaler operation

For the above reason, the counting clock is 1,024 Hz (0.9765625 msec) except during pulse correction. Consequently, frequency of the prescaler output clock (1,000 Hz), 100 Hz generated by SWD0–3 and 10 Hz generated by SWD4–7 are approximate values.

4.8.4 Capture buffer and hold function

The stopwatch data, 1/1,000 sec, 1/100 sec and 1/10 sec, can be read from SWD0–3 (FF4BH), SWD4–7 (FF4CH) and SWD8–11 (FF4DH), respectively. The counter data are latched in the capture buffer when reading, and are held until reading of three words is completed. For this reason, correct data can be read even when a carry from lower digits occurs during reading the three words. Further, three counter data are latched in the capture buffer at the same time when SWD0–3 (1/1,000 sec) is read. The data hold is released when SWD8–11 (1/10 sec) reading is completed. Therefore, data should be read in order of SWD0–3 → SWD4–7 → SWD8–11. If SWD4–7 or SWD8–11 is first read when data have not been held, the hold function does not work and data in the counter is directly read out. When data that has not been held is read in the stopwatch timer RUN status, you cannot judge whether it is correct or not.

The stopwatch timer has a LAP function using an external key input (explained later). The capture buffer is also used to hold LAP data. In this case, data is held until SWD8–11 is read. However, when a LAP input is performed before completing the reading, the content of the capture buffer is renewed at that point. Remaining data that have not been read become invalid by the renewal, and the hold status is not released if SWD8–11 is read. When SWD8–11 is read after the capture buffer is updated, the capture renewal flag CRNWF is set to "1" at that point. In this case, it is necessary to read from SWD0–3 again. The capture renewal flag is renewed by reading SWD8–11.

Figure 4.8.4.1 shows the timing for data holding and reading.

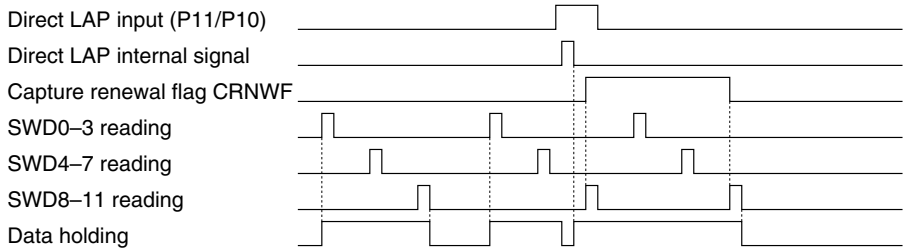


Fig. 4.8.4.1 Timing for data holding and reading

4.8.5 Stopwatch timer RUN/STOP and reset

RUN/STOP control and reset of the stopwatch timer can be done by the software.

Stopwatch timer RUN/STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count. The RUN/STOP operation of the stopwatch timer by writing to the SWRUN register is performed in synchronization with the falling edge of the 1,024 Hz same as the prescaler input clock. The SWRUN register can be read, and in this case it indicates the operating status of the stopwatch timer.

Figure 4.8.5.1 shows the operating timing when controlling the SWRUN register.

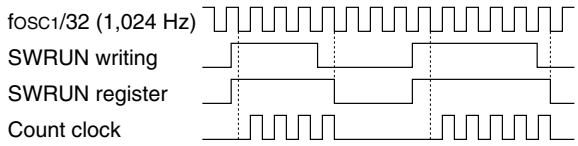


Fig. 4.8.5.1 Operating timing when controlling SWRUN

When the direct input function (explained in next section) is set, RUN/STOP control is done by an external key input. In this case, SWRUN becomes read only register that indicates the operating status of the stopwatch timer.

Stopwatch timer reset

The stopwatch timer is reset when "1" is written to SWRST. With this, the counter value is cleared to "000". Since this resetting does not affect the capture buffer, data that has been held in the capture buffer is not cleared and is maintained as is. When the stopwatch timer is reset in the RUN status, counting restarts from count "000". Also, in the STOP status the reset data "000" is maintained until the next RUN.

4.8.6 Direct input function and key mask

The stopwatch timer has a direct input function that can control the RUN/STOP and LAP operation of the stopwatch timer by external key input. This function is set by writing "1" to the EDIR register. When EDIR is set to "0", only the software control is possible as explained in the previous section.

Input port configuration

In the direct input function, the input ports P10 and P11 are used as the RUN/STOP and LAP input ports. The key assignment can be selected using the SWDIR register.

Table 4.8.6.1 RUN/STOP and LAP input ports

SWDIR	P10	P11
0	RUN/STOP	LAP
1	LAP	RUN/STOP

Direct RUN

When the direct input function is selected, RUN/STOP operation of the stopwatch timer can be controlled by using the key connected to the input port P10/P11 (selected by SWDIR). P10/P11 works as a normal input port, but the input signal is sent to the stopwatch control circuit. The key input signal from the P10/P11 port works as a toggle switch. When it is input in STOP status, the stopwatch timer runs, and in RUN status, the stopwatch timer stops. RUN/STOP status of the stopwatch timer can be checked by reading the SWRUN register. An interrupt is generated by direct RUN input.
The sampling for key input signal is performed at the falling edge of 1,024 Hz signal same as the SWRUN control. The chattering judgment is performed at the point where the key turns off, and a chattering less than 46.8–62.5 msec is removed. Therefore, more time is needed for an interval between RUN and STOP key inputs.
Figure 4.8.6.1 shows the operating timing for the direct RUN input.

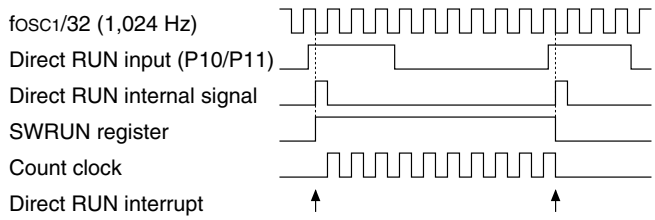


Fig. 4.8.6.1 Operating timing for direct RUN input

Direct LAP

Control for the LAP can also be done by key input same as the direct RUN. When the direct input function is selected, the input port P11/P10 (selected by SWDIR) becomes the LAP key input port. Sampling for the input signal and the chattering judgment are the same as a direct RUN.
By entering the LAP key, the counter data at that point is latched into the capture buffer and is held. The counter continues counting operation. Furthermore, an interrupt occurs by direct LAP input.
As stated above, the capture buffer data is held until SWD8–11 is read. If the LAP key is input when data has been already held, it renews the content of the capture buffer. When SWD8–11 is read after renewing, the capture renewal flag is set to "1". In this case, the hold status is not released by reading SWD8–11, and it continues. Normally the LAP data should be read after the interrupt is generated. After that, be sure to check the capture renewal flag. When the capture renewal flag is set, renewed data is held in the capture buffer. So it is necessary to read from SWD0–3 again.

The stopwatch timer sets the 1 Hz interrupt factor flag ISW1 to "1" when requiring a carry-up to 1-sec digit by an SWD8–11 overflow. If the capture buffer shifts into hold status (when SWD0–3 is read or when LAP is input) while the 1 Hz interrupt factor flag ISW1 is set to "1", the lap data carry-up request flag LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required for the processing of LAP input. In normal software processing, LAP processing may take precedence over 1-sec or higher digits processing by a 1 Hz interrupt, therefore carry-up processing using this flag should be used for time display in the LAP processing to prevent the 1-sec digit data decreasing by 1 second. This flag is renewed when the capture buffer shifts into hold status.
Figure 4.8.6.2 shows the operating timing for the direct LAP input, and Figure 4.8.6.3 shows the timings for data holding and reading during a direct LAP input and reading.

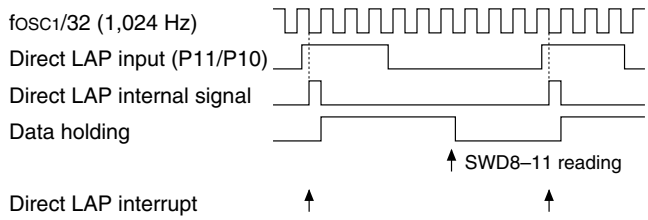


Fig. 4.8.6.2 Operating timing for direct LAP input

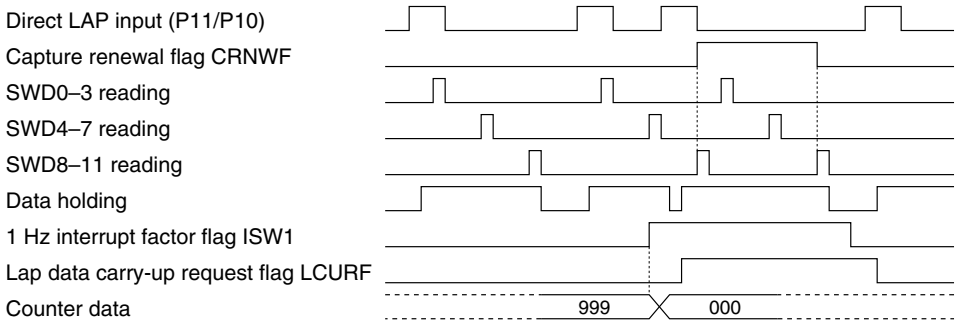


Fig. 4.8.6.3 Timing for data holding and reading during direct LAP input

Key mask

In stopwatch applications, some functions may be controlled by a combination of keys including direct RUN or direct LAP. For instance, the RUN key can be used for other functions, such as reset and setting a watch, by pressing the RUN key with another key. In this case, the direct RUN function or direct LAP function must be invalid so that it does not function. For this purpose, the key mask function is set so that it judges concurrence of input keys and invalidates RUN and LAP functions. A combination of the key inputs for this judgment can be selected using the DKM0–DKM2 registers.

Table 4.8.6.2 Key mask selection

DKM2	DKM1	DKM0	Mask key combination
0	0	0	None (at initial reset)
0	0	1	P12
0	1	0	P12, P13
0	1	1	P12, P13, P40
1	0	0	P40
1	0	1	P40, P41
1	1	0	P40, P41, P42
1	1	1	P40, P41, P42, P43

RUN or LAP inputs become invalid in the following status.

1. The RUN or LAP key is pressed when one or more keys that are included in the selected combination (here in after referred to as mask) are held down.
2. The RUN or LAP key has been pressed when the mask is released.

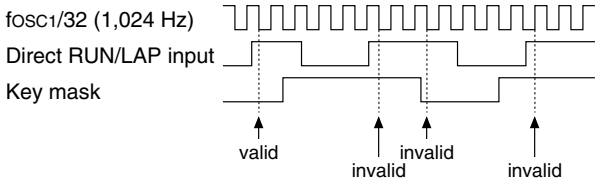


Fig. 4.8.6.4 Operation of key mask

RUN or LAP inputs become valid in the following status.

1. Either the RUN or LAP key is pressed independently if no other key is been held down.
2. Both the RUN and LAP keys are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)
3. The RUN or LAP key is pressed if either is held down. (RUN and LAP functions are effective.)
4. Either the RUN or LAP key and the mask key are pressed at the same time if no other key is held down.
5. Both the RUN and LAP keys and the mask key are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)

* Simultaneous key input is referred to as two or more key inputs are sampled at the same falling edge of 1,024 Hz clock.

4.8.7 Interrupt function

10 Hz and 1 Hz interrupts

The 10 Hz and 1 Hz interrupts can be generated through the overflow of stopwatch timers SWD4–7 and SWD8–11 respectively. Also, software can set whether to separately mask the frequencies described earlier.

Figure 4.8.7.1 is the timing chart for the counters.

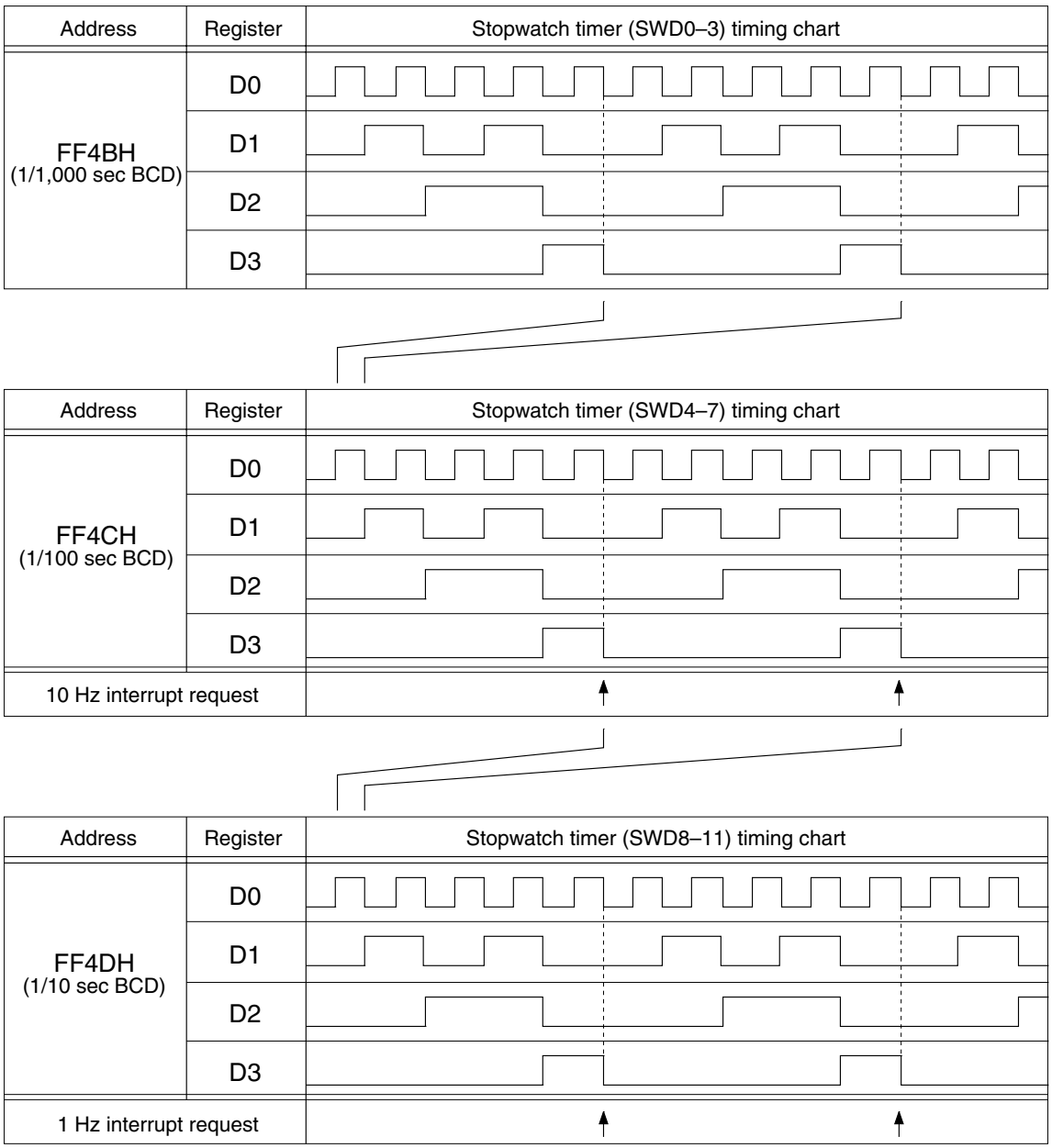


Fig. 4.8.7.1 Timing chart for counters

As shown in Figure 4.8.7.1, the interrupts are generated by the overflow of their respective counters ("9" changing to "0"). Also, at this time the corresponding interrupt factor flag (ISW10, ISW1) is set to "1". The respective interrupts can be masked separately through the interrupt mask registers (EISW10, EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

Direct RUN and direct LAP interrupts

When the direct input function is selected, the direct RUN and direct LAP interrupts can be generated. The respective interrupts occur at the rising edge of the internal signal for direct RUN and direct LAP after sampling the direct input signal in the falling edge of 1,024 Hz signal. Also, at this time the corresponding interrupt factor flag (IRUN, ILAP) is set to "1".
The respective interrupts can be masked separately through the interrupt mask registers (EIRUN, EILAP). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the inputs of the RUN and LAP.

The direct RUN and LAP functions use the P10 and P11 ports. Therefore, the direct input interrupt and the P10–P13 inputs interrupt may generate at the same time depending on the interrupt condition setting for the input port P10–P13. Consequently, when using the direct input interrupt, set the interrupt select registers SIP10 and SIP11 to "0" so that the input interrupt does not generate by P10 and P11 inputs.

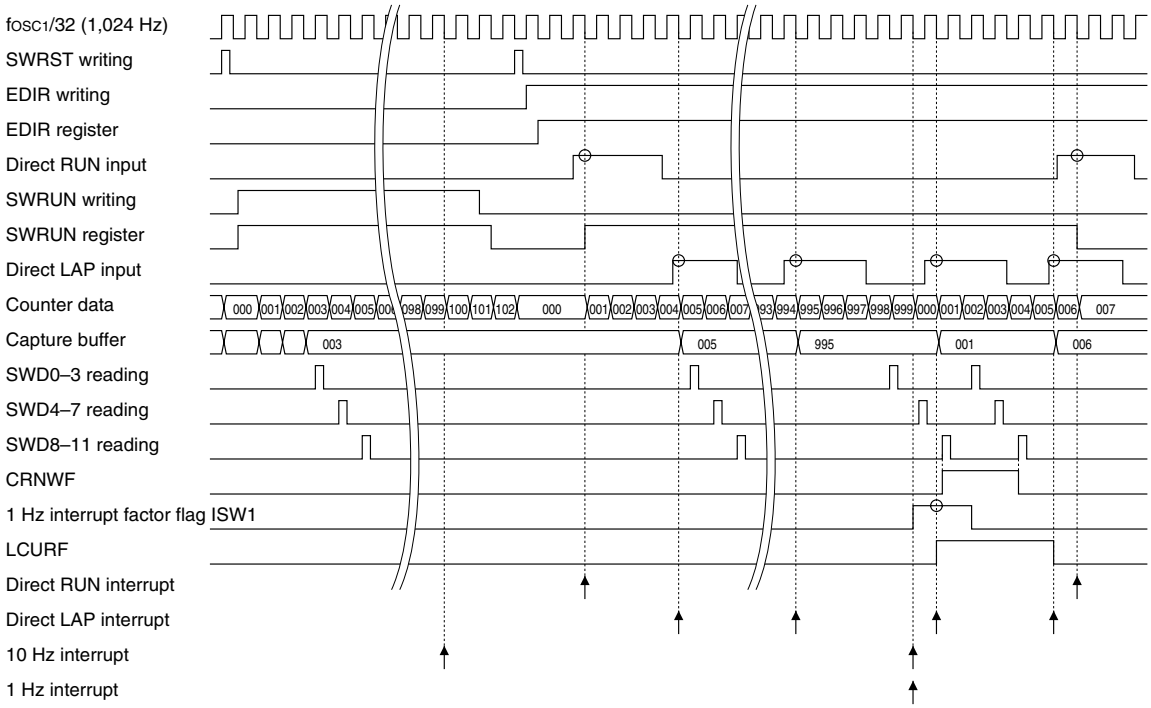


Fig. 4.8.7.2 Timing chart for stopwatch timer

4.8.8 I/O memory of stopwatch timer

Table 4.8.8.1 shows the I/O addresses and the control bits for the stopwatch timer.

Table 4.8.8.1 Control bits of stopwatch timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF16H	MDCKE	SGCKE	SWCKE	RTCKE	MDCKE	0	Enable	Disable	Integer multiplier clock enable
					SGCKE	0	Enable	Disable	Sound generator clock enable
	R/W				SWCKE	0	Enable	Disable	Stopwatch timer clock enable
					RTCKE	0	Enable	Disable	Clock timer clock enable
FF48H	0	0	SWDIR	EDIR	0 *3	– *2			Unused
					0 *3	– *2			Unused
					SWDIR	0			Stopwatch direct input switch
	R		R/W						0: P10=Run/Stop, P11=Lap 1: P10=Lap, P11=Run/Stop
					EDIR	0	Enable	Disable	Direct input enable
FF49H	0	DKM2	DKM1	DKM0	0 *3	– *2			Unused
					DKM2	0			Key mask selection: [DKM2–0] 0 1 2 3 / Key mask None P12 P12–13 P12–13,40 / [DKM2–0] 4 5 6 7 / Key mask P40 P40–41 P40–42 P40–43
	R	R/W			DKM1	0			
					DKM0	0			
FF4AH	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Request	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
FF4BH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/1000 sec)
					SWD2	0			
	R				SWD1	0			
					SWD0	0			
FF4CH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/100 sec)
					SWD6	0			
	R				SWD5	0			
					SWD4	0			
FF4DH	SWD11	SWD10	SWD9	SWD8	SWD11	0			Stopwatch timer data BCD (1/10 sec)
					SWD10	0			
	R				SWD9	0			
					SWD8	0			
FFEDH	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFFDH	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SWCKE: Stopwatch timer clock enable register (FF16H•D1)

Controls the operating clock supply to the stopwatch timer.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to SWCKE, the stopwatch timer operating clock is supplied from the clock manager. If it is not necessary to run the stopwatch timer, stop the clock supply by setting SWCKE to "0" to reduce current consumption.
At initial reset, this register is set to "0".

EDIR: Direct input function enable register (FF48H•D0)

Enables the direct input (RUN/LAP) function.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

The direct input function is enabled by writing "1" to EDIR, and then RUN/STOP and LAP control can be done by external key input. When "0" is written, the direct input function is disabled, and the stopwatch timer is controlled by the software only.
Further the function switching is actually done by synchronizing with the falling edge of fOSC1/32 (1,024 Hz) after the data is written to this register (after 977 µsec maximum).
At initial reset, this register is set to "0".

SWDIR: Direct input switch register (FF48H•D1)

Switches the direct-input key assignment for the P10 and P11 ports.

When "1" is written: P10 = LAP, P11 = RUN/STOP
When "0" is written: P10 = RUN/STOP, P11 = LAP
Reading: Valid

The direct-input key assignment is selected using this register. The P10 and P11 port statuses are input to the stopwatch timer as the RUN/STOP and LAP inputs according to this selection.
At initial reset, this register is set to "0".

DKM0–DKM2: Direct key mask select register (FF49H•D0–D2)

Selects a combination of the key inputs for concurrence judgment with RUN and LAP inputs when the direct input function is set.

Table 4.8.8.2 Key mask selection

DKM2	DKM1	DKM0	Mask key combination
0	0	0	None (at initial reset)
0	0	1	P12
0	1	0	P12, P13
0	1	1	P12, P13, P40
1	0	0	P40
1	0	1	P40, P41
1	1	0	P40, P41, P42
1	1	1	P40, P41, P42, P43

When the concurrence is detected, RUN and LAP inputs cannot be accepted until the concurrence is released.
At initial reset, this register is set to "0".

SWRST: Stopwatch timer reset (FF4AH•D0)

This bit resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained.
Since this reset does not affect the capture buffer, the capture buffer data in hold status is not cleared and is maintained.
This bit is write-only, and is always "0" at reading.

SWRUN: Stopwatch timer RUN/STOP (FF4AH•D1)

This register controls the RUN/STOP of the stopwatch timer, and the operating status can be monitored by reading this register.

• ***When writing data***

When "1" is written: RUN
When "0" is written: STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count. RUN/STOP control with this register is valid only when the direct input function is set to disable. When the direct input function is set, it becomes invalid.

• ***When reading data***

When "1" is read: RUN
When "0" is read: STOP

Reading is always valid regardless of the direct input function setting. "1" is read when the stopwatch timer is in the RUN status, and "0" is read in the STOP status.
At initial reset, this register is set to "0".

CRNWF: Capture renewal flag (FF4AH•D2)

This flag indicates that the content of the capture buffer has been renewed.

When "1" is read: Renewed
When "0" is read: Not renewed
Writing: Invalid

The content of the capture buffer is renewed if the LAP key is input when the data held into the capture buffer has not yet been read. Reading SWD8–11 in that status sets this flag to "1", and the hold status is maintained. Consequently, when data that is held by a LAP input is read, read this flag after reading the SWD8–11 and check whether the data has been renewed or not.
This flag is renewed when SWD8–11 is read.
At initial reset, this flag is set to "0".

LCURF: Lap data carry-up request flag (FF4AH•D3)

This flag indicates a carry that has been generated to 1 sec-digit when the data is held. Note that this flag is invalid when the direct input function is disabled.

When "1" is read: Carry is required
When "0" is read: Carry is not required
Writing: Invalid

If the capture buffer shifts into hold status while the 1 Hz interrupt factor flag ISW1 is set to "1", LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required. When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read this flag before processing and check whether carry-up is needed or not.
This flag is renewed (set/reset) every time the capture buffer shifts into hold status.
At initial reset, this flag is set to "0".

SWD0–SWD3: Stopwatch timer data 1/1,000 sec (FF4BH)

Data (BCD) of the 1/1,000 sec column of the capture buffer can be read out.
The hold function of the capture buffer works by reading this data.
These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

SWD4–SWD7: Stopwatch timer data 1/100 sec (FF4CH)

Data (BCD) of the 1/100 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

SWD8–SWD11: Stopwatch timer data 1/10 sec (FF4DH)

Data (BCD) of the 1/10 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

Note: Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

EIRUN, EILAP, EISW1, EISW10: Interrupt mask registers (FFEDH)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers EIRUN, EILAP, EISW1 and EISW10 are used to separately select whether to mask the direct RUN, direct LAP, 1 Hz and 10 Hz interrupts.
At initial reset, these registers are set to "0".

IRUN, ILAP, ISW1, ISW10: Interrupt factor flags (FFFDH)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IRUN, ILAP, ISW1 and ISW10 correspond to the direct RUN, direct LAP, 1 Hz and 10 Hz interrupts respectively. The software can judge from these flags whether there is a stopwatch timer interrupt. However, even if the interrupt is masked, the flags are set to "1" when the timing condition is established.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.8.9 Programming notes

(1) The interrupt factor flag should be reset after resetting the stopwatch timer.

(2) Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

(3) When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWD8–11 and check whether the data has been renewed or not.

(4) When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.9 Programmable Timer

4.9.1 Configuration of programmable timer

The S1C63632 has built-in four (Ch.A–Ch.D) units of 8 bits × 2-channel programmable timers. Each unit may be configured to 8-bit timer × 2 channels or 16-bit timer × 1 channel with software.
Ch.A: Timer 0 and Timer 1 (8 bits × 2 channels) or Timer 0 + 1 (16 bits x 1 channel)
Ch.B: Timer 2 and Timer 3 (8 bits × 2 channels) or Timer 2 + 3 (16 bits × 1 channel)
Ch.C: Timer 4 and Timer 5 (8 bits × 2 channels) or Timer 4 + 5 (16 bits × 1 channel)
Ch.D: Timer 6 and Timer 7 (8 bits × 2 channels) or Timer 6 + 7 (16 bits × 1 channel)

Figures 4.9.1.1 to 4.9.1.4 show the configuration of the programmable timers.
Each timer has an 8-bit down counter and an 8-bit reload data register. The down counter counts the internal clock of which the frequency can be selected with software. Furthermore, Timers 0, 2, 4, 6 also have an event counter function to count the clock input from the P12, P41, P42 and P43 terminals. When the down counter underflows during counting with the specified clock, the timer outputs the underflow and interrupt signals and resets the counter to its initial value. The reload data register is used to set that initial value.
The underflow signal of Timer 1 is used as the source clock of the R/f converter and serial interface, this makes it possible to program a flexible R/f converter count clock and the transfer rate of the serial interface.
Each timer has an 8-bit compare data register in addition to the above registers. This register is used to store data to be compared with the contents of the down counter. When the timer is set to PWM mode, the timer outputs the compare match signal if the contents between the down counter and the compare data register are matched, and an interrupt occurs at the same time. Also the compare match signal is used with the underflow signal to generate a PWM waveform.
The signal generated by the programmable timer can be output from the P13, P31, P32 or P33 port terminal.

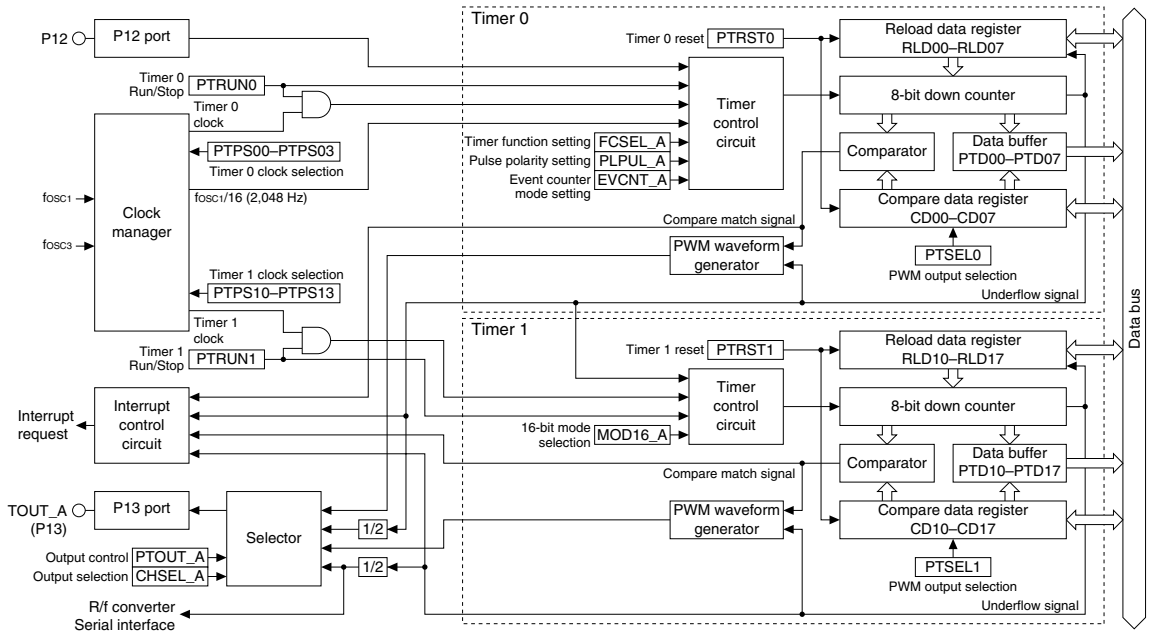


Fig. 4.9.1.1 Configuration of programmable timer Ch.A (Timers 0 and 1)

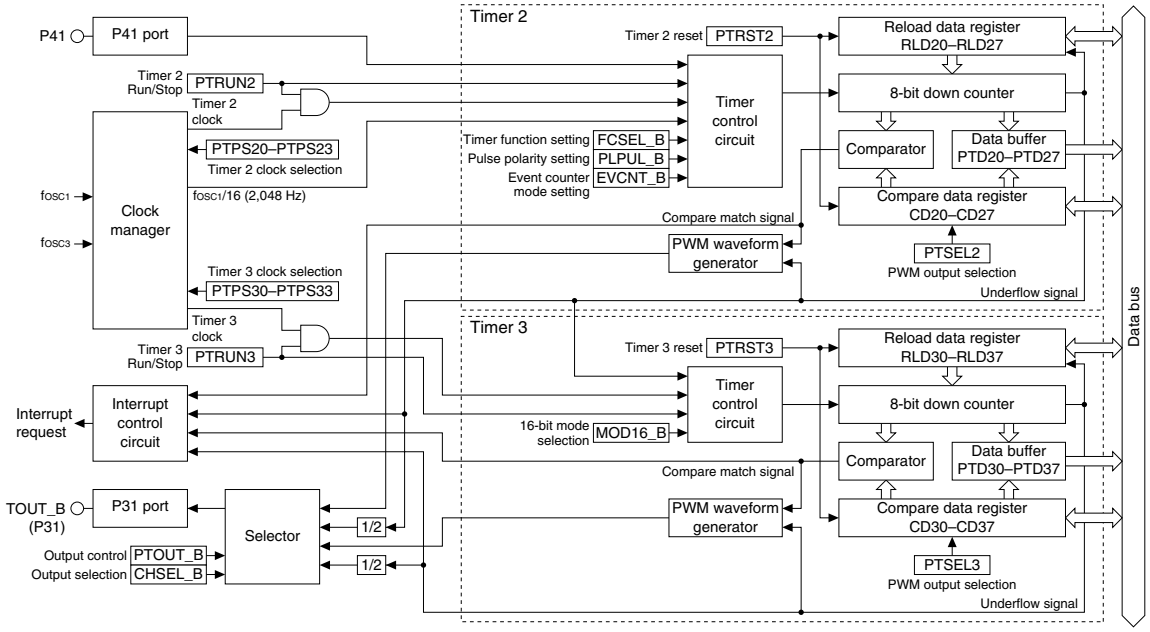


Fig. 4.9.1.2 Configuration of programmable timer Ch.B (Timers 2 and 3)

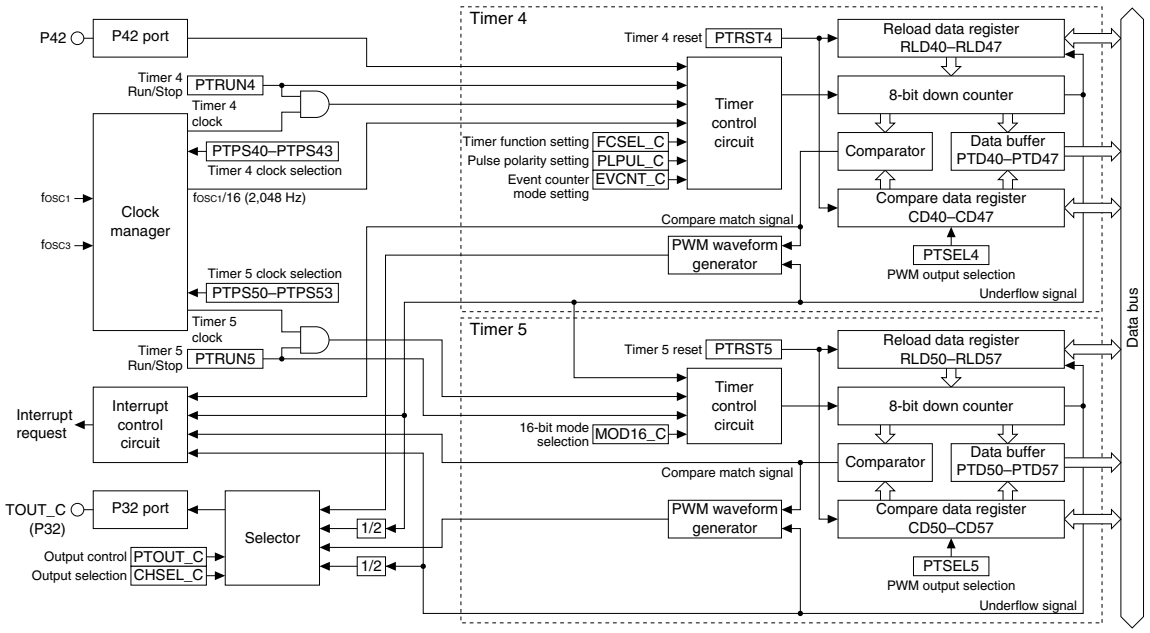


Fig. 4.9.1.3 Configuration of programmable timer Ch.C (Timers 4 and 5)

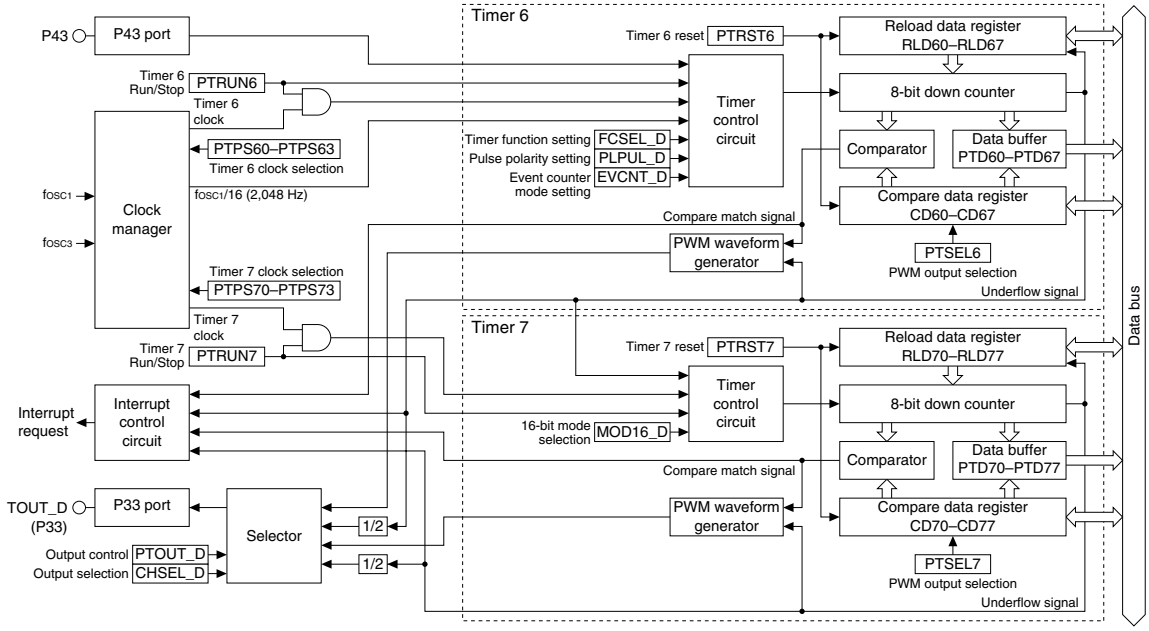


Fig. 4.9.1.4 Configuration of programmable timer Ch.D (Timers 6 and 7)

Notes:
- *All four timer units (Ch.A–Ch.D) have the same functions and structure except the register names, I/O ports used and their signal names. To simplify the explanations, the subsequent sections are described using Ch.A (Timers 0 and 1). The register and signal names have a timer number (0 to 7) or unit (Ch.) name (A to D). They are described using the names for Ch.A (Timers 0 and 1) or "x" (= timer number 0 to 7) except when a specific description is required. Description for Ch.A is applied to Ch.B to Ch.D.*
  Examples:
  Ch.A → Can be replaced with Ch.B, Ch.C and Ch.D
  EVCNT_A register → Can be replaced with EVCNT_B, EVCNT_C and EVCNT_D registers
  TOUT_A → Can be replaced with TOUT_B, TOUT_C and TOUT_D
  Descriptions for Timer 0, Timer 1, and Timer x are applied to other timers
  Examples:
  Timer 0 → Can be replaced with Timer 2, Timer 4 and Timer 6
  Timer 1 → Can be replaced with Timer 3, Timer 5 and Timer 7
  Timer x → Can be replaced with Timer 0 to Timer 7
  PTRUNx register → Can be replaced with PTRUN0 to PTRUN7 registers
- *If the TOUT_A–TOUT_D terminals are used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.*

4.9.2 Controlling clock manager

The clock manager generates the down-count clock for each timer by dividing the OSC1 or OSC3 clock. Table 4.9.2.1 lists the 15 count clocks that can be generated by the clock manager, and the clock to be used for each timer can be selected using the count clock frequency select register PTPSx0–PTPSx3. At initial reset, the PTPSx register is set to "0H" and the clock supply from the clock manager to the programmable timer is disabled. Before the timer can be run, select a clock to enable the clock supply.

Table 4.9.2.1 Selecting count clock frequency

PTPSx3	PTPSx2	PTPSx1	PTPSx0	Timer clock
1	1	1	1	f_{OSC3}
1	1	1	0	f_{OSC3} / 2
1	1	0	1	f_{OSC3} / 4
1	1	0	0	f_{OSC3} / 8
1	0	1	1	f_{OSC3} / 16
1	0	1	0	f_{OSC3} / 32
1	0	0	1	f_{OSC3} / 64
1	0	0	0	f_{OSC3} / 256
0	1	1	1	f_{OSC1} (32 kHz)
0	1	1	0	f_{OSC1} / 2 (16 kHz)
0	1	0	1	f_{OSC1} / 4 (8 kHz)
0	1	0	0	f_{OSC1} / 16 (2 kHz)
0	0	1	1	f_{OSC1} / 32 (1 kHz)
0	0	1	0	f_{OSC1} / 64 (512 Hz)
0	0	0	1	f_{OSC1} / 256 (128 Hz)
0	0	0	0	OFF

f_{OSC1}: OSC1 oscillation frequency. ( ) indicates the frequency when f_{OSC1} = 32 kHz.
f_{OSC3}: OSC3 oscillation frequency

Stop the clock supply to the timers shown below by setting PTPSx to "0H" to reduce current consumption.

- Unused timer
- Timer used as an event counter that inputs an external clock
- Upper 8-bit timer (Timer 1/3/5/7) when the timer unit is used as a 16-bit × 1 channel configuration.

4.9.3 Basic count operation

This section explains the basic count operation when each timer is used as an individual 8-bit timer.

Each timer has an 8-bit down counter and an 8-bit reload data register.
The reload data register RLDx0–RLDx7 is used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRSTx, the down counter loads the initial value set in the reload register. Therefore, down-counting is executed from the stored initial value by the input clock.
The PTRUNx register is provided to control the RUN/STOP for each timer. By writing "1" to this register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.
The counter data can be read via the data buffer PTDx0–PTDx7 in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data (PTDx4–PTDx7) when the low-order data (PTDx0–PTDx3) is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.
The counter reloads the initial value set in the reload data register when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation and pulse (TOUT_A signal) output. The underflow signal of Timer 1 (Ch.A) is also used to generate the clock to be supplied to the serial interface and R/f converter.

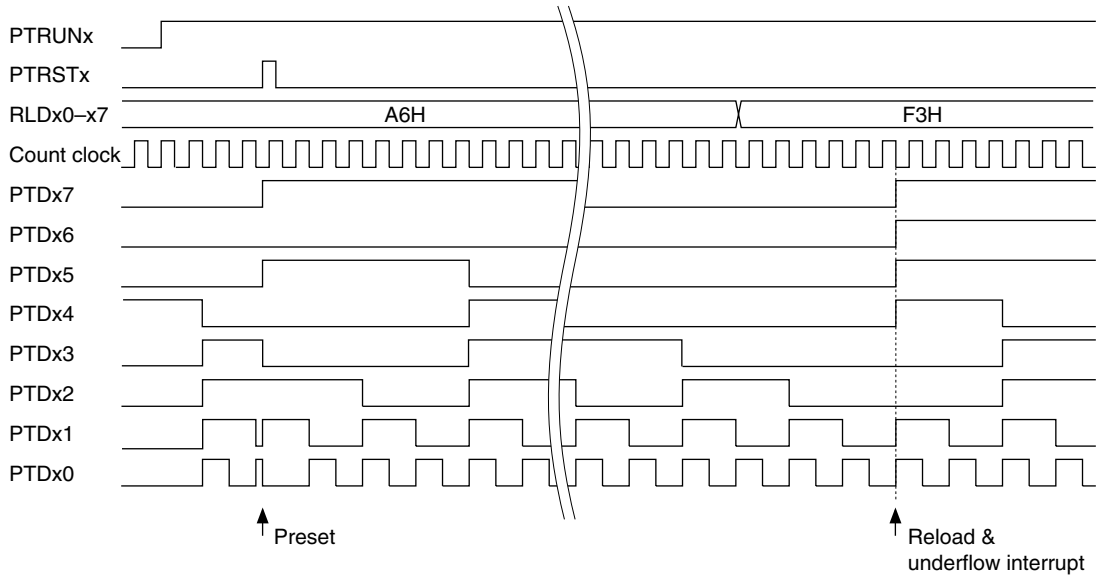


Fig. 4.9.3.1 Basic operation timing of down counter

4.9.4 Event counter mode (Timers 0, 2, 4 and 6)

Timer 0 has an event counter function that counts an external clock input to an I/O port. Table 4.9.4.1 lists the timers and their clock input ports.

Table 4.9.4.1 Event counter clock input port

Timer	External clock name	Input terminal	Control register
Timer 0 (Ch.A)	EVIN_A	P12	EVCNT_A
Timer 2 (Ch.B)	EVIN_B	P41	EVCNT_B
Timer 4 (Ch.C)	EVIN_C	P42	EVCNT_C
Timer 6 (Ch.D)	EVIN_D	P43	EVCNT_D

This function is selected by writing "1" to the counter mode select register EVCNT_A. This sets the corresponding I/O port to input mode and enables the port to send the input signal to Timer 0 as the count clock. At initial reset, EVCNT_A is set to "0" and Timer 0 is configured as a normal timer that counts the internal clock.
In the event counter mode, the clock is supplied to Timer 0 from outside the IC, therefore, the settings of the count clock frequency select register PTPS0 becomes invalid.
Count down timing can be selected from either the falling or rising edge of the input clock using the pulse polarity select register PLPUL_A. When "0" is written to the PLPUL_A register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.9.4.1.

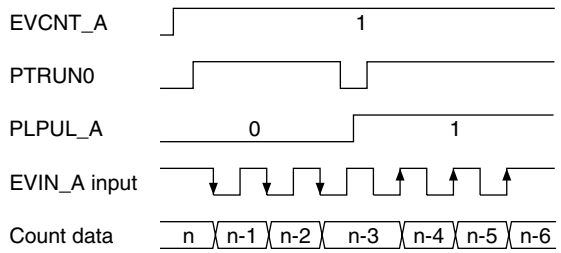


Fig. 4.9.4.1 Timing chart in event counter mode

The event counter mode also allows use of a noise reject function to eliminate noise such as chattering on the external clock (EVIN_A). This function is selected by writing "1" to the timer function select register FCSEL_A.
When the noise rejector is enabled, an input pulse width for both low and high levels must be 0.98 msec* or more to count reliably. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz* signal after changing the input level of the EVIN_A input terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec* or less.
(*: when f_{OSC1} = 32.768 kHz)
Figure 4.9.4.2 shows the count down timing with noise rejector.

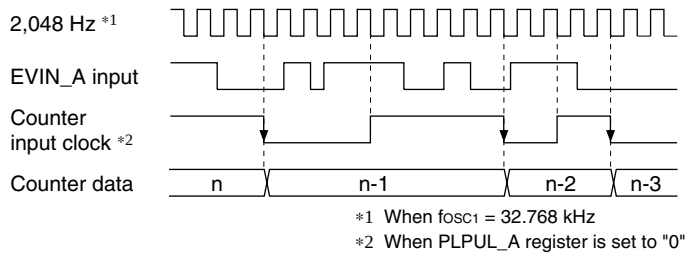


Fig. 4.9.4.2 Count down timing with noise rejector

The operation of the event counter mode is the same as the normal timer except it uses the EVIN_A input as the clock. Refer to Section 4.9.3, "Basic count operation" for basic operation and control.

4.9.5 PWM mode (Timers 0–7)

Each timer can generate a PWM waveform. When using this function, write "1" to the PTSELx register to set the timer to PWM mode.
The compare data register CDx0–CDx7 is provided for each timer to control the PWM waveform. In PWM mode, the timer compares data between the down counter and the compare data register and outputs the compare match signal if their contents are matched. At the same time a compare match interrupt occurs. Furthermore, the timer output signal rises with the underflow signal and falls with the compare match signal. As shown in Figure 4.9.5.1, the cycle and duty ratio of the output signal can be controlled using the reload data register and the compare data register, respectively, to generate a PWM signal. Note, however, the following condition must be met: RLD (reload data) > CD (compare data) and CD ≠ 0. If RLD ≤ CD, the output signal is fixed at "1" after the first underflow occurs and does not fall to "0".
The generated PWM signal can be output from an I/O port (P13, P31, P32 or P33) terminal (see Section 4.9.8).

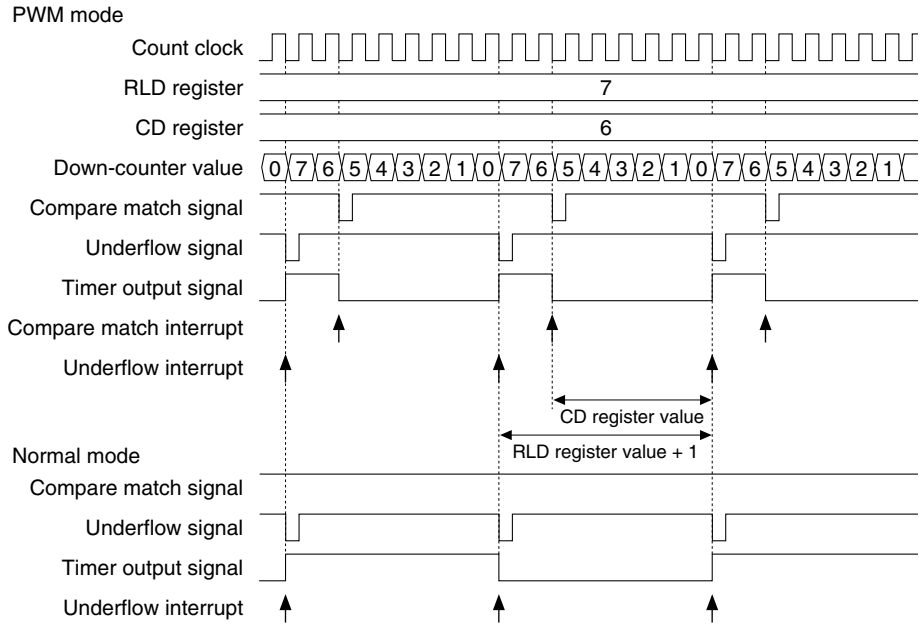


Fig. 4.9.5.1 Generating PWM waveform

4.9.6 16-bit timer mode (Timer 0 + 1, Timer 2 + 3, Timer 4 + 5, Timer 6 + 7)

Timers 0 and 1, Timers 2 and 3, Timers 4 and 5, and Timers 6 and 7 combinations can be used as 16-bit timers.
To use Timers 0 and 1 as a 16-bit timer, write "1" to the Timer 0 16-bit mode select register MOD16_A. The 16-bit timer is configured with Timer 0 for low-order byte and Timer 1 for high-order byte as shown in Figure 4.9.6.1.

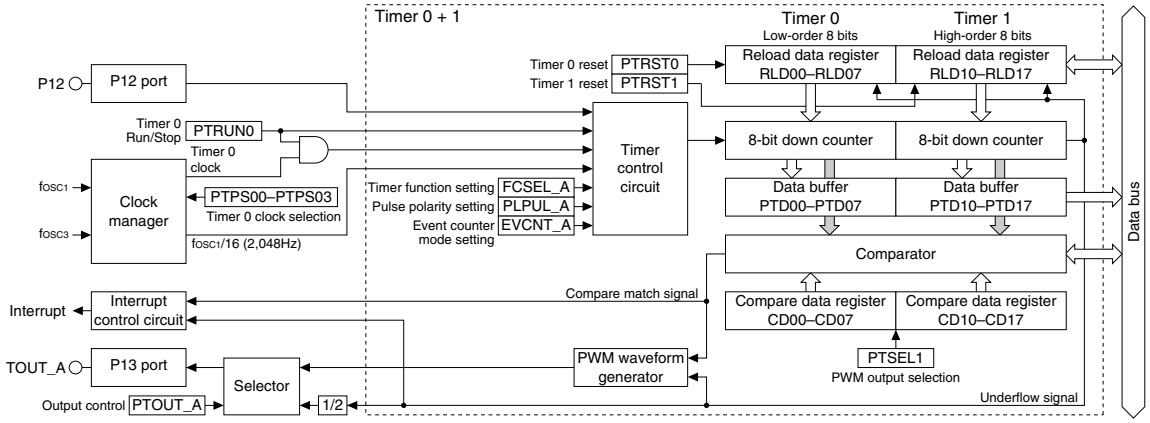


Fig. 4.9.6.1 Configuration of 16-bit timer (Timer 0 + 1)

In 16-bit timer mode, the Timer 0 register settings are effective for timer RUN/STOP control and count clock frequency selection. The event counter function can also be used. Timer 1 uses the Timer 0 underflow signal as the count clock, therefore, the Timer 1 RUN/STOP control and count clock frequency select registers become invalid. However, the PWM output function must be controlled using the Timer 1 control register. Timer 1 output signal is automatically selected for the TOUT_A output (the TOUT_A output select register is ineffective). The reload data must be preset to Timer 0 and Timer 1 separately using each PTRSTx register.

The counter data of a 16-bit timer must be read from the low-order 4 bits. In 16-bit timer mode, the high-order data (PTD04–PTD17) is latched by reading the low-order 4 bits (PTD00–PTD03). The counter keeps counting. However, the latched high-order data is maintained until the next reading of low-order data. Therefore, after the low-order 4-bit data (PTD00–PTD03) is read, the high-order data (PTD04–PTD17) can be read regardless of the order for reading. If data other than the low-order 4 bits (PTD00–PTD03) is read first, the hold function is not activated. In this case, the correct counter data cannot be read.

The description above is applied when Timers 2 and 3, Timers 4 and 5 or Timers 6 and 7 are used as a 16-bit timer.

4.9.7 Interrupt function

The programmable timer can generate interrupts from the underflow and compare match signals of each timer. See Figures 4.9.3.1 and 4.9.5.1 for the interrupt timing.

Note: The compare match interrupt can be generated only when the timer is set to PWM mode.

The underflow and compare match signals set the corresponding interrupt factor flag IPTx and ICTCx to "1", and an interrupt is generated. The interrupt can also be masked by setting the corresponding interrupt mask registers EIPTx and ECTCx. However, the interrupt factor flag is set to "1" by an underflow/compare match of the corresponding timer regardless of the interrupt mask register setting.

When Timers 0 and 1 are used as a 16-bit timer, an interrupt is generated by an underflow of Timer 1. In this case, IPT0 is not set to "1" by a Timer 0 underflow. The compare match interrupt uses ICTC1 of Timer 1. The same applies when other timers are used as a 16-bit timer.

4.9.8 Control of TOUT output

The programmable timer Ch.A (Timers 0 and 1) can generate the TOUT_A signal from the timer underflow and compare match signals. The TOUT_A signal is generated by dividing the underflow signal by 2 in normal mode. In PWM mode, the PWM signal generated as described above is output as the TOUT_A signal.

Table 4.9.8.1 TOUT outputs and control registers

Output clock name	Output terminal	Output control register	Output select register	Output timer
TOUT_A	P13	PTOUT_A	CHSEL_A="0"	Timer 0
			CHSEL_A="1"	Timer 1
TOUT_B	P31	PTOUT_B	CHSEL_B="0"	Timer 2
			CHSEL_B="1"	Timer 3
TOUT_C	P32	PTOUT_C	CHSEL_C="0"	Timer 4
			CHSEL_C="1"	Timer 5
TOUT_D	P33	PTOUT_D	CHSEL_D="0"	Timer 6
			CHSEL_D="1"	Timer 7

It is possible to select either Timer 0 or Timer 1 output to be used by the TOUT output channel select register CHSEL_A.
In 16-bit timer mode, Timer 1 is always selected for generating the TOUT_A signal regardless of how CHSEL_A is set.

The TOUT signal generated by each timer can be output from the P13, P31, P32 or P33 I/O port terminal to supply a clock to an external device.

The output of the TOUT_A signal is controlled by the PTOUT_A register. When "1" is written to the PTOUT_A register, the TOUT_A signal is output from the corresponding I/O port terminal.
When TOUT output is enabled, the I/O port is automatically set to output mode and it outputs the TOUT_A signal sent from the timer. The I/O control register (IOC13/IOC31/IOC32/IOC33) and the data register (P13/P31/P32/P33) are ineffective. When PTOUT_A is set to "0", the I/O port control registers become effective.
Since the TOUT_A signal is generated asynchronously from the PTOUT_A register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.
Figure 4.9.8.1 shows the output waveform of the TOUT_A signal.

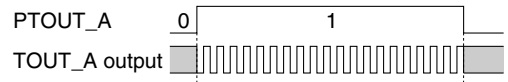


Fig. 4.9.8.1 Output waveform of the TOUT_A signal

The Ch.B to Ch.D can be controlled the same as above to output the TOUT signal.

4.9.9 Clock output to serial interface and R/f converter

The signal that is made from underflows of Timer 1 by dividing them by 2, can be used as the clock source for the serial interface and R/f converter.
Timer 1 always outputs the clock to the serial interface and R/f converter by setting Timer 1 into RUN state (PTRUN1 = "1"). It is not necessary to control with the PTOUT_A register.

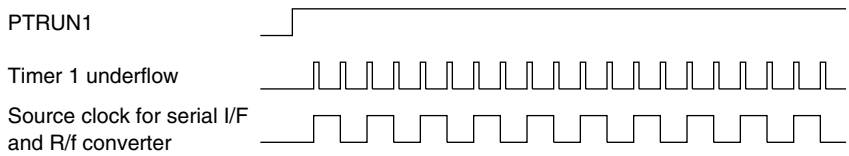


Fig. 4.9.9.1 Clock output to serial interface and R/f converter

A setting value for the RLD1x register according to a transfer rate of the serial interface is calculated by the following expression:

$$RLD1x = \frac{f_{CNT1}}{2 * bps} - 1$$

f_{CNT1}: Timer 1 count clock frequency set by the PTPS1 register (See Table 4.9.2.1.)
bps: Transfer rate
(00H can be set to RLD1x)

Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source.

4.9.10 I/O memory of programmable timer

Table 4.9.10.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.9.10.1(a) Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF18H	PTPS03	PTPS02	PTPS01	PTPS00	PTPS03	0			Programmable timer 0 count clock frequency selection [PTPS03–00] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS03–00] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS03–00] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS02	0			
	R/W				PTPS01	0			
					PTPS00	0			
FF19H	PTPS13	PTPS12	PTPS11	PTPS10	PTPS13	0			Programmable timer 1 count clock frequency selection [PTPS13–10] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS13–10] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS13–10] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS12	0			
	R/W				PTPS11	0			
					PTPS10	0			
FF1AH	PTPS23	PTPS22	PTPS21	PTPS20	PTPS23	0			Programmable timer 2 count clock frequency selection [PTPS23–20] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS23–20] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS23–20] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS22	0			
	R/W				PTPS21	0			
					PTPS20	0			
FF1BH	PTPS33	PTPS32	PTPS31	PTPS30	PTPS33	0			Programmable timer 3 count clock frequency selection [PTPS33–30] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS33–30] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS33–30] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS32	0			
	R/W				PTPS31	0			
					PTPS30	0			
FF1CH	PTPS43	PTPS42	PTPS41	PTPS40	PTPS43	0			Programmable timer 4 count clock frequency selection [PTPS43–40] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS43–40] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS43–40] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS42	0			
	R/W				PTPS41	0			
					PTPS40	0			
FF1DH	PTPS53	PTPS52	PTPS51	PTPS50	PTPS53	0			Programmable timer 5 count clock frequency selection [PTPS53–50] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS53–50] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS53–50] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS52	0			
	R/W				PTPS51	0			
					PTPS50	0			
FF1EH	PTPS63	PTPS62	PTPS61	PTPS60	PTPS63	0			Programmable timer 6 count clock frequency selection [PTPS63–60] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS63–60] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS63–60] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS62	0			
	R/W				PTPS61	0			
					PTPS60	0			
FF1FH	PTPS73	PTPS72	PTPS71	PTPS70	PTPS73	0			Programmable timer 7 count clock frequency selection [PTPS73–70] 0 1 2 3 4 5 Frequency Off fosc1/256 fosc1/64 fosc1/32 fosc1/16 fosc1/4 [PTPS73–70] 6 7 8 9 10 Frequency fosc1/2 fosc1 fosc3/256 fosc3/64 fosc3/32 [PTPS73–70] 11 12 13 14 15 Frequency fosc3/16 fosc3/8 fosc3/4 fosc3/2 fosc3
					PTPS72	0			
	R/W				PTPS71	0			
					PTPS70	0			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.9.10.1(b) Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF80H	MOD16_A	EVCNT_A	FCSEL_A	PLPUL_A	MOD16_A	0	16 bits	8 bits	PTM0–1 16-bit mode selection
					EVCNT_A	0	Event ct.	Timer	PTM0 counter mode selection
					FCSEL_A	0	With NR	No NR	PTM0 function selection (for event counter mode)
	R/W				PLPUL_A	0	↑	↓	PTM0 pulse polarity selection (for event counter mode)
FF81H	PTSEL1	PTSEL0	CHSEL_A	PTOUT_A	PTSEL1	0	PWM	Normal	Programmable timer 1 PWM output selection
					PTSEL0	0	PWM	Normal	Programmable timer 0 PWM output selection
					CHSEL_A	0	Timer 1	Timer 0	PTM0–1 TOUT_A output selection
	R/W				PTOUT_A	0	On	Off	PTM0–1 TOUT_A output control
FF82H	PTRST1	PTRUN1	PTRST0	PTRUN0	PTRST1*3	– *2	Reset	Invalid	Programmable timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Programmable timer 1 Run/Stop
	W	R/W	W	R/W	PTRST0*3	– *2	Reset	Invalid	Programmable timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Programmable timer 0 Run/Stop
FF84H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
					RLD01	0			
	R/W				RLD00	0			LSB
FF85H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
					RLD05	0			
	R/W				RLD04	0			LSB
FF86H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
					RLD11	0			
	R/W				RLD10	0			LSB
FF87H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
					RLD15	0			
	R/W				RLD14	0			LSB
FF88H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
					PTD01	0			
	R				PTD00	0			LSB
FF89H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
					PTD05	0			
	R				PTD04	0			LSB
FF8AH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
					PTD11	0			
	R				PTD10	0			LSB
FF8BH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
					PTD15	0			
	R				PTD14	0			LSB
FF8CH	CD03	CD02	CD01	CD00	CD03	0			MSB
					CD02	0			Programmable timer 0 compare data (low-order 4 bits)
					CD01	0			
	R/W				CD00	0			LSB
FF8DH	CD07	CD06	CD05	CD04	CD07	0			MSB
					CD06	0			Programmable timer 0 compare data (high-order 4 bits)
					CD05	0			
	R/W				CD04	0			LSB
FF8EH	CD13	CD12	CD11	CD10	CD13	0			MSB
					CD12	0			Programmable timer 1 compare data (low-order 4 bits)
					CD11	0			
	R/W				CD10	0			LSB
FF8FH	CD17	CD16	CD15	CD14	CD17	0			MSB
					CD16	0			Programmable timer 1 compare data (high-order 4 bits)
					CD15	0			
	R/W				CD14	0			LSB

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.9.10.1(c) Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF90H	MOD16_B	EVCNT_B	FCSEL_B	PLPUL_B	MOD16_B	0	16 bits	8 bits	PTM2–3 16-bit mode selection
					EVCNT_B	0	Event ct.	Timer	PTM2 counter mode selection
					FCSEL_B	0	With NR	No NR	PTM2 function selection (for event counter mode)
	R/W				PLPUL_B	0	↑	↓	PTM2 pulse polarity selection (for event counter mode)
FF91H	PTSEL3	PTSEL2	CHSEL_B	PTOUT_B	PTSEL3	0	PWM	Normal	Programmable timer 3 PWM output selection
					PTSEL2	0	PWM	Normal	Programmable timer 2 PWM output selection
					CHSEL_B	0	Timer 3	Timer 2	PTM2–3 TOUT_B output selection
	R/W				PTOUT_B	0	On	Off	PTM2–3 TOUT_B output control
FF92H	PTRST3	PTRUN3	PTRST2	PTRUN2	PTRST3*3	– *2	Reset	Invalid	Programmable timer 3 reset (reload)
					PTRUN3	0	Run	Stop	Programmable timer 3 Run/Stop
	W	R/W	W	R/W	PTRST2*3	– *2	Reset	Invalid	Programmable timer 2 reset (reload)
					PTRUN2	0	Run	Stop	Programmable timer 2 Run/Stop
FF94H	RLD23	RLD22	RLD21	RLD20	RLD23	0			MSB
					RLD22	0			Programmable timer 2 reload data (low-order 4 bits)
	R/W				RLD21	0			
					RLD20	0			LSB
FF95H	RLD27	RLD26	RLD25	RLD24	RLD27	0			MSB
					RLD26	0			Programmable timer 2 reload data (high-order 4 bits)
	R/W				RLD25	0			
					RLD24	0			LSB
FF96H	RLD33	RLD32	RLD31	RLD30	RLD33	0			MSB
					RLD32	0			Programmable timer 3 reload data (low-order 4 bits)
	R/W				RLD31	0			
					RLD30	0			LSB
FF97H	RLD37	RLD36	RLD35	RLD34	RLD37	0			MSB
					RLD36	0			Programmable timer 3 reload data (high-order 4 bits)
	R/W				RLD35	0			
					RLD34	0			LSB
FF98H	PTD23	PTD22	PTD21	PTD20	PTD23	0			MSB
					PTD22	0			Programmable timer 2 data (low-order 4 bits)
	R				PTD21	0			
					PTD20	0			LSB
FF99H	PTD27	PTD26	PTD25	PTD24	PTD27	0			MSB
					PTD26	0			Programmable timer 2 data (high-order 4 bits)
	R				PTD25	0			
					PTD24	0			LSB
FF9AH	PTD33	PTD32	PTD31	PTD30	PTD33	0			MSB
					PTD32	0			Programmable timer 3 data (low-order 4 bits)
	R				PTD31	0			
					PTD30	0			LSB
FF9BH	PTD37	PTD36	PTD35	PTD34	PTD37	0			MSB
					PTD36	0			Programmable timer 3 data (high-order 4 bits)
	R				PTD35	0			
					PTD34	0			LSB
FF9CH	CD23	CD22	CD21	CD20	CD23	0			MSB
					CD22	0			Programmable timer 2 compare data (low-order 4 bits)
	R/W				CD21	0			
					CD20	0			LSB
FF9DH	CD27	CD26	CD25	CD24	CD27	0			MSB
					CD26	0			Programmable timer 2 compare data (high-order 4 bits)
	R/W				CD25	0			
					CD24	0			LSB
FF9EH	CD33	CD32	CD31	CD30	CD33	0			MSB
					CD32	0			Programmable timer 3 compare data (low-order 4 bits)
	R/W				CD31	0			
					CD30	0			LSB
FF9FH	CD37	CD36	CD35	CD34	CD37	0			MSB
					CD36	0			Programmable timer 3 compare data (high-order 4 bits)
	R/W				CD35	0			
					CD34	0			LSB

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.9.10.1(d) Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFA0H	MOD16_C	EVCNT_C	FCSEL_C	PLPUL_C	MOD16_C	0	16 bits	8 bits	PTM4–5 16-bit mode selection
					EVCNT_C	0	Event ct.	Timer	PTM4 counter mode selection
					FCSEL_C	0	With NR	No NR	PTM4 function selection (for event counter mode)
	R/W				PLPUL_C	0	↑	↓	PTM4 pulse polarity selection (for event counter mode)
FFA1H	PTSEL5	PTSEL4	CHSEL_C	PTOUT_C	PTSEL5	0	PWM	Normal	Programmable timer 5 PWM output selection
					PTSEL4	0	PWM	Normal	Programmable timer 4 PWM output selection
					CHSEL_C	0	Timer 5	Timer 4	PTM4–5 TOUT_C output selection
	R/W				PTOUT_C	0	On	Off	PTM4–5 TOUT_C output control
FFA2H	PTRST5	PTRUN5	PTRST4	PTRUN4	PTRST5*3	– *2	Reset	Invalid	Programmable timer 5 reset (reload)
					PTRUN5	0	Run	Stop	Programmable timer 5 Run/Stop
	W	R/W	W	R/W	PTRST4*3	– *2	Reset	Invalid	Programmable timer 4 reset (reload)
					PTRUN4	0	Run	Stop	Programmable timer 4 Run/Stop
FFA4H	RLD43	RLD42	RLD41	RLD40	RLD43	0			MSB
					RLD42	0			Programmable timer 4 reload data (low-order 4 bits)
					RLD41	0			
	R/W				RLD40	0			LSB
FFA5H	RLD47	RLD46	RLD45	RLD44	RLD47	0			MSB
					RLD46	0			Programmable timer 4 reload data (high-order 4 bits)
					RLD45	0			
	R/W				RLD44	0			LSB
FFA6H	RLD53	RLD52	RLD51	RLD50	RLD53	0			MSB
					RLD52	0			Programmable timer 5 reload data (low-order 4 bits)
					RLD51	0			
	R/W				RLD50	0			LSB
FFA7H	RLD57	RLD56	RLD55	RLD54	RLD57	0			MSB
					RLD56	0			Programmable timer 5 reload data (high-order 4 bits)
					RLD55	0			
	R/W				RLD54	0			LSB
FFA8H	PTD43	PTD42	PTD41	PTD40	PTD43	0			MSB
					PTD42	0			Programmable timer 4 data (low-order 4 bits)
					PTD41	0			
	R				PTD40	0			LSB
FFA9H	PTD47	PTD46	PTD45	PTD44	PTD47	0			MSB
					PTD46	0			Programmable timer 4 data (high-order 4 bits)
					PTD45	0			
	R				PTD44	0			LSB
FFAAH	PTD53	PTD52	PTD51	PTD50	PTD53	0			MSB
					PTD52	0			Programmable timer 5 data (low-order 4 bits)
					PTD51	0			
	R				PTD50	0			LSB
FFABH	PTD57	PTD56	PTD55	PTD54	PTD57	0			MSB
					PTD56	0			Programmable timer 5 data (high-order 4 bits)
					PTD55	0			
	R				PTD54	0			LSB
FFACH	CD43	CD42	CD41	CD40	CD43	0			MSB
					CD42	0			Programmable timer 4 compare data (low-order 4 bits)
					CD41	0			
	R/W				CD40	0			LSB
FFADH	CD47	CD46	CD45	CD44	CD47	0			MSB
					CD46	0			Programmable timer 4 compare data (high-order 4 bits)
					CD45	0			
	R/W				CD44	0			LSB
FFAEH	CD53	CD52	CD51	CD50	CD53	0			MSB
					CD52	0			Programmable timer 5 compare data (low-order 4 bits)
					CD51	0			
	R/W				CD50	0			LSB
FFAFH	CD57	CD56	CD55	CD54	CD57	0			MSB
					CD56	0			Programmable timer 5 compare data (high-order 4 bits)
					CD55	0			
	R/W				CD54	0			LSB

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.9.10.1(e) Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFB0H	MOD16_D	EVCNT_D	FCSEL_D	PLPUL_D	MOD16_D	0	16 bits	8 bits	PTM6–7 16-bit mode selection
					EVCNT_D	0	Event ct.	Timer	PTM6 counter mode selection
					FCSEL_D	0	With NR	No NR	PTM6 function selection (for event counter mode)
	R/W				PLPUL_D	0	↑	↓	PTM6 pulse polarity selection (for event counter mode)
FFB1H	PTSEL7	PTSEL6	CHSEL_D	PTOUT_D	PTSEL7	0	PWM	Normal	Programmable timer 7 PWM output selection
					PTSEL6	0	PWM	Normal	Programmable timer 6 PWM output selection
					CHSEL_D	0	Timer 7	Timer 6	PTM6–7 TOUT_D output selection
	R/W				PTOUT_D	0	On	Off	PTM6–7 TOUT_D output control
FFB2H	PTRST7	PTRUN7	PTRST6	PTRUN6	PTRST7*3	– *2	Reset	Invalid	Programmable timer 7 reset (reload)
					PTRUN7	0	Run	Stop	Programmable timer 7 Run/Stop
	W	R/W	W	R/W	PTRST6*3	– *2	Reset	Invalid	Programmable timer 6 reset (reload)
					PTRUN6	0	Run	Stop	Programmable timer 6 Run/Stop
FFB4H	RLD63	RLD62	RLD61	RLD60	RLD63	0			MSB
					RLD62	0			Programmable timer 6 reload data (low-order 4 bits)
	R/W				RLD61	0			
					RLD60	0			LSB
FFB5H	RLD67	RLD66	RLD65	RLD64	RLD67	0			MSB
					RLD66	0			Programmable timer 6 reload data (high-order 4 bits)
	R/W				RLD65	0			
					RLD64	0			LSB
FFB6H	RLD73	RLD72	RLD71	RLD70	RLD73	0			MSB
					RLD72	0			Programmable timer 7 reload data (low-order 4 bits)
	R/W				RLD71	0			
					RLD70	0			LSB
FFB7H	RLD77	RLD76	RLD75	RLD74	RLD77	0			MSB
					RLD76	0			Programmable timer 7 reload data (high-order 4 bits)
	R/W				RLD75	0			
					RLD74	0			LSB
FFB8H	PTD63	PTD62	PTD61	PTD60	PTD63	0			MSB
					PTD62	0			Programmable timer 6 data (low-order 4 bits)
	R				PTD61	0			
					PTD60	0			LSB
FFB9H	PTD67	PTD66	PTD65	PTD64	PTD67	0			MSB
					PTD66	0			Programmable timer 6 data (high-order 4 bits)
	R				PTD65	0			
					PTD64	0			LSB
FFBAH	PTD73	PTD72	PTD71	PTD70	PTD73	0			MSB
					PTD72	0			Programmable timer 7 data (low-order 4 bits)
	R				PTD71	0			
					PTD70	0			LSB
FFBBH	PTD77	PTD76	PTD75	PTD74	PTD77	0			MSB
					PTD76	0			Programmable timer 7 data (high-order 4 bits)
	R				PTD75	0			
					PTD74	0			LSB
FFBCH	CD63	CD62	CD61	CD60	CD63	0			MSB
					CD62	0			Programmable timer 6 compare data (low-order 4 bits)
	R/W				CD61	0			
					CD60	0			LSB
FFBDH	CD67	CD66	CD65	CD64	CD67	0			MSB
					CD66	0			Programmable timer 6 compare data (high-order 4 bits)
	R/W				CD65	0			
					CD64	0			LSB
FFBEH	CD73	CD72	CD71	CD70	CD73	0			MSB
					CD72	0			Programmable timer 7 compare data (low-order 4 bits)
	R/W				CD71	0			
					CD70	0			LSB
FFBFH	CD77	CD76	CD75	CD74	CD77	0			MSB
					CD76	0			Programmable timer 7 compare data (high-order 4 bits)
	R/W				CD75	0			
					CD74	0			LSB

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.9.10.1(f) Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFE2H	General	General	EIPT0	EICTC0	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 underflow)
					EICTC0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 compare match)
FFE3H	General	General	EIPT1	EICTC1	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 underflow)
					EICTC1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 compare match)
FFE4H	General	General	EIPT2	EICTC2	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT2	0	Enable	Mask	Interrupt mask register (Programmable timer 2 underflow)
					EICTC2	0	Enable	Mask	Interrupt mask register (Programmable timer 2 compare match)
FFE5H	General	General	EIPT3	EICTC3	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT3	0	Enable	Mask	Interrupt mask register (Programmable timer 3 underflow)
					EICTC3	0	Enable	Mask	Interrupt mask register (Programmable timer 3 compare match)
FFE6H	General	General	EIPT4	EICTC4	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT4	0	Enable	Mask	Interrupt mask register (Programmable timer 4 underflow)
					EICTC4	0	Enable	Mask	Interrupt mask register (Programmable timer 4 compare match)
FFE7H	General	General	EIPT5	EICTC5	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT5	0	Enable	Mask	Interrupt mask register (Programmable timer 5 underflow)
					EICTC5	0	Enable	Mask	Interrupt mask register (Programmable timer 5 compare match)
FFE8H	General	General	EIPT6	EICTC6	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT6	0	Enable	Mask	Interrupt mask register (Programmable timer 6 underflow)
					EICTC6	0	Enable	Mask	Interrupt mask register (Programmable timer 6 compare match)
FFE9H	General	General	EIPT7	EICTC7	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT7	0	Enable	Mask	Interrupt mask register (Programmable timer 7 underflow)
					EICTC7	0	Enable	Mask	Interrupt mask register (Programmable timer 7 compare match)
FFF2H	0	0	IPT0	ICTC0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT0	0	(W)	(W)	Interrupt factor flag (Programmable timer 0 underflow)
					ICTC0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0 compare match)
FFF3H	0	0	IPT1	ICTC1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1 underflow)
					ICTC1	0	Reset	Invalid	Interrupt factor flag (Programmable timer 1 compare match)
FFF4H	0	0	IPT2	ICTC2	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT2	0	(W)	(W)	Interrupt factor flag (Programmable timer 2 underflow)
					ICTC2	0	Reset	Invalid	Interrupt factor flag (Programmable timer 2 compare match)
FFF5H	0	0	IPT3	ICTC3	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT3	0	(W)	(W)	Interrupt factor flag (Programmable timer 3 underflow)
					ICTC3	0	Reset	Invalid	Interrupt factor flag (Programmable timer 3 compare match)
FFF6H	0	0	IPT4	ICTC4	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT4	0	(W)	(W)	Interrupt factor flag (Programmable timer 4 underflow)
					ICTC4	0	Reset	Invalid	Interrupt factor flag (Programmable timer 4 compare match)
FFF7H	0	0	IPT5	ICTC5	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT5	0	(W)	(W)	Interrupt factor flag (Programmable timer 5 underflow)
					ICTC5	0	Reset	Invalid	Interrupt factor flag (Programmable timer 5 compare match)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.9.10.1(g) Control bits of programmable timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFF8H	0	0	IPT6	ICTC6	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT6	0	(W)	(W)	Interrupt factor flag (Programmable timer 6 underflow)
					ICTC6	0	Reset	Invalid	Interrupt factor flag (Programmable timer 6 compare match)
FFF9H	0	0	IPT7	ICTC7	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT7	0	(W)	(W)	Interrupt factor flag (Programmable timer 7 underflow)
					ICTC7	0	Reset	Invalid	Interrupt factor flag (Programmable timer 7 compare match)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

PTPS00-PTPS03: Timer 0 count clock frequency select register (FF18H)
PTPS10-PTPS13: Timer 1 count clock frequency select register (FF19H)
PTPS20-PTPS23: Timer 2 count clock frequency select register (FF1AH)
PTPS30-PTPS33: Timer 3 count clock frequency select register (FF1BH)
PTPS40-PTPS43: Timer 4 count clock frequency select register (FF1CH)
PTPS50-PTPS53: Timer 5 count clock frequency select register (FF1DH)
PTPS60-PTPS63: Timer 6 count clock frequency select register (FF1EH)
PTPS70-PTPS73: Timer 7 count clock frequency select register (FF1FH)

Selects the count clock frequency for each timer.

Table 4.9.10.2 Selecting count clock frequency

PTPSx3	PTPSx2	PTPSx1	PTPSx0	Timer clock
1	1	1	1	f_{OSC3}
1	1	1	0	f_{OSC3} / 2
1	1	0	1	f_{OSC3} / 4
1	1	0	0	f_{OSC3} / 8
1	0	1	1	f_{OSC3} / 16
1	0	1	0	f_{OSC3} / 32
1	0	0	1	f_{OSC3} / 64
1	0	0	0	f_{OSC3} / 256
0	1	1	1	f_{OSC1} (32 kHz)
0	1	1	0	f_{OSC1} / 2 (16 kHz)
0	1	0	1	f_{OSC1} / 4 (8 kHz)
0	1	0	0	f_{OSC1} / 16 (2 kHz)
0	0	1	1	f_{OSC1} / 32 (1 kHz)
0	0	1	0	f_{OSC1} / 64 (512 Hz)
0	0	0	1	f_{OSC1} / 256 (128 Hz)
0	0	0	0	OFF

The clock manager generates the down-count clock for each timer by dividing the OSC1 or OSC3 clock. Table 4.9.10.2 lists the 15 count clocks that can be generated by the clock manager, and the clock to be used for each timer can be selected using PTPSx0–PTPSx3. At initial reset, the PTPSx register is set to "0H" and the clock supply from the clock manager to the programmable timer is disabled. Before the timer can be run, select a clock to enable the clock supply.
Stop the clock supply to the timers shown below by setting PTPSx to "0H" to reduce current consumption.

- Unused timer
- Timer used as an event counter that inputs an external clock
- Upper 8-bit timer (Timer 1/3/5/7) when the timer unit is used as 16-bit × 1 channel configuration.

At initial reset, these registers are set to "0".

PLPUL_A: Timer 0 pulse polarity select register (FF80H•D0)
PLPUL_B: Timer 2 pulse polarity select register (FF90H•D0)
PLPUL_C: Timer 4 pulse polarity select register (FFA0H•D0)
PLPUL_D: Timer 6 pulse polarity select register (FFB0H•D0)
Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

The count timing in the event counter mode is selected from either the falling edge of the external clock input to the P12, P41, P42 and P43 I/O port terminals or the rising edge. When "0" is written to these registers, the falling edge is selected and when "1" is written, the rising edge is selected.
These registers are effective only when the timer is used in the event counter mode.
At initial reset, these registers are set to "0".

FCSEL_A: Timer 0 function select register (FF80H•D1)
FCSEL_B: Timer 2 function select register (FF90H•D1)
FCSEL_C: Timer 4 function select register (FFA0H•D1)
FCSEL_D: Timer 6 function select register (FFB0H•D1)
Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejector
When "0" is written: Without noise rejector
Reading: Valid

When "1" is written to these registers, the noise rejector is used and counting is done by an external clock (input from P12, P41, P42 or P43) with 0.98 msec* or more pulse width. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz* signal after changing the input level of the I/O port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec* or less.
(*: f_{OSC1} = 32.768 kHz)
When "0" is written to these registers, the noise rejector is not used and the counting is done directly by an external clock input to the P12, P41, P42 or P43 I/O port terminal.
This registers are effective only when the timer is used in the event counter mode.
At initial reset, these registers are set to "0".

EVCNT_A: Timer 0 counter mode select register (FF80H•D2)
EVCNT_B: Timer 2 counter mode select register (FF90H•D2)
EVCNT_C: Timer 4 counter mode select register (FFA0H•D2)
EVCNT_D: Timer 6 counter mode select register (FFB0H•D2)
Selects the counter mode for each timer.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

The counter modes for Timers 0, 2, 4 and 6 are selected from either the event counter mode or timer mode.
When "1" is written to these registers, event counter mode is selected. In this mode, Timers 0, 2, 4 and 6 count the external clock input from the P12, P41, P42 and P43 I/O ports, respectively.
When "0" is written, timer mode is selected. In this mode, the timer count the internal clock selected by the PTPS register.
This selection is effective even when these timer is used in 16-bit timer mode.
At initial reset, these registers are set to "0".

MOD16_A: Timer 0–1 16-bit timer mode select register (FF80H•D3)
MOD16_B: Timer 2–3 16-bit timer mode select register (FF90H•D3)
MOD16_C: Timer 4–5 16-bit timer mode select register (FFA0H•D3)
MOD16_D: Timer 6–7 16-bit timer mode select register (FFB0H•D3)
Selects 8-bit or 16-bit timer mode.

When "1" is written: 16-bit timer mode
When "0" is written: 8-bit timer mode
Reading: Valid

These registers are used to select whether Timers 0 and 1, Timers 2 and 3, Timers 4 and 5, and Timers 6 and 7 are used as two channels of independent 8-bit timers or one channel of combined 16-bit timer. When "0" is written to these registers, the timers are set to 8-bit timer mode. When "1" is written, the timers are set to 16-bit timer mode.
For example, when Timers 0 and 1 are used in 16-bit timer mode, Timer 1 operates with the Timer 0 underflow signal as the count clock (both timer mode or event counter mode). In 16-bit timer mode, the Timer 0 register settings are effective for timer RUN/STOP control and count clock frequency selection (Timer 1 registers are ineffective). However, the PWM output function must be controlled using the Timer 1 control register. The reload data must be preset to Timer 0 and Timer 1 separately using each PTRSTx register. These operations are the same when Timers 2 and 3, Timers 4 and 5 or Timers 6 and 7 are used as a 16-bit timer.
At initial reset, these registers are set to "0".

PTOUT_A: TOUT_A output control register (FF81H•D0)
PTOUT_B: TOUT_B output control register (FF91H•D0)
PTOUT_C: TOUT_C output control register (FFA1H•D0)
PTOUT_D: TOUT_D output control register (FFB1H•D0)
Controls TOUT signal outputs.

When "1" is written: TOUT output On
When "0" is written: TOUT output Off
Reading: Valid

When "1" is written to the register, the corresponding TOUT_A/TOUT_B/TOUT_C/TOUT_D signal is output from the P13/P31/P32/P33 terminal. When TOUT output is enabled, the I/O port is automatically set to output mode and it outputs the TOUT signal sent from the timer. The I/O control register (IOC13/IOC31/IOC32/IOC33) and the data register (P13/P31/P32/P33) are ineffective. When this register is set to "0", the I/O port control registers become effective.
At initial reset, these registers are set to "0".

CHSEL_A: TOUT_A output select register (FF81H•D1)
CHSEL_B: TOUT_B output select register (FF91H•D1)
CHSEL_C: TOUT_C output select register (FFA1H•D1)
CHSEL_D: TOUT_D output select register (FFB1H•D1)
Selects the timer used for TOUT signal output.

When "1" is written: Low-order Timer (Timers 0/2/4/6)
When "0" is written: High-order Timer (Timers 1/3/5/7)
Reading: Valid

These registers are used to select whether the low-order timer (Timer 0/2/4/6) output is used as the TOUT signal or the high-order timer (Timer 1/3/5/7) output is used. When "0" is written to the register, the low-order timer output is selected. When "1" is written, the high-order timer output is selected.
In 16-bit timer mode, the high-order timer output is always selected regardless of how these registers are set.
At initial reset, these registers are set to "0".

PTSEL0: Timer 0 PWM mode select register (FF81H•D2)
PTSEL1: Timer 1 PWM mode select register (FF81H•D3)
PTSEL2: Timer 2 PWM mode select register (FF91H•D2)
PTSEL3: Timer 3 PWM mode select register (FF91H•D3)
PTSEL4: Timer 4 PWM mode select register (FFA1H•D2)
PTSEL5: Timer 5 PWM mode select register (FFA1H•D3)
PTSEL6: Timer 6 PWM mode select register (FFB1H•D2)
PTSEL7: Timer 7 PWM mode select register (FFB1H•D3)
Sets Timer x for PWM output.

When "1" is written: PWM output
When "0" is written: Normal output
Reading: Valid

When "1" is written to the PTSELx, the compare data register becomes effective and PWM waveform is generated using the underflow and compare match signals. When "0" is written, the timer outputs the normal clock generated from the underflow signal.
In 16-bit timer mode, the PTSEL register for the low-order timer (Timer 0/2/4/6) is ineffective.
At initial reset, these registers are set to "0".

PTRUN0: Timer 0 RUN/STOP control register (FF82H•D0)
PTRUN1: Timer 1 RUN/STOP control register (FF82H•D2)
PTRUN2: Timer 2 RUN/STOP control register (FF92H•D0)
PTRUN3: Timer 3 RUN/STOP control register (FF92H•D2)
PTRUN4: Timer 4 RUN/STOP control register (FFA2H•D0)
PTRUN5: Timer 5 RUN/STOP control register (FFA2H•D2)
PTRUN6: Timer 6 RUN/STOP control register (FFB2H•D0)
PTRUN7: Timer 7 RUN/STOP control register (FFB2H•D2)
Controls the RUN/STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter in Timer x starts counting down by writing "1" to the PTRUNx register and stops by writing "0". In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.
In 16-bit timer mode, the PTRUN register for the high-order timer (Timer 1/3/5/7) is ineffective.
At initial reset, these registers are set to "0".

PTRST0: Timer 0 reset (reload) (FF82H•D1)
PTRST1: Timer 1 reset (reload) (FF82H•D3)
PTRST2: Timer 2 reset (reload) (FF92H•D1)
PTRST3: Timer 3 reset (reload) (FF92H•D3)
PTRST4: Timer 4 reset (reload) (FFA2H•D1)
PTRST5: Timer 5 reset (reload) (FFA2H•D3)
PTRST6: Timer 6 reset (reload) (FFB2H•D1)
PTRST7: Timer 7 reset (reload) (FFB2H•D3)
Resets the timer and preset reload data to the counter.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PTRSTx, the reload data in the reload register RLDx0–RLDx7 is preset to the counter in timer x. When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained.
No operation results when "0" is written.

The PTRSTx registers are all effective even in 16-bit timer mode, and reload data must be preset to both the high-order timer (Timer 1/3/5/7) and the low-order timer (Timer 0/2/4/6) separately.
Since these bits are exclusively for writing, always set to "0" during reading.

RLD00–RLD07: Timer 0 reload data register (FF84H, FF85H)
RLD10–RLD17: Timer 1 reload data register (FF86H, FF87H)
RLD20–RLD27: Timer 2 reload data register (FF94H, FF95H)
RLD30–RLD37: Timer 3 reload data register (FF96H, FF97H)
RLD40–RLD47: Timer 4 reload data register (FFA4H, FFA5H)
RLD50–RLD57: Timer 5 reload data register (FFA6H, FFA7H)
RLD60–RLD67: Timer 6 reload data register (FFB4H, FFB5H)
RLD70–RLD77: Timer 7 reload data register (FFB6H, FFB7H)

Sets the initial value for the counter.
The reload data written in these registers are loaded to the respective counters. The counter counts down using the data as the initial value for counting.
Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRSTx register, or when counter underflow occurs.
At initial reset, these registers are set to "00H".

PTD00–PTD07: Timer 0 counter data (FF88H, FF89H)
PTD10–PTD17: Timer 1 counter data (FF8AH, FF8BH)
PTD20–PTD27: Timer 2 counter data (FF98H, FF99H)
PTD30–PTD37: Timer 3 counter data (FF9AH, FF9BH)
PTD40–PTD47: Timer 4 counter data (FFA8H, FFA9H)
PTD50–PTD57: Timer 5 counter data (FFAAH, FFABH)
PTD60–PTD67: Timer 6 counter data (FFB8H, FFB9H)
PTD70–PTD77: Timer 7 counter data (FFBAH, FFBBH)

Count data in the programmable timer can be read from these latches.
The low-order 4 bits of the count data in Timer x can be read from PTDx0–PTDx3, and the high-order data can be read from PTDx4–PTDx7. Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first. In 16-bit timer mode, the high-order 12 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.
Since these latches are exclusively for reading, the writing operation is invalid.
At initial reset, these counter data are set to "00H".

CD00–CD07: Timer 0 compare data register (FF8CH, FF8DH)
CD10–CD17: Timer 1 compare data register (FF8EH, FF8FH)
CD20–CD27: Timer 2 compare data register (FF9CH, FF9DH)
CD30–CD37: Timer 3 compare data register (FF9EH, FF9FH)
CD40–CD47: Timer 4 compare data register (FFACH, FFADH)
CD50–CD57: Timer 5 compare data register (FFAEH, FFAFH)
CD60–CD67: Timer 6 compare data register (FFBCH, FFBDH)
CD70–CD77: Timer 7 compare data register (FFBEH, FFBFH)

Sets the compare data for PWM output.
When the timer is set to PWM mode, the compare data set in this register is compared with the counter data and outputs the compare match signal if they are matched. The compare match signal is used for generating an interrupt and controlling the duty ratio of the PWM waveform.
At initial reset, these registers are set to "00H".

EIPT0, EICTC0: Timer 0 interrupt mask registers (FFE2H•D1, D0)
EIPT1, EICTC1: Timer 1 interrupt mask registers (FFE3H•D1, D0)
EIPT2, EICTC2: Timer 2 interrupt mask registers (FFE4H•D1, D0)
EIPT3, EICTC3: Timer 3 interrupt mask registers (FFE5H•D1, D0)
EIPT4, EICTC4: Timer 4 interrupt mask registers (FFE6H•D1, D0)
EIPT5, EICTC5: Timer 5 interrupt mask registers (FFE7H•D1, D0)
EIPT6, EICTC6: Timer 6 interrupt mask registers (FFE8H•D1, D0)
EIPT7, EICTC7: Timer 7 interrupt mask registers (FFE9H•D1, D0)
These registers are used to select whether to mask the programmable timer interrupt or not.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

EIPTx and EICTCx are the interrupt mask registers that respectively correspond to the counter underflow and compare match interrupt factors. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, these registers are set to "0".

IPT0, ICTC0: Timer 0 interrupt factor flags (FFF2H•D1, D0)
IPT1, ICTC1: Timer 1 interrupt factor flags (FFF3H•D1, D0)
IPT2, ICTC2: Timer 2 interrupt factor flags (FFF4H•D1, D0)
IPT3, ICTC3: Timer 3 interrupt factor flags (FFF5H•D1, D0)
IPT4, ICTC4: Timer 4 interrupt factor flags (FFF6H•D1, D0)
IPT5, ICTC5: Timer 5 interrupt factor flags (FFF7H•D1, D0)
IPT6, ICTC6: Timer 6 interrupt factor flags (FFF8H•D1, D0)
IPT7, ICTC7: Timer 7 interrupt factor flags (FFF9H•D1, D0)
These flags indicate the status of the programmable timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

IPTx and ICTCx are the interrupt factor flags that respectively correspond to the interrupts for counter underflow and compare match, and are set to "1" by generation of each factor.
The underflow interrupt factor is generated at the point where the counter underflows.
The compare match interrupt factor is generated if the counter data and the compare data are matched when the timer is set in the PWM mode.
The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by an underflow and compare match of the corresponding counter.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.9.11 Programming notes

(1) When reading counter data, be sure to read the low-order 4 bits (PTDx0–PTDx3) first. The high-order 4 bits (PTDx4–PTDx7) are latched when the low-order 4 bits are read and they are held until the next reading of the low-order 4 bits. In 16-bit timer mode, the high-order 12 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.
When the CPU is running with the OSC1 clock and the programmable timer is running with the OSC3 clock, stop the timer before reading the counter data to read the proper data.

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.

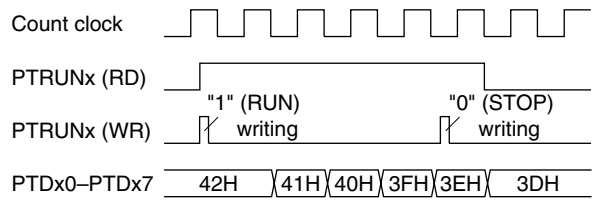


Fig. 4.9.11.1 Timing chart for RUN/STOP control (timer mode)

In event counter mode, the timer starts counting at the first event clock.

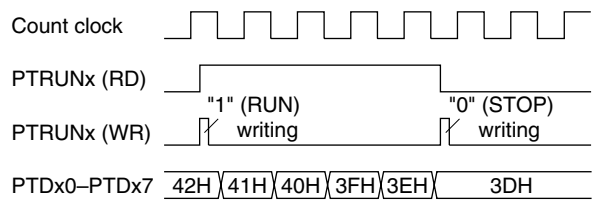


Fig. 4.9.11.2 Timing chart for RUN/STOP control (event counter mode)

(3) Since the TOUT_A–TOUT_D signals are generated asynchronously from the PTOUT_A–PTOUT_D registers, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the off state.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(6) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

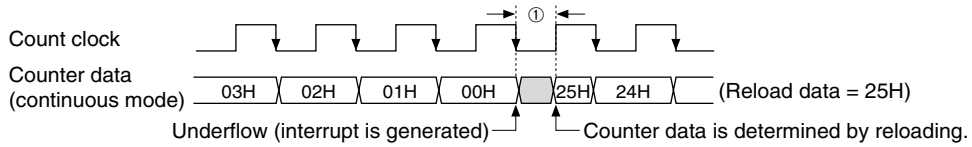


Fig. 4.9.11.3 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

(7) The programmable timer count clock does not synch with the CPU clock. Therefore, the correct value may not be obtained depending on the count data read and count-up timings. To avoid this problem, the programmable timer count data should be read by one of the procedures shown below.

- Read the count data twice and verify if there is any difference between them.
- Temporarily stop the programmable timer when the counter data is read to obtain proper data.

4.10 Serial Interface

4.10.1 Configuration of serial interface

The S1C63632 has a built-in 8-bit clock synchronous type serial interface.
The CPU, via the 8-bit shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8-bit shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of seven types of master mode (internal clock mode: when the S1C63632 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the S1C63632 is to be the slave for serial input/output).
The configuration of the serial interface is shown in Figure 4.10.1.1.

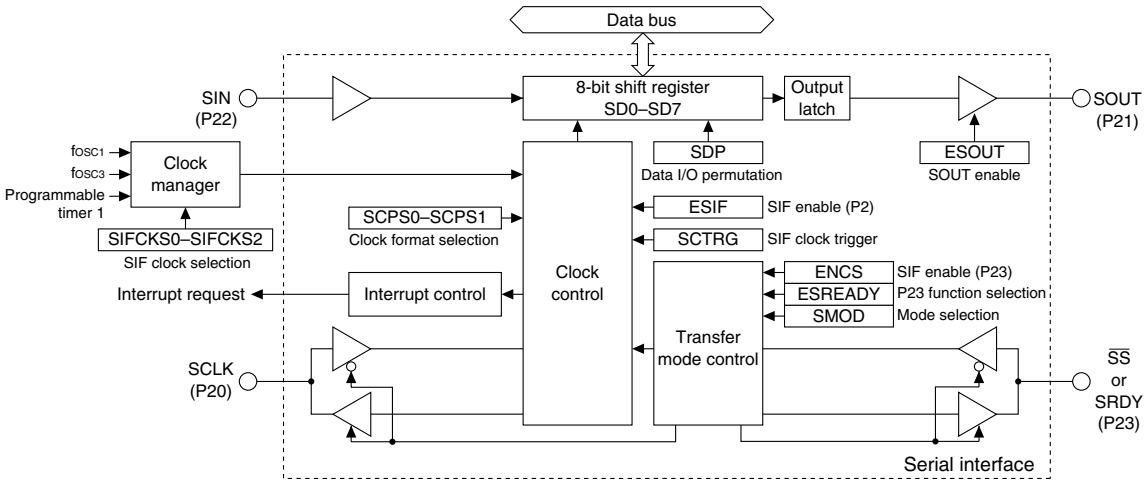


Fig. 4.10.1.1 Configuration of serial interface

4.10.2 Serial interface terminals

The following shows the terminals used in the serial interface and their functions:

SCLK (P20)

Inputs or outputs the serial clock. By writing "1" to the ESIF register to enable the serial interface, the P20 terminal is switched to the SCLK terminal. In master mode, the SCLK terminal is configured for output and it outputs the synchronous clock generated in the IC during data transfer. In slave mode, the SCLK terminal inputs the synchronous clock output by the external master device.

SIN (P22)

Inputs serial data. By writing "1" to the ESIF register to enable the serial interface, the P22 terminal is switched to the SIN terminal.

SOUT (P21)

Outputs serial data. By default, the SOUT terminal is not enabled even if "1" is written to the ESIF register. When using the SOUT output, write "1" to the ESOUT register.
If serial input only is required, the P21 terminal can be used as an I/O port terminal.

SRDY (P23)

In slave mode, this terminal outputs the SRDY signal to the master device to indicate that the serial interface is ready to transfer. By default, the SRDY terminal is not enabled even if the serial interface is set to slave mode. When using the SRDY output in slave mode, write "1" to the ENCS and ESREADY registers.

$\overline{SS}$ (P23)

Inputs the $\overline{SS}$ (Slave Select) signal when the S1C63632 is used as an SPI slave device. When using the $\overline{SS}$ input, write "1" to ENCS and write "0" to ESREADY.

The serial interface input/output ports are shared with the I/O port (P20–P23), and they are configured to the I/O port terminals at initial reset. When using these terminals for the serial interface, switch the function with software as described above. At least ESIF must be set to 1.
The switch operation automatically sets the input/output direction of the terminals. It is not necessary to set the I/O port control registers. The I/O control registers and data registers of the I/O ports can be used as general-purpose registers that do not affect the terminal status. However, the pull-up control registers and input interface select registers of the I/O ports are effective when they are used for the serial inputs.

4.10.3 Mask option

Since the input/output terminals of the serial interface are shared with the I/O ports (P20–P23), the mask option that selects the terminal specification for the I/O port is also applied to the serial interface terminals.

Output specification

The output specification of the SOUT, SCLK (in master mode) and SRDY (in slave mode) terminals that are used as the serial interface outputs is respectively selected by the mask options for P21, P20 and P23. Either complementary output or P-channel open drain output can be selected as the output specification. However, when P-channel open drain output is selected, do not apply voltage exceeding the power supply voltage to the terminal.

Pull-down resistor

The pull-down resistor for the SIN, SCLK (in slave mode) and $\overline{SS}$ (in SPI slave mode) terminals that are used as inputs can be incorporated by the mask options for P22, P20 and P23. When the pull-down resistor is not used, take care that a floating status does not occur.
When a pull-down resistor is incorporated at the serial input terminal, the pull-down resistor should be enabled/disabled using the pull-down control register of the I/O port.

SIN terminal: PUL22 register
SCLK terminal: PUL20 register
$\overline{SS}$ terminal: PUL23 register

Refer to Section 4.5, "I/O Ports", for controlling the pull-down resistors.

4.10.4 Operating mode of serial interface

The serial interface supports three operating modes: master mode, slave mode and SPI slave mode.

Master mode

Master mode is provided to use the S1C63632 as the master device for serial transfer. In this mode, the serial interface uses the internal clock supplied from the clock manager as the synchronous clock for serial transfer. The synchronous clock is also output from the SCLK (P20) terminal to the slave device. The ready signal sent from the slave device should be input through an I/O port (in input mode) and it should be read with software to control data transfer.
The S1C63632 set to master mode is also used as an SPI master device. The $\overline{SS}$ (Slave Select) signal should be output by controlling an I/O port (in output mode) with software.

Slave mode

Slave mode is provided to use the S1C63632 as a slave device for serial transfer. In this mode, the serial interface inputs the synchronous clock that is sent by the external master device from the SCLK terminal to perform serial transfer. For the master device to control data transfer, the serial interface can output a ready signal indicating that it is ready to transfer from the SRDY terminal by hardware control.

SPI slave mode

SPI slave mode is provided to use the S1C63632 as an SPI slave device. In this mode, the serial interface inputs the synchronous clock that is sent by the external master device from the SCLK terminal to perform serial transfer. The SPI master device outputs the $\overline{SS}$ (Slave Select) signal to select a slave device. SPI slave mode supports the $\overline{SS}$ signal input.

Sample basic serial connection diagrams are shown in Figure 4.10.4.1.

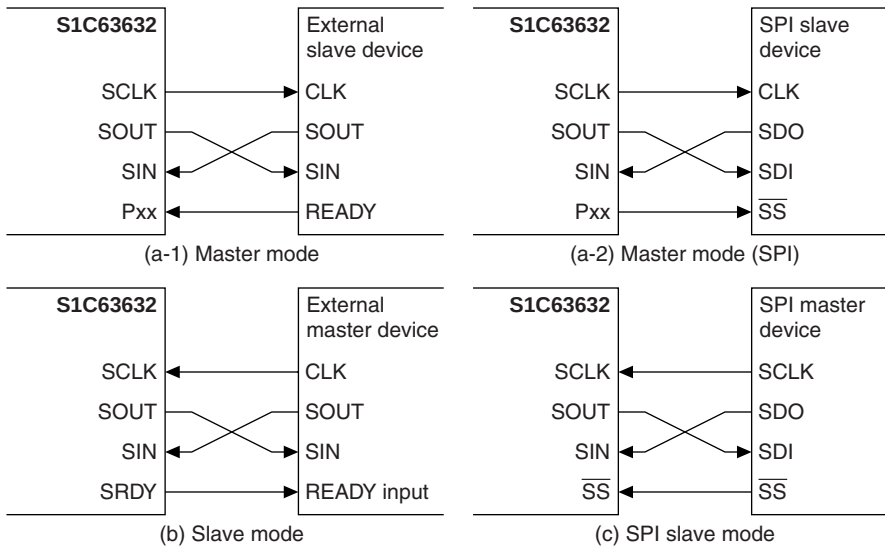


Figure 4.10.4.1 Sample basic connection of serial input/output terminals

The SMOD, ENCS and ESREADY registers are used for setting the mode.

Master mode: SMOD = "1", ENCS = "0", ESREADY = "0"
Slave mode: SMOD = "0", ENCS = "1", ESREADY = "1"
SPI slave mode: SMOD = "0", ENCS = "1", ESREADY = "0"

Table 4.10.4.1 lists the combination of mode settings and used terminal configurations.

Table 4.10.4.1 Mode settings and configurations of serial interface terminals

ESIF	SMOD	ENCS	ESREADY	ESOUT	Mode	P20 terminal	P21 terminal	P22 terminal	P23 terminal
1	1	1	1	*	Master mode	Prohibited			
1	1	*	0	1		SCLK (O)	SOUT (O)	SIN (I)	P23 (I/O)
1	1	0	1	1		SCLK (O)	SOUT (O)	SIN (I)	P23 (I/O)
1	1	*	0	0		SCLK (O)	P21 (I/O)	SIN (I)	P23 (I/O)
1	1	0	1	0		SCLK (O)	P21 (I/O)	SIN (I)	P23 (I/O)
1	0	1	1	1	Slave mode	SCLK (I)	SOUT (O)	SIN (I)	SRDY (O)
1	0	1	1	0		SCLK (I)	P21 (I/O)	SIN (I)	SRDY (O)
1	0	0	*	1		SCLK (I)	SOUT (O)	SIN (I)	P23 (I/O)
1	0	0	*	0		SCLK (I)	P21 (I/O)	SIN (I)	P23 (I/O)
1	0	1	0	1	SPI slave mode	SCLK (I)	SOUT (O)	SIN (I)	$\overline{SS}$ (I)
1	0	1	0	0		SCLK (I)	P21 (I/O)	SIN (I)	$\overline{SS}$ (I)
0	*	*	*	*	Serial I/F not used	P20 (I/O)	P21 (I/O)	P22 (I/O)	P23 (I/O)

4.10.5 Setting synchronous clock

Controlling clock manager

When the serial interface is used in master mode, it uses the internal clock supplied from the clock manager as the synchronous clock for serial transfer. The clock manager generates six serial interface clocks by dividing the OSC1 or OSC3 clock. The synchronous clock used in master mode can be selected from seven types (the above six clocks and the programmable timer 1 output clock). Use the SIFCKS0–SIFCKS2 register to select one of them as shown in Table 4.10.5.1.

Table 4.10.5.1 Serial interface clock frequencies

SIFCKS2	SIFCKS1	SIFCKS0	SIF clock (master mode)
1	1	1	f_{OSC3} / 4 *
1	1	0	f_{OSC3} / 2 *
1	0	1	f_{OSC3} / 1 *
1	0	0	Programmable timer 1 *
0	1	1	f_{OSC1} / 4 (8 kHz)
0	1	0	f_{OSC1} / 2 (16 kHz)
0	0	1	f_{OSC1} / 1 (32 kHz)
0	0	0	Off (slave mode) *

f_{OSC1}: OSC1 oscillation frequency. ( ) indicates the frequency when f_{OSC1} = 32 kHz.
f_{OSC3}: OSC3 oscillation frequency
* The maximum clock frequency is limited to 1 MHz.

When programmable timer 1 is selected, the programmable timer 1 underflow signal is divided by 2 before it is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.9, "Programmable Timer" for controlling the programmable timer.

Fix SIFCKS0–SIFCKS2 at "000B" in slave mode.
At initial reset, "internal clock Off (slave mode)" is selected.

Selecting the synchronous clock format

The format (polarity and phase) of the synchronous clock for the serial interface can be configured using the SCPS0–SCPS1 register.

Table 4.10.5.2 Configuration of synchronous clock format

SCPS1	SCPS0	Polarity	Phase
1	1	Negative ($\overline{SCLK}$)	Rising edge (⌐)
1	0	Negative ($\overline{SCLK}$)	Falling edge (¬)
0	1	Positive (SCLK)	Falling edge (¬)
0	0	Positive (SCLK)	Rising edge (⌐)

At initial reset, the clock polarity is set to positive and the phase is set to the rising edge.
See Figure 4.10.6.2 for the data transfer timings by the synchronous clock format selected.

4.10.6 Data input/output and interrupt function

The serial interface of S1C63632 can input/output data via the internal 8-bit shift register. The shift register operates by synchronizing with either the synchronous clock output from the SCLK (P20) terminal (master mode), or the synchronous clock input to the SCLK (P20) terminal (slave mode).
The serial interface generates an interrupt on completion of the 8-bit serial data input/output. Detection of serial data input/output is done by counting of the synchronous clock SCLK; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates an interrupt.
The serial data input/output procedure is explained below:

Serial data output procedure and interrupt

The S1C63632 serial interface is capable of outputting parallel data as serial data, in units of 8 bits. By setting the parallel data to the data registers SD0–SD3 and SD4–SD7 and writing "1" to SCTRG bit, it synchronizes with the synchronous clock and the serial data is output to the SOUT (P21) terminal. The synchronous clock used here is as follows: in master mode, internal clock which is output to the SCLK (P20) terminal while in slave mode, external clock which is input from the SCLK (P20) terminal. Shift timing of serial data is as follows:

- ***When positive polarity (SCPS1 = "0") is selected for the synchronous clock:***
  The serial data output to the SOUT (P21) terminal changes at the rising edge of the clock input or output from/to the SCLK (P20) terminal. The data in the shift register is shifted at the rising edge of the SCLK signal when the SCPS0 register is "0" or at the falling edge of the SCLK signal when the SCPS0 register is "1".

- ***When negative polarity (SCPS1 = "1") is selected for the synchronous clock:***
  The serial data output to the SOUT (P21) terminal changes at the falling edge of the clock input or output from/to the $\overline{\text{SCLK}}$ (P20) terminal. The data in the shift register is shifted at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "0" or at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "1".

When the output of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and an interrupt occurs. Moreover, the interrupt can be masked by the interrupt mask register EISIF. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after output of the 8-bit data.

Serial data input procedure and interrupt

The S1C63632 serial interface is capable of inputting serial data as parallel data, in units of 8 bits. The serial data is input from the SIN (P22) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8-bit shift register. The synchronous clock used here is the internal clock in master mode or the external clock in slave mode.
Shift timing of serial data is as follows:

- ***When positive polarity (SCPS1 = "0") is selected for the synchronous clock:***
  The serial data is read into the built-in shift register at the rising edge of the SCLK signal when the SCPS0 register is "0" or at the falling edge of the SCLK signal when the SCPS0 register is "1". The shift register is sequentially shifted as the data is fetched.
- ***When negative polarity (SCPS1 = "1") is selected for the synchronous clock:***
  The serial data is read into the built-in shift register at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "0" or at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "1". The shift register is sequentially shifted as the data is fetched.

When the input of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and an interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after input of the 8-bit data.
The data input in the shift register can be read from data registers SD0–SD7 by software.

Serial data input/output permutation

The S1C63632 allows the input/output permutation of serial data to be selected by the SDP register as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.10.6.1. The SDP register should be set before setting data to SD0–SD7.

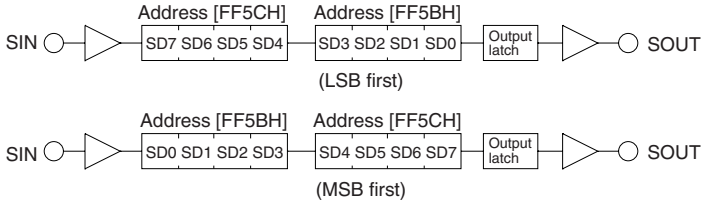


Fig. 4.10.6.1 Serial data input/output permutation

SRDY signal

When the S1C63632 serial interface is used in the slave mode, the SRDY signal is used to indicate whether the internal serial interface is ready to transmit or receive data for the master side (external) serial device. The SRDY signal is output from the SRDY (P23) terminal. When using the SRDY output in slave mode, write "1" to the ENCS and ESREADY registers (this signal cannot be used in SPI slave mode).

Output timing of SRDY signal is as follows:

- ***When positive polarity (SCPS1 = "0") is selected for the synchronous clock:***
  The SRDY signal goes "1" (high) when the S1C63632 serial interface is ready to transmit or receive data; normally, it is at "0" (low).
  The SRDY signal changes from "0" to "1" immediately after "1" is written to SCTRG and returns from "1" to "0" when "1" is input to the SCLK (P20) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the SRDY signal returns to "0".

- ***When negative polarity (SCPS1 = "1") is selected for the synchronous clock:***
  The $\overline{\text{SRDY}}$ signal goes "0" (low) when the S1C63632 serial interface is ready to transmit or receive data; normally, it is at "1" (high).
  The $\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to the $\overline{\text{SCLK}}$ (P20) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".

Timing chart

The S1C63632 serial interface timing charts are shown in Figures 4.10.6.2 .

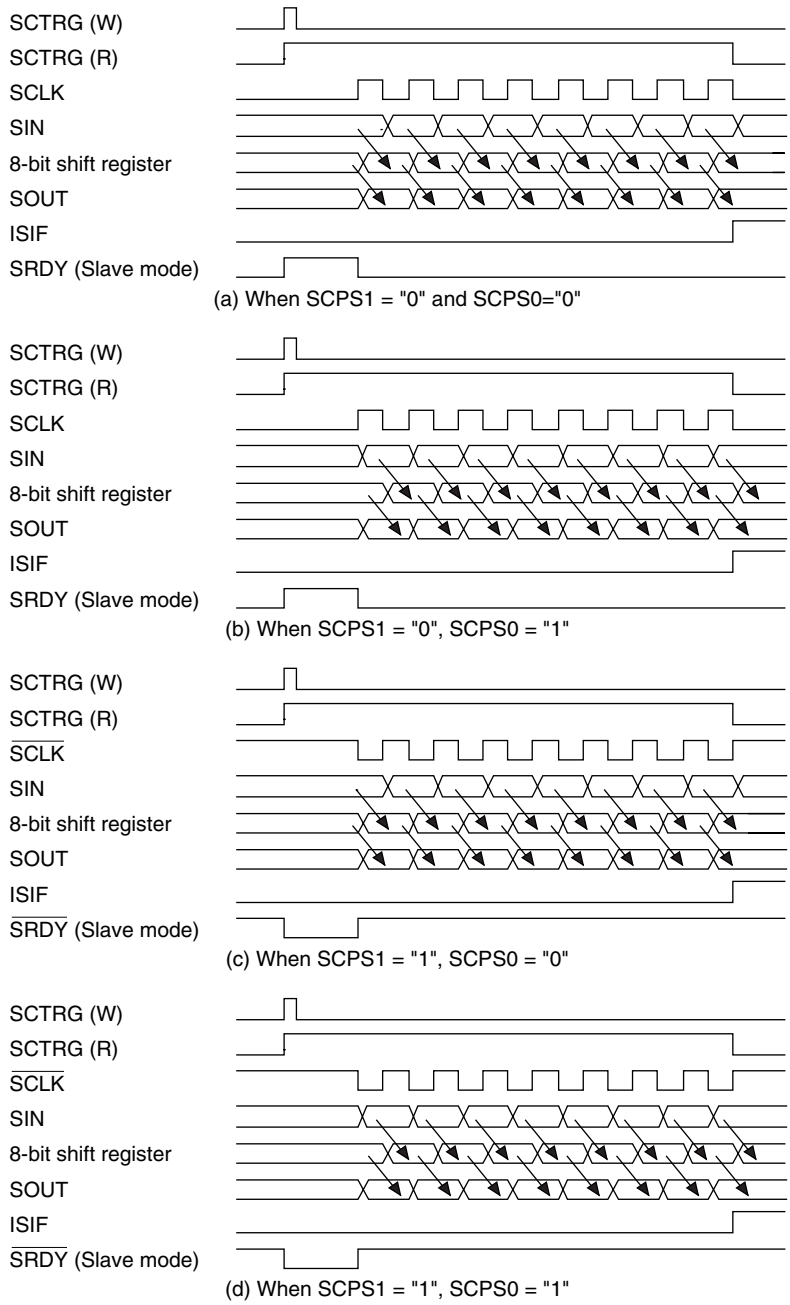


Fig. 4.10.6.2 Serial interface timing chart

4.10.7 Data transfer in SPI mode

The serial interface supports serial data transfer in SPI mode.
This mode has the same serial master and slave functions and control method except that the SRDY output cannot be used when P23 is configured to the $\overline{SS}$ terminal. Refer to Section 4.10.4, "Operating mode of serial interface", and Section 4.10.6, "Data input/output and interrupt function", for these common descriptions.

SPI slave device

When using the S1C63632 as an SPI slave device, set the serial interface to SPI slave mode.

ESIF = "1", SMOD = "0", ENCS = "1", ESREADY = "0", ESOUT = "1" (when SOUT is used)

The P23 terminal functions as the $\overline{SS}$ (Slave Select) signal input terminal.
To perform data transfer in this mode, write "1" to SCTRG to enable the serial interface to transmit/receive data the same as the slave mode described above. The serial interface starts data transfer when the external master device outputs the synchronous clock to the SCLK terminal after it asserts the slave select signal (set to low) input to the $\overline{SS}$ (P23) terminal. The external device must hold the $\overline{SS}$ signal (P23 terminal) active while data is being transferred. When the $\overline{SS}$ signal is inactive, the serial interface does not start data transfer even if the synchronous clock is input to the SCLK terminal.

SPI master device

When using the S1C63632 as an SPI master device, set the serial interface to master mode.

ESIF = "1", SMOD = "1", ENCS = "0", ESREADY = "0", ESOUT = "1" (when SOUT is used)

The $\overline{SS}$ signal output terminal is not available in master mode, set an I/O port to output mode and use it as the $\overline{SS}$ signal output terminal. The $\overline{SS}$ signal must be set to low before writing "1" to SCTRG and hold that active level while data is being transferred. After 8-bit data is transmitted/received, set the $\overline{SS}$ signal to high.

Timing chart

The data transfer timing chart in SPI mode is shown in Figures 4.10.7.1 .

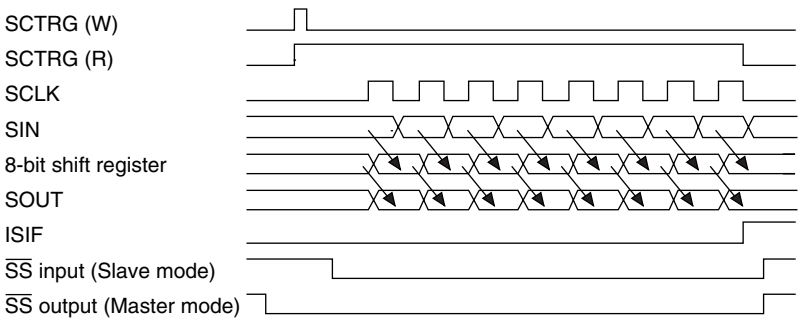


Figure 4.10.7.1 Timing chart in SPI mode (when SCPS1 = SCPS0 = "0")

Notes:
- *The S1C63632 serial interface does not have a transmit buffer and a receive buffer, therefore, data transfer must be processed in every one-byte transfer. The interrupt factor flag is set after a transfer for one byte has been completed. A start of data transfer from/to the SPI device cannot be used as a trigger to start the interrupt handler.*
- *If the $\overline{SS}$ signal becomes inactive during data transfer in SPI slave mode or if the master device outputs the SCLK signal before it asserts the $\overline{SS}$ signal, the serial interface cannot transmit/receive data normally.*

4.10.8 I/O memory of serial interface

Table 4.10.8.1 shows the I/O addresses and the control bits for the serial interface.

Table 4.10.8.1 Control bits of serial interface

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF14H	0	SIFCKS2	SIFCKS1	SIFCKS0	0 *3	– *2			Unused
					SIFCKS2	0			Serial I/F clock frequency selection [SIFCKS2–0] 0: Frequency Off/External fOSC1; 1: fOSC1/2; 2: fOSC1/4; 4: PT1; 5: fOSC3; 6: fOSC3/2; 7: fOSC3/4
					SIFCKS1	0			
	R	R/W			SIFCKS0	0			
FF2AH	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-down control register SS pull-down control register when SIF (slave, SS) is used functions as a general-purpose register when SIF (slave, SRDY) or FOUT is used
					PUL22	1	On	Off	P22 pull-down control register SIN pull-down control register when SIF is used
					PUL21	1	On	Off	P21 pull-down control register functions as a general-purpose register when SIF (SOUT) is used
	R/W				PUL20	1	On	Off	P20 pull-down control register SCLK (I) pull-down control register when SIF (slave) is used functions as a general-purpose register when SIF (master) is used
FF2BH	SMT23	SMT22	SMT21	SMT20	SMT23	1	Schmitt	CMOS	P23 input interface level select register SS input I/F level select register when SIF (slave, SS) is used functions as a general-purpose register when SIF (slave, SRDY) or FOUT is used
					SMT22	1	Schmitt	CMOS	P22 input interface level select register SIN input interface level select register when SIF is used
					SMT21	1	Schmitt	CMOS	P21 input interface level select register functions as a general-purpose register when SIF (SOUT) is used
	R/W				SMT20	1	Schmitt	CMOS	P20 input interface level select register SCLK (I) input I/F level select register when SIF (slave) is used functions as a general-purpose register when SIF (master) is used
FF58H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R	R/W					Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P2 port function selection)
FF59H	SCPS1	SCPS0	SDP	SMOD	SCPS1	0			Serial I/F clock format selection [SCPS1, 0] 0: Polarity P, phase ↓; 1: P, ↑; 2: N, ↓; 3: N, ↑
					SCPS0	0	↓	↑	
	R/W				SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
					SMOD	0	Master	Slave	Serial I/F mode selection
FF5AH	0	0	ESREADY	ENCS	0 *3	– *2			Unused
					0 *3	– *2			Unused
					ESREADY	0	SRDY	SS	P23 port function selection (ESREADY, ENCS): x,0: Slave (SMOD=0) I/O, Master (SMOD=1) I/O; 0,1: SS, SS; 1,1: SRDY, Prohibited
	R		R/W		ENCS	0	SIF	I/O	Serial I/F enable (P23 function selection)
FF5BH	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
					SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					SD1	– *2	High	Low	
	R/W				SD0	– *2	High	Low	LSB
FF5CH	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
					SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					SD5	– *2	High	Low	
	R/W				SD4	– *2	High	Low	LSB
FFEAH	General	General	General	EISIF	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
FFFAH	General	General	General	ISIF	General	0	(R)	(R)	General-purpose register
					General	0	Yes	No	General-purpose register
					General	0	(W)	(W)	General-purpose register
	R/W				ISIF	0	Reset	Invalid	Interrupt factor flag (Serial interface)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

SIFCKS0–SIFCKS2: Serial interface clock frequency select register (FF14H•D0–D2)
Selects the synchronous clock frequency in master mode.

Table 4.10.8.2 Serial interface clock frequencies

SIFCKS2	SIFCKS1	SIFCKS0	SIF clock (master mode)
1	1	1	f_{OSC3} / 4 *
1	1	0	f_{OSC3} / 2 *
1	0	1	f_{OSC3} / 1 *
1	0	0	Programmable timer 1 *
0	1	1	f_{OSC1} / 4 (8 kHz)
0	1	0	f_{OSC1} / 2 (16 kHz)
0	0	1	f_{OSC1} / 1 (32 kHz)
0	0	0	Off (slave mode) *

f_{OSC1}: OSC1 oscillation frequency. ( ) indicates the frequency when f_{OSC1} = 32 kHz.
f_{OSC3}: OSC3 oscillation frequency
* The maximum clock frequency is limited to 1 MHz.

When programmable timer 1 is selected, the programmable timer 1 underflow signal is divided by 2 before it is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.9, "Programmable Timer" for controlling the programmable timer.
Fix at "000B" in slave mode.
At initial reset, this register is set to "000B".

PUL20: SCLK (P20) pull-down control register (FF2AH•D0)
PUL22: SIN(P22) pull-down control register (FF2AH•D2)
PUL23: $\overline{SS}$ (P23) pull-down control register (FF2AH•D3)
Enables the pull-down of the SIN, SCLK (in slave mode) and $\overline{SS}$ (in SPI slave mode) terminals.

When "1" is written: Pull-down On
When "0" is written: Pull-down Off
Reading: Valid

Enables or disables the pull-down resistors built into the SIN (P22), SCLK (P20) and $\overline{SS}$ (P23) terminals. (Pull-down resistor is only built in the port selected by mask option.)
The SCLK and $\overline{SS}$ pull-down resistors are effective only in slave mode or SPI slave mode. In master mode, the PUL20 and PUL23 registers can be used as general purpose registers.
At initial reset, these registers are set to "1" and pull-down goes on.

SMT20: SCLK (P20) input interface level select register (FF2BH•D0)
SMT22: SIN (P22) input interface level select register (FF2BH•D2)
SMT23: $\overline{SS}$ (P23) input interface level select register (FF2BH•D3)
Selects the input interface level of the SIN, SCLK (in slave mode) and $\overline{SS}$ (in SPI slave mode) terminals.

When "1" is written: CMOS Schmitt level
When "0" is written: CMOS level
Reading: Valid

Sets the input interface level of the SIN (P22), SCLK (P20) and $\overline{SS}$ (P23) terminals.
The SCLK and $\overline{SS}$ input interface level settings are effective only in slave mode or SPI slave mode. In master mode, the SMT20 and SMT23 registers can be used as general purpose registers.
At initial reset, these registers are set to "1" and the ports are configured with a CMOS Schmitt level input interface.

ESIF: Serial interface enable register (P2 port function selection) (FF58H•D0)

Sets P20–P23 to the input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

When "1" is written to the ESIF register, P20, P21, P22 and P23 function as SIN, SOUT, SCLK and SRDY or $\overline{SS}$, respectively.
In slave mode, the P23 terminal functions as SRDY output or $\overline{SS}$ input terminal, while in master mode, it functions as the I/O port terminal.
At initial reset, this register is set to "0".

SCTRG: Clock trigger/status (FF58H•D1)

This is a trigger to start input/output of synchronous clock (SCLK).

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock (SCLK) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

• ***When reading***

When "1" is read: RUN (during input/output the synchronous clock)
When "0" is read: STOP (the synchronous clock stops)

When this bit is read, it indicates the status of serial interface clock.
After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation.
When the synchronous clock input/output is completed, this latch is reset to "0".
At initial reset, this bit is set to "0".

ESOUT: SOUT enable register (FF58H•D2)

Enables serial data output from the P21 port.

When "1" is written: Enabled (SOUT)
When "0" is written: Disabled (I/O port)
Reading: Valid

When serial data output is not used, the SOUT output can be disabled to use P21 as an I/O port. When performing serial output, write "1" to ESOUT to set P21 as the SOUT output port.
At initial reset, this register is set to "0".

SMOD: Operating mode select register (FF59H•D0)

Selects the serial interface operating mode from master mode and slave mode.

When "1" is written: Master mode
When "0" is written: Slave mode
Reading: Valid

In master mode, the serial interface uses the internal clock (selected in the clock manager) as the synchronous clock for serial transfer. The synchronous clock is also output from the SCLK (P20) terminal to control the external serial interface (slave device). In slave mode, the serial interface inputs the synchronous clock that is sent by the external serial interface (master device) from the SCLK terminal to perform serial transfer. Master mode is selected by writing "1" to SMOD, and slave mode is selected by writing "0". At initial reset, this register is set to "0".

SDP: Data input/output permutation select register (FF59H•D1)

Selects the serial data input/output permutation.

When "1" is written: MSB first
When "0" is written: LSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first.
At initial reset, this register is set to "0".

SCPS0, SCPS1: Clock format select register (FF59H•D2, D3)

Selects the timing for reading in the serial data input from the SIN (P22) terminal.

Table 4.10.8.3 Configuration of synchronous clock format

SCPS1	SCPS0	Polarity	Phase
1	1	Negative ($\overline{SCLK}$)	Rising edge (⌐)
1	0	Negative ($\overline{SCLK}$)	Falling edge (¬)
0	1	Positive (SCLK)	Falling edge (¬)
0	0	Positive (SCLK)	Rising edge (⌐)

- ***When positive polarity (SCPS1 = "0") is selected for the synchronous clock:***
  During receiving, the serial data is read into the built-in shift register at the rising edge of the SCLK signal when the SCPS0 register is "0" or at the falling edge of the SCLK signal when the SCPS0 register is "1". The shift register is sequentially shifted as the data is fetched.

  During transmitting, the serial data output to the SOUT (P21) terminal changes at the rising edge of the clock input or output from/to the SCLK (P20) terminal. The data in the shift register is shifted at the rising edge of the SCLK signal when the SCPS0 register is "0" or at the falling edge of the SCLK signal when the SCPS0 register is "1".
- ***When negative polarity (SCPS1 = "1") is selected for the synchronous clock:***
  During receiving, the serial data is read into the built-in shift register at the falling edge of the $\overline{SCLK}$ signal when the SCPS0 register is "0" or at the rising edge of the $\overline{SCLK}$ signal when the SCPS0 register is "1". The shift register is sequentially shifted as the data is fetched.

  During transmitting, the serial data output to the SOUT (P21) terminal changes at the falling edge of the clock input or output from/to the $\overline{SCLK}$ (P20) terminal. The data in the shift register is shifted at the falling edge of the $\overline{SCLK}$ signal when the SCPS0 register is "0" or at the rising edge of the $\overline{SCLK}$ signal when the SCPS0 register is "1".

At initial reset, this register is set to "0".

ENCS: Serial interface enable register (P23 port function selection) (FF5AH•D0)

Enables the serial input/output function of P23. Use this register with ESREADY.

When "1" is written: Enabled (Serial interface)
When "0" is written: Disabled (I/O port)
Reading: Valid

When ENCS is enabled, the P23 terminal can be used as SRDY output or $\overline{SS}$ input terminal in slave mode (SMOD = "0").
At initial reset, this register is set to "0".

ESREADY: P23 port function select register (FF5AH•D1)

Selects the P23 port function when ENCS = "1".

When "1" is written: SRDY output
When "0" is written: $\overline{SS}$ input
Reading: Valid

The P23 port function can be selected from SRDY output and $\overline{SS}$ input in slave mode (SMOD = "0"). At initial reset, this register is set to "0".

Table 4.10.8.4 Selecting P23 port function

Slave mode: SMOD = "0"

ESREADY	ENCS	P23 terminal
*	0	P23 (I/O)
0	1	$\overline{SS}$ (I)
1	1	SRDY (O)

Master mode: SMOD = "1"

ESREADY	ENCS	P23 terminal
*	0	P23 (I/O)
0	1	P23 (I/O)
1	1	Prohibited

SD0–SD3, SD4–SD7: Serial interface data register (FF5BH, FF5CH)

These registers are used for writing and reading serial data.

• ***When writing***

When "1" is written: High level
When "0" is written: Low level

Write data to be output in these registers. The register data is converted into serial data and output from the SOUT (P21) terminal; data bits set at "1" are output as high (V_{DD}) level and data bits set at "0" are output as low (V_{SS}) level.

• ***When reading***

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN (P22) terminal can be read from these registers.
The serial data input from the SIN (P22) terminal is converted into parallel data, as a high (V_{DD}) level bit into "1" and as a low (V_{SS}) level bit into "0", and is loaded to these registers. Perform data reading only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).
At initial reset, these registers are undefined.

EISIF: Interrupt mask register (FFEAH•D0)

Masking the interrupt of the serial interface can be selected with this register.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With this register, it is possible to select whether the serial interface interrupt is to be masked or not.
At initial reset, this register is set to "0".

ISIF: Interrupt factor flag (FFFAH•D0)

This flag indicates the occurrence of serial interface interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
This flag is set to "1" after an 8-bit data input/output even if the interrupt is masked.
This flag is reset to "0" by writing "1" to it.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, this flag is set to "0".

4.10.9 Programming notes

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when the programmable timer is used as the clock source or the serial interface is used in slave mode.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.11 Sound Generator

4.11.1 Configuration of sound generator

The S1C63632 has a built-in sound generator for generating a buzzer signal.
Hence, the generated buzzer signal can be output from the BZ terminal.
Aside permitting the respective setting of the buzzer signal frequency and sound level to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.
Figure 4.11.1.1 shows the configuration of the sound generator.

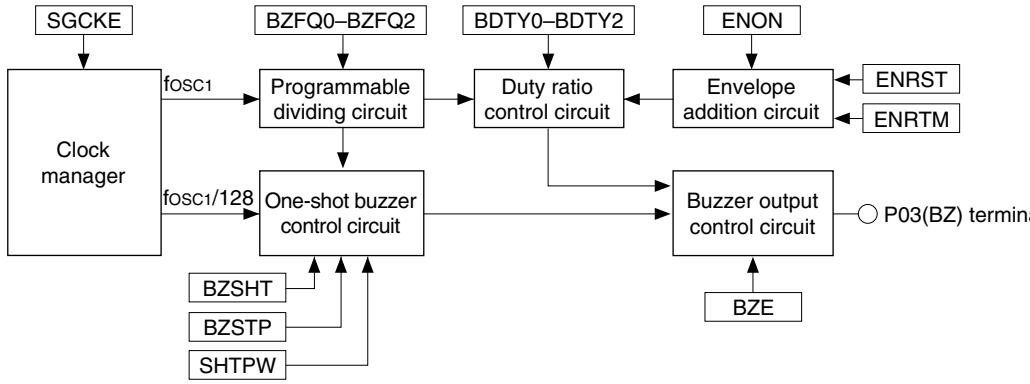


Fig. 4.11.1.1 Configuration of sound generator

Note: If the BZ terminal is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.

4.11.2 Controlling clock manager

To generate the buzzer signal, the clock for the sound generator must be supplied from the clock manager by writing "1" to the SGCKE register in advance.

Table 4.11.2.1 Controlling sound generator clock

SGCKE	Sound generator clock
1	Programmable dividing circuit input clock: fOSC1 (32 kHz) One-shot buzzer control circuit input clock: fOSC1 / 128 (256 Hz)
0	Off

If it is not necessary to run the sound generator, stop the clock supply by setting SGCKE to "0" to reduce current consumption.

4.11.3 Control of buzzer output

The BZ signal generated by the sound generator is output from the P03 (BZ) terminal by setting "1" for the buzzer output enable register BZE. The I/O control register IOC03 and data register P03 settings are ineffective while the BZ signal is being output.
When BZE is set to "0", the P03 port is configured as a general-purpose DC input/output port.

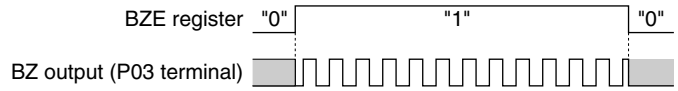


Fig. 4.11.3.1 Buzzer signal output timing chart

Note: Since it generates the buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

4.11.4 Setting of buzzer frequency and sound level

The divided signal of the OSC1 oscillation clock (32.768 kHz) is used for the buzzer signal and it is set up such that 8 types of frequencies can be selected by changing this division ratio. Frequency selection is done by setting the buzzer frequency select register BZFQ0–BZFQ2 as shown in Table 4.11.4.1.

Table 4.11.4.1 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer sound level is changed by controlling the duty ratio of the buzzer signal.
The duty ratio can be selected from among the 8 types shown in Table 4.11.4.2 according to the setting of the buzzer duty select register BDTY0–BDTY2.

Table 4.11.4.2 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

When the high level output time has been made TH and when the low level output time has been made TL due to the ratio of the pulse width to the pulse synchronization, the duty ratio becomes TH/(TH+TL).
When BDTY0–BDTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when BDTY0–BDTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.
The duty ratio that can be set is different depending on the frequency that has been set, so see Table 4.11.4.2.

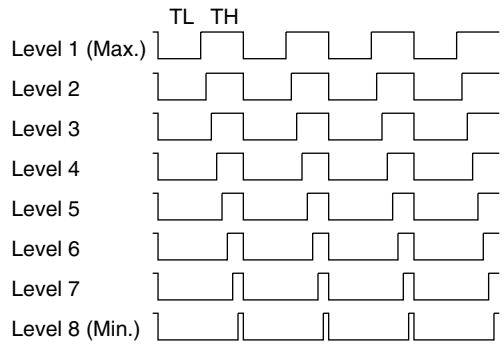


Fig. 4.11.4.1 Duty ratio of the buzzer signal waveform

Note: When a digital envelope has been added to the buzzer signal, the BDTY0–BDTY2 settings will be invalid due to the control of the duty ratio.

4.11.5 Digital envelope

A digital envelope for duty control can be added to the buzzer signal.
The envelope can be controlled by staged changing of the same duty envelope as detailed in Table 4.11.4.2 in the preceding item from level 1 (maximum) to level 8 (minimum).
The addition of an envelope to the buzzer signal can be done by writing "1" into ENON, but when "0" has been written it is not added.
When a buzzer signal output is begun (writing "1" into BZE) after setting ENON, the duty ratio shifts to level 1 (maximum) and changes in stages to level 8.
When attenuated down to level 8 (minimum), it is retained at that level. The duty ratio can be returned to maximum, by writing "1" into register ENRST during output of a envelope attached buzzer signal.
The envelope attenuation time (time for changing of the duty ratio) can be selected by the register ENRTM. The time for a 1 stage level change is 62.5 msec (16 Hz), when "0" has been written into ENRTM and 125 msec (8 Hz), when to "1" has been written. However, there is also a max. 4 msec error from envelope ON, up to the first change.
Figure 4.11.5.1 shows the timing chart of the digital envelope.

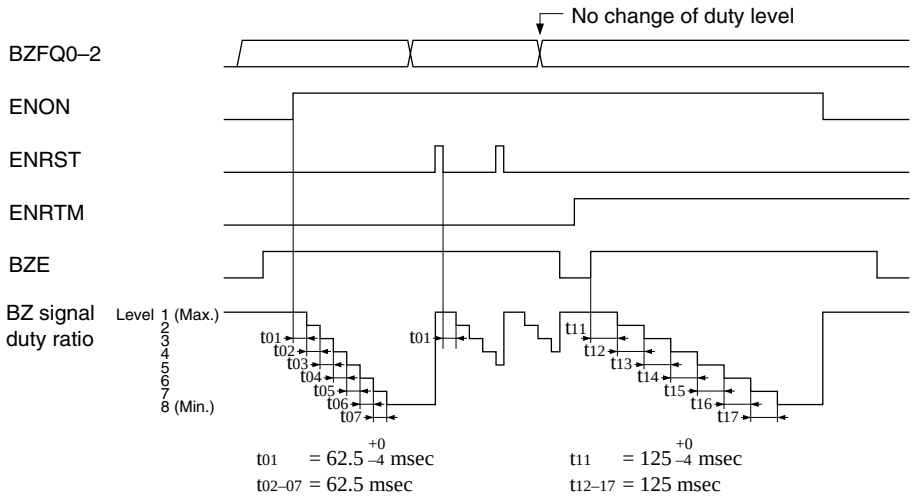


Fig. 4.11.5.1 Timing chart for digital envelope

4.11.6 One-shot output

The sound generator has a one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by SHTPW register for one-shot buzzer signal output time.
The output of the one-shot buzzer is controlled by writing "1" into the one-shot buzzer trigger BZSHT. When this trigger has been assigned, a buzzer signal in synchronization with the internal 256 Hz signal is output from the buzzer output terminal. Thereafter, when the set time has elapsed, a buzzer signal in synchronization with the 256 Hz signal goes off in the same manner as for the start of output.
The BZSHT also permits reading. When BZSHT is "1", the one-shot output circuit is in operation (during one-shot output) and when it is "0", it shows that the circuit is in the ready (outputtable) status.

In addition, it can also terminate one-shot output prior to the elapsing of the set time. This is done by writing a "1" into the one-shot buzzer stop BZSTP. In this case as well, the buzzer signal goes off in synchronization with the 256 Hz signal.

When "1" is written to BZSHT again during a one-shot output, a new one-shot output for 125 msec or 31.25 msec starts from that point (in synchronization with the 256 Hz signal).

The one-shot output cannot add an envelope for short durations. However, the sound level can be set by selecting the duty ratio, and the frequency can also be set.
One-shot output is invalid during normal buzzer output (during BZE = "1").

Figure 4.11.6.1 shows timing chart for one-shot output.

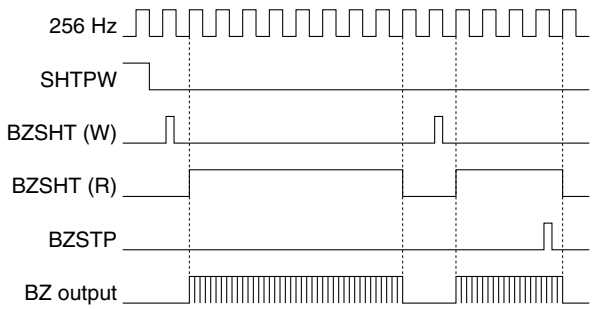


Fig. 4.11.6.1 Timing chart for one-shot output

4.11.7 I/O memory of sound generator

Table 4.11.7.1 shows the I/O addresses and the control bits for the sound generator.

Table 4.11.7.1 Control bits of sound generator

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF16H	MDCKE	SGCKE	SWCKE	RTCKE	MDCKE	0	Enable	Disable	Integer multiplier clock enable
					SGCKE	0	Enable	Disable	Sound generator clock enable
	R/W				SWCKE	0	Enable	Disable	Stopwatch timer clock enable
					RTCKE	0	Enable	Disable	Clock timer clock enable
FF44H	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
FF45H	0	BZSTP	BZSHT	SHTPW	0 *3	– *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FF46H	0	BZFQ2	BZFQ1	BZFQ0	0 *3	– *2			Unused
					BZFQ2	0			Buzzer frequency selection [BZFQ2–0] 0 1 2 3 / Frequency (Hz) 4096.0 3276.8 2730.7 2340.6 / [BZFQ2–0] 4 5 6 7 / Frequency (Hz) 2048.0 1638.4 1365.3 1170.3
					BZFQ1	0			
	R	R/W			BZFQ0	0			
FF47H	0	BDTY2	BDTY1	BDTY0	0 *3	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
	R	R/W			BDTY1	0			
					BDTY0	0			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SGCKE: Sound generator clock enable register (FF16H•D2)

Controls the clock supply to the sound generator.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to SGCKE, the sound generator operating clock is supplied from the clock manager. If it is not necessary to run the sound generator, stop the clock supply by setting SGCKE to "0" to reduce current consumption.
At initial reset, this register is set to "0".

BZE: Buzzer output enable register (FF44H•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output On
When "0" is written: Buzzer output Off
Reading: Valid

When "1" is written to BZE, the BZ signal is output from the P03 (BZ) terminal. The I/O control register IOC03 and data register P03 settings are ineffective while the BZ signal is being output.
When BZE is set to "0", the P03 port is configured as a general-purpose DC input/output port.
At initial reset, this register is set to "0".

ENON: Envelope On/Off control register (FF44H•D1)

Controls the addition of an envelope onto the buzzer signal.

When "1" is written: On
When "0" is written: Off
Reading: Valid

Writing "1" to ENON causes an envelope to be added during buzzer signal output. When a "0" has been written, an envelope is not added.
At initial reset, this register is set to "0".

ENRST: Envelope reset (FF44H•D2)

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

Writing "1" to ENRST resets envelope and the duty ratio becomes maximum. If an envelope has not been added (ENON = "0") and if no buzzer signal is being output, the reset becomes invalid. Writing "0" is also invalid.
This bit is dedicated for writing, and is always "0" for reading.

ENRTM: Envelope releasing time select register (FF44H•D3)

Selects the envelope releasing time that is added to the buzzer signal.

When "1" is written: 1.0 sec (125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec (62.5 msec × 7 = 437.5 msec)
Reading: Valid

The releasing time of the digital envelope is determined by the time for converting the duty ratio.
When "1" is written to ENRTM, it becomes 125 msec (8 Hz) units and when "0" is written, it becomes 62.5 msec (16 Hz) units.
At initial reset, this register is set to "0".

SHTPW: One-shot buzzer pulse width setting register (FF45H•D0)

Selects the output time of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

Writing "1" to SHTPW causes the one-short output time to be set at 125 msec, and writing "0" causes it to be set to 31.25 msec. It does not affect normal buzzer output.
At initial reset, this register is set to "0".

BZSHT: One-shot buzzer trigger/status (FF45H•D1)

Controls the one-shot buzzer output.

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

Writing "1" to BZSHT causes the one-short output circuit to operate and a buzzer signal to be output. This output is automatically turned off after the time set by SHTPW has elapsed. The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

• When reading

When "1" is read: BUSY
When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes off, it shifts to "0".
At initial reset, this bit is set to "0".

BZSTP: One-shot buzzer stop (FF45H•D2)

Stops the one-shot buzzer output.

When "1" is written: Stop
When "0" is written: No operation
Reading: Always "0"

Writing "1" to BZSTP permits the one-shot buzzer output to be turned off prior to the elapsing of the time set by SHTPW. Writing "0" is invalid and writing "1" is also invalid except during one-shot output.
This bit is dedicated for writing, and is always "0" for reading.

BZFQ0–BZFQ2: Buzzer frequency select register (FF46H•D0–D2)

Selects the buzzer signal frequency.

Table 4.11.7.2 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Select the buzzer frequency from among the above 8 types that have divided the oscillation clock.
At initial reset, this register is set to "0".

BDTY0–BDTY2: Duty level select register (FF47H•D0–D2)

Selects the duty ratio of the buzzer signal as shown in Table 4.11.7.3.

Table 4.11.7.3 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

The sound level of this buzzer can be set by selecting this duty ratio.
However, when the envelope has been set to on (ENON = "1"), this setting becomes invalid.
At initial reset, this register is set to "0".

4.11.8 Programming notes

(1) Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

(2) The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

4.12 Integer Multiplier

4.12.1 Configuration of integer multiplier

The S1C63632 has a built-in unsigned-integer multiplier. This multiplier performs 8 bits × 8 bits of multiplication or 16 bits ÷ 8 bits of division and returns the results and three flag states.
Figure 4.12.1.1 shows the configuration of the integer multiplier.

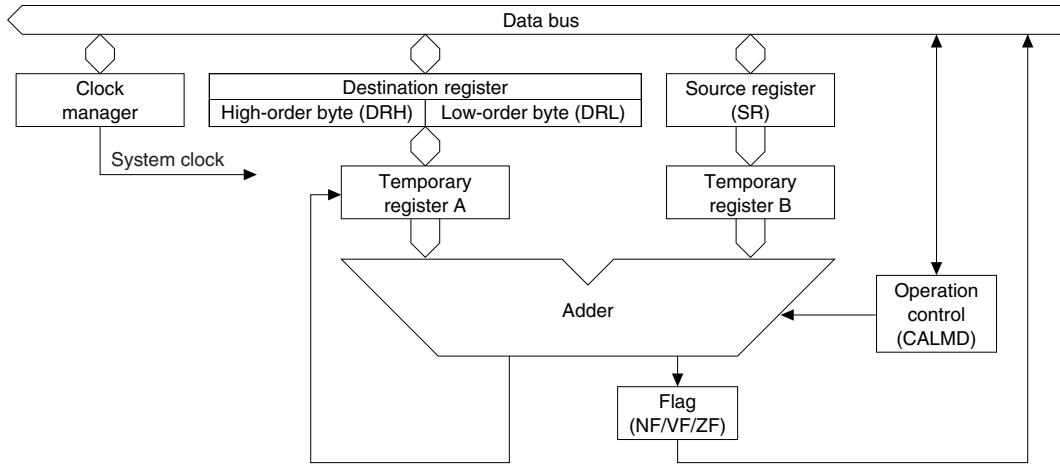


Fig. 4.12.1.1 Configuration of the integer multiplier

4.12.2 Controlling clock manager

The integer multiplier operates with the clock supplied by the clock manager (CPU operating clock selected by OSCC and CLKCHG). Before the integer multiplier can be run, write "1" to the MDCKE register to supply the operating clock to the integer multiplier.

Table 4.12.2.1 Controlling integer multiplier clock

MDCKE	Integer multiplier clock
1	When CLKCHG = "0": f_{OSC1} (32 kHz) When OSCC = 1", CLKCHG = "1": f_{OSC3}
0	Off

If it is not necessary to run the integer multiplier, stop the clock supply by setting MDCKE to "0" to reduce current consumption.

4.12.3 Multiplication mode

To perform a multiplication, set the multiplier to the source register (SR) and the multiplicand to the low-order 8 bits (DRL) of the destination register, then write "0" to the calculation mode select register (CALMD). The multiplication takes 10 CPU clock cycles from writing "0" to CALMD until the 16-bit product is loaded into the destination register (DRH and DRL). At the same time the result is loaded, the operation flags (NF, VF and ZF) are updated.
The following shows the conditions that change the operation flag states and examples of multiplication.

N flag: Set when the MSB of DRH is "1" and reset when it is "0".
V flag: Always reset after a multiplication.
Z flag: Set when the 16-bit value in DRH/DRL is 0000H and reset when it is not 0000H.

<Examples of multiplication>

DRL (multiplicand)	SR (multiplier)	DRH/DRL (product)	NF	VF	ZF
00H	64H	0000H	0	0	1
64H	58H	2260H	0	0	0
C8H	58H	44C0H	0	0	0
C8H	A5H	80E8H	1	0	0

4.12.4 Division mode

To perform a division, set the divisor to the source register (SR) and the dividend to the destination register (DRH and DRL), then write "1" to the calculation mode select register (CALMD). The division takes 10 CPU clock cycles from writing "1" to CALMD until the quotient is loaded into the low-order 8 bits (DRL) of the destination register and the remainder is loaded into the high-order 8 bits (DRH) of the destination register. At the same time the result is loaded, the operation flags (NF, VF and ZF) are updated.
However, when an overflow results (if the quotient exceeds the 8-bit range), the destination register (DRH and DRL) does not change its contents as it maintains the dividend.
The following shows the conditions that change the operation flag states and examples of division.

N flag: Set when the MSB of DRL is "1" and reset when it is "0".
V flag: Set when the quotient exceeds the 8-bit range and reset when it is within the 8-bit range.
Z flag: Set when the 8-bit value in DRL is 00H and reset when it is not 00H.

<***Examples of division***>

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
1A16H	64H	42H	4EH	0	0	0
332CH	64H	83H	00H	1	0	0
0000H	58H	00H	00H	0	0	1
2468H	13H	68H	24H	1	1	0

In the example of "2468H" ÷ "13H" shown above, DRH/DRL maintains the dividend because the quotient overflows the 8-bit. To get the correct results when an overflow has occurred, perform the division with two steps as shown below.

1. Divide the high-order 8 bits of the dividend (24H) by the divisor (13H) and then store the quotient (01H) to memory.

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
0024H	13H	01H	11H	0	0	0

2. Keep the remainder (11H) in DRH and load the low-order 8 bits of the dividend (68H) to DRL, then perform division again.

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
1168H	13H	EAH	0AH	1	0	0

The correct result is obtained as the quotient = 01EAH (the first and second results of DRL are merged) and the remainder = 0AH. However, since the operation flags (NF/VF/ZF) are changed in each step, they cannot indicate the states according to the final operation results.

Note: Make sure that the division results are correct using software as the hardware does not check.

4.12.5 Execution cycle

Both the multiplication and division take 10 CPU cycles for an operation. Therefore, before the results can be read from the destination register DRH/DRL, wait at least 5 bus cycles after writing to CALMD. The same applies to reading the operation flags NF/VF/ZF.
The following shows a sample program.

```
      ldb  %ext, src_data@h
      ldb  %xl, src_data@l      ; Set RAM address for operand
      ldb  %ext, au@h
      ldb  %yl, au@l            ; Set multiplier I/O memory address
;
      ldb  %ba, [%x]+
      ldb  [%y]+, %ba           ; Set data to SR
      ldb  %ba, [%x]+
      ldb  [%y]+, %ba           ; Set data to DRL
      ldb  %ba, [%x]+
      ldb  [%y]+, %ba           ; Set data to DRH
;
      ld   [%y], 0b0001         ; Start operation (select calculation mode)
;
      ldb  %ext, rslt_data@h
      ldb  %xl, rslt_data@l     ; Set result store address
      nop
      nop
      nop                       ; Dummy instructions to wait end of operation
;
      bit  [%y], 0b0100
      jrnz overflow             ; Jump to error routine if VF = "1"
;
      add  %y, -4               ; Set DRL again
;
      ldb  %ba, [%y]+
      ldb  [%x]+, %ba           ; Store result (quotient) into RAM
      ldb  %ba, [%y]+
      ldb  [%x]+, %ba           ; Store result (remainder) into RAM
```

4.12.6 I/O memory of integer multiplier

Table 4.12.6.1 shows the I/O addresses and the control bits for the integer multiplier.

Table 4.12.6.1 Control bits of integer multiplier

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF16H	MDCKE	SGCKE	SWCKE	RTCKE	MDCKE	0	Enable	Disable	Integer multiplier clock enable
					SGCKE	0	Enable	Disable	Sound generator clock enable
	R/W				SWCKE	0	Enable	Disable	Stopwatch timer clock enable
					RTCKE	0	Enable	Disable	Clock timer clock enable
FF70H	SR3	SR2	SR1	SR0	SR3	– *2			Source register (low-order 4 bits)
					SR2	– *2			
	R/W				SR1	– *2			
					SR0	– *2			LSB
FF71H	SR7	SR6	SR5	SR4	SR7	– *2			MSB
					SR6	– *2			Source register (high-order 4 bits)
	R/W				SR5	– *2			
					SR4	– *2			
FF72H	DRL3	DRL2	DRL1	DRL0	DRL3	– *2			Low-order 8-bit destination register (low-order 4 bits)
					DRL2	– *2			
	R/W				DRL1	– *2			
					DRL0	– *2			LSB
FF73H	DRL7	DRL6	DRL5	DRL4	DRL7	– *2			MSB
					DRL6	– *2			Low-order 8-bit destination register
	R/W				DRL5	– *2			(high-order 4 bits)
					DRL4	– *2			
FF74H	DRH3	DRH2	DRH1	DRH0	DRH3	– *2			High-order 8-bit destination register (low-order 4 bits)
					DRH2	– *2			
	R/W				DRH1	– *2			
					DRH0	– *2			LSB
FF75H	DRH7	DRH6	DRH5	DRH4	DRH7	– *2			MSB
					DRH6	– *2			High-order 8-bit destination register
	R/W				DRH5	– *2			(high-order 4 bits)
					DRH4	– *2			
FF76H	NF	VF	ZF	CALMD	NF	0	Negative	Positive	Negative flag
					VF	0	Overflow	No	Overflow flag
	R			R/W	ZF	0	Zero	No	Zero flag
					CALMD	0	Run	Stop	Operation status (reading)
							Div.	Mult.	Calculation mode selection (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

MDCKE: Integer multiplier clock enable register (FF16H•D3)

Controls the operating clock supply to the integer multiplier.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to MDCKE, the integer multiplier operating clock (CPU operating clock selected by OSCC and CLKCHG) is supplied from the clock manager. If it is not necessary to run the integer multiplier, stop the clock supply by setting MDCKE to "0" to reduce current consumption.
At initial reset, this register is set to "0".

SR0–SR7: Source register (FF70H, FF71H)

Used to set multipliers and divisors.
Set the low-order 4 bits of data to SR0–SR3 and the high-order 4 bits to SR4–SR7.
This register maintains the latest set value until the next writing, so it is not necessary to set data for each operation if the same multiplier and divisor is used in a series of operations.
At initial reset, this register is undefined.

DRL0–DRL7: Destination register low-order 8 bits (FF72H, FF73H)

Used to set multiplicands and low-order 8 bits of dividends.
Set the low-order 4 bits of data to DRL0–DRL3 and the high-order 4 bits to DRL4–DRL7.
Data written to this register is loaded to the arithmetic circuit when an operation starts (by writing to FF76H•D0), and then a multiplication or a division is performed in 10 CPU clock cycles (5 bus cycles). After the operation has finished, the low-order 8 bits of the product or the quotient are loaded to this register.
However, if an overflow occurs in a division process, the quotient is not loaded and the low-order 8 bits of the dividend remains.
At initial reset, this register is undefined.

DRH0–DRH7: Destination register high-order 8 bits (FF74H, FF75H)

Used to set high-order 8 bits of dividends.
Set the low-order 4 bits of data to DRH0–DRH3 and the high-order 4 bits to DRH4–DRH7.
At the start of a multiplication (by writing "0" to FF76H•D0), the contents in this register are ignored. After 10 CPU cycles (5 bus cycles) of multiplication process has finished, the high-order 8 bits of the product are loaded in this register.
In a division process, data written to this register is loaded to the arithmetic circuit when an operation starts (by writing "1" to FF76H•D0), and then a division is performed in 10 CPU clock cycles (5 bus cycles). After the operation has finished, the remainder is loaded to this register. However, if an overflow occurs in a division process, the remainder is not loaded and the high-order 8 bits of the dividend remains.
At initial reset, this register is undefined.

CALMD: Calculation mode select register/operation status (FF76H•D0)

Selects multiplication or division mode and starts operation.

When "1" is written: Selects/starts division
When "0" is written: Selects/starts multiplication
When "1" is read: Under operating
When "0" is read: Operation has finished

Writing to this register starts the specified operation. After that, this register is set to "1" and returns to "0" when the multiplication or division process has finished.
At initial reset, this register is reset to "0".

ZF: Zero flag (FF76H•D1)

Indicates whether the operation result is zero or not.

When "1" is read: Zero
When "0" is read: Not zero
Writing: Invalid

ZF is a read-only bit, so writing operation is invalid.
At initial reset, this flag is set to "0".

VF: Overflow flag (FF76H•D2)

Indicates whether an overflow has occurred or not in a division process.

When "1" is read: Overflow occurred
When "0" is read: Overflow has not occurred
Writing: Invalid

When a multiplication process has finished, this flag is always set to "0".
VF is a read-only bit, so writing operation is invalid.
At initial reset, this flag is set to "0".

NF: Negative flag (FF76H•D3)

Indicates whether the operation result is a positive value or a negative value.

When "1" is read: Negative value (MSB of the results is "1")
When "0" is read: Positive value (MSB of the results is "0")
Writing: Invalid

NF is a read-only bit, so writing operation is invalid.
At initial reset, this flag is set to "0".

4.12.7 Programming note

An operation process takes 10 CPU clock cycles (5 bus cycles) after writing to the calculation mode select register CALMD until the operation result is set to the destination register DRH/DRL and the operation flags. While this operation is in process, do not read/write from/to the destination register DRH/DRL and do not read NF/VF/ZF.

4.13 R/f Converter

4.13.1 Configuration of R/f converter

The S1C63632 has a built-in CR oscillation type R/f converter that can be used as an A/D converter. Two systems (channel 0 and channel 1) of CR oscillation circuits are built into the R/f converter, so it is possible to compose two types of R/f conversion circuits by connecting different sensors to each CR oscillation circuit.

Channel 0 can be used as an R/f (Resistor/frequency) conversion circuit using a DC bias resistive sensor such as a thermistor, and channel 1 can be used as an R/f conversion circuit the same as channel 0, or for an AC bias resistive sensor such as a humidity sensor.

The channel to be used and sensor type for channel 1 are selected with software.

Resistance value (relative value to external reference resistance) of the resistive sensor that has been connected to the sensor input terminal is converted into frequency by the CR oscillation circuit and the number of clocks is counted in the built-in measurement counter. By reading the value of the measurement counter, it can obtain the data after digitally-converting the value detected by the sensor.

Various sensor circuits such as temperature/humidity measurement circuits can be easily realized using this R/f converter.

The configuration of the R/f converter is shown in Figure 4.13.1.1.

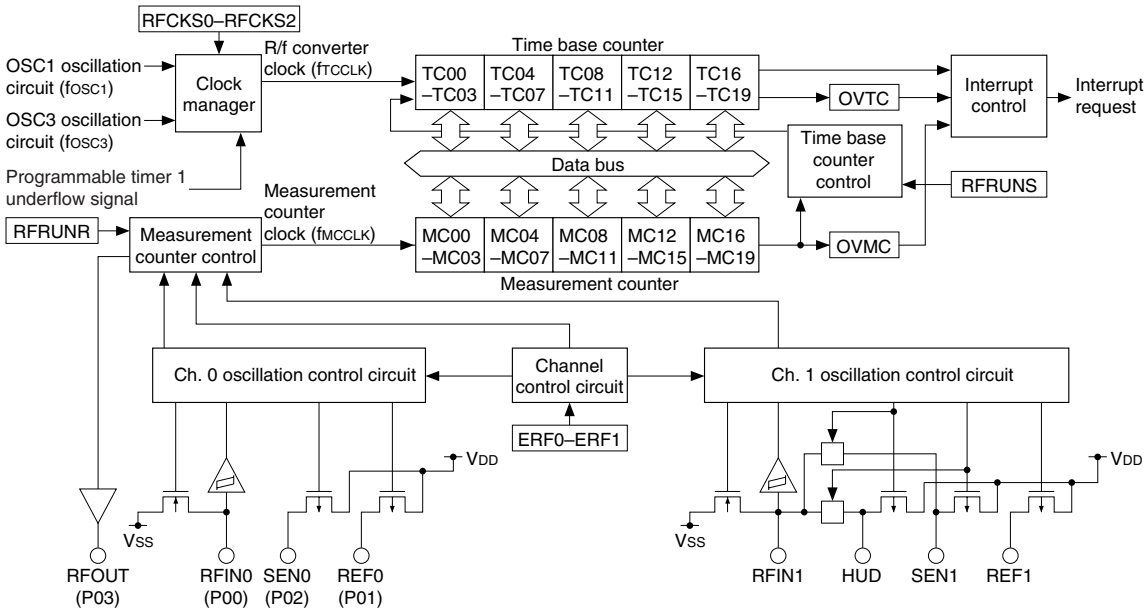


Fig. 4.13.1.1 Configuration of R/f converter

4.13.2 Controlling clock manager

The R/f converter uses the clock supplied from the clock manager as its operating clock and the count clock for the time base counter. The clock manager generates six R/f converter clocks by dividing the OSC1 and OSC3 clocks. The R/f converter clock can be selected from seven types (the above six clocks and the programmable timer 1 output clock). Use the RFCKS0–RFCKS2 register to select one of them as shown in Table 4.13.2.1.

Table 4.13.2.1 R/f converter clock frequencies

RFCKS2	RFCKS1	RFCKS0	R/f converter clock
1	1	1	f_{OSC3} / 4
1	1	0	f_{OSC3} / 2
1	0	1	f_{OSC3} / 1
1	0	0	Programmable timer 1
0	1	1	f_{OSC1} / 4 (8 kHz)
0	1	0	f_{OSC1} / 2 (16 kHz)
0	0	1	f_{OSC1} / 1 (32 kHz)
0	0	0	Off

f_{OSC1}: OSC1 oscillation frequency. ( ) indicates the frequency when f_{OSC1} = 32 kHz.
f_{OSC3}: OSC3 oscillation frequency

When programmable timer 1 is selected, the programmable timer 1 underflow signal is divided by 2 before it is used as the R/f converter clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.9, "Programmable Timer" for controlling the programmable timer.

If it is not necessary to run the R/f converter, stop the clock supply by setting RFCKS0–RFCKS2 to "000B" to reduce current consumption.

4.13.3 Connection terminals and CR oscillation circuit

The R/f converter channel 0 input/output terminals and the RFOUT output terminal are shared with the I/O port (P00–P03), and the terminal functions must be switched with software when using these terminals for the R/f converter.
By setting the ERF0–ERF1 register to other than "00B", P00, P01 and P02 are configured as the RFIN0, REF0 and SEN0 terminals, respectively.
The RFOUT output through the P03 port is effective when "1" is written to the RFOUT register. When the RFOUT register is "0", P03 is used as an I/O port.
The table below lists the correspondence between the P00 to P03 terminals and the R/f converter input/output.

Table 4.13.3.1 Setting input/output terminal functions

Terminal name	R/f converter input/output
P00	RFIN0
P01	REF0
P02	SEN0
P03	RFOUT

Note: At initial reset, P00 to P03 are configured as the I/O ports.
When using the R/f converter channel 0, switch the terminal functions (ERF0–ERF1 = "01B", RFOUT = "1") in the initialize routine.

Two systems of CR oscillation circuits, channel 0 and channel 1, are built into the R/f converter and perform CR oscillation with the external resistor and capacitor.
The counter that is used to obtain R/f converted values is shared with channel 0 and channel 1. Therefore, operation for two channels is realized by switching the CR oscillation circuit that performs R/f conversion. The channel to perform R/f conversion and the sensor type should be selected using the ERF0–ERF1 register in advance.

Table 4.13.3.2 Selecting channel and sensor type

ERF1	ERF0	Channel and sensor type
1	1	Ch.1 DC
1	0	Ch.1 AC
0	1	Ch.0 DC
0	0	I/O

DC: R/f conversion using a DC bias resistive sensor such as a thermistor
AC: R/f conversion using an AC bias resistive sensor such as a humidity sensor

(1) R/f conversion using a DC bias resistive sensor such as a thermistor

Channel 0 supports this conversion method only, and channel 1 is selected into this method by setting ERFx to "11B". This method should be selected for R/f conversion using a normal resistive sensor (DC bias), such as temperature measurement using a thermistor. At initial reset, channel 1 is set into this conversion method.
Figure 4.13.3.1 shows the connection diagram of external elements.

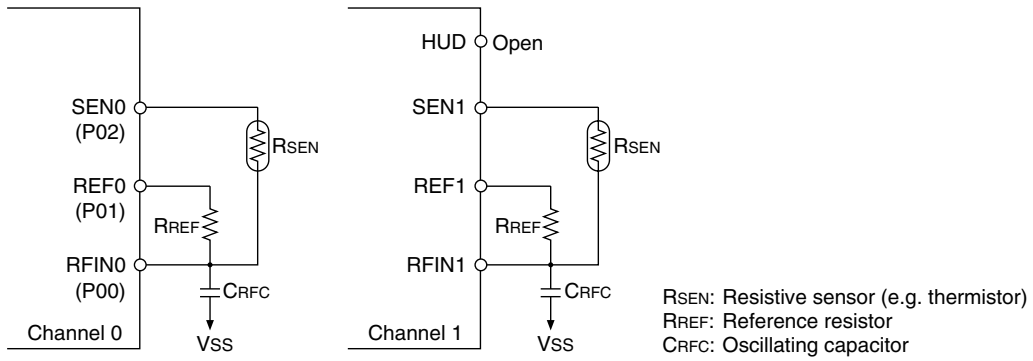


Fig. 4.13.3.1 Connection diagram in case of R/f conversion

CR oscillation waveforms are shaped by the schmitt trigger and sent to the measurement counter. The clock sent to the measurement counter is also output from the RFOUT terminal while the sensor is oscillating. As a result, the oscillation frequency can be measured by an oscilloscope or other equipment. Since this monitor has no effect on oscillation frequency, it can be used to adjust R/f conversion accuracy.
Oscillation waveforms and waveforms output from the RFOUT terminal are shown in Figure 4.13.3.2.

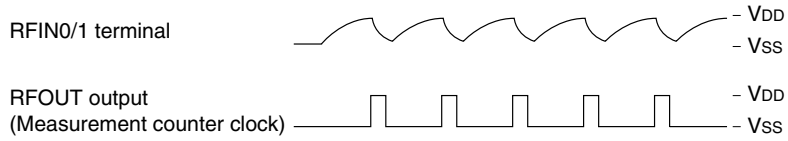


Fig. 4.13.3.2 Oscillation waveform

(2) R/f conversion using an AC bias resistive sensor such as a humidity sensor

This conversion is possible only in channel 1, and this method is selected by setting ERFx to "10B". This is basically the same as the R/f conversion described above (1), but the AC bias circuit works for a sensor (e.g. humidity sensor) to which DC bias cannot be applied for a long time. The oscillating operation by reference resistance is the same as the R/f conversion described above (1).
Figure 4.13.3.3 shows the connection diagram of external devices.

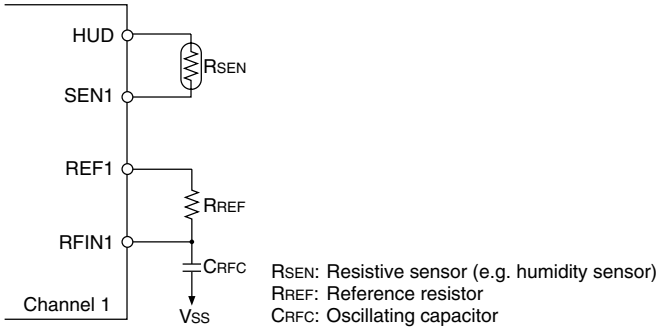


Fig. 4.13.3.3 Connection diagram of resistive humidity sensor

The oscillation waveform is the same as Figure 4.13.3.2.

4.13.4 Operation of R/f conversion

Counter

The R/f converter incorporates two types of counters: measurement counter MCxx and time base counter TCxx. The measurement counter is a 20-bit up counter that counts the CR oscillation clock with the reference resistance or sensor selected by software. The R/f conversion results can be obtained by reading this counter. The time base counter is a 20-bit up/down counter to equal both oscillation times for the reference resistance and the sensor. The time base counter uses the R/f converter clock selected by the RFCKSx register (OSC1 or OSC3). Each counter permits reading and writing on a 4-bit basis.
First start an R/f conversion for the reference resistance. The measurement counter starts counting up and the time base counter starts counting down. The counters stop counting when the measurement counter overflows (counter = "00000H"). By resetting the time base counter to "00000H" before starting an R/f conversion for the reference resistance, the reference oscillation time will be obtained from the time base counter.
Then start an R/f conversion for the sensor, the measurement counter starts counting up from "00000H" and the time base counter starts counting up from the counted value. The counters stop counting when the time base counter overflows (counter = "00000H"). The oscillation time in this phase is the same as that of the reference resistance.
Therefore, by converting a appropriate initial value for counting of the oscillation of the reference resistance into a complement (value subtracted from "00000H") and setting it into the measurement counter before starting to count, the number of counts for the sensor oscillation is obtained by reading the measurement counter after the R/f conversion. In other words, the difference between the reference resistance and sensor oscillation frequencies can be found easily. For instance, if resistance values of the reference resistance and the sensor are equivalent, the same value as the initial value before converting into a complement will be obtained as the result.
The time base counter allows reading of the counter value and presetting of data. By saving the counter value after the reference oscillation has completed into the RAM, the subsequent reference oscillation phase can be omitted. The sensor oscillation can be started after setting the saved value to the time base counter and "00000H" to the measurement counter.

Note: When setting the measurement counter, always write 5 words of data continuously in order from the lower address (FF62H → FF63H → FF64H → FF65H → FF66H). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used.

R/f conversion sequence

An R/f conversion for the reference resistance starts by writing "1" to the RFRUNR register. However, an initial value must be set to the measurement counter and the time base counter must be cleared to "00000H" before starting the R/f conversion.
When R/f conversion is initiated by the RFRUNR register, oscillation by the reference resistance begins, and the measurement counter starts counting up from the initial value by the oscillation clock. The time base counter also starts counting down by the OSC1 clock.
If the measurement counter becomes "00000H" due to overflow, the oscillation is terminated. At the same time an interrupt occurs and the RFRUNR register is set to "0", and the R/f converter circuit stops operation completely.
The time base counter value should be saved into the RAM for R/f conversion of the sensor.
Figure 4.13.4.1 shows a timing chart for the reference oscillation.

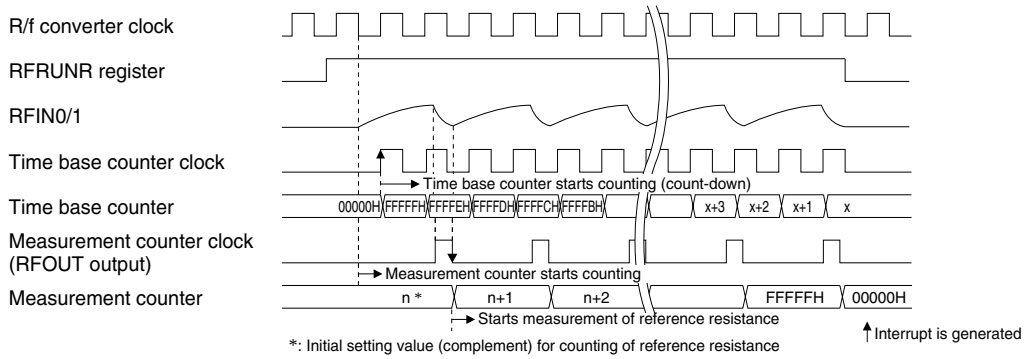


Fig. 4.13.4.1 Reference oscillation timing chart

An R/f conversion for the sensor starts by writing "1" to the RFRUNS register. When performing this sensor oscillation after an reference oscillation has completed, it is not necessary to set initial values to the counters. If converting the sensor resistance independently, the measurement counter must be set to "00000H" and the time base counter must be set to the value measured at the time of a reference oscillation. When R/f conversion is initiated by the RFRUNS register, oscillation by the sensor begins, and the measurement counter starts counting up from "00000H" by the oscillation clock. The time base counter also starts counting up by the input clock. If the time base counter becomes "00000H", the oscillation is terminated. At the same time an interrupt occurs and the RFRUNS register is set to "0", and the R/f converter circuit stops operation completely.
Figure 4.13.4.2 shows a timing chart for the sensor oscillation.

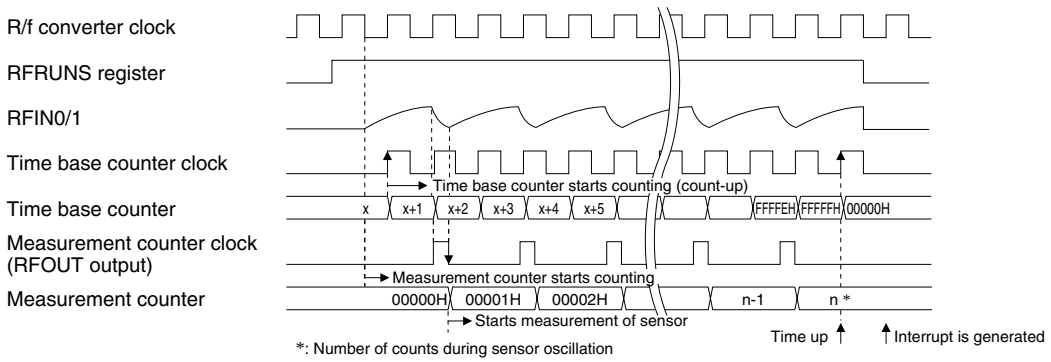


Fig. 4.13.4.2 Sensor oscillation timing chart

By the above operation, the sensor is oscillated for the same period of time as the reference resistance is oscillated. Therefore, the difference in oscillation frequency can be measured from the values counted by the measurement counter.

Since the reference resistance is oscillated until the measurement counter overflows, an appropriate initial value needs to be set before R/f conversion is started. If a smaller initial value is set, a longer counting period is possible, thereby ensuring more accurate detection. Convert the initial value into a complement (value subtracted from "00000H") before setting it on the measurement counter. Since the data output from the measurement counter after R/f conversion matches data detected by the sensor, process the difference between that value and the initial value before it is converted into a complement according to the program and calculate the target value.

The above operations are shown in Figure 4.13.4.3.

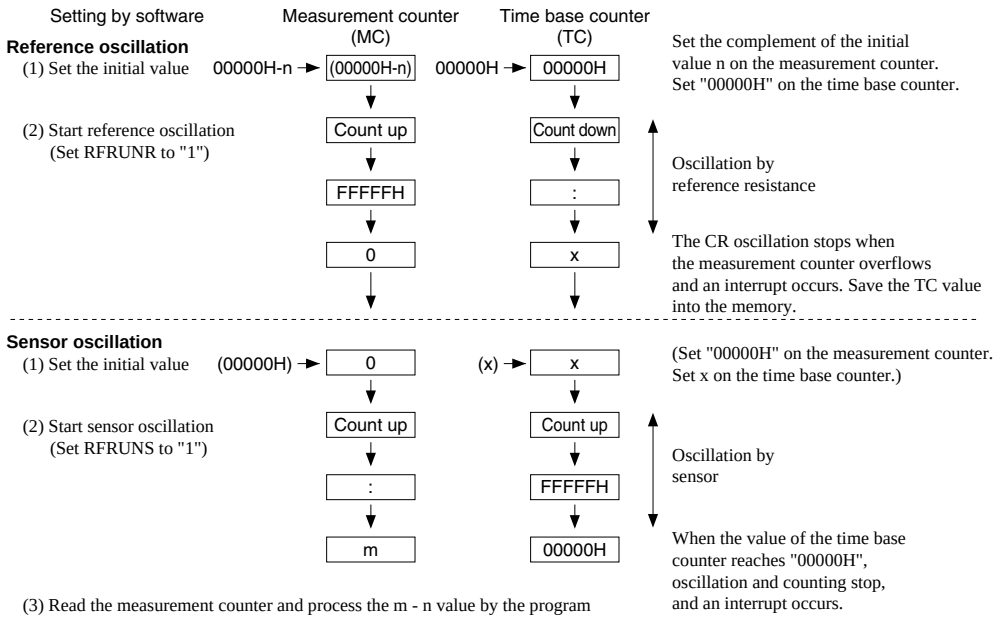


Fig. 4.13.4.3 Sequence of R/f conversion

Note: Set the initial value of the measurement counter taking into account the measurable range and the overflow of counters.

4.13.5 Interrupt function

The R/f converter has a function which allows interrupt to occur when an R/f conversion has completed or an error has occurred.
When the measurement counter reaches "00000H" during counting of the reference oscillation, both counters stop counting and RFRUNR is set to "0". At the same time, the interrupt factor flag IRFR is set to "1".
When the time base counter reaches "00000H" during counting of the sensor oscillation, both counters stop counting and RFRUNS is set to "0". At the same time, the interrupt factor flag IRFS is set to "1".
If the measurement counter overflows during counting of the sensor oscillation, both counters stop counting and RFRUNS is set to "0". In this case, the interrupt factor flag IRFE is set to "1". At the same time, the OVMC flag is also set to 1.
If the time base counter overflows during counting of the reference oscillation, both counters stop counting and RFRUNR is set to "0". In this case, the interrupt factor flag IRFE is set to "1". At the same time, the OVTC flag is also set to 1.
These interrupt factors allow masking by the interrupt mask registers EIRFR, EIRFS and EIRFE, and an interrupt is generated to the CPU when these registers are set to "1". When the mask register is set to "0", an interrupt is not generated to the CPU even if the interrupt factor flag is set to "1". The interrupt factor flag is reset to "0" by writing "1".
Timing of interrupt by the R/f converter is shown in Figures 4.13.5.1 to 4.13.5.4.

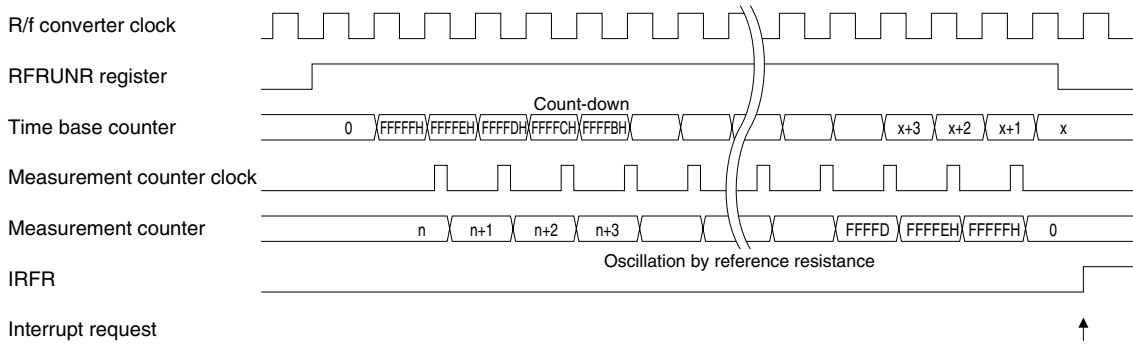


Fig. 4.13.5.1 Reference oscillate completion interrupt

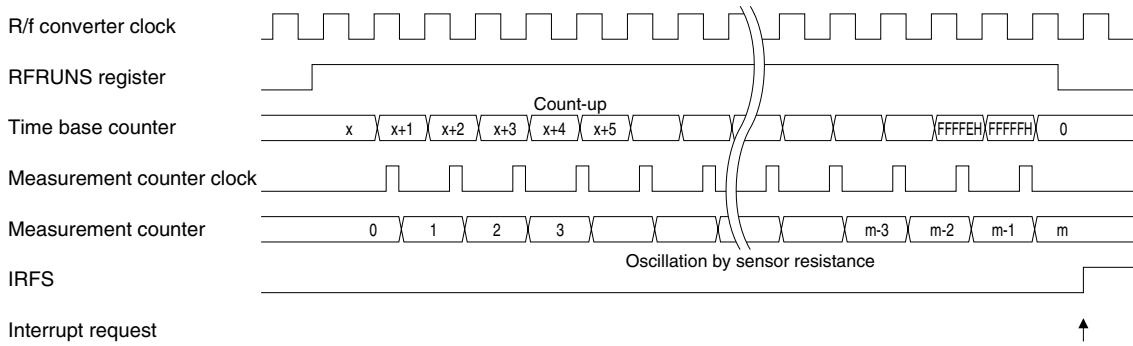


Fig. 4.13.5.2 Sensor oscillate completion interrupt

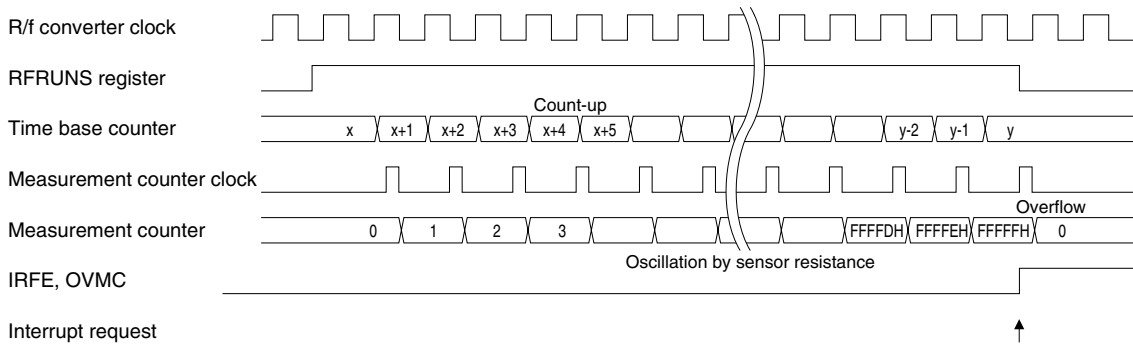


Fig. 4.13.5.3 Error interrupt due to measurement counter overflow

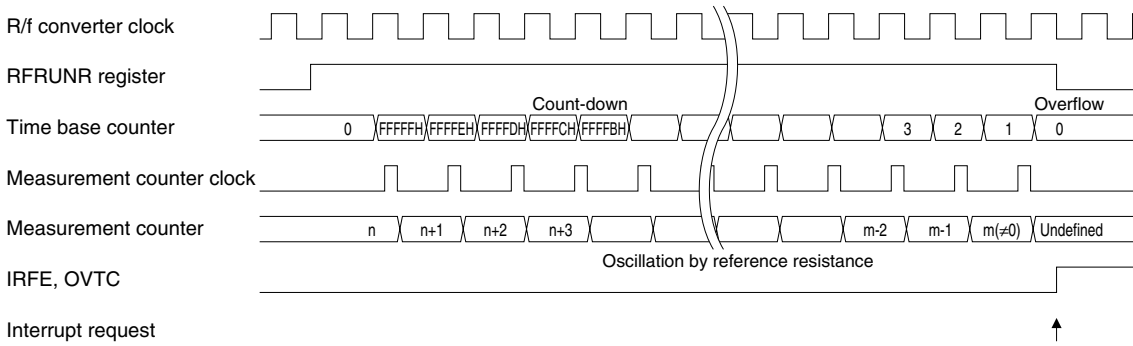


Fig. 4.13.5.4 Error interrupt due to time base counter overflow

Note: When an error interrupt occurs, reset the overflow flag (OVMC or OVTC) by writing "1". The same error interrupt will occur again if the overflow flag is not reset.

4.13.6 Continuous oscillation function

By setting the RFCNT register to "1", the reference oscillation or sensor oscillation can be continued even if the stop condition has been met. This function with RFOUT enabled allows easy measurement of the CR oscillation frequency.

Note: An interrupt will occur when an interrupt condition has been met even if RFCNT is set to "1".

4.13.7 I/O memory of R/f converter

Table 4.13.7.1 shows the I/O addresses and the control bits for the R/f converter.

Table 4.13.7.1(a) Control bits of R/f converter

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF15H	General	RFCKS2	RFCKS1	RFCKS0	General	0	1	0	General-purpose register
					RFCKS2	0			R/f converter clock frequency selection [RFCKS2–0] 0 1 2 3 / Frequency Off fOSC1 fOSC1/2 fOSC1/4
					RFCKS1	0			[RFCKS2–0] 4 5 6 7 / Frequency PT1 fOSC3 fOSC3/2 fOSC3/4
	R/W				RFCKS0	0			
FF60H	RFCNT	RFOUT	ERF1	ERF0	RFCNT	0	Continue	Normal	Continuous oscillation enable
					RFOUT	0	Enable	Disable	RFOUT enable
					ERF1	0			R/f conversion selection [ERF1, 0] 0 1 2 3 / R/f conversion I/O Ch.0 DC Ch.1 AC Ch.1 DC
	R/W				ERF0	0			
FF61H	OVTC	OVMC	RFRUNR	RFRUNS	OVTC	0	Overflow	Non-ov	Time base counter overflow flag
					OVMC	0	Overflow	Non-ov	Measurement counter overflow flag
					RFRUNR	0	Run	Stop	Reference oscillation Run control/status
	R/W				RFRUNS	0	Run	Stop	Sensor oscillation Run control/status
FF62H	MC3	MC2	MC1	MC0	MC3	– *2			Measurement counter MC0–MC3
					MC2	– *2			
					MC1	– *2			
	R/W				MC0	– *2			LSB
FF63H	MC7	MC6	MC5	MC4	MC7	– *2			Measurement counter MC4–MC7
					MC6	– *2			
					MC5	– *2			
	R/W				MC4	– *2			
FF64H	MC11	MC10	MC9	MC8	MC11	– *2			Measurement counter MC8–MC11
					MC10	– *2			
					MC9	– *2			
	R/W				MC8	– *2			
FF65H	MC15	MC14	MC13	MC12	MC15	– *2			Measurement counter MC12–MC15
					MC14	– *2			
					MC13	– *2			
	R/W				MC12	– *2			
FF66H	MC19	MC18	MC17	MC16	MC19	– *2			MSB
					MC18	– *2			Measurement counter MC16–MC19
					MC17	– *2			
	R/W				MC16	– *2			
FF67H	TC3	TC2	TC1	TC0	TC3	– *2			Time base counter TC0–TC3
					TC2	– *2			
					TC1	– *2			
	R/W				TC0	– *2			
FF68H	TC7	TC6	TC5	TC4	TC7	– *2			Time base counter TC4–TC7
					TC6	– *2			
					TC5	– *2			
	R/W				TC4	– *2			
FF69H	TC11	TC10	TC9	TC8	TC11	– *2			Time base counter TC8–TC11
					TC10	– *2			
					TC9	– *2			
	R/W				TC8	– *2			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.13.7.1(b) Control bits of R/f converter

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF6AH	TC15	TC14	TC13	TC12	TC15	– *2			Time base counter TC12–TC15
					TC14	– *2			
	R/W				TC13	– *2			
					TC12	– *2			
FF6BH	TC19	TC18	TC17	TC16	TC19	– *2			MSB Time base counter TC16–TC19
					TC18	– *2			
	R/W				TC17	– *2			
					TC16	– *2			
FFE1H	General	EIRFE	EIRFR	EIRFS	General	0	1	0	General-purpose register
					EIRFE	0	Enable	Mask	Interrupt mask register (R/f converter error)
	R/W				EIRFR	0	Enable	Mask	Interrupt mask register (R/f converter reference oscillate completion)
					EIRFS	0	Enable	Mask	Interrupt mask register (R/f converter sensor oscillate completion)
FFF1H	0	IRFE	IRFR	IRFS	0 *3	– *2	(R)	(R)	Unused
					IRFE	0	Yes	No	Interrupt factor flag (R/f converter error)
	R	R/W			IRFR	0	(W)	(W)	Interrupt factor flag (R/f converter reference oscillate completion)
					IRFS	0	Reset	Invalid	Interrupt factor flag (R/f converter sensor oscillate completion)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

RFCKS0–RFCKS2: R/f converter clock frequency select register (FF15H•D0–D2)

Selects the R/f converter clock frequency.

Table 4.13.7.2 R/f converter clock frequencies

RFCKS2	RFCKS1	RFCKS0	R/f converter clock
1	1	1	f_{OSC3} / 4
1	1	0	f_{OSC3} / 2
1	0	1	f_{OSC3} / 1
1	0	0	Programmable timer 1
0	1	1	f_{OSC1} / 4 (8 kHz)
0	1	0	f_{OSC1} / 2 (16 kHz)
0	0	1	f_{OSC1} / 1 (32 kHz)
0	0	0	Off

f_{OSC1}: OSC1 oscillation frequency. ( ) indicates the frequency when f_{OSC1} = 32 kHz.
f_{OSC3}: OSC3 oscillation frequency

When programmable timer 1 is selected, the programmable timer 1 underflow signal is divided by 2 before it is used as the R/f converter clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.8, "Programmable Timer" for controlling the programmable timer.
If it is not necessary to run the R/f converter, stop the clock supply by setting this register to "000B" to reduce current consumption.
At initial reset, this register is set to "000B".

ERF0, ERF1: R/f conversion select register (FF60H•D0–D1)

Selects the channel and sensor type to perform R/f conversion.

Table 4.13.7.3 Selecting channel and sensor type

ERF1	ERF0	Channel and sensor type
1	1	Ch.1 DC
1	0	Ch.1 AC
0	1	Ch.0 DC
0	0	I/O

DC: R/f conversion using a DC bias resistive sensor such as a thermistor
AC: R/f conversion using an AC bias resistive sensor such as a humidity sensor

The R/f converter channel 0 input/output terminals are shared with the I/O port (P00–P02). By setting this register to other than "00B", P00, P01 and P02 are configured as the RFIN0, REF0 and SEN0 terminals, respectively.
At initial reset, this register is set to "00B".

RFOUT: RFOUT enable register (FF60H•D2)

Enables RFOUT output from the P03 port.

When "1" is written: Enabled (RFOUT)
When "0" is written: Disabled (I/O port)
Reading: Valid

When using the RFOUT output, write "1" to RFOUT to set P03 as the RFOUT output port.
At initial reset, this register is set to "0".

RFCNT: Continuous oscillation enable register (FF60H•D3)

Enables the R/f converter to oscillate continuously.

When "1" is written: Continuous oscillation
When "0" is written: Normal oscillation
Reading: Valid

By writing "1" to RFCNT, the reference oscillation or sensor oscillation can be continued even if the stop condition has been met. This function with RFOUT enabled allows easy measurement of the CR oscillation frequency.
At initial reset, this register is set to "0".

RFRUNS: Sensor oscillation RUN control/status (FF61H•D0)

Starts R/f conversion for the sensor and indicates the operating (RUN/STOP) status.

When "1" is written: R/f conversion starts
When "0" is written: No operation

When "1" is read: RUN status
When "0" is read: STOP status

Writing "1" to RFRUNS starts an R/f conversion for the sensor. The register is held at "1" while the R/f conversion is being processed and is set to "0" when the R/f conversion has completed. Writing "0" during an R/f conversion stops the CR oscillation.
When the channel 1 sensor type (AC bias and DC bias) is changed by ERF0–ERF1 during sensor oscillation, RFRUNS is not reset. In this case, reset RFRUNS by writing "0".
If RFRUNS and RFRUNR are set to "1" simultaneously, RFRUNR is effective.
At initial reset, this register is set to "0".

RFRUNR: Reference oscillation RUN control/status (FF61H•D1)

Starts R/f conversion for the reference resistance and indicates the operating (RUN/STOP) status.

When "1" is written: R/f conversion starts
When "0" is written: No operation

When "1" is read: RUN status
When "0" is read: STOP status

Writing "1" to RFRUNR starts an R/f conversion for the reference resistance. The register is held at "1" while the R/f conversion is being processed and is set to "0" when the R/f conversion has completed. Writing "0" during an R/f conversion stops the CR oscillation.
When the channel 1 sensor type (AC bias and DC bias) is changed by ERF0–ERF1 during reference oscillation, RFRUNR is not reset. In this case, reset RFRUNR by writing "0". RFRUNR is reset when the channel for R/f conversion is changed.
If RFRUNS and RFRUNR are set to "1" simultaneously, RFRUNR is effective.
At initial reset, this register is set to "0".

OVMC: Measurement counter overflow flag (FF61H•D2)
Indicates whether the measurement counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred

When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the sensor, OVMC is set to "1" and an error interrupt occurs at the same time.
This flag is reset by writing "1" or starting R/f conversion.
At initial reset, this flag is set to "0".

OVTC: Time base counter overflow flag (FF61H•D3)
Indicates whether the time base counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred

When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the reference resistance, OVTC is set to "1" and an error interrupt occurs at the same time.
This flag is reset by writing "1" or starting R/f conversion.
At initial reset, this flag is set to "0".

MC0–MC19: Measurement counter (FF62H–FF66H)
The measurement counter counts up according to the CR oscillation clock. It permits writing and reading on a 4-bit basis.
The complement of the number of clocks to be counted by the oscillation of the reference resistance must be entered in this counter prior to reference oscillation. When the counter reaches "00000H" due to overflow, the oscillation of the reference resistance stops. When converting a sensor oscillation, "00000H" must be set in this register (it is unnecessary when it is done immediately after a reference oscillation has completed). The sensor oscillation and measurement counter stop when the time base counter overflows. Number of clocks counted by the sensor oscillation can be evaluated from the value indicated by the counter when it stops. Calculate the target value by processing the above counted number according to the program. Measurable range and the overflow of the counter must be taken into account when setting an initial value to be entered prior to R/f conversion.
At initial reset, this counter is undefined.

TC0–TC19: Time base counter (FF67H–FF6BH)
Writing and reading is possible on a 4-bit basis by the time base counter that is used to adjust the CR oscillation time between the reference resistance and the sensor.
The time base counter counts down during oscillation of the reference resistance and counts up to "00000H" during oscillation of the sensor.
"00000H" needs to be entered in the counter prior to a reference oscillation in order to adjust the CR oscillating time (number of clocks) of both counts. The counter value after a reference oscillation has completed should be read from this register and save it in the memory. The saved value should be set in this counter before starting a sensor oscillation.
At initial reset, this counter is undefined.

Note: When setting the measurement counter or time base counter, always write 5 words of data continuously in order from the lower address (FF62H → FF63H → FF64H → FF65H → FF66H, FF67H → FF68H → FF69H → FF6AH → FF6BH). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used. If data other than low-order 4 bits is written, the counter cannot be set to the desired value.

EIRFS, EIRFR, EIRFE: Interrupt mask registers (FFE1H•D0–D2)

Selects whether to mask interrupt with the R/f converter.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

EIRFS, EIRFR and EIRFE are the interrupt mask registers for the sensor oscillate completion interrupt, reference oscillate completion interrupt and error interrupt. The R/f converter interrupt is permitted when "1" is written to the interrupt mask register. When "0" is written, interrupt is masked.
At initial reset, these registers are set to "0".

IRFS, IRFR, IRFE: Interrupt factor flags (FFF1H•D0–D2)

These flags indicate the status of the R/f converter interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

IRFR is set to "1" when an R/f conversion for the reference resistor is completed.
IRFS is set to "1" when an R/f conversion for the sensor is completed.
IRFE is set to "1" when the time base counter overflows during reference oscillation or when the measurement counter overflows during sensor oscillation.
From the status of these flags, the software can decide whether an R/f converter interrupt has occurred. Further this flag is set in the above timing regardless of the interrupt mask register setting (except for debug mode). These flags are reset to "0" by writing "1". After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
After an initial reset, these flags are set to "0".

4.13.8 Programming notes

(1) When an error interrupt occurs, reset the overflow flag (OVMC or OVTC) by writing "1". The same error interrupt will occur again if the overflow flag is not reset.

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) When setting the measurement counter or time base counter, always write 5 words of data continuously in order from the lower address (FF62H → FF63H → FF64H → FF65H → FF66H, FF67H → FF68H → FF69H → FF6AH → FF6BH). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used. If data other than low-order 4 bits is written, the counter cannot be set to the desired value.

4.14 SVD (Supply Voltage Detection) Circuit

4.14.1 Configuration of SVD circuit

The S1C63632 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit on/off and the SVD criteria voltage setting can be done with software. Figure 4.14.1.1 shows the configuration of the SVD circuit.

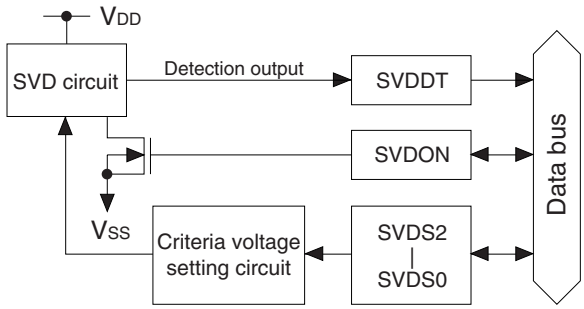


Fig. 4.14.1.1 Configuration of SVD circuit

4.14.2 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (VDD terminal–VSS terminal) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.

The criteria voltage can be selected from 16 types shown in Table 4.14.2.1 using the SVDS3–SVDS0 register.

Table 4.14.2.1 Criteria voltage

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
1	1	1	1	3.2
1	1	1	0	3.1
1	1	0	1	3.0
1	1	0	0	2.9
1	0	1	1	2.8
1	0	1	0	2.7
1	0	0	1	2.6
1	0	0	0	2.5
0	1	1	1	2.4
0	1	1	0	2.3
0	1	0	1	2.2
0	1	0	0	2.1
0	0	1	1	2.0
0	0	1	0	1.9
0	0	0	1	1.8
0	0	0	0	1.6

When the SVDON register is set to "1", supply voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes off. To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is on, the IC draws a large current, so keep the SVD circuit off unless it is.

4.14.3 I/O memory of SVD circuit

Table 4.14.3.1 shows the I/O addresses and the control bits for the SVD circuit.

Table 4.14.3.1 Control bits of SVD circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting
					SVDS2	0			[SVDS3–0] 0 1 2 3 4 5 6 7
	R/W				SVDS1	0			Voltage (V) 1.6 1.8 1.9 2.0 2.1 2.2 2.3 2.4
					SVDS0	0			[SVDS3–0] 8 9 10 11 12 13 14 15
									Voltage (V) 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SVDS3–SVDS0: SVD criteria voltage setting register (FF04H)

Criteria voltage for SVD is set as shown in Table 4.14.2.1.
At initial reset, this register is set to "0".

SVDON: SVD circuit On/Off register (FF05H•D0)

Turns the SVD circuit on and off.

When "1" is written: SVD circuit On
When "0" is written: SVD circuit Off
Reading: Valid

When SVDON is set to "1", a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec.
At initial reset, this register is set to "0".

SVDDT: SVD evaluation data (FF05H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

4.14.4 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned off because SVD operation increase current consumption.

4.15 Interrupt and HALT/SLEEP

<Interrupt types>

The S1C63632 provides the following interrupt functions.

External interrupt:	• Key input interrupt	(8 systems)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Programmable timer interrupt	(16 systems)
	• Serial interface interrupt	(1 system)
	• Clock timer interrupt	(8 systems)
	• Stopwatch timer interrupt	(4 systems)
	• R/f converter interrupt	(3 systems)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.15.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

<HALT/SLEEP>

The S1C63632 has the HALT and SLEEP functions that considerably reduce current consumption when it is not necessary.
The CPU enters HALT status when the HALT instruction is executed. In HALT status, the operation of the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.

When the CPU enters SLEEP status as the result of the SLP instruction, the CPU stops its operation and the OSC1 and OSC3 oscillation circuits are also stop.
Reactivating from SLEEP status can only be done by generation of a key input interrupt request from a P1x or P4x port. Therefore, set the following flag and the registers for the I/O port to be used to cancel SLEEP status before executing the SLP instruction.
- Interrupt flag (I flag) = "1" (interrupts are enabled)
- Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected)
- Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled)
- Noise rejector select register NRSPxx = "00" (noise rejector is bypassed)

When SLEEP status is canceled by an I/O port interrupt, wait for oscillation to stabilize, then restart the CPU operation (input port interrupt processing).
Refer to the "S1C63000 Core CPU Manual" for transition to the HALT/SLEEP status and timing of its cancellation.

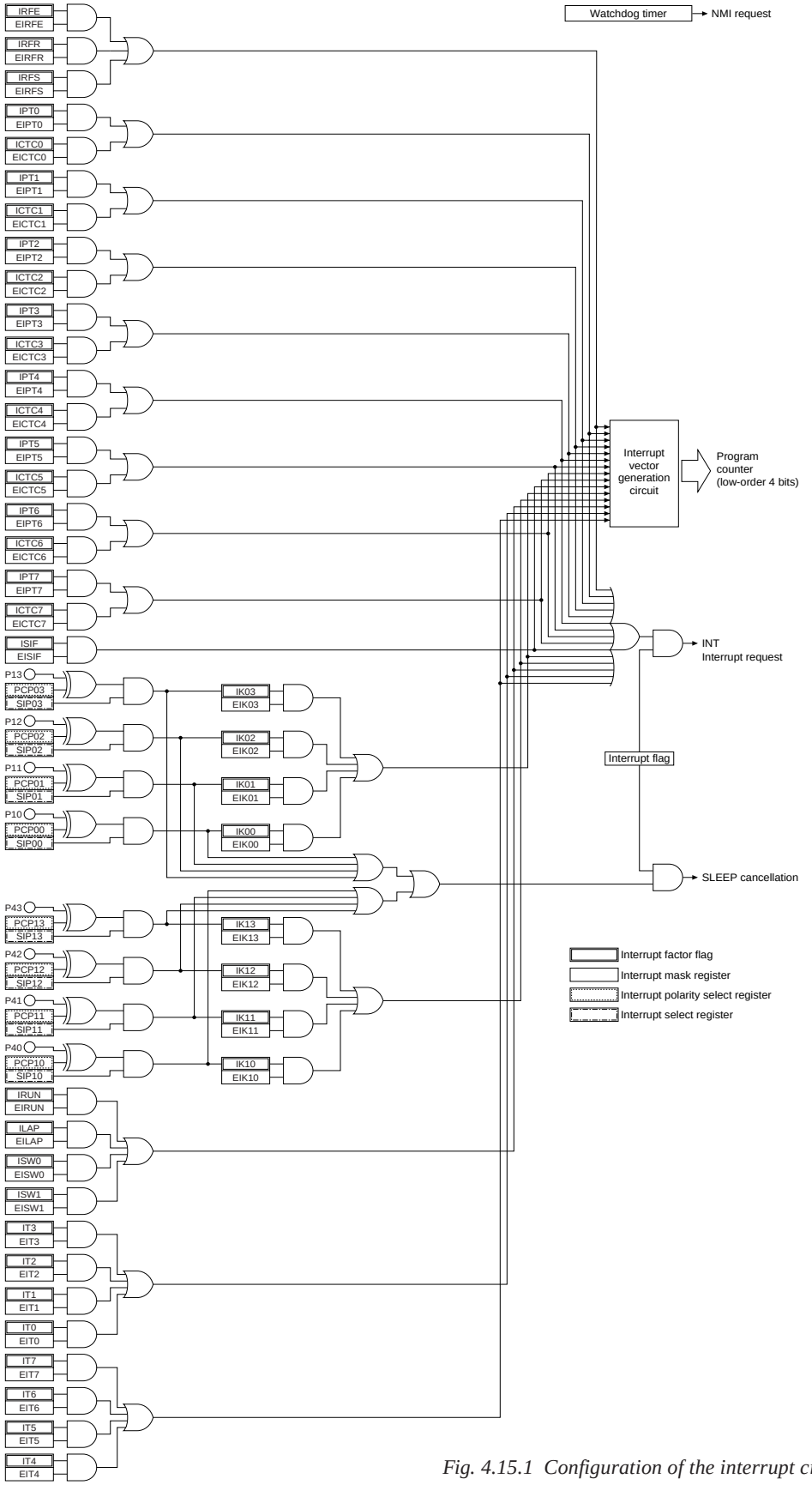


Fig. 4.15.1 Configuration of the interrupt circuit

4.15.1 Interrupt factor

Table 4.15.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.
At initial reset, the interrupt factor flags are reset to "0".

∗ Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.15.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
R/f converter (error)	IRFE	(FFF1H•D2)
R/f converter (end of reference conversion)	IRFR	(FFF1H•D1)
R/f converter (end of sensor conversion)	IRFS	(FFF1H•D0)
Programmable timer 0 (underflow)	IPT0	(FFF2H•D1)
Programmable timer 0 (compare match)	ICTC0	(FFF2H•D0)
Programmable timer 1 (underflow)	IPT1	(FFF3H•D1)
Programmable timer 1 (compare match)	ICTC1	(FFF3H•D0)
Programmable timer 2 (underflow)	IPT2	(FFF4H•D1)
Programmable timer 2 (compare match)	ICTC2	(FFF4H•D0)
Programmable timer 3 (underflow)	IPT3	(FFF5H•D1)
Programmable timer 3 (compare match)	ICTC3	(FFF5H•D0)
Programmable timer 4 (underflow)	IPT4	(FFF6H•D1)
Programmable timer 4 (compare match)	ICTC4	(FFF6H•D0)
Programmable timer 5 (underflow)	IPT5	(FFF7H•D1)
Programmable timer 5 (compare match)	ICTC5	(FFF7H•D0)
Programmable timer 6 (underflow)	IPT6	(FFF8H•D1)
Programmable timer 6 (compare match)	ICTC6	(FFF8H•D0)
Programmable timer 7 (underflow)	IPT7	(FFF9H•D1)
Programmable timer 7 (compare match)	ICTC7	(FFF9H•D0)
Serial interface (8-bit data input/output completion)	ISIF	(FFFAH•D0)
Key input interrupt <P13>	IK03	(FFFBH•D3)
Key input interrupt <P12>	IK02	(FFFBH•D2)
Key input interrupt <P11>	IK01	(FFFBH•D1)
Key input interrupt <P10>	IK00	(FFFBH•D0)
Key input interrupt <P43>	IK13	(FFFCH•D3)
Key input interrupt <P42>	IK12	(FFFCH•D2)
Key input interrupt <P41>	IK11	(FFFCH•D1)
Key input interrupt <P40>	IK10	(FFFCH•D0)
Stopwatch timer (Direct RUN)	IRUN	(FFFDH•D3)
Stopwatch timer (Direct LAP)	ILAP	(FFFDH•D2)
Stopwatch timer (1 Hz)	ISW1	(FFFDH•D1)
Stopwatch timer (10 Hz)	ISW10	(FFFDH•D0)
Clock timer 16 Hz (falling edge)	IT3	(FFFEH•D3)
Clock timer 32 Hz (falling edge)	IT2	(FFFEH•D2)
Clock timer 64 Hz (falling edge)	IT1	(FFFEH•D1)
Clock timer 128 Hz (falling edge)	IT0	(FFFEH•D0)
Clock timer 1 Hz (falling edge)	IT7	(FFFFH•D3)
Clock timer 2 Hz (falling edge)	IT6	(FFFFH•D2)
Clock timer 4 Hz (falling edge)	IT5	(FFFFH•D1)
Clock timer 8 Hz (falling edge)	IT4	(FFFFH•D0)

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.15.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is reset to "0".
Table 4.15.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.15.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIRFE	(FFE1H•D2)	IRFE	(FFF1H•D2)
EIRFR	(FFE1H•D1)	IRFR	(FFF1H•D1)
EIRFS	(FFE1H•D0)	IRFS	(FFF1H•D0)
EIPT0	(FFE2H•D1)	IPT0	(FFF2H•D1)
EICTC0	(FFE2H•D0)	ICTC0	(FFF2H•D0)
EIPT1	(FFE3H•D1)	IPT1	(FFF3H•D1)
EICTC1	(FFE3H•D0)	ICTC1	(FFF3H•D0)
EIPT2	(FFE4H•D1)	IPT2	(FFF4H•D1)
EICTC2	(FFE4H•D0)	ICTC2	(FFF4H•D0)
EIPT3	(FFE5H•D1)	IPT3	(FFF5H•D1)
EICTC3	(FFE5H•D0)	ICTC3	(FFF5H•D0)
EIPT4	(FFE6H•D1)	IPT4	(FFF6H•D1)
EICTC4	(FFE6H•D0)	ICTC4	(FFF6H•D0)
EIPT5	(FFE7H•D1)	IPT5	(FFF7H•D1)
EICTC5	(FFE7H•D0)	ICTC5	(FFF7H•D0)
EIPT6	(FFE8H•D1)	IPT6	(FFF8H•D1)
EICTC6	(FFE8H•D0)	ICTC6	(FFF8H•D0)
EIPT7	(FFE9H•D1)	IPT7	(FFF9H•D1)
EICTC7	(FFE9H•D0)	ICTC7	(FFF9H•D0)
EISEIF	(FFEAH•D0)	ISIF	(FFFAH•D0)
EIK03	(FFEBH•D3)	IK03	(FFFBH•D3)
EIK02	(FFEBH•D2)	IK02	(FFFBH•D2)
EIK01	(FFEBH•D1)	IK01	(FFFBH•D1)
EIK00	(FFEBH•D0)	IK00	(FFFBH•D0)
EIK13	(FFECH•D3)	IK13	(FFFCH•D3)
EIK12	(FFECH•D2)	IK12	(FFFCH•D2)
EIK11	(FFECH•D1)	IK11	(FFFCH•D1)
EIK10	(FFECH•D0)	IK10	(FFFCH•D0)
EIRUN	(FFEDH•D3)	IRUN	(FFFDH•D3)
EILAP	(FFEDH•D2)	ILAP	(FFFDH•D2)
EISW1	(FFEDH•D1)	ISW1	(FFFDH•D1)
EISW10	(FFEDH•D0)	ISW10	(FFFDH•D0)
EIT3	(FFEEH•D3)	IT3	(FFFEH•D3)
EIT2	(FFEEH•D2)	IT2	(FFFEH•D2)
EIT1	(FFEEH•D1)	IT1	(FFFEH•D1)
EIT0	(FFEEH•D0)	IT0	(FFFEH•D0)
EIT7	(FFEFH•D3)	IT7	(FFFFH•D3)
EIT6	(FFEFH•D2)	IT6	(FFFFH•D2)
EIT5	(FFEFH•D1)	IT5	(FFFFH•D1)
EIT4	(FFEFH•D0)	IT4	(FFFFH•D0)

4.15.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

1 The content of the flag register is evacuated, then the I flag is reset.
2 The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).
3 The interrupt request causes the value of the interrupt vector (0100H–010FH) to be set in the program counter.
4 The program at the specified address is executed (execution of interrupt handler routine by software).

Table 4.15.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.15.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High
0101H	R/f converter	↑
0102H	Programmable timer 0	
0103H	Programmable timer 1	
0104H	Programmable timer 2	
0105H	Programmable timer 3	
0106H	Programmable timer 4	
0107H	Programmable timer 5	
0108H	Programmable timer 6	
0109H	Programmable timer 7	
010AH	Serial interface	
010BH	Key input interrupt <P1>	
010CH	Key input interrupt <P4>	
010DH	Stopwatch timer	
010EH	Clock timer (128 Hz, 64 Hz, 32 Hz, 16 Hz)	↓
010FH	Clock timer (8 Hz, 4 Hz, 2 Hz, 1 Hz)	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

Note: The interrupt handler routine must be located within the range from "Interrupt vector address (100H–10FH)" -7FH to +80H. If it is difficult, make a relay point within that range as the destination of the vector jump and branch the program to the interrupt handler from there.
Example:

```
;************************************************************************
;**  interrupt vector area  **
;************************************************************************
      .org  0x0100
      JR    INT_DUMMY   ;WATCH DOG TIMER INTERRUPT VECTOR(0x100)
      JR    INT_RFC     ;RFC INTERRUPT VECTOR(0x101)
      JR    INT_DUMMY   ;PTIMER0 INTERRUPT VECTOR(0x102)
      JR    INT_DUMMY   ;PTIMER1 INTERRUPT VECTOR(0x103)
      JR    INT_DUMMY   ;PTIMER2 INTERRUPT VECTOR(0x104)
      JR    INT_DUMMY   ;PTIMER3 INTERRUPT VECTOR(0x105)
      JR    INT_DUMMY   ;PTIMER4 INTERRUPT VECTOR(0x106)
      JR    INT_DUMMY   ;PTIMER5 INTERRUPT VECTOR(0x107)
      JR    INT_DUMMY   ;PTIMER6 INTERRUPT VECTOR(0x108)
      JR    INT_DUMMY   ;PTIMER7 INTERRUPT VECTOR(0x109)
      JR    INT_DUMMY   ;SIO INTERRUPT VECTOR(0x10A)
      JR    INT_DUMMY   ;P1x PORT INTERRUPT VECTOR(0x10B)
      JR    INT_DUMMY   ;P4x PORT INTERRUPT VECTOR(0x10C)
      JR    INT_DUMMY   ;STOPWATCH INTERRUPT VECTOR(0x10D)
      JR    INT_DUMMY   ;CLOCK TIMER1 INTERRUPT VECTOR(0x10E)
      JR    INT_DUMMY   ;CLOCK TIMER2 INTERRUPT VECTOR(0x10F)
```

```
;*****************************************************************************
;**  subinterrupt vector area  **
;*****************************************************************************
      .org  0x120
INT_RFC:
      CALR  INTRFC      ;call Interrupt RFC
      RETI
INT_DUMMY:
      RETI

;*****************************************************************************
;**  Interrupt RFC  **
;*****************************************************************************
      .org  0x800
INTRFC:
      LDB   %yl,P5CTL0@l
      LDB   %xl,ITC_RFC1@l
      LD    [%y],[%x]   ;Port Output
      RET
```

4.15.4 I/O memory of interrupt

Tables 4.15.4.1 shows the I/O addresses and the control bits for controlling interrupts.

Table 4.15.4.1(a) Control bits of interrupt

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF3CH	SIP03	SIP02	SIP01	SIP00	SIP03	0	Enable	Disable	P10–P13 interrupt select register
					SIP02	0	Enable	Disable	
	R/W				SIP01	0	Enable	Disable	
					SIP00	0	Enable	Disable	
FF3DH	PCP03	PCP02	PCP01	PCP00	PCP03	1	↓	↑	P10–P13 interrupt polarity select register
					PCP02	1	↓	↑	
	R/W				PCP01	1	↓	↑	
					PCP00	1	↓	↑	
FF3EH	SIP13	SIP12	SIP11	SIP10	SIP13	0	Enable	Disable	P40–P43 interrupt select register
					SIP12	0	Enable	Disable	
	R/W				SIP11	0	Enable	Disable	
					SIP10	0	Enable	Disable	
FF3FH	PCP13	PCP12	PCP11	PCP10	PCP13	1	↓	↑	P40–P43 interrupt polarity select register
					PCP12	1	↓	↑	
	R/W				PCP11	1	↓	↑	
					PCP10	1	↓	↑	
FFE1H	General	EIRFE	EIRFR	EIRFS	General	0	1	0	General-purpose register
					EIRFE	0	Enable	Mask	Interrupt mask register (R/f converter error)
	R/W				EIRFR	0	Enable	Mask	Interrupt mask register (R/f converter reference oscillate completion)
					EIRFS	0	Enable	Mask	Interrupt mask register (R/f converter sensor oscillate completion)
FFE2H	General	General	EIPT0	EICTC0	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 underflow)
					EICTC0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 compare match)
FFE3H	General	General	EIPT1	EICTC1	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 underflow)
					EICTC1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 compare match)
FFE4H	General	General	EIPT2	EICTC2	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT2	0	Enable	Mask	Interrupt mask register (Programmable timer 2 underflow)
					EICTC2	0	Enable	Mask	Interrupt mask register (Programmable timer 2 compare match)
FFE5H	General	General	EIPT3	EICTC3	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT3	0	Enable	Mask	Interrupt mask register (Programmable timer 3 underflow)
					EICTC3	0	Enable	Mask	Interrupt mask register (Programmable timer 3 compare match)
FFE6H	General	General	EIPT4	EICTC4	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT4	0	Enable	Mask	Interrupt mask register (Programmable timer 4 underflow)
					EICTC4	0	Enable	Mask	Interrupt mask register (Programmable timer 4 compare match)
FFE7H	General	General	EIPT5	EICTC5	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT5	0	Enable	Mask	Interrupt mask register (Programmable timer 5 underflow)
					EICTC5	0	Enable	Mask	Interrupt mask register (Programmable timer 5 compare match)
FFE8H	General	General	EIPT6	EICTC6	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT6	0	Enable	Mask	Interrupt mask register (Programmable timer 6 underflow)
					EICTC6	0	Enable	Mask	Interrupt mask register (Programmable timer 6 compare match)
FFE9H	General	General	EIPT7	EICTC7	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				EIPT7	0	Enable	Mask	Interrupt mask register (Programmable timer 7 underflow)
					EICTC7	0	Enable	Mask	Interrupt mask register (Programmable timer 7 compare match)
FFEAH	General	General	General	EISIF	General	0	1	0	General-purpose register
					General	0	1	0	General-purpose register
	R/W				General	0	1	0	General-purpose register
					EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.15.4.1(b) Control bits of interrupt

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFEBH	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (Key input interrupt 3 <P13>)
					EIK02	0	Enable	Mask	Interrupt mask register (Key input interrupt 2 <P12>)
					EIK01	0	Enable	Mask	Interrupt mask register (Key input interrupt 1 <P11>)
	R/W				EIK00	0	Enable	Mask	Interrupt mask register (Key input interrupt 0 <P10>)
FFECH	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (Key input interrupt 7 <P43>)
					EIK12	0	Enable	Mask	Interrupt mask register (Key input interrupt 6 <P42>)
					EIK11	0	Enable	Mask	Interrupt mask register (Key input interrupt 5 <P41>)
	R/W				EIK10	0	Enable	Mask	Interrupt mask register (Key input interrupt 4 <P40>)
FFEDH	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
					EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
	R/W				EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFEEH	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
					EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 64 Hz)
	R/W				EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 128 Hz)
FFEFH	EIT7	EIT6	EIT5	EIT4	EIT7	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT6	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
					EIT5	0	Enable	Mask	Interrupt mask register (Clock timer 4 Hz)
	R/W				EIT4	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
FFF1H	0	IRFE	IRFR	IRFS	0 *3	– *2	(R)	(R)	Unused
					IRFE	0	Yes	No	Interrupt factor flag (R/f converter error)
	R	R/W			IRFR	0	(W)	(W)	Interrupt factor flag (R/f converter reference oscillate completion)
					IRFS	0	Reset	Invalid	Interrupt factor flag (R/f converter sensor oscillate completion)
FFF2H	0	0	IPT0	ICTC0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT0	0	(W)	(W)	Interrupt factor flag (Programmable timer 0 underflow)
					ICTC0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0 compare match)
FFF3H	0	0	IPT1	ICTC1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1 underflow)
					ICTC1	0	Reset	Invalid	Interrupt factor flag (Programmable timer 1 compare match)
FFF4H	0	0	IPT2	ICTC2	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT2	0	(W)	(W)	Interrupt factor flag (Programmable timer 2 underflow)
					ICTC2	0	Reset	Invalid	Interrupt factor flag (Programmable timer 2 compare match)
FFF5H	0	0	IPT3	ICTC3	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT3	0	(W)	(W)	Interrupt factor flag (Programmable timer 3 underflow)
					ICTC3	0	Reset	Invalid	Interrupt factor flag (Programmable timer 3 compare match)
FFF6H	0	0	IPT4	ICTC4	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT4	0	(W)	(W)	Interrupt factor flag (Programmable timer 4 underflow)
					ICTC4	0	Reset	Invalid	Interrupt factor flag (Programmable timer 4 compare match)
FFF7H	0	0	IPT5	ICTC5	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT5	0	(W)	(W)	Interrupt factor flag (Programmable timer 5 underflow)
					ICTC5	0	Reset	Invalid	Interrupt factor flag (Programmable timer 5 compare match)
FFF8H	0	0	IPT6	ICTC6	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT6	0	(W)	(W)	Interrupt factor flag (Programmable timer 6 underflow)
					ICTC6	0	Reset	Invalid	Interrupt factor flag (Programmable timer 6 compare match)
FFF9H	0	0	IPT7	ICTC7	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT7	0	(W)	(W)	Interrupt factor flag (Programmable timer 7 underflow)
					ICTC7	0	Reset	Invalid	Interrupt factor flag (Programmable timer 7 compare match)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.15.4.1(c) Control bits of interrupt

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFFAH	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial interface)
FFFBH	IK03	IK02	IK01	IK00	IK03	0	(R)	(R)	Interrupt factor flag (Key input interrupt 3 <P13>)
					IK02	0	Yes	No	Interrupt factor flag (Key input interrupt 2 <P12>)
	R/W				IK01	0	(W)	(W)	Interrupt factor flag (Key input interrupt 1 <P11>)
					IK00	0	Reset	Invalid	Interrupt factor flag (Key input interrupt 0 <P10>)
FFFCH	IK13	IK12	IK11	IK10	IK13	0	(R)	(R)	Interrupt factor flag (Key input interrupt 7 <P43>)
					IK12	0	Yes	No	Interrupt factor flag (Key input interrupt 6 <P42>)
	R/W				IK11	0	(W)	(W)	Interrupt factor flag (Key input interrupt 5 <P41>)
					IK10	0	Reset	Invalid	Interrupt factor flag (Key input interrupt 4 <P40>)
FFFDH	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)
FFFEH	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 16 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 64 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 128 Hz)
FFFFH	IT7	IT6	IT5	IT4	IT7	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT6	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT5	0	(W)	(W)	Interrupt factor flag (Clock timer 4 Hz)
					IT4	0	Reset	Invalid	Interrupt factor flag (Clock timer 8 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

SIP03–SIP00, SIP13–SIP10: Interrupt select registers (FF3CH, FF3EH)
PCP03–PCP00, PCP13–PCP10: Interrupt polarity select registers (FF3DH, FF3FH)
EIK03–EIK00, EIK13–EIK10: Interrupt mask registers (FFEBH, FFECH)
IK03–IK00, IK13–IK10: Interrupt factor flags (FFFBH, FFFCH)

Refer to Section 4.5, "I/O Ports".

EIRFE, EIRFR, EIRFS: Interrupt mask registers (FFE1H•D2, D1, D0)
IRFE, IRFR, IRFS: Interrupt factor flags (FFF1H•D2, D1, D0)

Refer to Section 4.13, "R/f Converter".

EIPT0, EICTC0: Interrupt mask registers (FFE2H•D1, D0)
EIPT1, EICTC1: Interrupt mask registers (FFE3H•D1, D0)
EIPT2, EICTC2: Interrupt mask registers (FFE4H•D1, D0)
EIPT3, EICTC3: Interrupt mask registers (FFE5H•D1, D0)
EIPT4, EICTC4: Interrupt mask registers (FFE6H•D1, D0)
EIPT5, EICTC5: Interrupt mask registers (FFE7H•D1, D0)
EIPT6, EICTC6: Interrupt mask registers (FFE8H•D1, D0)
EIPT7, EICTC7: Interrupt mask registers (FFE9H•D1, D0)
IPT0, ICTC0: Interrupt factor flags (FFF2H•D1, D0)
IPT1, ICTC1: Interrupt factor flags (FFF3H•D1, D0)
IPT2, ICTC2: Interrupt factor flags (FFF4H•D1, D0)
IPT3, ICTC3: Interrupt factor flags (FFF5H•D1, D0)
IPT4, ICTC4: Interrupt factor flags (FFF6H•D1, D0)
IPT5, ICTC5: Interrupt factor flags (FFF7H•D1, D0)
IPT6, ICTC6: Interrupt factor flags (FFF8H•D1, D0)
IPT7, ICTC7: Interrupt factor flags (FFF9H•D1, D0)

Refer to Section 4.9, "Programmable Timer".

EISIF: Interrupt mask register (FFEAH•D0)
ISIF: Interrupt factor flag (FFFAH•D0)
Refer to Section 4.10, "Serial Interface".

EIRUN, EILAP, EISW1, EISW10: Interrupt mask registers (FFEDH)
IRUN, ILAP, ISW1, ISW10: Interrupt factor flags (FFFDH)
Refer to Section 4.8, "Stopwatch Timer".

EIT3–EIT0, EIT7–EIT4: Interrupt mask registers (FFEEH, FFEFH)
IT3–IT0, IT7–IT4: Interrupt factor flags (FFFEH, FFFFH)
Refer to Section 4.7, "Clock Timer".

4.15.5 Programming notes

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

(4) When using the SLEEP function, set the interrupt flag and the registers for the I/O port to be used to cancel SLEEP status as below before executing the SLP instruction.
- Interrupt flag (I flag) = "1" (interrupts are enabled)
- Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected)
- Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled)
- Noise rejector select register NRSPxx = "00" (noise rejector is bypassed)

(5) The interrupt handler routine must be located within the range from "Interrupt vector address (100H–10FH)" -7FH to +80H. If it is difficult, make a relay point within that range as the destination of the vector jump and branch the program to the interrupt handler from there.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The S1C63632 contains control registers for each of the circuits so that current consumption can be reduced.
These control registers reduce the current consumption through programs that operate the circuits at the minimum levels.
The following lists the circuits that can control operation and their control registers. Refer to these when programming.

Table 5.1.1 Circuits and control registers

Circuit (and item)	Control register
CPU	HALT and SLP instructions
CPU operating frequency	CLKCHG, OSCC
Power supply voltage booster/halver	DBON, HLON
LCD system voltage regulator	LPWR
SVD circuit	SVDON

Refer to Chapter 7, "Electrical Characteristics" for current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0")
OSC3 oscillation circuit is in off status (OSCC = "0")

Power supply voltage booster/halver: Off status (DBON = "0", HLON = "0")

LCD system voltage regulator: Off status (LPWR = "0")

SVD circuit: Off status (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

(1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Table 4.1.1 for the peripheral I/O area.

(2) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(3) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 1FFFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63632 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access. After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

Power control

(1) When the power supply voltage booster/halver is turned on, the V_{D2} output voltage requires about 1 msec to stabilize. Do not switch the power source for the voltage regulator (LCD system voltage regulator) to V_{D2} until the stabilization time has elapsed.

(2) HLON is prohibited from use, as it may cause malfunctions. Always be sure to set to "0".

(3) Do not set DBON to "1" (boost mode) and VCSEL to "1" (driving with V_{D2}) if the supply voltage V_{DD} exceeds 2.5 V, as it may cause damage of the IC.

(4) Current consumption increases in heavy load protection mode, therefore do not set heavy load protection mode with software if unnecessary.

Watchdog timer

When the watchdog timer is being used, the software must reset it within 3-second cycles. Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Oscillation circuit

(1) When the high speed CPU operation is not necessary, you should operate the peripheral circuits according to the setting outline indicate below.
- CPU operating clock: OSC1
- OSC3 oscillation circuit: Off

(When the OSC3 clock is not necessary for some peripheral circuits.)

(2) Since 1 msec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit on. Consequently, you should switch the CPU operating clock (OSC1 → OSC3) after allowing for a sufficient waiting time once the OSC3 oscillation goes on. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "Electrical Characteristics".)

(3) When switching the clock from OSC3 to OSC1, be sure to switch OSC3 oscillation off with separate instructions. Using a single instruction to process simultaneously can cause a malfunction of the CPU.

(4) The S1C63632 supports the SLEEP function and both the OSC1 and OSC3 oscillation circuits stop oscillating when the CPU enters SLEEP mode. To prevent the CPU from a malfunction when it resumes operating from SLEEP mode, switch the CPU clock to OSC1 before placing the CPU into SLEEP mode.

I/O port

(1) When an I/O ports in input mode is changed from high to low by the pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input data, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 375 kΩ (Max.)

(2) Be sure to turn the noise rejector off before executing the SLP instruction.

(3) Reactivating from SLEEP status can only be done by generation of a key input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt select register (SIPxx = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction. Furthermore, enable the key input interrupt using the corresponding interrupt mask register (EIKxx = "1") before executing the SLP instruction to run key input interrupt handler routine after SLEEP status is released.

(4) A hazard may occur when the TOUT_A–TOUT_D and FOUT signals are turned on and off.

(5) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output. Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

(6) Before the port function is configured, the circuit that uses the port (e.g. input interrupt, multiple key entry reset, serial interface, event counter input, direct RUN/LAP input for stopwatch) must be disabled.

LCD driver

(1) When a program that access no memory implemented area (F080H–F0FFH, F180H–F1FFH, F280H–F2FFH, F380H–F3FFH) is made, the operation is not guaranteed.

(2) When driving the LCD system voltage regulator with V_{D2}, wait at least 1 msec for stabilization of the voltage before switching the power voltage for the LCD system voltage regulator to V_{D2} using VCSEL after the power supply voltage booster/halver is turned on.

Clock timer

(1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) The clock timer count clock does not synch with the CPU clock. Therefore, the correct value may not be obtained depending on the count data read and count-up timings. To avoid this problem, the clock timer count data should be read by one of the procedures shown below.

- Read the count data twice and verify if there is any difference between them.
- Temporarily stop the clock timer when the counter data is read to obtain proper data.

Stopwatch timer

(1) The interrupt factor flag should be reset after resetting the stopwatch timer.

(2) Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

(3) When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWD8–11 and check whether the data has been renewed or not.

(4) When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

Programmable timer

(1) When reading counter data, be sure to read the low-order 4 bits (PTDx0–PTDx3) first. The high-order 4 bits (PTDx4–PTDx7) are latched when the low-order 4 bits are read and they are held until the next reading of the low-order 4 bits. In 16-bit timer mode, the high-order 12 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.
When the CPU is running with the OSC1 clock and the programmable timer is running with the OSC3 clock, stop the timer before reading the counter data to read the proper data.

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.

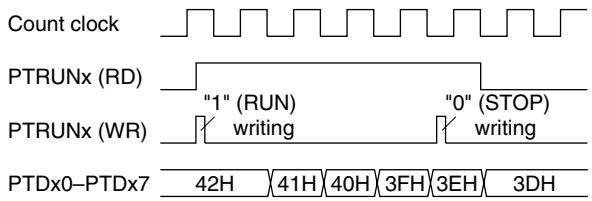


Fig. 5.2.1 Timing chart for RUN/STOP control (timer mode)

In event counter mode, the timer starts counting at the first event clock.

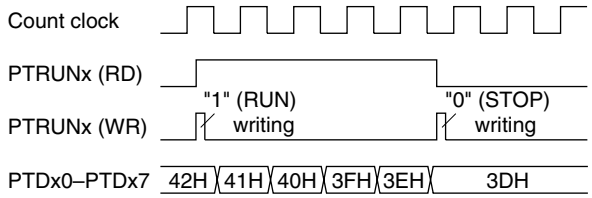


Fig. 5.2.2 Timing chart for RUN/STOP control (event counter mode)

(3) Since the TOUT_A–TOUT_D signals are generated asynchronously from the PTOUT_A–PTOUT_D registers, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the off state.

(5) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

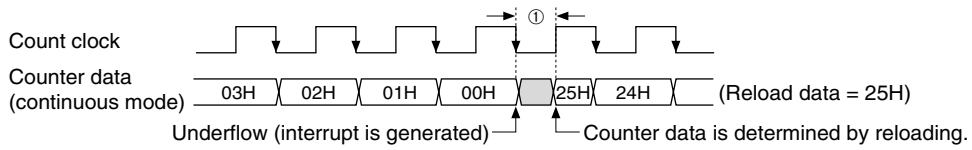


Fig. 5.2.3 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

(6) The programmable timer count clock does not synch with the CPU clock. Therefore, the correct value may not be obtained depending on the count data read and count-up timings. To avoid this problem, the programmable timer count data should be read by one of the procedures shown below.

- Read the count data twice and verify if there is any difference between them.
- Temporarily stop the programmable timer when the counter data is read to obtain proper data.

Serial interface

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when the programmable timer is used as the clock source or the serial interface is used in slave mode.

Sound generator

(1) Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

(2) The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

Integer multiplier

An operation process takes 10 CPU clock cycles (5 bus cycles) after writing to the calculation mode select register CALMD until the operation result is set to the destination register DRH/DRL and the operation flags. While this operation process, do not read/write from/to the destination register DRH/DRL and do not read NF/VF/ZF.

R/f converter

(1) When an error interrupt occurs, reset the overflow flag (OVMC or OVTC) by writing "1". The same error interrupt will occur again if the overflow flag is not reset.

(2) When setting the measurement counter or time base counter, always write 5 words of data continuously in order from the lower address (FF62H → FF63H → FF64H → FF65H → FF66H, FF67H → FF68H → FF69H → FF6AH → FF6BH). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used. If data other than low-order 4 bits is written, the counter cannot be set to the desired value.

SVD circuit

(1) To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned off because SVD operation increase current consumption.

Interrupt

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

(4) When using the SLEEP function, set the interrupt flag and the registers for the I/O port to be used to cancel SLEEP status as below before executing the SLP instruction.
- Interrupt flag (I flag) = "1" (interrupts are enabled)
- Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected)
- Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled)
- Noise rejector select register NRSPxx = "00" (noise rejector is bypassed)

(5) The interrupt handler routine must be located within the range from "Interrupt vector address (100H–10FH)" -7FH to +80H. If it is difficult, make a relay point within that range as the destination of the vector jump and branch the program to the interrupt handler from there.

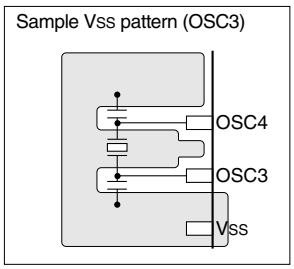
5.3 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals. Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VDD, please keep enough distance between OSC1/OSC3 and VDD or other signals on the board pattern.

<Reset Circuit>

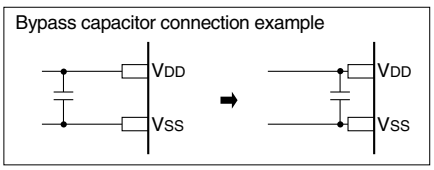
- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product. When using the built-in pull-down resistor of the RESET terminal, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD and VSS terminals with patterns as short and large as possible.

  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.

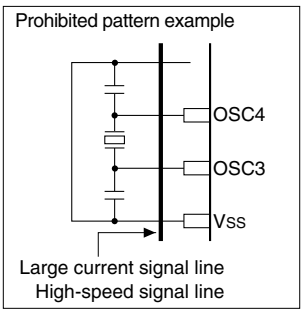


  (3) Components which are connected to the VD1, VD2, VOSC and VC1–VC5 terminals, such as capacitors, should be connected in the shortest line.
  In particular, the VC1–VC5 voltages affect the display quality.

- Do not connect anything to the VC1–VC5 terminals when the LCD driver is not used.

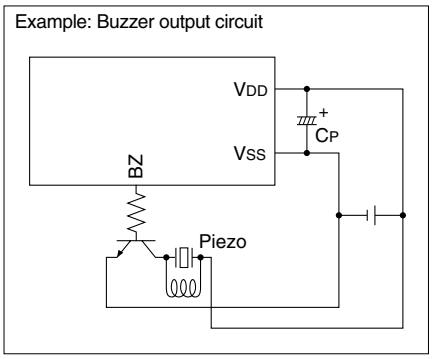
<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit and analog input unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit and analog input unit.



<Output Terminals>

- When an output terminal is used to drive an external component that consumes a large amount of current, the operation of the external component affects the built-in power supply circuit of this IC and the output voltage may vary. When driving a bipolar transistor by a periodic signal such as the BZ or timer output in particular, it may cause variations in the voltage output from the LCD system voltage circuit that affects the contrast of the LCD display. To prevent this, separate the traces on the printed circuit board. Put one between the power supply and the IC's VDD and VSS terminals, and another between the power supply and the external component that consumes the large amount of current. Furthermore, use an external component with as low a current consumption as possible.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change electrical characteristics. It may cause the IC to malfunction or the nonvolatile memory data to be erased. When developing products, consider the following precautions to prevent malfunctions caused by visible radiation.

  (1) Design the product and bond the IC on the board so that it is shielded from visible radiation in actual use.

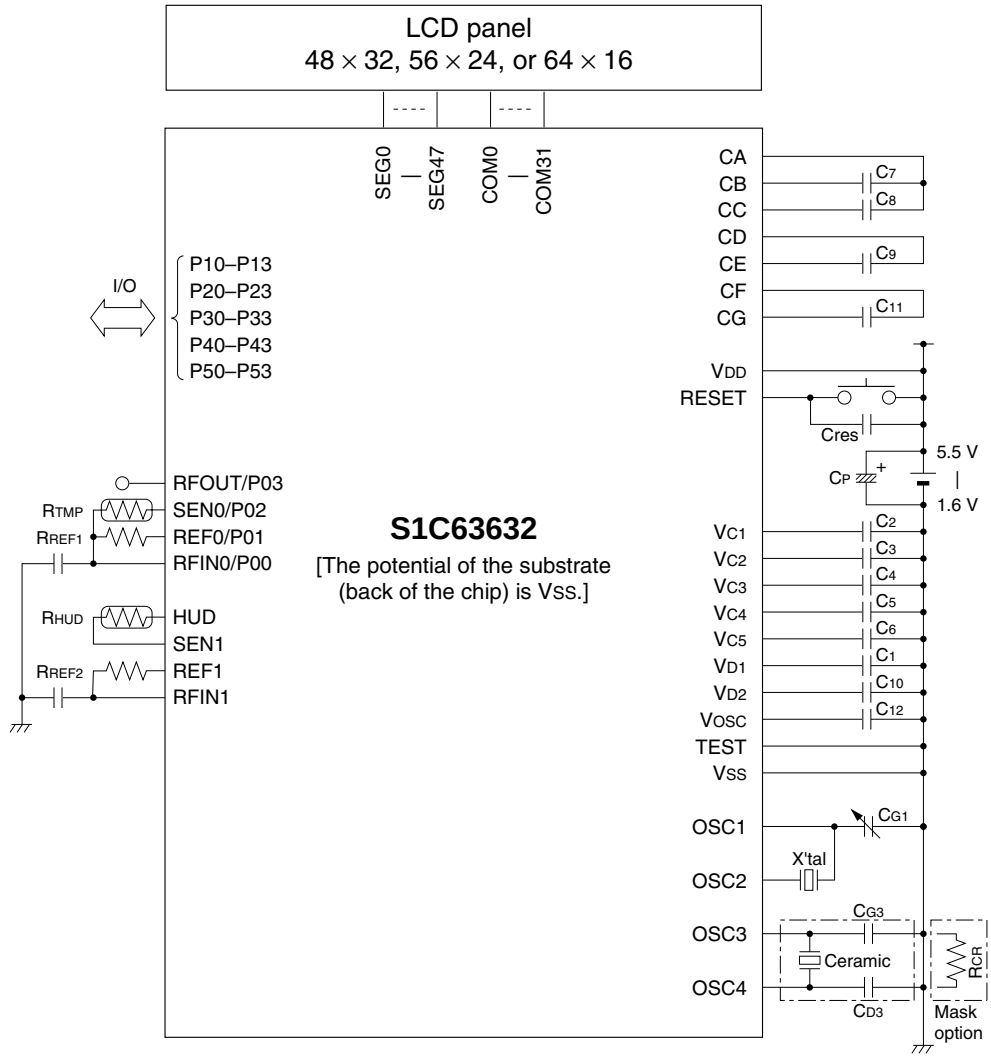
  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) Shield not only the face of the IC but the back and side as well.

  (4) After the shielded package has been opened, the IC chip should be bonded on the board within one week. If the IC chip must be stored after the package has been opened, be sure to shield the IC from visible radiation.

  (5) If there is a possibility that heat stress exceeding the reflow soldering condition is applied to the IC in the bonding process, perform enough evaluation of data stored in the nonvolatile memory before the product is shipped.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz
C_{G1}	Trimmer capacitor	0–25 pF
Ceramic	Ceramic oscillator	0.3–4.2 MHz
C_{G3}	Gate capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)
C_{D3}	Drain capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)
R_{CR}	Resistor for CR oscillation	30 kΩ
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF

Symbol	Name	Recommended value
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7~C_9	Booster capacitors	0.1 µF
C_{10}	Capacitor between V_{SS} and V_{D2}	0.1 µF
C_{11}	Booster capacitor	0.1 µF
C_{12}	Capacitor between V_{SS} and V_{OSC}	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for RESET terminal	0.47 µF

Note: C_4, C_{10} and C_{11} are not necessary depending on the selected option for the LCD drive power. Refer to Section 4.6.1, "Configuration of LCD driver", for details.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{SS}=0V)

Item	Symbol	Condition	Rated value	Unit
Power supply voltage	V_{DD}		-0.3 to +6.0	V
LCD power supply voltage	V_{C5}		-0.3 to +6.0	V
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V
High level output current	I_{OH}	1 terminal	-5	mA
		Total of all terminals	-20	mA
Low level output current	I_{OL}	1 terminal	5	mA
		Total of all terminals	20	mA
Permissible dissipation ∗1	P_D		200	mW
Operating temperature	Ta		-45 to +85	°C
Storage temperature	Tstg		-65 to +150	°C
Soldering temperature / time	Tsol		260°C, 10sec (lead section)	–

∗1 In case of plastic package (QFP20-144pin).

7.2 Recommended Operating Conditions

(Ta=-45 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	V_{SS}=0V	1.6	–	5.5	V
Operating frequency	f_{OSC1}	Crystal oscillation	–	32.768	–	kHz
	f_{OSC3}	CR oscillation (external R)	30	–	2,200	kHz
		Ceramic oscillation	30	–	4,200	kHz
Capacitor between V_{D1} and V_{SS}	C_1		–	0.1	–	µF
Capacitor between V_{C1} and V_{SS}	C_2	∗1	–	0.1	–	µF
Capacitor between V_{C2} and V_{SS}	C_3	∗1	–	0.1	–	µF
Capacitor between V_{C3} and V_{SS}	C_4	∗1, ∗2	–	0.1	–	µF
Capacitor between V_{C4} and V_{SS}	C_5	∗1	–	0.1	–	µF
Capacitor between V_{C5} and V_{SS}	C_6	∗1	–	0.1	–	µF
Capacitor between CA and CB	C_7	∗1	–	0.1	–	µF
Capacitor between CA and CC	C_8	∗1	–	0.1	–	µF
Capacitor between CD and CE	C_9	∗1	–	0.1	–	µF
Capacitor between V_{D2} and V_{SS}	C_{10}	∗1	–	0.1	–	µF
Capacitor between CF and CG	C_{11}	∗1	–	0.1	–	µF
Capacitor between V_{OSC} and V_{SS}	C_{12}		–	0.1	–	µF

∗1 When LCD drive power is not used, the capacitor is not necessary. In this case, leave the V_{C1} to V_{C5} and CA to CG terminals open.

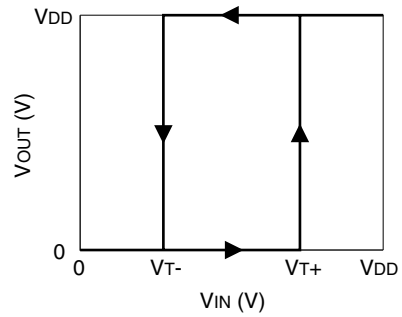
∗2 When 1/4 bias is selected, C_4 is not necessary. In this case, leave the V_{C3} terminal open.

7.3 DC Characteristics

Unless otherwise specified:
V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-45 to 85°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		Pxx	0.8V_{DD}	–	V_{DD}	V
Low level input voltage	V_{IL}		Pxx	0	–	0.2V_{DD}	V
High level Schmitt input voltage (1)	V_{T1+}		RESET	0.5V_{DD}	–	0.9V_{DD}	V
Low level Schmitt input voltage (1)	V_{T1-}		RESET	0.1V_{DD}	–	0.5V_{DD}	V
High level Schmitt input voltage (2)	V_{T2+}		Pxx ∗1	0.5V_{DD}	–	0.9V_{DD}	V
Low level Schmitt input voltage (2)	V_{T2-}		Pxx ∗1	0.1V_{DD}	–	0.5V_{DD}	V
High level output current	I_{OH}	V_{OH}=0.9V_{DD}	Pxx, REF1, SEN1, HUD	–	–	-0.5	mA
Low level output current	I_{OL}	V_{OL}=0.1V_{DD}	Pxx, REF1, SEN1, HUD	0.5	–	–	mA
Input leak current	I_{LI}		Pxx, RESET, RFIN1	-1	–	1	µA
Output leak current	I_{LO}		Pxx, REF1, SEN1, HUD	-1	–	1	µA
Input pull-down resistance	R_{IN}		Pxx, RESET	100	–	500	kΩ
Input terminal capacitance	C_{IN}	V_{IN}=0V, Ta=25°C	Pxx, RESET, RFIN1	–	–	15	pF
Segment/Common output current	I_{SEGH}	V_{SEGH}=V_{C5}-0.1V	SEGxx, COMxx	–	–	-5	µA
	I_{SEGL}	V_{SEGL}=V_{SS}+0.1V	SEGxx, COMxx	5	–	–	µA

∗1 When CMOS Schmitt level is selected. (P00–P13)



7.4 Analog Circuit Characteristics and Current Consumption

LCD drive voltage (1/5 bias, V_{C2} reference)

Unless otherwise specified:
V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=25°C, C_2–C_{11}=0.1µF, When a checker pattern is displayed, No panel load
A 1 MΩ load resistor is connected between V_{SS}–V_{C1}, V_{SS}–V_{C2}, V_{SS}–V_{C3}, V_{SS}–V_{C4}, and V_{SS}–V_{C5}.
The voltage booster is used when V_{DD}=1.6–2.5V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}		0.192V_{C5}	–	0.217V_{C5}	V
	V_{C2}		0.376V_{C5}	–	0.424V_{C5}	V
	V_{C3}		0.573V_{C5}	–	0.646V_{C5}	V
	V_{C4}		0.752V_{C5}	–	0.848V_{C5}	V
	V_{C5}	LC0–3="0H"		4.20		V
		LC0–3="1H"		4.30		
		LC0–3="2H"		4.40		
		LC0–3="3H"		4.50		
		LC0–3="4H"		4.60		
		LC0–3="5H"		4.70		
		LC0–3="6H"		4.80		
		LC0–3="7H"	Typ.	4.90	Typ.	
		LC0–3="8H"	× 0.94	5.00	× 1.06	
		LC0–3="9H"		5.10		
		LC0–3="AH"		5.20		
		LC0–3="BH"		5.30		
		LC0–3="CH"		5.40		
		LC0–3="DH"		5.50		
		LC0–3="EH"		5.60		
		LC0–3="FH"		5.70		

LCD drive voltage (1/4 bias, V_{C2} reference)

Unless otherwise specified:
V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=25°C, C_2–C_{11}=0.1µF, When a checker pattern is displayed, No panel load
A 1 MΩ load resistor is connected between V_{SS}–V_{C1}, V_{SS}–V_{C2}, V_{SS}–V_{C4}, and V_{SS}–V_{C5}.
The voltage booster is used when V_{DD}=1.6–2.5V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}		0.235V_{C5}	–	0.265V_{C5}	V
	V_{C2}		0.472V_{C5}	–	0.532V_{C5}	V
	V_{C4}		0.705V_{C5}	–	0.795V_{C5}	V
	V_{C5}	LC0–3="0H"		3.60		V
		LC0–3="1H"		3.68		
		LC0–3="2H"		3.76		
		LC0–3="3H"		3.84		
		LC0–3="4H"		3.92		
		LC0–3="5H"		4.00		
		LC0–3="6H"		4.08		
		LC0–3="7H"	Typ.	4.16	Typ.	
		LC0–3="8H"	× 0.94	4.24	× 1.06	
		LC0–3="9H"		4.32		
		LC0–3="AH"		4.40		
		LC0–3="BH"		4.48		
		LC0–3="CH"		4.56		
		LC0–3="DH"		4.64		
		LC0–3="EH"		4.72		
		LC0–3="FH"		4.80		

LCD drive voltage (1/4 bias, V_{C1} reference)

Unless otherwise specified:
V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=25°C, C_2–C_{11}=0.1µF, When a checker pattern is displayed, No panel load
A 1 MΩ load resistor is connected between V_{SS}–V_{C1}, V_{SS}–V_{C2}, V_{SS}–V_{C4}, and V_{SS}–V_{C5}.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}		0.244V_{C5}	–	0.276V_{C5}	V
	V_{C2}		0.476V_{C5}	–	0.536V_{C5}	V
	V_{C4}		0.720V_{C5}	–	0.812V_{C5}	V
	V_{C5}	LC0–3="0H"		3.60		V
		LC0–3="1H"		3.68		
		LC0–3="2H"		3.76		
		LC0–3="3H"		3.84		
		LC0–3="4H"		3.92		
		LC0–3="5H"		4.00		
		LC0–3="6H"		4.08		
		LC0–3="7H"	Typ.	4.16	Typ.	
		LC0–3="8H"	× 0.94	4.24	× 1.06	
		LC0–3="9H"		4.32		
		LC0–3="AH"		4.40		
		LC0–3="BH"		4.48		
		LC0–3="CH"		4.56		
		LC0–3="DH"		4.64		
		LC0–3="EH"		4.72		
		LC0–3="FH"		4.80		

SVD circuit

Unless otherwise specified:
V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD}	SVDS0–3="0H"		1.6		V
		SVDS0–3="1H"		1.8		
		SVDS0–3="2H"		1.9		
		SVDS0–3="3H"		2.0		
		SVDS0–3="4H"		2.1		
		SVDS0–3="5H"		2.2		
		SVDS0–3="6H"		2.3		
		SVDS0–3="7H"	Typ.	2.4	Typ.	
		SVDS0–3="8H"	× 0.97	2.5	× 1.03	
		SVDS0–3="9H"		2.6		
		SVDS0–3="AH"		2.7		
		SVDS0–3="BH"		2.8		
		SVDS0–3="CH"		2.9		
		SVDS0–3="DH"		3.0		
		SVDS0–3="EH"		3.1		
		SVDS0–3="FH"		3.2		
SVD circuit response time	t_{SVD}		–	–	500	µs

R/F converter circuit

Unless otherwise specified:
V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reference/sensor oscillation frequencies *1	f_{RFCLK}	Ta=-40 to 85°C	1	–	2000	kHz
Reference/sensor oscillation frequency/IC deviation *2	$\Delta f_{RFCLK}/\Delta IC$		-40	–	40	%
Reference/sensor resistance *3	R_{REF}/R_{SEN}		10	–	–	kΩ
Reference capacitor and capacitive sensor capacitance *3	C_{RFC}/C_{SEN}		100	–	2000	pF
Time base counter clock frequency	f_{TCCLK}		–	–	4200	kHz

*1 The oscillation frequency/IC deviation characteristic value may increase due to variations in oscillation frequency caused by leakage current if the oscillation frequency is 1 kHz or lower.

*2 In these characteristics, unevenness between production lots, and variations in board, resistances and capacitances used in the measurement environment are taken into account (variations in temperature are not included).

*3 The CR oscillation can be performed if the resistance or capacitance is out of the range shown in the table (see characteristic curves), note, however, that the oscillation frequency/IC deviation characteristic value may increase due to parasitic elements on the board and those in the IC.

Current consumption

Unless otherwise specified:

V_{DD}=1.6 to 5.5V, V_{SS}=0V, DBON=HLON=0(V_{D2}=OFF), FLCKSx=0H(32Hz), Ta=25°C, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in SLEEP	I_{SLP}	When SLP is executed: OSC1=ON, OSC3=OFF	–	0.08	0.50	µA
Current consumption in HALT mode	I_{HALT1}	OSC1=32kHz Crystal, OSC3=OFF	–	0.60	2.00	µA
	I_{HALT2}	OSC1=32kHz Crystal, OSC3=4MHz Ceramic	–	70	150	µA
	I_{HALT3}	OSC1=32kHz Crystal, OSC3=2MHz CR	–	120	240	µA
Current consumption during execution	I_{EXE1}	OSC1=32kHz Crystal, OSC3=OFF, CPUclk=OSC1	–	2.5	4.0	µA
	I_{EXE2}	OSC1=32kHz Crystal, OSC3=4MHz Ceramic, CPUclk=OSC3	–	320	600	µA
	I_{EXE3}	OSC1=32kHz Crystal, OSC3=2MHz CR, CPUclk=OSC3	–	250	500	µA
Current consumption during execution in heavy load protection mode	I_{EXE1H}	OSC1=32kHz Crystal, OSC3=OFF, CPUclk=OSC1, HLMOD=1	–	13	30	µA
LCD circuit current (1/5 bias, V_{C2} reference)	I_{LCD11}	LCDCx=All on, LCx=FH, f_{OSC1}=32.768kHz, V_{DD}=2.5 to 5.5V *1	–	1.8	3.0	µA
LCD circuit current in heavy load protection mode (1/5 bias, V_{C2} reference)	I_{LCD11H}	LCDCx=All on, LCx=FH, f_{OSC1}=32.768kHz, V_{DD}=2.5 to 5.5V, HLMOD=1 *2	–	14	20	µA
LCD circuit current when the power voltage booster is active (1/5 bias, V_{C2} reference)	I_{LCD12}	LCDCx=All on, LCx=FH, f_{OSC1}=32.768kHz, DBON=1, V_{DD}=1.6 to 2.5V *3	–	3.5	6.0	µA
LCD circuit current in heavy load protection mode when the power voltage booster is active (1/5 bias, V_{C2} reference)	I_{LCD12H}	LCDCx=All on, LCx=FH, f_{OSC1}=32.768kHz, DBON=1, V_{DD}=1.6 to 2.5V, HLMOD=1 *4	–	26	50	µA
LCD circuit current (1/4 bias, V_{C2} reference)	I_{LCD21}	LCDCx=All on, LCx=FH, f_{OSC1}=32.768kHz, V_{DD}=2.5 to 5.5V *1	–	0.9	1.5	µA
LCD circuit current in heavy load protection mode (1/4 bias, V_{C2} reference)	I_{LCD21H}	LCDCx=All on, LCx=FH, f_{OSC1}=32.768kHz, V_{DD}=2.5 to 5.5V, HLMOD=1 *2	–	9	18	µA
LCD circuit current when the power voltage booster is active (1/4 bias, V_{C2} reference)	I_{LCD22}	LCDCx=All on, LCx=FH, f_{OSC1}=32.768kHz, DBON=1, V_{DD}=1.6 to 2.5V *3	–	1.7	3.0	µA
LCD circuit current in heavy load protection mode when the power voltage booster is active (1/4 bias, V_{C2} reference)	I_{LCD22H}	LCDCx=All on, LCx=FH, f_{OSC1}=32.768kHz, DBON=1, V_{DD}=1.6 to 2.5V, HLMOD=1 *4	–	18	36	µA
LCD circuit current (1/4 bias, V_{C1} reference)	I_{LCD31}	LCDCx=All on, LCx=FH, f_{OSC1}=32.768kHz, V_{DD}=1.6 to 5.5V *1	–	1.2	2.5	µA
LCD circuit current in heavy load protection mode (1/4 bias, V_{C1} reference)	I_{LCD31H}	LCDCx=All on, LCx=FH, f_{OSC1}=32.768kHz, V_{DD}=1.6 to 5.5V, HLMOD=1 *2	–	5.5	11.0	µA
SVD circuit current	I_{SVD}	V_{DD}=3.6V *5	–	9	15	µA
R/f converter circuit current	I_{RF}	V_{DD}=5.5V, C_{REF}=C_{SEN}=1000pF, R_{REF}=R_{SEN}=10kΩ *6	–	300	400	µA

*1 This value is added to the current consumption in HALT mode or current consumption during execution when the LCD circuit is active. Current consumption increases according to the display contents and panel load.

*2 This value is added to the current consumption during execution in heavy load protection mode when the LCD circuit is active. Current consumption increases according to the display contents and panel load.

*3 This value is added to the current consumption in HALT mode or current consumption during execution when the power voltage booster/halver and the LCD circuit are active. Current consumption increases according to the display contents and panel load.

*4 This value is added to the current consumption during execution in heavy load protection mode when the power voltage booster/halver and the LCD circuit are active. Current consumption increases according to the display contents and panel load.

*5 This value is added to the current consumption during execution or current consumption during execution in heavy load protection mode when the SVD circuit is active.

*6 This value is added to the current consumption during execution when the R/f converter circuit is active.

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:

V_{DD}=1.6 to 5.5V, V_{SS}=0V, Crystal oscillator=C-002RX(R_1=30kΩ(Typ.), C_L=12.5pF), Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta		–	–	3	s
External gate capacitance	C_{G1}	Including the board capacitance	0	–	25	pF
Built-in drain capacitance	C_{D1}	Chip	–	14	–	pF
Frequency/IC deviation	Δf/ΔIC	V_{DD}=constant	-10	–	10	ppm
Frequency/voltage deviation	Δf/ΔV		–	–	1	ppm/V
Frequency adjustment range	Δf/ΔC_G	V_{DD}=constant, C_G=0 to 25pF	25	–	–	ppm

OSC3 ceramic oscillation circuit

Unless otherwise specified:

V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta		–	–	1	ms

OSC3 CR oscillation circuit (external R type)

Unless otherwise specified:

V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta		–	–	1	ms
Frequency/IC deviation	Δf/ΔIC	R_{CR}=constant	-25	–	25	ppm

7.6 Serial Interface AC Characteristics

Master mode

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-45 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd	–	–	200	ns
Receiving data input set-up time	tsms	400	–	–	ns
Receiving data input hold time	tsmh	200	–	–	ns

Note that the maximum clock frequency is limited to 1 MHz.

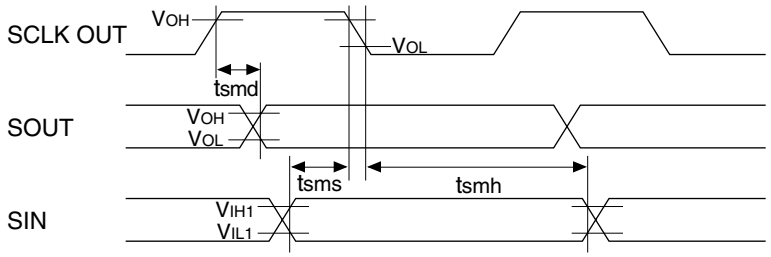
Slave mode

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-45 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

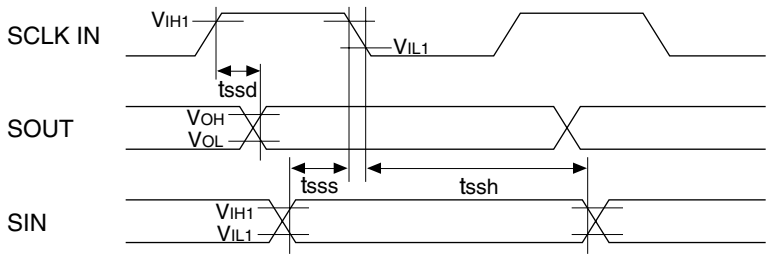
Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd	–	–	500	ns
Receiving data input set-up time	tsss	400	–	–	ns
Receiving data input hold time	tssh	200	–	–	ns

Note that the maximum clock frequency is limited to 1 MHz.

<Master mode>

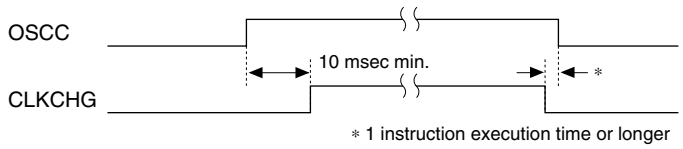


<Slave mode>



7.7 Timing Chart

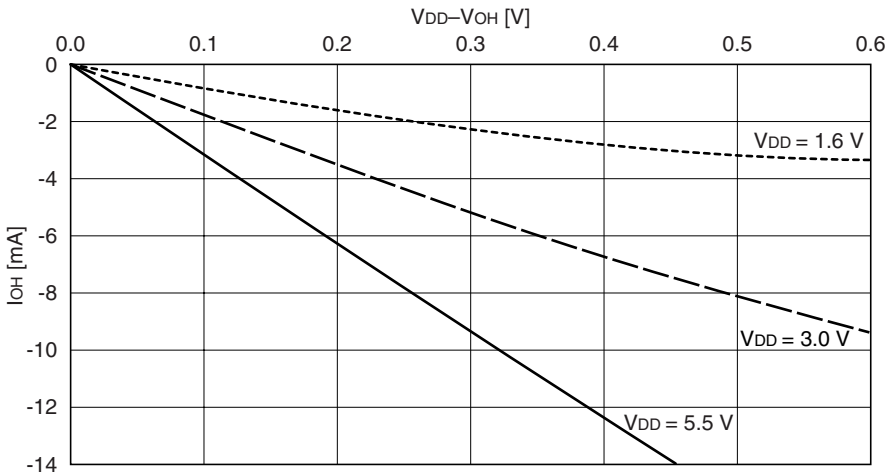
System clock switching



7.8 Characteristics Curves (reference value)

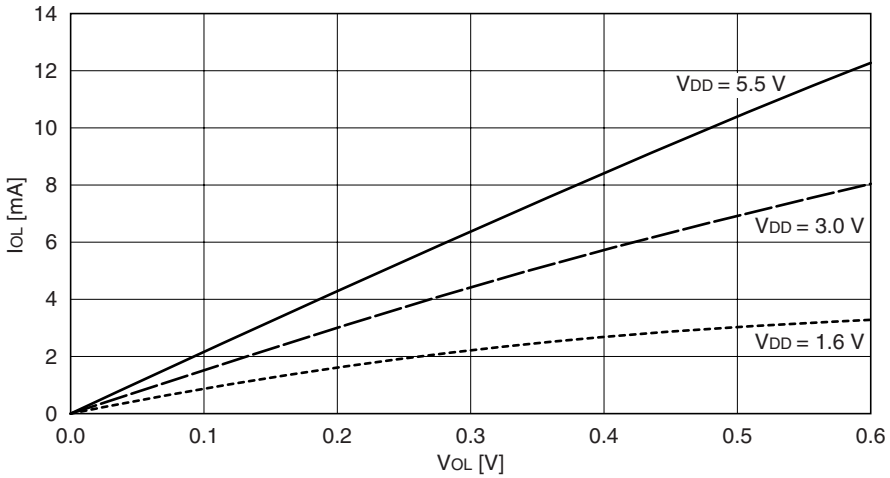
High level output current-voltage characteristic

Ta = 85°C, Max. value



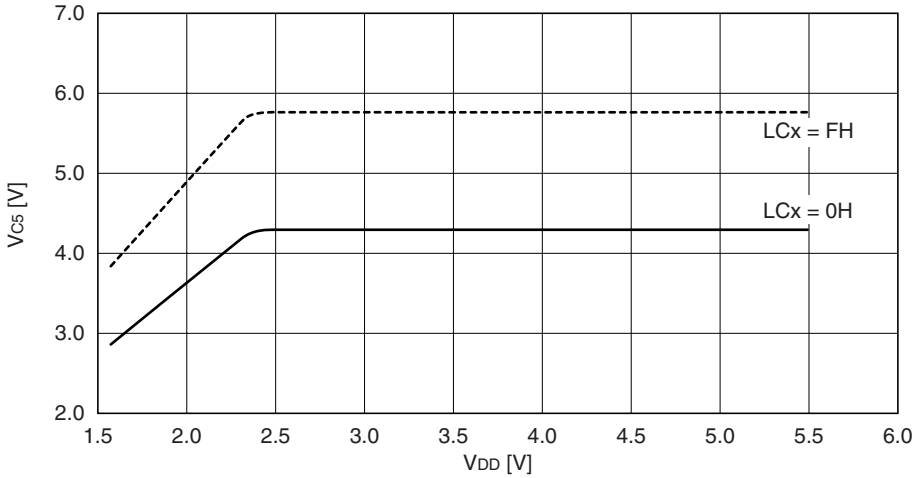
Low level output current-voltage characteristic

Ta = 85°C, Min. value



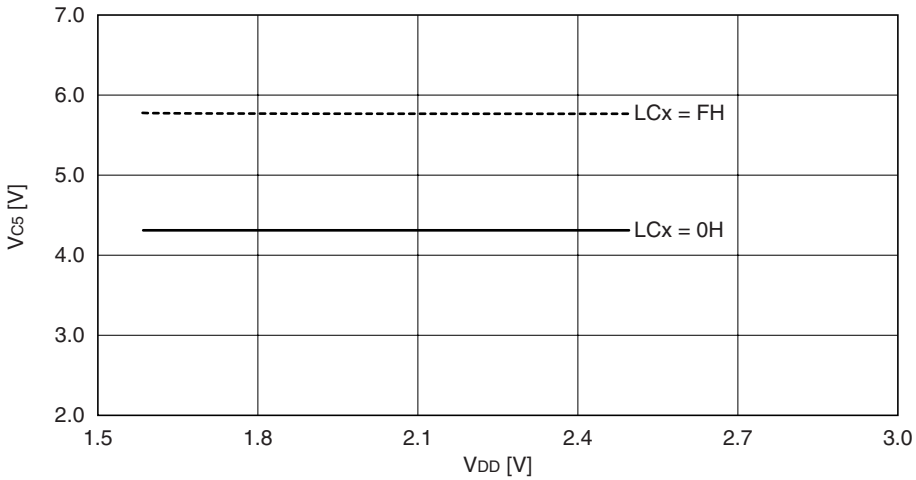
LCD drive voltage - supply voltage characteristic (1/5 bias, V_{C2} reference, power supply voltage booster/halver not used)

Ta = 25°C, Typ. value



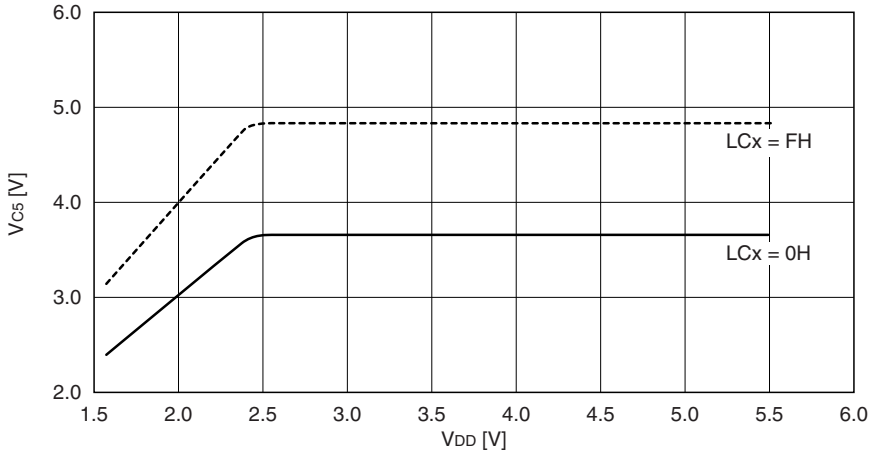
LCD drive voltage - supply voltage characteristic (1/5 bias, V_{C2} reference, power supply voltage booster/halver used)

Ta = 25°C, Typ. value



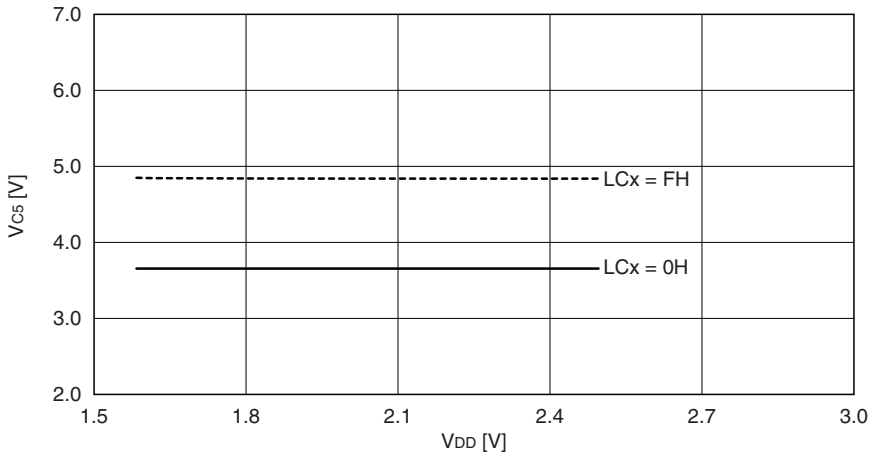
LCD drive voltage - supply voltage characteristic (1/4 bias, V_{C2} reference, power supply voltage booster/halver not used)

Ta = 25°C, Typ. value



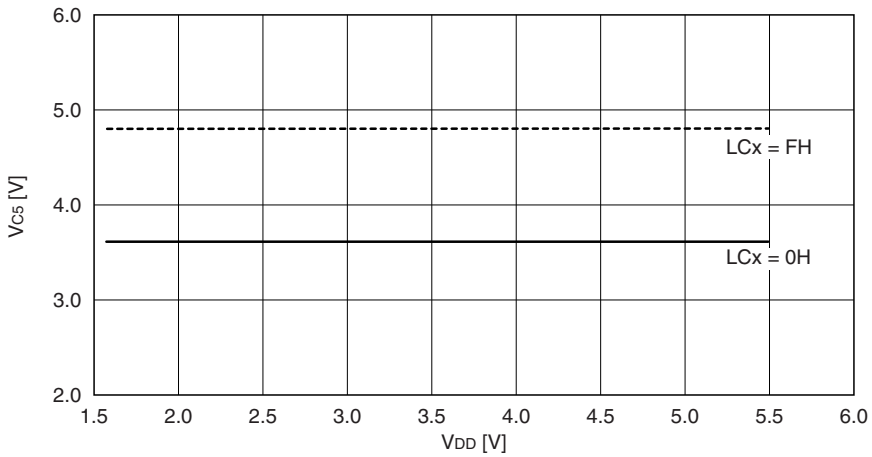
LCD drive voltage - supply voltage characteristic (1/4 bias, V_{C2} reference, power supply voltage booster/halver used)

Ta = 25°C, Typ. value



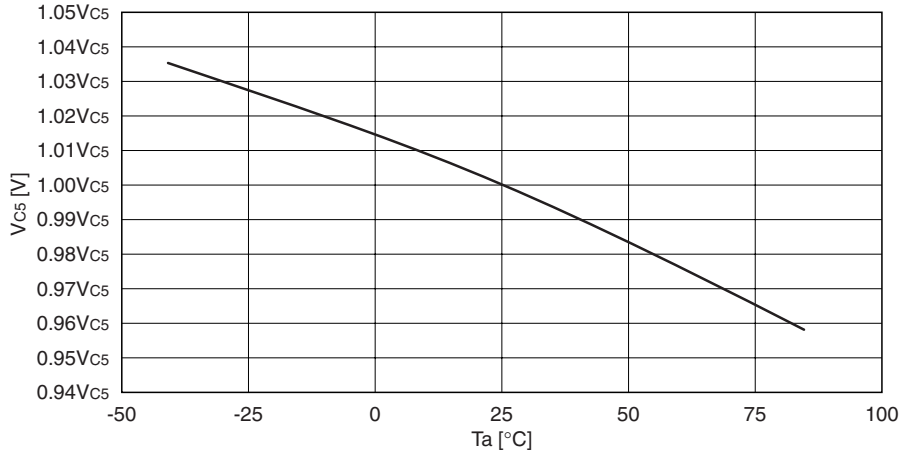
LCD drive voltage - supply voltage characteristic (1/4 bias, V_{C1} reference, power supply voltage booster/halver not used)

Ta = 25°C, Typ. value



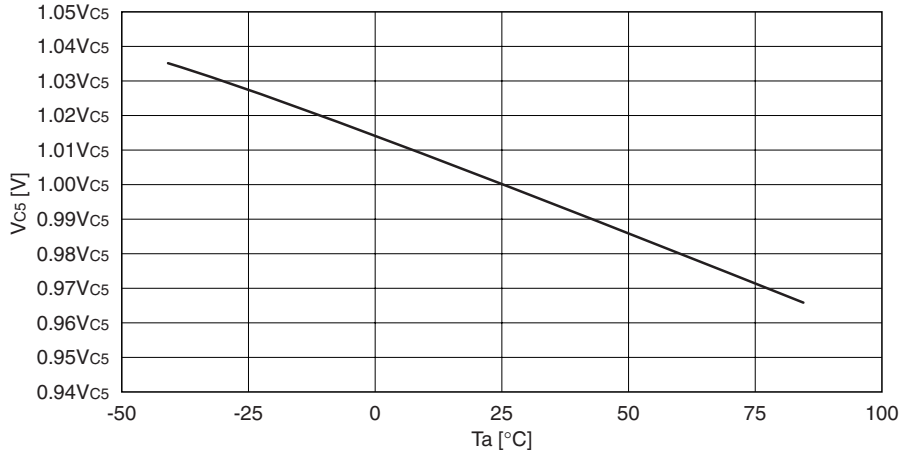
LCD drive voltage - ambient temperature characteristic (1/5 bias, V_{C2} reference, power supply voltage booster/halver not used)

V_{DD} = 3.0 V, Typ. value



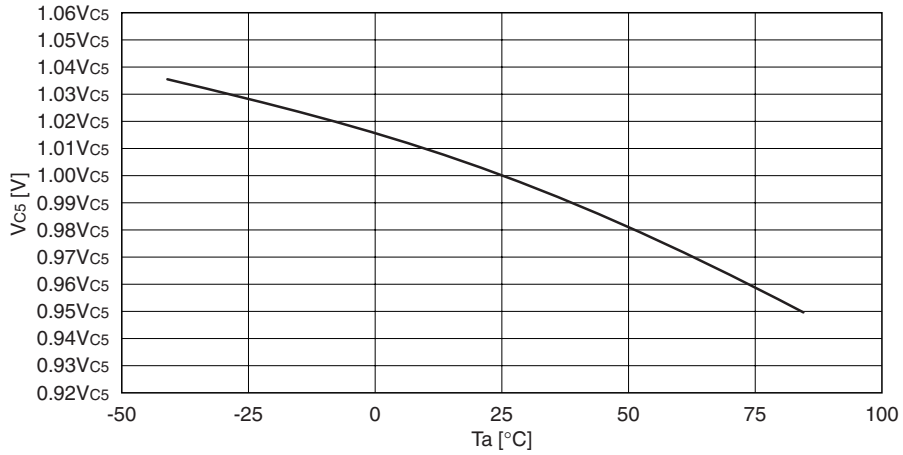
LCD drive voltage - ambient temperature characteristic (1/4 bias, V_{C2} reference, power supply voltage booster/halver not used)

V_{DD} = 3.0 V, Typ. value



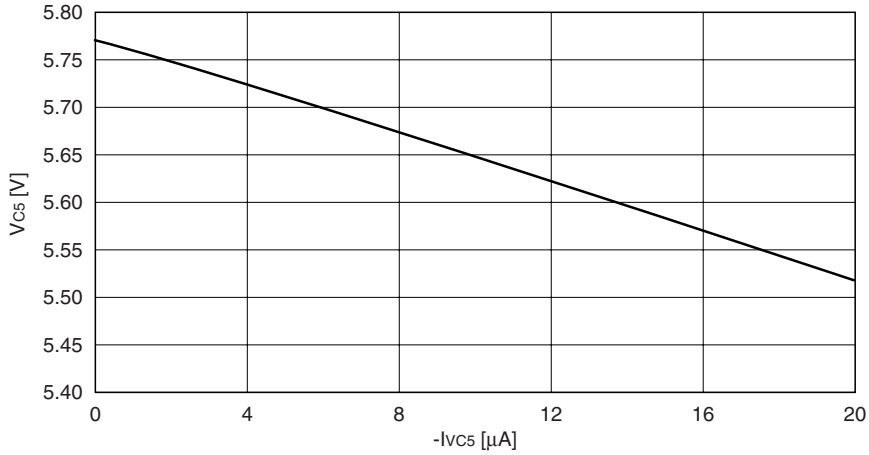
LCD drive voltage - ambient temperature characteristic (1/4 bias, V_{C1} reference, power supply voltage booster/halver not used)

V_{DD} = 3.0 V, Typ. value



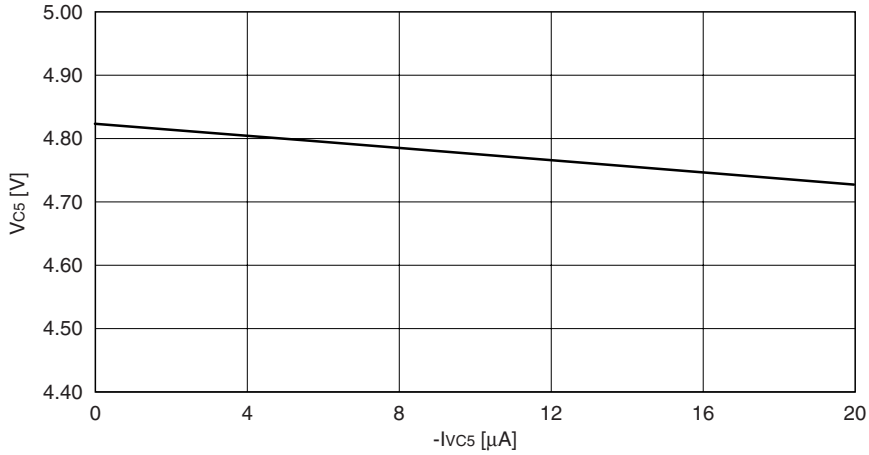
LCD drive voltage - load characteristic
(1/5 bias, V_{C2} reference, power supply voltage booster/halver not used)

When a load is connected to V_{C5} terminal only — LCx = FH, Ta = 25°C, Typ. value



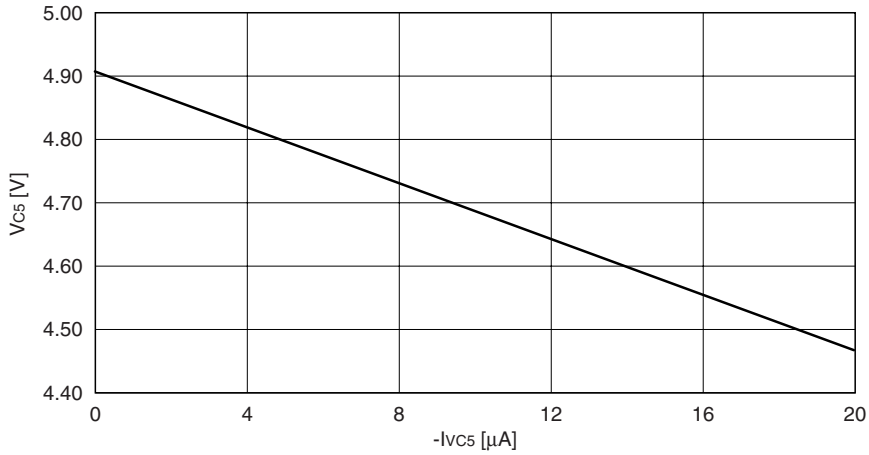
LCD drive voltage - load characteristic
(1/4 bias, V_{C2} reference, power supply voltage booster/halver not used)

When a load is connected to V_{C5} terminal only — LCx = FH, Ta = 25°C, Typ. value



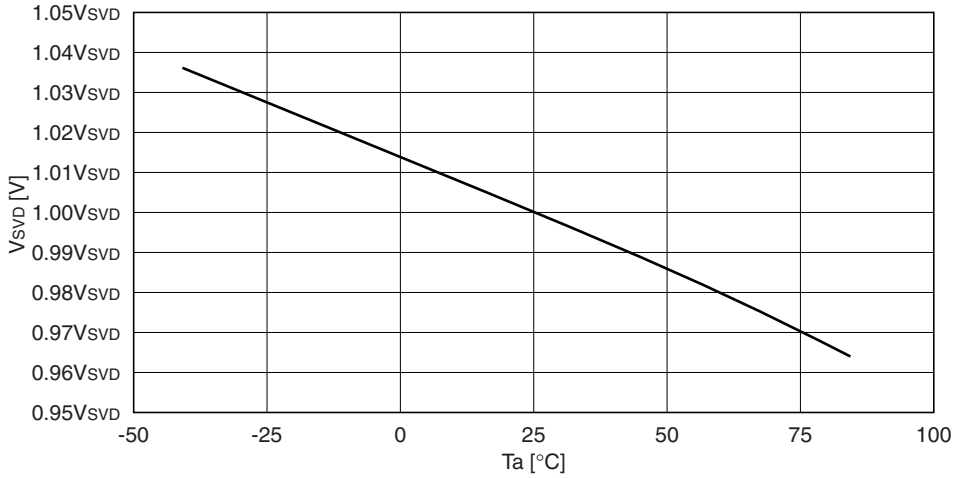
LCD drive voltage - load characteristic
(1/4 bias, V_{C1} reference, power supply voltage booster/halver not used)

When a load is connected to V_{C5} terminal only — LCx = FH, Ta = 25°C, Typ. value



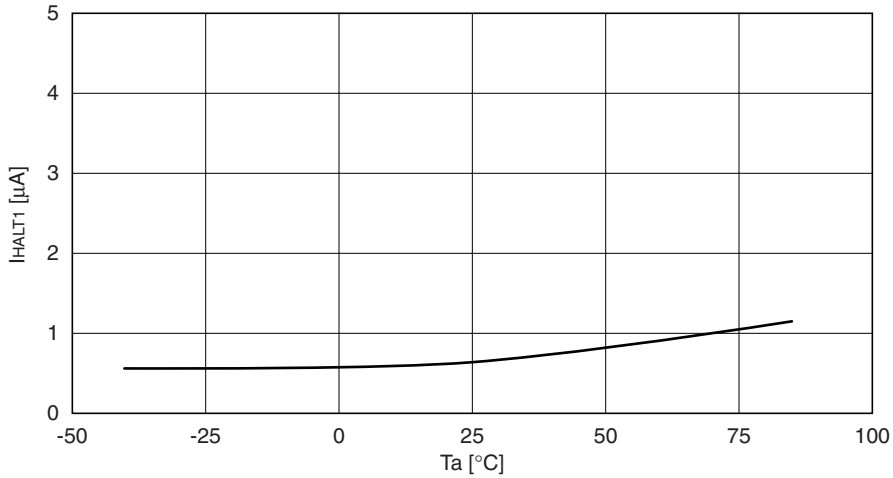
SVD voltage - ambient temperature characteristic

SVDSx = FH, Typ. value



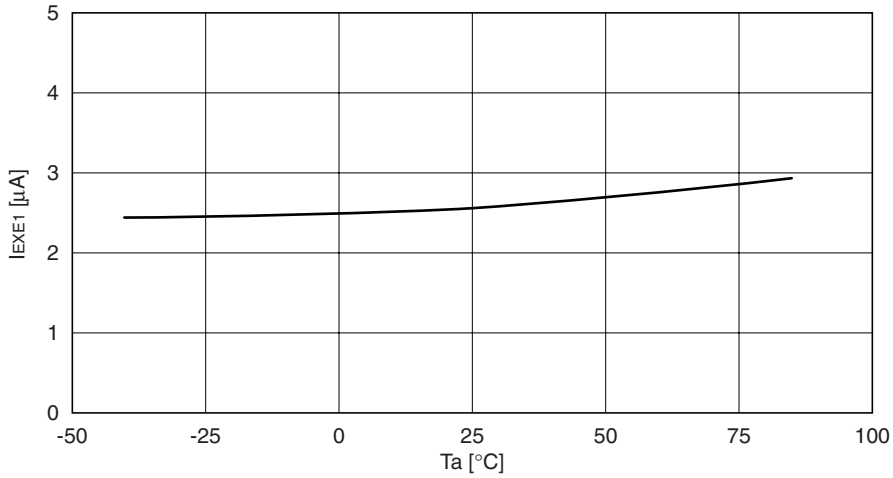
HALT state current consumption - temperature characteristic (During operation with OSC1) <Crystal oscillation, fOSC1 = 32.768 kHz>

VDD = 5.5 V, OSC3 = OFF, Clock manager = OFF, Typ. value



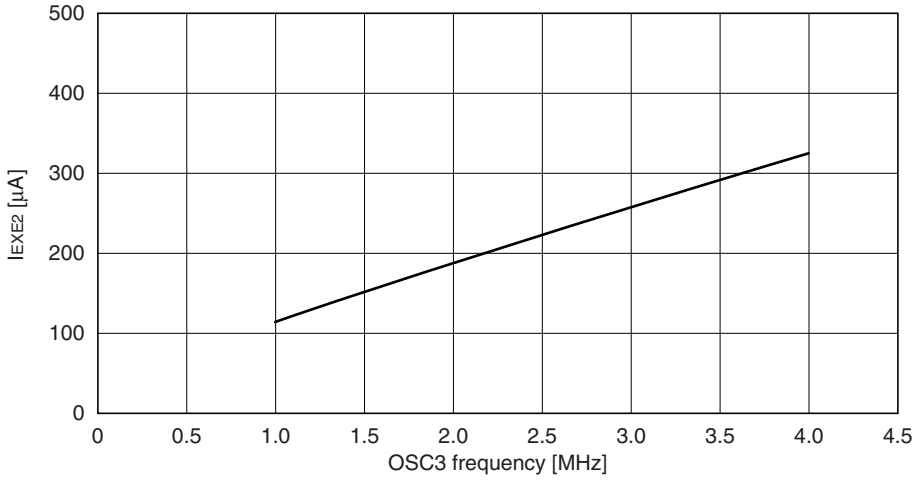
RUN state current consumption - temperature characteristic (During operation with OSC1) <Crystal oscillation, fOSC1 = 32.768 kHz>

VDD = 5.5 V, OSC3 = OFF, Clock manager = OFF, Typ. value



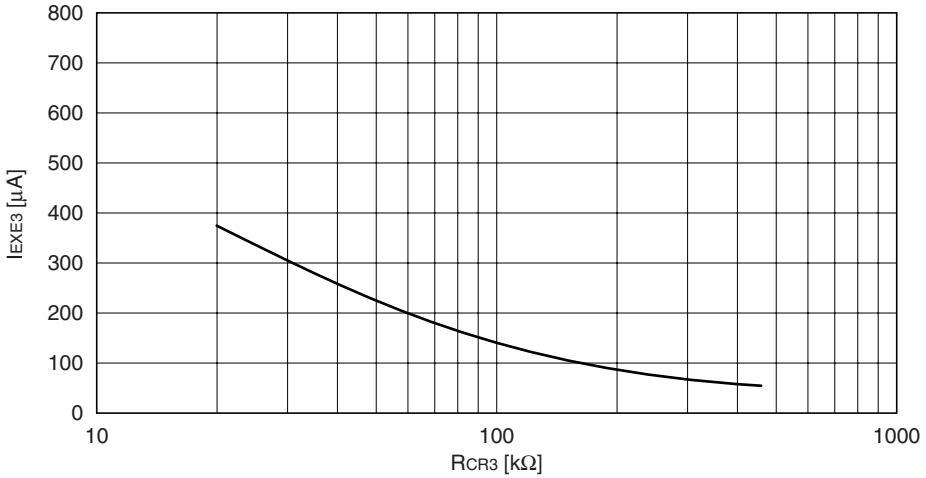
RUN state current consumption - frequency characteristic (During operation with OSC3) <Ceramic oscillation>

V_{DD} = 5.5 V, Ta = 25°C, Typ. value



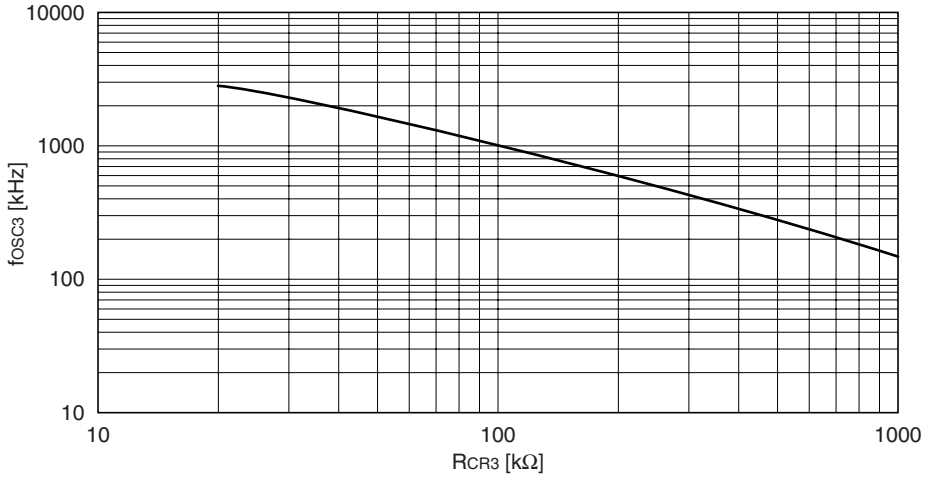
RUN state current consumption - resistor characteristic (During operation with OSC3) <CR oscillation>

V_{DD} = 5.5 V, Ta = 25°C, Typ. value



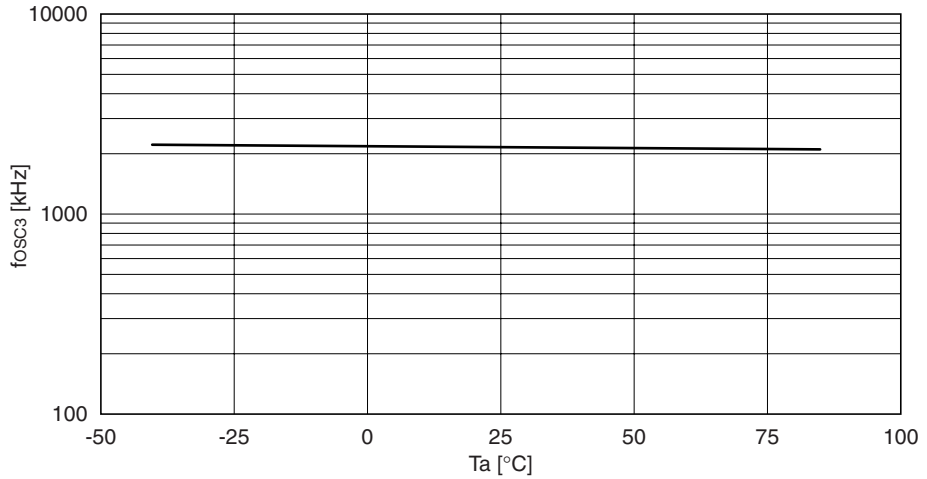
Oscillation frequency - resistor characteristic (OSC3) <CR oscillation>

V_{DD} = 5.5 V, Ta = 25°C, Typ. value



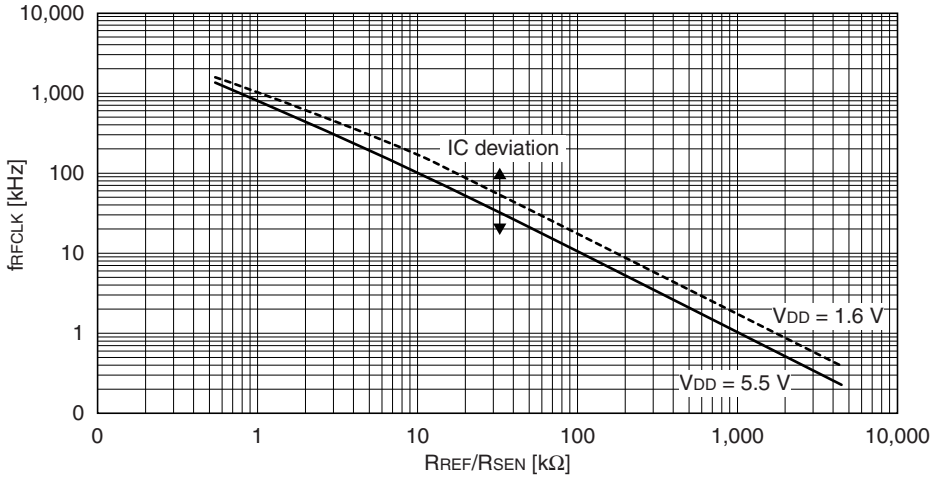
Oscillation frequency - temperature characteristic (OSC3) <CR oscillation>

R_{CR3} = 30 kΩ, Typ. value



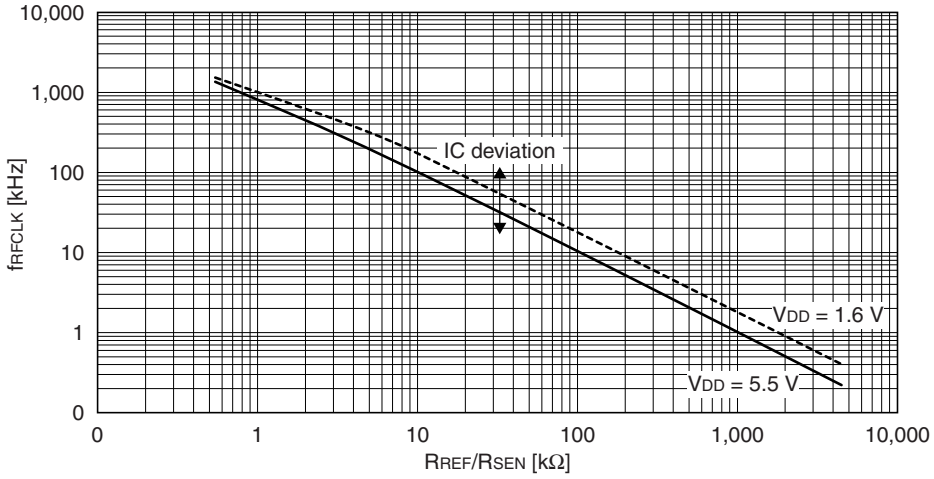
RFC reference/sensor oscillation frequency - resistance characteristic (DC oscillation mode)

C_{SEN} = 1000 pF, Ta = 25°C, Typ. value



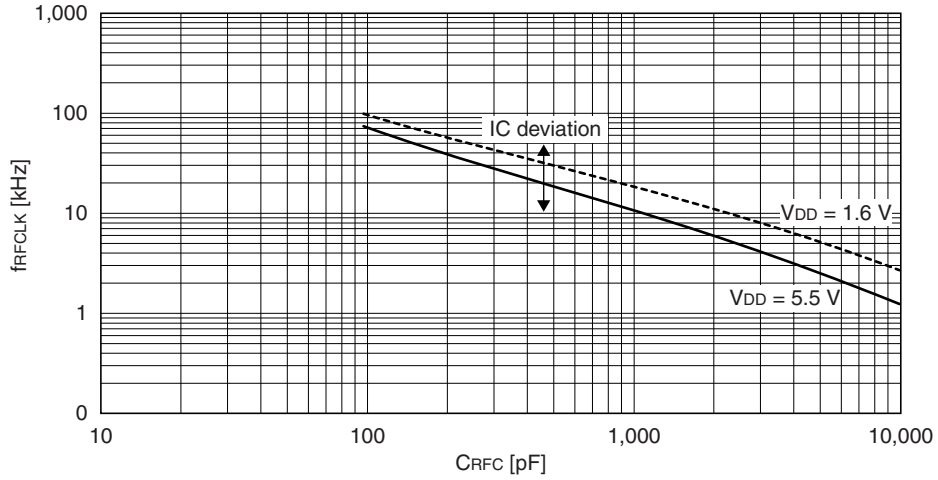
RFC reference/sensor oscillation frequency - resistance characteristic (AC oscillation mode)

C_{SEN} = 1000 pF, Ta = 25°C, Typ. value



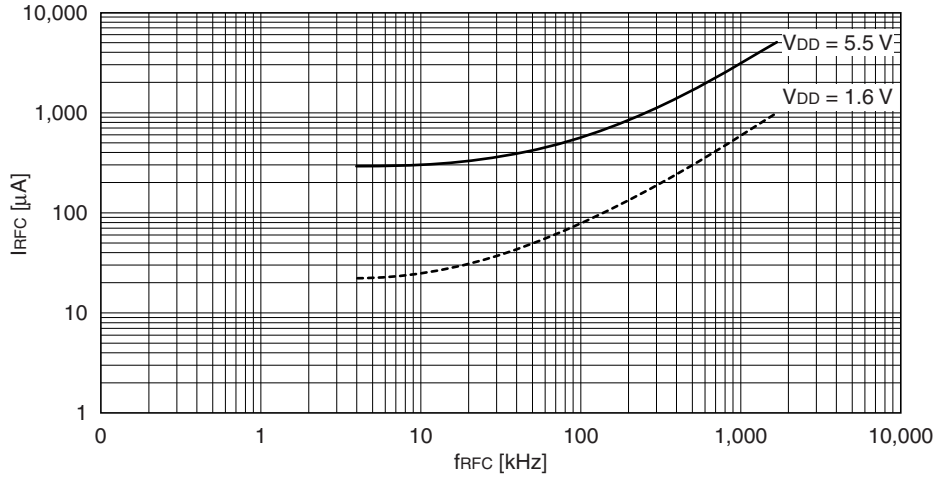
RFC reference/sensor oscillation frequency - capacitance characteristic (DC/AC oscillation mode)

R_{SEN} = 100 kΩ, Ta = 25°C, Typ. value



RFC reference/sensor oscillation frequency - current consumption characteristic (DC/AC oscillation mode)

C_{RFC} = 1000 pF, Ta = 25°C, Typ. value

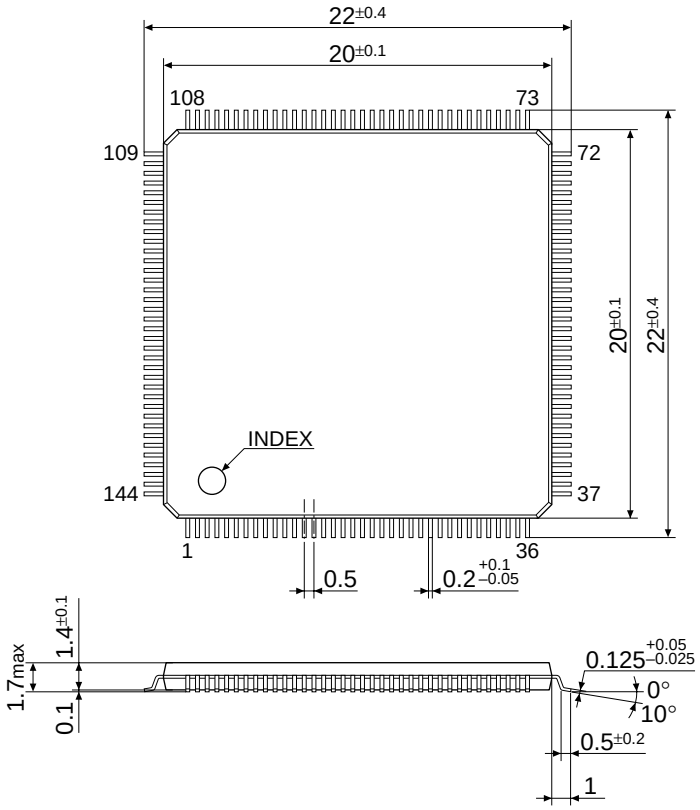


CHAPTER 8 PACKAGE

8.1 Plastic Package

QFP20-144pin

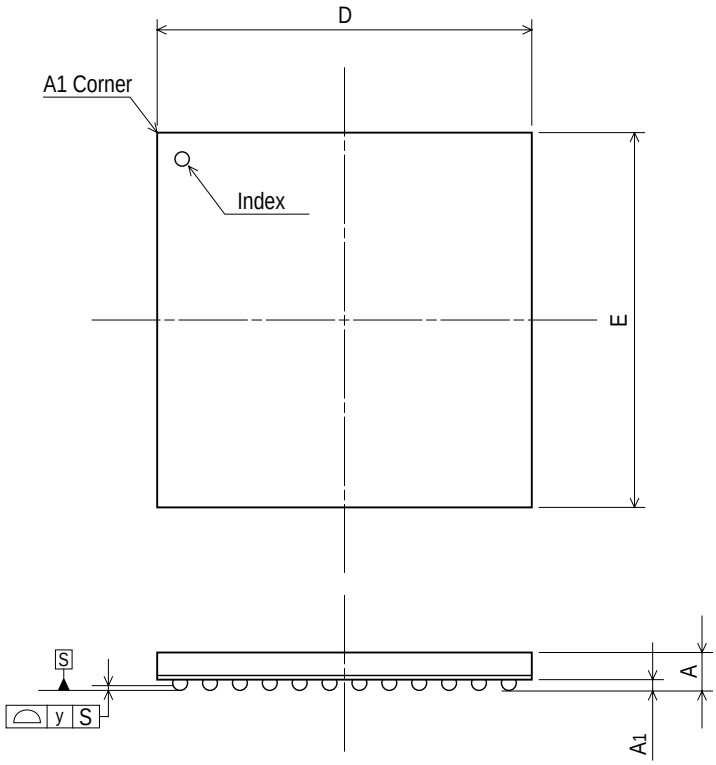
(Unit: mm)



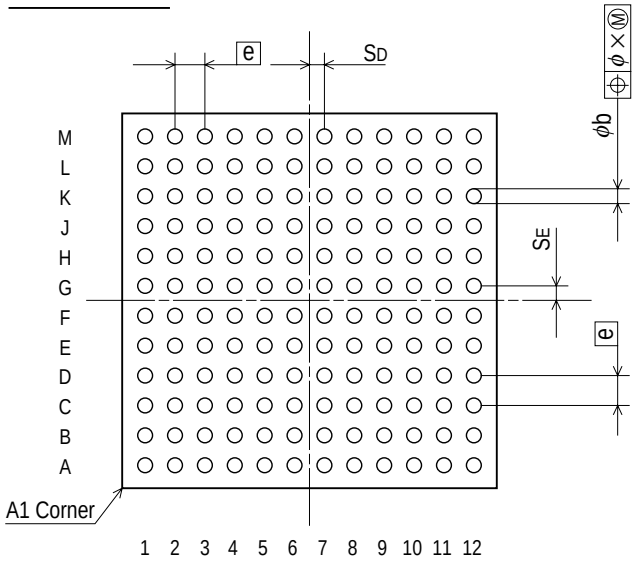
The dimensions are subject to change without notice.

VFBGA10H-144

Top View



Bottom View

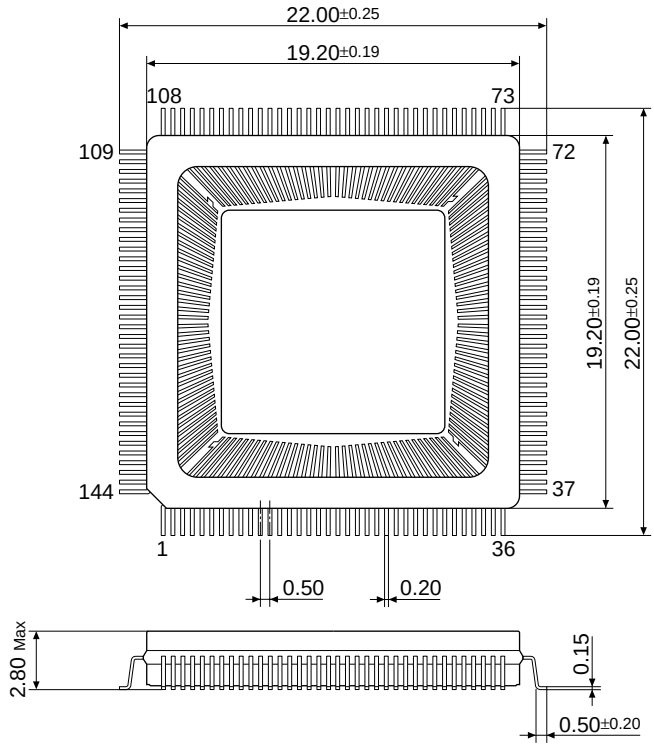


Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	–	10	–
E	–	10	–
A	–	–	1.2
A_1	–	0.3	–
e	–	0.8	–
b	0.38	–	0.48
x	–	–	0.08
y	–	–	0.1
S_D	–	0.4	–
S_E	–	0.4	–

8.2 Ceramic Package for Test Samples

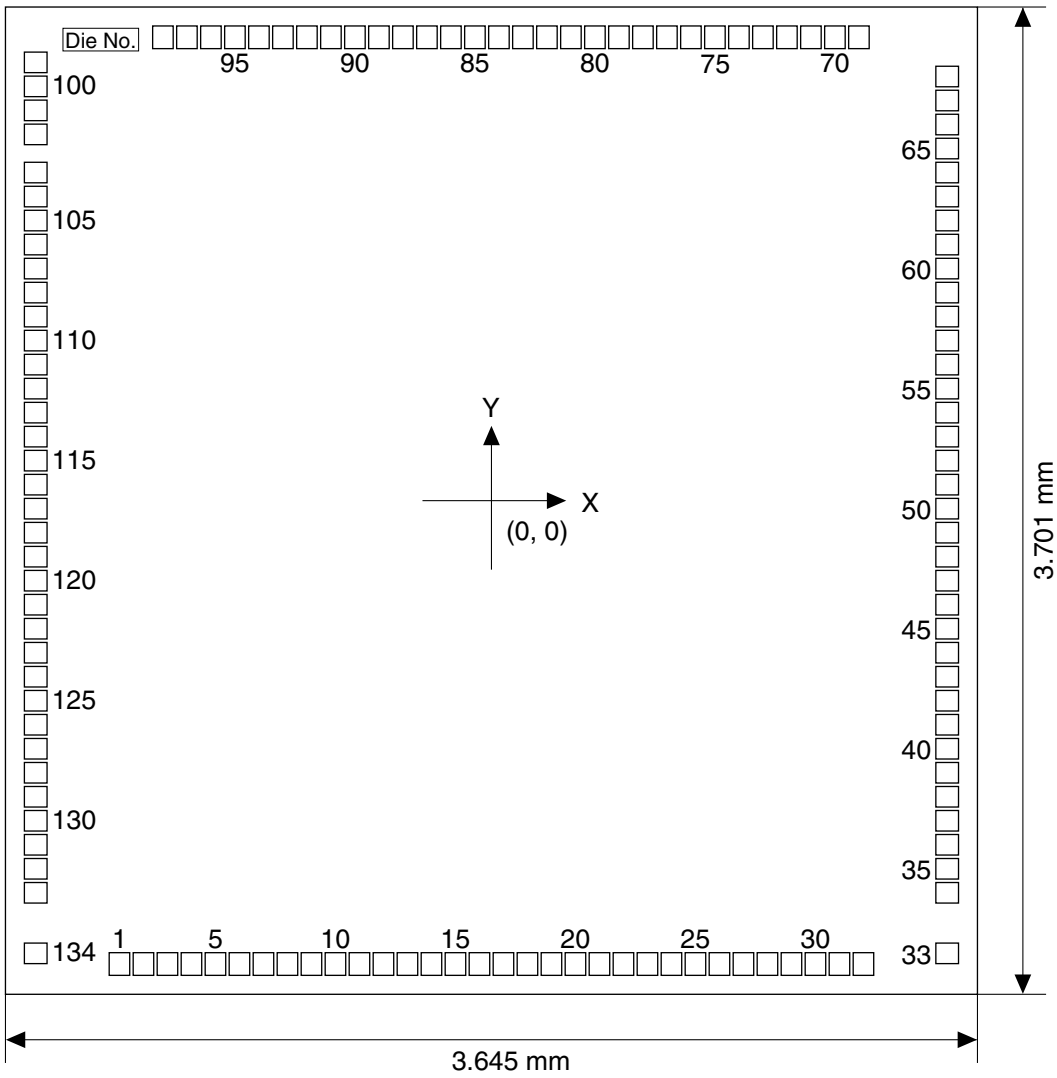
QFP17-144pin

(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 77 × 85 µm

9.2 Pad Coordinates

Unit: mm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	SEG16	-1.395	-1.737	46	COM18/SEG61	1.709	-0.390	91	P11/RUN/LAP	-0.602	1.737
2	SEG17	-1.305	-1.737	47	COM17/SEG62	1.709	-0.300	92	P10/RUN/LAP	-0.692	1.737
3	SEG18	-1.215	-1.737	48	COM16/SEG63	1.709	-0.210	93	P03/RFOUT/BZ	-0.782	1.737
4	SEG19	-1.125	-1.737	49	V_{SS}	1.709	-0.120	94	V_{DD}	-0.872	1.737
5	SEG20	-1.035	-1.737	50	V_{D2}	1.709	-0.030	95	P02/SEN0	-0.962	1.737
6	SEG21	-0.945	-1.737	51	CG	1.709	0.060	96	P01/REF0	-1.052	1.737
7	SEG22	-0.855	-1.737	52	CF	1.709	0.150	97	P00/RFIN0	-1.142	1.737
8	SEG23	-0.765	-1.737	53	CE	1.709	0.240	98	V_{SS}	-1.232	1.737
9	SEG24	-0.675	-1.737	54	CD	1.709	0.330	99	RFIN1	-1.709	1.643
10	SEG25	-0.585	-1.737	55	CC	1.709	0.420	100	REF1	-1.709	1.553
11	SEG26	-0.495	-1.737	56	CB	1.709	0.510	101	SEN1	-1.709	1.463
12	SEG27	-0.405	-1.737	57	CA	1.709	0.600	102	HUD	-1.709	1.373
13	SEG28	-0.315	-1.737	58	V_{C5}	1.709	0.690	103	COM0	-1.709	1.230
14	SEG29	-0.225	-1.737	59	V_{C4}	1.709	0.780	104	COM1	-1.709	1.140
15	SEG30	-0.135	-1.737	60	V_{C3}	1.709	0.870	105	COM2	-1.709	1.050
16	SEG31	-0.045	-1.737	61	V_{C2}	1.709	0.960	106	COM3	-1.709	0.960
17	SEG32	0.045	-1.737	62	V_{C1}	1.709	1.050	107	COM4	-1.709	0.870
18	SEG33	0.135	-1.737	63	V_{DD}	1.709	1.140	108	COM5	-1.709	0.780
19	SEG34	0.225	-1.737	64	OSC3	1.709	1.230	109	COM6	-1.709	0.690
20	SEG35	0.315	-1.737	65	OSC4	1.709	1.320	110	COM7	-1.709	0.600
21	SEG36	0.405	-1.737	66	V_{SS}	1.709	1.410	111	COM8	-1.709	0.510
22	SEG37	0.495	-1.737	67	OSC1	1.709	1.500	112	COM9	-1.709	0.420
23	SEG38	0.585	-1.737	68	OSC2	1.709	1.590	113	COM10	-1.709	0.330
24	SEG39	0.675	-1.737	69	V_{D1}	1.378	1.737	114	COM11	-1.709	0.240
25	SEG40	0.765	-1.737	70	V_{OSC}	1.288	1.737	115	COM12	-1.709	0.150
26	SEG41	0.855	-1.737	71	TEST	1.198	1.737	116	COM13	-1.709	0.060
27	SEG42	0.945	-1.737	72	RESET	1.108	1.737	117	COM14	-1.709	-0.030
28	SEG43	1.035	-1.737	73	P53	1.018	1.737	118	COM15	-1.709	-0.120
29	SEG44	1.125	-1.737	74	P52	0.928	1.737	119	SEG0	-1.709	-0.210
30	SEG45	1.215	-1.737	75	P51	0.838	1.737	120	SEG1	-1.709	-0.300
31	SEG46	1.305	-1.737	76	P50	0.748	1.737	121	SEG2	-1.709	-0.390
32	SEG47	1.395	-1.737	77	P43/EVIN_D	0.658	1.737	122	SEG3	-1.709	-0.480
33	COM31/SEG48	1.709	-1.697	78	P42/EVIN_C	0.568	1.737	123	SEG4	-1.709	-0.570
34	COM30/SEG49	1.709	-1.470	79	P41/EVIN_B	0.478	1.737	124	SEG5	-1.709	-0.660
35	COM29/SEG50	1.709	-1.380	80	P40	0.388	1.737	125	SEG6	-1.709	-0.750
36	COM28/SEG51	1.709	-1.290	81	P33/TOUT_D	0.298	1.737	126	SEG7	-1.709	-0.840
37	COM27/SEG52	1.709	-1.200	82	P32/TOUT_C	0.208	1.737	127	SEG8	-1.709	-0.930
38	COM26/SEG53	1.709	-1.110	83	P31/TOUT_B	0.118	1.737	128	SEG9	-1.709	-1.020
39	COM25/SEG54	1.709	-1.020	84	P30	0.028	1.737	129	SEG10	-1.709	-1.110
40	COM24/SEG55	1.709	-0.930	85	P23/SRDY/$\overline{SS}$/FOUT	-0.062	1.737	130	SEG11	-1.709	-1.200
41	COM23/SEG56	1.709	-0.840	86	P22/SIN	-0.152	1.737	131	SEG12	-1.709	-1.290
42	COM22/SEG57	1.709	-0.750	87	P21/SOUT	-0.242	1.737	132	SEG13	-1.709	-1.380
43	COM21/SEG58	1.709	-0.660	88	P20/SCLK	-0.332	1.737	133	SEG14	-1.709	-1.470
44	COM20/SEG59	1.709	-0.570	89	P13/TOUT_A	-0.422	1.737	134	SEG15	-1.709	-1.697
45	COM19/SEG60	1.709	-0.480	90	P12/EVIN_A	-0.512	1.737	–	–	–	–

APPENDIX A PERIPHERAL CIRCUIT BOARDS FOR S1C63632

This section describes how to use the Peripheral Circuit Boards for the S1C63632 (S5U1C63000P6 and S5U1C63632P2), which provide emulation functions when mounted on the debugging tool for the S1C63 Family of 4-bit single-chip microcomputers, the ICE (S5U1C63000H2/S5U1C63000H6).

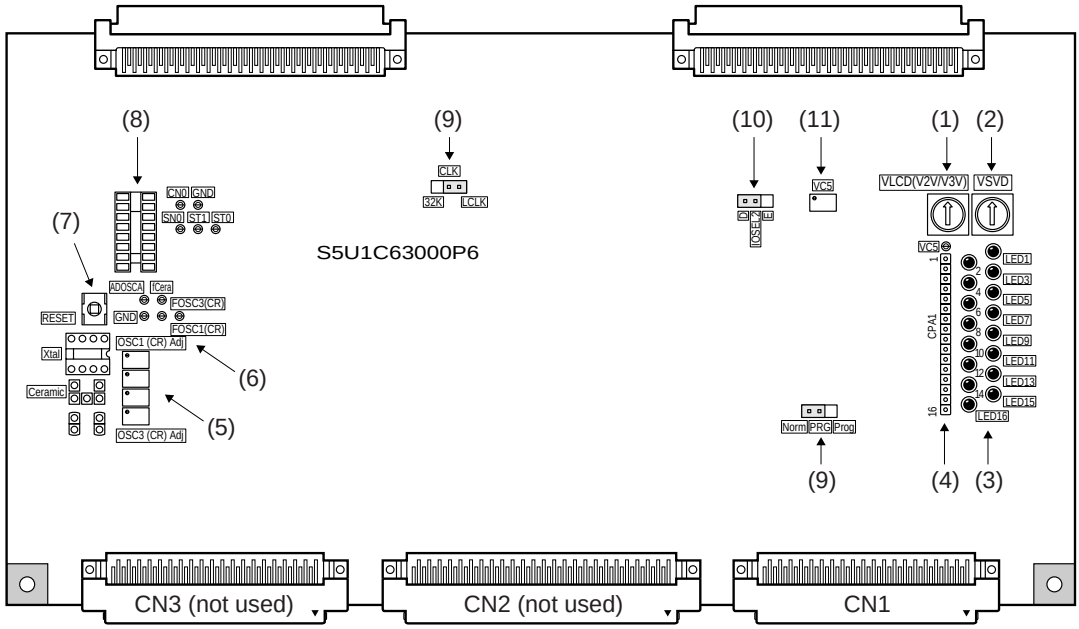
This description of the S1C63 Family Peripheral Circuit Board (S5U1C63000P6) provided in this document assumes that circuit data for the S1C63632 has already been downloaded to the board. For information on downloading various circuit data, please see Section A.3. Please refer to the manual provided with your ICE for detailed information on its functions and method of use.

Note: The S5U1C63000P1 cannot be used for developing the S1C63632 applications.

A.1 Names and Functions of Each Part

A.1.1 S5U1C63000P6

The S5U1C63000P6 board provides peripheral circuit functions of S1C63 Family microcomputers other than the core CPU. The following explains the names and functions of each part of the S5U1C63000P6 board.



(1) VLCD

Unused

(2) VSVD

This control allows you to vary the power supply voltage artificially in order to verify the operation of the power supply voltage detect function (SVD).

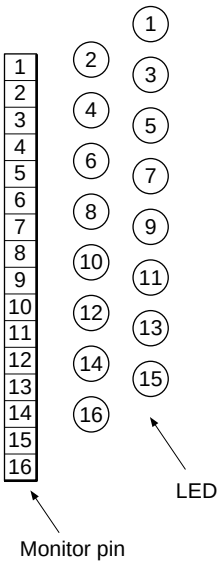
(3) Register monitor LEDs

These LEDs correspond one-to-one to the registers and motor driver outputs listed below. The LED lights when the data is logic "1" and goes out when the data is logic "0".
OSCC, CLKCHG, DBON, HLON, VCSEL, VDSEL, VCHLMOD, VDHLMOD, SVDON, SVDS0–SVDS3

(4) Register monitor pins

These pins correspond one-to-one to the registers and motor driver outputs listed below. The pin outputs a high for logic "1" and a low for logic "0".

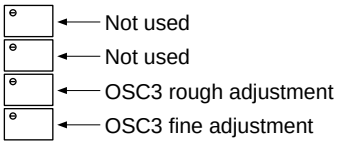
Monitor		LED	
Pin No.	Name	LED No.	Name
1	DONE *1	1	DONE *1
2	OSCC	2	OSCC
3	CLKCHG	3	CLKCHG
4	VDSEL	4	VDSEL
5	VCSEL	5	VCSEL
6	HLON	6	HLON
7	DBON	7	DBON
8	VCHLMOD	8	VCHLMOD
9	VDHLMOD	9	VDHLMOD
10	SVDON	10	SVDON
11	SVDS0	11	SVDS0
12	SVDS1	12	SVDS1
13	SVDS2	13	SVDS2
14	SVDS3	14	SVDS3
15	–	15	–
16	–	16	–



*1 DONE: The monitor pin outputs a high while the LED lights when initialization of this board completes without problems.

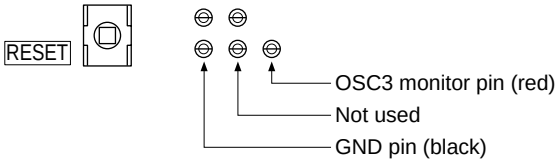
(5) CR oscillation frequency adjusting control

This control allows you to adjust the OSC3 oscillation frequency. This function is effective when ceramic oscillation is selected for the OSC3 oscillation circuit by mask option as well as when CR oscillation is selected. The oscillation frequency can be adjusted in the range of approx. 100 kHz to 8 MHz. Note that the actual IC does not operate with all of these frequencies; refer to Chapter 7, "Electrical Characteristics", to select the appropriate operating frequency.



(6) CR oscillation frequency monitor pins

These pins allow you to monitor the clock waveform from the CR oscillation circuit with an oscilloscope. Note that these pins always output a signal waveform whether or not the oscillation circuit is operating.



(7) RESET switch

This switch initializes the internal circuits of this board and feeds a reset signal to the ICE.

(8) External part connecting socket

Unused

(9) CLK and PRG switch

If power to the ICE is shut down before circuit data downloading is complete, the circuit configuration in this board will remain incomplete, and the debugger may not be able to start when you power on the ICE once again. In this case, temporarily power off the ICE and set CLK to the 32K position and the PRG switch to the Prog position, then switch on power for the ICE once again. This should allow the debugger to start up, allowing you to download circuit data. After downloading the circuit data, temporarily power off the ICE and reset CLK and PRG to the LCLK and the Norm position, respectively. Then power on the ICE once again.

(10) IOSEL2

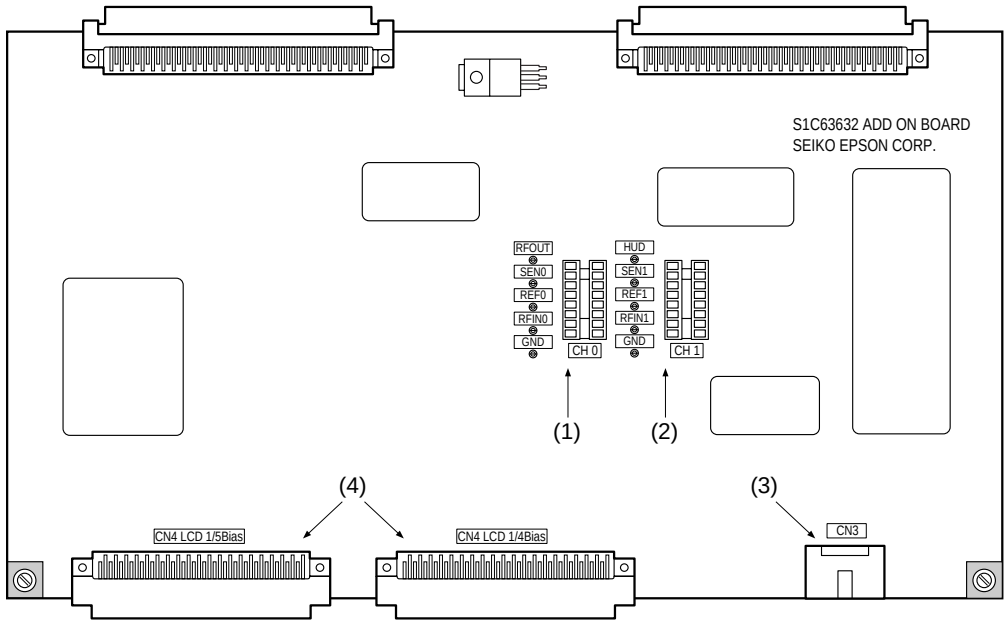
When downloading circuit data, set IOSEL2 to the "E" position. Otherwise, set to the "D" position.

(11) VC5

Unused

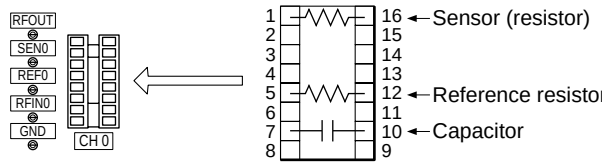
A.1.2 S5U1C63632P2

The S5U1C63632P2 board provides the R/f converter function that supports resistive sensors such as a thermistor and resistive humidity sensors and the LCD driver function.
The following explains the names and functions of each part of the S5U1C63632P2 board.



(1) R/f converter monitor pins and external part connecting socket (Channel 0)

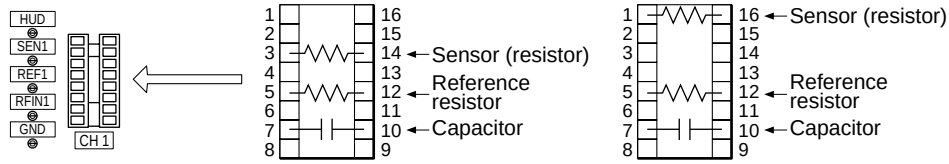
These monitor pins are used to check the operation of R/f converter channel 0. The socket is used to connect external resistors and a capacitor for R/f conversion.
Mount resistors and a capacitor on the platform attached with the S5U1C63632P2 and then connect it to the onboard socket.



Connecting a DC-bias
resistive sensor (e.g. thermistor)

(2) R/f converter monitor pins and external part connecting socket (Channel 1)

These monitor pins are used to check the operation of R/f converter channel 1. The socket is used to connect external resistors and a capacitor for R/f conversion.
Mount resistors and a capacitor on the platform attached with the S5U1C63632P2 and then connect it to the onboard socket.



Connecting a AC-bias
resistive humidity sensor

Connecting a DC-bias
resistive sensor (e.g. thermistor)

The sensor connect position changes according to the sensor type to be used.
Do not mount an AC bias sensor and a DC bias sensor at the same time as it causes a malfunction.

(3) CN3 (P0 I/O connector)

This is a user connector to input/output the P00 to P03 port signals. The P00 to P03 terminals of the actual IC are shared with the terminals for R/f converter channel 0. The S5U1C63632P2 board provides this connector separated with the R/f converter socket and monitor pins shown in (1) above. Therefore, be sure to leave this connector open when R/f converter channel 0 is used.

(4) CN4 (LCD connector)

This is a user connector to output the COM and SEG signals of the LCD driver. There are two connectors provided: one is for 1/5 bias and another is for 1/4 bias. Be sure to use one of them according to the specification of the target system. Use of the both connectors at the same time may cause a malfunction.

A.2 Connecting to the Target System

This section explains how to connect the target system.
First insert the S5U1C63000P6 board into the second upper slot of the ICE and the S5U1C63632P2 board into the top slot.
Download the circuit data to the S5U1C63000P6 board before installing the S5U1C63632P2 board if the S5U1C63000P6 board does not include the correct circuit data. See Section A.3 for downloading circuit data.

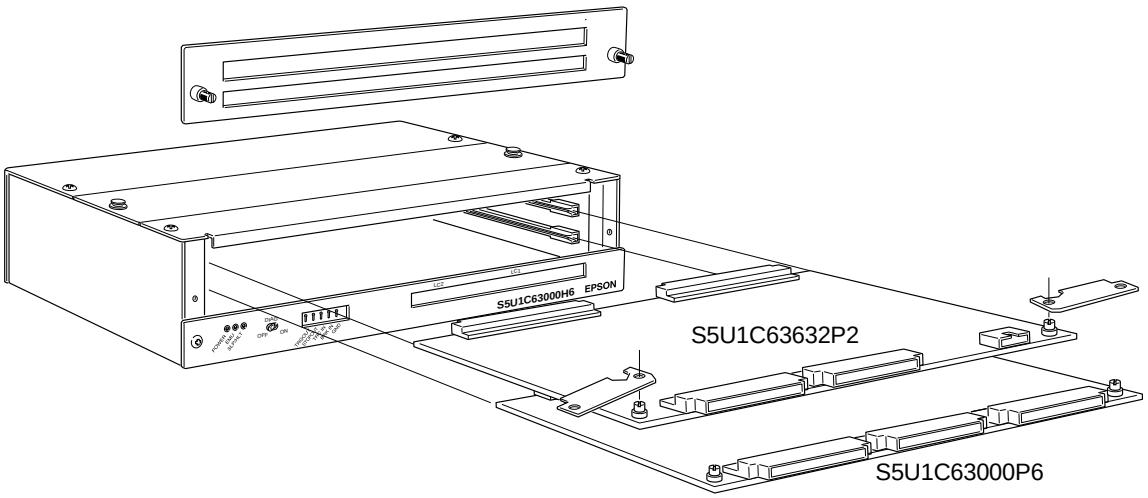


Fig. A.2.1 Installing the peripheral circuit boards to the ICE

- **Installing the S5U1C63000P6/63632P2 board**

Set the jig included with the ICE into position as shown in Figure A.2.2. Using this jig as a lever, push it toward the inside of the board evenly on the left and right sides. After confirming that the board has been firmly fitted into the internal slot of the ICE, remove the jig.

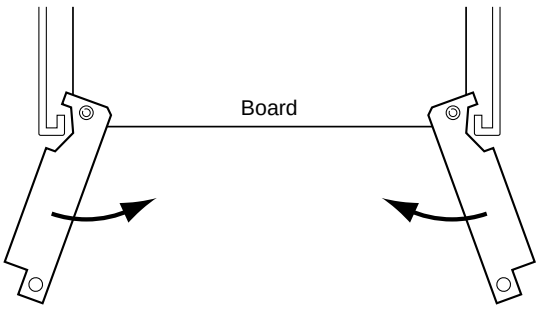


Fig. A.2.2
Installing the board

- **Dismounting the S5U1C63000P6/63632P2 board**

Set the jig included with the ICE into position as shown in Figure A.2.3. Using this jig as a lever, push it toward the outside of the board evenly on the left and right sides. After confirming that the board has been dismounted from the backboard connector, pull the board out of the ICE.

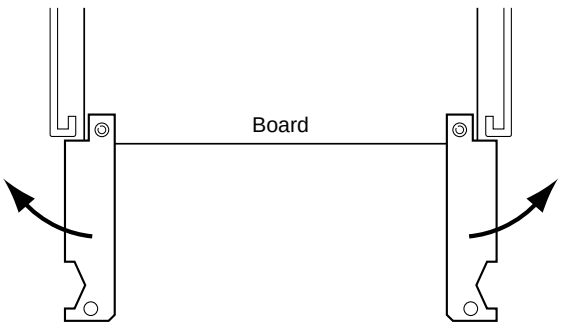


Fig. A.2.3
Dismounting the board

To connect the S5U1C63000P6 and S5U1C63632P2 to the target system, use the I/O connecting cables supplied with these boards. Take care when handling the connectors, since they conduct electrical power (V_{DD} = +3.3 V).

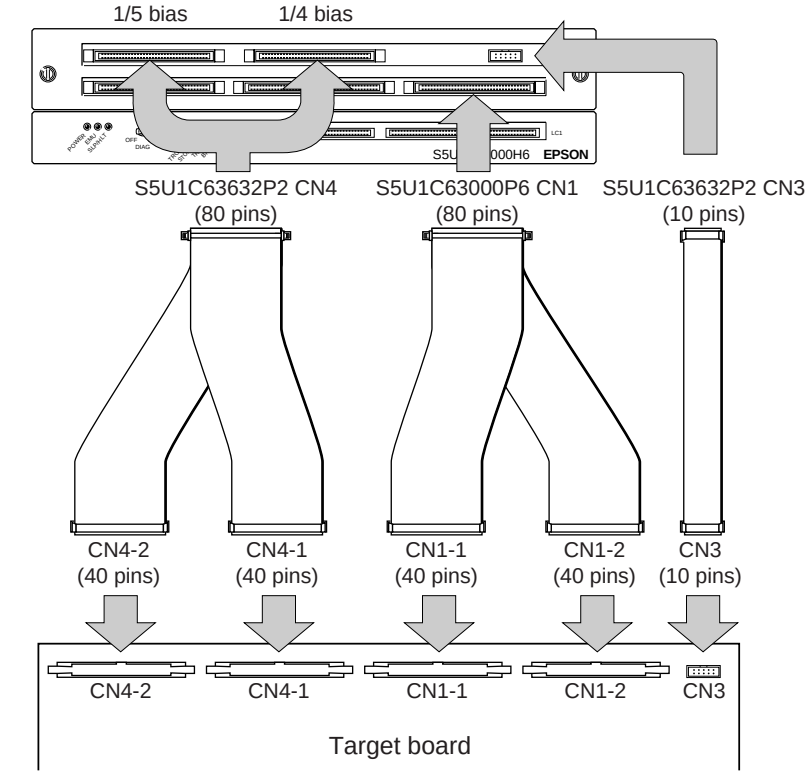


Fig. A.2.4 Connecting the S5U1C63000P6 and S5U1C63632P2 to the target system

Table A.2.1 S5U1C63000P6 I/O connector pin assignment

40-pin CN1-1 connector		40-pin CN1-2 connector	
No.	Pin name	No.	Pin name
1	VDD (= 3.3 V)	1	VDD (= 3.3 V)
2	VDD (= 3.3 V)	2	VDD (= 3.3 V)
3	Cannot be connected	3	Cannot be connected
4	Cannot be connected	4	Cannot be connected
5	Cannot be connected	5	Cannot be connected
6	Cannot be connected	6	Cannot be connected
7	Cannot be connected	7	Cannot be connected
8	Cannot be connected	8	Cannot be connected
9	Cannot be connected	9	Cannot be connected
10	Cannot be connected	10	Cannot be connected
11	VSS	11	VSS
12	VSS	12	VSS
13	P10	13	Cannot be connected
14	P11	14	Cannot be connected
15	P12	15	Cannot be connected
16	P13	16	Cannot be connected
17	P20	17	Cannot be connected
18	P21	18	Cannot be connected
19	P22	19	Cannot be connected
20	P23	20	Cannot be connected
21	VDD (= 3.3 V)	21	VDD (= 3.3 V)
22	VDD (= 3.3 V)	22	VDD (= 3.3 V)
23	P30	23	Cannot be connected
24	P31	24	Cannot be connected
25	P32	25	Cannot be connected
26	P33	26	Cannot be connected
27	P40	27	Cannot be connected
28	P41	28	Cannot be connected
29	P42	29	Cannot be connected
30	P43	30	Cannot be connected
31	Vss	31	VSS
32	Vss	32	VSS
33	P50	33	Cannot be connected
34	P51	34	Cannot be connected
35	P52	35	Cannot be connected
36	P53	36	Cannot be connected
37	Cannot be connected	37	Cannot be connected
38	Cannot be connected	38	RESET
39	Vss	39	VSS
40	Vss	40	VSS

Table A.2.2 S5U1C63632P2 I/O connector pin assignment

10-pin CN3 connector	
No.	Pin name
1	VDD (= 3.3 V)
2	VDD (= 3.3 V)
3	P00
4	P01
5	P02
6	P03
7	Cannot be connected
8	Cannot be connected
9	Vss
10	Vss

40-pin CN4-1 connector		40-pin CN4-2 connector	
No.	Pin name	No.	Pin name
1	COM0	1	SEG24
2	COM1	2	SEG25
3	COM2	3	SEG26
4	COM3	4	SEG27
5	COM4	5	SEG28
6	COM5	6	SEG29
7	COM6	7	SEG30
8	COM7	8	SEG31
9	COM8	9	SEG32
10	COM9	10	SEG33
11	COM10	11	SEG34
12	COM11	12	SEG35
13	COM12	13	SEG36
14	COM13	14	SEG37
15	COM14	15	SEG38
16	COM15	16	SEG39
17	SEG0	17	SEG40
18	SEG1	18	SEG41
19	SEG2	19	SEG42
20	SEG3	20	SEG43
21	SEG4	21	SEG44
22	SEG5	22	SEG45
23	SEG6	23	SEG46
24	SEG7	24	SEG47
25	SEG8	25	COM31/SEG48
26	SEG9	26	COM30/SEG49
27	SEG10	27	COM29/SEG50
28	SEG11	28	COM28/SEG51
29	SEG12	29	COM27/SEG52
30	SEG13	30	COM26/SEG53
31	SEG14	31	COM25/SEG54
32	SEG15	32	COM24/SEG55
33	SEG16	33	COM23/SEG56
34	SEG17	34	COM22/SEG57
35	SEG18	35	COM21/SEG58
36	SEG19	36	COM20/SEG59
37	SEG20	37	COM19/SEG60
38	SEG21	38	COM18/SEG61
39	SEG22	39	COM17/SEG62
40	SEG23	40	COM16/SEG63

A.3 Downloading to S5U1C63000P6

Note: The S1C63632 circuit data is available only for the S5U1C63000P6, and it cannot be downloaded to the previous S5U1C63000P1 board.

A.3.1 Downloading Circuit Data 1 – when new ICE (S5U1C63000H2/S5U1C63000H6) is used

The S5U1C63000P6 board comes with the FPGA that contains factory inspection data, therefore the circuit data for the model to be used should be downloaded. The following explains the downloading procedure.

1) Remove the ICE (S5U1C63000H2/S5U1C63000H6) top cover and then set the DIP switch "IOSEL2" on the S5U1C63000P6 board to the "E" position.
2) Connect the ICE to the host PC. Then turn the host PC and ICE on.
3) Invoke the debugger included in the assembler package (ver. 5 or later for the S5U1C63000H2, ver. 9 or later for the S5U1C63000H6). For how to use the ICE and debugger, refer to the manuals supplied with the ICE and assembler package.
4) Download the circuit data file (.mot) corresponding to the model by entering the following commands in the command window.

`>XFER`	(erase all)
`>XFWR` <*file name*>	(download the specified file)*
`>XFCP` <*file name*>	(compare the specified file and downloaded data)

   * The downloading takes about 15 minutes in the S5U1C63000H2 or about 3 minutes in the S5U1C63000H6.
5) Terminate the debugger and then turn the ICE off.
6) Set the DIP switch "IOSEL2" on the S5U1C63000P6 board to the "D" position.
7) Turn the ICE on and invoke the debugger again. Debugging can be started here.

A.3.2 Downloading Circuit Data 2 – when previous ICE (S5U1C63000H1) is used

The standard ICE (S5U1C63000H1, previous model) did not support the circuit data download function for the S5U1C63000P6 board. To use the download function, update the ICE firmware according to the following procedure.

1) Set the baud rate of the ICE to 9600 bps. Refer to the manual supplied with the ICE for setting the DIP switch.
2) Connect the ICE to the host PC and then start up the host PC in DOS. When Windows is running, restart in DOS mode.

   Note: Do not use the DOS prompt of Windows.
3) Turn the ICE on.
4) Configure the RS232C parameters for the host PC as follows:

   `C:\>MODE COM1:9600,n,8,1,p` (9600 bps, 8-bit data, 1 stop bit, no parity)
5) Copy the following files included in the assembler package (ver. 5 or later) to a directory on the hard disk.

   `tm63.exe, ice63.com, i63com.o, i63par`
6) Move to the directory in Step 5, run the TM63. TM63 enters command ready status after invocation, enter a command as follows:

```
C:\>tm63 xat↵
TM63 start on IBM PC
TM63 start V01.01
>dlf ice63.com i63com.o i63par 0b↵
                ...
>q↵
```

7) Enter "q" to terminate TM63 after the prompt mark is displayed.
8) The ICE firmware is now updated. Turn the ICE off and then download the circuit data by the procedure described in Section A.3.1.

A.4 Usage Precautions

To ensure correct use of the peripheral circuit board, please observe the following precautions.

A.4.1 Operational precautions

(1) Before inserting or removing cables, turn off power to all pieces of connected equipment.
(2) Do not turn on power or load mask option data if all of the I/O ports (P10–P13) are held low. Doing so may activate the multiple key entry reset function.
(3) Before debugging, always be sure to load mask option data.

A.4.2 Differences with the actual IC

(1) Differences in I/O

<Interface power supply>
S5U1C63000P6 and target system interface voltage is set to +3.3 V. To obtain the same interface voltage as in the actual IC, attach a level shifter circuit, etc. on the target system side to accommodate the required interface voltage.

<Each output port's drive capability>
The drive capability of each output port on S5U1C63000P6 is higher than that of the actual IC. When designing application system and software, refer to Chapter 7, "Electrical Characteristics", to confirm each output port's drive capability.

<Each port's protective diode>
All I/O ports incorporate a protective diode for V_{DD} and V_{SS}, and the interface signals between S5U1C63000P6 and the target system are set to +3.3 V. Therefore, S5U1C63000P6 and the target system cannot be interfaced with voltages exceeding V_{DD} by setting the output ports for open-drain mode.

<Pull-down resistance value>
The pull-down resistance values on S5U1C63000P6 are set to 220 kΩ which differ from those for the actual IC. For the resistance values on the actual IC, refer to Chapter 7, "Electrical Characteristics". Note that when using pull-down resistors to pull the input pins low, the input pins may require a certain period to reach a valid low level. Exercise caution if a key matrix circuit is configured using a combination of output and input ports, since fall delay times on these input ports differ from those of the actual IC.

<Schmitt input>
The I/O ports of the actual IC allow use of Schmitt input interface. The S5U1C63000P6 supports CMOS level interface only and does not supports Schmitt inputs.

(2) Differences in current consumption

The amount of current consumed by the peripheral circuit boards differ significantly from that of the actual IC. Inspecting the LEDs on S5U1C63000P6 may help you keep track of approximate current consumption. The following factors/components greatly affect device current consumption:

<Those which can be verified by LEDs and monitor pins>
a) Run and Halt execution ratio (verified by LEDs and monitor pins on the ICE)
b) OSC3 oscillation on/off circuit (OSCC)
c) CPU clock select circuit (CLKCHG)
d) SVD circuit on/off circuit (SVDON)

<Those that can only be counteracted by system or software>
e) Current consumed by the internal pull-down resistors
f) Input ports in a floating state

(3) Functional precautions

<LCD driver>

The S1C63632 chips included in the S5U1C63632P2 board generate the LCD drive waveform. The S5U1C63632P2 has two on-board S1C63632 chips and one of them is used for 1/4 bias drive and another is used for 1/5 bias drive. Note that both the CN4 connector for 1/4 bias and CN4 connector for 1/5 bias on the S5U1C63632P2 board output the LCD drive waveforms regardless of which option is selected. The target board must be connected to the connector for the drive bias used in the application.

<SVD circuit>

- The SVD function is realized by artificially varying the power supply voltage using the VSVD control on S5U1C63000P6. However, the S5U1C63000P6 supports detection of eight levels (0000B to 0111B) only and the SVD3 register value is ignored (e.g. the same detection results are obtained when SVDS = 1111B and when SVDS = 0111B). The SVDS3 value should be checked with the monitor LED.
- There is a finite delay time from when the power to the SVD circuit turns on until actual detection of the voltage. On S5U1C63000P6, there is no delay, which differs from that of the actual IC. Refer to Chapter 7, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.

<Oscillation circuit>

- A wait time is required before oscillation stabilizes after the OSC3 oscillation control circuit (OSCC) is turned on. On S5U1C63000P6, even when OSC3 oscillation is changed (CLKCHG) without a wait time, OSC3 will function normally. Refer to Chapter 7, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.
- Use separate instructions to switch the clock from OSC3 to OSC1 and to turn off the OSC3 oscillation circuit. If executed simultaneously with a single instruction, these operations, although good with S5U1C63000P6, may not function properly well with the actual IC.
- Because the logic level of the oscillation circuit is high, the timing at which the oscillation starts on S5U1C63000P6 differs from that of the actual IC.
- S5U1C63000P6 contains oscillation circuits for OSC1 and OSC3. Keep in mind that even though the actual IC may not have a resonator connected to its OSC3, its emulator can operate with the OSC3 circuit.
- S5U1C63000P6 generates the OSC3 clock using the onboard CR oscillation circuit even if ceramic oscillation is selected for the OSC3 oscillation circuit by mask option.

<Access to undefined address space>

If any undefined space in the S1C63632's internal ROM/RAM or I/O is accessed for data read or write operations, the read/written value is indeterminate. Additionally, it is important to remain aware that indeterminate state differs between S5U1C63000P6 and the actual IC. Note that the ICE (S5U1C63000H2/S5U1C63000H6) incorporates the program break function caused by accessing to an undefined address space.

<Reset circuit>

Keep in mind that the operation sequence from when the ICE and the peripheral circuit boards (S5U1C63000P6 and S5U1C63632P2) are powered on until the time at which the program starts running differs from the sequence from when the actual IC is powered on till the program starts running. This is because S5U1C63000P6 becomes capable of operating as a debugging system after the user program and optional data are downloaded. When operating the ICE after placing it in free-running mode*, always apply a system reset. A system reset can be performed by pressing the reset switch on S5U1C63000P6, by a reset pin input, or by holding the input ports high simultaneously.
(* Free running mode: supported by S5U1C63000H1/2 only)

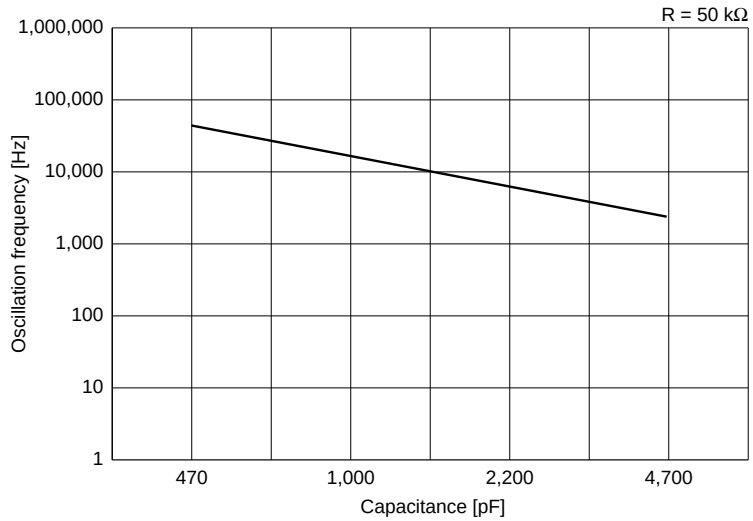
<I/O ports>

- Do not set the P1x ports used for multiple key entry reset to output mode as the S5U1C63000P6 and S5U1C63632P2 may be reset.
- Do not enable the input interrupt or peripheral input function of the I/O port that has been set to output mode. An interrupt processing may start in the S5U1C63000P6 and S5U1C63632P2.

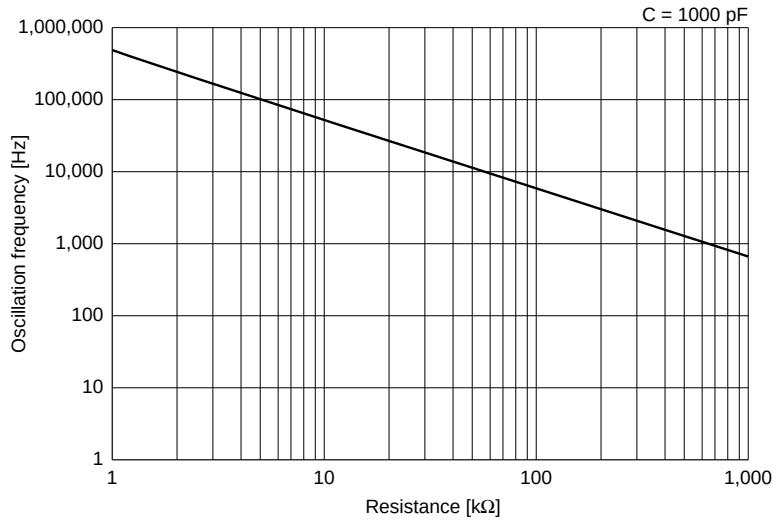
<R/f converter>

- The R/f converter function is implemented using the S1C63632 chip included in the S5U1C63632P2 board.
- If the debugger makes program execution to break while the R/f converter is counting the oscillation, the R/f converter does not stop counting. Note that the R/f converter will not able to load a proper result if program execution is resumed from that point.
- The following shows the oscillation characteristics (reference value) of the R/f converter on the S5U1C63632P2:

R/f converter oscillation frequency - capacitance characteristic (reference value)



R/f converter oscillation frequency - resistance characteristic (reference value)



A.5 Product Specifications

A.5.1 Specifications of S5U1C63000P6

S5U1C63000P6

Dimension:	254 mm (wide) × 144.8 mm (depth) × 16 mm (height)	(including screws)
Weight:	Approx. 250 g	
Power supply:	DC 5 V ± 5%, less than 1 A	(supplied from ICE main unit)

I/O connection cable (80-pin)

S5U1C63000P6 connector:	KEL8830E-080-170L-F	
Cable connector (80-pin):	KEL8822E-080-171-F	
Cable connector (40-pin):	3M7940-6500SC	1 pair
Cable:	40-conductor flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

I/O connection cable (100-pin)

S5U1C63000P6 connector:	KEL8830E-100-170L-F	
Cable connector (100-pin):	KEL8822E-100-171-F	
Cable connector (50-pin):	3M7950-6500SC	1 pair
Cable:	50-conductor flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

Accessories

40-pin connector for connecting to target system:		
	3M3432-6002LCPL	× 2
50-pin connector for connecting to target system:		
	3M3433-6002LCPL	× 2

A.5.2 Specifications of S5U1C63632P2

S5U1C63632P2

Dimension:	254 mm (width) × 144.8 mm (depth) × 13 mm (height) (including screws)
Weight:	Approx. 170 g
Power supply:	DC 5 V ± 5%, less than 50 mA (supplied from ICE main unit and converted into 3.3 V by the onboard regulator)

I/O connection cable (80-pin)

S5U1C63632P2 connector:	KEL8830E-080-170L-F	
Cable connector (80-pin):	KEL8822E-080-171-F	
Cable connector (40-pin):	3M7940-6500SC	1 pair
Cable:	40-conductor flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

I/O connection cable (10-pin)

S5U1C63632P2 connector:	3M3654-5002-PL
Cable connector (10-pin):	3M7910-6500SC
Cable:	10-conductor flat cable
Interface:	CMOS interface (3.3 V)
Length:	Approx. 40 cm

Accessories

40-pin connector for connecting to target system:
3M3432-6002LCPL × 2

10-pin connector for connecting to target system:
3M3662-6002LCPL × 1

Discreet platform (for mounting external resistors and capacitors of the R/f converter):
DIS12-016-403 (KEL) × 2

Revision History

Code No.	Page	Contents
411863800	All	New establishment

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