S1C17554/564



16-bit Single Chip Microcontroller

- ●48-pin wafer-chip-scale package (WCSP)
- ●10-bit A/D converter
- Code-efficient architecture optimized for the C language, single-cycle instruction high processing performance, serial ICE, and built-in 16-bit RISC PCU core S1C17

■ DESCRIPTIONS

The S1C17554/564 is a compact 16-bit MCU that delivers high-speed, low power operation with large address space and on-chip ICE. It integrates A/D converter and thus various analog-interface sensors are connectable. The ultra small power-saving 48-pin WCSP is most suitable for sensor-applied products that require low power consumption and high-speed processing.

■ FEATURES

The main features of the S1C17554/564 are listed below.

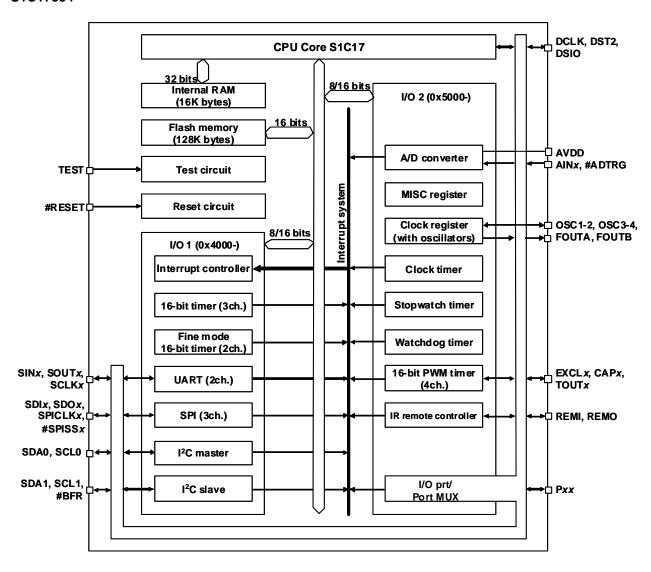
Model	S1C17554	S1C17564
CPU		
CPU core	Seiko Epson original 16-bit RISC CPU core S1C17	
Multiplier/Divider (COPRO)	16-bit × 16-bit multiplier 16-bit × 16-bit + 32-bit multiply and accumulation unit 16-bit ÷ 16-bit divider	
Embedded Flash memory		
Capacity	128K bytes (for both instructions and data)	
Erase/program count	Min. 1 time	
Other	 Read/program protection function An erasing/programming power supply (VPP) is required. Allows on-board programming using a debugging tool such as ICDmini. 	
Embedded RAM		<u> </u>
Capacity	16K bytes	
Clock generator		
System clock source	2 sources (OSC3/OSC1)	3 sources (IOSC/OSC3/OSC1)
IOSC oscillator circuit		2/4/8/12 MHz(typ.) internal oscillator circuit
OSC3 oscillator circuit	24 MHz (max.) crystal or ceramic oscillator circuit Supports an external clock input.	
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator circuit Supports an external clock input.	
Other	Core clock frequency control Peripheral module clock supply control	
I/O ports		
Number of general-purpose I/C ports	Max. 40 bits (TQFP13-64pin package) Max. 34 bits (WCSP-48 package) (Pins are shared with the peripheral I/O.)	Max. 40 bits (Pins are shared with the peripheral I/O.)
Serial interfaces	1 1 2 2 2 2 7	1
SPI	3 channels	
I ² C master (I2CM)	1 channel	
I ² C slave (I2CS)	1 channel	
UART	2 channels (IrDA1.0 supported)	
IR remote controller (REMC)	1 channel	
Universal serial interface (USI)		2 channels (Usable as a UART, SPI, or I ² C)
Timers		
16-bit timer (T16)	3 channels	
Fine mode 16-bit timer (T16F)	2 channels	
16-bit PWM timer (T16A)	4 channels	
Clock timer (CT)	1 channel	
Stopwatch timer (SWT)	1 channel	

S1C17554/564

Watchdog timer (WDT)	1 channel		
A/D converter			
Conversion method	Successive approximation type		
Number of analog input channels	4 channels (max.)		
Resolution	10 bits		
Interrupts	1		
Reset interrupt	#RESET pin		
NMI	Watchdog timer		
Programmable interrupts	23 systems (8 levels)		
Power supply voltage	(0.0.00)		
Core voltage (LVDD)	1.65 V to 1.95 V	1.65 V to 1.95 V (Not required	
Coro voltago (EVEE)	1.00 V 10 1.00 V	when the regulator is used.)	
I/O voltage (HVDD)	1.65 V to 5.5 V	2.0 V to 5.5 V (Regulator used) 1.65 V to 5.5 V (Regulator not used)	
Analog voltage (AVDD)	2.7 V to 5.5 V		
Flash programming voltage (VPP)	7 V/7.5V		
Regulator	1		
Input voltage		2.0 V to 5.5 V	
Output voltage		1.8 V	
Other		Enables the system to operate with	
		a 3.3 V or 5.0 V single power supply.	
Operating temperature		1 0.0 v dirigio power cappiy.	
Operating temperature range -40° C to 85° C			
Current consumption (Typ value, LVDD = HVDD = 1.8 V)			
SLEEP state	0.8 µA	1.2 µA	
	(OSC1 = Off, OSC3 = Off)	(OSC1 = Off, IOSC = Off, OSC3 = Off)	
HALT state	2.7 μA (OSC1 = 32 kHz, OSC3 = Off)	3.1 μA (OSC1 = 32 kHz, IOSC = Off, OSC3 = Off)	
Run state	16 μA (OSC1 = 32 kHz, OSC3 = Off)	16 μA (OSC1 = 32 kHz, IOSC = Off, OSC3 = Off)	
	3000 μA (OSC1 = Off, OSC3 = 8 MHz ceramic)	3000 µA (OSC1 = Off, IOSC = Off, OSC3 = 8 MHz ceramic)	
		4500 μA (OSC1 = Off, IOSC = 12 MHz, OSC3 = Off)	
A/D conversion	380 μA (AVDD = 3.6 V, 100 kHz sampling, FSEL[1:0] = 0x0, XPD[1:0] = 0x3)		
Shipping form			
1	TQFP13-64pin (10 mm × 10 mm × 1.0 mm, lead pitch: 0.5 mm)		
2	Die form (3.137 mm × 3.137 mm, pad pitch: 140 μm)		
3	WCSP-48 (3.137 mm × 3.137 mm		
	× 0.72 mm, ball pitch: 0.4 mm)		

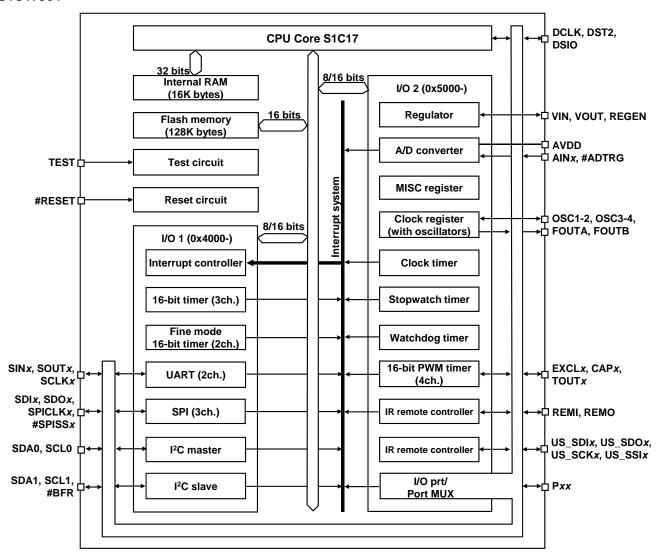
■ BLOCK DIAGRAM

S1C17554



S1C17554/564

S1C17564



NOTICE:

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. When exporting the products or technology described in this material, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You are requested not to use, to resell, to export and/or to otherwise dispose of the products (and any technical information furnished, if any) for the development and/or manufacture of weapon of mass destruction or for other military purposes.

All brands or product names mentioned herein are trademarks and/or registered trademarks of their respective companies.

©Seiko Epson Corporation 2013 All rights reserved

SEIKO EPSON CORPORATION

MICRODEVICES OPERATIONS DIVISION

IC Sales & Marketing Department 421-8 Hino, Hino-shi, Tokyo 191-8501, JAPAN Phone: +81-42-587-5814 FAX: +81-42-587-5117 EPSON semiconductor website

http://www.epson.jp/device/semicon_e/

Document code: 411827101 First issue April, 2010 Revised Aug, 2013.