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S2S65A30
Technical Manual (2)

SEIKO EPSON CORPORATION

Rev.1.3

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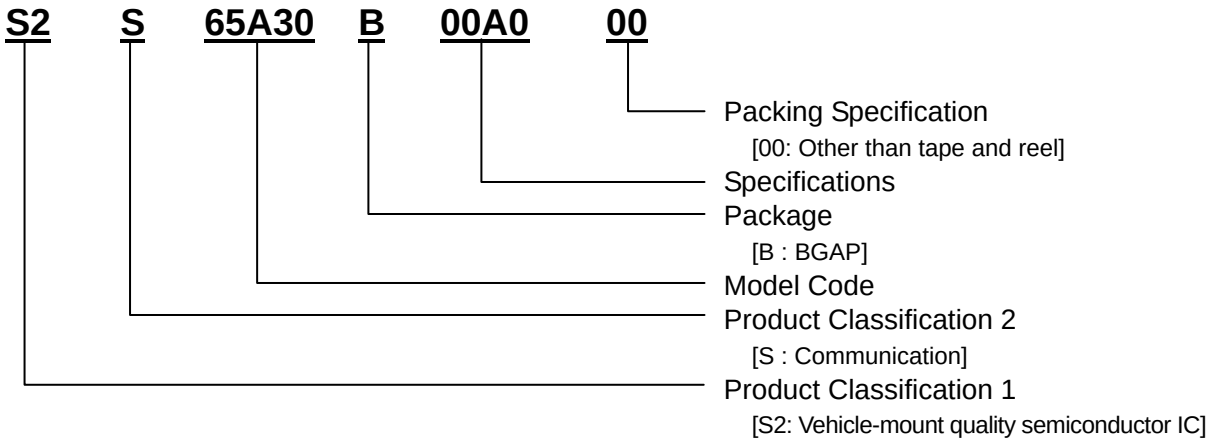
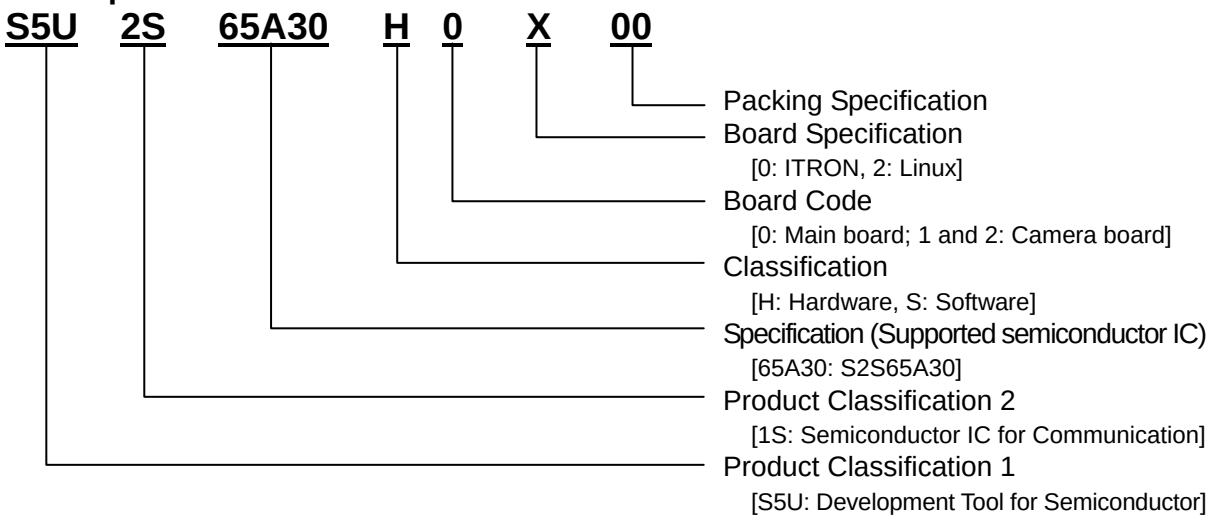
Configuration of product number

● **Device**



● **Development tool**



Precautions in Use

For descriptions of the registers in this document, be careful with the following:

For descriptions of the registers in this document, the following abbreviations may be used.

- R/W: Read and Write
- RO: Read Only
- WO: Write Only
- RSV: Reserved bit/register (write down “0”, if not otherwise specified)
- n/a: not available (write down “0”, if not otherwise specified)

If not otherwise specified, set “0” in the reserved bits for the registers. If a write operation performed on a reserved bit, unexpected results may occur. The bits specified as “n/a” have no impact on the hardware.

Some of the resisters can be accessed only under certain conditions. Read/write to the non-accessible registers is ineffective.

Table of Contents

19. SERIAL PERIPHERAL INTERFACE (SPI)

19.1 Description

The Serial Peripheral Interface (SPI) has a one-channel configuration.
The SPI supports operations in either master or slave mode and transfers data in bits 1 to 32. It can insert a delay ranging from 0 to 65535 clocks between each data transfer and can also generate an internal interrupt. It has data buffers for transmission and reception. The SPI provides four pins. The pin for SRDY# signal is internally fixed to LOW and cannot be used as an external pin.

19.1.1 Master Mode

An SPI set to master mode controls data transfer with a slave device connected to the SPI bus. An SPI supplies serial clock through the SCLK pin. Serial data is output from the MOSI pin and input to the MISO pin. An SPI has an SS (slave select) pin. Although this pin is not required for data transfer, it can be used for mode violation error detection. A mode violation error occurs when more than one device are set as the master at the same time in a multi-master SPI system. When an SPI in master mode detects that the SS pin becomes active level, a mode violation error interrupt is generated and the SPI is automatically reset to slave mode in order to avoid signal contention. If you do not have to detect mode violation errors, you can use the SS pin as a general I/O port.
To start a data transfer, enable the SPI (operable) and then write data to the transmit data register (TXD).
Figure 19.1 shows the control/operation flow in master mode.

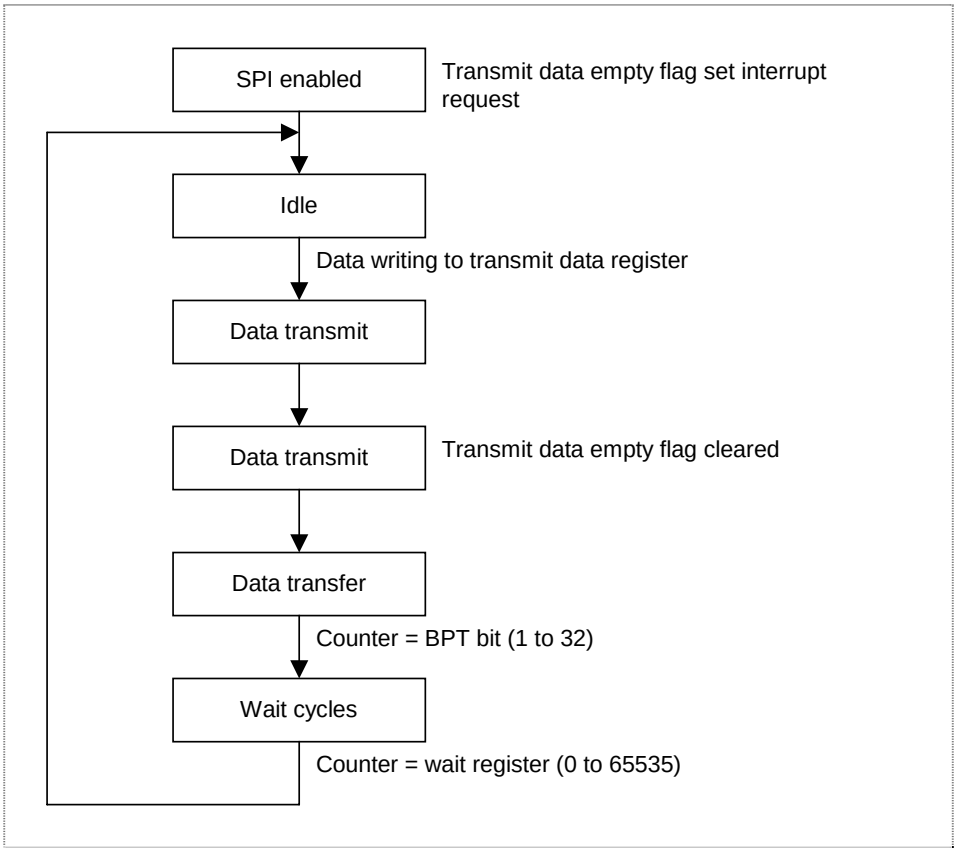


Figure 19.1 Transmission Flow in SPI Master Mode

19.1.2 Slave Mode

If an SPI is set to slave mode, an external SPI master controls data transfer with the SPI. A slave SPI receives operation clock from the external master at the SCLK pin and uses it. Serial data is input to the MOSI pin and output from the MISO pin. SS (slave select) pin is used for input.
Serial clock input and transfer operation are enabled as a result of the SS pin becoming active level.
After SPI is enabled (brought to operable), the external SPI master starts a transfer. The built-in counter that operates with SCLK clock controls transmission and reception for the specified number of transfer bits.
If more SCLK clock than the specified number of transfer bits is input, the transfer data is guaranteed only for the specified number of transfer bits.
Figure 19.2 shows the control/operation flow in slave mode.

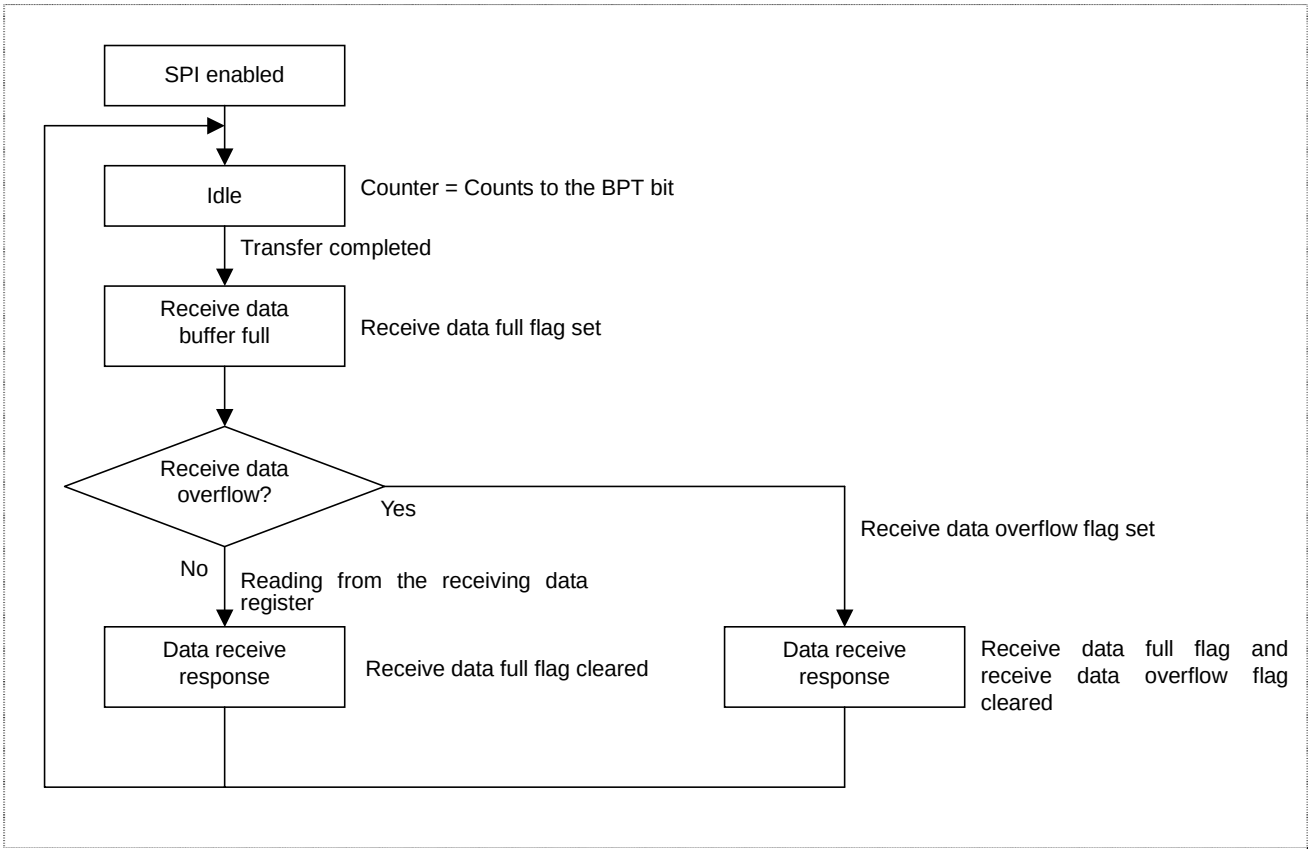


Figure 19.2 Reception Flow in SPI Slave Mode

19.2 Block Diagram

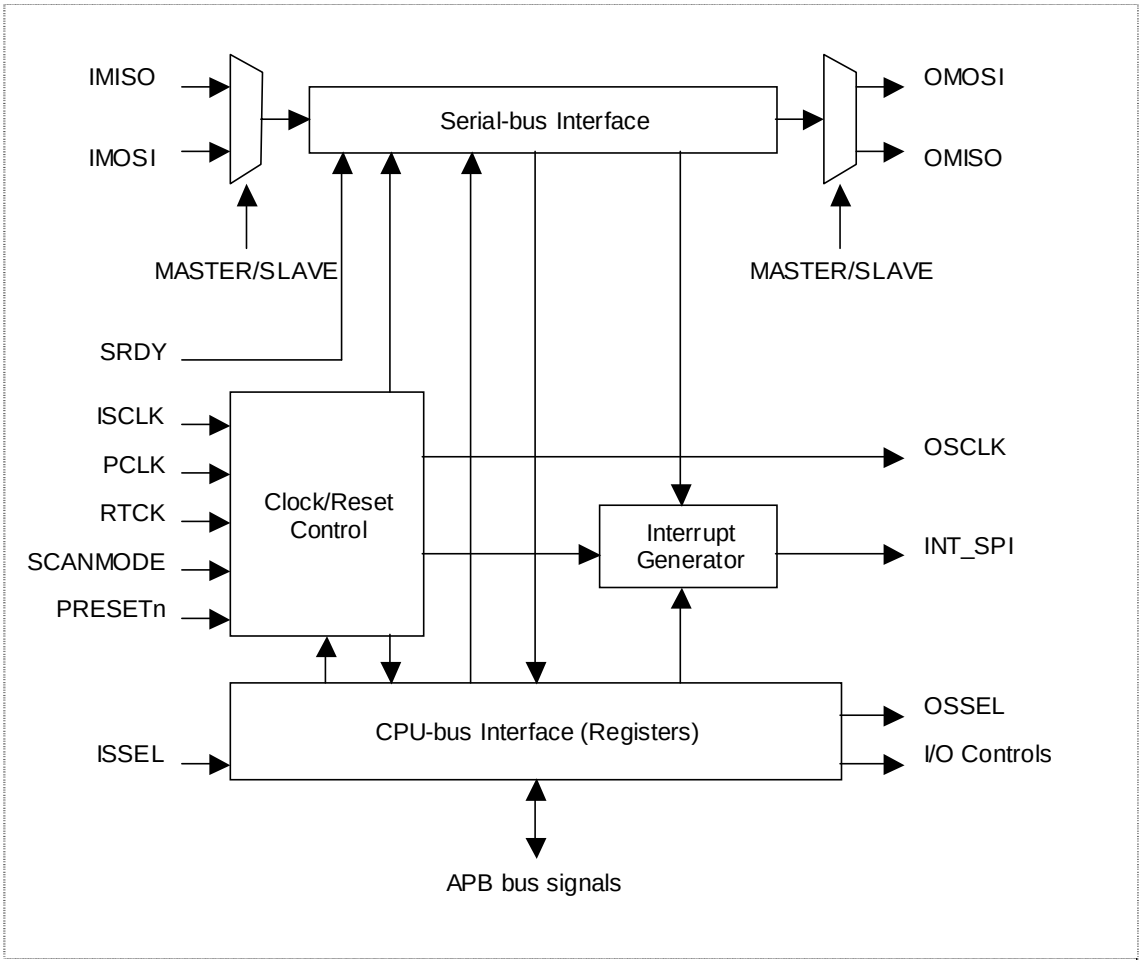


Figure 19.3 SPI Block Diagram

19.3 External Pins

The external pins related to the serial peripheral interface are as follows.

Pin Name	Input/Output	Pin Functions	Multiplex Pin/Remarks
SPI_SCLK	Input and output	SPI serial clock	GPIOC5*
SPI_SS	Input and output	SPI chip select	GPIOC4*
SPI_MISO	Input and output	SPI serial data master input/slave output	GPIOC6*
SPI_MOSI	Input and output	SPI serial data master output/slave input	GPIOC7*

Note (*): The external pins for SPI are multiplexed with GPIO pins or other pins. You can use the functions for SPI by setting “Function 2 of other than GPIO” through the GPIO pin function register.

19.4 Clock and Data Transfer Timing

If you use an SPI in master mode, use internal SCLK clock to make the shift register operate that is responsible for input and output of transfer data. There are four types of SCLKs to choose from that have different combination of clock phases and polarities.
You select a clock phase by using the CPHA bit (Bit 9 of the SPI control register 1). If the CPHA bit is set to "0", the output data changes at the falling edge of the clock (output from the shift register) and the input data is captured into the shift register at the rising edge of the clock (the bits in the sift register sequentially shift). Writing data to the transmit data register outputs MSB. If the CPHA bit is set to "1", the output changes at the rising edge and the input is captured at the falling edge. The MSB of the data is output at the first rising edge of the SCLK.
You select a clock polarity by using the CPOL bit (Bit 8 of the SPI control register 1). If the CPOL bit is set to "0", it means active high; "1", active low. In the above mentioned description of CPHA, the input and output timings assume that the clock is active high. If the CPOL bit is set to "1", the rising and falling edges are reversed. However, the timings of the edge trigger events inside the SIP are not reversed.
Figure 19.4 illustrates SCLK clock waveform for each option. This flexibility allows the interface to support most of the commercially available serial peripheral devices.

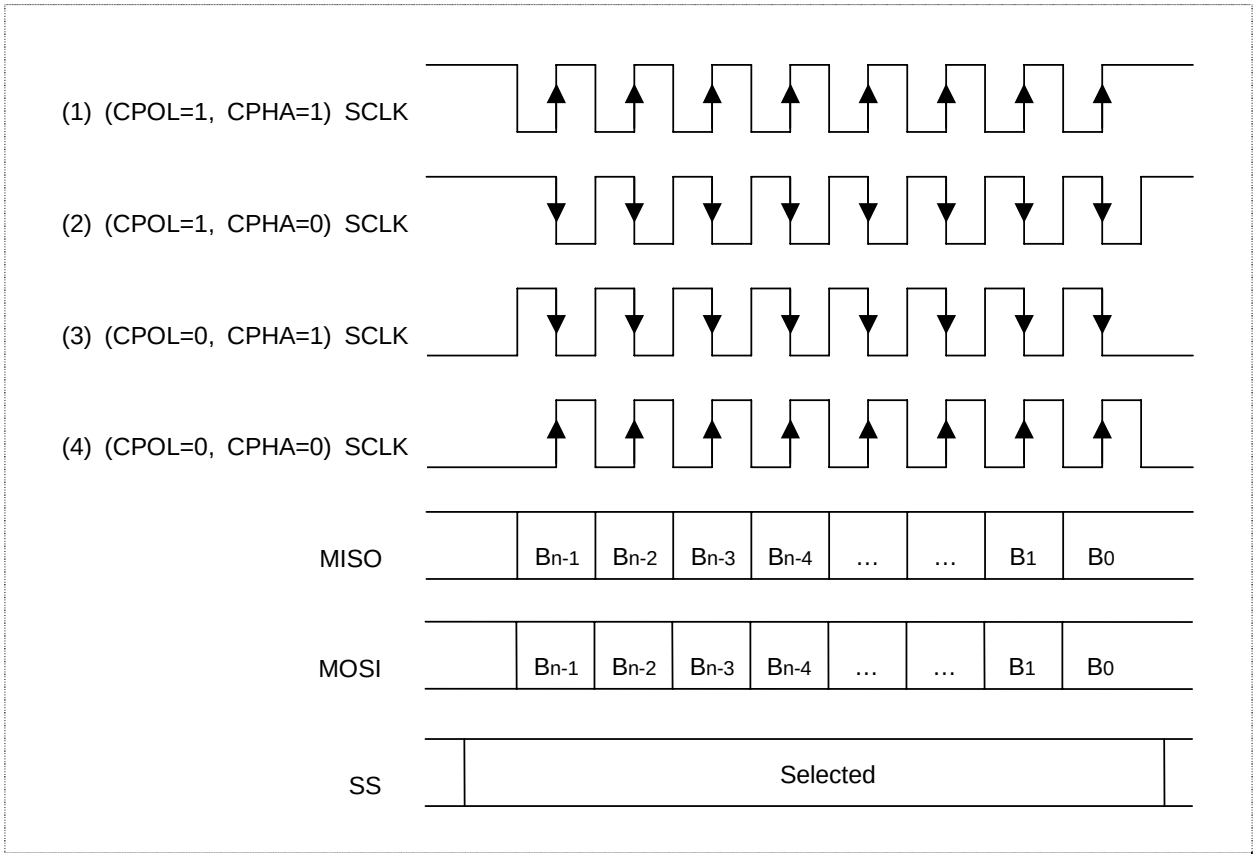


Figure 19.4 SPI Master Mode Clock Settings (where the number of bits of the transfer data is n)

Figure 19.5 illustrates SCLK clock waveform of SPI Slave mode.

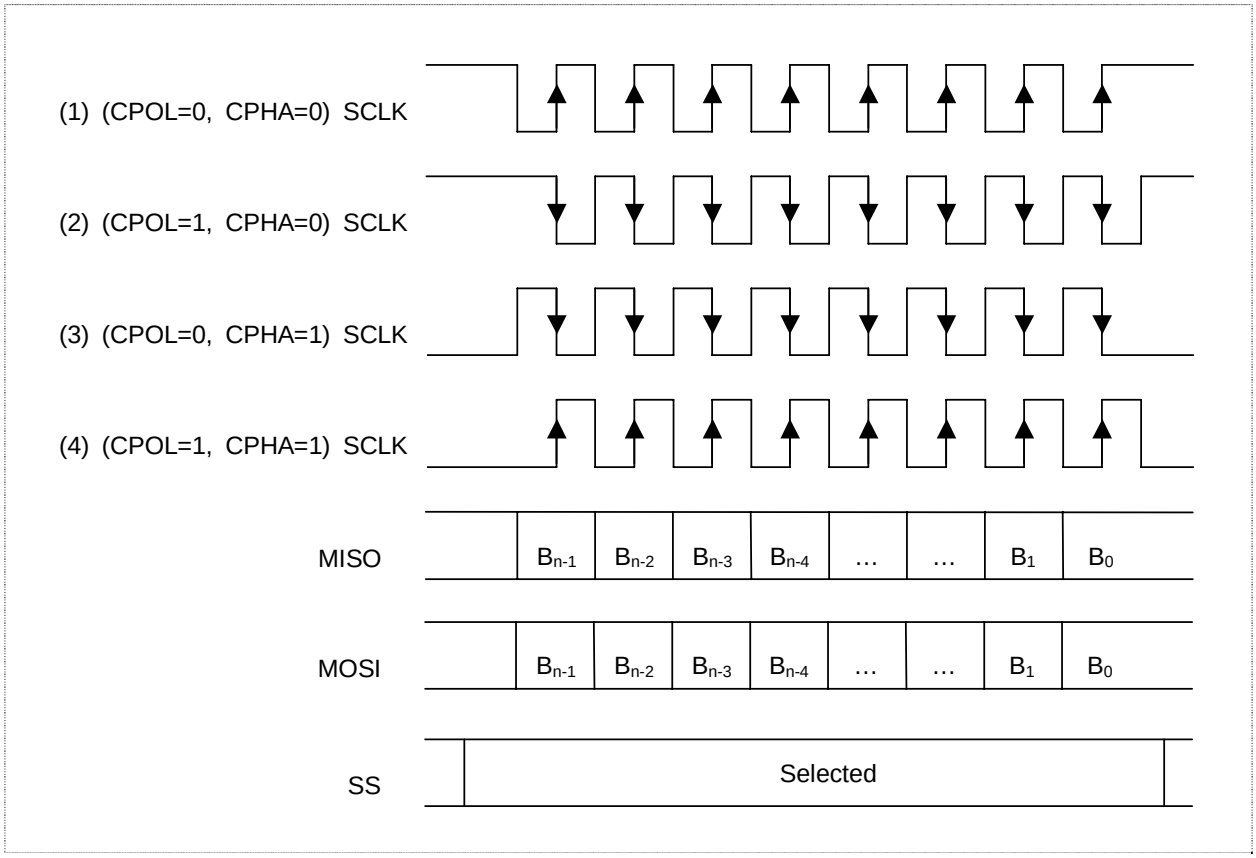


Figure 19.5 SPI Slave Mode Clock Settings (where the number of bits of the transfer data is n)

19.5 Description of Registers

19.5.1 List of Registers

The default base address where the SPI control registers are located is 0xFFFF_2000.
If not otherwise specified, the default value of any register bit that is not reserved is "0".

Table 19.1 List of SPI Registers (Base Address: 0xFFFF_2000)

Address Offset	Register Name	Default Value	R/W	Data Access Size
SPI Control Register				
0x00	SPI Receiving Data Register	0x0000_0000	RO	32
0x04	SPI Sending Data Register	0x0000_0000	R/W	32
0x08	SPI Control Register 1	0x0000_0000	R/W	32
0x0C	SPI Control Register 2	0x0000_0000	R/W	32
0x10	SPI Wait Register	0x0000_0000	R/W	32
0x14	SPI Status Register	0x0000_0010	RO	32
0x18	SPI Interrupt Control Register	0x0000_0000	R/W	32

19.5.2 Detailed Description of Registers

SPI Receiving Data Register

SPI[0x00] Default value = 0x0000_0000 Read Only

Receive Data [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Receive Data [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [31:0]: **Receive Data Bits [31:0]**

Data received from an external serial peripheral device can be read.

SPI Sending Data Register

SPI[0x04] Default value = 0x0000_0000 Read/Write

Transmit Data [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Transmit Data [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [31:0]: **Transmit Data Bits [31:0]**

This is a buffer to which transmit data is written. Data can be written when the TDEF bit (Bit 4 of the SPI status register) is set to "1", which indicate that this register is empty.

SPI Control Register 1

SPI[0x08] Default value = 0x0000_0000 Read/Write

n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
N/a	BPT [4:0]					CPHA	CPOL	n/a	MCBR [2:0]			CLKS	RX RAW	Mode	ENA
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [14:10]: **BPT[4:0] Number of transfer bits**

Specifies the bit length of the data transmitted/received in one transfer.

00000: 1 bit
00001: 2 bits
:
11110: 31 bits
11111: 32 bits

Bit 9: **CPHA Serial Clock Phase Select**

Selects the phase of the SCLK clock.

0: Generates a clock pulse in the last half of the data cycle (See Figure 20.4. (2)(4))
1: Generates a clock pulse in the first half of the data cycle (See Figure 20.4. (1)(3))

Bit 8: **CPOL Serial Clock Polarity Select**

Selects the polarity of the SCLK clock.

0: Active HIGH (Generates a HIGH pulse as clock) (See Figure 20.4. (3)(4))
1: Active LOW (Generates a LOW pulse as clock) (See Figure 20.4. (1)(2))

Bits [6:4]: **MCBR [2:0] Master Clock Bit Rate Select**

Sets the SCLK clock rate in master mode. Using the setting of this bit, the dividing ratio of the source clock (bus clock) is obtained from the following expression.

Dividing ratio = $4 * 2^{MCBR[2:0]}$

Therefore the SPI master clock is:

Master clock frequency (f_{SCLK}) = bus clock frequency/$(4 * 2^{MCBR[2:0]})$

Note: In slave mode, and in master mode as well, if you select a real time clock (32.768KHz) as the source clock (Bit 3 of this register is set to "1"), this bit is ignored.

Bit 3: **CLKS Source Clock Select**

Selects the source clock to generate SCLK clock in master mode.

0: Bus clock
1: Real time clock (32.768KHz)

Bit 2: **RXDATA RAW**

0: RXDATA is masked by the BPT width.
1: RXDATA is unmasked data of the shift register.

Bit 1: **Mode SPI Mode Select**

Selects whether to use this interface in master mode or in slave mode.

0: Slave Mode
1: Master Mode

Bit 0: **ENA SPI Enable**

Enables the transmit/receive circuits of the SPI.

0: Disable
1: Enable

SPI Control Register 2

SPI[0x0C] Default value = 0x0000_0000 Read/Write

n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a				SSA	SS	SSP	SSC	n/a					Reserved (0)		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit 11: **SSA Slave Select Pin (SS) Auto Control**

This bit sets the following when operating in master mode.

0: The SS pin is controlled by SS (Bit10) if the pin is set to output.

1: The SS pin is controlled by internal transfer timing if the pin is set to output.

This bit has no effect when operating in slave mode.

Bit 10: **SS Slave Select Pin (SS) Control**

Controls the output of the SS pin if the pin is set to output when operating in master mode.

0: The SS pin outputs inactive level.

1: The SS pin outputs active level.

If the SS pin is set as invalid input (SSC = 0) when operating in slave mode:

0: This SPI is not selected.

1: This SPI is selected.

In other cases, this bit has no effect.

Bit 9: **SSP Slave Select Pin (SS) Polarity Select**

0: Active LOW

1: Active HIGH

Bit 8: **SSC Slave Select Pin (SS) Setting**

Switches the input/output direction of the SS pin when operating in master mode.

0: Input (Mode violation detection)

1: Output (Slave select output)
HIGH/LOW output can be set by using the SS bit (Bit 10 of this register).
Mode violation cannot be detected.

In slave mode:

0: Sets the SS pin as invalid input. Selection in the SS bit (Bit 10) becomes effective.

1: Sets the SS pin as valid input.

The following table summaries the settings in Bits [10:8].

Table 19.2 Settings in the SS Pin

Mode selected *	Bit 8: SSC SS Setting	Bit 11: SSA SS Auto Select	Bit 9: SSP SS Polarity Select	Bit 10: SS SS Control	State of SS Pin (Active Level)
Master Mode	0: SS pin is for input (Mode violation detection)	No effect	0: Active LOW	No effect	SS input (LOW)
			1: Active HIGH		SS input (HIGH)
	1: SS pin is for output	0: Controlled by SS the bit	0: Active LOW	0: Inactive	SS output = HIGH (LOW)
				1: Active	SS output = LOW (LOW)
			1: Active HIGH	0: Inactive	SS output = LOW (HIGH)
				1: Active	SS output = HIGH (HIGH)
		1: Auto control	0: Active LOW	No effect	SS output = auto control (LOW)
			1: Active HIGH		SS output = auto control (HIGH)
Slave Mode	0: SS pin as invalid input	No effect	No effect	0: Not Selected	SS input (HIGH) <Not selected>
				1: Selected	SS input (HIGH) <Selected>
	1: SS pin as valid input		0: Active LOW	No effect	SS input (LOW)
			1: Active HIGH		SS input (HIGH)

*: You select a mode by using the Mode bit (Bit 1 of the SPI control register 1).

Bits [2:0]: **Reserved (0)**

SPI Wait Register

SPI[0x10] Default value = 0x0000_0000 Read/Write

n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WAIT Cycles [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [15:0]: **WAIT Cycles [15:0] WAIT Cycles**

Sets the wait time to insert between each data transmit/receive operation in the unit of SCLK clock. (Wait time = WAIT Cycles [15:0] × SCLK cycles)

0000h (w): 0 clock
0001h (w): 1 clock
0002h (w): 2 clocks
:
FFFFh (w): 65535 clocks

The setting of this bit is effective only in master mode.

SPI Status Register

SPI[0x14] Default value = 0x0000_0010 Read Only

n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a									BSYF	MFEF	TDEF	RDOF	RDFF	n/a	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit 6: **BSYF Transfer Busy Flag**

Indicates the SPI is performing a transmit/receive operation.

0: Standby

1: Transmission or reception is in progress.

This flag is automatically set when a transmission or reception starts. The set flag is automatically cleared when the transfer completes and the interface becomes standby.

This flag is effective only in master mode. In slave mode, it always remains "0".

Bit 5: **MFEF Mode Violation Flag**

Indicates that a mode violation error occurs.

0: No error exists

1: Error occurred

This flag is set if the SS pin is brought to active level by an external serial device when the SPI is in master mode. This flag is automatically cleared by canceling the error. To cancel the error, the SPI operates in slave mode while the flag and the MFIE bit (Bit 5 of the SPI interrupt control register) are set and disables all output without starting data transfer.

Bit 4: **TDEF Transmit Data Empty Flag**

Indicates that the sending data register is empty.

0: Transmit data exists

1: No transmit data exists (Default)

This flag is set when the data written to the sending data register is sent to a serial interface (or at reset). Owing to this function, the next transmit data can be written to the sending data register and the set flag is cleared by writing data to the sending data resister.

Bit 3: **RDOF Receive Data Overflow Flag**

Indicates that a receive data overflow occurs.

0: No overflow occurred

1: Overflow occurred

This flag is set when the next receive data is sent to the receive data register from a serial interface while the receive data full flag is set (the receive data is not read). The set flag is cleared by reading the receive data register.

Bit 2: **RDFF Receive Data Full Flag**

Indicates that there is receive data in the receive data register.

0: No receive data exists

1: Receive data exists

This flag is set when receive data is sent to the receive data register through the serial interface. The set flag is cleared by reading the receive data register.

Note: This register is also cleared entirely when the SPI Enable bit (Bit 0 of the SPI control register 1) is set to "0" to disable the SPI.

SPI Interrupt Control Register

SPI[0x18] Default value = 0x0000_0000 Read/Write

n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a										MFIE	TEIE	ROIE	RFIE	MIRQ	IRQE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit 5: **MFIE Mode Violation Interrupt Enable**

Enables (permits)/disables (prohibits) a mode violation interrupt.

0: Interrupt disable
1: Interrupt enable

This setting is effective when the SPI operates in master mode and the SS pin is configured for mode violation detection.

Bit 4: **TEIE Transmit Data Register Empty Interrupt Enable**

Enables/disables a transmit data register empty interrupt.

0: Interrupt disable
1: Interrupt enable

Bit 3: **ROIE Receive Data Overflow Error Interrupt Enable**

Enables/disables a receive data overflow error interrupt.

0: Interrupt disable
1: Interrupt enable

Bit 2: **RFIE Receive Data Register Full Interrupt Enable**

Enables/disables a receive data full interrupt.

0: Interrupt disable
1: Interrupt enable

Bit 1: **MIRQ Manual Interrupt Request Set/Clear**

Sets/Clears a manual interrupt request of the SPI.

0: Clears the interrupt request.
1: Sets the interrupt request.

This bit allows the software to generate an SPI interrupt. If IRQE (Bit 0) is set to "0 (interrupt is prohibited)", controls by this bit has no effect.

Bit 0: **IRQE Interrupt Request Enable**

Enables/disables an SPI interrupt request.

0: Interrupt request disable
1: Interrupt request enable

20. COMPACT FLASH (CF) CARD INTERFACE

20.1 Description

The CF card interface has the following features.
- CF card attribute memory space (2KB space)
- CF card common memory space (2KB space)
- CF card IO space (2KB space)
- Support of interrupt output (STSCHG#, IRQ)
- Command strobe timing output in various ranges of internal PCLK clocks (50 MHz to 6 MHz)
- Support of programmable idle cycle insertion and programmable command cycle insertion for CFIORD#,CFIOWR#
- Support of True IDE mode on CF interface (if CFOE# pull-down circuit and CSSEL signal are used, and Low Active Reset is externally supported)

Note: The S2S65A30 does not have the following signal lines due to the limited number of pins. They are internally fixed to logical LOW.
- **CD [2:1]#**
- **VS [2:1]#**
- **BVD2#**
- **WP/IOIS16#**

20.2 Block Diagram

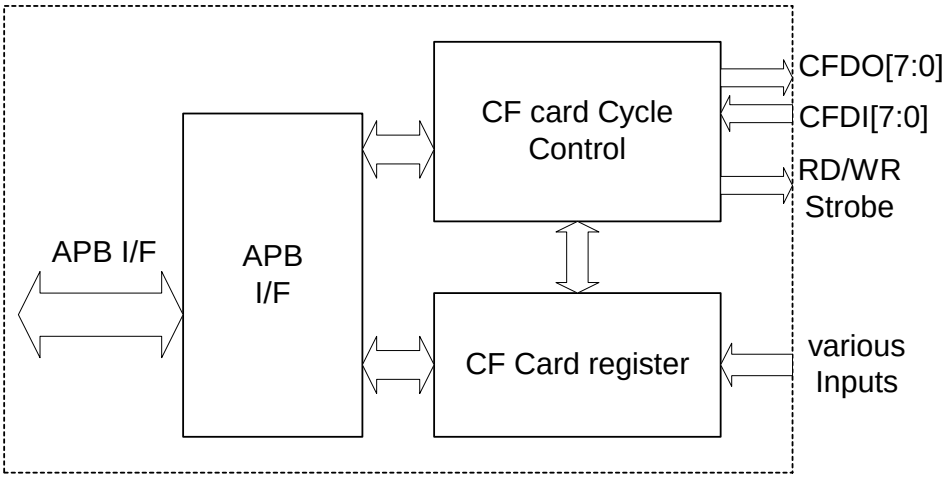


Figure 20.1 CF Card I/F Block Diagram

20.3 CF Card I/F Space Assignment

Table 20.1 CF Card I/F Space Assignment

Description	Address Range	Size
CF card attribute space	0xFFFE4000 - 0xFFFE47FF	2KB
CF card common space	0xFFFE4800 - 0xFFFE4FFF	2KB
CF card I/O space	0xFFFE5000 - 0xFFFE57FF	2KB
CF card true IDE CS1# space	0xFFFE5800 - 0xFFFE5BFF	1KB
CF card true IDE CS2# space	0xFFFE5C00 - 0xFFFE5FFF	1KB
CF card interface setting	0xFFFE6000 - 0xFFFE6FFF	4KB

Caution: Either 8-bit or 16-bit data of each CF card space must be accessed. An access to 32-bit data of the card causes an abnormal operation.
The 16- or 32-bit data access must be used for the register access during CF card interface setting.

To allow true IDE access:

The True IDE access via the CF I/F of the S2S65A30 is not realized by access to the specified space only. The signals must be operated at the system level (on the board).
Actually, the following two signals must be used correctly.

- OE# (Alias: ATASEL)
- CSSEL

Specify the OE# signal of CF Card I/F to be sampled as logical Low at Power-On Reset time (the power must be switched from OFF to ON state).
Furthermore, be sure to set the CSSEL signal to Pull Up or Pull Down status or to the Open status when determining if the IDE device operates as the master or a slave unit.

During True IDE access, the CS1# and CS2# spaces have the following addresses.

- The accessible registers of CS1# are the address space having low-order 3 bits of 0x0 to 0x7 shown on the above table.
- The accessible registers of CS2# are the address space having low-order 3 bits of 0x6 to 0x7 shown on the above table.

For example, the Alternate Status register has been assigned the address space having low-order 3 bits of 0x7 within the CS2# space.

20.4 External Pins

The following defines the external pins of the CF card interface.

Table 20.2 External Pins (CF)

Pin Name	Input/Output	Pin Functions	Multiplex Pin/Remarks
CFCE2#	Output	CF card enable 2 (CE2#) output	GPIOH0*
CFCE1#	Output	CF card enable 1 (CE1#) output	GPIOH1*
CFIORD#	Output	CF I/O read strobe output	GPIOH2*
CFIOWR#	Output	CF I/O write strobe output	GPIOH3*
CFWAIT#	Input	Wait request input from CF card	GPIOH4*
CFRST	Output	Reset output to CF card	GPIOH5* or GPIOC2*
CFIRQ	Input	Interrupt request input from CF card	GPIOH6*
CFSTSCHG#	Input	Status change input from CF card	GPIOH7*
CFDEN#	Output	CF card external buffering data enable output	GPIOI0*
CFDDIR	Output	CF data bus direction indication output	GPIOI1*
CFREG#	Output	CF attribute space and I/O space selection REG signal	MA11**
CFADDR [10:0]	Output	CF address signal	MA [10:0]**
CFDATA [15:0]	Input/Output	16-bit CF data signal	MD [15:0]**
CFOE#	Output	CF interface memory and attribute space output enable signal	MOE#**
CFWE#	Output	CF interface memory and attribute space write enable signal	MWE0#**

* As the CF external pin is multiplexed with the GPIO pin, this function can be used if “Function 1 other than GPIO” is set using the GPIO Pin Function register.

** When the CF is operating, the memory controller pin functions as the CF external pin.

20.5 Registers

20.5.1 List of Registers

The CF card interface registers have base address 0xFFFE_6000.

Table 20.3 Register List **(Base address 0xFFFE_6000)**

Address Offset	Register Name	Abbreviation Name	Default Value	R/W	Data Access Size
0x00	CF Card Interface Control Register	CFCTL	0x1000	(R/W)	16 (/32)
0x04	CF Card Pin Status Register	CFPINSTS	0x0XXX	RO	16 (/32)
0x08	CF Card IRQ Source & Clear Register	CFINTRSTS	0x0XXX	R/W	16 (/32)
0x0C	CF Card IRQ Enable Register	CFINTMSTS	0x0000	R/W	16 (/32)
0x10	CF Card IRQ Status Register	CFINTSTS	0x0000	RO	16 (/32)
0x14	CF Card MISC Register	CFMISC	0x0000	R/W	16 (/32)

20.5.2 Detailed Description of Registers

CF Card Interface Control Register (CFCTL)

CF[0x00] Default value = 0x1000 (Read/Write)

PROG CYCEN	PROG IDLE [2:0]			PROG CYC [3:0]			
			R/W				
15	14	13	12	11	10	9	8
Reserved (0)	IOIS8_IO	IOIS8_MEM	PROG IDLE EN	CFRST	CFCARDEN	PCKMD[1:0]	
RO				R/W			
7	6	5	4	3	2	1	0

Bit 15: **PROG_CYCEN**

Enables the programmable command cycle function for CFIORD#/CFIOWR# signals.
Usually, it must be disabled.

0: Disable (After RESET/ Default)
1: Enable

Bits [14:12]: **PROG_IDLE[2:0]**

Set the idle cycle count of CF card interface. (Default is logical 1.)

Bits [11:8]: **PROG_CYC[3:0]**

Set the command active cycle count of CFIORD#/CFIOWR# signals.
Valid if PROG_CYCEN=1 only.

Bit 7: **Reserved**

Bit 6: **IOIS8_IO**

Sets the device size of CF card I/O space.

0: Allows operating as a 16-bit CF card device.
1: Allows operating as an 8-bit CF card device.

Bit 5: **IOIS8_MEM**

Sets the device size of CF card common memory space.

0: Allows operating as a 16-bit CF card device.
1: Allows operating as an 8-bit CF card device.

Bit 4: **PROG_IDLE_EN**

Enables the programmable command cycle function for CFIORD#/CFIOWR# signals until commands from CFCE1# • CFCE2# are made active. Usually, it must be disabled.

0: Disable
1: Enable

Bit 3: **CFRST**

Allows the direct control of CFRST pin if the CF I/F function is selected.

0: Sets the CFRST pin to Low.
1: Sets the CFRST pin to High.

Bit 2: **CFCARDEN**

0: Disables the CF card interface.
1: Enables the CF card interface.

Bits [1:0]: **PCKMD[1:0]**

Allows the value change so that the CF card I/F operates according to the clock frequency.

00: Use this value if the PCLK is approximately 50 MHz (-25 MHz).
01: Use this value if the PCLK is approximately 24 MHz.
10: Use this value if the PCLK is approximately 12 MHz.
11: Use this value if the PCLK is approximately 6 MHz.

CF Card Pin Status Register (CFPINSTS)

CF[0x04] Default value = 0x0XXX Read Only

15	14	13	12	11	10	9	8
0							IREQ#2
WP	IREQ#1	BVD2#	BVD1#/ STSCHG	VS2#	VS1#	CD2#	CD1#
7	6	5	4	3	2	1	0

The pin status value (except for bits 1 and 0) is reflected on each bit.
Bits [1:0] (CD2#, CD1#) The pin status after signal noise filtering is indicated.

Bit 8: **IREQ#2 input**

This bit reference is useful for interrupt input if the IREQ# pin is active high.
This bit indicates the IREQ# pin status of CF card interface.

Bit 7: **WP pin input**

Indicates the WP pin status of CF card interface.

Bit 6: **RDY/BSY, IREQ pin input (The name changes depending on the mode selected for the CF card.)**

This bit reference is useful for interrupt input if the IREQ# pin is active low.
The inverted input status of RDY/BSY or IREQ pin of CF card interface can be checked.

Bit 5: **BVD2# pin input**

Indicates the BVD2# pin status of CF card interface.

Bit 4: **BVD1#/STSCHG# pin input**

Indicates the BVD1#/STSCHG# pin status of CF card interface.

Bit 3: **VS2# pin input**

Indicates the VS2# pin status of CF card interface.

Bit 2: **VS1# pin input**
Indicates the VS2# pin status of CF card interface.

Bit 1: **CD2# pin input**
Indicates the CD2# pin status of CF card interface after noise filtering.

Bit 0: **CD1# pin input**
Indicates the CD1# pin status of CF card interface after noise filtering.

Note: Bits 7, 5, and 3 to 0 are not supported by the S2S65A30.

CF Card IRQ Source & Clear Register (CFINTRSTS)
CF[0x08] Default value = 0x0XXX Read/Write

Reserved							IRQ#2
15	14	13	12	11	10	9	8
Reserved	IRQ#1	Reserved	BVD1/ STSCHG	Reserved		CD2	CD1
7	6	5	4	3	2	1	0

This register is used to indicate the interrupt request source (not masked), and if value 1 is written in it, the respective bit is cleared.

Bits [15:7]: **Reserved bits**
Zeros (0s) are read. Zeros (0s) must be entered during writing.

Bit 8: **IRQ#2 input**
This bit reference is useful for interrupt input if the CFIRQ pin is active high.
After the CF card has been programmed to the I/O mode, if this bit is logical 1, it indicates an occurrence of CFIRQ interrupt request. If this bit is logical 0, no interrupt request has occurred at the CFIRQ pin.

Bit 6: **IRQ#1 (Inverting input)**
This bit reference is useful for interrupt input if the CFIRQ pin is active low.
After the CF card has been programmed to the I/O mode, if this bit is logical 1, it indicates an occurrence of CFIRQ interrupt request. If this bit is logical 0, no interrupt request has occurred at the CFIRQ pin.

Bit 4: **BVD1/STSCHG#**
After the CF card has been programmed to the I/O mode, if this bit is logical 0, it indicates that STSCHG# is logical 0, that is, the RDY/BSY# or WP signal status has been changed. If this bit is logical 1, the RDY/BSY# or WP signal status has not changed.

Bit 1: **CD2 pin status change**
If this signal (after noise filtering) status changes from Low to High or from High to Low, it is set to logical 1. This is one of interrupt signal sources, and the signal is cleared if this bit is set to 1.

Bit 0: **CD1 pin status change**
If this signal (after noise filtering) status changes from Low to High or from High to Low, it is set to logical 1. This is one of interrupt signal sources, and the signal is cleared if this bit is set to 1.

Note: Bits 1 and 0 are not supported by the S2S65A30.

CF Card IRQ Enable Register (CFINTMSTS)

CF[0x0C] Default value = 0x0000 Read/Write

Reserved							IRQEN#EN2
15	14	13	12	11	10	9	8
Reserved	IREQ#EN1	Reserved	BVD1EN/ STSCHGEN	Reserved		CD2EN	CD1EN
7	6	5	4	3	2	1	0

Each bit corresponds to the respective bit of CF Card IRQ Source & Clear register.
Each bit is set as follows.

0: Masks an interrupt.
1: Unmasks (or enables) an interrupt.

Note: Bits 1 and 0 are not supported by the S2S65A30.

CF Card IRQ Status Register (CFINTSTS)

CF[0x10] Default value = 0x0000 Read Only

Reserved							IREQ#2
15	14	13	12	11	10	9	8
Reserved	IREQ#1	Reserved	BVD1/ STSCHG	Reserved		CD2	CD1
7	6	5	4	3	2	1	0

The respective bits of the IRQ Source register and IRQ Enable register are ANDed and set in this register.

0: No interrupt has occurred, or the interrupt is masked.
1: The interrupt is enabled and an interrupt cause already exists.

Note: Bits 1 and 0 are not supported by the S2S65A30.

CF Card MISC Register (CFMISC)

CF[0x14] Default value = 0x0000 Read/Write

Reserved							
15	14	13	12	11	10	9	8
Reserved							CSRDEN
7	6	5	4	3	2	1	0

This register is reserved for the certain hardware. Do not write any value in usual application.

Bits [15:2]: **Reserved bits**

Bit 0: **CSRDEN**

Activates both CFCE1# and CFCE2# or not during reading.

0: Normal operation
1: Activates both CFCE1# and CFCE2# during reading.

20.6 Application Restrictions of CF Card Interface

This device does not have the following pins due to the limited number of mount pins, and those pin signals are internally fixed to Low. Therefore, the application of some registers is restricted.

- CD [2:1]#
- VS [2:1]#
- BVD2#
- WP/IOIS16#

The following lists the registers that are restricted to use for this device.

Offset address	Register bit name	Restrictions
CF[0x04] Bit 7	WP pin input	Unavailable
CF[0x04] Bit 5	BVD2# pin input	Unavailable
CF[0x04] Bit 3	VS2# pin input	Unavailable
CF[0x04] Bit 2	VS1# pin input	Unavailable
CF[0x04] Bit 1	CD2# pin input	Unavailable
CF[0x04] Bit 0	CD1# pin input	Unavailable
CF[0x08] Bit 1	CD2 pin status change	Unavailable
CF[0x08] Bit 0	CD1 pin status change	Unavailable
CF[0x0C] Bit 1	CD2EN	Unavailable
CF[0x0C] Bit 0	CD1EN	Unavailable
CF[0x10] Bit 1	CD2	Unavailable
CF[0x10] Bit 0	CD1	Unavailable

21. SD MEMORY CARD INTERFACE

21.1 Description

The SD memory card interface conforms the SD Memory Card Physical Layer Specification Version 2.00.
For details, see S2S65A30 SDMMC Interface.

22. TIMER A (TIMA)

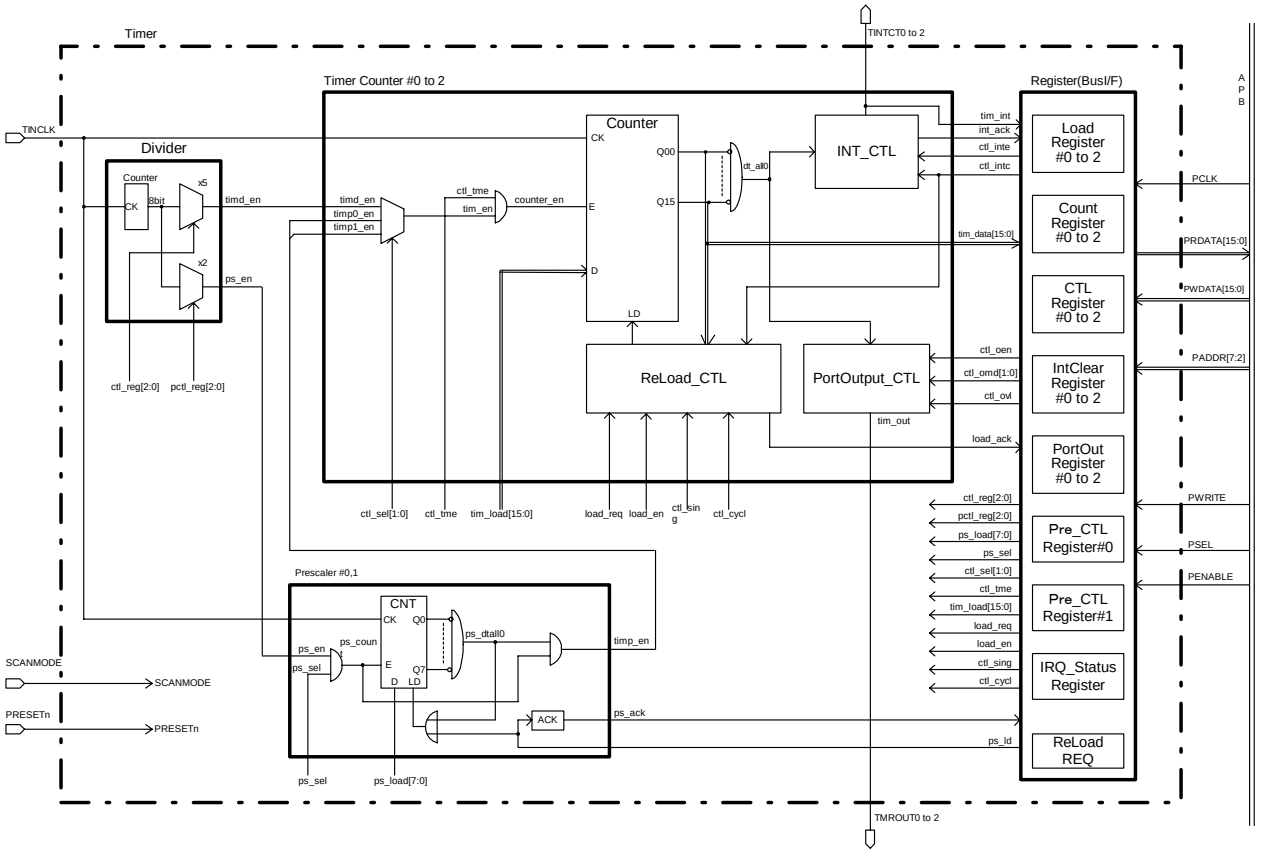
22.1 Description

Timer A has the following features.

- Built-in 3-channel, 16-bit down count timer (The 3-channel timers have the same structure.)
- Supports two types of timer mode (Cyclic mode and Single mode).
- Generates an interrupt with unmasked IRQ each time the timer count reaches zero (0).
- Built-in 8-bit counter for signal dividing (from 1/1 to 1/256)
- Allows setting any counting of clocks (divided by the divider) using the 8-bit counter for 2-channel prescaler.
- Timer output mode functions during signal underflow (3 types):
  Underflow signal, any value-0 or 1 output, and underflow frequency toggle output

22.2 Block Diagram

The following shows a block diagram of Timer A. The timer block consists of the Register block (Register (Bus I/F)), Divider block (Divider), 2-channel Prescaler block (Prescaler #0, 1), and 3-channel Timer Counter block (Timer Counter #0 to 2).
As every prescaler and timer counter channels are the same, the typical structure of channel 0 is only shown in the following block diagram. All channels are controlled by the divider and registers. The clock for timer counter (TINCLK) is supplied by the system controller, and the PCLK clock divided by 8 (the 1/8 PCLK) is used. For details, see the System Controller section.



＜16bit TIMER BLOCK＞

Figure 22.1 Block Diagram

22.3 External Pins

The following defines the external pins for Timer A.

Pin Name	Input/Output	Pin Functions	Multiplex Pin*/Remarks
TimerA0out	Output	Timer A0 output	GPIOB4/INT4 (*)
TimerA1out	Output	Timer A1 output	GPIOB4/INT5 (*)
TimerA2out	Output	Timer A2 output	GPIOB5/INT6 (*)

* As timer-A external pins are multiplexed with GPIO and other pins, this function can be used if “Function 1 other than GPIO” is set using the GPIO Pin Function register.

22.4 Registers

22.4.1 List of Registers

These registers have base address 0xFFFF_B000.

Table 22.1 List of Registers (Base Address: 0xFFFF_B000)

Address Offset	Register Name	Register Abbreviation	Default Value	R/W	Data Access Size
0x00	Timer A0 Load register	TMA0LD	0x0000	R/W	16 (/32) *1
0x04	Timer A0 Count register	TMA0CNT	0x0000	RO	16 (/32) *1
0x08	Timer A0 Control register	TMA0CTRL	0x0000	(R/W)	16 (/32) *1
0x0C	Timer A0 IRQ Flag Clear register	TMA0IRQ	—	WO	8 (/16/32) *2
0x10	Timer A0 Port Output Control register	TMA0POUT	0x0000	(R/W)	8 (/16/32) *2
0x20	Timer A1 Load register	TMA1LD	0x0000	R/W	16 (/32) *1
0x24	Timer A1 Count register	TMA1CNT	0x0000	RO	16 (/32) *1
0x28	Timer A1 Control register	TMA1CTRL	0x0000	(R/W)	16 (/32) *1
0x2C	Timer A1 IRQ Flag Clear register	TMA1IRQ	—	WO	8 (/16/32) *2
0x30	Timer A1 Port Output Control register	TMA1POUT	0x0000	(R/W)	8 (/16/32) *2
0x40	Timer A2 Load register	TMA2LD	0x0000	R/W	16 (/32) *1
0x44	Timer A2 Count register	TMA2CNT	0x0000	RO	16 (/32) *1
0x48	Timer A2 Control register	TMA2CTRL	0x0000	(R/W)	16 (/32) *1
0x4C	Timer A2 IRQ Flag Clear register	TMA2IRQ	—	WO	8 (/16/32) *2
0x50	Timer A2 Port Output Control register	TMA2POUT	0x0000	(R/W)	8 (/16/32) *2
0x60-0x9C	Reserved	—	—	—	—
0xA0	Prescaler 0 Control register	PS0CTRL	0x0000	(R/W)	16 (/32) *1
0xA4	Prescaler 1 Control register	PS1CTRL	0x0000	(R/W)	16 (/32) *1
0xB0	Timer A IRQ Status register	TMAIRQSTS	0x0000	RO	8 (/16/32) *2

*1: Access to 16-bit or 32-bit data is enabled.
*2: Access to various size of data (8, 16 and 32-bit data) is enabled.

22.4.2 Detailed Description of Registers

Timer A0 Load Register (TMA0LD)

TIM[0x00] Default value = 0x0000 Read/Write

Timer A0 load value [15:8]							
15	14	13	12	11	10	9	8
Timer A0 load value [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **TMA0LD [15:0] Timer A0 load value bits [15:0]**

This register sets the (16-bit) initial count to be loaded in timer A0.

Timer A0 Count Register (TMA0CNT)

TIM[0x04] Default value = 0x0000 Read only

Timer A0 current count [15:8]							
15	14	13	12	11	10	9	8
Timer A0 current count [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **TMA0CNT [15:0] Timer A0 current count bits [15:0]**

The current count of timer A0 can be read.

Timer A0 Control Register (TMA0CTRL)

TIM[0x08] Default value = 0x0000 (Read/Write)

n/a RO						Divider/Prescaler [1:0] R/W	
15	14	13	12	11	10	9	8
Timer A0 enable R/W	n/a RO	Mode selection R/W	Divider dividing ratio [2:0] R/W			Immediate load request R/W	IRQ request R/W
7	6	5	4	3	2	1	0

Bits [9:8]: **Divider/prescaler selection [1:0]**

Sets the dividing source of the clock to be used for timer A0.

- 0x: Divider
- 10: Prescaler #0
- 11: Prescaler #1

Bit 7: **Timer A0 enable**

When this bit is enabled, the countdown starts in the mode being set by the mode selection bit of this register.

- 0: Disable timer A0.
- 1: Enables timer A0 (in Cyclic mode or Single mode).

Bit 5: **Selects a mode.**

- 0: Cyclic mode
- 1: Single mode

Bits [4:2]: **Divider dividing ratio [2:0]**

000: Do not divide. →1/1
001: Divide by 4. →1/4
010: Divide by 8. →1/8
011: Divide by 16. →1/16
100: Divide by 32. →1/32
101: Divide by 64. →1/64
110: Divide by 128. →1/128
111: Divide by 256. →1/256

Bit 1: **Immediate load request (in Cyclic mode)**

Requests for a reload timing of the load value of timer A0 in the Cyclic mode.

0: Reloads the written load value when the counter reaches "0x0000".
1: Reloads the load value immediately when it is written in the register.

Note: In the Single mode, however, the load value is reflected immediately when it is written regardless of this bit setting.

Bit 0: **Timer A0 interrupt request enable**

0: Disables an interrupt request (IRQ mask).
1: Enables an interrupt request.

Timer A0 IRQ Flag Clear Register (TMA0IRQ)

TIM[0x0C] Default value = — Write Only

15	14	13	12	11	10	9	8
Any data							
7	6	5	4	3	2	1	0
Any data							

This register is a write-only port to clear the interrupt request (IRQ) of timer A0. The IRQ flag is cleared if any data is written in this register.

Timer A0 Port Output Control Register (TMA0POUT)

TIM[0x10] Default value = 0x0000 (Read/Write)

15	14	13	12	11	10	9	8
n/a RO							
7	6	5	4	3	2	1	0
n/a RO				Output mode select R/W		Output enable R/W	Output value R/W

Bits [3:2]: **Output mode select**

00: Outputs a value (bit 0) during underflow.
01: Underflow output
10: Toggle output in each occurrence of underflow
11: Reserved

Bit 1: **Output enable**

0: Disables the output mode.
1: Enables the output mode.
If the corresponding port has been set as GPIO port and if this bit is set to 1, the port operates in the output mode selected by bits [3:2].

Bit 0: **Output value**

If the output mode (Bits [3:2]) is "00", this bit value is output.

Timer A1 Load Register (TMA1LD)

TIM[0x20] Default value = 0x0000 Read/Write

Timer A1 load value [15:8]							
15	14	13	12	11	10	9	8
Timer A1 load value [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **TMA1LD [15:0] Timer A1 load value bits [15:0]**

This register sets the (16-bit) initial count to be loaded in timer A1.

Timer A1 Count Register (TMA1CNT)

TIM[0x24] Default value = 0x0000 Read Only

Timer A1 current count [15:8]							
15	14	13	12	11	10	9	8
Timer A1 current count [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **TMA1CNT [15:0] Timer A1 current count bits [15:0]**

The current count of timer A1 can be read.

Timer A1 Control Register (TMA1CTRL)

TIM[0x28] Default value = 0x0000 (Read/Write)

n/a RO						Divider/Prescaler [1:0 R/W	
15	14	13	12	11	10	9	8
Timer A1 enable R/W	n/a RO	Mode select R/W	Divider dividing ratio [2:0] R/W			Immediate load request R/W	IRQ request R/W
7	6	5	4	3	2	1	0

Bits [9:8]: **Divider/prescaler selection [1:0]**

Sets the dividing source of the clock to be used for timer A1.

0x: Divider
10: Prescaler #0
11: Prescaler #1

Bit 7: **Timer A1 enable**

When this bit is enabled, the countdown starts in the mode being set by the mode selection bit of this register.

0: Disables timer A1.
1: Enables timer A1 (in Cyclic mode or Single mode).

Bit 5: **Mode select**

0: Cyclic mode
1: Single mode

Bits [4:2]: **Divider dividing ratio [2:0]**

000: Do not divide. →1/1
001: Divide by 4. →1/4
010: Divide by 8. →1/8
011: Divide by 16. →1/16
100: Divide by 32. →1/32
101: Divide by 64. →1/64
110: Divide by 128. →1/128
111: Divide by 256. →1/256

Bit 1: **Immediate load request (in Cyclic mode)**

Sets a reload timing of the load value of timer A1 in the Cyclic mode.

0: Reloads the written load value when the counter reaches "0x0000".
1: Reloads the load value immediately when it is written in the register.

Caution: In the Single mode, however, the load value is reloaded immediately when it is written regardless of this bit value.

Bit 0: **Timer A1 interrupt request enable**

0: Disables an interrupt request (IRQ mask).
1: Enables an interrupt request.

Timer A1 IRQ Flag Clear Register (TMA1IRQ)

TIM[0x2C] Default value = —

Write Only

15	14	13	12	11	10	9	8
Any data							
7	6	5	4	3	2	1	0
Any data							

This register is a write-only port to clear the interrupt request (IRQ) of timer A1. The IRQ flag is cleared if any data is written in this register.

Timer A1 Port Output Control Register (TMA1POUT)

TIM[0x30] Default value = 0x0000

(Read/Write)

15	14	13	12	11	10	9	8
				n/a RO			
7	6	5	4	3	2	1	0
n/a RO				Output mode select R/W		Output enable R/W	Output value R/W

Bits [3:2]: **Output mode select**

00: Outputs a value (bit 0) during underflow.
01: Underflow output
10: Toggle output in each occurrence of underflow
11: Reserved

Bit 1: **Output enable**

0: Disables the output mode.
1: Enables the output mode.
If the corresponding port has been set as GPIO port and if this bit is set to 1, the port operates in the output mode selected by bits [3:2].

Bit 0: **Output value**

If the output mode (Bits [3:2]) is "00", this bit value is output.

Timer A2 Load Register (TMA2LD)

TIM[0x40] Default value = 0x0000 Read/Write

Timer A2 load value [15:8]							
15	14	13	12	11	10	9	8
Timer A2 load value [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **TMA2LD [15:0] Timer A2 load value bits [15:0]**

This register sets the (16-bit) initial count to be loaded in timer A2.

Timer A2 Count Register (TMA2CNT)

TIM[0x44] Default value = 0x0000 Read only

Timer A2 current count [15:8]							
15	14	13	12	11	10	9	8
Timer A2 current count [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **TMA2CNT [15:0] Timer A2 current count bits [15:0]**

The current count of timer A2 can be read.

Timer A2 Control Register (TMA2CTRL)

TIM[0x48] Default value = 0x0000 (Read/Write)

n/a RO						Divider/Prescaler [1:0] R/W	
15	14	13	12	11	10	9	8
Timer A2 enable R/W	n/a RO	Mode select R/W	Divider dividing ratio [2:0] R/W			Immediate load request R/W	IRQ request R/W
7	6	5	4	3	2	1	0

Bits [9:8]: **Divider/prescaler selection [1:0]**

Sets the dividing source of the clock to be used for timer A2.

- 0x: Divider
- 10: Prescaler #0
- 11: Prescaler #1

Bit 7: **Timer A2 enable**

When this bit is enabled, the countdown starts in the mode being set by the mode selection bit of this register.

- 0: Disables timer A2.
- 1: Enables timer A2 (in Cyclic mode or Single mode).

Bit 5: **Mode select**

- 0: Cyclic mode
- 1: Single mode

Bits [4:2]: **Divider dividing ratio [2:0]**

000 : Do not divide. →1/1
001 : Divide by 4. →1/4
010 : Divide by 8. →1/8
011 : Divide by 16. →1/16
100 : Divide by 32. →1/32
101 : Divide by 64. →1/64
110 : Divide by 128. →1/128
111 : Divide by 256. →1/256

Bit 1: **Immediate load request (in Cyclic mode)**

Sets a reload timing of the load value of timer A2 in the Cyclic mode.

0: Reloads the written load value when the counter reaches "0x0000".
1: Reloads the load value immediately when it is written in the register.

Caution: In the Single mode, however, the load value is reflected immediately when it is written regardless of this bit setting.

Bit 0: **Timer A2 interrupt request enable**

0: Disables an interrupt request (IRQ mask).
1: Enables an interrupt request.

Timer A2 IRQ Flag Clear Register (TMA2IRQ)

TIM[0x4C] Default value = — Write Only

15	14	13	12	11	10	9	8
Any data							
7	6	5	4	3	2	1	0
Any data							

This register is a write-only port to clear the interrupt request (IRQ) of timer A2. The IRQ flag is cleared if any data is written in this register.

Timer A2 Port Output Control Register (TMA2POUT)

TIM[0x50] Default value = 0x0000 (Read/Write)

15	14	13	12	11	10	9	8
n/a RO							
7	6	5	4	3	2	1	0
n/a RO				Output mode select R/W		Output enable R/W	Output value R/W

Bits [3:2]: **Output mode select**

00: Enables an output (bit 0) during underflow.
01: Underflow output
10: Toggle output in each occurrence of underflow
11: Reserved

Bit 1: **Output enable**

0: Disables the output mode.
1: Enables the output mode.
If the corresponding port has been set as GPIO port and if this bit is set to 1, the port operates in the output mode selected by bits [3:2].

Bit 0: **Output value**

This bit value is output if the output mode (bits 3 and 2) are set to "00".

Prescaler 0 Control Register (PS0CTRL)

TIM[0xA0] Default value = 0x0000 (Read/Write)

Divider dividing ratio [2:0]			n/a				
R/W			RO				
15	14	13	12	11	10	9	8
Prescaler 0 load value [7:0]							
R/W							
7	6	5	4	3	2	1	0

Bits [15:13]: **Divider dividing ratio [2:0]**

000: Do not divide. →1/1
001: Divide by 4. →1/4
010: Divide by 8. →1/8
011: Divide by 16. →1/16
100: Divide by 32. →1/32
101: Divide by 64. →1/64
110: Divide by 128. →1/128
111: Divide by 256. →1/256

Bits [7:0]: **Prescaler 0 load value bits [7:0]**

This register sets the count of the clock divided by the divider in prescaler 0.

Prescaler 1 Control Register (PS1CTRL)

TIM[0xA4] Default value = 0x0000 (Read/Write)

Divider dividing ratio			n/a				
R/W			RO				
15	14	13	12	11	10	9	8
Prescaler 1 load value [7:0]							
R/W							
7	6	5	4	3	2	1	0

Bits [15:13]: **Divider dividing ratio [2:0]**

000: Do not divide. →1/1
001: Divide by 4. →1/4
010: Divide by 8. →1/8
011: Divide by 16. →1/16
100: Divide by 32. →1/32
101: Divide by 64. →1/64
110: Divide by 128. →1/128
111: Divide by 256. →1/256

Bits [7:0]: **Prescaler 1 load value bits [7:0]**

This register sets a value to count the clock divided by the divider in prescaler 1.

Timer-A IRQ Status Register (TMAIRQSTS)

TIM[0xB0] Default value = 0x0000 Read Only

n/a							
15	14	5	4	3	2	1	0
n/a			Reserved		Timer2 IRQ	Timer1 IRQ	Timer0 IRQ
7	6	5	4	3	2	1	0

Bits [4:3]: **Reserved**

Bit 2: **Timer A2 IRQ status**

Indicates the interrupt status of timer A2.

0: No interrupt request was issued (or IRQ masked).

1: An interrupt request was issued.

This interrupt status is cleared by the timer-A2 IRQ flag clear register.

Bit 1: **Timer A1 IRQ status**

Indicates the interrupt status of timer A1.

0: No interrupt request was issued (or IRQ masked).

1: An interrupt request was issued.

This interrupt status is cleared by the timer-A1 IRQ Flag Clear register.

Bit 0: **Timer A0 IRQ status**

Indicates the interrupt status of timer A0.

0: No interrupt request was issued (or IRQ masked).

1: An interrupt request was issued.

This interrupt status is cleared by the timer-A0 IRQ Flag Clear register.

22.5 Setting the Load Value in Each Mode

22.5.1 Timer Counter Modes

Each of 3-channel timers can be operated in any of the following two modes.
This section explains how to set the load value in each mode.

(1) Cyclic mode
The load value being set by the Load register is counted down to value 0.
The value is loaded in the following two types of timing.

a) If an immediate load request is issued
If bit 1 (Immediate Load Request bit) of Timer-A Control register is set to logical 1, the load value is reflected on the counter immediately.
To do so, set the Immediate Load Request bit to 1 when you wish to reflect, and set the load value that you wish to reflect using the Load register. The load value is forcibly written in the counter regardless of the bit 7 (Timer-A Enable bit) status of Timer-A Control register.

b) If an immediate load request is NOT issued
If bit 1 (Immediate Load Request bit) of Timer-A Control register is set to logical 0, an interrupt is generated when all bits of the down counter are set to 0. At this time, the value being set in the Load register is reloaded and the countdown starts.
To use it in the free-running mode, set value FFFFh as the load value.

(2) Single mode
The load value being set by the Load register is counted down. When all counter outputs reach value 0, an interrupt is generated and the countdown is stopped. The counter continues to stop even if the interrupt is cleared by the IRQ Flag Clear register.

When a load value is set by the Load register, it is reloaded and reflected immediately on the counter regardless of the bit 1 (Immediate Load Request bit) value of Timer-A Control register. The load value can be written forcibly in the counter regardless of the bit 7 (Timer-A Enable bit) status of Timer-A Control register.

22.6 Timer Internal Clock Setting Examples (1 KHz, 1 MHz)

22.6.1 Divider and Prescaler Settings

You can set the dividing ratio and the count value for three channel timers using their dividers and 2-channel prescalers. The timers can be counted down in any of two cycles.
If you operate the timer with the dividing ratio of the diver without using the prescaler, you can set the dividing ratio for each of three channel timers.
The APB bus clock (PCLK) divided by 8 is entered as the input clock (TINCLK) of the timer.
Table 22.2 gives the 1-msec (1KHz) and 1-µsec (1MHz) cycle setting examples when the 6MHz TINCLK (if PCLK=48MHz) is entered. Set the corresponding Prescaler Control registers as follows. If you set the count to 1/1, set the prescaler load value to "0x00". To set the count to 1/2, set the load value to "0x01" and to set the count to 1/3, set the load value to "0x02" and so on.

Table 22.2 Millisecond and Microsecond Cycle Setting Examples *

Cycle	Divider dividing ratio	Prescaler load value	Frequency
1ms	Bits [15:13] = 100b (1/ 32 ratio selection)	Bits [7:0] = 1011 1010b (0xBA) (1/ 187 ratio selection)	1.002673KHz
	Bits [15:13] = 101b (1/ 64 ratio selection)	Bits [7:0] = 0101 1101b (0x5D) (1/ 94 ratio selection)	0.997340KHz
1µs	Bits [15:13] = 000b (1/ 1 ratio selection)	Bits [7:0] = 0000 0101b (0x05) (1/ 6 ratio selection)	1.000000MHz

* An example during 6MHz f_{TINCLK} input (48MHz f_{PCLK} input).

The following gives an expression to calculate the frequency you create using the PCLK frequency.
Set the divider's dividing ratio and the prescaler load value in the Prescaler [1:0] Control register so that its frequency closes to the frequency you wish to create.

$$\text{Frequency (f) to be created} = \underbrace{f_{PCLK} \div 8}_{f_{TINCLK}} \div \underbrace{\text{Value set by bits [15:13]}}_{\text{Divider dividing ratio}} \div \underbrace{\text{Value set by bits [7:0]}}_{\text{Prescaler load value}}$$

* : Prescaler [1:0] Control registers (TIM[0xA0], TIM[0xA4])

Calculation examples if settings of Table 22.2 are used

Example 1: 1kHz ≒ 48MHz ÷ 8 ÷ 32 ÷ 187 = 1.002673KHz

Example 2: 1KHz ≒ 48MHz ÷ 8 ÷ 64 ÷ 94 = 0.997340KHz

Example 3: 1MHz ≒ 48MHz ÷ 8 ÷ 1 ÷ 6 = 1.000000MHz

22.7 Timing Diagrams

22.7.1 Immediate Load Request in Cyclic Mode

The following shows a timing chart if an immediate load request is issued in the Cyclic mode and if the load value is reflected immediately. The Enable cycle of the counter is set to 1/3 by the prescaler.

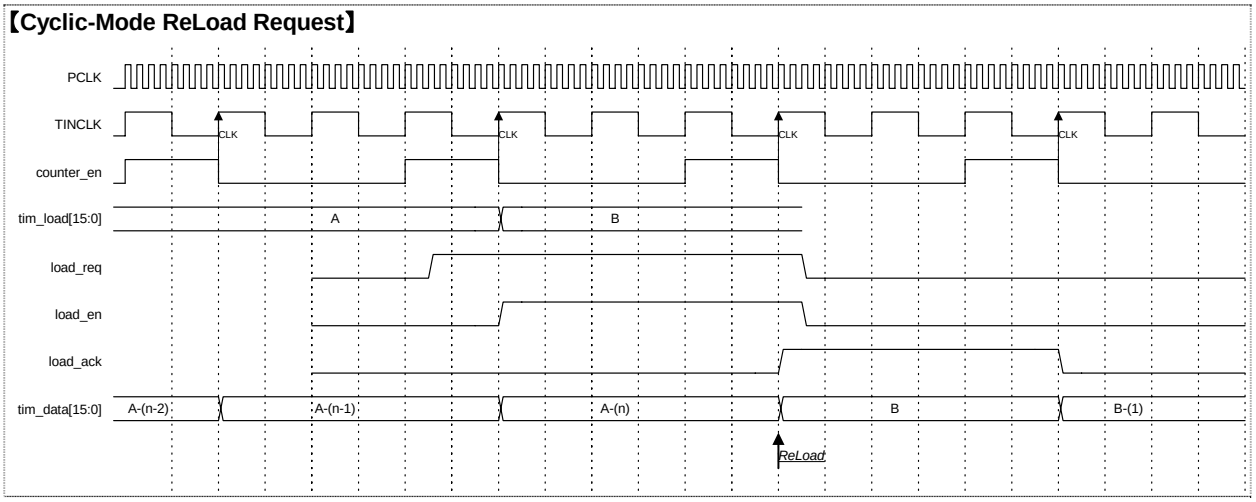


Figure 22.2 Immediate Load Request in Cyclic Mode

22.7.2 Normal Reloading in Cyclic Mode

The following shows a timing chart of normal cycle countdown if an immediate load request is NOT issued in the Cyclic mode and if the load value is reloaded when all counter outputs reach zero (0). This chart shows the interrupt occurrence and the reloading without clock dividing.

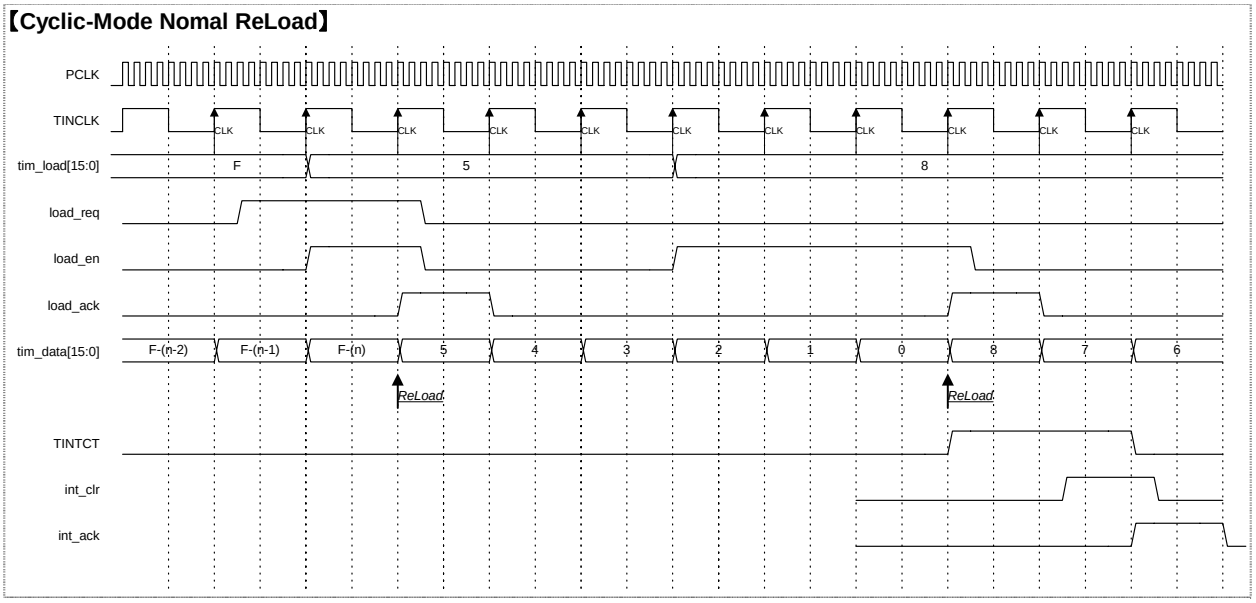


Figure 22.3 Normal Reloading in Cyclic Mode

22.7.3 Normal Reloading in Single Mode

The following shows a timing chart where an interrupt occurs when all counter outputs reach zero (0) in the Single mode and the load value is written. The clock is not divided in this example.

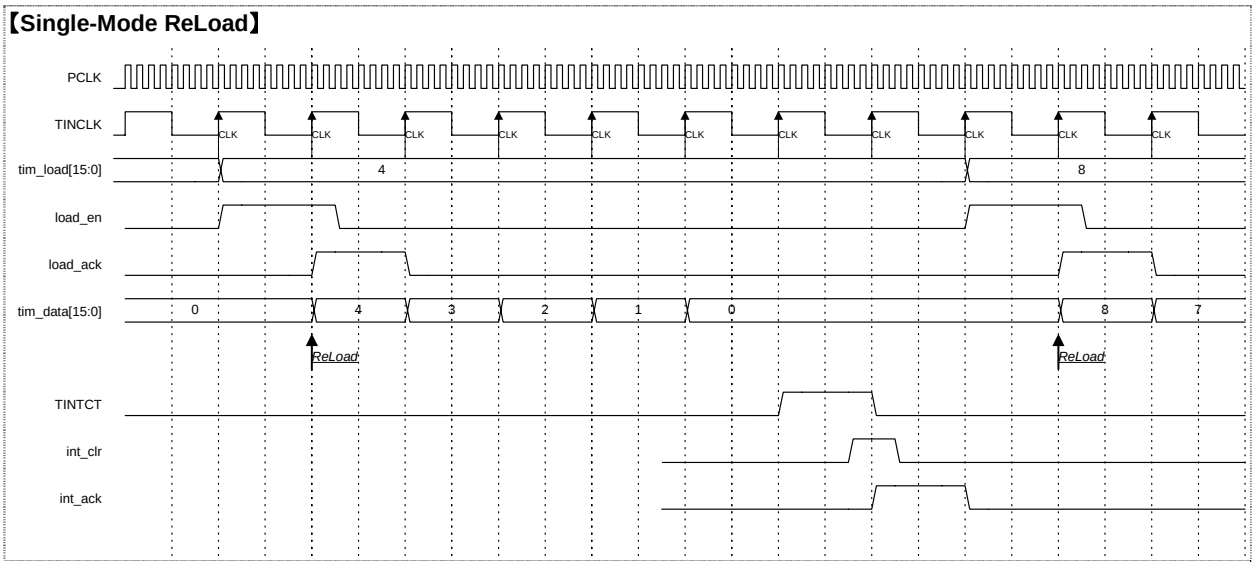


Figure 22.4 Normal Reloading in Single Mode

22.7.4 Port Outputs

The following shows the timing charts for port outputs if an underflow occurs in each mode.
Note that each chart shows the waveforms when the default divider and prescaler values (1/1) are set.

(1) Outputs a value (bit 0) during underflow (Output mode="00")
If an underflow occurs, bit 0 (output value bit) value of the Port Output Control register is held and it is output.

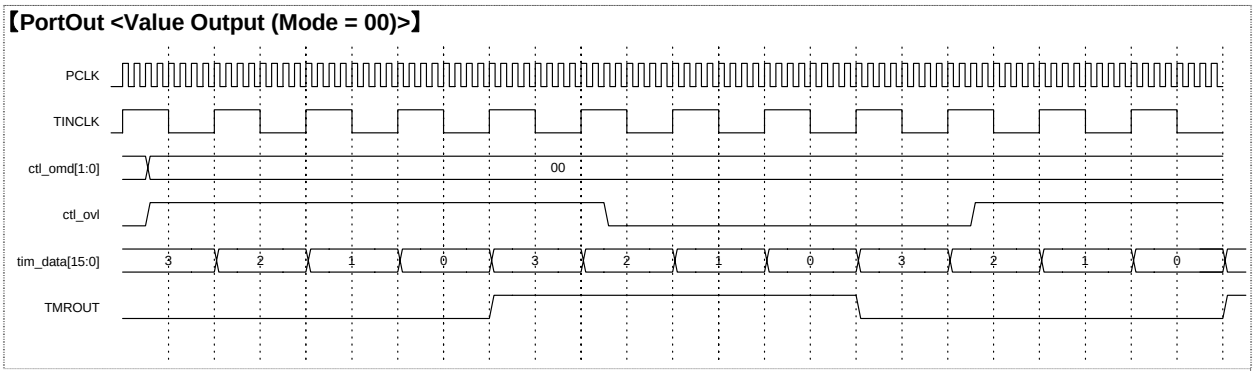


Figure 22.5 Outputs (Output Values) during Underflow

(2) Output of underflow (Output mode = “01”)
If an underflow occurs, the underflow data itself is output.
The TMROUT underflow pulse width is the same as the downcount data width. When the count changes from zero (0) to the load value (“3” in this figure), the underflow signal is output.

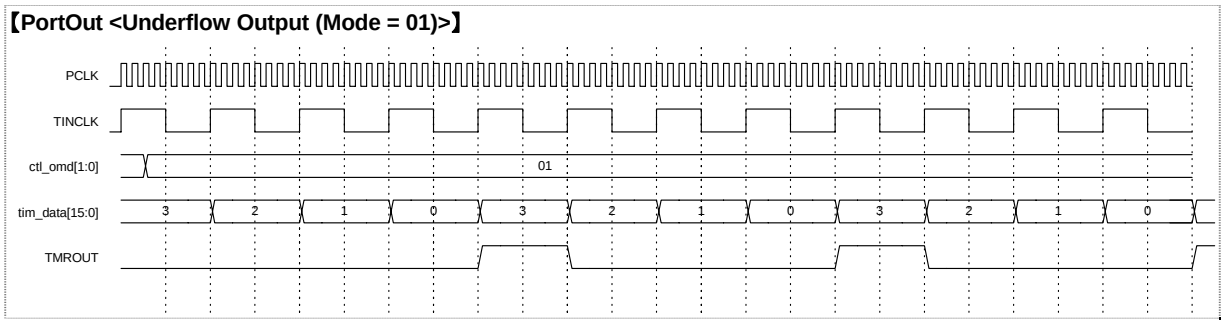


Figure 22.6 Outputs during Underflow (Underflow Output)

(3) Toggle output during underflow (Output mode=“10”)
If an underflow occurs, the signal is inverted and output.

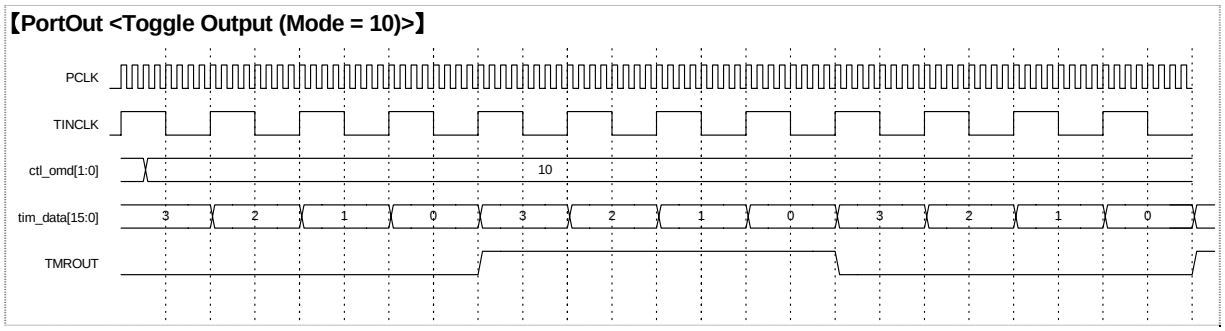


Figure 22.7 Outputs during Underflow (Toggle Output)

23. TIMER B (TIMB)

23.1 Description

Timer B is a 16-bit timer having the Output Compare function and the Input Capture function. This timer can also be operated as an event counter using externally input pulses. This is the multi-functional timer that can output pulses with any duty ratio based on the compare signals between the timer counter and four Common registers.

23.2 Features

- Counter input clock:
  1/16 to 1/2048 of external clock or internal system clock
- Can process up to 4 lines of pulse output.
- Four Common registers
  Each of them can be set as an Output register or an Input Capture register.
- Timer I/O function:
  Output compare: Allows 0 output, 1 output, or toggle output.
  Input capture: Can detect a rising edge, a falling edge, or both edges of signal waveforms.
  Allows PWM output.
- When operated as Input Capture registers, the current count and the previous count are held.
- Can count events using the externally input pulses.
- Five types of interrupt causes:
- Four (4) interrupt causes for compare matching or input capturing, and one (1) overflow interrupt

23.3 Block Diagram

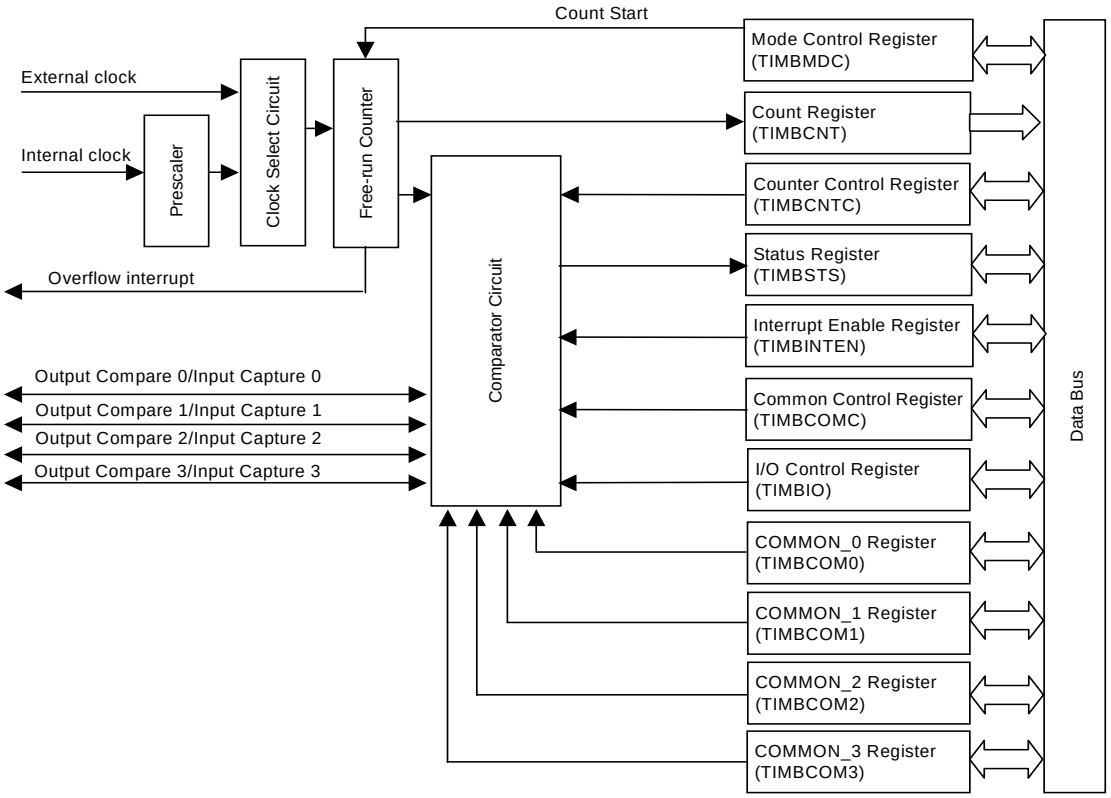


Figure 23.1 Timer-B Block Diagram

23.4 External Pins

The following defines the external pins for Timer B.

Pin Name	Input/Output	Pin Functions	Multiplex Pin*/Remarks
TimerBIn	Input	External clock input pin	GPIOB7
TimerB0IO	Input/Output	COMMON_0 register: Output compare output/Input capture input pin	GPIOC0
TimerB1IO	Input/Output	COMMON_1 register: Output compare output/Input capture input pin	GPIOC1
TimerB2IO	Input/Output	COMMON_2 register: Output compare output/Input capture input pin	GPIOC2
TimerB3io	Input/Output	COMMON_3 register: Output compare output/Input capture input pin	GPIOC3/ UART3_CLK

* As timer-B external pins are multiplexed with GPIO and other pins, this function can be used if “Function 1 other than GPIO” is set using the GPIO Pin Function register.

23.5 Registers

23.5.1 List of Registers

These registers have base address 0xFFFD_3000.

Table 23.1 List of Registers (Base Address: 0xFFFD_3000)

Address Offset	Register Name	Register Abbreviation	Default value	R/W	Data Access Size
0x00	Timer B Mode Control register	TIMBMDC	0x0000	R/W	16 (/32)
0x04	Timer B Counter Control register	TIMBCNTC	0x0000	R/W	16 (/32)
0x08	Timer B Status register	TIMBSTS	0x0000	R/W	16 (/32)
0x0C	Timer B Interrupt Enable register	TIMBINTEN	0x0000	R/W	16 (/32)
0x10	Timer B Count register	TIMBCNT	0x0000	R/W	16 (/32)
0x14	Timer B Common Control register	TIMBCOMC	0x0000	R/W	16 (/32)
0x18	Timer B I/O Control register	TIMBIO	0x0000	R/W	16 (/32)
0x1C	Timer B Cycle register	TIMBDUTY	0x0000	R/W	16 (/32)
0x20	Timer B COMMON_0 register	TIMBCOM0	0x0000	R/W	16 (/32)
0x24	Timer B COMMON_1 register	TIMBCOM1	0x0000	R/W	16 (/32)
0x28	Timer B COMMON_2 register	TIMBCOM2	0x0000	R/W	16 (/32)
0x2C	Timer B COMMON_3 register	TIMBCOM3	0x0000	R/W	16 (/32)
0x30	Timer B COMINP_0 register	TIMBINP0	0x0000	RO	16 (/32)
0x34	Timer B COMINP_1 register	TIMBINP1	0x0000	RO	16 (/32)
0x38	Timer B COMINP_2 register	TIMBINP2	0x0000	RO	16 (/32)
0x3C	Timer B COMINP_3 register	TIMBINP3	0x0000	RO	16 (/32)

23.5.2 Detailed Description of Registers

Timer B Mode Control Register (TIMBMDC)							
TIMB[0x00] Default value = 0x0000							Read/Write
clr_B3o	clr_B2o	clr_B1o	clr_B0o	set_B3o	set_B2o	set_B1o	set_B0o
15	14	13	12	11	10	9	8
Reserved				B3pwm	B2pwm	B1pwm	B0pwm
7	6	5	4	3	2	1	0

Bit 15: **clr_B3o Timer output 3 forcible clear**
- (W) 1: Forcibly sets the TimerB3io output to Low. (Invalid during input capturing)
- 0: Disabled
- (R) : Shows the current TimerB3io output status. (Invalid during input capturing)

Bit 14: **clr_B2o Timer output 2 forcible clear**
- (W) 1: Forcibly sets the TimerB2io output to Low. (Invalid during input capturing)
- 0: Disabled
- (R) : Shows the current TimerB2io output status. (Invalid during input capturing)

Bit 13: **clr_B1o Timer output 1 forcible clear**
- (W) 1: Forcibly sets the TimerB1io output to Low. (Invalid during input capturing)
- 0: Disabled
- (R) : Shows the current TimerB1io output status. (Invalid during input capturing)

Bit 12: **clr_B0o Timer output 0 forcible clear**
- (W) 1: Forcibly sets the TimerB0io output to Low. (Invalid during input capturing)
- 0: Disabled
- (R) : Shows the current TimerB0io output status. (Invalid during input capturing)

Bit 11: **set_B3o Timer output 3 forcible set**
- (W) 1: Forcibly sets the TimerB3io output to High. (Invalid during input capturing)
- 0: Disabled
- (R) : Shows the current TimerB3io output status. (Invalid during input capturing)

Bit 10: **set_B2o Timer output 2 forcible set**
- (W) 1: Forcibly sets the TimerB2io output to High. (Invalid during input capturing)
- 0: Disabled
- (R) : Shows the current TimerB2io output status. (Invalid during input capturing)

Bit 9: **set_B1o Timer output 1 forcible set**
- (W) 1: Forcibly sets the TimerB1io output to High. (Invalid during input capturing)
- 0: Disabled
- (R) : Shows the current TimerB1io output status. (Invalid during input capturing)

Bit 8: **set_B0o Timer output 0 forcible set**
- (W) 1: Forcibly sets the TimerB0io output to High. (Invalid during input capturing)
- 0: Disabled
- (R) : Shows the current TimerB0io output status. (Invalid during input capturing)

Bits [7:4]: **Reserved**

Bits 3: **B3pwm PWM mode 3 (TimerB3io output)**
- 0: Compare output
- 1: PWM output

Bits 2: **B2pwm PWM mode 2 (TimerB2io output)**
- 0: Compare output
- 1: PWM output

Bits 1: **B1pwm PWM mode 1 (TimerB1io output)**

0: Compare output
1: PWM output

Bits 0: **B0pwm PWM mode 0 (TimerB0io output)**

0: Compare output
1: PWM output

Timer B Counter Control Register (TIMBCNTC)

TIMB[0x04] Default value = 0x0000 Read/Write

BcntTST	Reserved			Bclksel			
15	14	13	12	11	10	9	8
BcntCLR	Reserved						BcntST
7	6	5	4	3	2	1	0

Bits 15: **BcntTST counter test mode (Reserved)**

Do not write value 1 here.

Bits [14:12]: **Reserved**

Bits [11:8]: Bclksel clock select *

0000: The internal system clock divided by 16
0001: The internal system clock divided by 32
0010: The internal system clock divided by 64
0011: The internal system clock divided by 128
0100: The internal system clock divided by 256
0101: The internal system clock divided by 512
0110: The internal system clock divided by 1024
0111: The internal system clock divided by 2048
1xxx: External clock

* The clock division by 8 by the system controller is included in these dividing ratios of internal system clock.

Bits 7: **BcntCLR count mode set**

0: Operates as a free-run counter. (When the counter reaches 0xFFFF, it returns to 0x0000.)
1: Operates as a cycle counter. (When the counter reaches the TIMBDUTY Cycle register value, it returns to 0x0000.)

Bits [6:1] : **Reserved**

Bits 0: **BcntST counter start**

0: Stops timer counting.
1: Starts timer counting.

Timer B Status Register (TIMBSTS)

TIMB[0x08] Default value = 0x0000 Read/Write

Reserved						Bmatch	Bovf
15	14	13	12	11	10	9	8
Reserved				B3sts	B2sts	B1sts	B0sts
7	6	5	4	3	2	1	0

Bits [15:10]: **Reserved**

Bits 9: **Bmatch Cycle register compare match status**

(R) 1: When the Cycle register value matches the timer counter value
(R) 0: No counter matching

(W) 1: Clears the Status register.
(W) 0: Invalid

Bits 8: **Bovf overflow**

(R) 1: When the timer counter overflows from FFFFh to 0000h
(R) 0: No overflow

(W) 1: Clears the Status register.
(W) 0: Invalid

Bits [7:4]: **Reserved**

Bits 3: **B3sts TimerB3io input capture/compare match status**

(R) 1: When the counter value matches during output compare setting, or
When the counter value is transferred to TIMBCOM3 by input capture setting
(R) 0: No status flag interrupt occurs.

(W) 1: Clears the Status register.
(W) 0: Invalid

Bits 2: **B2sts TimerB2io input capture/compare match status**

(R) 1: When the counter value matches during output compare setting, or
When the counter value is transferred to TIMBCOM2 by input capture setting
(R) 0: No status flag interrupt occurs.

(W) 1: Clears the Status register.
(W) 0: Invalid

Bits 1: **B1sts TimerB1io input capture/compare match status**

(R) 1: When the counter value matches during output compare setting, or
When the counter value is transferred to TIMBCOM1 by input capture setting
(R) 0: No status flag interrupt occurs.

(W) 1: Clears the Status register.
(W) 0: Invalid

Bits 0: **B0sts TimerB0io input capture/compare match status**

(R) 1: When the counter value matches during output compare setting, or
When the counter value is transferred to TIMBCOM0 by input capture setting
(R) 0: No status flag interrupt occurs.

(W) 1: Clears the Status register.
(W) 0: Invalid

Timer B Interrupt Enable Register (TMBINTEN)

TIMB[0x0C] Default value = 0x0000 Read/Write

Reserved						BmatchEN	BovfEN
15	14	13	12	11	10	9	8
reserved				B3intEN	B2intEN	B1intEN	B0intEN
7	6	5	4	3	2	1	0

Bits [15:10]: **Reserved**

Bits 9: **BmatchEN Cycle register compare match interrupt control flag**

1: Interrupt enabled
0: Interrupt disabled

Bits 8: **BovfEN TimerBovf overflow interrupt control flag**

1: Interrupt enabled
0: Interrupt disabled

Bits [7:4]: **Reserved**

Bits 3: **B3intEN TimerB3io input capture/compare match interrupt control flag**

1: Interrupt enabled
0: Interrupt disabled

Bits 2: **B2intEN TimerB2io input capture/compare match interrupt control flag**

1: Interrupt enabled
0: Interrupt disabled

Bits 1: **B1intEN TimerB1io input capture/compare match interrupt control flag**

1: Interrupt enabled
0: Interrupt disabled

Bits 0: **B0intEN TimerB0io input capture/compare match interrupt control flag**

1: Interrupt enabled
0: Interrupt disabled

Timer B Count Register (TIMBCNT)

TIMB[0x10] Default value = 0x0000 Read/Write

Bcount [15:8]							
15	14	13	12	11	10	9	8
Bcount [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **Bcount current count bits [15:0]**

The current count of timer B can be read.
If the timer counting is stopped (BcntST is set to 0), any count can be set.

Timer B Common Control Register (TIMBCOMC)

TIMB[0x14] Default value = 0x0000 Read/Write

Reserved							
15	14	13	12	11	10	9	8
Reserved				B3comFUNC	B2comFUNC	B1comFUNC	B0comFUNC
7	6	5	4	3	2	1	0

Bits [15:4]: **Reserved**

Bits 3: **B3comFUNC TIMBCOM3 function select**

0: Functions as the Output Compare register.
1: Functions as the Input Capture register.

Bits 2: **B2comFUNC TIMBCOM2 function select**

0: Functions as the Output Compare register.
1: Functions as the Input Capture register.

Bits 1: **B1comFUNC TIMBCOM1 function select**

0: Functions as the Output Compare register.
1: Functions as the Input Capture register.

Bits 0: **B0comFUNC TIMBCOM0 function sele**

0: Functions as the Output Compare register.
1: Functions as the Input Capture register.

Timer B I/O Control Register (TIMBIO)

TIMB[0x18] Default value = 0x0000 Read/Write

Reserved[15:8]							
15	14	13	12	11	10	9	8
B3comIO		B2comIO		B1comIO		B0comIO	
7	6	5	4	3	2	1	0

Bits [15:8]: **Reserved**

Bits [7:6]: **B3comIO**

If the TIMBCOM3 functions as the Output Compare register:

00: Inhibits pin output during compare matching.
01: Outputs logical 0 to TimerB3io during compare matching.
10: Outputs logical 1 to TimerB3io during compare matching.
11: Outputs toggle signal to TimerB3io during compare matching.

If the TIMBCOM3 functions as the Input Capture register:

00: Captures the input in TIMBCOM3 at the TimerB3io rising edge.
01: Captures the input in TIMBCOM3 at the TimerB3io falling edge.
10: Captures the input in TIMBCOM3 at TimerB3io rising and falling edges.
11: Reserved

Bits [5:4]: **B2comIO**

If the TIMBCOM2 functions as the Output Compare register:
- 00: Inhibits pin output during compare matching.
- 01: Outputs logical 0 to TimerB2io during compare matching.
- 10: Outputs logical 1 to TimerB2io during compare matching.
- 11: Outputs toggle signal to TimerB2io during compare matching.

If the TIMBCOM2 functions as the Input Capture register:
- 00: Captures the input in TIMBCOM2 at the TimerB2io rising edge.
- 01: Captures the input in TIMBCOM2 at the TimerB2io falling edge.
- 10: Captures the input in TIMBCOM2 at TimerB2io rising and falling edges.
- 11: Reserved

Bits [3:2]: **B1comIO**

If the TIMBCOM1 functions as the Output Compare register:
- 00: Inhibits pin output during compare matching.
- 01: Outputs logical 0 to TimerB1io during compare matching.
- 10: Outputs logical 1 to TimerB1io during compare matching.
- 11: Outputs toggle signal to TimerB1io during compare matching.

If the TIMBCOM1 functions as the Input Capture register:
- 00: Captures the input in TIMBCOM1 at the TimerB1io rising edge.
- 01: Captures the input in TIMBCOM1 at the TimerB1io falling edge.
- 10: Captures the input in TIMBCOM1 at TimerB1io rising and falling edges.
- 11: Reserved

Bits [1:0]: **B0comIO**

If the TIMBCOM0 functions as the Output Compare register:
- 00: Inhibits pin output during compare matching.
- 01: Outputs logical 0 to TimerB0io during compare matching.
- 10: Outputs logical 1 to TimerB0io during compare matching.
- 11: Outputs toggle signal to TimerB0io during compare matching.

If the TIMBCOM0 functions as the Input Capture register:
- 00: Captures the input in TIMBCOM0 at the TimerB0io rising edge.
- 01: Captures the input in TIMBCOM0 at the TimerB0io falling edge.
- 10: Captures the input in TIMBCOM0 at TimerB0io rising and falling edges.
- 11: Reserved

Timer B Cycle Register (TIMBDUTY)

TIMB[0x1C] Default value = 0x0000 Read/Write

Bduty[15:8]							
15	14	13	12	11	10	9	8
Bduty [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **Bduty Duty register**

Set a cycle count value in the Cycle Count mode.

Timer B COMMON_0 Register (TIMBCOM0)

TIMB[0x20] Default value = 0x0000 Read/Write

B0com[15:8]							
15	14	13	12	11	10	9	8
B0com [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **B0com COMMON_0 register**

Set a counter value in the Output Compare mode.

The immediately preceding B0inp content is held in the Input Capture mode.

Timer B COMMON_1 Register (TIMBCOM1)

TIMB[0x24] Default value = 0x0000 Read/Write

B1com[15:8]							
15	14	13	12	11	10	9	8
B1com [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **B1com COMMON_1 register**

Set a counter value in the Output Compare mode.

The immediately preceding B1inp content is held in the Input Capture mode.

Timer B COMMON_2 Register (TIMBCOM2)

TIMB[0x28] Default value = 0x0000 Read/Write

B2com[15:8]							
15	14	13	12	11	10	9	8
B2com[7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **B2com COMMON_2 register**

Set a counter value in the Output Compare mode.

The immediately preceding B2inp content is held in the Input Capture mode.

Timer B COMMON_3 Register (TIMBCOM3)

TIMB[0x2C] Default value = 0x0000 Read/Write

B3com[15:8]							
15	14	13	12	11	10	9	8
B3com[7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **B3com COMMON_3 register**

Set a counter value in the Output Compare mode.

The immediately preceding B3inp content is held in the Input Capture mode.

Timer B COMINP_0 Register (TIMBINP0)

TIMB[0x30] Default value = 0x0000 Read Only

B0inp[15:8]							
15	14	13	12	11	10	9	8
B0inp [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **B0inp COMINP_0 register**

The counter value is entered in the Input Capture mode.

Timer B COMINP_1 Register (TIMBINP1)

TIMB[0x34] Default value = 0x0000 Read Only

B1inp[15:8]							
15	14	13	12	11	10	9	8
B1inp [7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **B1inp COMINP_1 register**

The counter value is entered in the Input Capture mode.

Timer B COMINP_2 Register (TIMBINP2)

TIMB[0x38] Default value = 0x0000 Read Only

B2inp[15:8]							
15	14	13	12	11	10	9	8
B2inp[7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **B2inp COMINP_2 register**

The counter value is entered in the Input Capture mode.

Timer B COMINP_3 register (TIMBINP3)

TIMB[0x3C] Default value = 0x0000 Read Only

B3inp[15:8]							
15	14	13	12	11	10	9	8
B3inp[7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **B3inp COMINP_3 register**

The counter value is entered in the Input Capture mode.

23.6 Explanation of Operations

23.6.1 Count Operations

There are two types of timer counter operations: the free-running count operation using the 16-bit up counter, and the cycle count operation.

(1) Free-running count operation
If the count mode setting bit (Bit[7]) of Counter Control register (TIMBCNTC) is set to 0 and if the counter start bit (Bit[0]) is set to 1, the free-running count operation starts. The count clock is divided by the built-in prescaler based on the clock select bits (Bits[3:1]) of Counter Control register (TIMBCNTC). When the counter overflows from FFFFh to 0000h, the overflow bit (Bovf bit[8]) of Status register (TIMBSTS) is set to 1. If the overflow control flag (Bit[8]) of Interrupt Enable register (TIMBINTEN) has been set to interrupt enabled, an interrupt request (TimerBovf) occurs.
The interrupt request (Bovf) is cleared by the software. Figure 23.2 illustrates the free-running count operation.

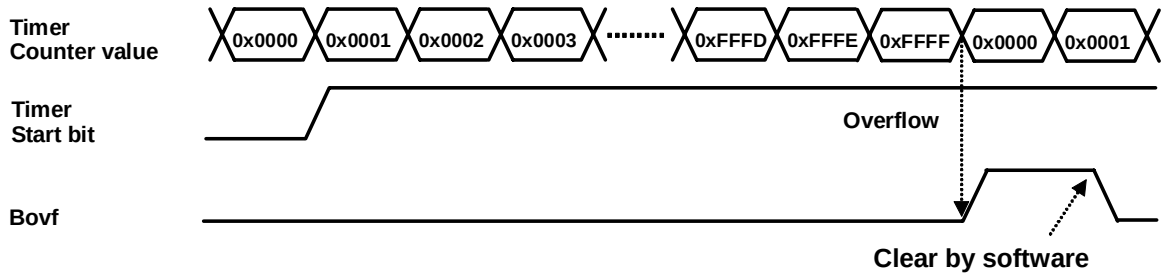


Figure 23.2 Free-running Count Operation

(2) Cycle count operation
If the count mode setting bit (Bit[7]) of Counter Control register (TIMBCNTC) is set to 1, the cycle count operation starts with the Cycle register value. When the counter value matches the Cycle register value, the timer counter is cleared to 0000h and the cycle register compare match (Bit[9]) of Status register (TIMBSTS) is set to 1. If the cycle register compare match interrupt control flag (Bit[9]) of Interrupt Enable register (TIMBINTEN) has been set to interrupt enabled, an interrupt request (TimerBovf) occurs. The interrupt request (Bmatch) is cleared by the software. Figure 23.3 illustrates the cycle count operation if the Cycle register value is 12FFh.

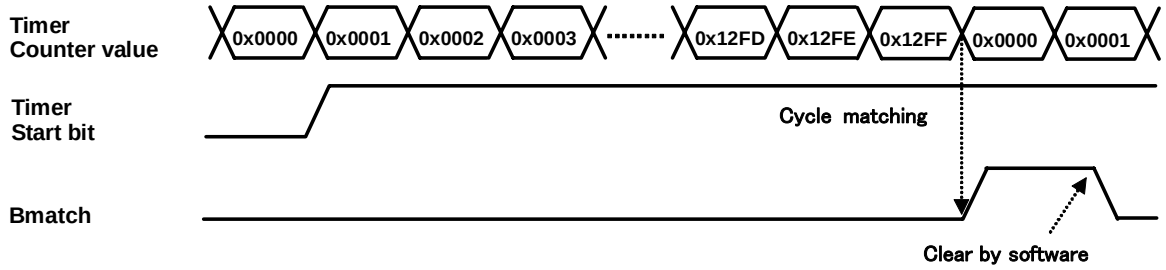


Figure 23.3 Cycle Count Operation (if Cycle Register Value is 12FFh)

23.6.2 Timer I/O Functions

Timer B has the following three input and output function modes. Each mode can be set for each pin (TimerB0/1/2/3io) separately.

- Output compare
- PWM output
- Input capture

(1) Output compare operations

If the TimerB0io, TimerB1io, TimerB2io, and TimerB3io functions of Common Control registers (TIMBCOM) are set in the Output Compare registers and if the function of I/O Control register (TIMBIO) is selected, the logical 0, logical 1 or toggle signals can be output at TimerB0io, TimerB1io, and TimerB3io pins.

Figure 23.4 shows the operations if the timer counter operates in the free-running mode, if value AAAAh is set in the COMMON_0 register, value BBBBh is set in the COMMON_1 register, and value AAAAh is set in the COMMON_2 register, and if TimerB0io pin is set for logical 1 output, TimerB1io pin is set for logical 0 output, and TimerB2io pin is set for toggle output.

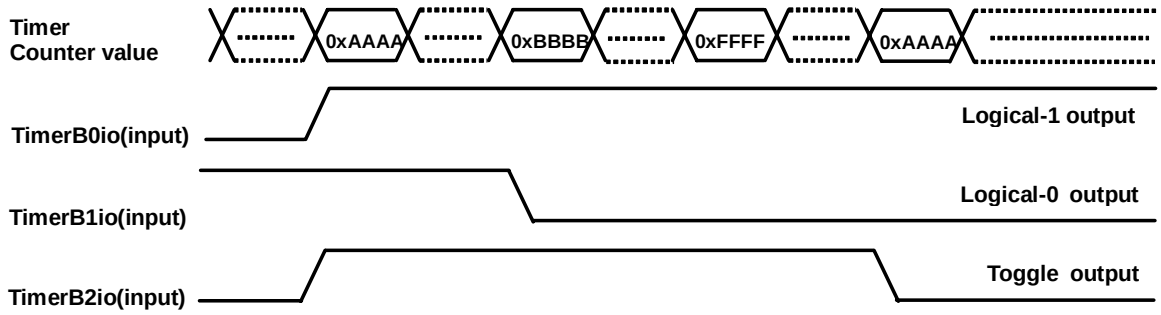


Figure 23.4 Output Settings

When the Common register value matches the counter value, the “B*sts” interrupt cause occurs regardless of the change of “imerB*io” pin output.

(2) PWM operations

In the PWM mode, the PWM waveforms are output at each of TimerB0io, TimerB1io, TimerB2io, and TimerB3io output pins based on the values of Common registers (TIMBCOM0, TIMBCOM1, TIMBCOM2, and TIMBCOM3) against the Cycle register (TIMBDUTY). Up to 4 phases of PWM waveforms can be output. If the PWM mode output function (Bits[3:0]) is selected using the Mode Control register (TIMBMDC), the selected Common register functions as the Compare register for PWM. If the Cycle register (TIMBDUTY) and Common register values are identical, the output value does not change even when a compare match occurs.

Figure 23.5 shows the operation if the Cycle register is set to FF00h, the TIMBCOM0 is set to AA00h, and TIMBCOM1 is set to BB00h and if the output level is high at TimerB0io and TimerB1io pins.

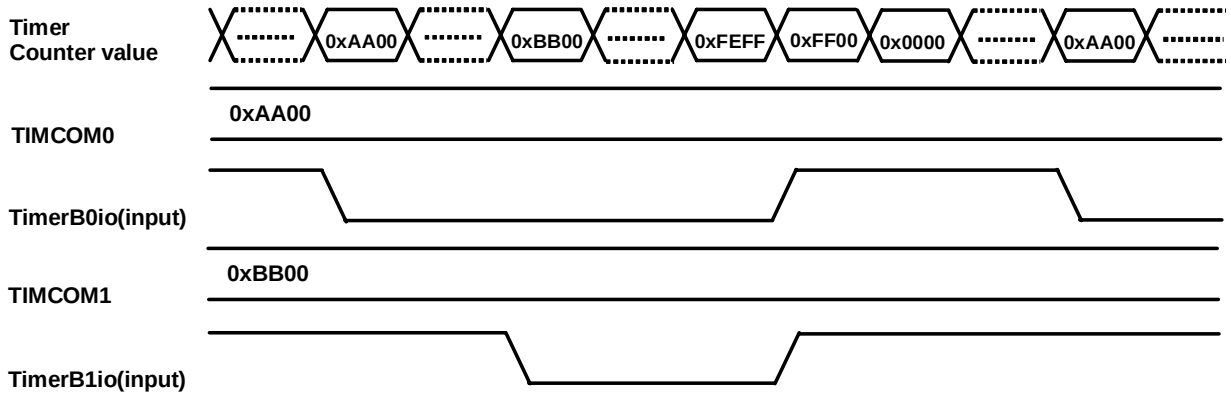


Figure 23.5 PWM Operations

(3) Input capture operations

If the TimerB0io, TimerB1io, TimerB2io, and TimerB3io functions of common control registers (TIMBCOMC) are set as Input Capture registers, an input signal edge is detected at TimerB0io, TimerB1io, TimerB2io, and TimerB3io pins and the timer counter value can be sent to the COMINP_0 register, COMINP_1 register, COMINP_2 register, and COMINP_3 register. Also, the previous COMINP_* register content is saved in the COMMON_* register. Therefore, the interval of input signal edges can be calculated accurately based on the contents of both registers and the occurrence count of overflow interrupts. A rising edge, a falling edge, or both edges of signals can be detected if its function is set by the I/O Control register (TIMBIO). You can measure the signal pulse width and cycle using these functions.

Figure 23.6 shows the operations if the timer counter is set to the free-running operation, if both rising and falling edges of a signal are detected at TimerB0io pin with the input capture function, and if a raising edge of signal is detected at TimerB1io pin with the input capture function.

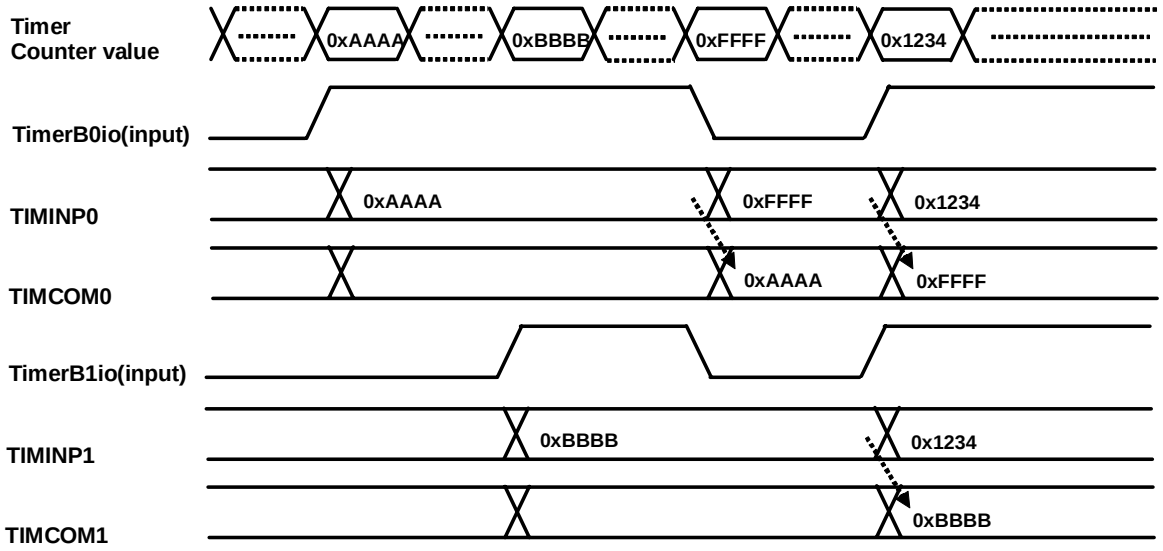


Figure 23.6 Operation Settings

24. REAL-TIME CLOCK (RTC)

24.1 Description

The real-time clock (called the RTC) receives the 32,768Hz input clock, measures the time using the 256Hz clock output prescaler, 8-bit dividing timer, and second, minute, hour, day, month and year counters. Also, this RTC has various time measuring functions including the watch and stopwatch. Each data can be read by the software. Also, the RTC can generate an interrupt when 32Hz, 8Hz, 2Hz, 1 second, 1 minute, 1 hour or 1 day is counted up. It can be used for cyclic interrupt and as the wakeup source. Also, an alarm can be generated by specifying the minutes, hours, day, month and year. The RTC can be used as the wakeup source and for alarming. If the 32,768Hz clock is running, the RTC can operate even when the CPU and other built-in peripheral circuits are standing by. Because the system reset does not affect on the RTC's time measurement, it can continue to measure the time even if an external reset signal is entered.
The RTC has the 8-byte, built-in RAM as the backup memory.
The RTC can operate in the backup mode that can greatly reduce its power consumption. This can be realized if all device circuits are powered, if the BUP# pin is set to logical 0, and if the power supply to all pins is stopped except for the RTCVDD pin. During this time, the RTC cannot be accessed.

24.2 Block Diagram

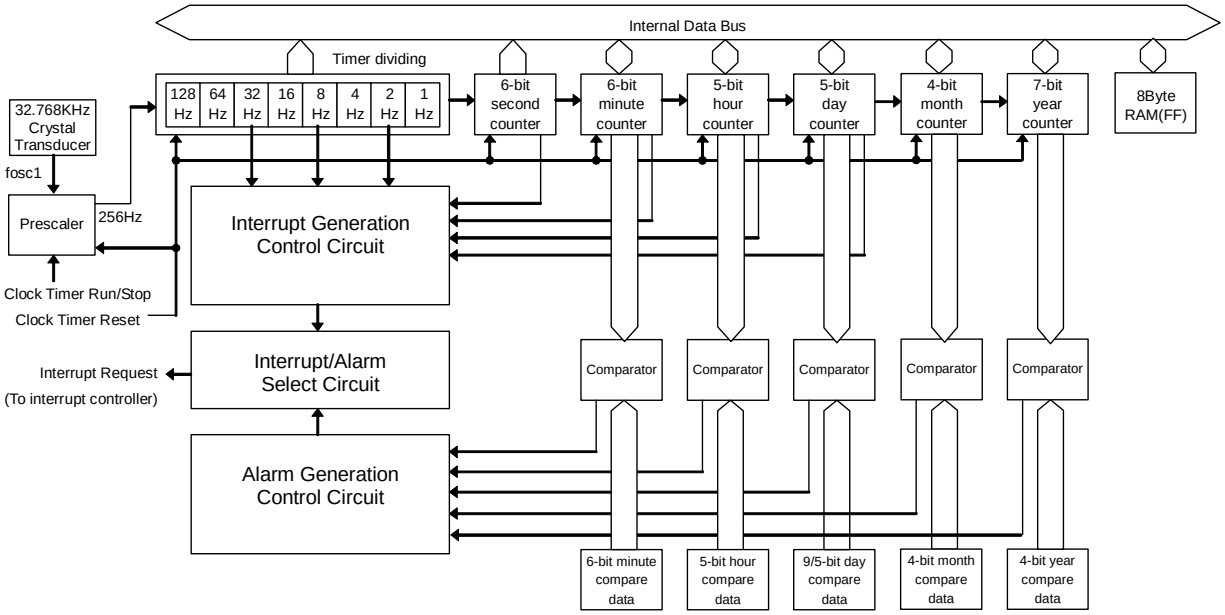


Figure 24.1 Block Diagram

24.3 External Pins

The following defines the RTC external pins.

Pin Name	Input/Output	Bus Width	Pin Functions	Multiplex Pin/Remarks
BUP#	Input	1	Switch to standby mode (1.8 V pin)	
SYS_OSCI	Input	1	Crystal transducer connect pin	
SYS_OSCO	Output	1	Crystal transducer connect pin	

The BUP# pin is provided to prevent an irregular state from being propagated to the RTC from any other part after the main power (LVDD) is shut down. The pin must be set to Low before the LVDD is shut down. The RTC is not accessible when the pin is in Low state.

24.4 Registers

24.4.1 List of Registers

These registers have base address 0xFFFF_8000.

Table 24.1 List of Registers (Base Address: 0xFFFF_8000)

Address Offset	Register Name	Register Abbreviation	Default value	Data Access Size
0x00	RTC Run/Stop Control Register	xxx- --xx b	R/W	8 (/16/32)
0x04	RTC Interrupt Register	0x XXXX	R/W	16 (/32)
0x08	RTC Timer Dividing Register	xxxx xxxx b	R/(W)	8 (/16/32)
0x0C	RTC Second Counter Register	--xx xxxx b	R/W	8 (/16/32)
0x10	RTC Minute Counter Register	--xx xxxx b	R/W	8 (/16/32)
0x14	RTC Hour Counter Register	---x xxxx b	R/W	8 (/16/32)
0x18	RTC Day Counter Register	---x xxxx b	R/W	8 (/16/32)
0x1C	RTC Month Counter Register	---- xxxx b	R/W	8 (/16/32)
0x20	RTC Year Counter Register	-xxx xxxx b	R/W	8 (/16/32)
0x24	RTC Alarm Minute Compare Register	--xx xxxx b	R/W	8 (/16/32)
0x28	RTC Alarm Month Compare Register	---x xxxx b	R/W	8 (/16/32)
0x2C	RTC Alarm Day Compare Register	---x xxxx b	R/W	8 (/16/32)
0x30	RTC Alarm Month Compare Register	---- xxxx b	R/W	8 (/16/32)
0x34	RTC Alarm Year Compare Register	-xxx xxxx b	R/W	8 (/16/32)
0x38 - 0x3C	n/a			
0x40	RTC Test Register	---x xxxx b	R/W	8 (/16/32)
0x44	RTC Prescaler Register	-xxx xxxx b	R/(W)	8 (/16/32)
0x48	RTC Test Clock Register	xxxx xxxx b	RO	8 (/16/32)
0x4C – 0x5C	n/a			
0x60	RTC RAM0	xxxx xxxx b	R/W	8 (/16/32)
0x64	RTC RAM1	xxxx xxxx b	R/W	8 (/16/32)
0x68	RTC RAM2	xxxx xxxx b	R/W	8 (/16/32)
0x6C	RTC RAM3	xxxx xxxx b	R/W	8 (/16/32)
0x70	RTC RAM4	xxxx xxxx b	R/W	8 (/16/32)
0x74	RTC RAM5	xxxx xxxx b	R/W	8 (/16/32)
0x78	RTC RAM6	xxxx xxxx b	R/W	8 (/16/32)
0x7C	RTC RAM7	xxxx xxxx b	R/W	8 (/16/32)

24.4.2 Detailed Description of Registers

All reserved bits must be set to logical 0 unless otherwise specified. If these reserved bits are read by the software, those values should be ignored.

RTC Run/Stop Control Register (8 bit)							
RTC[0x00] Default value = xxx- --xx b							Read/Write
BUSY	BUSYWIDTH[1:0]		Reserved			TCADJ	TCRUN
x	xx		—			—	x
RO	R/W					WO	R/W
7	6	5	4	3	2	1	Bit0

x: Undefined bit

Bit 7: **BUSY Busy (Read only)**

In existing models, it is not guaranteed that correct data is read since update cycle is in progress in the clock register in the RTC when this bit is "1". With the S2S65A30, it is possible to read a value even when this bit is "1". To provide software compatibility with existing models, discard a value if this bit is "1" and wait until it goes to "0".

This bit remains "1" for the duration specified by bits [6:5] (BUSYWIDTH) of RTC Run/Stop Control register. The S2S65A30 may not operate correctly during this duration. Avoid setting clocks and alarms.

Bits [6:5]: **BUSYWIDTH busy interval**

Sets a busy interval.

- 00: Approx. 244 µsec
- 01: Approx. 122 µsec
- 10: Approx. 61 µsec
- 11: Reserved

This bit is not initialized by system reset.

To assure the normal operation, you must reset the system when the RTC is stopped.

Bits [4:2]: **Reserved Reserved**

Bit 1: **TCADJ RTC adjust (Write Only)**

- 0: Normal mode
  When this bit is read, the signal is always set to logical 0.
- 1: Adjust RTC counter
  If this bit is set to logical 1 and if bit 0 of RTC run/stop control register is set to logical 0 simultaneously, only the prescaler counter and the 128-1Hz counter are reset.

If the RTC is operating, this adjustment is made invalid.

Bit 0: **TCRUN**

Read

- 0: When RTC is stopped
- 1: When RTC is operating

Write

- 0: Stops the RTC.
- 1: Starts the RTC.

The operation or shutdown occurs after approximately 30 to 61 µsec for synchronization with the 32KHz clock.

RTC Interrupt Register (16 bit)

RTC[0x04] Default value = 0xXXXX Read/Write

Reserved					TCISE[2:0]		
—	—	—	—	—	x	x	x
					R/W	R/W	R/W
15	14	13	12	11	10	9	8
Reserved	TCASE[4:0]					TCIF	TCAF
—	x	x	x	x	x	x	x
	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [15:11]: **Reserved Reserved**

Bits [10:8]: **TCISE[2:0] interrupt source enable select bits**

000: Carry from “32Hz” (Once every 1/32 sec)
001: Carry from “8Hz” (Once every 1/8 sec)
010: Carry from “2Hz” (Once every 1/2 sec)
011: Carry from “1Hz” (Once every second)
100: Carry from “1 minute” (Once every minute)
101: Carry from “1 hour” (Once every hour)
110: Carry from “Day” (Once every day)
111: No interrupt source (Default)

Because the status change of carry is used as the interrupt source, the interrupt occurs only once in the specified internal.

Bits [6:2]: **TCASE[4:0] RTC alarm source select bit**

00000: No alarm (Default)
xxxx1: Minute alarm enable
xxx1x: Hour alarm enable
xx1xx: Day Hour alarm enable
x1xxx: Month alarm enable
1xxxx: Year alarm enable

If the alarm source counter being set to logical 1 matches the Alarm Compare register value, an interrupt occurs. If multiple sources have been enabled and if all of them match the Alarm Compare register value, an interrupt occurs.

This interrupt is generated as soon as the value of each alarm source changes and matches the Alarm Compare register value. In existing models, when the Hour and Day Hour alarms are enabled, an interrupt would occur as soon as an alarm source is set within one hour after the occurrence of an interrupt. In the S2S65A30, an interrupt occurs as soon as each alarm source changes.

Bit 1: **An interrupt request flag from TCIF RTC timer**

Read
0: No pending interrupt exists.
1: A pending interrupt request from RTC timer exists.
Write
0: N/A
1: The interrupt request from RTC timer is cleared.

Bit 0: **An interrupt request flag from TCAF alarm**

Read
0: No pending interrupt exists.
1: A pending interrupt request from the alarm exists.
Write
0: N/A
1: The interrupt request from the alarm is cleared.

RTC Timer Dividing Register (8 bit)

RTC[0x008] Default value = xxxx xxxx b Read/(Write)

TCD[7:0]							
x	x	x	x	x	x	x	x
R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)
7	6	5	4	3	2	1	0

x: Undefined bit

Bit 7: **TCD7: 1Hz indicator** 1: High; 0: Low
Bit 6: **TCD6: 2Hz indicator** 1: High; 0: Low
Bit 5: **TCD5: 4Hz indicator** 1: High; 0: Low
Bit 4: **TCD4: 8Hz indicator** 1: High; 0: Low
Bit 3: **TCD3: 16Hz indicator** 1: High; 0: Low
Bit 2: **TCD2: 32Hz indicator** 1: High; 0: Low
Bit 1: **TCD1: 64Hz indicator** 1: High; 0: Low
Bit 0: **TCD0: 128Hz indicator** 1: High; 0: Low

This register is reset to 0 when bit 1 (TCADJ) of RTC Run/Stop Control register (RTC[0x00]) is set to logical 1. The software can consider this register as the up counter. Because this register does not have the circuit to synchronize the 32KHz signal with the system clock, the clock value must be read multiple times and the same value must be used as the correct one.
This register is write enabled only when the dividing counter is set to the write enabled mode by the RTC Test register (RTC[0x40]). Because this is the hardware test function, the data written in this register during dividing counter in the write enabled mode is unreliable.

RTC Second Counter Register (8 bit)

RTC[0x0C] Default value = --xx xxxx b Read/Write

Reserved		TCMD[5:0]					
—	—	x	x	x	x	x	x
		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [7:6]: **Reserved Reserved**

Bits [5:0]: **TCMD[5:0]**
These 6 bits show the binary data indicating from 0 to 59 seconds.
TCMD5=MSB, TCMD0=LSB.
If a value greater than 59 is written, it is reflected as it is.

RTC Minute Counter Register (8 bit)

RTC[0x10] Default value = --xx xxxx Read/Write

Reserved		TCHD[5:0]					
—	—	x	x	x	x	x	x
		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [7:6]: **Reserved Reserved**

Bits [5:0]: **TCHD[5:0]**
These 6 bits show the binary data indicating from 0 to 59 minutes.
TCHD5=MSB, TCHD0=LSB.
If a value greater than 59 is written, it is reflected as it is.

RTC Hour Counter Register (8 bit)
RTC[0x14] Default value = ---x xxxx b Read/Write

Reserved			TCDD[4:0]				
—	—	—	x	x	x	x	x
			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [7:5]: **Reserved Reserved**

Bits [4:0]: **TCDD[4:0]**
These 5 bits show the binary data indicating from 0 to 23 hours.
TCDD4=MSB, TCDD0=LSB.
If a value greater than 23 is written, it is reflected as it is.

RTC Day Counter Register (8 bit)
RTC[0x18] Default value = ---x xxxx b Read/Write

Reserved			TCND [4:0]				
—	—	—	x	x	x	x	x
			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [7:5]: **Reserved Reserved**

Bits [4:0]: **TCND[4:0]**
These 5 bits show the binary data indicating from the first to 31st day.
TCND4 = MSB, TCND0 = LSB.
If value 0 or a value greater than 31 is written, it is reflected as it is.

RTC Month Counter Register (8 bit)
RTC[0x1C] Default value = ---- xxxx b Read/Write

Reserved				TCDD[3:0]			
—	—	—	—	x	x	x	x
				R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [7:4]: **Reserved Reserved**

Bits [3:0]: **TCTD[3:0]**
These 4 bits show the binary data indicating from January to December.
TCTD3=MSB, TCTD0=LSB.
If value 0 or a value greater than 12 is written, it is reflected as it is.

RTC Year Counter Register (8 bit)

RTC[0x20] Default value = -xxx xxxx b Read/Write

Reserved	TCYD[6:0]						
—	x	x	x	x	x	x	x
	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bit 7: **Reserved Reserved**

Bits [6:0]: **TCYD[6:0]**
These 7 bits show the binary data indicating from year 01 to year 99.
TCYD6=MSB, TCTD0=LSB.
If value 0 or a value greater than 99 is written, it is reflected as it is.

RTC Alarm Minute Compare Register (8 bit)

RTC[0x24] Default value = --xx xxxx b Read/Write

Reserved		TCCH[5:0]					
—	—	x	x	x	x	x	x
		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [7:6]: **Reserved Reserved**

Bits [5:0]: **TCCH[5:0]**
These 6 bits show the binary data indicating from 0 to 59 minutes.
TCCH5=MSB, TCCH0=LSB.
If a value greater than 59 is written, it is reflected as it is.

RTC Alarm Hour Compare Register (8 bit)

RTC[0x28] Default value = ---x xxxx b Read/Write

Reserved			TCCD[4:0]				
—	—	—	x	x	x	x	x
			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [7:5]: **Reserved Reserved**

Bits [4:0]: **TCCD[4:0]**
These 5 bits show the binary data indicating from 0 to 23 hours.
TCCD4=MSB, TCCD0=LSB.
If a value greater than 23 is written, it is reflected as it is.

RTC Alarm Day Compare Register (8 bit)

RTC[0x2C] Default value = ---- ---x xxxx xxxx b Read/Write

Reserved			TCCN[4:0]				
—	—	—	X	x	x	x	x
			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [4:0]: **TCCN[4:0]**

These 4 bits show the binary data indicating from 0 to 31st day.
TCCN4=MSB, TCCN0=LSB.
If value 0 or a value greater than 31 is written, it is reflected as it is.

RTC Alarm Month Compare Register (8 bit)

RTC[0x30] Default value = ---- xxxx b Read/Write

Reserved				TCCT[3:0]			
—	—	—	—	x	x	x	x
				R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit (b)

Bits [7:4]: **Reserved Reserved**

Bits [3:0]: **TCCT[3:0]**

These 4 bits show the binary data indicating from 0 to 15 months.
TCCT3=MSB, TCCT0=LSB.
If value 0 or a value greater than 12 is written, it is reflected as it is.

RTC Alarm Year Compare Register (8 bit)

RTC[0x34] Default value = -xxx xxxx b Read/Write

Reserved	TCCY[6:0]						
—	x	x	x	x	x	x	x
	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bit 7: **Reserved Reserved**

Bits [3:0]: **TCCY[6:0]**

These 7 bits show the binary data indicating from 0 to 127 years.
TCCY6=MSB, TCCY0=LSB.
If value 0 or a value greater than 99 is written, it is reflected as it is.

RTC Test Register (8 bit)

RTC[0x40] Default value = ---x xxxx b — Read/Write

Reserved			RTST4	RTST3	RTST2	RTST1	RTST0
—			x	x	x	x	x
—			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [7:5]: **Reserved Reserved**

Bits [4:1]: **RTST[4:1] Test mode set**

0000: Dividing counter write-enabled mode
The dividing counter is write enabled in this mode.

xx10: Test Clock mode
In the Test Clock mode, clock signals are written in the RTC Test Clock register instead of the 32KHz clock, and the generated pulses are used.

x1xx: Second, minute, hour, day, year and month counter carry bypass mode
Carries of second, minute, hour, day, year and month counters are used as clocks.

1xxx: Dividing counter carry bypass mode
The dividing counter carry is used as the clock.

Bit 0 **RTST0 Test mode enable**

If logical 1 is written in the previous time and if logical 0 is written next, the Test mode is selected.

RTC Prescaler Register (8 bit)

RTC[0x44] Default value = -xxx xxxx b — Read/(Write)

Reserved	TCP [6:0]						
—	x	x	x	x	x	x	x
	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)
7	6	5	4	3	2	1	0

x: Undefined bit

Bits 7: **Reserved Reserved**

Bits [6:0]: **TCP[6:0]**

These 7 bits show the prescaler value.
TCP8=MSB, TCP0=LSB.
This register is not initialized by system reset.
This register is write enabled only when the dividing counter is set to the write enabled mode by the RTC Test register. Because this is the hardware test function, the data written in this register during dividing counter in the write enabled mode is unreliable.

RTC Test Clock Register (8 bit)

RTC[0x48] Default value = -xxx xxxx b — Write Only

TSTCLK[7:0]							
x	x	x	x	x	x	x	x
WO	WO	WO	WO	WO	WO	WO	WO
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [7:0]: **TSTCLK[7:0] Test clock**

If the Test Clock mode is set by the RTC Test register and if any value is written in this register, a single pulse of test clock is generated. Because this function is for the hardware test only, the operation is unreliable if this register is used.

RTC RAM0-7 Register (8 bit)

RTC[0x60 - 0x7C] Default value = xxxx xxxx b Read/Write

TCRAM0[7:0]							
x	x	x	x	x	x	x	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

x: Undefined bit

Bits [7:0]: **TCRAM0 to 7[7:0]**

These 8 bits can be used as the RAM.
TCRAM0-7[7]=MSB, TCRAM0-7 [0]=LSB.
This register is not initialized by the system reset or ADJ bit.

24.5 Setting RTC Registers

If the Test register or Test Clock register is used or if the device is operated in the Test mode, the resulting operation is unreliable and it is not guaranteed. Also, all registers are NOT initialized by the system reset.

24.5.1 Initialization after Power-On

All registers in the RTC are unstable immediately after the system power-On. The following initialization procedure must be used.

A) Set all bits of RTC Test register (RTC[0x40]) to “0x00” twice.
B) Because you must stop the RTC during various settings, set bit 0 of RTC Run/Stop Control register (RTC[0x00]) to “0b0” to stop writing.
C) Make sure that bit 0 of RTC Run/Stop Control register (RTC[0x00]) is “0b0”.
(When this bit is “0b0”, the RTC has been stopped. When it is “0b1”, the RTC is operating. You must securely check that the RTC has been stopped. This is because the RTC stops with a delay of 30 to 61 µsec so that various register settings are synchronized with the 32KHz system circuit operations. Bit 0 of RTC Run/Stop Control register (RTC[0x00]) is set based on the Run/Stop Control signal of the 32KHz system circuit that has been synchronized again. Therefore, a certain delay occurs due to the synchronization.)
D) Set bits 1 and 0 of RTC Run/Stop Control register (RTC[0x00]) to “0b10” so that the prescaler and the dividing timer are reset.
(Because all registers are unstable during power-On, both the prescaler and dividing timer can be initialized to zero (0) by this operation. Note that bit 1 must be set to “0b1” and bit 0 must be set to “0b0”.)
E) Before setting the date and time, be sure to disable an interrupt and clear all flags. Write value “0x0703” in the RTC Interrupt register (RTC[0x04]) so that the interrupt controller is not affected.
F) After you have set the RTC Interrupt register (RTC[0x04]), set the date and time. Set the Second, Minute, Hour, Day, Month and Year counters correctly.
(You must enter these values correctly because the counter may malfunction if you write nonexistent time and if a lower digit is carried up.)
G) To set an alarm, set the Minute, Hour, Day, Month, and Year Alarm Compare registers. Also, if you set an interrupt, enable both the cycle interrupt and the alarm interrupt of RTC Interrupt register (RTC[0x04]).
H) We recommend you to clear an interrupt flag and initialize the 8-byte RAM because its initial value is still unreliable.
I) Finally, set the BUSY signal width of the RTC Run/Stop Control register (RTC[0x00]). We recommend you to set the BUSY signal width that is greater than the time the software process ends. For example, if the setting process (including a process that is terminated by another process) can ends within 100 µsec,

you should set the BUSYWIDTH value to "01" (122 μsec). Because the RTC has been stopped, the Second counter setting through the BUSY signal width setting may be made in a different order. You can set them in any order without any problem.

J) After these settings, set bit 0 of RTC Run/Stop Control register (RTC[0x00]) to "0b1" so that the RTC starts. The RTC starts operating after 30 to 61 μsec.

24.5.2 Stop and Restart of Operations

Set bit 0 of RTC Run/Stop Control register (RTC[0x00]) to "0b0" and wait until bit 0 of RTC Run/Stop Control register (RTC[0x00]) is set to "0b0" (approximately 30 to 61 μsec). When bit 0 is set to "0b0", the operation is stopped. Each counter value is held even when the operation is stopped. To restart the operation, set bit 0 of RTC Run/Stop Control register (RTC[0x00]) to "0b1". Counting starts from the held value. If you restart the operation after interrupt processing, clear the interrupt flag first. Then, set bits 1 and 0 of RTC Run/Stop Control register to "10" and reset both prescaler and dividing timer. Then, set bit 0 of RTC Run/Stop Control register (RTC[0x00]) to "0b1" so that the write operation restarts.

24.5.3 Repeated Setting without Operation Stop

If you access to any bit during operation, except for bit 0 of RTC Run/Stop Control register (RTC[0x000]), the operation becomes unreliable. Especially, if you reset the prescaler and the dividing timer during operation, a malfunction may result.
You can change the settings of RTC Interrupt register and the Minute, Hour, Day, Month and Year Alarm Compare register when the BUSY bit is logical 0. However, disable an RTC interrupt using the interrupt controller before changing the register settings. After the change, you must clear the interrupt controller and RTC interrupt flag. Then, you must enable an RTC interrupt using the interrupt controller. This is required to inhibit unnecessary interrupts that may occur during change of settings.
You can change the Second, Minute, Hour, Day, Month and Year Counter register contents when the BUSY bit is logical 0. Because the repeated setting of this counter register completes instantaneously, you can complete this setting by checking the BUSY bit only once if you have disabled any interrupt of peripheral circuits during this time.

24.5.4 Repeated Setting during Operation after System Reset

If a system reset occurs when the RTC is operating, the operation continues without affecting on the RTC. (All registers in the RTC are not affected by the system reset.)
The RTC continues to operate without missing the RTCVDD signal (1.8V typical).

24.5.5 Cautions during Programming

- All registers in the RTC are unstable immediately after the power-On. Initialize the registers by following the procedure given in Section "24.5.1 Initialization after Power-On"
- If you reset the prescaler and the dividing timer, first stop the RTC from operating. Then, set bits 1 and 0 of RTC Run/Stop Control register (RTC[0x00]) to "0b10". You must set bit 1 to logical 1 and set bit 1 to logical 0. If the system is reset when the RTC is operating, this setting is made invalid.
- If you change the interrupt cause and alarm cause settings to prevent undesired interrupts, first disable the RTC interrupt using the interrupt controller. Also, before enabling the interrupts, be sure to clear the interrupt cause flag and the alarm cause flag.

25. WATCHDOG TIMER (WDT)

25.1 Description

The watchdog timer (WDT) is a system overrun monitoring unit, and it consists of 16-bit down counter whose value can be preset by the software. Counting down starts from the initially set value, and when the counter reaches zero (0), an interrupt request or a reset request is generated by following the settings of watchdog timer operation select bit (WDT[0x08], bit 4). The software periodically loads the preset data on the counter so that the counter does not reach zero (0). Therefore, if an interrupt request or a reset request occurs, it means that the program has failed to execute normally.
After the counter has reached 0, it returns to "0xFFFF". The counter value can be read by the software any time when desired. Note that the counter is set to "0xFFFF" when the system is reset or when the watchdog timer enable bit (WDT[0x08], bit 5) is set to logical 0. This counting is stopped if the watchdog timer enable bit is set to logical 0. The watchdog timer operates even in the HALT mode.
The watchdog timer uses the APB clock as the source clock. Because the watchdog timer has the built-in prescaler, this timer can control the dividing ratio of source clock and set the frequency of the count clock.

25.2 Block Diagram

The following shows a watchdog timer block diagram.
The watchdog timer consists of the register block (Read, Load and Control registers, the 16-bit Down counter, and the prescaler block having 11-bit Down counter.

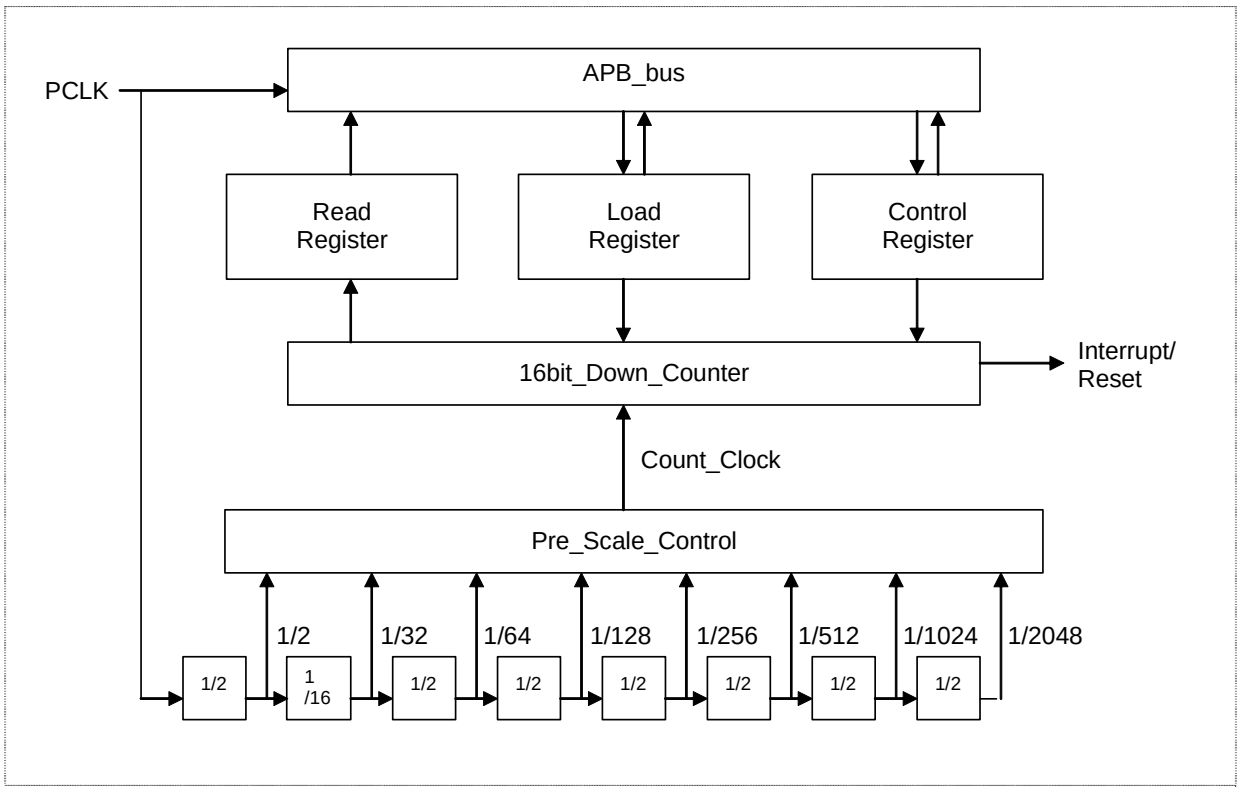


Figure 25.1 WDT Block Diagram

25.3 External Pins

There is no external pin that relates to the watchdog timer.

25.4 Registers

25.4.1 List of Registers

These registers have base address 0xFFFF_C000.

Table 25.1 List of Registers (Base Address: 0xFFFF_C000)

Address Offset	Register Name	Default Value	R/W	Data Access Size
0x00	Watchdog Timer Load register	0x0000_FFFF	R/W	16 (/32)
0x04	Watchdog Timer Count register	0x0000_FFFF	RO	16 (/32)
0x08	Watchdog Timer Control register	0x0000_0000	R/W	16 (/32)

25.4.2 Detailed Description of Registers

The Watchdog Timer Control registers have base address 0xFFFF_C000. If not reserved, all register bits are zeros (0s) unless otherwise noted.

Watchdog Timer Load Register

WDT[0x00] Default value = 0x0000_FFFF Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Timer load value															

Bits [15:0]: **Timer load value bits [15:0]**
If data is written here, it is loaded on the counter.

Watchdog Timer Count Register

WDT[0x04] Default value = 0x0000_FFFF Read Only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Current timer count value															

Bits [15:0]: **Current timer count value bits [15:0]**
The current counter value can be read.

Watchdog Timer Control Register

WDT[0x08] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (Fixed to A5h)								n/a	WDT status (RO)	WDT enable	WDT operation select	n/a	Prescaler dividing ratio		

Bits [15:8]: **Reserved**

Must always be 0xA5 during writing.

Bit 6: **Watchdog timer status (Read only)**

Indicates whether the counter has reached zero (0) or not.

0: The counter is not zero.

1: The counter is zero.

This bit is set to logical 1 when the counter reaches zero (0), and its status is kept. To clear this status, you must once set the watchdog timer enable bit (bit 5 of this register) to logical 0 so that the watchdog timer is reset.

Bit 5: **Watchdog timer enable**

Enables or disables the watchdog timer counting.

0 (r/w): Disables the timer.

If this bit is set to logical 0, the current counting is stopped. At the same time, the counter is reset to "0xFFFF" and the watchdog timer status bit (bit 6 of this register) is also reset to logical 0.

1 (r/w): Enables the timer.

When this bit is set to logical 1, the watchdog timer starts countdown.

Bit 4: **Watchdog timer operation**

Specifies an operation that starts when the counter reaches zero (0).

0 (r/w): Outputs a reset request signal.

When the counter reaches zero (0), the watchdog timer outputs a reset request signal (logical High WRST signal) to the system controller. The reset request signal returns to logical Low when the counter becomes a non-zero value.

1 (r/w): Outputs an interrupt request signal.

When the counter reaches zero (0), the watchdog timer outputs an interrupt request signal (logical High WINT signal). The interrupt request signal returns to logical Low when the watchdog timer enable bit (bit 5 of this register) is disabled.

Bits [2:0]: **Prescaler dividing ratio bits [2:0]**

Select a dividing ratio of the prescaler for count clock generation. The prescaler uses the APB clock as the source clock.

Bits [2:0]	Prescaler dividing ratio n*
000	2
001	32
010	64
011	128
100	256
101	512
110	1024
111	2048

*: Prescaler dividing ratio $n = 2$ ••• If Bits[2:0]=0

$= 2^{(4 + Bits[2:0])}$ ••• If Bits[2:0] are not equal to 0

The count clock frequency ("f" count clock) can be expressed using the APB system clock (PCLK) frequency (f PCLK) and the prescaler dividing ratio (n) as follows:

$$f_{count\ clock} = f_{PCLK} / n$$

26. GPIO

26.1 Description

This functional block consists of the GPIO function and the registers which are used to select pin functions multiplexed with GPIO pins.
This GPIO has the following features.

- Supports ten (10) 8-bit GPIO ports such as:
  GPIOA, GPIOB, GPIOC, GPIOD, GPIOE, GPIOF, GPIOG, GPIOH, GPIOJ, GPIOK
- Supports a single 2-bit GPIO port such as:
  GPIOI
- Allows changing the input or output direction of all GPIO pins separately.
- Some pins are multiplexed with other functions.
- Allows selecting the multi-function I/O pins using the Pin Function register.
- Supports the interrupt input function at GPIOA and GPIOB pins.
- Allows selecting an interrupt signal edge, its level, and logical High or Low polarity from GPIOA and GPIOB pins.

26.2 External Pins

The following defines the external pins relating to the GPIO.

Port	Pin Name	Input/Output	Pin Functions	Multiplex Pin/Remarks		
				Shared	Function 1	Function 2
A	GPIOA0	Input/Output	General-purpose I/O port A0 input/output		TXD1	
	GPIOA1	Input/Output	General-purpose I/O port A1 input/output		RXD1	
	GPIOA2	Input/Output	General-purpose I/O port A2 input/output		RTS1	I2S1_WS
	GPIOA3	Input/Output	General-purpose I/O port A3 input/output		CTS1	I2S1_SCK
	GPIOA4	Input/Output	General-purpose I/O port A4 input/output		TXD2	
	GPIOA5	Input/Output	General-purpose I/O port A5 input/output		RXD2	
	GPIOA6	Input/Output	General-purpose I/O port A6 input/output		RTS2	SCL
	GPIOA7	Input/Output	General-purpose I/O port A7 input/output		CTS2	SDA
B	GPIOB0	Input/Output	General-purpose I/O port B0 input/output	INT0	I2S0_WS	
	GPIOB1	Input/Output	General-purpose I/O port B1 input/output	INT1	I2S0_SCK	
	GPIOB2	Input/Output	General-purpose I/O port B2 input/output	INT2	I2S0_SD	
	GPIOB3	Input/Output	General-purpose I/O port B3 input/output	INT3	I2S1_SD	
	GPIOB4	Input/Output	General-purpose I/O port B4 input/output	INT4	TimerA0out	
	GPIOB5	Input/Output	General-purpose I/O port B5 input/output	INT5	TimerA1out	DREQ#
	GPIOB6	Input/Output	General-purpose I/O port B6 input/output	INT6	TimerA2out	
	GPIOB7	Input/Output	General-purpose I/O port B7 input/output	INT7	TimerBIn	
C	GPIOC0	Input/Output	General-purpose I/O port C0 input/output		TimerB0IO	
	GPIOC1	Input/Output	General-purpose I/O port C1 input/output		TimerB1IO	DACK#
	GPIOC2	Input/Output	General-purpose I/O port C2 input/output		TimerB2IO	CFRST
	GPIOC3	Input/Output	General-purpose I/O port C3 input/output		TimerB3IO	UART3_CLK
	GPIOC4	Input/Output	General-purpose I/O port C4 input/output		SPI_SS	TXD3
	GPIOC5	Input/Output	General-purpose I/O port C5 input/output		SPI_SCLK	RXD3
	GPIOC6	Input/Output	General-purpose I/O port C6 input/output		SPI_MISO	RTS3
	GPIOC7	Input/Output	General-purpose I/O port C7 input/output		SPI_MOSI	CTS3
D	GPIOD0	Input/Output	General-purpose I/O port D0 input/output		MA20	
	GPIOD1	Input/Output	General-purpose I/O port D1 input/output		MA21	
	GPIOD2	Input/Output	General-purpose I/O port D2 input/output		MA22	
	GPIOD3	Input/Output	General-purpose I/O port D3 input/output		MA23	
	GPIOD4	Input/Output	General-purpose I/O port D4 input/output		MCS2#	
	GPIOD5	Input/Output	General-purpose I/O port D5 input/output		MCS3#	
	GPIOD6	Input/Output	General-purpose I/O port D6 input/output		SDDQM2	
	GPIOD7	Input/Output	General-purpose I/O port D7 input/output		SDDQM3	
E	GPIOE0	Input/Output	General-purpose I/O port E0 input/output		CM1DATA0	IPC1DATA0
	GPIOE1	Input/Output	General-purpose I/O port E1 input/output		CM1DATA1	IPC1DATA1
	GPIOE2	Input/Output	General-purpose I/O port E2 input/output		CM1DATA2	IPC1DATA2
	GPIOE3	Input/Output	General-purpose I/O port E3 input/output		CM1DATA3	IPC1DATA3
	GPIOE4	Input/Output	General-purpose I/O port E4 input/output		CM1DATA4	IPC1DATA4
	GPIOE5	Input/Output	General-purpose I/O port E5 input/output		CM1DATA5	IPC1DATA5
	GPIOE6	Input/Output	General-purpose I/O port E6 input/output		CM1DATA6	IPC1DATA6
	GPIOE7	Input/Output	General-purpose I/O port E7 input/output		CM1DATA7	IPC1DATA7
F	GPIOF0	Input/Output	General-purpose I/O port F0 input/output		CM1VREF	IPC1VREF
	GPIOF1	Input/Output	General-purpose I/O port F1 input/output		CM1HREF	IPC1HREF
	GPIOF2	Input/Output	General-purpose I/O port F2 input/output		CM1CLKOUT	IPC1FIELD
	GPIOF3	Input/Output	General-purpose I/O port F3 input/output		CM1CLKIN	IPC1CLKIN
	GPIOF4	Input/Output	General-purpose I/O port F4 input/output		CM2VREF	IPC2VREF
	GPIOF5	Input/Output	General-purpose I/O port F5 input/output		CM2HREF	IPC2HREF
	GPIOF6	Input/Output	General-purpose I/O port F6 input/output		CM2CLKOUT	IPC2FIELD
	GPIOF7	Input/Output	General-purpose I/O port F7 input/output		CM2CLKIN	IPC2CLKIN

Port	Pin Name	Input/Output	Pin Functions	Multiplex Pin/Remarks		
				Shared	Function 1	Function 2
G	GPIOG0	Input/Output	General-purpose I/O port G0 input/output		CM2DATA0	IPC2DATA0
	GPIOG1	Input/Output	General-purpose I/O port G1 input/output		CM2DATA1	IPC2DATA1
	GPIOG2	Input/Output	General-purpose I/O port G2 input/output		CM2DATA2	IPC2DATA2
	GPIOG3	Input/Output	General-purpose I/O port G3 input/output		CM2DATA3	IPC2DATA3
	GPIOG4	Input/Output	General-purpose I/O port G4 input/output		CM2DATA4	IPC2DATA4
	GPIOG5	Input/Output	General-purpose I/O port G5 input/output		CM2DATA5	IPC2DATA5
	GPIOG6	Input/Output	General-purpose I/O port G6 input/output		CM2DATA6	IPC2DATA6
	GPIOG7	Input/Output	General-purpose I/O port G7 input/output		CM2DATA7	IPC2DATA7
H	GPIOH0	Input/Output	General-purpose I/O port H0 input/output		CFCE2#	SDMDATA0
	GPIOH1	Input/Output	General-purpose I/O port H1 input/output		CFCE1#	SDMDATA1
	GPIOH2	Input/Output	General-purpose I/O port H2 input/output		CFIORD#	SDMDATA2
	GPIOH3	Input/Output	General-purpose I/O port H3 input/output		CFIOWR#	SDMDATA3
	GPIOH4	Input/Output	General-purpose I/O port H4 input/output		CFWAIT#	SDMCMD
	GPIOH5	Input/Output	General-purpose I/O port H5 input/output		CFRST	SDMCLK
	GPIOH6	Input/Output	General-purpose I/O port H6 input/output		CFIRQ	SDMCD#
	GPIOH7	Input/Output	General-purpose I/O port H7 input/output		CFSTSCHG#	SDMWP
I	GPIOI0	Input/Output	General-purpose I/O port I0 input/output		CFDEN#	SDMGPO
	GPIOI1	Input/Output	General-purpose I/O port I1 input/output		CFDDIR	
J	GPIOJ0	Input/Output	General-purpose I/O port J0 input/output		SDD16	
	GPIOJ1	Input/Output	General-purpose I/O port J1 input/output		SDD17	
	GPIOJ2	Input/Output	General-purpose I/O port J2 input/output		SDD18	
	GPIOJ3	Input/Output	General-purpose I/O port J3 input/output		SDD19	
	GPIOJ4	Input/Output	General-purpose I/O port J4 input/output		SDD20	
	GPIOJ5	Input/Output	General-purpose I/O port J5 input/output		SDD21	
	GPIOJ6	Input/Output	General-purpose I/O port J6 input/output		SDD22	
	GPIOJ7	Input/Output	General-purpose I/O port J7 input/output		SDD23	
K	GPIOK0	Input/Output	General-purpose I/O port K0 input/output		SDD24	
	GPIOK1	Input/Output	General-purpose I/O port K1 input/output		SDD25	
	GPIOK2	Input/Output	General-purpose I/O port K2 input/output		SDD26	
	GPIOK3	Input/Output	General-purpose I/O port K3 input/output		SDD27	
	GPIOK4	Input/Output	General-purpose I/O port K4 input/output		SDD28	
	GPIOK5	Input/Output	General-purpose I/O port K5 input/output		SDD29	
	GPIOK6	Input/Output	General-purpose I/O port K6 input/output		SDD30	
	GPIOK7	Input/Output	General-purpose I/O port K7 input/output		SDD31	

26.3 Registers

26.3.1 List of Registers

These registers have base address 0xFFFF_1000.

Table 26.1 List of Registers (Base Address: 0xFFFF_1000)

Address Offset	Register Name	Abbreviation Name	Default Value	R/W	Data Access Size
0x00	GPIOA Data register	GPIOA_DATA	0x0000	R/W	8 (/16/32) *1
0x04	GPIOA Pin Function register	GPIOA_FNC	0x0000	R/W	16 (/32) *2
0x08	GPIOB Data register	GPIOB_DATA	0x0000	R/W	8 (/16/32) *1
0x0C	GPIOB Pin Function register	GPIOB_FNC	0x0000	R/W	16 (/32) *2
0x10	GPIOC Data register	GPIOC_DATA	0x0000	R/W	8 (/16/32) *1
0x14	GPIOC Pin Function register	GPIOC_FNC	0x0000	R/W	16 (/32) *2
0x18	GPIOD Data register	GPIOD_DATA	0x0000	R/W	8 (/16/32) *1
0x1C	GPIOD Pin Function register	GPIOD_FNC	0x0000	R/W	16 (/32) *2
0x20	GPIOE Data register	GPIOE_DATA	0x0000	R/W	8 (/16/32) *1
0x24	GPIOE Pin Function register	GPIOE_FNC	0x0000	R/W	16 (/32) *2
0x28	GPIOF Data register	GPIOF_DATA	0x0000	R/W	8 (/16/32) *1
0x2C	GPIOF Pin Function register	GPIOF_FNC	0x0000	R/W	16 (/32) *2
0x30	GPIOG Data register	GPIOG_DATA	0x0000	R/W	8 (/16/32) *1
0x34	GPIOG Pin Function register	GPIOG_FNC	0x0000	R/W	16 (/32) *2
0x38	GPIOH Data register	GPIOH_DATA	0x0000	R/W	8 (/16/32) *1
0x3C	GPIOH Pin Function register	GPIOH_FNC	0x0000	R/W	16 (/32) *2
0x40	GPIOI Data register	GPIOI_DATA	0x0000	R/W	8 (/16/32) *1
0x44	GPIOI Pin Function register	GPIOI_FNC	0x0000	R/W	16 (/32) *2
0x48	GPIOJ Data register	GPIOJ_DATA	0x0000	R/W	8 (/16/32) *1
0x4C	GPIOJ Pin Function register	GPIOJ_FNC	0x0000	R/W	16 (/32) *2
0x50	GPIOK Data register	GPIOK_DATA	0x0000	R/W	8 (/16/32) *1
0x54	GPIOK Pin Function register	GPIOK_FNC	0x0000	R/W	16 (/32) *2
0x58-5C	N/a				
0x60	GPIOA&B IRQ Type register	GPIOAB_ITYP	0x0000	R/W	16 (/32) *2
0x64	GPIOA&B IRQ Polarity register	GPIOAB_IPOL	0x0000	R/W	16 (/32) *2
0x68	GPIOA&B IRQ Enable register	GPIOAB_IEN	0x0000	R/W	16 (/32) *2
0x6C	GPIOA&B IRQ Status & Clear register	GPIOAB_ISTS	0x0000	R/W	16 (/32) *2

*1: Access to 8-, 16- or 32-bit data is enabled
*2: Access to 16- or 32-bit data is enabled

26.3.2 Detailed Description of Registers

26.3.2.1 GPIOA Registers

GPIOA Data Register (GPIOA_DATA)

GPIO[0x00] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
GPIOADATA [7:0]							

This is the GPIOA data register. The register is write and read enabled. If the GPIOA is set to output, the contents of this register are read. If GPIOA is set to input, the pin status can be read.

GPIOA Pin Function Register (GPIOA_FNC)

GPIO[0x04] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
GPA7MD [1:0]		GPA6MD [1:0]		GPA5MD [1:0]		GPA4MD [1:0]	
15	14	13	12	11	10	9	8
GPA3MD [1:0]		GPA2MD [1:0]		GPA1MD [1:0]		GPA0MD [1:0]	
7	6	5	4	3	2	1	0

Selects a GPIOA pin function. Two bits are used to select a pin function for each GPIOA port.

Table 26.2 Port-A Pin Select Function

GPAxMD1	GPAxMD0	Pin Function (“x” identifies the bit position on the port.)
0	0	GPIOAx port input (Default)
0	1	Function 1 other than GPIO
1	0	GPIOAx port output
1	1	Function 2 other than GPIO (Only GPIOA[7:6], [3:2] can be set.)

26.3.2.2 GPIOB Register

GPIOB Data Register (GPIOB_DATA)							
GPIO[0x08] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOBDATA [7:0]							
7	6	5	4	3	2	1	0

This is the GPIOB data register. Data can be written into and read from the register. If the GPIOB is set to output, data is read from the register. If set to input, the pin status can be read.

GPIOB Pin Function Register (GPIOB_FNC)							
GPIO[0x0C] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPB7MD [1:0]		GPB6MD [1:0]		GPB5MD [1:0]		GPB4MD [1:0]	
15	14	13	12	11	10	9	8
GPB3MD [1:0]		GPB2MD [1:0]		GPB1MD [1:0]		GPB0MD [1:0]	
7	6	5	4	3	2	1	0

Selects a GPIOB pin function. Two bits are used to select a pin function for each GPIOB port.

Table 26.3 Port-B Pin Select Function

GPBxMD1	GPBxMD0	Pin Function (“x” identifies the bit position on the port.)
0	0	GPIOBx port input (Default)
0	1	Function 1 other than GPIO
1	0	GPIOBx port output
1	1	Function 2 other than GPIO (Only GPIOB5 can be set.)

26.3.2.3 GPIOC Register

GPIOC Data Register (GPIOC_DATA)

GPIO[0x10] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
GPIOCDATA [7:0]							

This is the GPIOC data register. Data can be written into and read from the register. If the GPIOC is set to output, data is read from the register. If set to input, the pin status can be read.

GPIOC Pin Function Register (GPIOC_FNC)

GPIO[0x14] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
GPC7MD [1:0]		GPC6MD [1:0]		GPC5MD [1:0]		GPC4MD [1:0]	
15	14	13	12	11	10	9	8
GPC3MD [1:0]		GPC2MD [1:0]		GPC1MD [1:0]		GPC0MD [1:0]	
7	6	5	4	3	2	1	0

Selects a GPIOC pin function. Two bits are used to select a pin function for each GPIOC port.

Table 26.4 Port-C Pin Select Function

GPCxMD1	GPCxMD0	Pin Function (“x” identifies the bit position on the port.)
0	0	GPIOCx port input (Default)
0	1	Function 1 other than GPIO
1	0	GPIOCx port output
1	1	Function 2 other than GPIO (Only GPIOC[7:1] can be set.)

26.3.2.4 GPIOD Register

GPIOD Register (GPIOD_DATA)							
GPIO[0x18] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIODDATA [7:0]							
7	6	5	4	3	2	1	0

This is the GPIOD data register. Data can be written into and read from the register. If the GPIOD is set to output, data is read from the register. If set to input, the pin status can be read.

GPIOD Pin Function Register (GPIOD_FNC)							
GPIO[0x1C] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPD7MD [1:0]		GPD6MD [1:0]		GPD5MD [1:0]		GPD4MD [1:0]	
15	14	13	12	11	10	9	8
GPD3MD [1:0]		GPD2MD [1:0]		GPD1MD [1:0]		GPD0MD[1:0]	
7	6	5	4	3	2	1	0

Selects a GPIOD pin function. Two bits are used to select a pin function for each GPIOD port.

Table 26.5 Port-D Pin Select Function

GPDxMD1	GPDxMD0	Pin Function (“x” identifies the bit position on the port.)
0	0	GPIODx port input (Default)
0	1	Function 1 other than GPIO
1	0	GPIODx port output
1	1	Reserved

26.3.2.5 GPIOE Register

GPIOE Data Register (GPIOE_DATA)							
GPIO[0x20] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOEDATA [7:0]							
7	6	5	4	3	2	1	0

This is the GPIOE data register. Data can be written into and read from the register. If the GPIOE is set to output, data is read from the register. If set to input, the pin status can be read.

GPIOE Pin Function Register (GPIOE_FNC)							
GPIO[0x24] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPE7MD [1:0]		GPE6MD [1:0]		GPE5MD [1:0]		GPE4MD [1:0]	
15	14	13	12	11	10	9	8
GPE3MD [1:0]		GPE2MD [1:0]		GPE1MD [1:0]		GPE0MD [1:0]	
7	6	5	4	3	2	1	0

Selects a GPIOE pin function. Two bits are used to select a pin function for each GPIOE port.

Table 26.6 Port-E Pin Select Function

GPExMD1	GPExMD0	Pin Function (“x” identifies the bit position on the port.)
0	0	GPIOEx port input (Default)
0	1	Function 1 other than GPIO
1	0	GPIOEx port output
1	1	Function 2 other than GPIO

26.3.2.6 GPIOF Register

GPIOF Data Register (GPIOF_DATA)							
GPIO[0x28] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOFDATA [7:0]							
7	6	5	4	3	2	1	0

This is the GPIOF data register. Data can be written into and read from the register. If the GPIOF is set to output, data is read from the register. If set to input, the pin status can be read.

GPIOF Pin Function Register (GPIOF_FNC)							
GPIO[0x2C] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPF7MD [1:0]		GPF6MD [1:0]		GPF5MD [1:0]		GPF4MD [1:0]	
15	14	13	12	11	10	9	8
GPF3MD [1:0]		GPF2MD [1:0]		GPF1MD [1:0]		GPF0MD [1:0]	
7	6	5	4	3	2	1	0

Selects a GPIOF pin function. Two bits are used to select a pin function for each GPIOF port.

Table 26.7 Port-F Pin Select Function

GPFxMD1	GPFxMD0	Pin Function (“x” identifies the bit position on the port.)
0	0	GPIOFx port input (Default)
0	1	Function 1 other than GPIO
1	0	GPIOFx port output
1	1	Function 2 other than GPIO

26.3.2.7 GPIOG Register

GPIOG Data Register (GPIOG_DATA)							
GPIO[0x30] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOGDATA [7:0]							
7	6	5	4	3	2	1	0

This is the GPIOG data register. Data can be written into and read from the register. If the GPIOG is set to output, data is read from the register. If set to input, the pin status can be read.

GPIOG Pin Function Register (GPIOG_FNC)							
GPIO[0x34] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPG7MD [1:0]		GPG6MD [1:0]		GPG5MD [1:0]		GPG4MD [1:0]	
15	14	13	12	11	10	9	8
GPG3MD [1:0]		GPG2MD [1:0]		GPG1MD [1:0]		GPG0MD [1:0]	
7	6	5	4	3	2	1	0

Selects a GPIOG pin function. Two bits are used to select a pin function for each GPIOG port.

Table 26.8 Port-G Pin Select Function

GPGxMD1	GPGxMD0	Pin Function (“x” identifies the bit position on the port.)
0	0	GPIOGx port input (Default)
0	1	Function 1 other than GPIO
1	0	GPIOGx port output
1	1	Function 2 other than GPIO

26.3.2.8 GPIOH Register

GPIOH Data Register (GPIOH_DATA)							
GPIO[0x38] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOHDATA[7:0]							
7	6	5	4	3	2	1	0

This is the GPIOH data register. Data can be written into and read from the register. If the GPIOH is set to output, data is read from the register. If set to input, the pin status can be read.

GPIOH Pin Function Register (GPIOH_FNC)							
GPIO[0x3C] Default value = 0x0000_0000							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPH7MD [1:0]		GPH6MD [1:0]		GPH5MD [1:0]		GPH4MD [1:0]	
15	14	13	12	11	10	9	8
GPH3MD [1:0]		GPH2MD [1:0]		GPH1MD [1:0]		GPH0MD [1:0]	
7	6	5	4	3	2	1	0

Selects a GPIOH pin function. Two bits are used to select a pin function for each GPIOH port.

Table 26.9 Port-H Pin Select Function

GPHxMD1	GPHxMD0	Pin Functions
0	0	GPIOHx port input (Default)
0	1	Function 1 other than GPIO
1	0	GPIOHx port output
1	1	Function 2 other than GPIO

26.3.2.9 GPIOI Registers

GPIOI Data Register (GPIOI_DATA)

GPIO[0x40] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						GPIOIDATA[1:0]	

This is the GPIOI data register. Data can be written into and read from the register. If the GPIOI is set to output, data is read from the register. If set to input, the pin status can be read.

GPIOI Pin Function Register (GPIOI_FNC)

GPIO[0x44] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a				GPI1MD [1:0]		GPI0MD [1:0]	

Selects a GPIOI pin function. Two bits are used to select a pin function for each GPIOI port.

Table 26.10 Port-I Pin Select Function

GPIxMD1	GPIxMD0	Pin Functions
0	0	GPIOIx port input (Default)
0	1	Function 1 other than GPIO (Only GPIOI[1:0] can be set.)
1	0	GPIOIx port output
1	1	Function 2 other than GPIO (Only GPIO[0] can be set.)

26.3.2.10 GPIOJ Register

GPIOJ Data Register (GPIOJ_DATA)

GPIO[0x48] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
GPIOJDATA[7:0]							

This is the GPIOJ data register. Data can be written into and read from the register. If the GPIOJ is set to output, data is read from the register. If set to input, the pin status can be read.

GPIOJ Pin Function Register (GPIOJ_FNC)

GPIO[0x4C] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
GPJ7MD [1:0]		GPJ6MD [1:0]		GPJ5MD [1:0]		GPJ4MD [1:0]	
15	14	13	12	11	10	9	8
GPJ3MD [1:0]		GPJ2MD [1:0]		GPJ1MD [1:0]		GPJ0MD [1:0]	
7	6	5	4	3	2	1	0

Selects a GPIOJ pin function. Two bits are used to select a pin function for each GPIOJ port.

Table 26.11 Port-J Pin Select Function

GPJxMD1	GPJxMD0	Pin Functions
0	0	GPIOJ0 port input (Default)
0	1	Function 1 other than GPIO
1	0	GPIOJ0 port output
1	1	Reserved

26.3.2.11 GPIOK Register

GPIOK Data Register (GPIOK_DATA)

GPIO[0x50] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
GPIOKDATA[7:0]							

This is the GPIOK data register. Data can be written into and read from the register. If the GPIOK is set to output, data is read from the register. If set to input, the pin status can be read.

GPIOK Pin Function Register (GPIOK_FNC)

GPIO[0x54] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
GPK7MD [1:0]		GPK6MD [1:0]		GPK5MD [1:0]		GPK4MD [1:0]	
15	14	13	12	11	10	9	8
GPK3MD [1:0]		GPK2MD [1:0]		GPK1MD [1:0]		GPK0MD [1:0]	
7	6	5	4	3	2	1	0

Selects a GPIOK pin function. Two bits are used to select a pin function for each GPIOK port.

Table 26.12 Port-K Pin Select Function

GPKxMD1	GPKxMD0	Pin Functions
0	0	GPIOK0 port input (Default)
0	1	Function 1 other than GPIO
1	0	GPIOK0 port output
1	1	Reserved

GPIOA&B IRQ Registers

IRQ14 interrupt requests are set by GPIO[0x60] to GPIO[0x6C] registers as follows.

GPIOA&B IRQ TYPE

GPIOA&B IRQ Type Register (GPIOAB_ITYP)

GPIO[0x60] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PORTB_IRQ_TYPE [7:0]							
7	6	5	4	3	2	1	0
PORTA_IRQ_TYPE [7:0]							

Bits [15:8]: **PORTB_IRQ_TYPE**

Bits [7:0]: **PORTA_IRQ_TYPE**

Each bit can be set for level triggering or signal edge interruption as follows.

0: Uses an interrupt request as a level trigger signal.

1: Uses an interrupt as a signal edge for detection.

GPIOA&B IRQ Polarity

GPIOA&B IRQ Polarity Register (GPIOAB_IPOL)

GPIO[0x64] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PORTB_IRQ_POL [7:0]							
7	6	5	4	3	2	1	0
PORTA_IRQ_POL [7:0]							

Bits [15:8]: **PORTB_IRQ_POL**

Bits [7:0]: **PORTA_IRQ_POL**

0: Considers a logical High level as an interrupt request if the level signal of interrupt request is used. If the signal edge of interrupt request is used, a rising edge of signal is considered as an interrupt request.

1: Considers a logical Low level as an interrupt request if the level signal of interrupt request is used. If the signal edge of interrupt request is used, a falling edge of signal is considered as an interrupt request.

GPIOA&B IRQ ENABLE

GPIOA&B IRQ Enable Register (GPIOAB_IEN)

GPIO[0x68] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PORTB_IEN [7:0]							
7	6	5	4	3	2	1	0
PORTA_IEN [7:0]							

Bits [15:8]: **PORTB_IEN[7:0]**

These bits correspond to PORTB[7:0] bits for interrupt enable/disable setting.

0: Disables an interrupt from GPIOB.

1: Enables an interrupt from GPIOB.

Bits [7:0]: **PORTA_IEN[7:0]**

These bits correspond to PORTA[7:0] bits for interrupt enable/disable setting.

0: Disables an interrupt from GPIOA.

1: Enables an interrupt from GPIOA.

GPIOA&B IRQ STATUS & Clear

GPIOA&B IRQ Status & Clear Register (GPIOAB_ISTS)

GPIO[0x6C] Default value = 0x0000_0000 Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PORTB_IRQ [7:0]							
7	6	5	4	3	2	1	0
PORTA_IRQ [7:0]							

Bits [15:8]: **PORTB_IRQ[7:0]**

These bits correspond to PORTB[7:0] bits for interrupt status display and clearing.

[Read]

0: No interrupt request has been issued.

1: An interrupt request has been issued.

[Write]

0: No status changes.

1: The interrupt request cause is cleared if logical 1 is written.

Bits [7:0]: **PORTA_IRQ[7:0]**

These bits correspond to PORTA[7:0] bits for interrupt status display and clearing.

[Read]

0: No interrupt request has been issued.

1: An interrupt request has been issued.

[Write]

0: No status changes.

1: The interrupt request cause is cleared if logical 1 is written.

Note: The interrupt requests of these bits from GPIOA and GPIOB pins are "logically ORed" and posted to the controller. Therefore, the port where the interrupt request has been generated must be determined within the GPIO IRQ handler using the software.

26.4 GPIOA and GPIOB Interrupt Logic

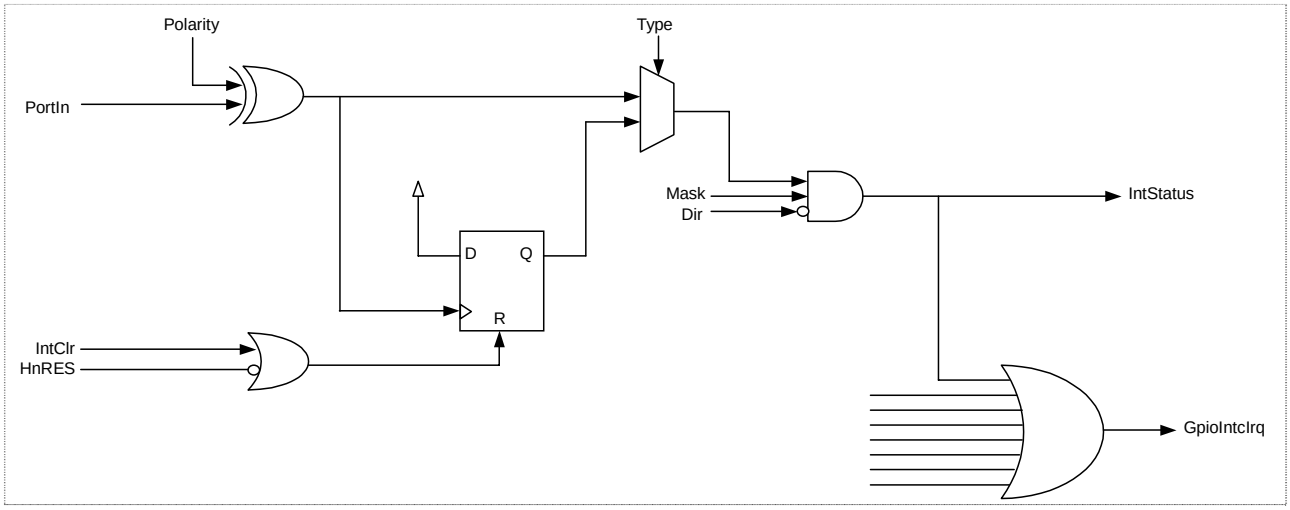


Figure 26.1 GPIOA and GPIOB Interrupt Logic

Note: If the interrupt type or its signal polarity is changed, a false interrupt may be inserted. To avoid this problem, be sure to clear the interrupt cause before use if you have changed the interrupt type or its signal polarity.

27. A/D CONTROLLER (ADC)

27.1 Description

When an 8-pin analog signal (ADIN[7:0]) is entered in the circuit, the built-in 10-bit ADC converts the analog signal into digital form, and the digital signal is output. This device also has the A/D converter controller (called the ADC).
Analog input voltage can be from 0 to 3.3 volts, and the signal at 8 channels can be sampled continuously.
The time of single A/D conversion is 20 µsec or less (when system clock sets about 49MHz), and an interrupt can be generated at the completion of signal conversion.

27.2 Block Diagram

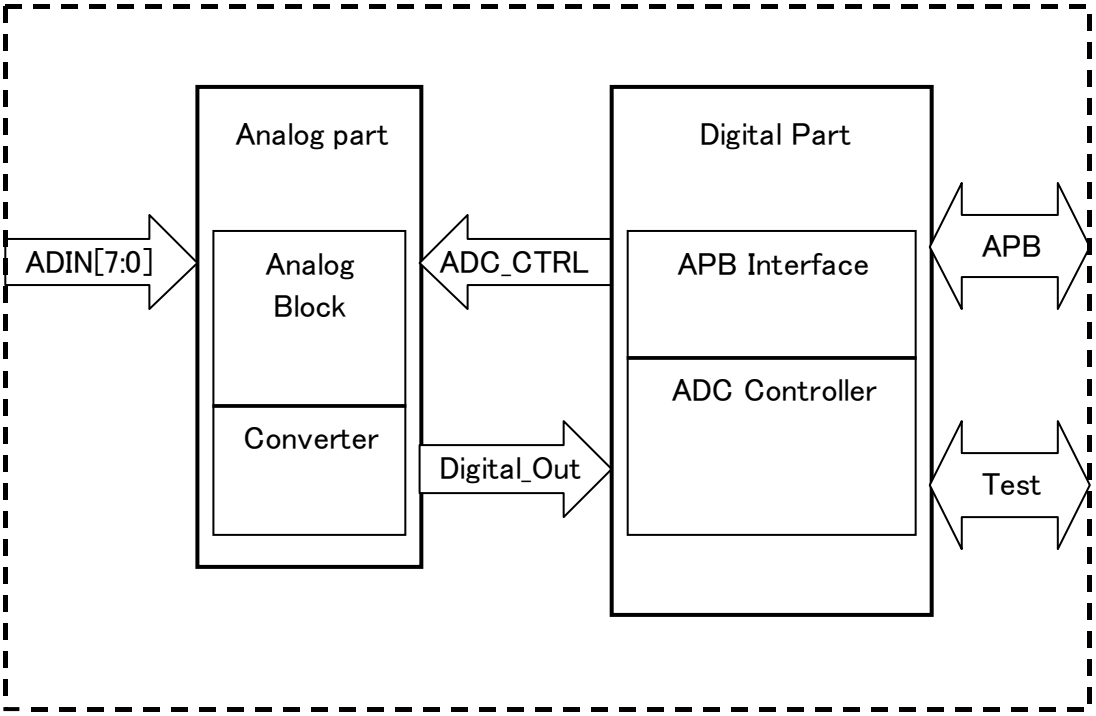


Figure 27.1 ADC Block Diagram

27.3 External Pins

The following defines the external pins that relate to the ADC.

Table 27.1 External Pins (CF)

Pin Name	Input/Output	Pin Functions	Multiplex Pin/Remarks
ADIN[7:0]	Input	Analog signal input and output	

27.4 Operation State

The ADC operates in the following state.

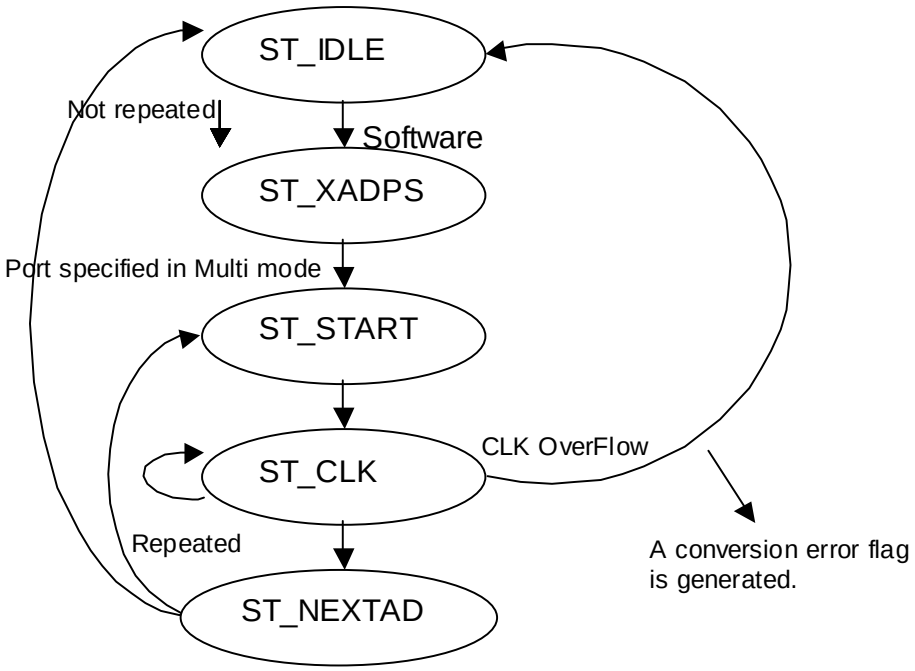


Figure 27.2 ADC Operation State

ST_IDLE : This is the initial status.
This status is kept until an input by the software occurs.

ST_XADPS : Activates the XADPS signal to start the A/D conversion.
The A/D power is turned ON in this state.

ST_START : Activates the START signal.

ST_CLK : The A/D conversion is executed in this state.
The A/D conversion takes a certain time. However, if it exceeds this time, this state may return to the ST_IDLS state due to the error. It it has occurred, bit 3 of ADC Flag register is set to logical 1. (During this time, the A/D conversion result is unreliable.)
If the Single port is used, the operation state returns to ST_IDLE after the A/D conversion.

ST_NEXTAD : If the A/D conversion is specified for multiple ports and if all of A/D conversions are not complete, the operation state returns to ST_START and the A/D conversion is restarted.
When the A/D conversion is complete at all of multiple ports, the operation state returns to the ST_IDLE.

27.5 Registers

27.5.1 List of Registers

The ADC registers have base address 0xFFFD_C000.

Table 27.2 List of Registers (Base Address: 0xFFFD_C000)

Address Offset	Register Name	Abbreviation Name	Default Value	R/W	Data Access Size
0x00	ADC Data Register 0	ADCDT0	0x0000	RO	16 (/32)
0x04	ADC Data Register 1	ADCDT1	0x0000	RO	16 (/32)
0x08	ADC Data Register 2	ADCDT2	0x0000	RO	16 (/32)
0x0C	ADC Data Register 3	ADCDT3	0x0000	RO	16 (/32)
0x10	ADC Data Register 4	ADCDT4	0x0000	RO	16 (/32)
0x14	ADC Data Register 5	ADCDT5	0x0000	RO	16 (/32)
0x18	ADC Data Register 6	ADCDT6	0x0000	RO	16 (/32)
0x1C	ADC Data Register 7	ADCDT7	0x0000	RO	16 (/32)
0x20	ADC Control Register	ADCCTL	0x00	R/W	8 (/16/32)
0x24	ADC Flag Register	ADCFLG	0x0000	R/W	16 (/32)

27.5.2 Detailed Description of Registers

ADC Data Register 0 (ADCDT0)

ADC[0x00] Default value = 0x0000 Read Only

15	14	13	12	11	10	9	8
Data 0 [9:2] RO							

7	6	5	4	3	2	1	0
Data 0 [1:0] RO		Reserved RO					

Bit [15:6]: **Data 0 [9:0]**

Channel 0 10-bit A/D conversion data [9:0]

The conversion result of channel 0 (analog input in ADIN0 pin) is read.

Bits [5:0]: **Reserved**

ADC Data Register 1 (ADCDT1)

ADC[0x04] Default value = 0x0000 Read Only

15	14	13	12	11	10	9	8
Data 1 [9:2] RO							

7	6	5	4	3	2	1	0
Data 1 [1:0] RO		Reserved RO					

Bit [15:6]: **Data 1 [9:0]**

Channel 1 10-bit A/D conversion data [9:0]

The conversion result of channel 1 (analog input in ADIN1 pin) is read.

Bits [5:0]: **Reserved**

ADC Data Register 2 (ADCDT2)

ADC[0x08] Default value = 0x0000 Read Only

15	14	13	12	11	10	9	8
Data 2 [9:2] RO							
Data 2 [1:0] RO		Reserved RO					
7	6	5	4	3	2	1	0

Bit [15:6]: **Data 2 [9:0]**

Channel 2 10-bit A/D conversion data [9:0]

The conversion result of channel 2 (analog input in ADIN2 pin) is read.

Bits [5:0]: **Reserved**

ADC Data Register 3 (ADCDT3)

ADC[0x0C] Default value = 0x0000 Read Only

15	14	13	12	11	10	9	8
Data 3 [9:2] RO							
Data 3 [1:0] RO		Reserved RO					
7	6	5	4	3	2	1	0

Bit [15:6]: **Data 3 [9:0]**

Channel 3 10-bit A/D conversion data [9:0]

The conversion result of channel 3 (analog input in ADIN3 pin) is read.

Bits [5:0]: **Reserved**

ADC Data Register 4 (ADCDT4)

ADC[0x10] Default value = 0x0000 Read Only

15	14	13	12	11	10	9	8
Data 4 [9:2] RO							
Data 4 [1:0] RO		Reserved RO					
7	6	5	4	3	2	1	0

Bit [15:6]: **Data 4 [9:0]**

Channel 4 10-bit A/D conversion data [9:0]

The conversion result of channel 4 (analog input in ADIN4 pin) is read.

Bits [5:0]: **Reserved**

ADC Data Register 5 (ADCDT5)

ADC[0x14] Default value = 0x0000 Read Only

15	14	13	12	11	10	9	8
Data 5 [9:2] RO							
Data 5 [1:0] RO		Reserved RO					
7	6	5	4	3	2	1	0

Bit [15:6]: **Data 5 [9:0]**

Channel 5 10-bit A/D conversion data [9:0]

The conversion result of channel 5 (analog input in ADIN5 pin) is read.

Bits [5:0]: **Reserved**

ADC Data Register 6 (ADCDT6)

ADC[0x18] Default value = 0x0000 Read Only

15	14	13	12	11	10	9	8
Data 6 [9:2] RO							
Data 6 [1:0] RO		Reserved RO					
7	6	5	4	3	2	1	0

Bit [15:6]: **Data 6 [9:0]**

Channel 6 10-bit A/D conversion data [9:0]

The conversion result of channel 6 (analog input in ADIN6 pin) is read.

Bits [5:0]: **Reserved**

ADC Data Register 7 (ADCDT7)

ADC[0x1C] Default value = 0x0000 Read Only

15	14	13	12	11	10	9	8
Data 7 [9:2] RO							
Data 7 [1:0] RO		Reserved RO					
7	6	5	4	3	2	1	0

Bit [15:6]: **Data 7 [9:0]**

Channel 7 10-bit A/D conversion data [9:0]

The conversion result of channel 7 (analog input in ADIN7 pin) is read.

Bits [5:0]: **Reserved**

ADC Control Register (ADCCTL)

ADC[0x20] Default value = 0x00 Read/Write

Reserved	ADCIEN	ADCSTT	ADCMLT	ADCEXT	ADCCH2	ADCCH1	ADCCH0
RW	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0

Bit 7: Reserved

Bit 6: **A/D interrupt enable**

Enables or disables an A/D conversion end interrupt.

0 (r/w): Disables the interrupt.

1 (r/w): Enables the interrupt.

This interrupt enable bit must always be set to logical 1. If you wish to suppress an interrupt, disable an interrupt of the interrupt control module.

Bit 5: **Starts A/D conversion.**

0 (r): Ends the A/D conversion.

1 (r/w): Starts the A/D conversion.

When the A/D conversion has completed on all of the specified channels, this bit automatically returns to logical 0.

The A/D conversion does not end even if this bit is set to logical 0 during A/D conversion.

If the A/D conversion does not end at the specified clock, the 0x24[3] bit may have been set to logical 1. You can check the error status by referring to this bit.

Bit 4: **Multi-mode select**

Selects an A/D conversion mode (Single mode or Multiple mode).

0 (r/w): Single mode

1 (r/w): Multiple mode

In the Single mode, the A/D conversion of only single-channel input occurs. In the Multiple mode, the A/D conversion is continued for the input of all channels. In both modes, you can switch the channel of input using the channel select bits (bits [2:0]).

Bit 3: **External trigger enable**

0: Disables an external trigger.

1: Enables an external trigger.

If this register is enabled, a falling edge of signal sent from Timer B is detected and the A/D conversion is triggered.

When a falling edge of signal from Timer B is detected during A/D conversion, the operation is stopped when the current conversion ends. You must restart the A/D conversion.

The signal sent from Timer B must be 1 μsec or longer.

Bit [2:0]: **Channel select bits [2:0]**

Selects a channel for A/D signal conversion. The options vary depending on the Single or Multiple mode selection.

Bits[2:0]	Functional Description	
CH[2:0]	Single Mode	Multi Mode
000	AN0	AN0
001	AN1	AN0-AN1
010	AN2	AN0AN2
011	AN3	AN0AN3
100	AN4	AN0-AN4
101	AN5	AN0-AN5
110	AN6	AN0-AN6
111	AN7	AN0-AN7

The A/D conversion can be triggered with a signal sent from Timer B if the external trigger enable bit is set to logical 1. Therefore, if you transfer the converted data to another place, we recommend you to detect an interrupt after A/D conversion and to read the data after the interrupt occurrence.
When the converted data is read, the End flag is set to logical 0. If the End flag is logical 1 and if another input is received from Timer B, the End flag is set to logical 1 and the next A/D conversion is started.
If data is transferred during its A/D conversion, the value is unreliable.

ADC Flag Register (ADCFLG)

ADC[0x24] Default value = 0x00 Read/Write

Reserved				ADCERR	ADCCNV	Reserved	
—	—	—	—			—	—
7	6	5	4	3	2	1	0

Bit [7:4]: **Reserved**

Bit 3: **ADCERR**

If an abnormality occurs during A/D conversion, this bit is set to logical 1.
The logical-1 bit means that the A/D conversion is not completed although the A/D conversion clock has been generated 15 times or more. Because the converted data is not written in the data register, the register value before the A/D conversion is read. However, if the A/D conversion is executed normally even if this flag has occurred, the data register value is updated correctly.
The logical-1 bit is set to 0 when the system is reset or when this bit is set to 1.

Bit 2: **ADCCNV**

Indicates that the A/D conversion has completed normally and the converted data has been stored in the data register.
In the Multiple mode, this bit shows that A/D conversion has completed on all of the specified channels and all data has been stored in the data register. To make this bit effective, you must enable the A/D interrupt of ADC[0x20], Bit 6.
The ADCCNV signal that is output from the Analog part is traced. When the A/D conversion has completed and when the Conversion End flag is output from the Analog part and the converted data is stored in the register, this bit is set to logical 1. When the A/D conversion is started again, this bit is returned to logical 0.
After AD convertion is finished, please read this regsiter at first. This register's value is cleared by reading ADC[0x00-0x1C] register and writing ADC[0x20] register.

Bit [1:0]: **Reserved**

27.6 Application Examples

- Single mode

  A single-channel analog input can be converted into digital form in the Single mode.
  When bit 5 of ADC Control register (called "ADC[0x20]" hereafter) is set to logical 1 by the software or by the external trigger input, A/D conversion of the specified channel data starts.
  The following explains the A/D conversion if only ADIN1 pin is used in the Single mode.

  1. Select the Single mode and enable an ADIN1 input and an interrupt (that is, set bits [7:0] of ADC[0x20] to 61h and start the A/D conversion).
  2. After the A/D conversion has completed, bit 7 of ADC[0x20] is set to logical 1 but bit 5 of ADC[0x20] is reset to logical 0. The next A/D conversion is waited. Then, the A/D conversion result is set in Data Register 1.
  3. If an ADC conversion interrupt is enabled by the interrupt controller, an interrupt is accepted after the A/D conversion. If you read data from Data Register 1 and set it in the interrupt process routine, you can read the A/D conversion result of ADIN1.
  4. After execution of interrupt process routine, you can start the next A/D conversion by setting bit 5 of ADC[0x20] to logical 1.

- Multiple mode

  The multiple-channel analog inputs (including the input of channel 1) can be converted into digital form sequentially in the Multiple mode.
  If you select the Multiple mode and set bits [2:0] of ADC[0x20] to "001", the A/D conversion of ADIN1 starts immediately after A/D conversion of ADIN0. The A/D conversion ends when analog data of all channels has been converted into digital data. The End flag (ADCFLG) is set to logical 1, and it shows that the data conversion has completed.
  The converted digital data is held in ADC Data registers of the respective channels.
  The following explains the A/D conversion if ADIN0, ADIN1 and ADIN2 pins are used in the Multiple mode.

  1. Select the Multiple mode and enable ADIN0, ADIN1 and ADIN2 inputs and an interrupt (that is, set bits [7:0] of ADC[0x20] to 72h and start A/D conversion).
  2. The ADIN0 analog data is first converted into digital form. After its conversion, the result is set in Data Register 0. Similarly, ADIN1 and ADIN2 analog data are converted sequentially, and the conversion results are set in the respective data registers. The last ADIN2 data is stored in registers only after the End flag has been set.
  3. After the ADIN2 data conversion has completed, bit 7 of ADC[0x20] is set to logical 1 but bit 5 of ADC[0x20] is reset to logical 0. The next A/D conversion is waited. Then, the A/D conversion result is set in Data Register 2.
  4. If an ADC conversion end interrupt is enabled by the interrupt controller, an interrupt is accepted after the A/D conversion. If you read data from Data Register 1, 2 or 3 and set it in the interrupt process routine, you can read the A/D conversion result of ADIN1, ADIN2 or ADIN3.
  5. After execution of interrupt process routine, you can start the next A/D conversion by setting bit 5 of ADC[0x20] to logical 1.

27.7 Input Voltages and Converted Data Values

The values listed below can be entered in ADC Data Registers 0 to 7 [15:0] using the input voltages.
This ADC can convert 10-bit analog data into digital form but it has an error within ±2 bits. Therefore, bits 15 to 8 of ADC Data Register [7:0] must be checked.

Input Voltage [V]	Conversion Reference Value	ADC Data Register0-7[15:0]		Remarks
		Min.	Max.	
0.0	0	0x00_00	0x00_C0	
0.3	0x5D	0x16_80	0x18_00	
0.6	0xB5	0x2D_C0	0x2F_40	
0.9	0x117	0x45_00	0x46_80	
1.2	0x1174	0x5C_40	0x5D_C0	
1.5	0x1D1	0x73_80	0x75_00	
1.8	0x22E	0x8A_C0	0x8C_40	
2.1	0x28B	0xA2_00	0xA3_80	
2.4	0x2E8	0xB9_40	0xBA_C0	
2.7	0x345	0xD0_80	0xD2_00	
3.0	0x3A2	0xE7_C0	0xE9_40	
3.3	0x3FF	0xFF_00	0xFF_C0	

28. AREA SENSOR (ARS)

28.1 Description

A screen image of YUV input signals sent from the camera I/F can be divided into 16 square partitions, and any of YUV components can be selected and each partition of signal components can be calculated and set in registers. If this calculation value is compared with the previous calculation value, a partial image movement can be detected in real-time mode without increasing the CPU load.

[An example of 2MB pixel camera (1632*1220 pixels)]
Although the calculated data width is 1632x1224x63/16 = 7865424 (decimal) = 780450 (hex) = 23 bits, the actual width is 21 bits because the calculation is made only once for 4 pixels of data.

Area 0	Area 1	Area 2	Area 3
Area 4	Area 5	Area 6	Area 7
Area 8	Area 9	Area 10	Area 11
Area 12	Area 13	Area 14	Area 15

Figure 28.1 Distribution of Image Partition Areas (Areas 0 to 15)

28.1.1 Functions

The Area Sensor (ARS) provides the following basic functions.

- Divides a picture image into 16 partitions, selects any of Y, U and V components in each partition, and calculates the components.
- Calculates data of 16 partitioned areas automatically according to the data size (H/V Sync).
- Can respond to the quick movement and slow movement because any calculation and comparison cycle is selectable.
- Allows to set a change ratio of calculation value and to generate an interrupt by detecting a change that exceeds the preset change ratio.
- Allows to determine a contrast change in a square partitioned area by reading data of status register.
- Can enable and clear an interrupt in each partitioned area separately.
- Can read the calculated value (21-bit data) and the magnitude relation data when compared with the previous frame in each area.
- Can switch between Camera 1 and Camera 2 using the registers.

28.2 Block Diagram

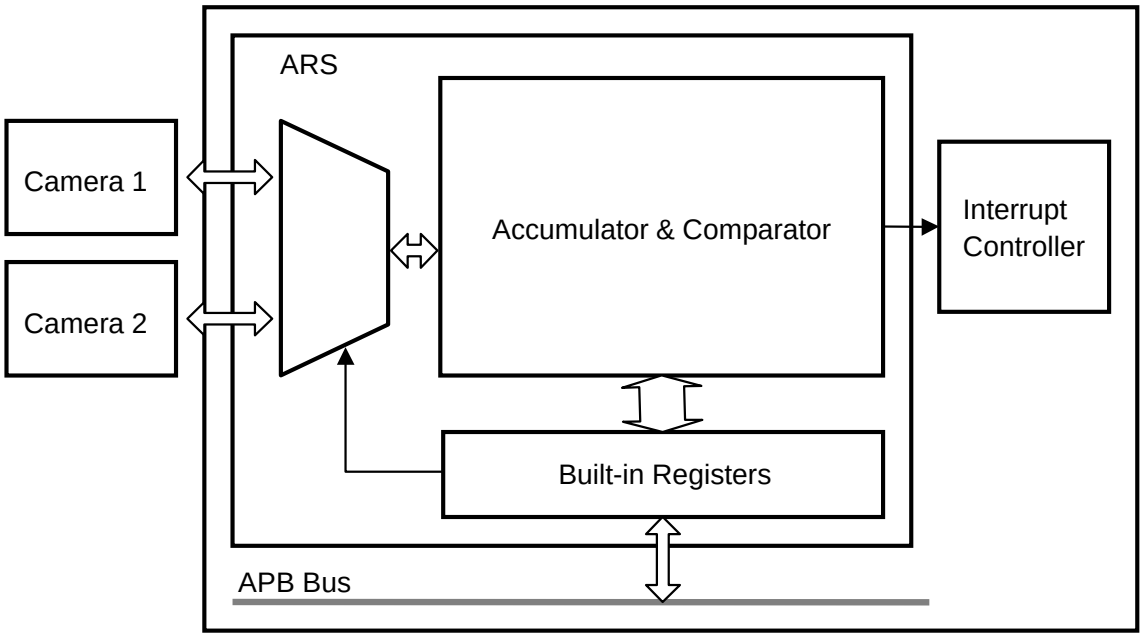


Figure 28.2 ARS Block Diagram

28.3 External Pins

There is no external pin that relates to the ARS. The internal camera input module supplies each camera input and clock.

28.4 Description of Registers

28.4.1 List of Registers

The ARS Control register locates at the default base address of 0xFFFE_7000.
Unless otherwise specified, all register bits are set to logical 0 by default if not reserved.

Table 28.1 ARS Register List

Address Offset	Register Name	Default Value	R/W	Data Access Size
ARS Control register Base address: 0xFFFE_7000				
0x00	ARS Control register (ARSCTRL)	0x0000_0080	R/W	32
0x04	ARS Area Select register (ARSASEL)	0x0000_0000	R/W	32
0x0C	ARS Status register (ARSSTAT)	0x0000_0000	R/W	32
0x10	ARS Interrupt Cause register (ARSINT)	0x0000_0000	R/W	32
0x40	ARS Accumulation register 0 (ARSADD0)	0x0000_0000	RO	32
0x44	ARS Accumulation register 1 (ARSADD1)	0x0000_0000	RO	32
0x48	ARS Accumulation register 2 (ARSADD2)	0x0000_0000	RO	32
0x4C	ARS Accumulation register 3 (ARSADD3)	0x0000_0000	RO	32
0x50	ARS Accumulation register 4 (ARSADD4)	0x0000_0000	RO	32
0x54	ARS Accumulation register 5 (ARSADD5)	0x0000_0000	RO	32
0x58	ARS Accumulation register 6 (ARSADD6)	0x0000_0000	RO	32
0x5C	ARS Accumulation register 7 (ARSADD7)	0x0000_0000	RO	32
0x60	ARS Accumulation register 8 (ARSADD8)	0x0000_0000	RO	32
0x64	ARS Accumulation register 9 (ARSADD9)	0x0000_0000	RO	32
0x68	ARS Accumulation register 10 (ARSADD10)	0x0000_0000	RO	32
0x6C	ARS Accumulation register 11 (ARSADD11)	0x0000_0000	RO	32
0x70	ARS Accumulation register 12 (ARSADD12)	0x0000_0000	RO	32
0x74	ARS Accumulation register 13 (ARSADD13)	0x0000_0000	RO	32
0x78	ARS Accumulation register 14 (ARSADD14)	0x0000_0000	RO	32
0x7C	ARS Accumulation register 15 (ARSADD15)	0x0000_0000	RO	32

28.4.2 Detailed Description of Registers

ARS Control Register

ARS[0x00] Default value = 0x0000_0080 Read/Write

SWRST (WO)	Reserved		ADDCYC (R/W)				
15	14	13	12	11	10	9	8
ADDOFF (RO)	CHGRATE (R/W)			CAMSEL (R/W)	YUVSEL (R/W)		ARSEN (R/W)
7	6	5	4	3	2	1	0

Bit 15: **SWRST Software Reset**

Allow to reset the area sensor module.

0: Nothing occurs.

1: Executes the reset by software.

Bits [14:13]: **(Reserved)**

Bits [12:8]: **ADDCYC Accumulation cycle set**

Sets a cycle for accumulation and comparison. The value set in this register is used to accumulate the YUV components of picture images, which are sent through camera interface, and to compare them with the previous value.

00000 : Does not accumulate. (Default)

00001 : Accumulates for each frame.

00010 : Accumulates for every two frames.

:

11111 : Accumulates for every 31 frames.

Bit 7: **ADDOFF Accumulation On/Off status display (Read Only)**

Shows the accumulation On/Off status. Refer to this register and make sure that the accumulation status is Off before reading the accumulated values and status register values.

0: Accumulation On (Default)
1: Accumulation Off

Bits [6:4]: **CHGRATE Change rate set**

If the accumulated value changes greater than the threshold, each status bit of the Status register (ARS[0x08]) is set to logical 1 and an interrupt is generated.

000: Approx. 1.5% (Default)
001: Approx. 3%
010: Approx. 6%
011: Approx. 13%
100: Approx. 25%
101: Approx. 50%
11x: (Reserved)

Bit 3: **CAMSEL Camera select**

Selects a camera input for accumulation.

0: Camera 0 (Default)
1: Camera 1

Bits [2:1]: **YUVSEL Accumulation element select**

Select the Y/U/V value to be accumulated.

00: Does not accumulate. (Default)
01: Accumulates Y values.
10: Accumulates U values.
11: Accumulates V values.

Bit 0: **ARSEN ARS enable**

Turns the ARS accumulation function On or Off. If this bit is set to logical 1, the accumulation starts at the next frame. Also, if this bit is set to logical 0, the ARS accumulation function is stopped after the current frame has ended.

0: Disables the ARS.
1: Enables the ARS.

ARS Area Select Register

ARS[0x04] Default value = 0x0000_0000 Read/Write

ASEL[15:8]							
15	14	13	12	11	10	9	8
ASEL[7:0]							
7	6	5	4	3	2	1	0

Bit[15:0]: **ASEL Area Select register**

Selects a change detection area or areas. (Multiple areas can be selected.) For the relationship between divided areas, see Figure 28.1 “Distribution of Split Areas”.

ARS Status Register

ARS[0x0C] Default value = 0x0000_0000 Read/Write

ARSSTAT [15:8]							
15	14	13	12	11	10	9	8
ARSSTAT[7:0]							
7	6	5	4	3	2	1	0

Bit[15:0]: **ARSSTAT Area status register**

Indicates a change exceeding the change ratio being set for each of divided areas.

0: No change occurs in the area.

1: A change occurred in the area.

This indication is cleared if each bit is set to logical 1.

ARS Interrupt Status Register

ARS[0x10] Default value = 0x0000_0000 Read/Write

ARSINT [15:8]							
15	14	13	12	11	10	9	8
ARSINT[7:0]							
7	6	5	4	3	2	1	0

Bits [15:0]: **ARSINT[15:0] ARS Interrupt Cause register**

Indicates that an interrupt cause exists or not in each of divided areas. The interrupt cause is cleared if each bit is set to logical 1.

ARS Accumulation Registers 0 to 15

ARS[0x40] to ARS[0x7C] Default value = 0000_0000 Read Only

GTO	(Reserved)										ADDV[20:16]				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDV[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit [31]: **GTO Accumulation Value Increment/Decrement register**

Indicates an increase or decrease of the current accumulation value when compared with the previous one.

0: Decreased

1: Increased

Bits [20:0]: **ADDV [20:0] Area accumulation value register**

Indicates the accumulated value of each area.

29. DMA CONTROLLER 3 (DMAC3)

29.1 Description

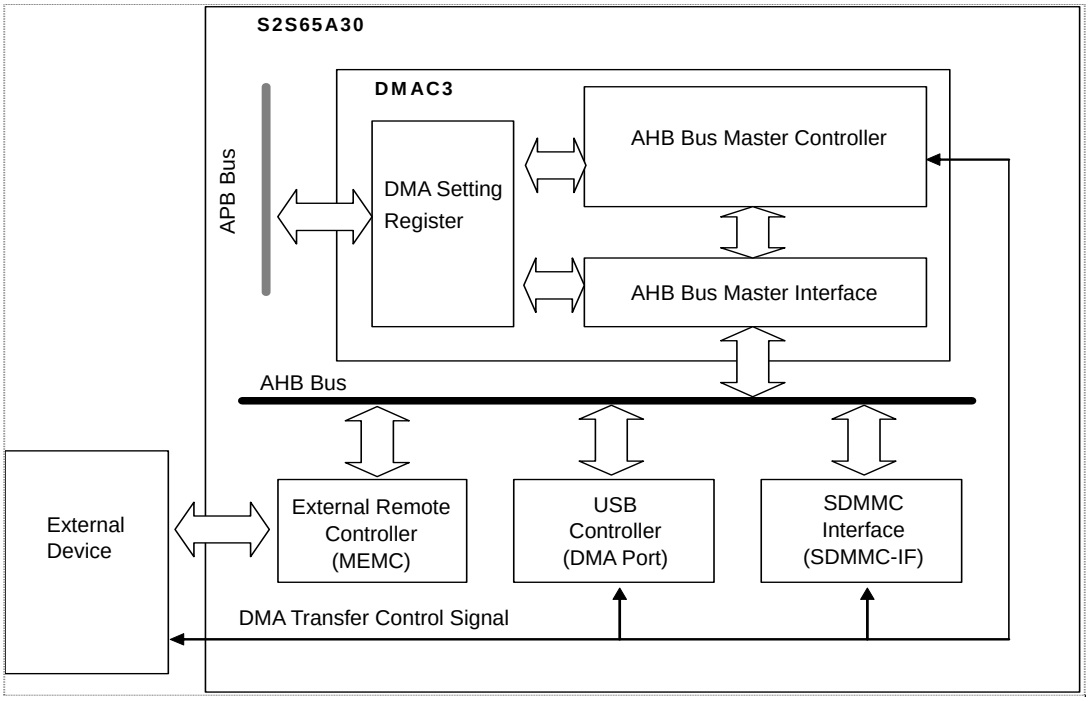
The DMA controller 3 in the S2S65A30 is provided for fast data transfer between external or memory devices that are connected to the built-in SDMMC interface, built-in USB 2.0 HS device controller and SRAM/SDRAM interface. It supports DMA transfer between I/O devices as well as allowing for optimal DMA transfer between devices of varying data access size.
It is also possible to perform a DMA transfer by using the external DREQ# and the external DACK# pins while the handshaking with external devices takes place.

29.1.1 Overview of Functions

The overview of the functions is as follows:

- Number of DMA transfer channels: One channel
- Supports memory-to-memory transfer, memory-to-I/O device transfer and I/O device-to-I/O device transfer.
- Allows the continuous transfer of 32-byte data for every request from an I/O device.
- Enables setting single/burst transfers for transfer source and destination.
- Supports data transfer sizes of 8, 16 and 32 bits.
- Supports transfers between devices with different transfer sizes.
- Free-running feature that ensures continuous transfers without setting transfer byte count.
- Contains a 2-byte transfer buffer.

29.2 Block Diagram



*Note that the I/O register areas (0xFFFD-0000 to 0xFFFF_FFFF) of the built-in device, FIFO of the JPEG controller 1/2 and the AHB area (0xD000_0000 to 0xEFFF_FFFF) of the line buffer cannot be accessed from the DMAC3.

29.3 External Pins

The external pins related to the DMA controller 3 are as follows.

Table 29.1 External Pins for DMA Controller 3

Pin Name	Input/Output	Pin functions	Multiplex Pin/Remarks*
DREQ#	I	External DMA request signal	GPIOB5, INT5, TimerA1Out
DACK#	O	External DMA response signal	GPIOC1, TimerB1IO

Note(*): These external pins are multiplexed with GPIO pins or other pins and can be used by setting "Function 2 other than GPIO" through the GPIO pin function register.

29.4 Register

29.4.1 List of Registers

The registers for DMA controller 3 are listed below. These registers have base address 0xFFFF_3000.

Table 29.2 List of Registers **(Base Address: 0xFFFF_3000)**

Address Offset	Register Name	Abbreviation	Initial Value	R/W	Data Access Size
DMA Controller 3 Registers					
0x00	DMAC3 Transfer Source Address Register	SADR	0x0000_0000	R/W	32
0x04	DMAC3 Transfer Destination Address Register	DADR	0x0000_0000	R/W	32
0x08	DMAC3 Transfer Byte Count Register	TBYTE	0x0000_0000	R/W	32
0x0C	DMAC3 Transfer Control Register	DCTRL	0x0000_0000	R/W	32
0x10	DMAC3 Operation Control Register	DOPSR	0x0000_0000	R/W	32
0x14 -	(Reserved)	—	0xXXXX_XXXX	R	—

29.4.2 Register Details

DMAC3 Transfer Source Address Register (SADR)

DMAC3[0x00] Default value = 0x0000_0000 Read/Write

SADR[31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADR[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [31:0]: **SADR[31:0]**

Specifies the DMA transfer souce adress.

This address must be adjusted to the transfer data size. For example, if the size of transfer source data is 32-bit, bits [1:0] of the register must be “00”.

In addition, the setting of this register is automatically updated to the next source address by hardware when the data transfer from the source has been completed.

* DMA controller 3 does not align the byte positions of the data transferred from the source with the destination address. Thus, the lower 2 bits of the destination address register (DADR) must be the same as the lower 2 bits of the source address register (SADR).

DMAC3 Transfer Destination Address Register (DADR)

DMAC3[0x04] Default value = 0x0000_0000 Read/Write

DADR[31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADR[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [31:0]: **DADR[31:0]**

Specifies the DMA transfer destination address.

This address must be adjusted to the transfer data size. For example, if the size of transfer the destination data is 32-bit, bits [1:0] of the register must be “00”.

In addition, the setting of this register is automatically updated to the next destination address by hardware when the data transfer to the destination has been completed.

* DMA controller 3 does not align the byte positions of the data transferred from the source with the destination address. Thus, the lower 2 bits of the destination address register (DADR) must be the same as the lower 2 bits of the source address register (SADR).

DMAC3 Transfer Byte Count Register (TBYTE)

DMAC3[0x08] Default value = 0x0000_0000 Read/Write

TBYTE[31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBYTE[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [31:0]: **TBYTE[31:0]**

Specifies the bite count for DMA transfer. The value of this register is automatically decremented by the hardware. It is updated when the reading of data from the source has been completed.

An interrupt at the end of DMA transfer occures when the value of this transfer byte count register is “0”. This register must not be set to “0” unless the counter operates in the free-running mode.

DMAC3 Transfer Control Register (DCTRL)

DMAC3[0x10] Default value = 0x0000_0000 Read/Write

DRS[1:0]		SRS[1:0]		DDRM	SDRM	ERP	LCK	(RSV)		EAW[1:0]		(RSV)		DAM	SAM
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
(RSV)				FRM	(RSV)	DTM	STM	DTS[1:0]		STS[1:0]		(RSV)	IE	TE	DE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [31:30]: **DRS[1:0] Transfer Destination Resouce Selection**

Selects the transfer destination DMA request resource.

- 00: USB2.0 HS device controller (Default value)
- 01: SDMMC controller
- 10: DREQ# external pins
- 11: Software request

Bits [29:28]: **SRS[1:0] Transfer Source Resource Selection**

Selects the transfer source DMA request resouce.

- 00: USB2.0 HS device controller (Default value)
- 01: SDMMC controller
- 10: DREQ# external pins
- 11: Software request

Bit 27: **DDRM Transfer Destination Request Mode**

Specifies the transfer destination DREQ mode.

- 0: Executes single word transfer for every transfer request (Default value).
- 1: Executes 32-byte transfer for every single transfer request.

Bit 26: **SDRM Transfer Source Request Mode**

Specifies the transfer source DREQ mode.

- 0: Executes single word transfer for every transfer request (Default value).
- 1: Executes 32-byte transfer for every single transfer request.

Bit 25: **ERP External DREQ Polarity Setting**

Specifies the polarity of the external DREQ# input and DACK# output pins.

- 0: External DREQ# and DACK# pins are low active (Default value).
- 1: External DREQ# and DACK# pins are High active.

Bits[24:22]: **Reserved (0)**

Bits[21:20]: **EAW[1:0] External DREQ Wait Setting**

Specifies the wait time from the time of output from external DACK# pin to the time of DMA request from DREQ# pin is accepted. The transfer request mode for the external devices that are set in bit 27 and bit 26 is “0”, the handshaking may not function properly due to the circuit for asynchronous data transfer. Use this register to insert a wait where necessary. For most external devices, a wait cycle is set by the memory controller (MEMC). As a result, this register needs not be set. Note that this register may need to be set for a device having longer count of cycles between the moment the S2S65A30 outputs a DACK# and the moment it drops a DREQ#. In addition, it does not need to be set when performing a DMA transfer without using the DACK# signal.

- 00: No wait cycle (Default value)
- 01: Inserts one wait cycle
- 10: Inserts two wait cycles.
- 01: Inserts three wait cycles.

Bits[19:18]: **Reserved (0)**

Bit 17: **DAM Transfer Destination Address Mode**

Specifies whether or not to increment the destination address for each transfer.
* Note the relationship between this setting and bit 9 (destination transfer mode). Whenever bit 9 (destination transfer mode) is set to "1" (incremental burst), always set this bit to "1".

0: Fixes the destination address (default value).
1: Increments the destination address.

Bit 16: **SAM Source Address Mode**

Specifies whether or not to increment the source address for each transfer.
* Note the relationship between this setting and bit 8 (source transfer mode). Whenever bit 9 (destination transfer mode) is set to "1" (incremental burst), always set this bit to "1".

0: Fixes the destination address (Default value).
1: Increments the destination address.

Bits[15:12]: **Reserved (0)**

Bit 11: **FRM Free-Running Mode**

Setting this bit to "1" causes the DMA controller 3 to execute DMA transfers in continuous mode regardless of the value of the transfer byte register. (No interrupt is generated when a transfer is completed.)

0: In normal mode (default value)
1: Free-Running Mode

Bit 10: **Reserved (0)**

Bit 9: **DTM Destination Transfer Mode**

Specifies the transfer mode of the destination. If burst transfer is enabled and the address is incremented, set this bit to "1".

0: Single transfer (Default value)
1: INCR (Incremental burst) transfer

Bit 8: **STM Source Transfer Mode**

Specifies the transfer mode of the source. If burst transfer is enabled and the address is incremented, set this bit to "1".

0: Single transfer (Default value)
1: INCR (Incremental burst) transfer

Bits [7:6]: **DTS [1:0] Transfer Size for Destination**

Specifies the size of data to be transferred to the destination. Selects the size appropriate for the destination device.

00: 8-bit (Default value)
01: 16-bit
10: 32-bit
11: Reserved

Bits [5:4]: **STS[1:0] Transfer Size for Source**

Specifies the size of data to be transferred from the source. Selects the size appropriate for the source device.

00: 8-bit (Default)
01: 16-bit
10: 32-bit
11: Reserved

Bit 3: **Reserved (0)**

Bit 2: **IE Interrupt Enable**

Enables or disables interrupts upon completion of the DMA transfer.

0: Disables interrupts (Default value).

1: Enables interrupts.

The TE bit (DMA transfer end bit) will not be set to "1" after DMA transfer has completed unless this bit is set to "1".

Bit 1: **TE DMA Transfer End**

This bit is set to "1" if the transfer byte counter reaches "0" as a result of DMA transfer. This bit also functions as an interrupt source flag. This bit is cleard by being set to "0".

0: Read: Transfer has not completed (Default value).

1: Read: Transfer has completed.

Bit 0: **DE DMA Transfer Enable**

Controls the start and stop of the DMA transfer.

0: Stops DMA transfer (Default value).

1: Enables DMA transfer.

This bit is automatically reset to "0". after the DMA transfer has completed in other than free-running mode.

DMAC3 Operation Control Register (DOPSR)

DMAC3[0x10] Default value = 0x0000_0000 Read/Write

(RSV)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
(RSV)															DGE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [31:1]: **Reserved (0)**

Bit 0: **DGE DMA Global Enable**

This bit enables the entire DMAC3 module. Writing a "0" to this bit during a DMA transfer will immediately interrupt the transfer. To return to the original state, it is required to issue a software reset for the system controller to reset the entire system. Usually, interrupt DMA transfers only by using the DMA transfer enable (DMAC3[0x0C]:Bit 0).

0: Disable the DMA module (Default value)

1: Enable the DMA module.

Reserved Register

DMAC3[0x14] Default value = 0xXXXX_XXXX - / -

RSV															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This is a reserved resister. Don't access this resister.

30. IP CONVERSION MODULE (IPC) [2:1]

30.1 Description

The IP (Interlaced-to-Progressive) conversion module that is contained in the S2S65A30 converts an interlaced (Interlaced Scan) image in the YUV422 format that is input through the camera interface to a progressive (Progressive Scan) image. An external SDRM is used as an image buffer for the IP conversion. The data is compressed to about 50% in the IP conversion module and is stored the data to SDRAM to reduce the memory area and bus bandwidth.
When reading image data from the SDRAM, compressed image data is decompressed and output as images in a progressive format (YUV422 format) to the camera interface for the JPEG controller that is contained in the S2S65A30.
In addition, the module incorporates aspect ratio adjustment and image correction functions.

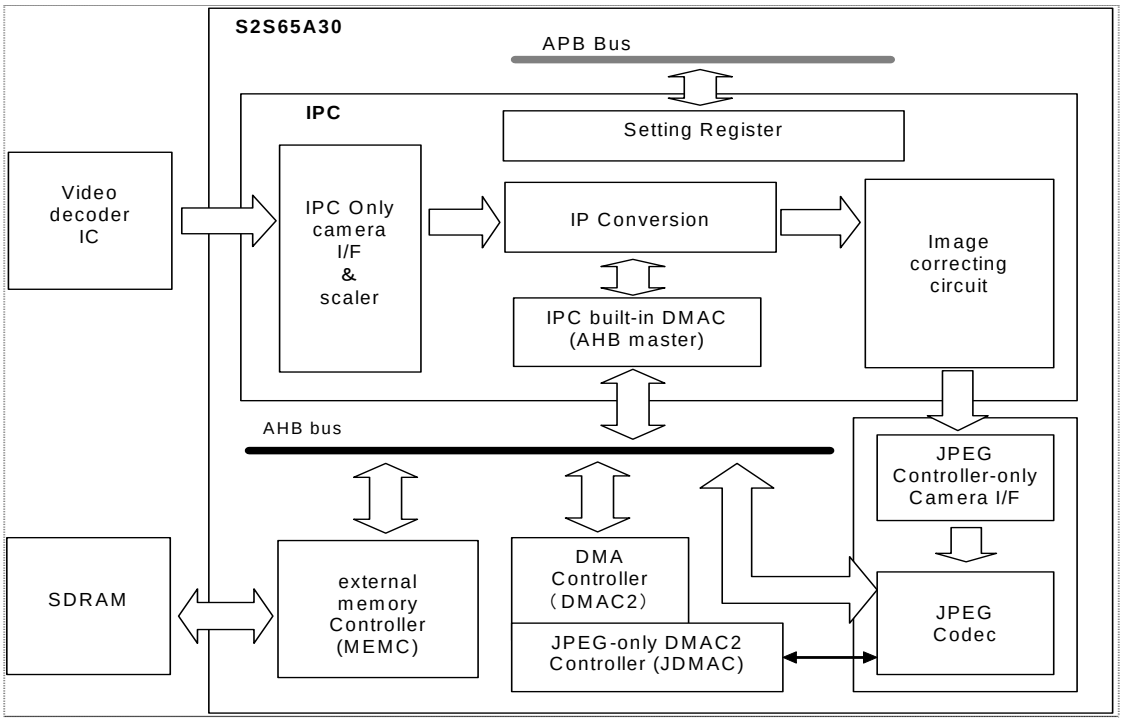
* It is possible to use only its image correction function without performing an IP conversion.

30.1.1 Overview of Functions

The overview of the functions is as follows:

- Allowable format: BT.601 with synchronous signals input /BT.656 formats (8-bit YUV422 format)
- Incorporates a scaler for aspect ratio adjustment
- IP conversion (Weave: Simple synthesis/Bob: Doubling, Interpolate: Linear interpolation)
- Uses an external SDRAM as an image buffer for the IP conversion
- Compresses image data to be storad in SDRAN approx. 50%
- Incorporates image correction function

30.2 Block Diagram



30.3 External Pins

The external pins related to the IP conversion module are as follows.

Table 30.1 List of External Pins related to the IP conversion

Pin Name	Input/Output	Pin functions	Multiplex Pin/Remarks*
IPC1VREF	I	IPC1 vertical sync signal input	CM1VREF, GPIOF0
IPC1HREF	I	IPC1 horizontal sync signal input	CM1HREF, GPIOF1
IPC1FIELD	I	IPC1 field signal input	CM1CLKOUT, GPIOF2
IPC1CLKIN	I	IPC1 clock input	CM1CLKIN, GPIOF3
IPC1DATA[7:0]	I	IPC1 Data Input (8-bit)	CM1DATA[7:0], GPIOE[7:0]
IPC2VREF	I	IPC2 vertical sync signal input	CM2VREF, GPIOF4
IPC2HREF	I	IPC2 horizontal sync signal input	CM2HREF, GPIOF5
IPC2FIELD	I	IPC2 field signal input	CM2CLKOUT, GPIOF6
IPC2CLKIN	I	IPC2 clock input	CM2CLKIN, GPIOF7
IPC2DATA[7:0]	I	IPC2 data input (8-bit)	CM2DATA[7:0], GPIOG[7:0]

Note (*): These external pins are multiplexed with GPIO pins or other pins and can be used by setting “Function 2 other than GPIO” through the GPIO pin function register.

30.4 Register

30.4.1 List of Registers

The registers for the IP conversion module [2:1] are listed below. These registers have base addresses IPC1:0xFFFE_1000 and IPC2:0xFFFD_1000.

Table 30.2 List of Registers **(Base Address: 0xFFF(E/D)_1000)**

Address Offset	Register Name	Abbreviation	Default value	R/W	Data Access Size
IPC Camera I/F Register (IPC1: 0xFFFE_1000 / IPC2: 0xFFFD_1000)					
0x000	IPC Camera Input Mode Setting	INMODE	0x0000	R/W	16/8bit
0x010	IPC Camera Input Setting	INCONFIG	0x0001	R/W	16/8bit
0x000-0FC	(Reserved)	—	—	—	—
IPC Input Timing Register (IPC1: 0xFFFE_1100 / IPC2: 0xFFFD_1100)					
0x108	IPC X-Direction Start Position Setting	XSTART	0x0001	R/W	16/8bit
0x10C	IPC Y-Direction Start Position Setting / Odd Field Y-Direction Start Position Setting	YSTART / YSTART_O	0x0001	R/W	16/8bit
0x110	IPC EVEN Field Y-Direction Start Position Setting	YSTART_E	0x0001	R/W	16/8bit
0x114	IPC Interrupt Setting	INTSEL	0x0000	R/W	16/8bit
0x118-0x1FC	(Reserved)	—	—	—	—
IPC Scaler Register (IPC1: 0xFFFE_1200 / IPC2: 0xFFFD_1200)					
0x200	IPC Scaler Setting	CONTROL	0x0001	R/W	16/8bit
0x204-3FC	(Reserved)	—	—	—	—
IPC Buffer Control Register (IPC1: 0xFFFE_1400 / IPC2: 0xFFFD_1400)					
0x400	IPC Conversion Buffer SDRAM Start Address 1	IPCBUF_SADR_L	0x0000	R/W	16bit
0x404	IPC Conversion Buffer SDRAM Start Address 2	IPCBUF_SADR_H	0x0000	R/W	16bit
0x408-0x4FC	(Reserved)	—	—	—	—

IPC Format Register (IPC1: 0xFFFE_1500 / IPC2: 0xFFFD_1500)					
0x500-50C	(Reserved)	—	—	—	—
0x510	IPC Video Output X-Direction Effective Pixels	VOUT_HD	0x0280	R(/W)	16bit
0x514-0x51C	(Reserved)	—	—	—	—
0x520	IPC Video Output X-Direction Length Setting	VOUT_HT	0x02DA	R(/W)	16bit
0x524-0x530	(Reserved)	—	—	—	—
0x534	IPC Video Output Vertical Blank Line Number	VOUT_VP	0x0001	R/W	16bit
0x538-0x53C	(Reserved)	—	—	—	—
0x540	IPC Video Output Y-Direction Effective Pixcels	VOUT_VD	0x01E0	R(/W)	16bit
0x544-0x6FC	(Reserved)	—	—	—	—
IPC Mode Register (IPC1: 0xFFFE_1700 / IPC2: 0xFFFD_1700)					
0x700	IPC Interlaced-to-Progressive Conversion Mode	IPC_MODE	0x0080	R/W	16/8bit
0x704-7FC	(Reserved)	—	—	—	—
IPC Output Control Register (IPC1: 0xFFFE_1800 / IPC2: 0xFFFD_1800)					
0x800	IPC Sync Signal Output Polarity Setting	OUTCONFIG	0x0003	R/W	16/8bit
0x804	IPC Image Correction Circuit Bypass Setting	BYPASS	0x0000	R/W	16/8bit
0x808	IPC Image Correction Setting Update Register	UPDATE	0x0000	R/W	16/8bit
0x80C-0x9FC	Correction Value Setting Register Area (Reserved)	—	—	—	16bit

30.4.2 Register Details

IPC Camera Input Mode Setup (INMODE)

IPC[0x000] Default value = 0x0000 Read/Write

(RSV)								EN	(RSV)				MODE[2:0]		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits[15:8]: **Reserved (0)**

Bit [7]: **EN Camera Input Enable**

Sets Enable/Disable of input image data to the IP conversion module.

0: Disabled (Default value)

1: Enabled

Bits[6:3]: **Reserved (0)**

Bits[2:0]: **MODE [2:0] Input Mode**

Sets the mode of imput image data to the IP conversion module.

* When using only the image correction function without using IP conversion function of IP conversion module, select VGA Progressive in this register.

000: NTSC (720) Interlaced Input 720 × 480 pixels (Default value)

001: NTSC (704) Interlaced input 704 × 480 pixels

010: PAL Interlaced input 720 × 576 pixels

100: VGA Progressive 640 × 480 pixels

Values other than the above: Cannot be set.

IPC Camera Input Setting (INCONFIG)

IPC[0x010] Default value = 0x0001 Read/Write

(RSV)									FORM[1:0]		ITU	ODDPOL	HSPOL	VSPOL	CKPOL
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits[15:7]: **Reserved (0)**

Bits [6:5]: **FORM [1:0] Input YUV Format**

Specifies input order of YUV data that are input to the IP conversion module.

00: U - Y0 - V - Y1(Default value)
01: V - Y0 - U - Y1
10: Y0 - U - Y1 - V
11: Y0 - U - Y1 - V

Bit [4]: **ITUSEL Input Standard Setting**

Specifies standard of the images that are input to the IP conversion module.

0: ITU-R BT601(Default value)
1: ITU-R BT656

Bit [3]: **ODDPOL Odd Field Select Signal Polarity Setting**

Specifies the polarity of the field signals (IPC1FIELD and IPC2FIELD) that are input to the IP conversion module. Sets the polarity of a field signal during odd fields. This bit is invalid if ITU-R BT656 is selected in INTSEL. In case of BT.656 is selected, Please do not connect any signals to IPC1FIELD/IPC2FIEDL pin, or plese set the IPC camera input enable register to "1" after set the GPIO module's pin function as GPIO input or output and this register to "1".

0: Low Active (Default value)
1: High Active

Bit [2]: **HSPOL Horizontal Sync Signal Polarity Setting**

Specifies the polarity of the HSYNC signals (IPC1HREF and IPC2HREF) that are input to the IP conversion module. This bit is invalid if ITU-R BT656 is selected in INTSEL. In case of BT.656 is selected, Please do not connect any signals to IPC1HREF/IPC2HREF pin, or plese set the IPC camera input enable register to "1" after set the GPIO module's pin function as GPIO input or output and this register to "1".

0: Low Active (Default value)
1: High Active

Bit [1]: **VSPOL Vertical Sync Signal Polarity Setting**

Specifies the polarity of the VSYNC signals (IPC1VREF and IPC2VREF) that are input to the IP conversion module. This bit is invalid if ITU-R BT656 is selected in INTSEL. In case of BT.656 is selected, Please do not connect any signals to IPC1VREF/IPC2VREF pin, or plese set the IPC camera input enable register to "1" after set the GPIO module's pin function as GPIO input or output and this register to "1".

0: Low Active (Default value)
1: High Active

Bit [0]: **CKPOL Clock Signal Polarity Setting**

Specifies the polarity of the image clock signals (IPC1CLKIN and IPC2CLKIN) that are input to the IP conversion module.

0: Operated by falling edge.
1: Operated by rising edge (Default value).

IPC Horizontal Direction Start Position Setting (XSTART)

IPC[0x108] Default value = 0x0001 Read/Write

(RSV)								XSTART[7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits[15:8]: **Reserved (0)**

Bits [7:0]: **XSTART[7:0] Horizontal Direction Start Position**

Specifies the start position of horizontal effective pixels.

For input effective pixels in the ITU-R BT.656 or similar mode, specifies the horizontal pixel position from which to start effective pixels.

IPC Vertical Direction Start Position Setting / Odd Frame Vertical Direction Start Position Setting (YSTART/YSTART_O)

IPC[0x10C] Default value = 0x0001 Read/Write

(RSV)								XSTART[7:0] / XSTASRT_O[7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits[15:8]: **Reserved (0)**

Bits [7:0]: **YSTART [7:0] Horizontal Direction Start Position**
/ YSTART_O [7:0] Odd Field Horizontal Direction Start Position

Specifies the start position of horizontal effective pixels. For input of image in an interlace format, specifies the start position of effective pixels in the odd fields.

For image input in ITU-R BT.656 or similar mode, specifies the vertical pixel position from which to start effective pixels.

IPC Even Frame Vertical Direction Start Position Setting (YSTART_E)

IPC[0x110] Default value = 0x0001 Read/Write

(RSV)								YSTART_E[7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits[15:8]: **Reserved (0)**

Bits [7:0]: **YSTART_E[7:0] Even Field Horizontal Start Position**

Specifies the start position of effective pixels in interlace input odd field. For image input in a progressive format, this register is invalid.

For image input in ITU-R BT.656 or similar mode, specifies the vertical pixel position from which to start effective pixels.

IPC Interrupt Setting (INTSEL)

IPC[0x114] Default value = 0x0000 Read/Write

(RSV)														HINT	VINT
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits[15:2]: **Reserved (0)**

Bit [1]: **HINT HSYNC Interrupt**

Interrupt can be generated from horizontal sync signal. In ITU-R BT601 mode, interrupt can be generated if the IPCxHREF pin (When Low Active Setting) changes its status from Low to High. In ITU-R BT656 mode, an interrupt is generated if an embedded horizontal sync signal bit changes its status from "1" to "0".

0: Interrupt inhibited (Default value)
1: Interrupt permitted.

Bit [0]: **VINT VSYNC Interrupt**

Interrupt can be generated from a vertical sync signal. In ITU-R BT601 mode, interrupt can be generated if the IPCxVREF pin (When Low Active Setting) changes its status from Low to High. In ITU-R BT656 mode, interrupt can be generated if an embedded vertical sync signal bit changes its status from "1" to "0".

0: Interrupt inhibited (Default value)
1: Interrupt permitted.

IPC Scaler Configuration (CONTROL)

IPC[0x200] Default value = 0x0001 Read/Write

(RSV)															SCLE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits[15:1]: **Reserved (Read: Undefined/Write: 0)**

Bit [0]: **SCLE Enable Scaler Circuit**

This bit controls enable or disable of the scaler circuit. The resister values must not be changed while set to "1".

0: Disables scaler curcuit
1: Enables scaler circuit (default value)

IPC Conversion Buffer SDRAM Start Address 1 (IPCBUF_SADR_L)

IPC[0x400] Default value = 0x0000 Read/Write

IPCBUF_SADR[15:2]														(RSV)	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

IPC Conversion Buffer SDRAM Start Address 2 (IPCBUF_SADR_H)

IPC[0x404] Default value = 0x0000 Read/Write

IPCBUF_SADR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

0x400 Bits [15:2] **IPCBUF_SADR[15:2] IP Conversion Buffer Start Address [15:2]**
0x404 Bits [15:0] **IPCBUF_SADR[31:16] IP Conversion Buffer Start Address [31:16]**

Specifies the start address of the SDRAM that is used as a buffer for the IP conversion. Do not set these bits in other than SDRAM area due to shortage of memory band with or capacity.

Allocate more than 467 Kbytes for the IP conversion buffer area for NTSC or allocate more than 671 Kbytes for the IP conversion buffer area for PAL in minimum, and allocate more than 778Kbytes for NTSC or allocate more than 1118Kbytes for PAL in case of video decoder output the signal, which is out of the standards, at the time of the change between video decoder's internal signal and camera's signal.

But it cannot estimate the allocation, in case of frequent switching between video decoder's internal signal and camera's signal or video decoder output many even frames in continuously, and then it is strongly

recommended to place this buffer area to the end of available SDRAM area (The attention is necessary for mirrored area of SDRAM, so allocates it to nearly 0x4FFF_FFFF or 0x5FFF_FFFF), to avoid confliction with the SDRAM area which is allocated for software related.

IPC Video Output X-Direction Valid Pixel (VOUT_HD)

IPC[0x510] Default value = 0x0280 (640d) NTSC / 0x0300 (768d) PAL Read/Write

(RSV)						HD[9:0]									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [15:10]: **Reserved (0)**

Bits [9:0]: **HD[9:0] Number of Output Horizontal Effective Pixels**

Specifies the number of horizontal (X) effective pixels of video output image data after IP conversion on a pixel basis. Usually, this register is read only, so use the default value .

IPC Video Output X-Direction Length (VOUT_HT)

IPC[0x520] Default value = 0x02DA (730d) NTSC / 0x035A (858) PAL Read/Write

(RSV)						HT[9:0]									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [15:10]: **Reserved (0)**

Bits [9:0]: **HD[9:0] Number of Output Horizontal Pixels**

Specifies the horizontal (X) length of video output image data after IP-conversion on a pixel basis. Be sure to specify the value that is set in VOUT_HD and added 0x5A(90d). Usually, this register is read only, so use the default value.

IPC Video Output Vertical Blank Line Number (VOUT_VP)

IPC[0x534] Default value = 0x0001 (1d) Read/Write

(RSV)										VP[5:0]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [15:6]: **Reserved (0)**

Bits [5:0]: **VP[9:0] Line Number of Vertical Blank**

Specifies the vertical blank of video output image data after IP-conversion on a line basis. In case of using interrupt function, which VREF goes active to inactive, of camera inetrface (Chapter 4 in S2S65A30 Technical Manual), interrupt processing may not be finished in time (until the start of next frame), so please set the value, which is enough to finish the interrupt processing, to this register.

Vertical blank interval is estimated by this expression.
[value of this register] x [IPC video output X-direction length] x [period of system clock] x 4
***The maximum value of this register is "0x0040" with NTSC camera, and if you set more than "0x0040", this module may not work normally, which is depending on frequency and period jitter of system clock and video input clock. This maximum value may be decreased by modification of VOUT_HD and VOUT_VD registers.**
This value cannot be increased with PAL camera. If you want to JPEG encoding every frame (25fps@PAL), you should do the ActAgain processing of RESIZER in JPEG controller within active frame period of IP-Converter's output, that is equal to input of camera interface (Chapter 7).

IPC Video Output Y-Direction Effective Pixels (VOUT_VD)

IPC[0x540] Default value = 0x01E0 (480d) NTSC / 0x0240 (576) PAL Read/Write

(RSV)						VD[9:0]									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [15:10]: **Reserved (0)**

Bits [9:0]: **VD[9:0] Number of Output Vertical Effective Pixels**

Specifies the number of vertical effective pixels of video output after IP conversion image data on a pixel basis. Usually, this register is read only, so use the default value .

IPC Interlace-to-Progressive Conversion Mode (IPC_MODE)

IPC[0x700] Default value = 0x0080 Read/Write

(RSV)								IPCE	(RSV)					MODE	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [15:8]: **Reserved (0)**

Bit [7]: **IPCE Enable IP Conversion Module**

Specifies Enable/Disable of the circuit for the IP conversion. This module must be set Enable even if the IP conversion is not performed (the image correction function is used via Progressive Scan).

0: Disables IP conversion circuit
1: Enables IP conversion circuit (Default value)

Bits [6:2]: **Reserved (0)**

Bits [1:0]: **MODE[1:0] IP Conversion Mode Selection**

Specifies the Interlaced-to-Progressive Conversion Mode.

00: Weave Mode: Simple synthesis (Default value)
01: Bob Mode: Doubling
10: Interpolation Mode: Linear Interpolation
11: Reserved

IPC Sync Signal Output Polarity Configuration (OUTCONFIG)

IPC[0x800] Default value = 0x0003 Read/Write

(RSV)														OPOL	HSEL
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [15:2]: **Reserved (0)**

Bit [1]: **OPOL Output Polarity Setting**

Specifies the polarity of the sync signal in an image output from the IP conversion circuit. Usually, use the default value of this bit and use the setting of the camera interface for the S2S65A Series JPEG controller that is connected to the subsequent stage in the IP conversion circuit based on the setting of this bit.

0: Positive logic
1: Negative logic (Default value)

Bit [0]: **HSEL Horizontal Sync Type Selection**

Specifies the type of the sync signal in an image output from the IP conversion circuit. Usually, use the default value of this bit and use the setting of the camera interface for the S2S65A Series JPEG controller that is connected to the subsequent stage in the IP conversion circuit based on the setting of this bit.

0: HSYNC output
1: Data valid (HVALID) output (Default value)

IPC Image Correction Circuit Bypass Setting (BYPASS)

IPC[0x804] Default value = 0x0000 Read/Write

(RSV)														BYPS	(RSV)
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [15:2]: **Reserved (0)**

Bit [1]: **BYPS Image Correction Circuit Bypass Setting**

Specifies whether to bypass the image correction circuit.

0: Uses image correction circuit (Default value).

1: Bypasses image correction circuit.

Bit [0]: **Reserved (0)**

IPC Image Correction Setting Update (UPDATE)

IPC[0x808] Default value = 0x0000 Read/Write

(RSV)														UPDATE[1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [15:2]: **Reserved (0)**

Bits [1:0]: **UPDATE[1:0] Image Correction Setting Update**

Sets “11” to update the image correction setting. The setting is reflected from the next frames.

00: Does not update (Default value)

01: Cannot be set

10: Cannot be set

11: Updates image correction setting.

Image Correction Setting Area

IPC [0x80C-9FC] Default value = 0xXXXX - / -

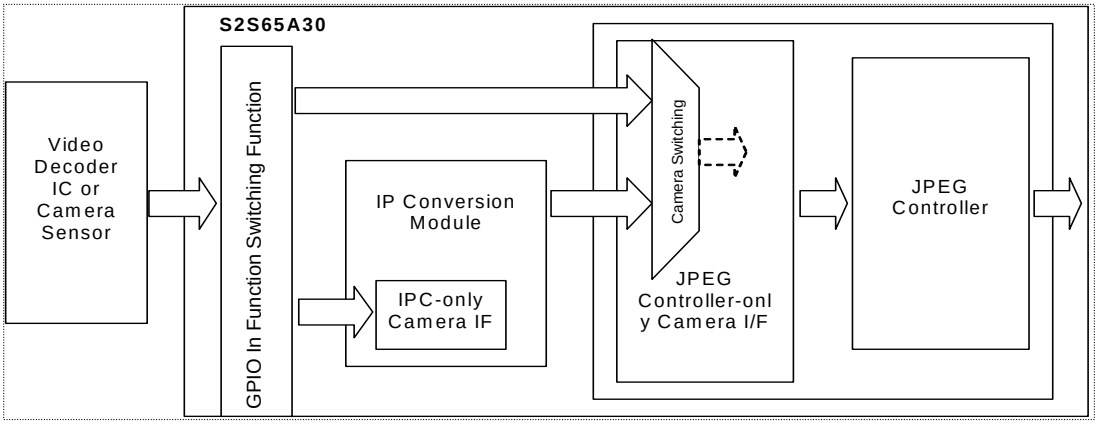
(RSV)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This is an Image Correction Setting Area.
The register of this area is accessible only via sample software.

30.5 Notes on Using the IP Conversion Circuit

30.5.1 Precautions

The IP conversion module [2:1] is inserted into a pre-stage of the camera interface for the JPEG encoder. Switching to S2S65A00-compatible functions is implemented by the GPIO pin switching and camera interfaces for the JPEG encoder. To use the IP conversion module, appropriately set the GPIO pin switching and the camera port switching in the camera interfaces for the JPEG encoder. To set the GPIO pin function, “Pin Function 2 other than GPI0” must be selected. To set the camera interfaces for the JPEG controller, “Camera input 2” must be selected.



30.5.2 Restrictions

The IP conversion circuit uses an external SDRAM as an image buffer for the IP conversion. The image data that is to be temporarily stored in the SDRAM is of an image in which YUV data is compressed to about 50% before JPEG compression is performed and, thus, takes up a large amount of bandwidth of the internal bus and of the SDRAM. Note that the following restrictions are posed when you use the IP conversion circuit.

[Limited Range]

A) There are limits on the system frequencies and the clock frequencies for images that are supplied to the IP conversion circuit.
B) The types of SDRAMs available and the settings of the memory controller (MEMC) are limited.
C) It is not possible to capture YUV data without performing JPEG image compression
D) , E) Certain types of DMA transfers that occupies memory areas or internal bus are limited.

		A) System Frequencies	B) Setting the types of SDRAM & MEMC	C) YUV Data Capture	D) and E) Restrictions on DMA Function
IP conversion Function	Use one channel only.	— (*)	— (**)	○	— (***)
	Use two channels.	○	○(**)	○	○(***)

○ The restrictions are applied.

(*) : The input clock of an image must be less than 2/3 of the system clock frequency.
(**) : The bus width of SDRAM must be 32 bits.
(***) : The access wait cycle of SRAM type external devices should be less than 13.

[Details of Restrictions]

A) The system frequency must be 50.00 MHz and the image input clock must be less than 27 MHz (typ.).

B) The SDRAM must support the settings given below. These settings must be made for the memory controller as well.
- ◆ CAS latency : Less than 2 cycles (CL=2 or CL=1)
- ◆ RAS-CAS delay : Less than 2 cycles

* In addition, the hold count of the auto-refresh for the memory controller (MEMC[0x74]-bits [11:8]) must be set to “0x1”.

C) It is not possible to capture images in a form of YUV data without JPEG encoding due to shortage of the bus bandwidth. (This causes due to overflow of the line buffer in the JPEG controller.)

D) The incremental burst transfer function (DMAC3[0x10]-Bits [9:8]) in the DMA controller 3 is not

available.

E) To perform DMA transfers between an external SRAM and an external I/O device via the memory controller (MEMC) using DMA controller 3, sets the access wait cycle of an external device to satisfy the reference values given below. Even if DMA controller 3 is not used, the access wait cycle (WAITRD+WAITRH or WAITWR+WAITWH) of external devices should be less than 13.

<1> The wait cycle setting for the SRAM device [3:0] timing register (MEMC[0x20, 0x30, 0x40, 0x50]) should be 6 or below cycles. Selects a value as small as possible.

(a) Read Setting : WAITRD + WAITRH ≤ 6

(b) Write Setting : WAITWR + WAITWH + 1 ≤ 6

<2> If the above requirements are not satisfied, use a value as small as possible so that the sum of wait cycles between a device that performs DMA transfers using DMA controller 3 and any other device that is below 12 cycles.

(c) Read Setting : $WAITRD_{(DMA+No\ DMA)} + WAITRH_{(DMA+\ No\ DMA)} \leq 12$

(d) Write Setting : $WAITRD_{(DMA+No\ DMA)} + WAITRH_{(DMA+\ No\ DMA)} + 1 \leq 12$

31. ABSOLUTE MAXIMUM RATINGS

31.1 Absolute Maximum Ratings

(VSS = 0 [V])

Item	Symbol	Rated Value	Unit
Power voltage	HVDD, UVDD3, C1VDD, C2VDD, SDVDD, AVDD	-0.3 to +4.0	V
	LVDD, UPVDD, UXVDD, RTCVDD, PLLVDD	-0.3 to +2.5	V
Input voltage	HVI	-0.3 to HVDD+0.5	V
	LVI	-0.3 to LVDD+0.5	V
	USBVDD	-0.3 to 6.0	V
Output voltage	HVO	-0.3 to HVDD+0.5	V
	LVO	-0.3 to LVDD+0.5	V
Output current/pin	I_{OUT}	± 10	mA
Storage temperature	T_{stg}	-65 to +150	°C

31.2 Recommended Operating Conditions (Dual Power Supplies, 3.3V I/O Buffers)

(UVSS = PVSS = XVSS = 0 [V]
VSS = PLLVSS = AVSS = 0 [V])

Item		Symbol	Min.	Typ.	Max.	Unit
Power voltage (High-voltage)	I/O cell power supply	HVDD	3.00	3.30	3.60	V
	USB power supply	UVDD3	3.00	3.30	3.60	V
	Camera-1 I/F power supply	C1VDD	2.40	3.00	3.60	V
	Camera-2 I/F power supply	C2VDD	2.40	3.00	3.60	V
	SDRAM I/F power supply	SDVDD	2.70	3.00	3.60	V
	A/D converter power supply	AVDD	3.00	3.30	3.60	V
Power voltage (Low-voltage)	(Internal) core power supply	LVDD	1.65	1.80	1.95	V
	USB power supply	UPVDD	1.65	1.80	1.95	V
	USB power supply	UXVDD	1.65	1.80	1.95	V
	Analog (PLL) power supply	PLLVDD	1.65	1.80	1.95	V
	RTC power supply	RTCVDD	1.65	1.80	1.95	V
Input voltage	I/O cell power supply	HV_I	VSS	—	HVDD	V
	USB power supply	$UV3_I$	UVSS	—	UVDD3	V
	Camera-1 I/F power supply	$C1V_I$	VSS	—	C1VDD	V
	Camera-2 I/F power supply	$C2V_I$	VSS	—	C2VDD	V
	SDRAM I/F power supply	SDV_I	VSS	—	SDVDD	V
	A/D converter power supply	AV_I	AVSS	—	AVDD	V
	(Internal) core power supply	LV_I	VSS	—	LVDD	V
	USB power supply	UPV_I	PVSS	—	UPVDD	V
	USB power supply	UXV_I	XVSS	—	UXVDD	V
	Analog (PLL) power supply	$PLLV_I$	PLLVSS	—	PLLVDD	V
	RTC power supply	$RTCV_I$	VSS	—	RTCVDD	V
Ambient temperature		Ta	-40	25	85*	°C
Input rise time (normal input)		t_{ri}	—	—	50	ns
Input fall time (normal input)		t_{fa}	—	—	50	ns
Input rise time (Schmitt input)		t_{ri}	—	—	5	ms
Input fall time (Schmitt input)		t_{fa}	—	—	5	ms

*: This temperature range is the recommended ambient temperature range if Tj=-40 to 125°C.

31.3 Power-ON Timing

The 3.3V power supply (HVDD) and 1.8V power supply (LVDD) must be turned On in the following sequence.

(1) After turning on a power supply, turn on the other in a second. We recommend you to reduce this delay as much as possible and turn On 1.8V power supply at first. And in case of only HVDD power is supplied, your system will be unstable. Please design your system so as not to cause malfunction by this unstable situation.

(2) After the HVDD and LVDD signals have become stable, keep the RESET# signal in logical Low more than the 32KHz oscillation start time.

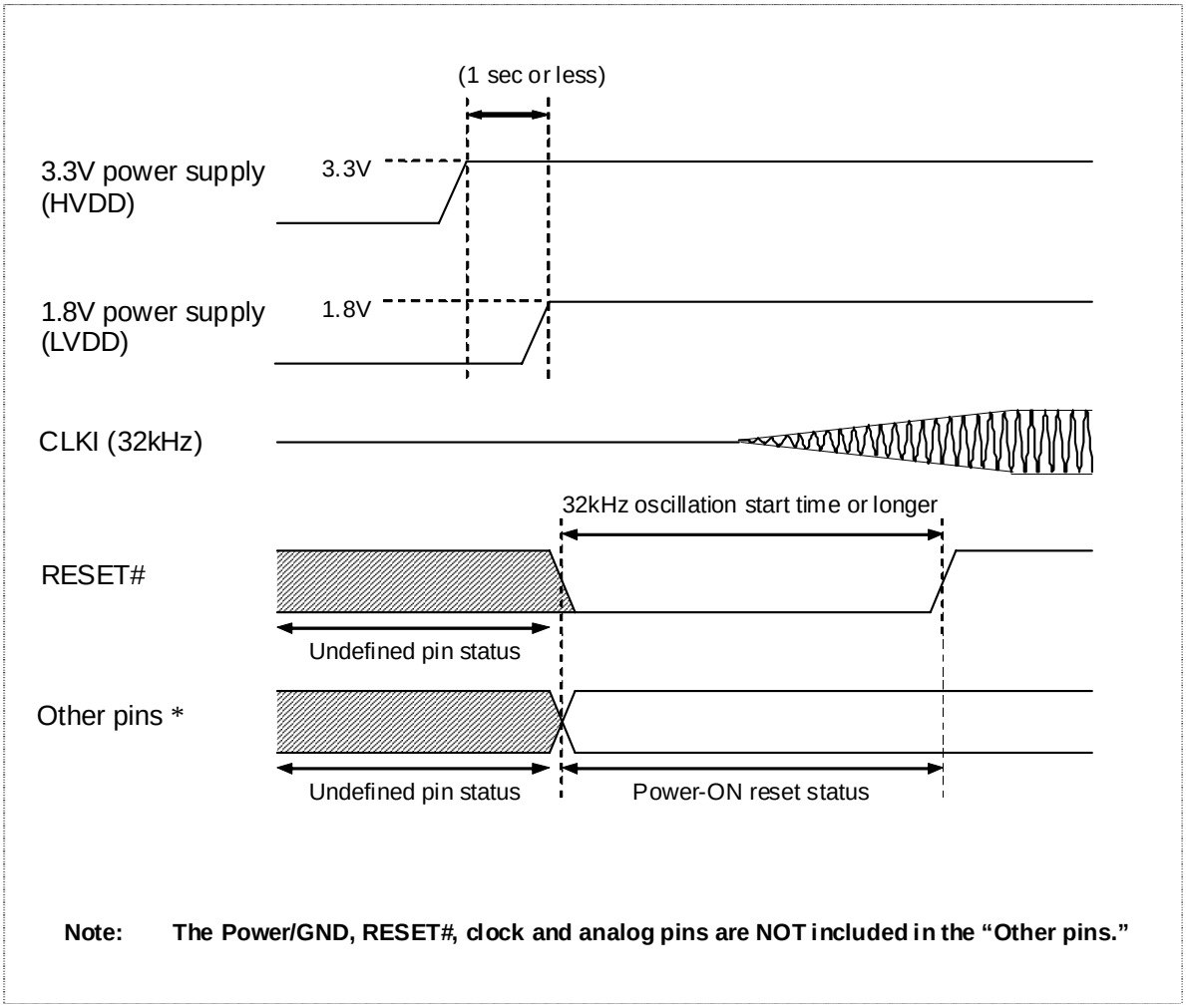


Figure 31.1 Power-ON Timing

31.4 Power-OFF Timing

The 3.3V power supply (HVDD) and 1.8V power supply (LVDD) must be turned Off in the following sequence.

(1) After turning off a power supply, turn off the other in a second. We recommend you to reduce this delay as much as possible.

(2) If the 1.8V power supply is only turned Off, the pin status is unstable. You must design the system to avoid the system malfunction due to this unstable pin status.

32. ELECTRICAL CHARACTERISTICS

32.1 DC Characteristics

Table 32.1 DC Characteristics (3.3V)

(HVDD = 3.3V ± 0.3V, VSS = 0V, Ta= -40 to 85°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leak current	I_{LI}	—		-5	—	5	µA
Off-state leak current	I_{OZ}	—		-5	—	5	µA
High-level output voltage (*1)	V_{OH}	I_{OH} = -4mA HVDD=Min.		HVDD -0.4	—	—	V
Low-level output voltage (*1)	V_{OL}	I_{OL} = 4mA HVDD=Min.		—	—	0.4	V
High-level input voltage	V_{IH1}	LVCMOS level, HVDD=Max.		2.2	—	—	V
Low-level input voltage	V_{IL1}	LVCMOS level, HVDD=Min.		—	—	0.8	V
High-level input voltage	V_{T1+}	LVCMOS Schmitt input		1.4	—	2.7	V
Low-level input voltage	V_{T1-}	LVCMOS Schmitt input		0.6	—	1.8	V
Hysteresis voltage	V_{H1}	LVCMOS Schmitt input		0.3	—	—	V
High-level input voltage	V_{IH2}	LVTTL level, HVDD=Max.		2.0	—	—	V
Low-level input voltage	V_{IL2}	LVTTL level, HVDD=Min.		—	—	0.8	V
Pull-up resistance	P_{PU}	VI=0V		25	50	120	KΩ
Pull-down resistance	P_{PD}	VI=HVDD	Other pins *2	25	50	120	kΩ
			MD[15:0] pin	50	100	240	
Input pin capacity	C_I	f=1MHz, HVDD = 0V		—	—	8	pF
Output pin capacity	C_O	f=1MHz, HVDD = 0V		—	—	8	pF
Input and output pin capacity	C_{IO}	f=1MHz, HVDD = 0V		—	—	8	pF
AD Converter current	I_{ADC}	—		—	—	1	mA
Input impedance of ADC	P_{ADC}	—		—	5	—	kΩ

*1: Applied to all output and I/O pins.
*2: The pin has pull-down resistance except for MD[15:0] pin.

Table 32.2 DC Characteristics (1.8V)

(RTCVDD = 1.8V ± 0.15V, VSS = 0V, Ta= -40 to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input leak current	I_{LI}	—	-5	—	5	µA
Off-state leak current	I_{OZ}	—	-5	—	5	µA
High-level input voltage	V_{T1+}	LVCMOS Schmitt input	0.6	—	1.4	V
Low-level input voltage	V_{T1-}	LVCMOS Schmitt input	0.3	—	1.1	V
Hysteresis voltage	V_{H1}	LVCMOS Schmitt input	0.02	—	—	V
Input pin capacity	C_I	f=1MHz, HVDD = 0V	—	—	8	pF

Table 32.3 USBVBUS Judgment voltage

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level trigger voltage	VB_{TH}	UVDD3 = 3.6V	1.86	—	2.85	V
Low-level trigger voltage	VB_{TL}	UVDD3 = 3.0V	1.48	—	2.23	V
Hysteresis voltage	VB_H	UVDD3 = 3.0V	0.31	—	0.64	V

Table 32.4 Current Consumption (Reference values, at Room Temperature)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption (LVDD)	I_{LOW}	Low-speed mode*1	—	180	—	µA
	I_{LOWh}	Low-speed HALT mode*2	—	155	—	µA
	I_{FO1}	High-speed mode 1*3	—	120	—	mA
	I_{FO2}	High-speed mode 2*4	—	95	—	mA
	I_{FO3}	High-speed mode 3*5	—	145	—	mA
Power consumption (PTCVDD)	I_{RTCO}	RTC Stand-alone Operations (BUP#=LOW)*6	—	1	—	µA
	I_{RTCH}	RTC Normal Operations (BUP#=HIGH)*7	—	450	—	µA
Current Consumption (PLLVDD)	I_{DDPLL}	PLL Frequency = 50.00MHz	—	1.8	—	µA
	I_{DDPD}	During PLL Power-down	—	1	—	µA

*1: When system is operated at 32KHz
*2: When the system is operated at 32KHz and the internal bus clock is stopped
*3: When two camera is connected and executed IP conversion and JPEG encode (30fps@VGA) and recorded on a SD memory
*4: When A JPEG file stored in an external SDRAM is being recorded on a SD memory with the camera interfaces and the JPEG controller being stopped.
*5: When two cameras are connected, and IP conversion and JPEG encoding (30fps@VGA) are executed and images are being displayed on a PC via a USB cable.
*6: Timekeeping on the RTC is active and other power supplies are shut down (Battery backup mode)
*7: The current consumption of RTC portion when the system is operated at 50 MHz.

32.2 AC Characteristics

32.2.1 AC Characteristics Measuring Conditions

HVDD, AVDD, UVDD3, = 3.3V ± 0.3V
C1VDD, C2VDD = 3.0V ± 0.6V
SDVDD = 2.7V to 3.6V
LVDD, UPVDD, UXVDD, PLLVDD, RTCVDD = 1.8V ± 0.15V
T_A = -40°C to 85°C
CL=50 pF (unless otherwise noted)

32.2.2 AC Characteristics Signal Timing List

32.2.2.1 Clock Timing

Table 32.5 Clock (CLKI) Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SYSCLKI frequency	f_{clkI}	—	32.768	—	KHz	—
SYSCLKI input cycle time	t_{clkI}	—	1/ f_{OSC}	—	s	—
SYSCLKI high-level pulse width	t_{CLKIH}	5	—	—	µs	—
SYSCLKI low-level pulse width	t_{CLKIL}	5	—	—	µs	—
SYSCLKI rise time (from 10% to 90%)	t_{CLKIR}	—	—	12	µs	—
SYSCLKI fall time (from 90% to 10%)	t_{CLKIF}	—	—	12	µs	—
System clock frequency	fsys	—	—	50.01	MHz	*0
System clock frequency cycle	Ts	1/fsys —	—	—	ns	—

*0: The period jitter(2%) of PLL is already included to this calculation.

32.2.2.2 CPU Control Signal Timing

Table 32.6 CPU Control Signal Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
RESET# pulse width	t_{RESW}	10	—	—	T_{CLKI}	*1
IRQ/FIQ pulse width	t_{IRQW}	10	—	—	T_S	*2
Clock restart time	t_{WAK}	—	—	4	T_S	*2
PLL stability time	t_{PLLST}	—	—	100	ms	—

*1: T_{CLKI}=32 KHz unit. A signal amplitude to turn off the threshold voltage is required.
*2: T_S=System clock cycle time, that has 2% of period jitter(Thereafter omission).

32.2.2.3 Battery Backup Mode Timing

Table 32.7 Battery Backup Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
BUP# pin delay time at power supply start time	t_{BUPPO}	0	—	—	ns	
Power shutdown time at backup start time	t_{BUPS}	10	—	—	ns	
Power supply stability time at backup recovery time	t_{BUPH}	10	—	—	T_{CLKI}	*1
RESET# effective time after backup release	t_{BUPRST}	10	—	—	T_{CLKI}	*1

*1: T_{CLKI}=32 KHz unit. A signal amplitude to turn off the threshold voltage is required.

32.2.2.4 Camera Interface (CAM) Timing

Table 32.8 Camera Interface (CAM) Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
From CMVREF rise edge to CMHREF rise edge	t_{CAM1}	0	—	—	T_C	*3
Horizontal blank period	t_{CAM2}	4	—	—	T_C	*3
From CMHREF fall edge to CMVREF fall edge	t_{CAM3}	0	—	—	T_C	*3
Vertical blank period	t_{CAM4}	1	—	—	Line	—
Camera input clock period	t_{CAM5}	1.6 (3.2)	—	—	T_S	*2
Camera input clock low-level pulse width	t_{CAM6}	0.8 (1.6)	—	—	T_S	*2
Camera input clock high-level pulse width	t_{CAM7}	0.8 (1.6)	—	—	T_S	*2
Data setup time	t_{CAM8}	10	—	—	ns	—
Data hold time	t_{CAM9}	10	—	—	ns	—
CMVREF and CMHREF setup time	t_{CAM10}	10	—	—	ns	—
CMVREF and CMHREF hold time	t_{CAM11}	10	—	—	ns	—

*2: T_S = System clock cycle time
The minimum value is obtained during high-speed sampling, and the minimum value during normal sampling is shown in parentheses.
*3: T_C = Camera interface input clock cycle time

32.2.2.5 Memory Controller (MEMC) Timing

■ Static Memory Controller Timing

Table 32.9 Static Memory Timing 1 (MCS0#/MCS1#)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Address signal setup time	t_{MAS}	1	—	—	ns	
Address signal hold time (to MOE#)	t_{MAHOE}	$n_1Ts + 1$	—	—	ns	*2 *4
Address signal hold time (to MWE#)	t_{MAHWE}	$(n_2+1)Ts - 1$	—	—	ns	*2 *5
Address signal hold time (to MCSx#)	t_{MAHCE}	$1Ts - 3$	—	—	ns	*2
Data output enable signal delay time	t_{MOED}	$n_3Ts - 6$	—	—	ns	*2 *6
Data output enable signal effective period	t_{MOEV}	$n_4Ts - 0.5$	—	—	ns	*2 *7
Data output enable signal interval period	t_{MOEI}	—	n_3	—	Ts	*2
Chip select hold time (to MOE#)	t_{MCEHOE}	$n_1Ts + 1$	—	—	ns	*2 *4
Read data setup time	t_{MDRS}	—	—	16	ns	
Read data hold time	t_{MDRH}	0	—	—	ns	
Write effective signal delay time	t_{MWED}	$n_5Ts - 3$	—	—	ns	*2 *8
Write effective signal effective period	t_{MWEV}	$n_6Ts - 0.5$	—	—	ns	*2 *9
Write effective signal interval period	t_{MWEI}	—	n_7	—	Ts	*10
Chip select signal hold time (to MWE#)	t_{MCEHWE}	$(n_2+1)Ts + 0$	—	—	ns	*2 *5
Byte enable signal delay time	t_{MBED}	0	—	—	ns	
Byte enable signal hold time	t_{MBEH}	$(n_2+1)Ts - 5$	—	—	ns	*2 *5
Write data setup time	t_{MDWS}	—	—	$n_6Ts - 6$	ns	*2 *9
Write data hold time	t_{MDWH}	$(n_2+1)Ts - 5$	—	—	ns	*2 *5

Table 32.10 Static Memory Timing 2 (MCS2#/MCS3#)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Address signal setup time	t_{MAS}	0	—	—	ns	
Address signal hold time (to MOE#)	t_{MAHOE}	n_1Ts + 1	—	—	ns	*2 *4
Address signal hold time (to MWE#)	t_{MAHWE}	(n_2+1)Ts – 1	—	—	ns	*2 *5
Address signal hold time (to MCSx#)	t_{MAHCE}	1Ts – 1	—	—	ns	*2
Data output enable signal delay time	t_{MOED}	n_3Ts – 2.5	—	—	ns	*2 *6
Data output enable signal effective period	t_{MOEV}	n_4Ts – 0.5	—	—	ns	*2 *7
Data output enable signal interval period	t_{MOEI}	—	n_3	—	Ts	*2
Chip select hold time (to MOE#)	t_{MCEHOE}	n_1Ts + 0	—	—	ns	*2 *4
Read data setup time	t_{MDRS}	—	—	16	ns	
Read data hold time	t_{MDRH}	0	—	—	ns	
Write effective signal delay time	t_{MWED}	n_5Ts + 0	—	—	ns	*2 *8
Write effective signal effective period	t_{MWEV}	n_6Ts – 0.5	—	—	ns	*2 *9
Write effective signal interval period	t_{MWEI}	—	n_{7+1}	—	Ts	*10
Chip select signal hold time (to MWE#)	t_{MCEHWE}	(n_2+1)Ts – 3	—	—	ns	*2 *5
Byte enable signal delay time	t_{MBED}	0	—	—	ns	
Byte enable signal hold time	t_{MBEH}	(n_2+1)Ts – 5	—	—	ns	*2 *5
Write data setup time	t_{MDWS}	—	—	n_6Ts – 6	ns	*2 *9
Write data hold time	t_{MDWH}	(n_2+1)Ts – 5	—	—	ns	*2 *5

* 2 Ts = System clock cycle time
* 4 n_1 = The Value set by WAITRH registers (MEMC:0x20,0x30,0x40,0x50)
* 5 n_2 = The value set by WAITWH register (MEMC:0x20, 0x30, 0x40, 0x50)
* 6 n_3 = The value set by WAITOE register add to the value set by WAITRH register (MEMC:0x20, 0x30, 0x40, 0x50)
* 7 n_4 = The value obtained by deducting the value of WAITOE register from the value of WAITRD register (MEMC:0x20, 0x30, 0x40, 0x50)
* 8 n_5 = The value set by WAITWE register (MEMC:0x20, 0x30, 0x40, 0x50)
* 9 n_6 = The value obtained by deducting the value of WAITWE register from the value of WAITWR register (MEMC:0x20, 0x30, 0x40, 0x50)
*10 n7= The value set by WAITWE register add to the value set by WAITWH register (MEMC:0x20, 0x30, 0x40, 0x50)

■ SDRAM Controller Timing

Table 32.11 SDRAM Controller Timing (SDVDD=3.3V±0.3V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SDCKE delay time	t_{CKED}	2.5	—	10	ns	—
SDCS[1:0]# delay time	t_{CSD}	2.5	—	10	ns	—
SDRAS# delay time	t_{RASD}	2.5	—	10	ns	—
SDCAS# delay time	t_{CASD}	2.5	—	10	ns	—
SDWE# delay time	t_{WED}	2.5	—	10	ns	—
SDDQM[3:0] delay time	t_{DQMD}	2.5	—	11	ns	—
Address delay time	t_{ADD}	2.5	—	11	ns	—
Write data delay time	t_{WDD}	2.5	—	16.5	ns	—
Read data setup time	t_{RDS}	12	—	—	ns	—
Read data hold time	t_{RDH}	0	—	—	ns	—

Table 32.12 SDRAM Controller Timing (SDVDD=3.0V±0.3V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SDCKE delay time	t_{CKED}	2.5	—	10	ns	—
SDCS[1:0]# delay time	t_{CSD}	2.5	—	10	ns	—
SDRAS# delay time	t_{RASD}	2.5	—	10	ns	—
SDCAS# delay time	t_{CASD}	2.5	—	10	ns	—
SDWE# delay time	t_{WED}	2.5	—	10	ns	—
SDDQM[3:0] delay time	t_{DQMD}	2.5	—	11	ns	—
Address delay time	t_{ADD}	2.5	—	11	ns	—
Write data delay time	t_{WDD}	2.5	—	16.5	ns	—
Read data setup time	t_{RDS}	12.5	—	—	ns	—
Read data hold time	t_{RDH}	0	—	—	ns	—

32.2.2.6 I^2C Single Master Core Module (I2C) Timing

Table 32.13 I^2C Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCL cycle time	$t_{C(SCL)}$	8	—	30720	T_S	*2
SCL pulse width (High)	$t_{WH(SCL)}$	—	1/2	—	$T_{C(SCL)}$	*10
SCL pulse width (Low)	$t_{WL(SCL)}$	—	1/2	—	$T_{C(SCL)}$	*10
SDA output delay time	$t_{D(OSDA)}$	—	1/4	—	$T_{C(SCL)}$	*10
SDA input setup time	$t_{SU(ISDA)}$	0	—	—	ns	*11
SDA input hold time	$t_{HD(ISDA)}$	0	—	—	ns	*11
SDA sample time	$t_{SMP(SDA)}$	—	1/4	—	$T_{C(SCL)}$	*10
Start condition startup time	$t_{S(ST)}$	1/4	—	—	$T_{C(SCL)}$	*10
Start condition completion time	$t_{E(ST)}$	1/2	—	—	$T_{C(SCL)}$	*10
Stop condition startup time	$t_{S(SP)}$	1/4	—	—	$T_{C(SCL)}$	*10
Stop condition completion time	$t_{E(SP)}$	1/2	—	—	$T_{C(SCL)}$	*10

*2: T_S = System clock cycle time
*11: $T_{C\,(SCL)}$ = SCL (I^2C clock) cycle time
*12: See SDA sample time ($T_{smp\,(SDA)}$).

32.2.2.7 I^2STiming

Table 32.14 I^2S Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK cycle time	t_{SCKCT}	2	—	512	T_S	*2
SCK pulse width (High)	t_{SCKWH}	1	—	—	T_S	*2
SCK pulse width (Low)	t_{SCKWL}	1	—	—	T_S	*2
SCK duty ratio	t_{SCKDT}	—	50	—	%	*12
WS cycle time	t_{WSCT}	32	—	256	t_{SCKCT}	*13
WS output delay time	t_{WSOD}	-1	—	1	T_S	*2
WS input setup time	t_{WSISU}	1	—	—	T_S	*2
WS input hold time	t_{WSIHD}	1	—	—	T_S	*2
SD output delay time	t_{SDOD}	-1	—	1	T_S	*2
SD input setup time	t_{SDISU}	1	—	—	T_S	*2
SD input hold time	t_{SDIHD}	1	—	—	T_S	*2

*2: TS = System clock cycle time
*13: $t_{SCKDT} = t_{SCKWH} / (t_{SCKWH} + t_{SCKWL})$
*14: t_{SCKCT} = SCK cycle time

32.2.2.8 Serial Peripheral Device Interface (SPI) Timing

Table 32.15 SPI Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCLK cycle time	$t_{C(SCLK)}$	4	—	512	T_S	*2
SCLK pulse width (first half)	$t_{WH1(SCLK)}$	—	1/2	—	$T_{C(SCLK)}$	*14
SCLK pulse width (second half)	$t_{WH2(SCLK)}$	—	1/2	—	$T_{C(SCLK)}$	*14
SS output start time (during auto control)	$t_{S(OSS)}$	3	—	—	T_S	*2
SS output completion time (during auto control)	$t_{E(OSS)}$	1	—	—	T_S	*2
SS input setup time	$t_{SU(ISS)}$	3	—	—	T_S	*2
SS input hold time	$t_{HD(ISS)}$	1	—	—	T_S	*2
MISO input setup time	$t_{SU(MI)}$	30	—	—	ns	
MISO input hold time	$t_{HD(MI)}$	0	—	—	ns	
MISO output delay time	$t_{D(SO)}$	—	—	30	ns	
MOSI input setup time	$t_{SU(SI)}$	10	—	—	ns	
MOSI input hold time	$t_{HD(SI)}$	10	—	—	ns	
SCLK cycle time	$t_{D(MO)}$	—	—	0	ns	

*2: T_S = System clock cycle time
*15: $T_{C(SCLK)}$ = SCLK (SPI clock) cycle time = (4×2^{MCBR}) T_S

32.2.2.9 Compact Flash Memory Interface (CF) Timing

■ CF Attribute Memory Timing

Table 32.16 CF Attribute Memory Read Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read cycle time	t_{ATRC}	—	20	—	T_S	*2
Address setup time	t_{ADSAR}	—	4	—	T_S	*2
Address hold time (from MOE# inactive state)	t_{ADHMOE}	—	2	—	T_S	*2
CE effective time before read	t_{CEVBR}	—	3	—	T_S	*2
CE effective time after read	t_{CEVAR}	—	2	—	T_S	*2
MOE# active time	t_{MOEW}	—	14	—	T_S	*2
Read data setup time	t_{RDS}	$1T_S$+16	—	—	ns	
Read data hold time	t_{RDH}	0	—	—	ns	

*2: T_S = System clock cycle time

Table 32.17 CF Attribute Memory Write Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Write cycle time	t_{ATWC}	—	16	—	T_S	*2
Address setup time	t_{ADSAW}	—	3	—	T_S	*2
MWE0# active time	t_{MWE0W}	—	9	—	T_S	*2
Write recovery time	t_{WREC}	—	2	—	T_S	*2
Write data effective time 1	t_{WDV1}	—	11	—	T_S	*2
Write data effective time 2	t_{WDV2}	—	2	—	T_S	*2

■ CF Common Memory Timing

Table 32.18 CF Common Memory Read Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read cycle time	t_{CMRC}	—	17	—	Ts	*2
Address setup time	t_{CRADS}	—	4	—	Ts	*2
Address hold time (from MOE# inactive state)	t_{ADHMOE}	—	2	—	Ts	*2
CE effective time before read	t_{CEVBR}	—	3	—	Ts	*2
CE effective time after read	t_{CEVAR}	—	2	—	Ts	*2
Wait active allowable time after read	t_{WTATAR}	—	—	6	Ts	*2
Data setup time after wait release	t_{DSAWT}	—	—	0	Ts	*2
Wait active time	t_{WTW}	—	—	3000	ns	
Read data setup time	t_{RDS}	1Ts+16	—	—	ns	
Read data hold time	t_{RDH}	0	—	—	ns	

Table 32.19 CF Common Memory Write Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Write cycle time	t_{CMWC}	—	17	—	Ts	*2
Address setup time	t_{ADS}	—	4	—	Ts	*2
Address hold time	t_{ADH}	—	4	—	Ts	*2
CE effective time before write	t_{CEVBW}	—	3	—	Ts	*2
CE effective time after write	t_{CEVAW}	—	2	—	Ts	*2
MWE0# active time	t_{MWE0W}	—	9	—	Ts	*2
Data effective time before write	t_{DVBW}	—	11	—	Ts	*2
Data effective time after write	t_{DVAW}	—	2	—	Ts	*2
Write recovery time	t_{WREC}	—	2	—	Ts	*2
Wait active allowable time after write	t_{WTATAW}	—	—	6	Ts	*2
Write active time after wait release	t_{WWAWT}	—	—	3	Ts	*2
Wait active time	t_{WTW}	—	—	3000	ns	

■ CF I/O Space/IDE Timing

Table 32.20 CF I/O Space/IDE Read Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read cycle time	t_{IORC}	—	20	—	Ts	*2
IORD# active time	t_{IORW}	—	10	—	Ts	*2
Address setup time	t_{ADSIO}	—	6	—	Ts	*2
Address hold time	t_{ADHIO}	—	4	—	Ts	*2
CE effective time before IO read	$t_{CEVBIOR}$	—	5	—	Ts	*2
CE effective time after IO read	$t_{CEVAIOR}$	—	3	—	Ts	*2
REG effective time before IO read	$t_{REGVBIOR}$	—	6	—	Ts	*2
REG effective time after IO read	$t_{REGVAIOR}$	—	4	—	Ts	*2
Wait allowable time after IO read active	$t_{WTATIOR}$	—	—	6	Ts	*2
Data delay allowable time after wait release	t_{DATAWT}	—	—	0	Ts	*2
Wait active time	t_{WTW}	—	—	3000	ns	
Read data setup time	t_{RDS}	1Ts+16	—	—	ns	
Read data hold time	t_{RDH}	0	—	—	ns	

Table 32.21 CF I/O Space/IDE Write Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Write cycle time	t_{IOWC}	—	20	—	Ts	*2
IOWR# active time	t_{IOWW}	—	10	—	Ts	*2
Address setup time	t_{ADSIO}	—	6	—	Ts	*2
Address hold time	t_{ADHIO}	—	4	—	Ts	*2
CE effective time before IO write	$t_{CEVBIOW}$	—	5	—	Ts	*2
CE effective time after IO write	$t_{CEVAIOW}$	—	3	—	Ts	*2
REG effective time before IO write	$t_{REGVBIOW}$	—	6	—	Ts	*2
REG effective time after IO write	$t_{REGVAIOW}$	—	4	—	Ts	*2
Data effective time before IO write	t_{DVBIOW}	—	14	—	Ts	*2
Data effective time after IO write	t_{DVAIOW}	—	3	—	Ts	*2
Wait allowable time after IO write	$t_{WTATIOW}$	—	—	6	Ts	*2
IO write inactive time after wait release	t_{WITAWT}	—	—	2	Ts	*2
Wait active time	t_{WTW}	—	—	3000	ns	

32.2.3 Timing Charts

32.2.3.1 Clock Timing

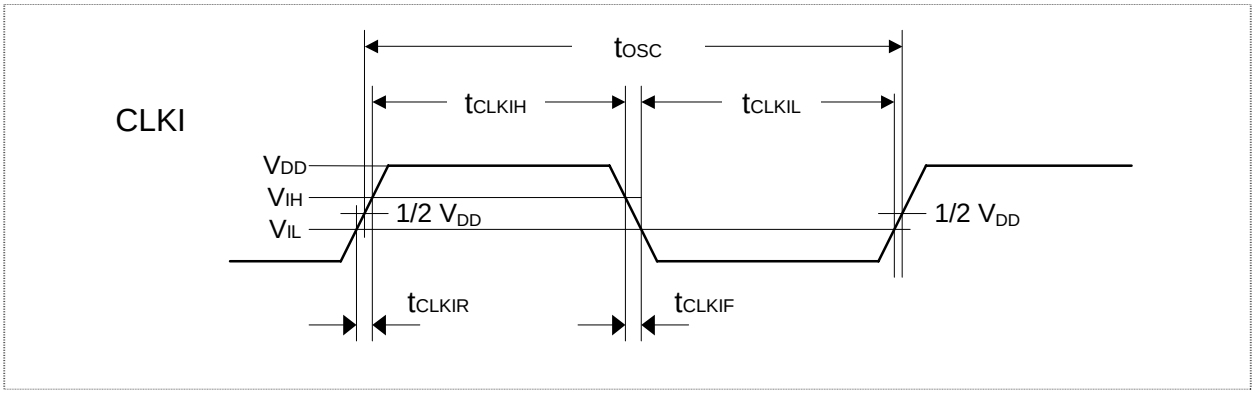


Figure 32.1 Clock Timing

32.2.3.2 CPU Control Signal Timing

■ RESET# Timing

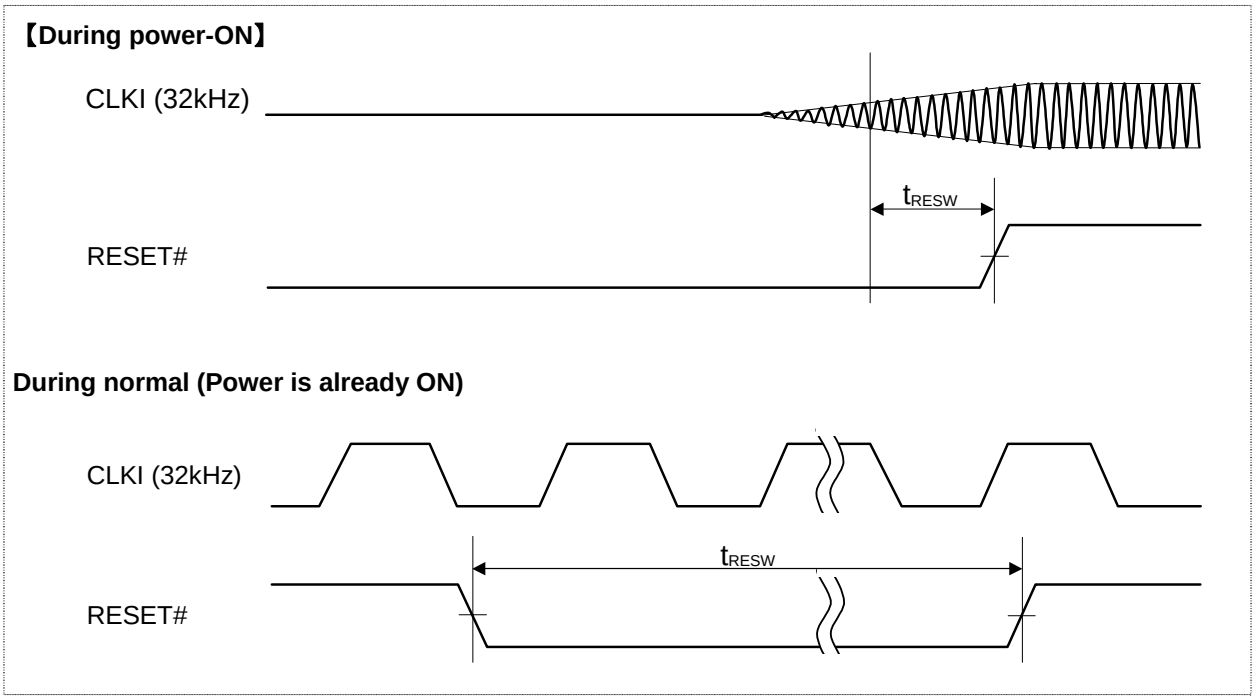


Figure 32.2 RESET# Timing

■ Interrupt Signal Timing

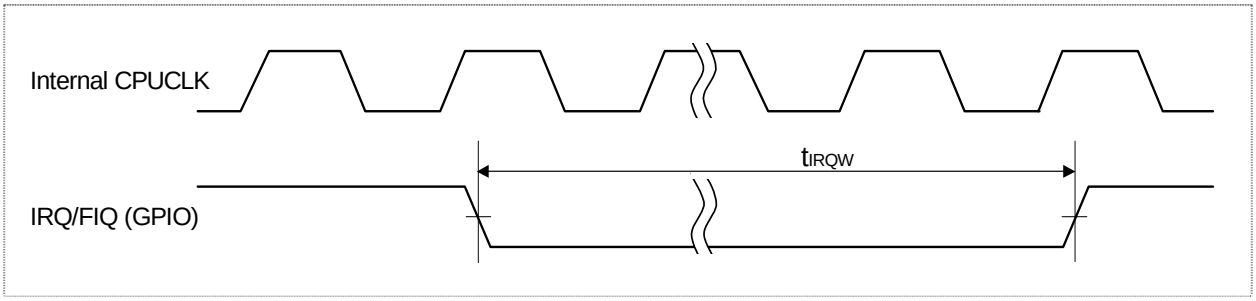
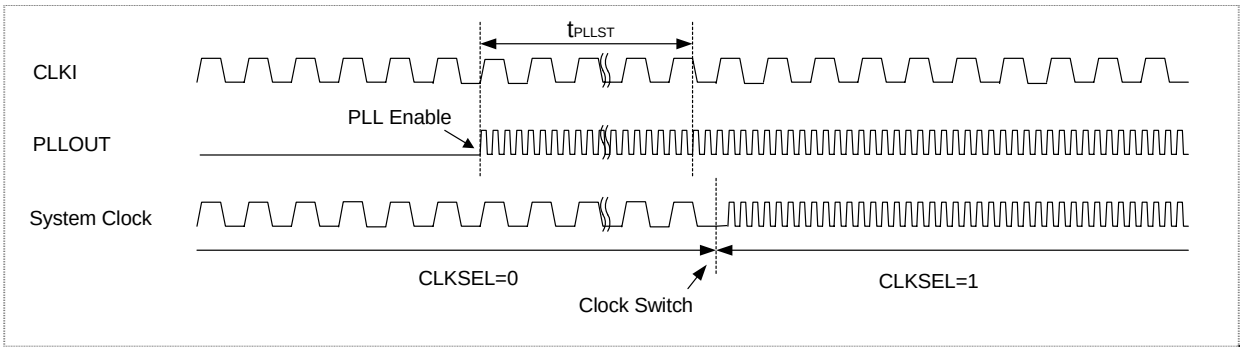


Figure 32.3 Interrupt Signal Timing

■ PLL Related Timing

(1) Clock Switch 1 (PLL Enable)

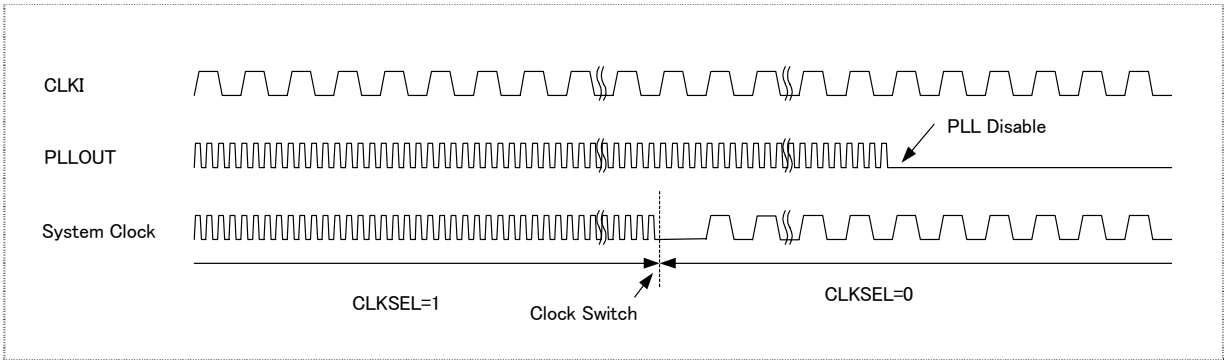


System Clock = CPUCLK / HCLK1 / HCLK2 / PCLK

Figure 32.4 Clock Switch 1 (PLL Enable)

This is the internal clock timing that is used to switch the 32KHz system clock to the PLL output.
Set bit 0 (PLLEN) of PLL Setting Register 2 (SYS[0x0C]) of the system controller to logical 1 and enable the PLL output. After the PLL stabilization time (tPLLST) has passed, set bit 0 (CLKSEL) of Clock Select Register (SYS[0x18]) to logical 1 and select the PLL output as the system clock.

(2) Clock Switch 2 (PLL Disable)

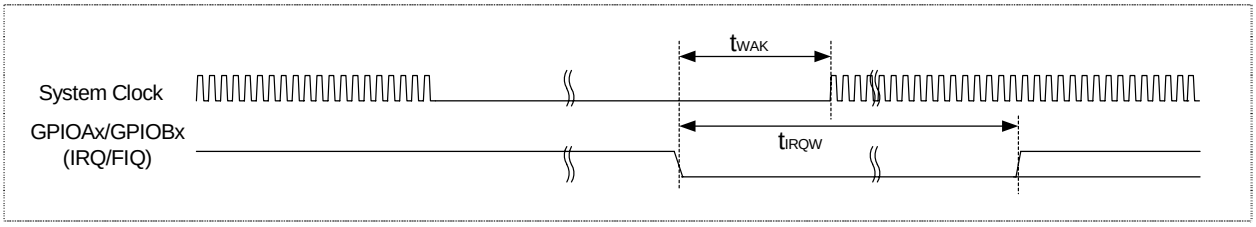


System Clock = CPUCLK / HCLK1 / HCLK2 / PCLK

Figure 32.5 Clock Switch 2 (PLL Disable)

This is the internal clock timing that is used to switch the PLL output to the 32KHz system clock.
Set bit 0 (CLKSEL) of Clock Select Register (SYS[0x18]) to logical 0, and select the CLKI (32KHz) as the system clock. Then, set bit 0 (PLLEN) of PLL Setting Register 2 (SYS[0x0C]) of the system controller to logical 1, and disable the PLL signal.

(3) Clock Restart by Interrupt in High-Speed HALT Mode

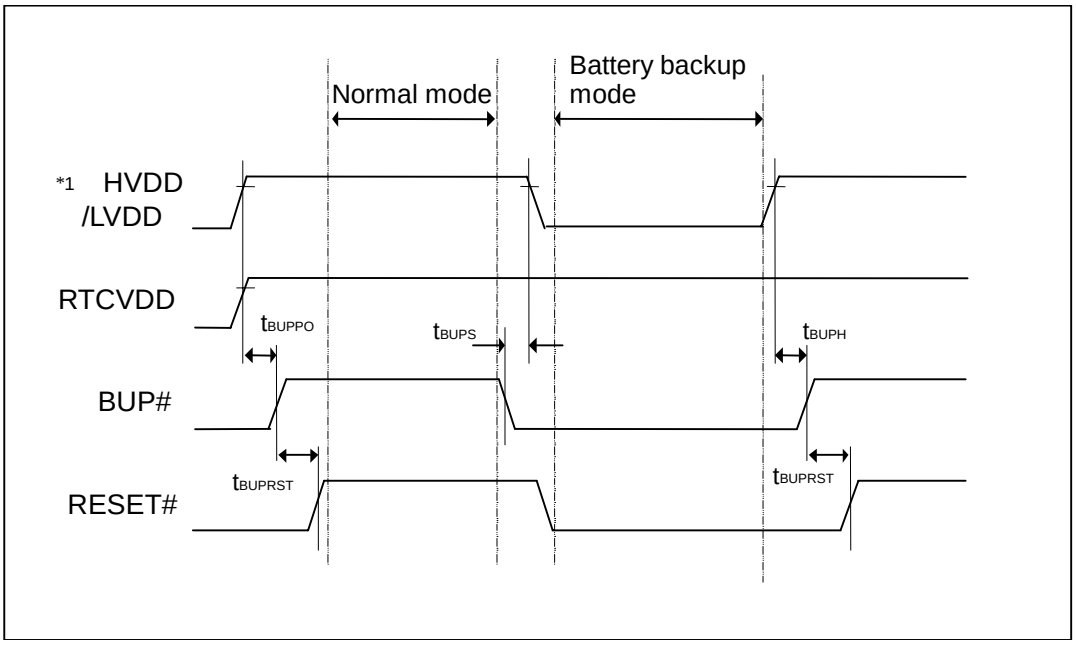


System Clock = CPUCLK / HCLK1 / HCLK2 / PCLK

Figure 32.6 Clock Restart Timing

This is the signal timing that is used to transition to the High-Speed mode when an interrupt occurs in the High-Speed HALT mode. The system clock restarts after the clock restart time (tWAK) has passed. The interrupt pulse width (tIRQW) must be longer enough than this timing.

32.2.3.3 Battery Backup Mode Timing



*1 : Contains C1VDD,C2VDD,SDVDD,AVDD,ULDD3,UPVDD,UXVDD,PLLVDD

32.2.3.4 Camera Interface Timing

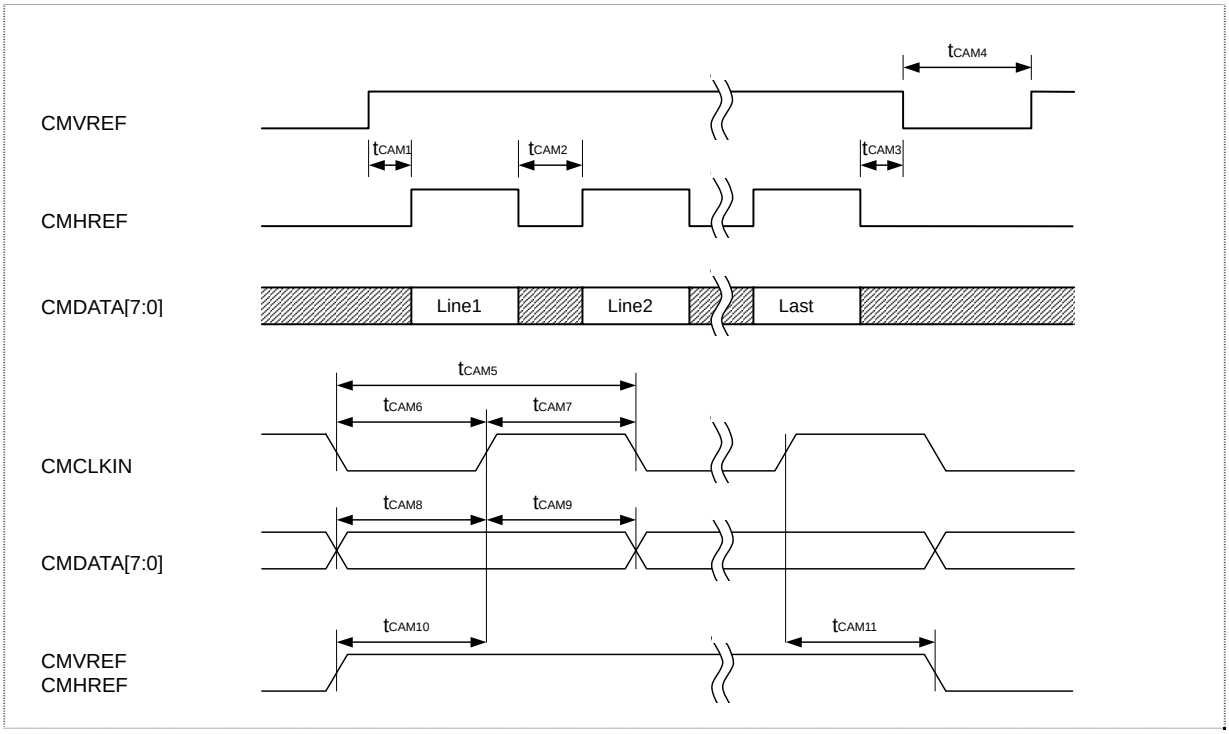


Figure 32.7 Camera Interface Timing

The effective CMCLKIN signal edge can be changed by the software. This figure shows a timing where data is read when the CMCLKIN signal changes from logical Low to logical High.

32.2.3.5 Memory Interface Controller

32.2.3.5.1 Static Memory Controller Timing (Flash EEPROM, SRAM, etc.)

■ Static Memory Read Timing

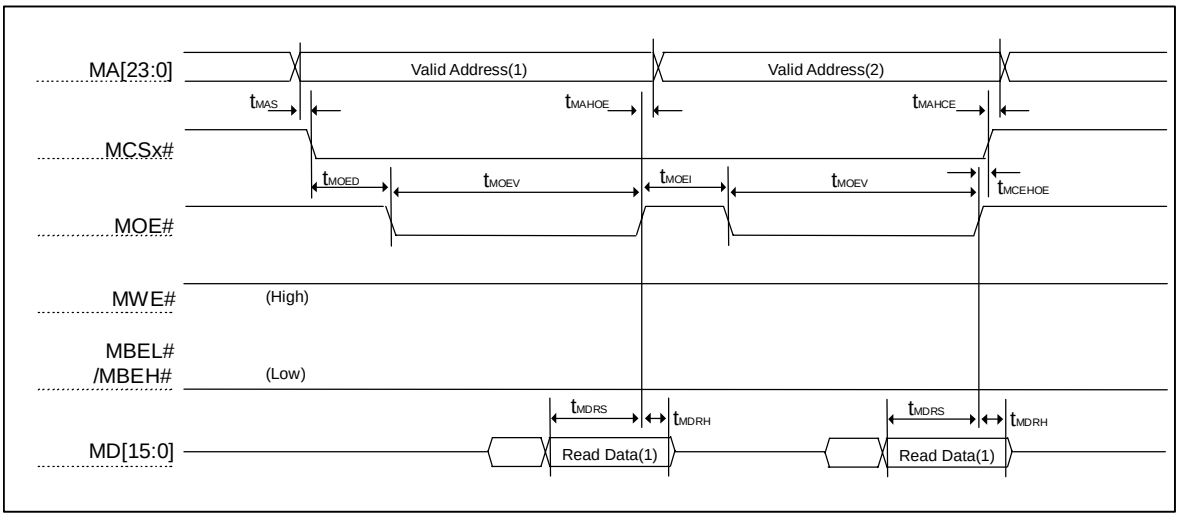


Figure 32.8 Static Memory Read Timing

■ Static Memory Write Timing

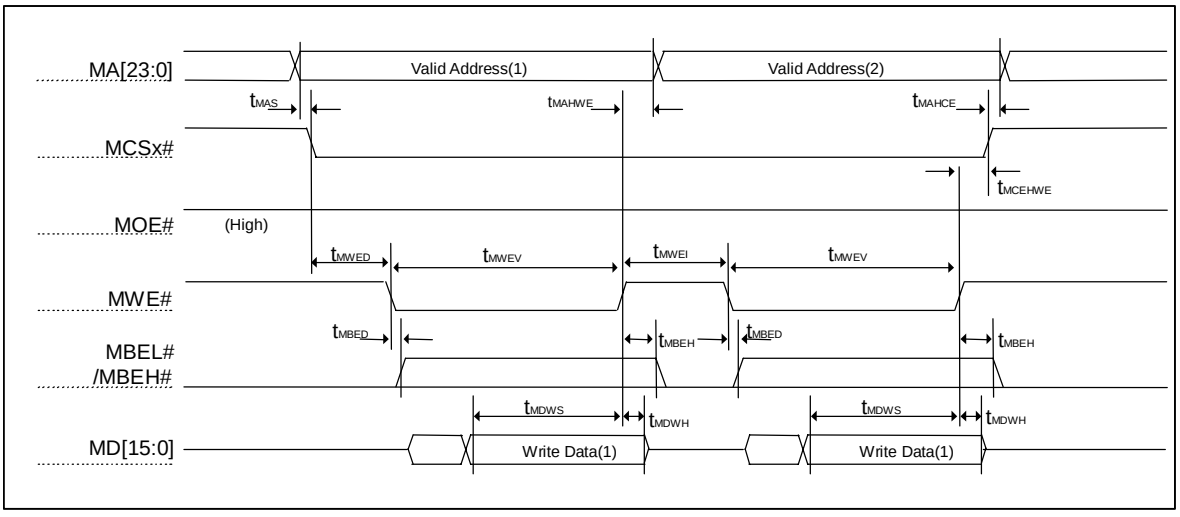


Figure 32.9 Static Memory Write Timing

32.2.3.5.2 SDRAM Controller AC Timing

The following shows an AC timing of the SDRAM controller.
The commands used in the figure are defined on this table.

Command	Function	MCS2#	MRAS#	MCAS#	MWE1#	Address and others
ACT	Bank active	L	L	H	H	Bank/Row
RD	Read	L	H	L	H	Bank/Col
WR	Write	L	H	L	L	Bank/Col
BT	Burst terminate	L	H	H	L	—
PCGA	Precharge all bank	L	L	H	L	SDA10 = HIGH
PCG	Precharge	L	L	H	L	SDA10 = LOW
AREF	Auto refresh	L	L	L	H	SDCLKEN = HIGH
SELF_IN	Self-refresh start	L	L	L	H	SDCLKEN = LOW
SELF_OUT	Self-refresh terminate	H	x	x	x	SDCLKEN = HIGH
LMR	Mode register set	L	L	L	L	—

■ SDRAM Read Cycles

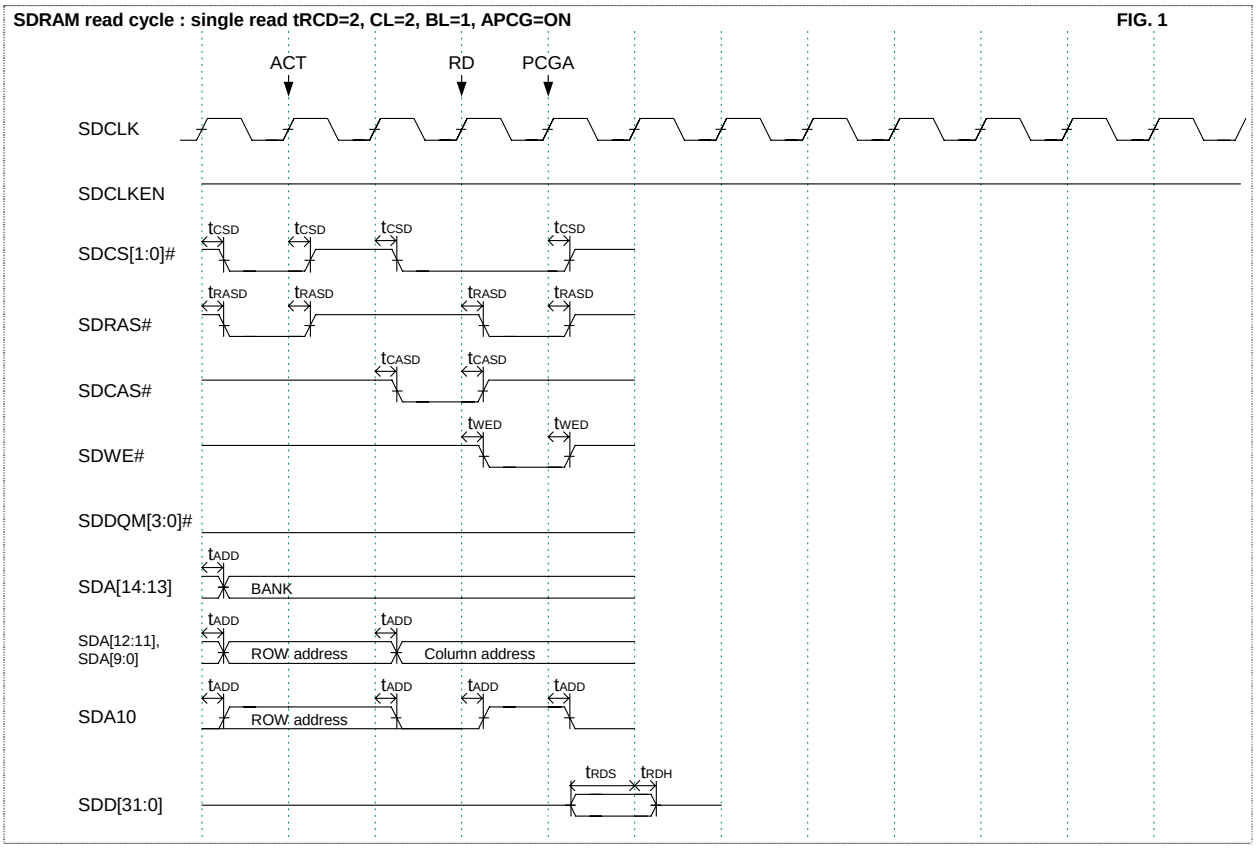


Figure 32.10 SDRAM Read Cycle 1: Single read cycle; tRCD=2, CL=2, BL=1, APCG=ON

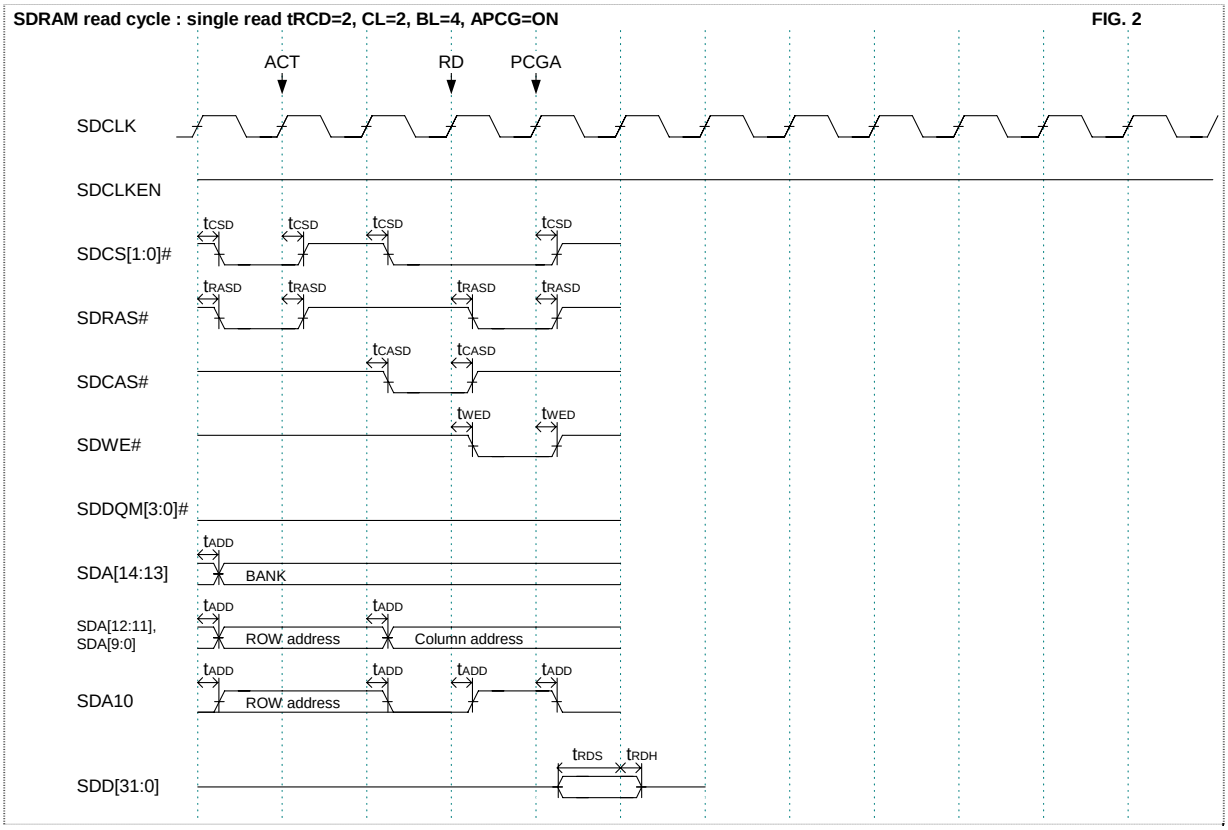


Figure 32.11 SDRAM Read Cycle 2: Single read cycle; tRCD=2, CL=2, BL=4, APCG=ON

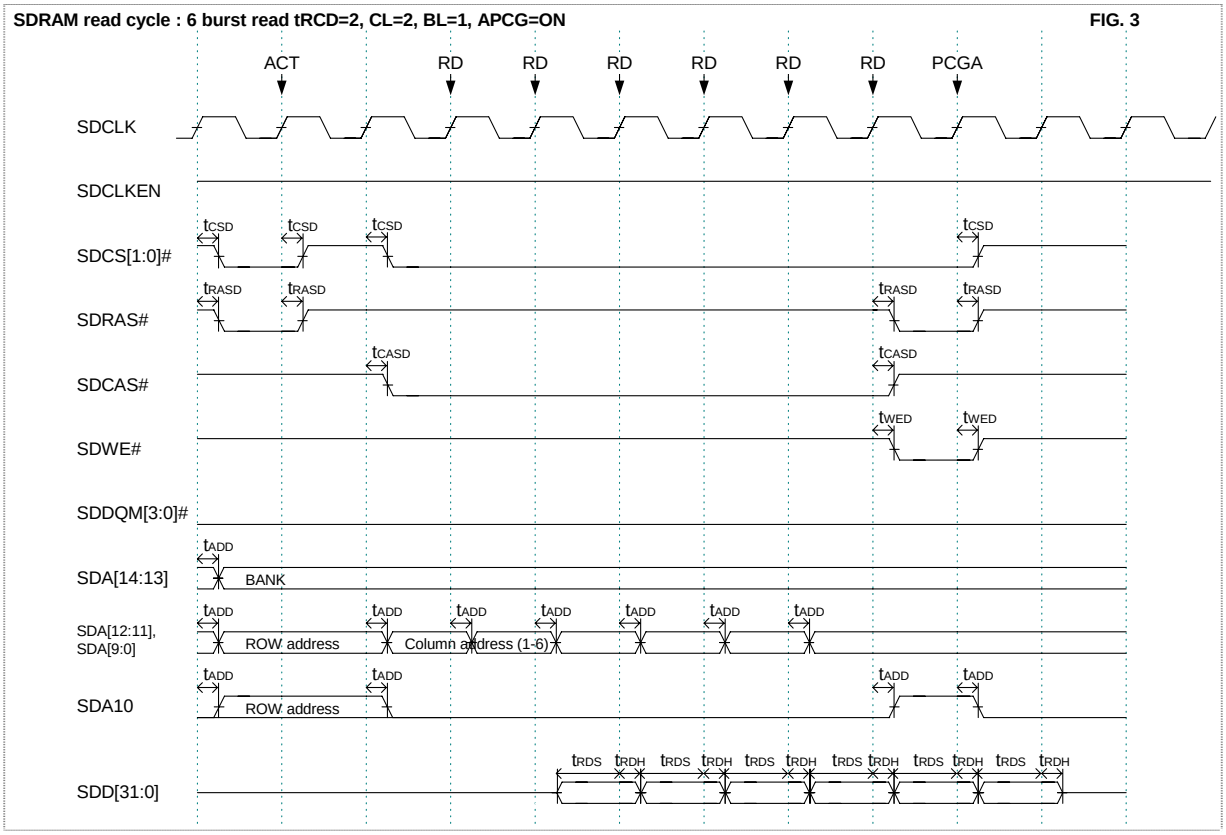


Figure 32.12 SDRAM Read Cycle 3: 6 burst read cycles; tRCD=2, CL=2, BL=1, APCG=ON

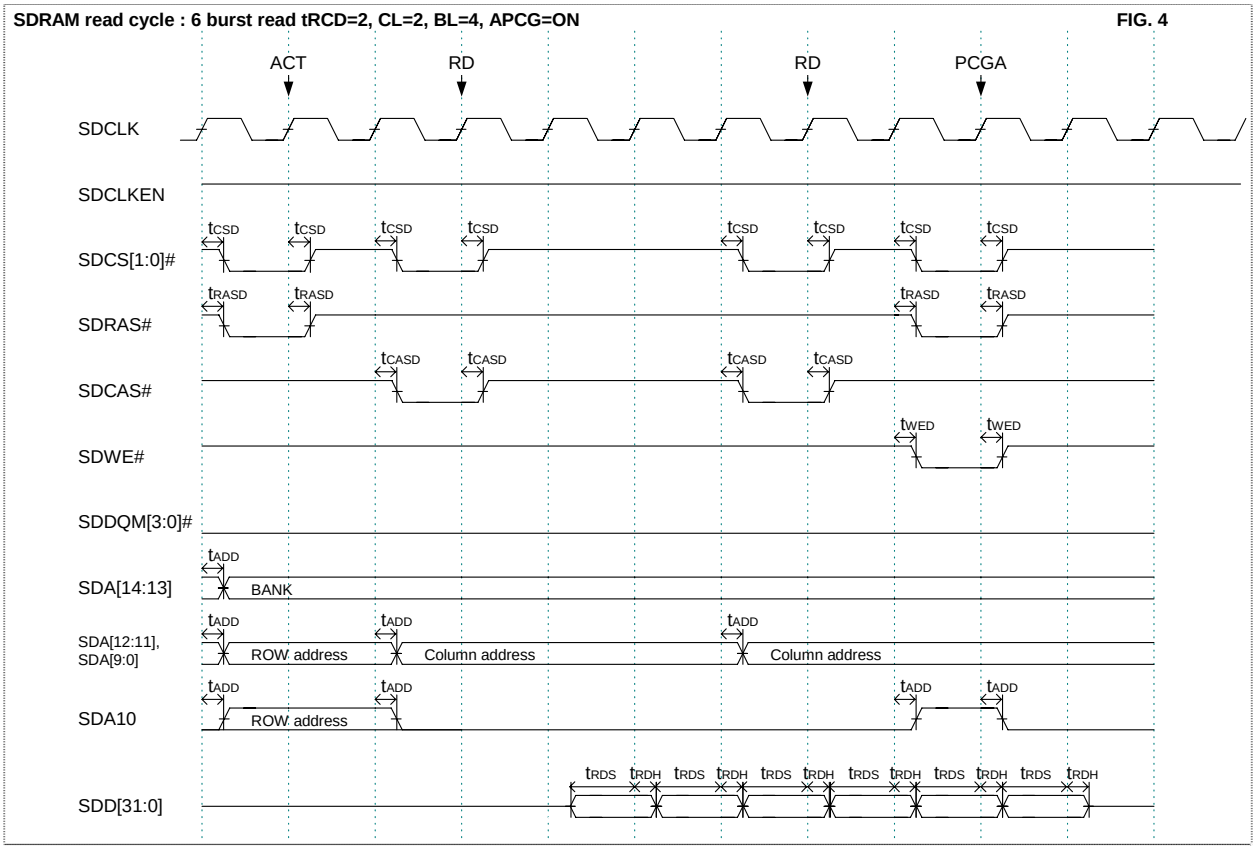


Figure 32.13 SDRAM Read Cycle 4: 6 burst read cycles; tRCD=2, CL=2, BL=4, APCG=ON

■ SDRAM Write Cycles

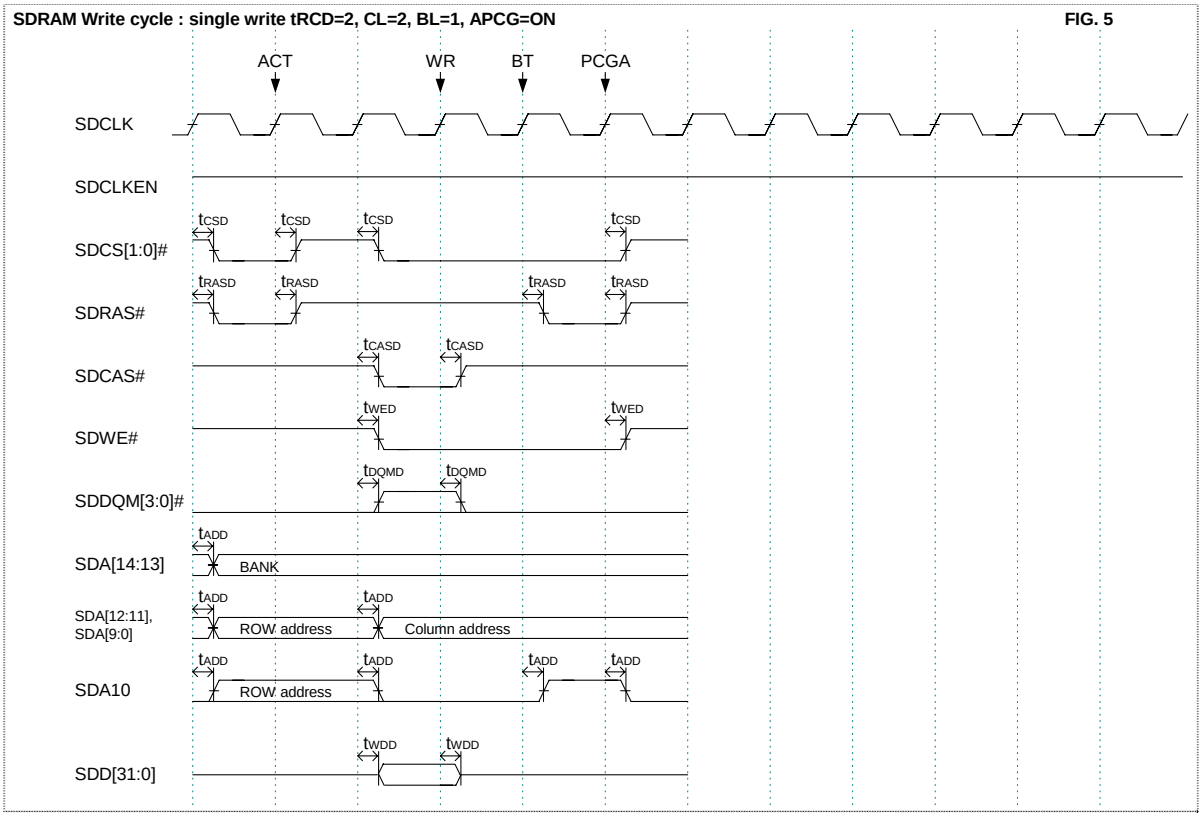


Figure 32.14 SDRAM Write Cycle 1: Single write cycle; tRCD=2, CL=2, BL=1, APCG=ON

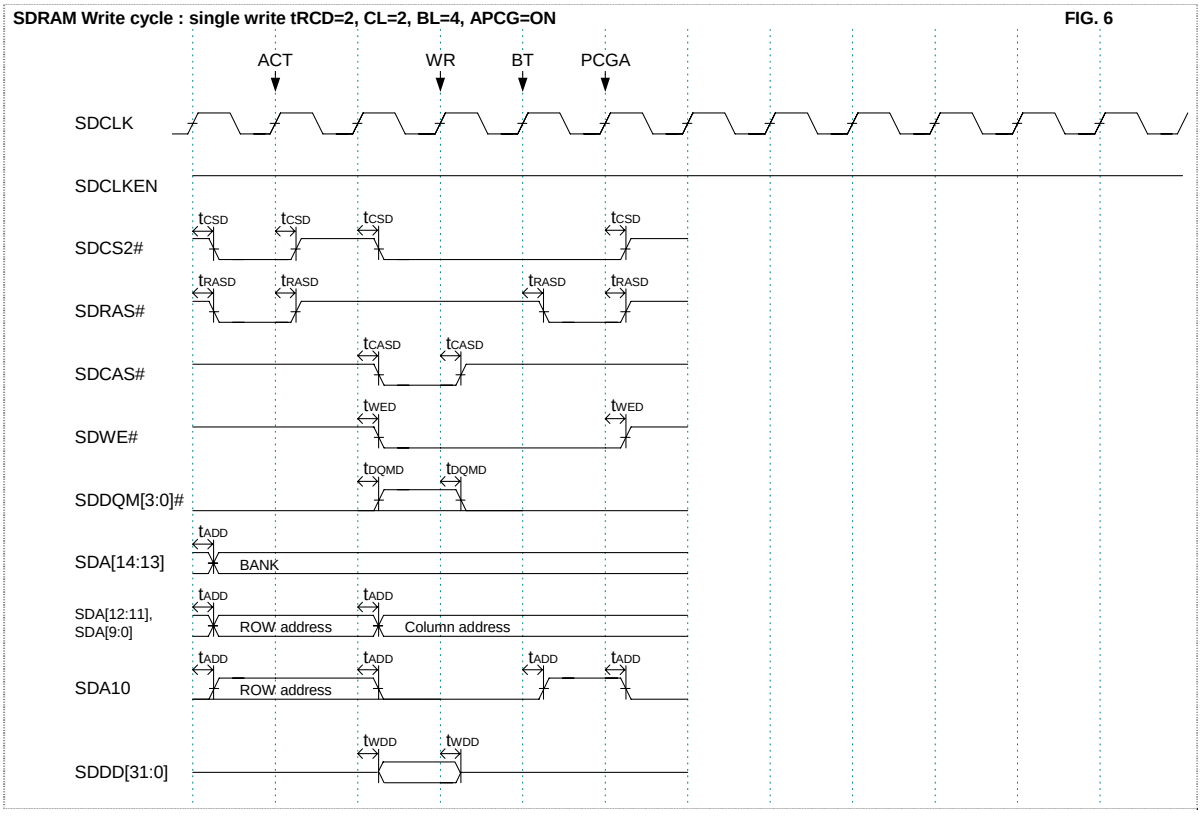


Figure 32.15 SDRAM Write Cycle 2: Single write cycle; tRCD=2, CL=2, BL=4, APCG=ON

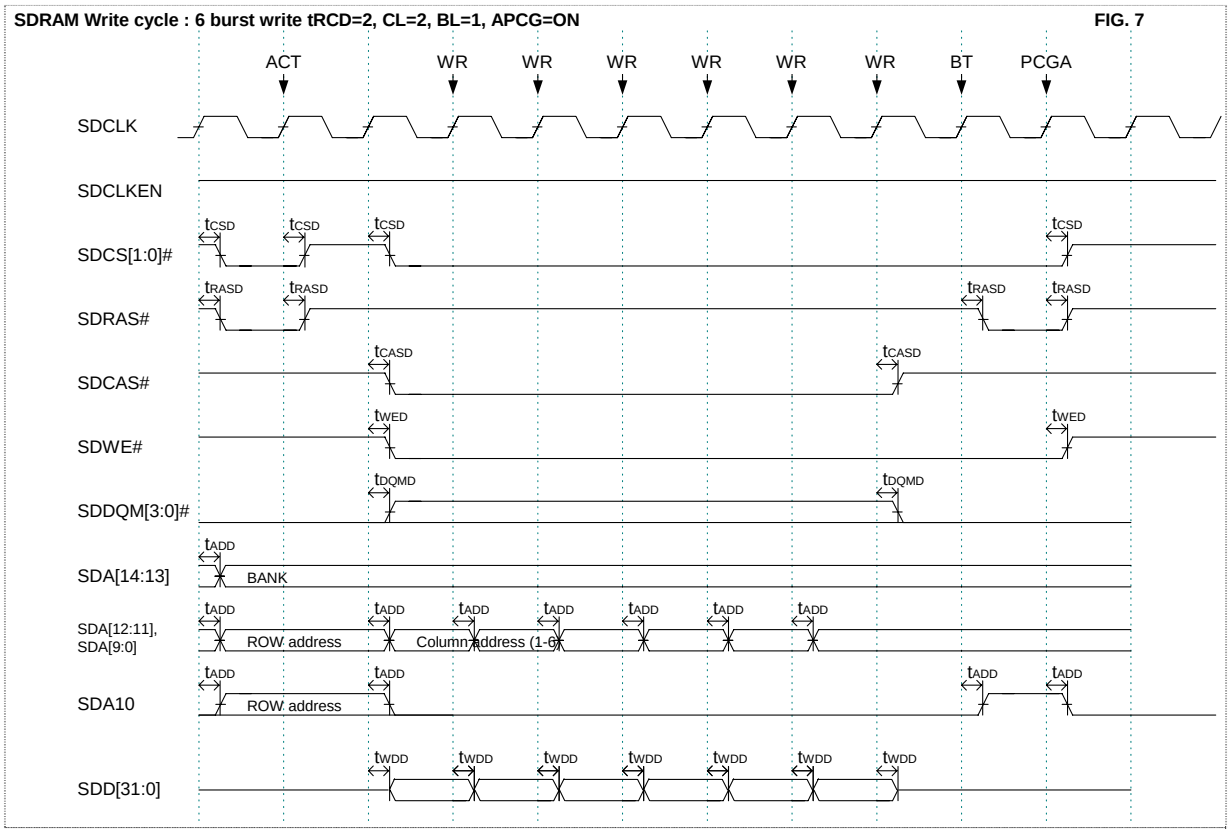


Figure 32.16 SDRAM Write Cycle 3: 6 burst write cycles; tRCD=2, CL=2, BL=1, APCG=ON

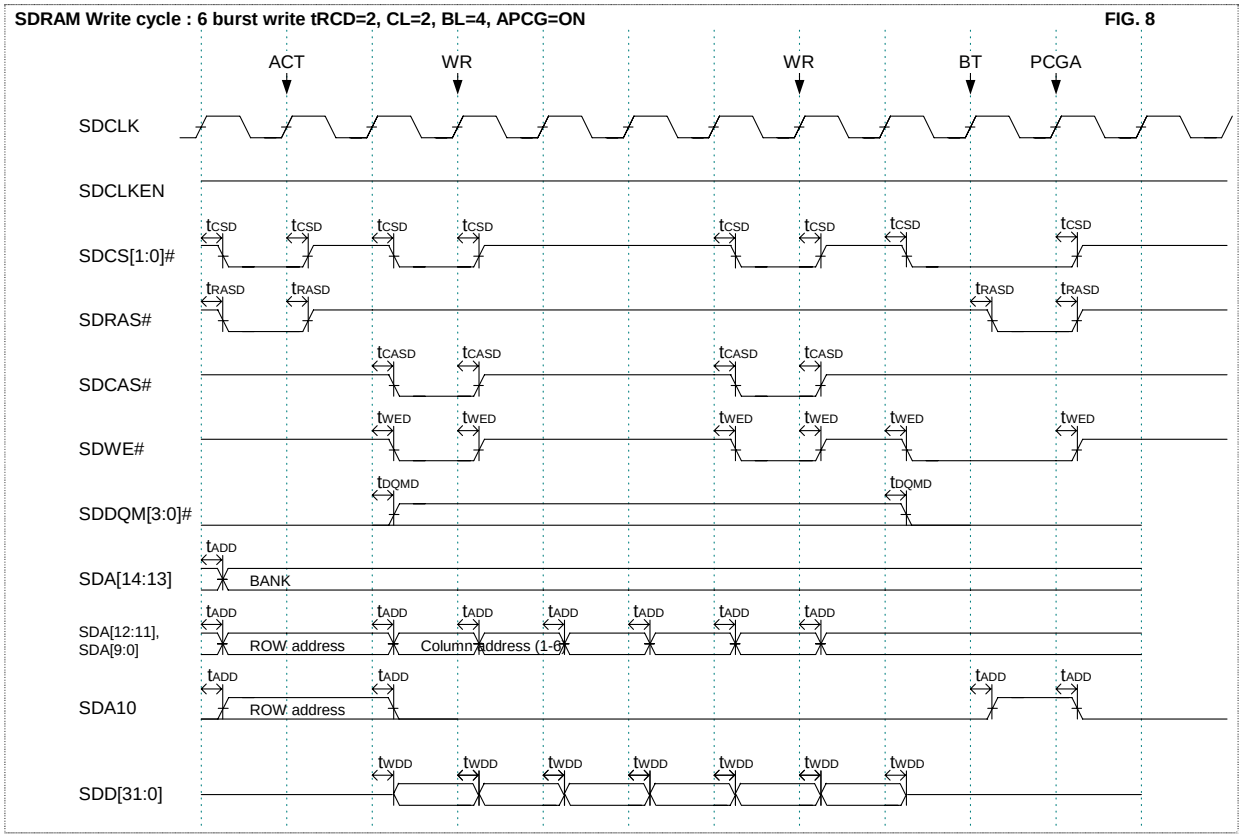


Figure 32.17 SDRAM Write Cycle 4: 6 burst write cycles; tRCD=2, CL=2, BL=4, APCG=ON

■ SDRAM Read Cycles (Row Active Mode)

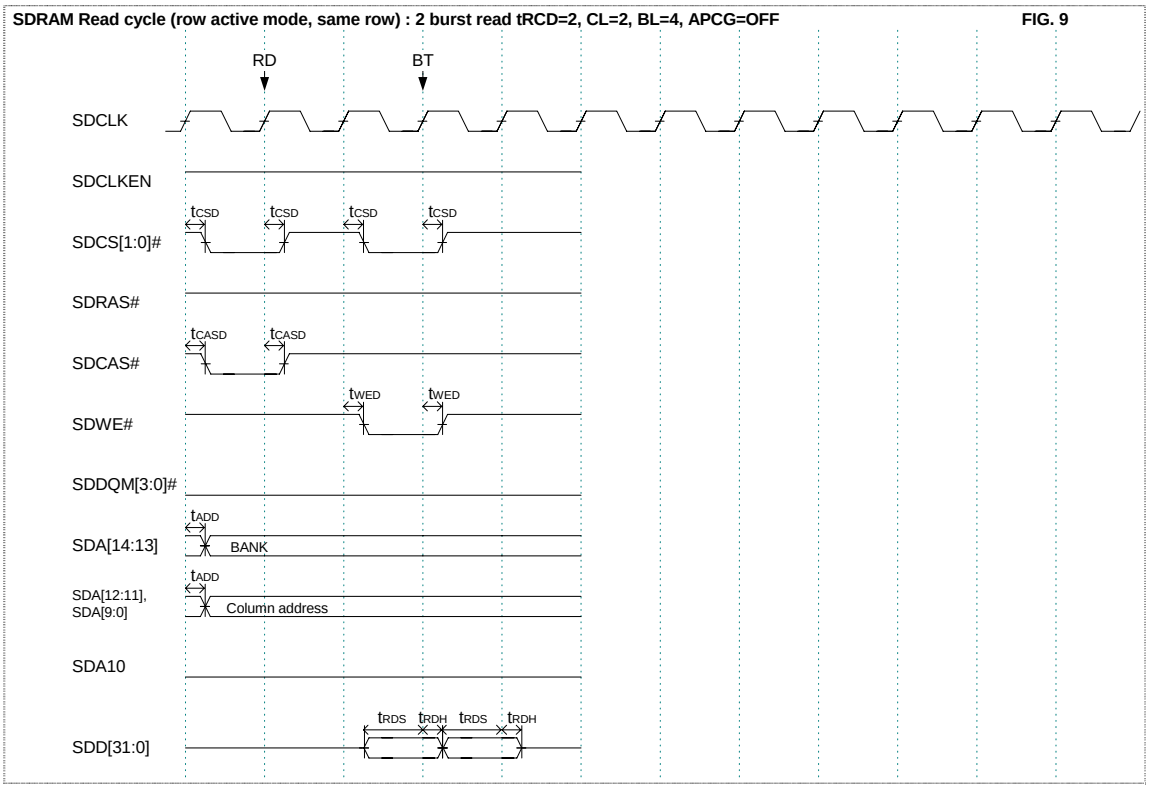


Figure 32.18 SDRAM Read Cycle, Row Active Mode 1 (Same row): 2 burst read cycles;tRCD=2, CL=2, BL=4, APCG=OFF

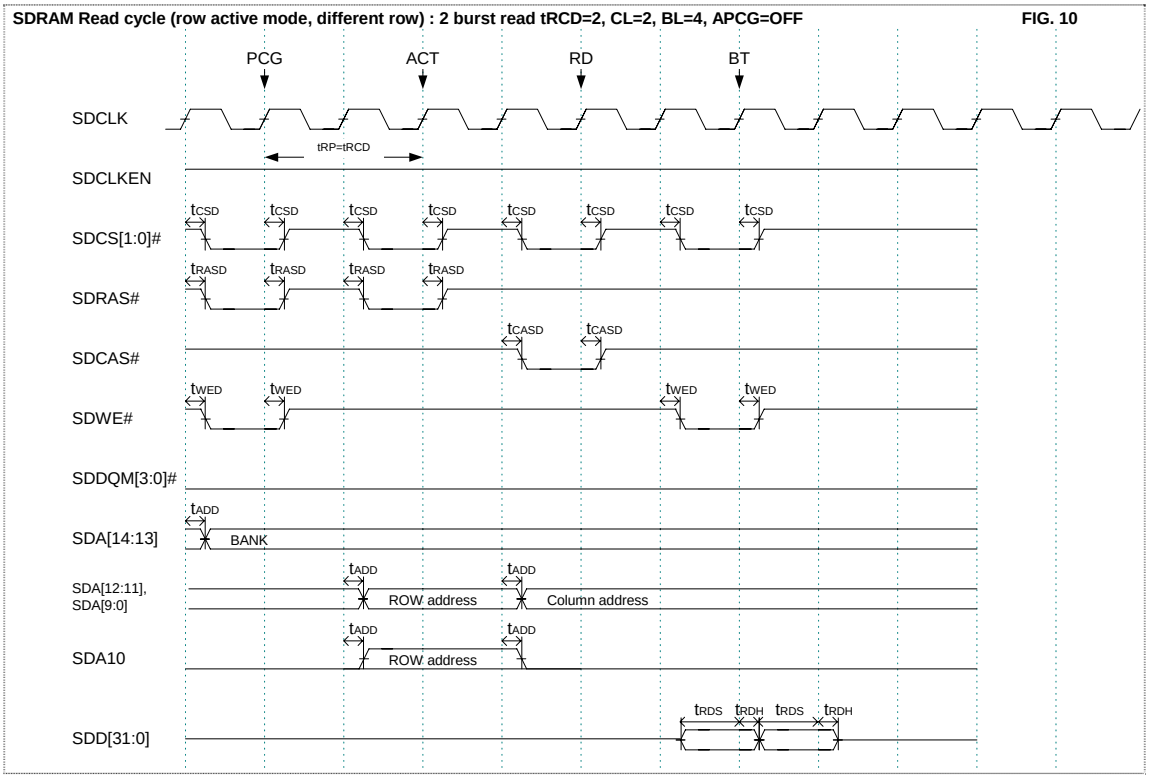


Figure 32.19 SDRAM Read Cycle, Row Active Mode 2 (Different row): 2 burst read cycles;tRCD=2, CL=2, BL=4, APCG=OFF

■ SDRAM Write Cycle (Row Active Mode)

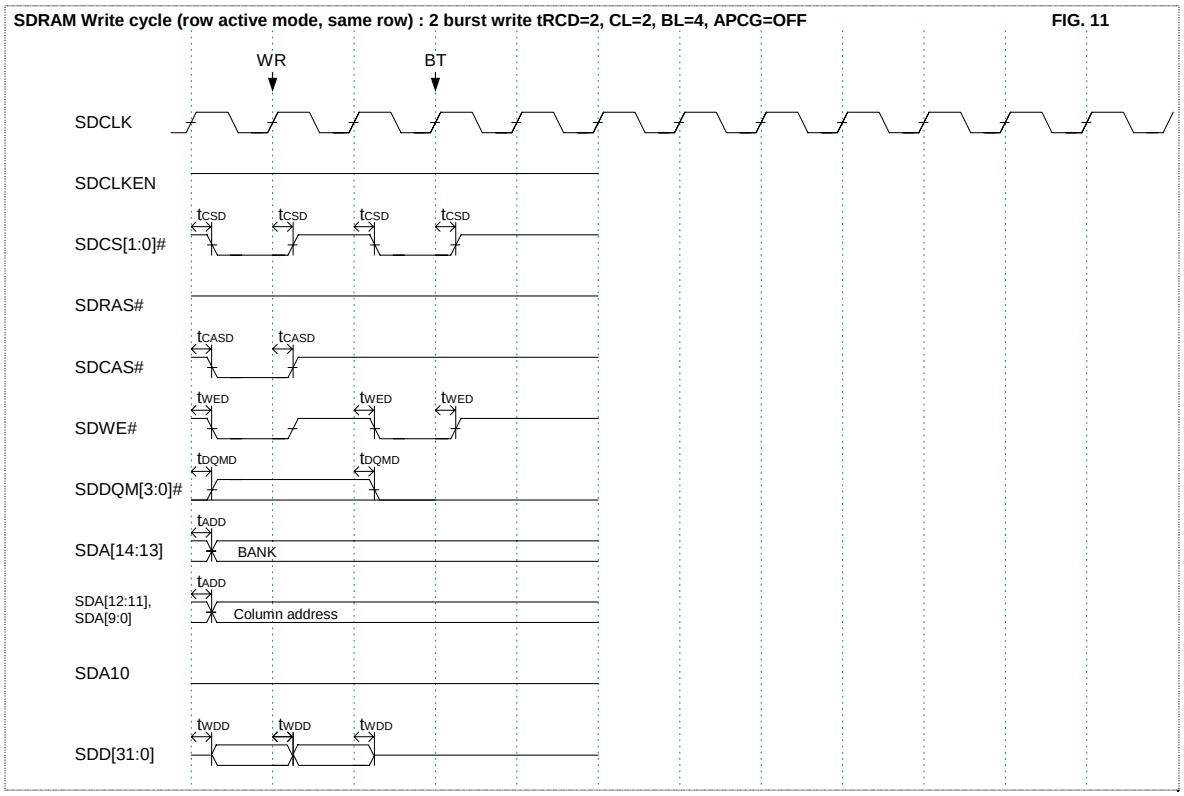


Figure 32.20 SDRAM Write Cycle, Row Active Mode 1 (Same row): 2 burst write cycles;tRCD=2, CL=2, BL=4, APCG=OFF

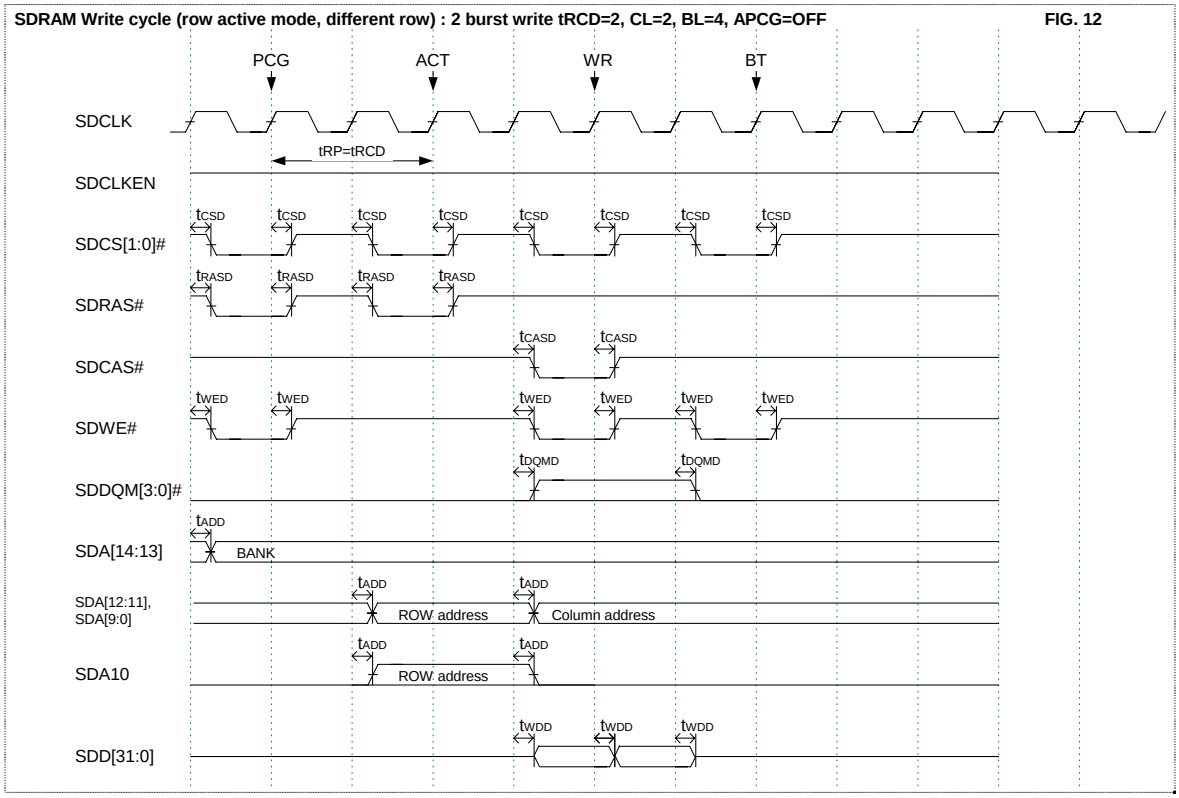


Figure 32.21 SDRAM Write Cycle, Row Active Mode 2 (Different row): 2 burst write cycles;tRCD=2, CL=2, BL=4, APCG=OFF

■ SDRAM Auto Refresh Cycle

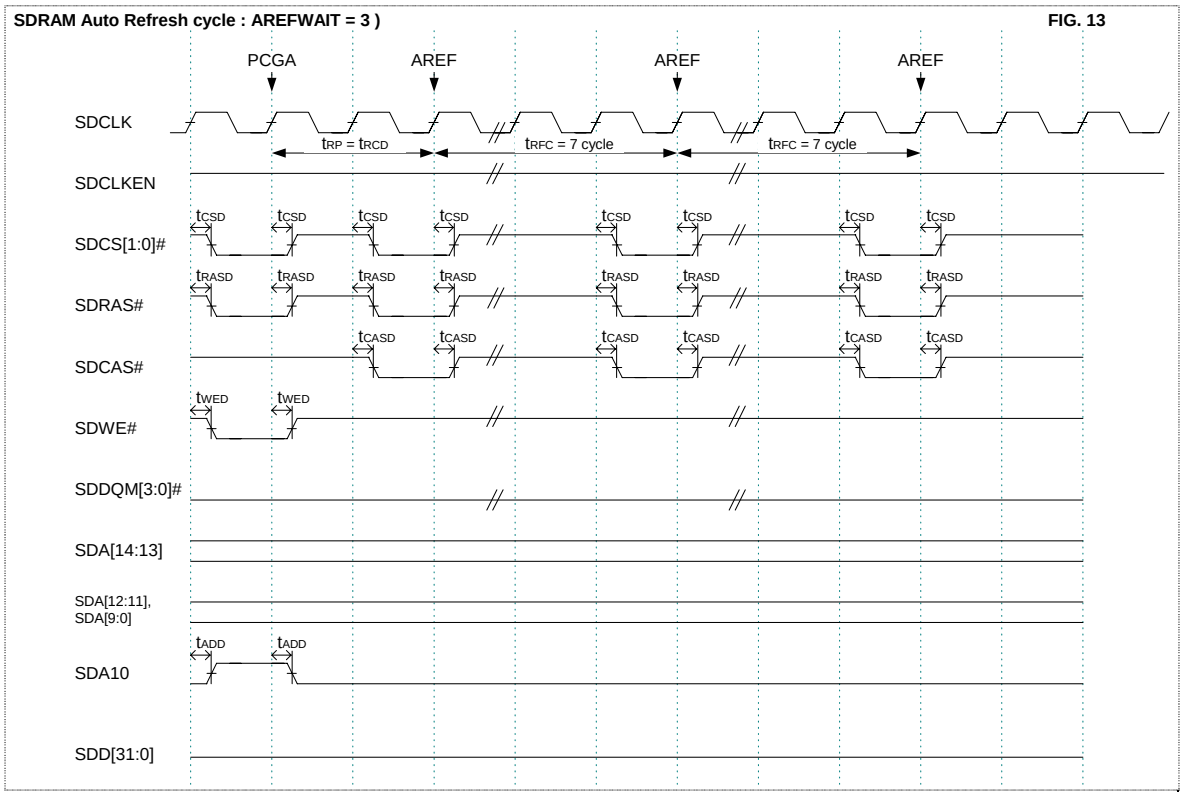


Figure 32.22 SDRAM Auto Refresh Cycle: AREFWAIT=3

■ SDRAM Self-Refresh Cycle

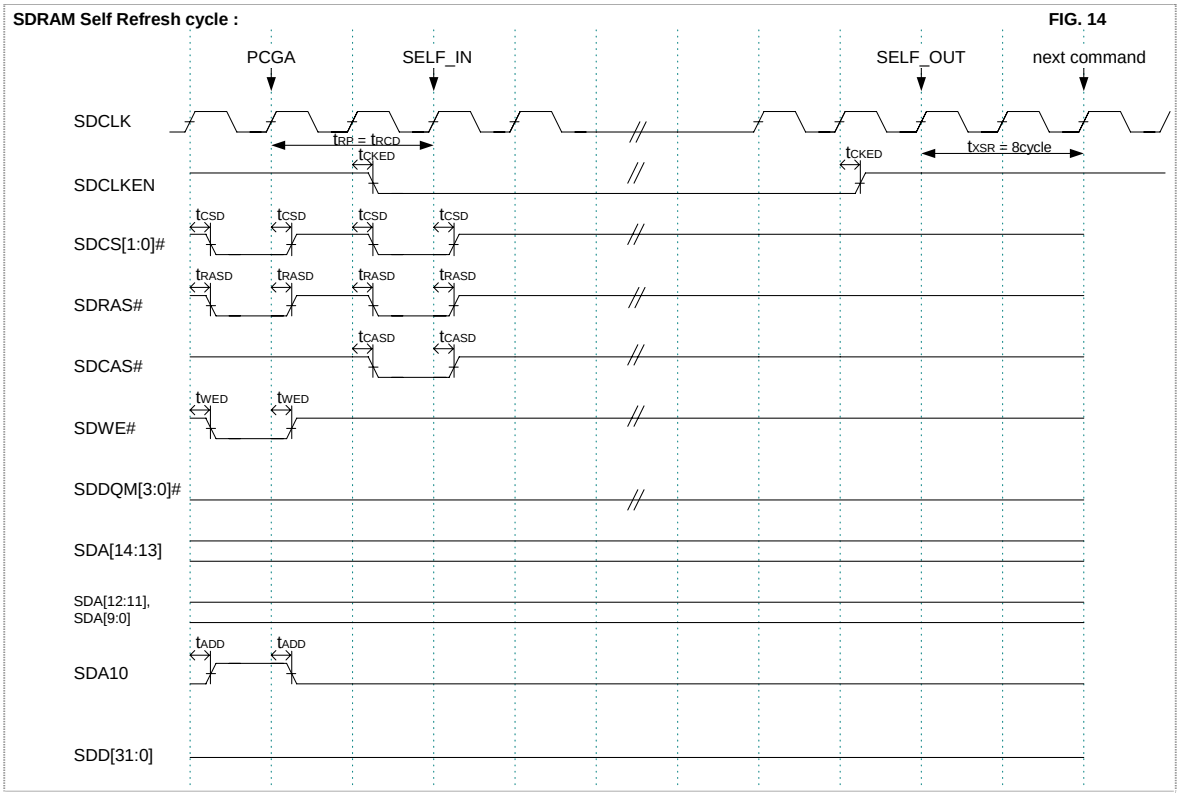


Figure 32.23 SDRAM Self-Refresh Cycle

■ SDRAM Initialization Cycle

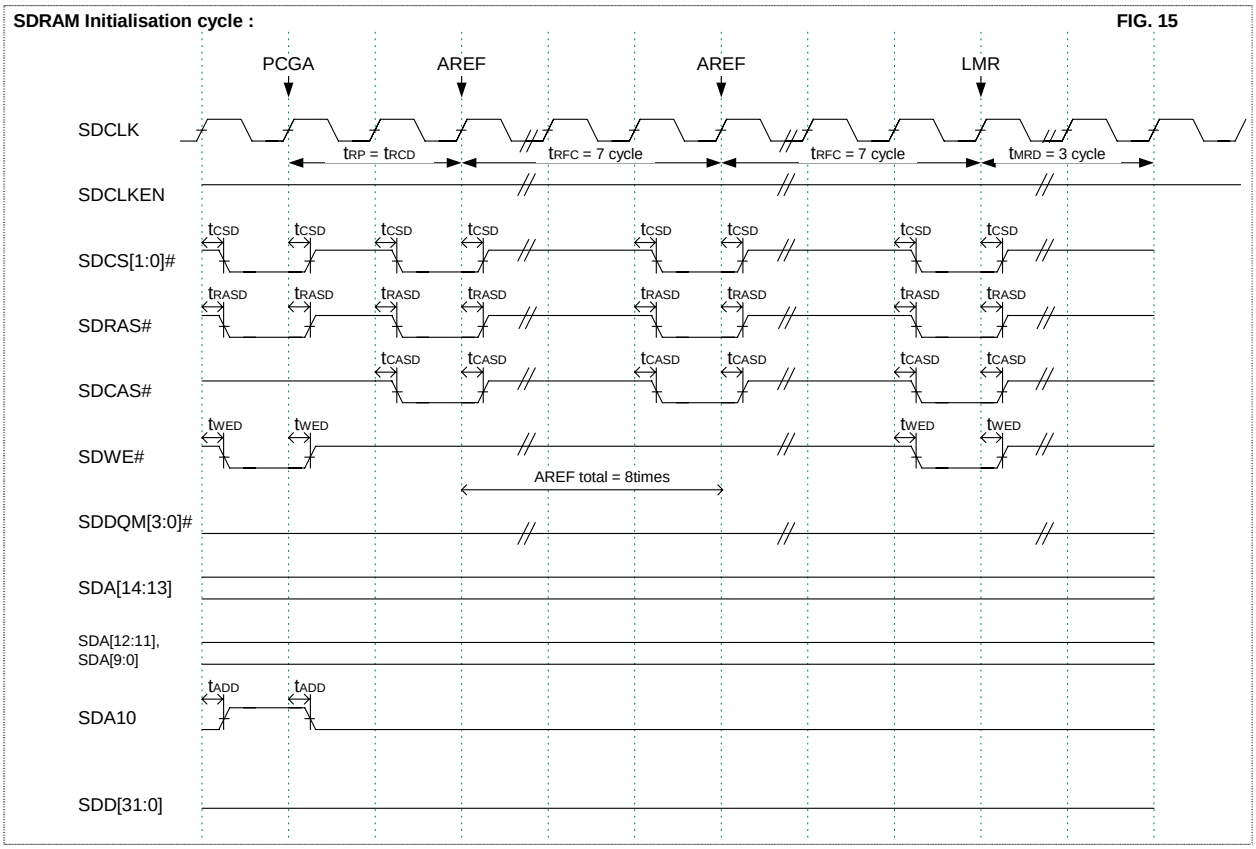


Figure 32.24 SDRAM Initialization Cycle

■ SDCLK/SDCLKEN Control

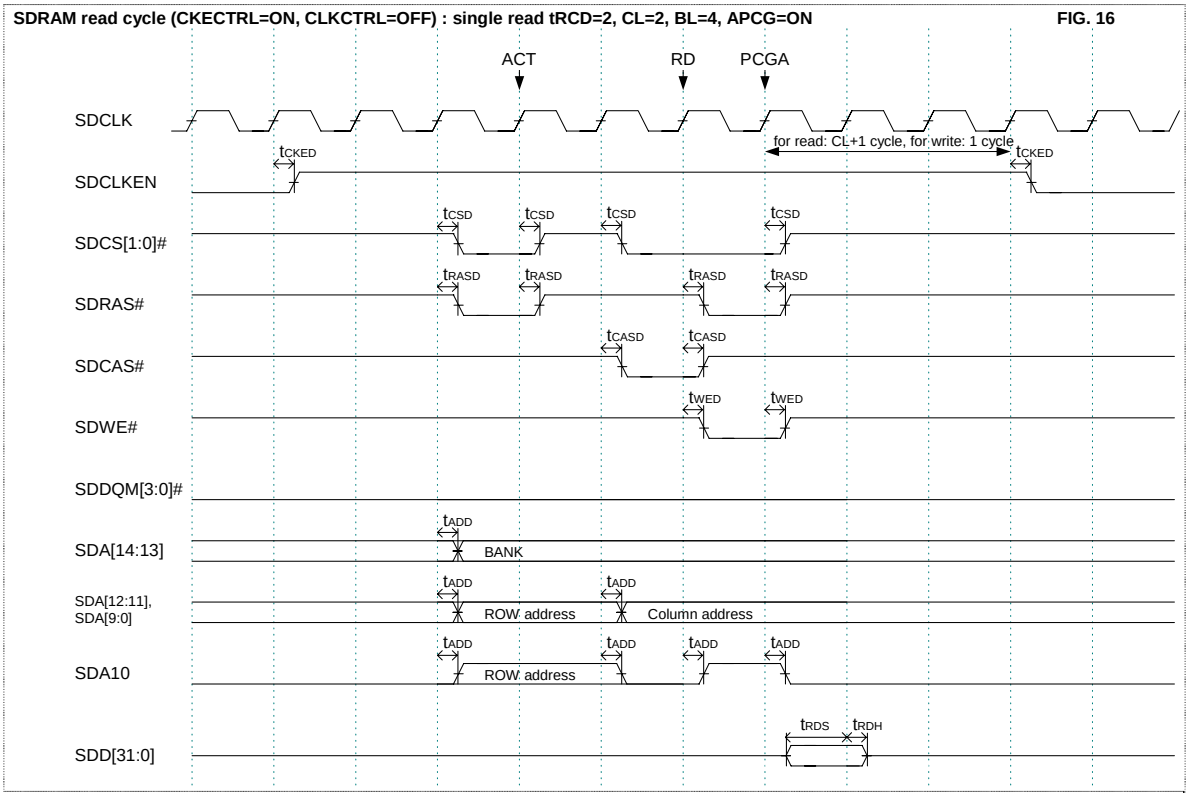


Figure 32.25 SDCLK/SDCLKEN Control 1 (CKECTRL=ON, CLKCTRL=OFF): Single read cycle; tRCD=2, CL=2, BL=4, APCG=ON

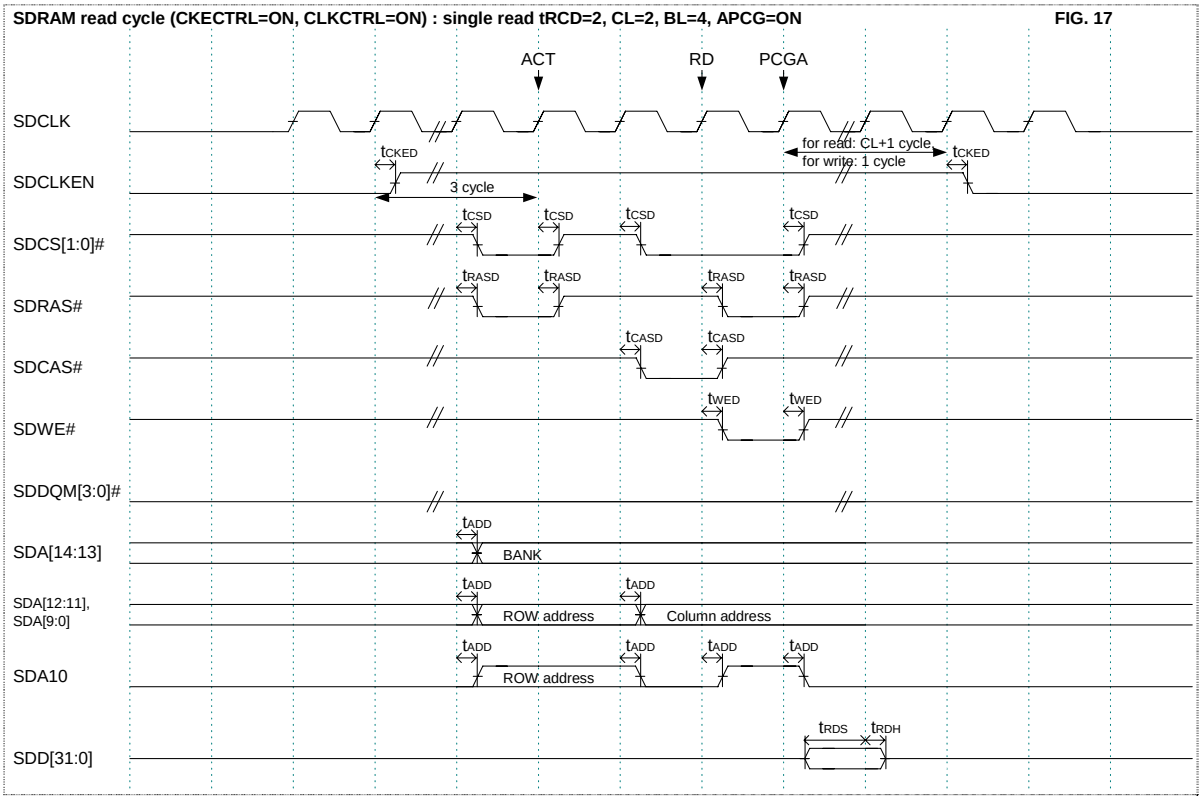


Figure 32.26 SDCLK/SDCLKEN Control 2 (CKECTRL=ON, CLKCTRL=ON): Single read cycle; tRCD=2, CL=2, BL=4, APCG=ON

32.2.3.6 I2C Single Master Core Module Timing

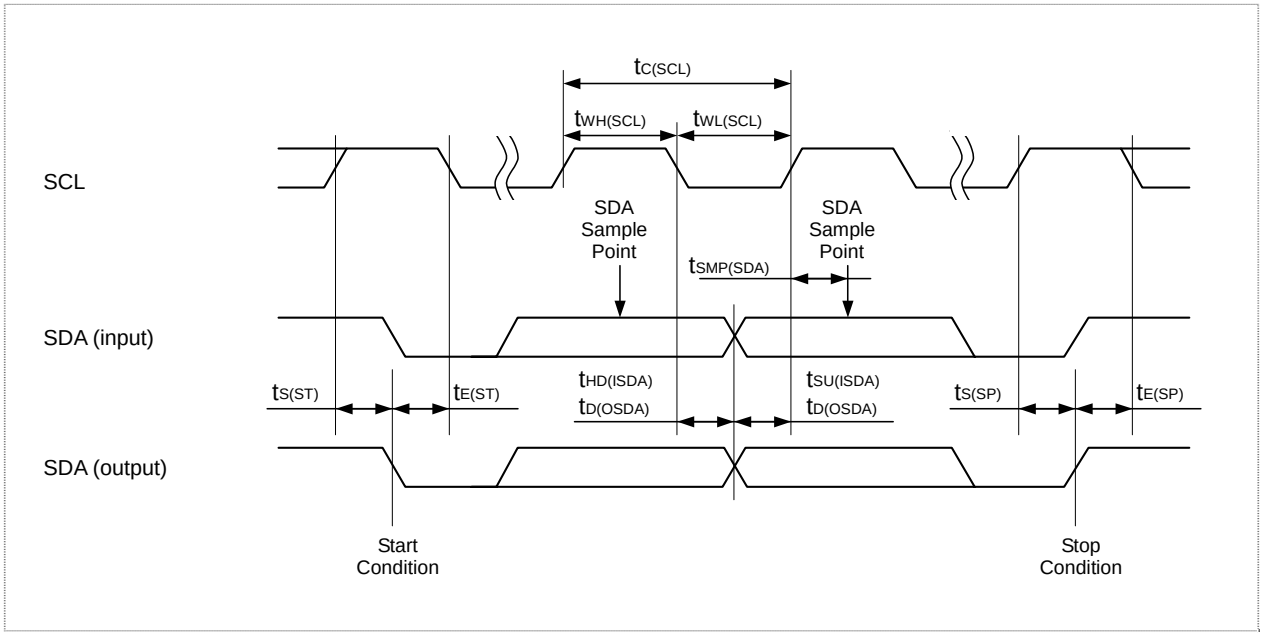


Figure 32.27 I2C Single Master Core Module Timing

32.2.3.7 I2STiming

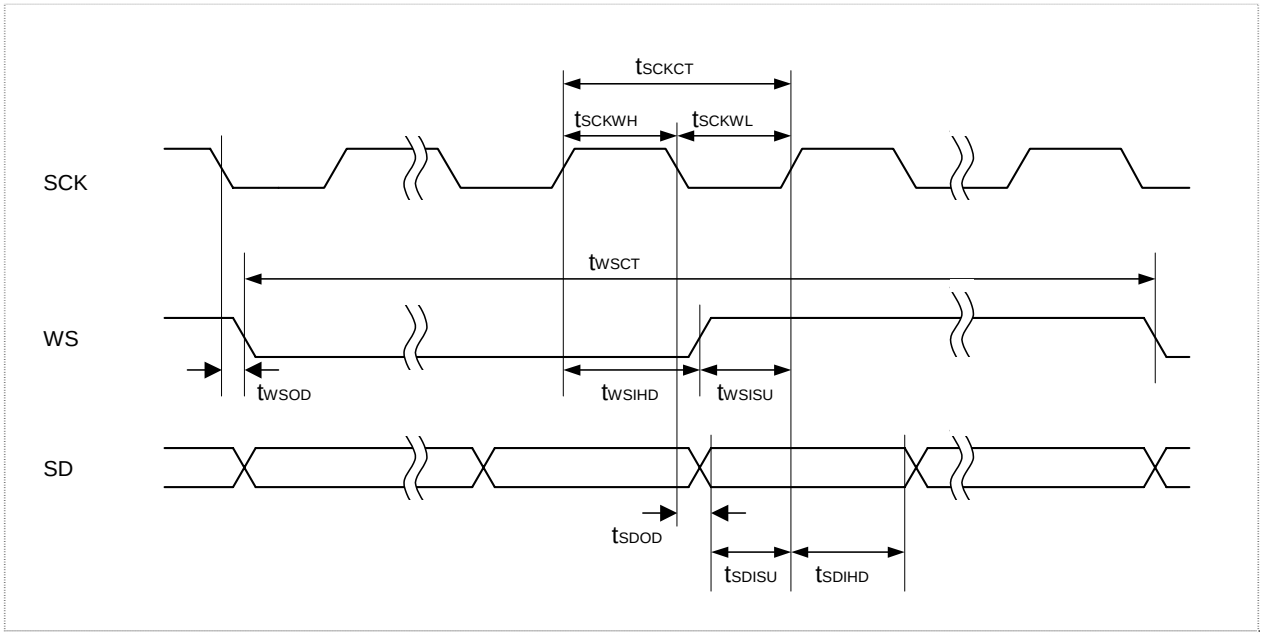


Figure 32.28 I2S Timing

32.2.3.8 Serial Peripheral Device Interface Timing

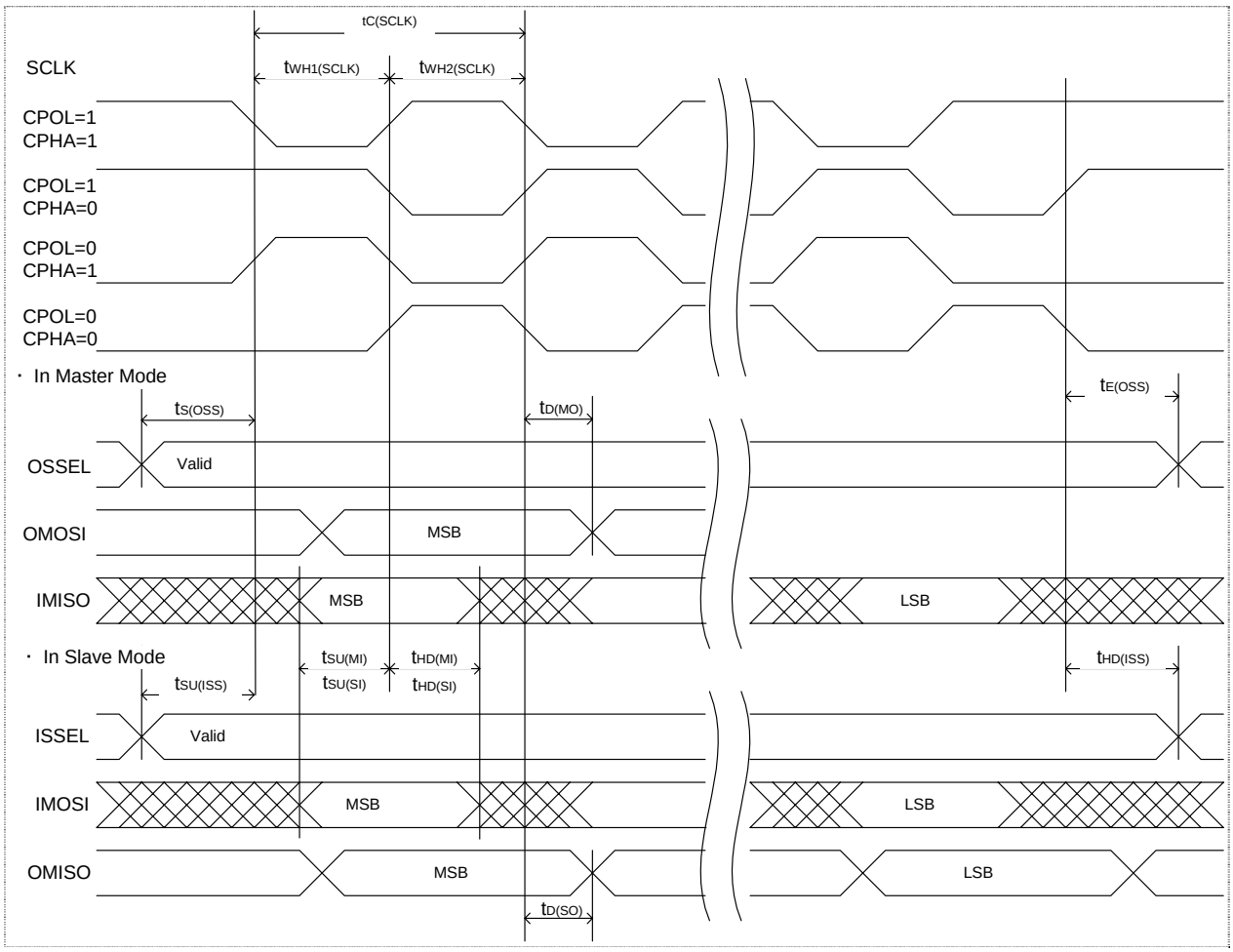


Figure 32.29 Serial Peripheral Device Interface Timing

32.2.3.9 Compact Flash Memory Interface (CF) Timing

■ CF Attribute Memory Read Cycle

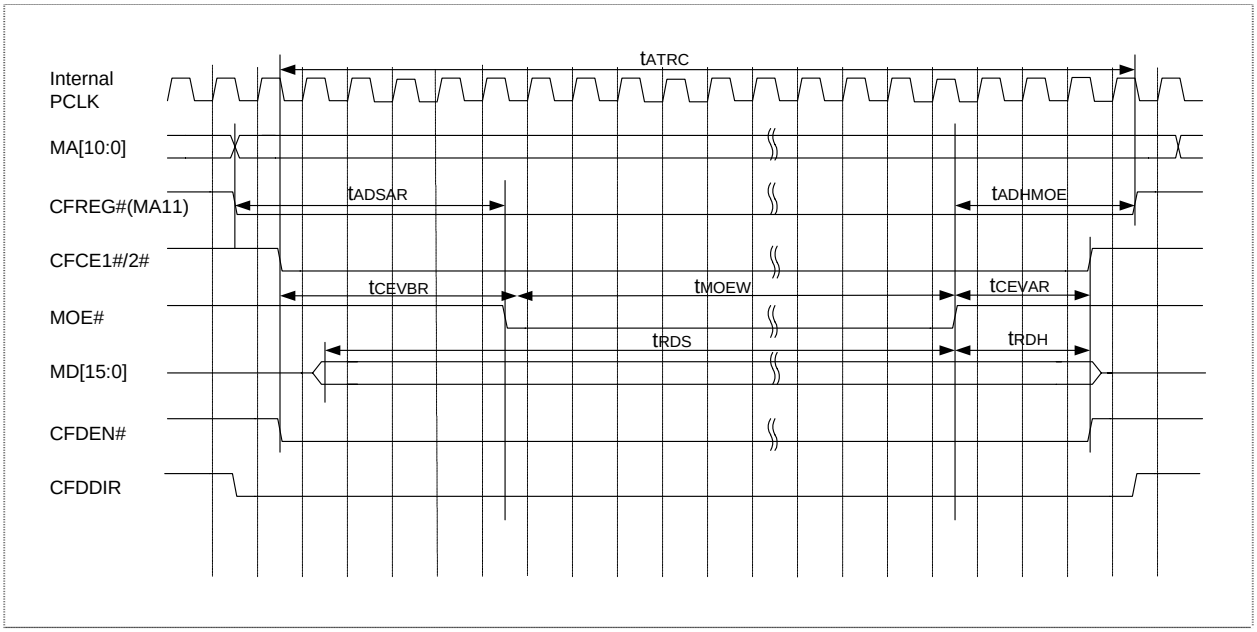


Figure 32.30 CF Attribute Memory Read Cycle

■ CF Attribute Memory Write Cycle

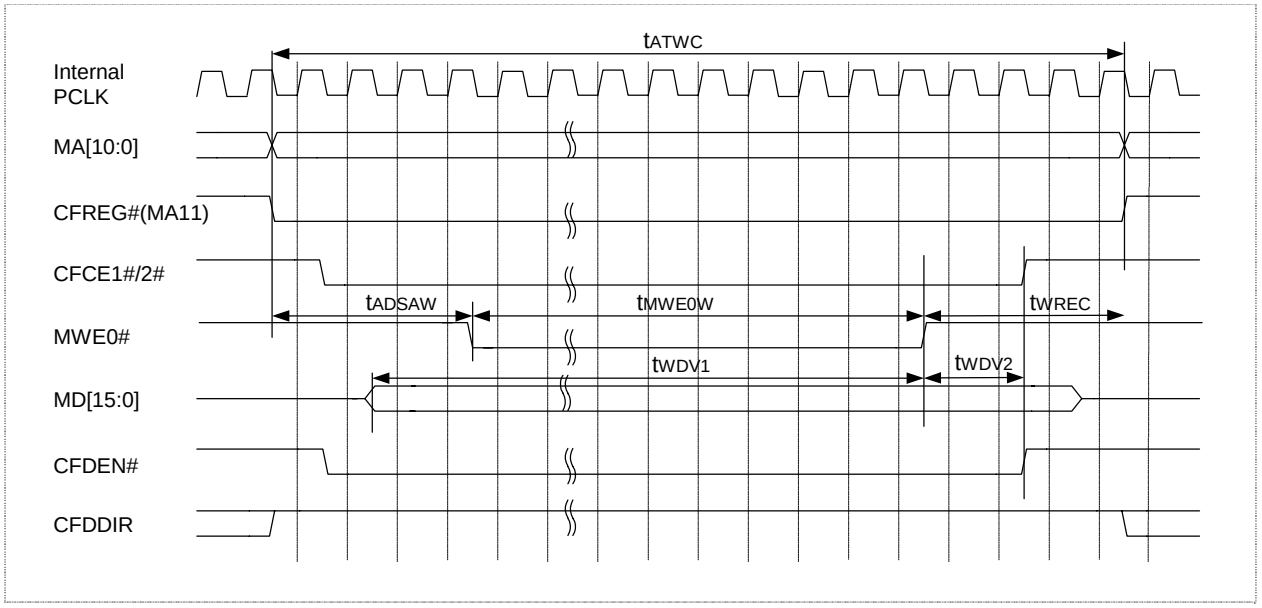


Figure 32.31 CF Attribute Memory Write Cycle

■ CF Common Memory Read Cycle

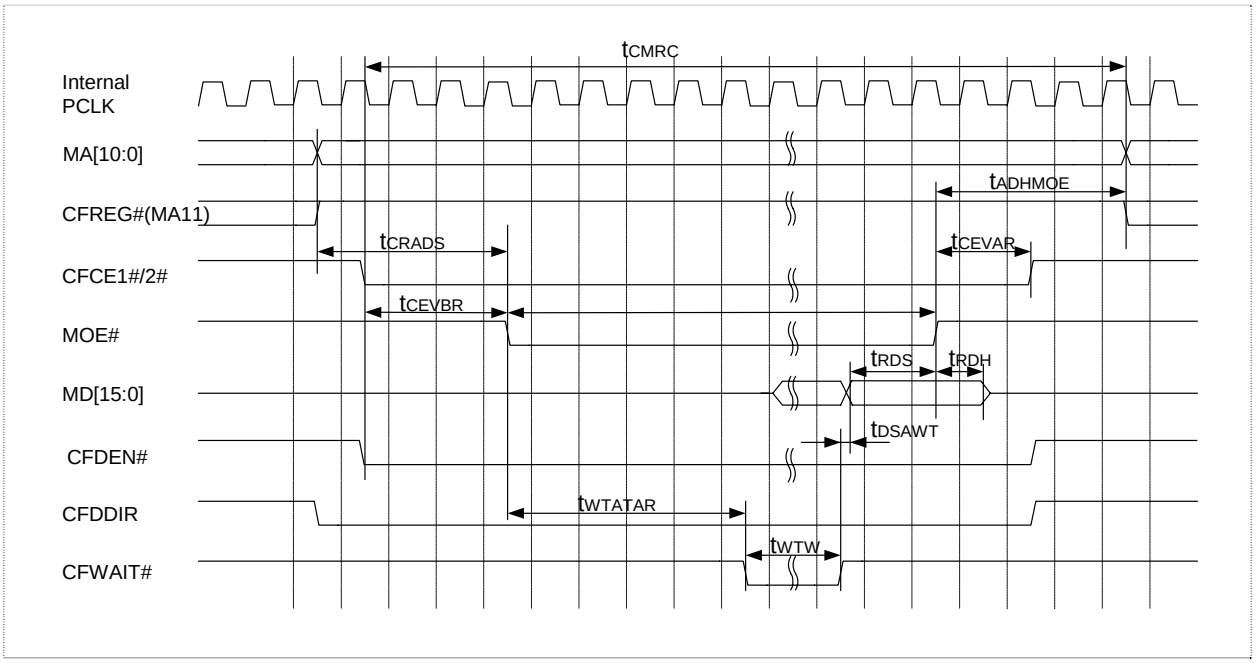


Figure 32.32 CF Common Memory Read Cycle

■ CF Common Memory Write Cycle

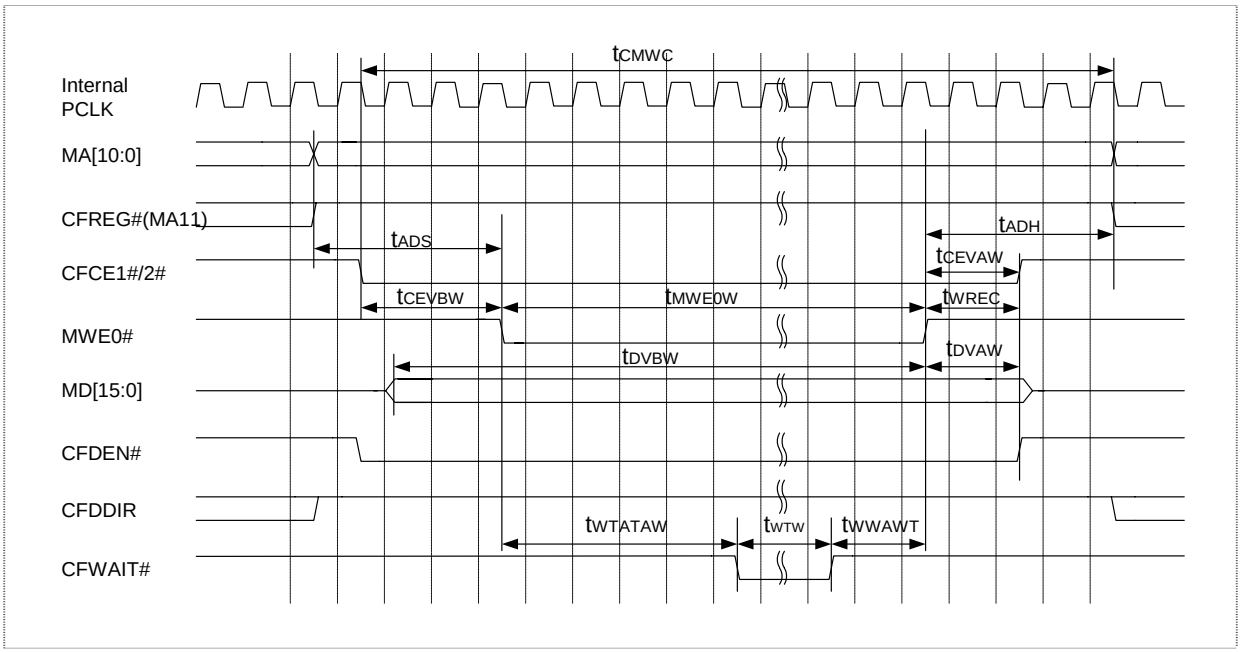


Figure 32.33 CF Common Memory Write Cycle

■ CF I/O Space/IDE Read Cycle

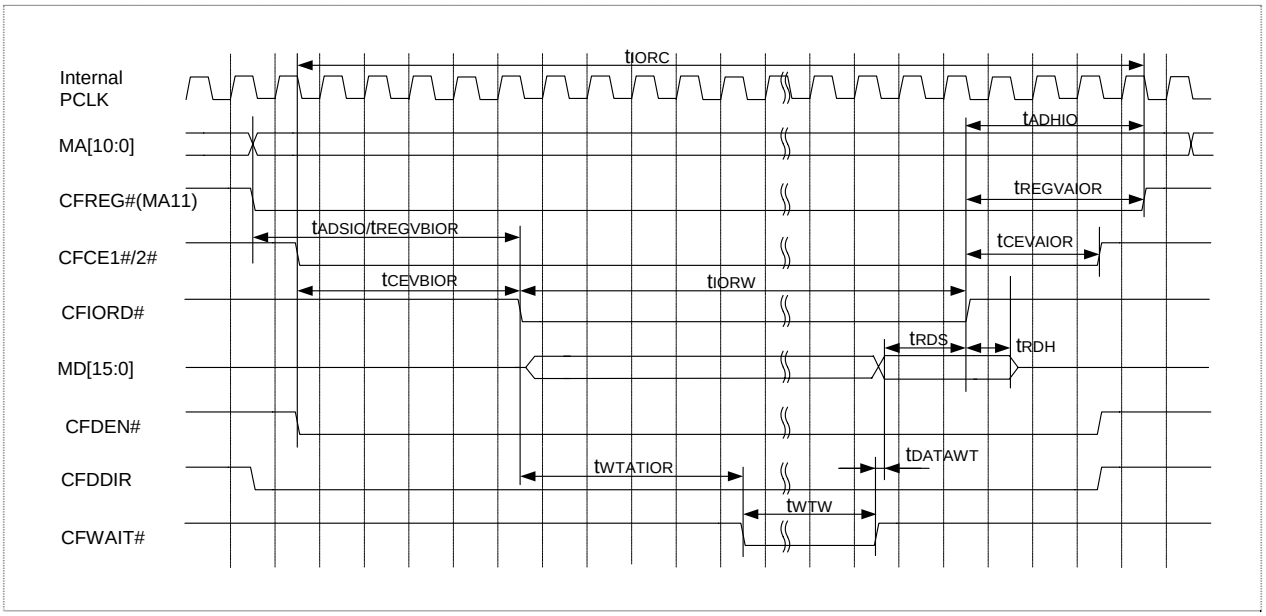


Figure 32.34 CF I/O Space/IDE Read Cycle

■ CF I/O Space/IDE Write Cycle

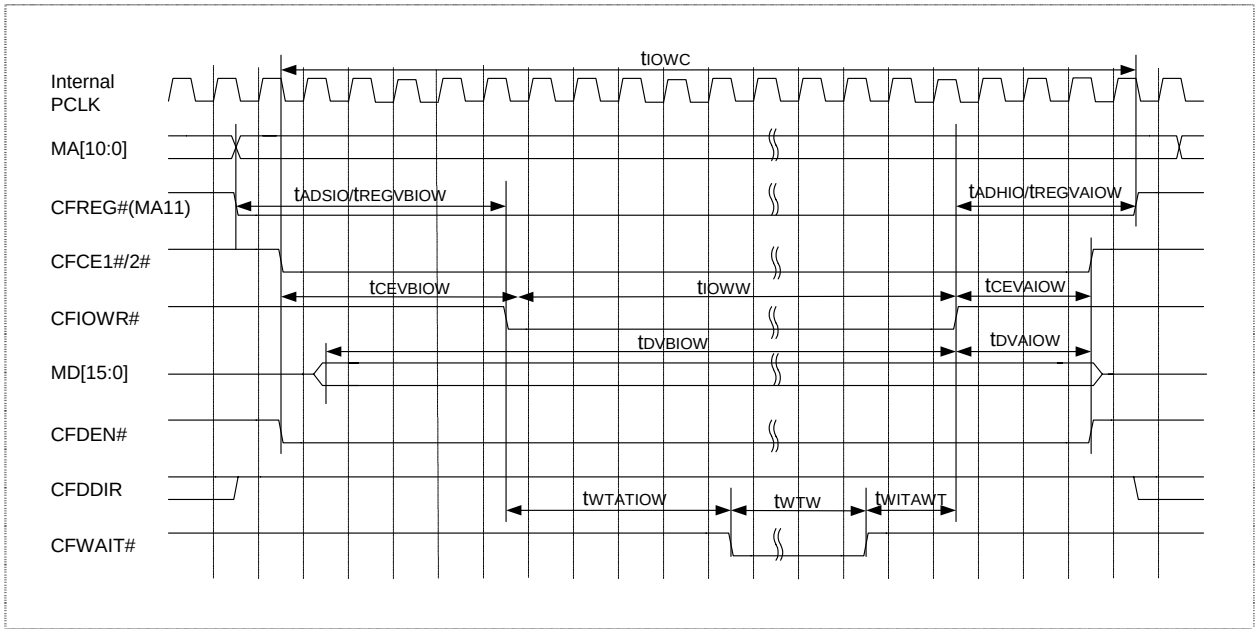


Figure 32.35 CF I/O Space/IDE Write Cycle

33. EXTERNAL CONNECTION EXAMPLES (REFERENCE)

33.1 Memory Connection Examples

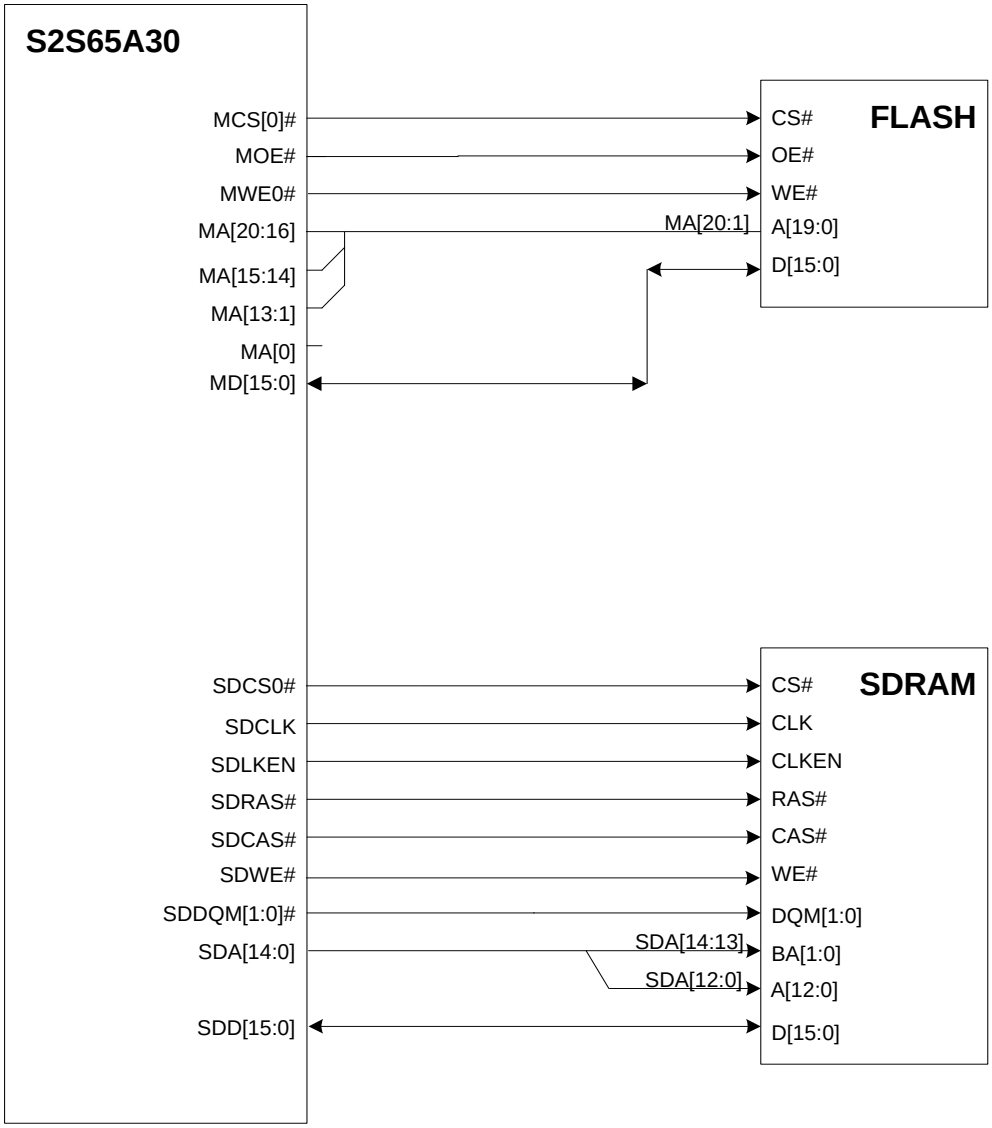


Figure 33.1 Memory Connection Example (1)

Note: Connect SDMA[14:13] to the SDRAM bank address (BA[1:0]).

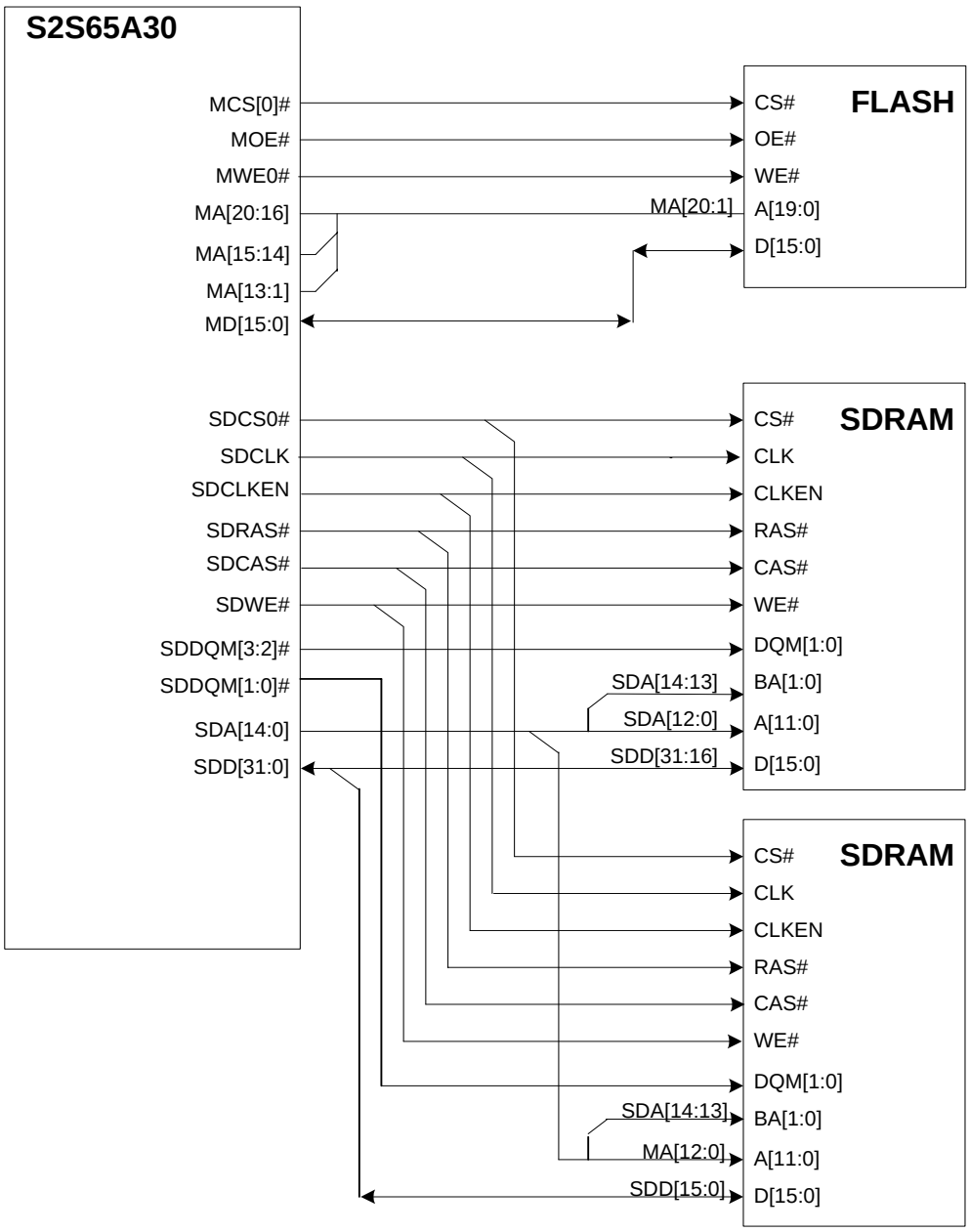


Figure 33.2 Memory Connection Example (2)

Note: Connect SDA[14:13] to the SDRAM bank address (BA[1:0]).

33.2 Compact Flash Memory Connection Example (for 16-Bit Bus Support Model)

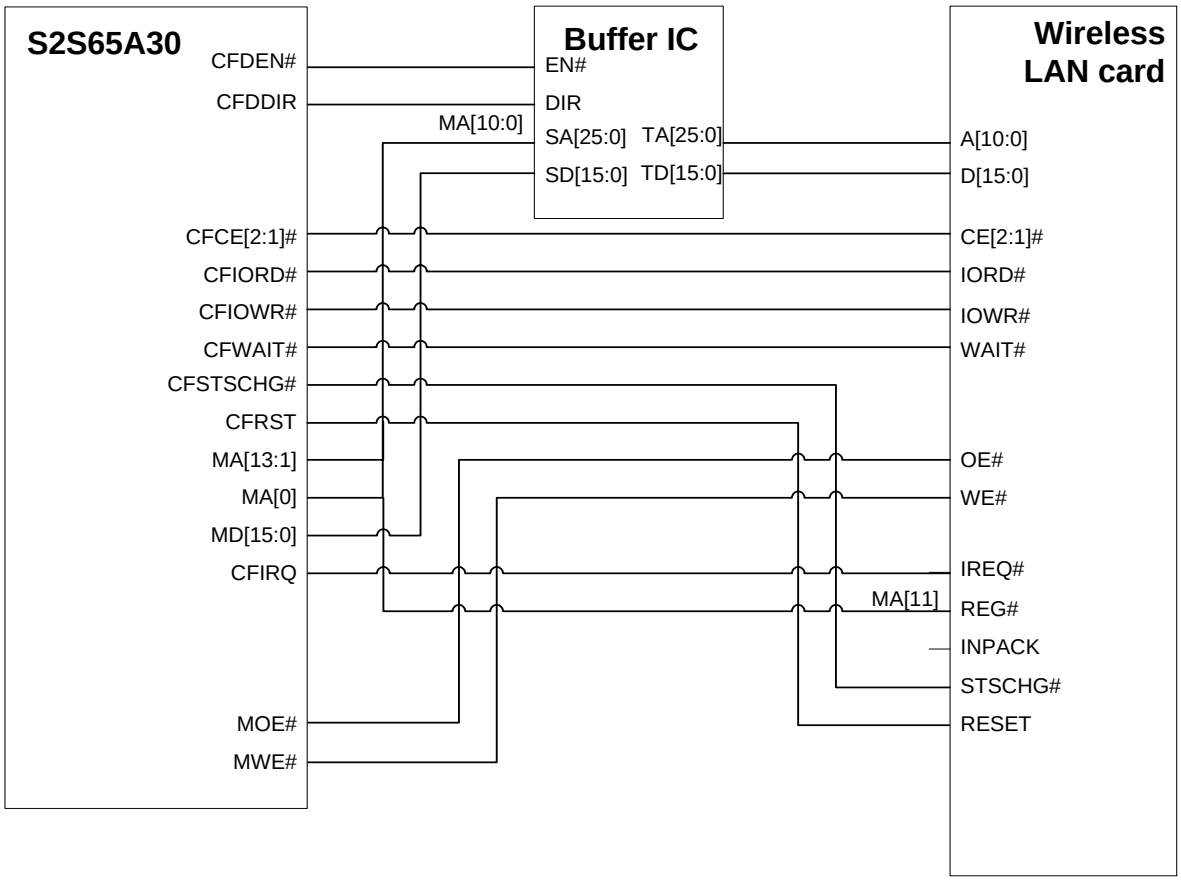
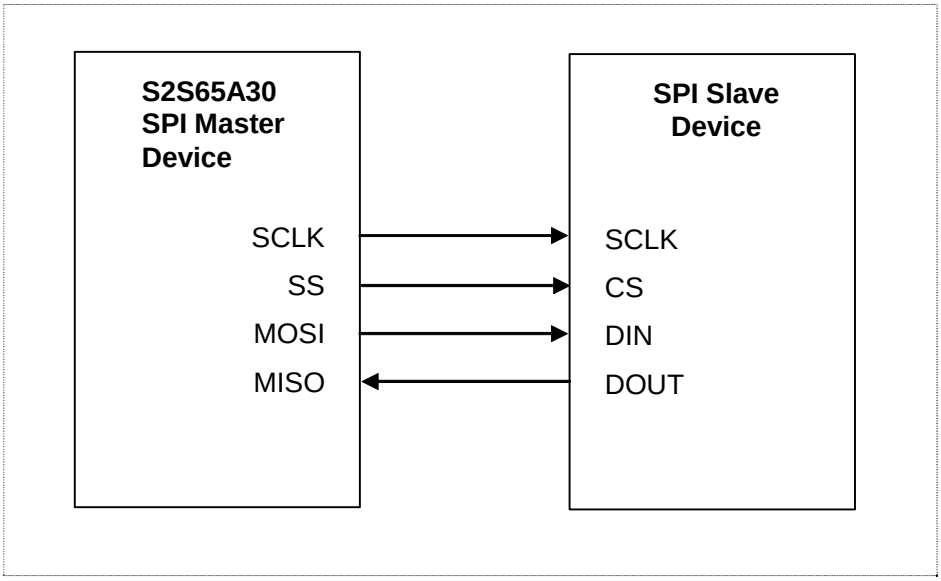


Figure 33.3 Compact Flash Memory I/F Connection Example

33.3 Serial Peripheral Device Interface (SPI) Connection Examples

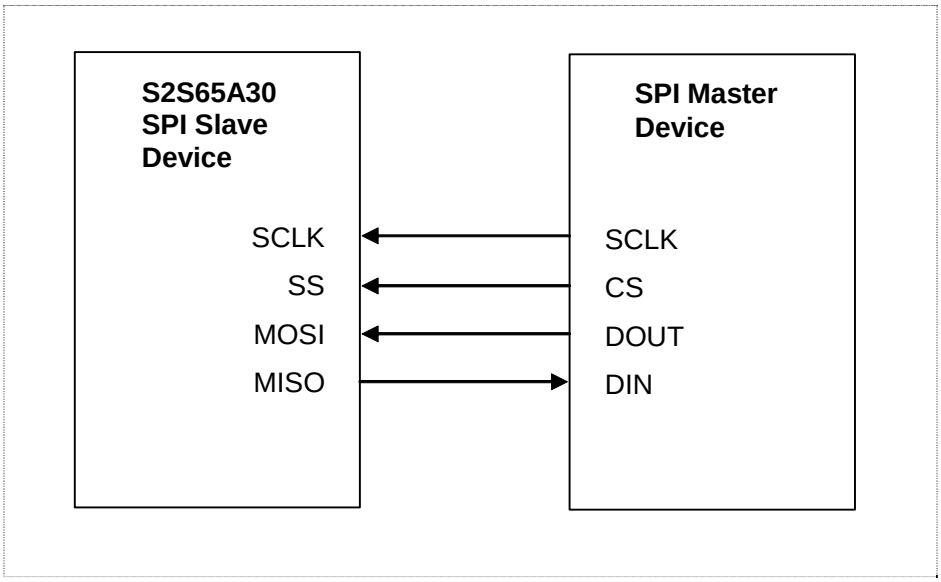
33.3.1 Master Mode

A connection example if S2S65A30 is used as master device



33.3.2 Slave Mode

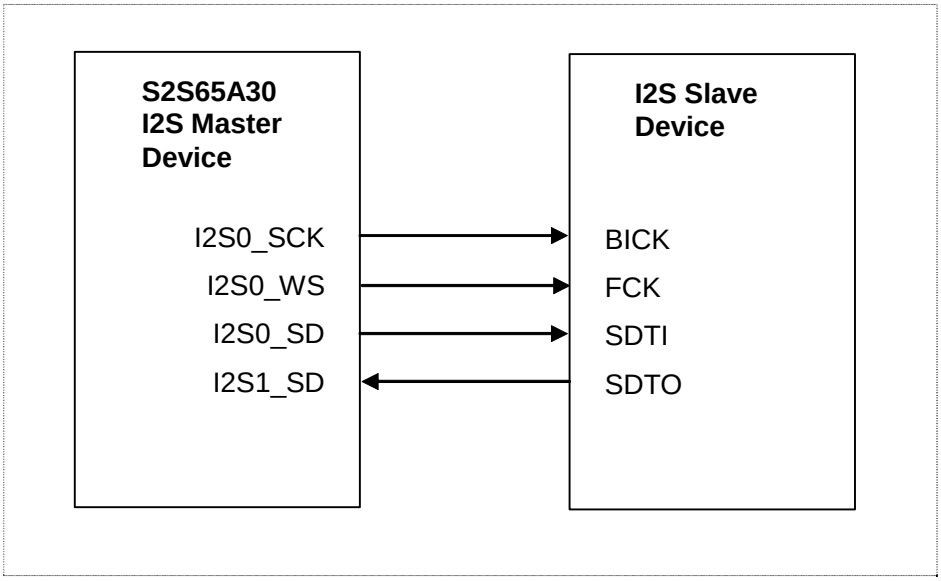
A connection example if S2S65A30 is used as slave device



33.4 I²S Connection Examples

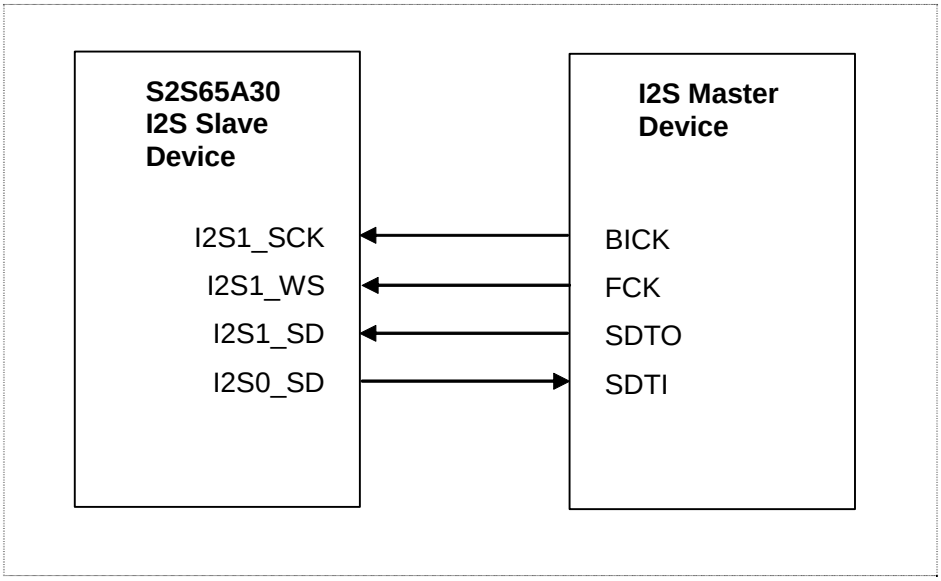
33.4.1 Master Mode

A connection example if S2S65A30 is used as master device.



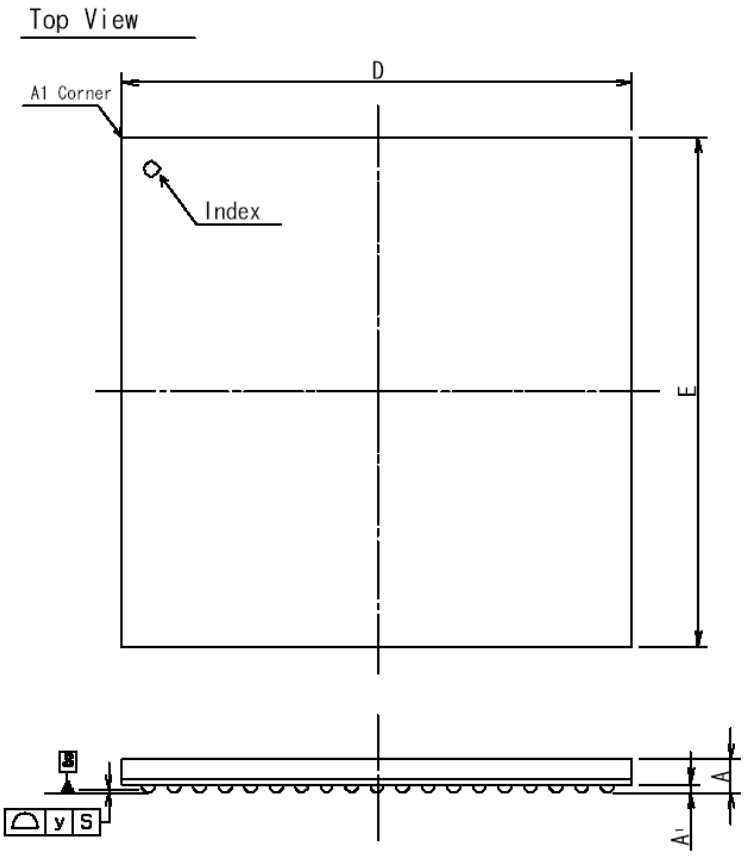
33.4.2 Slave Mode

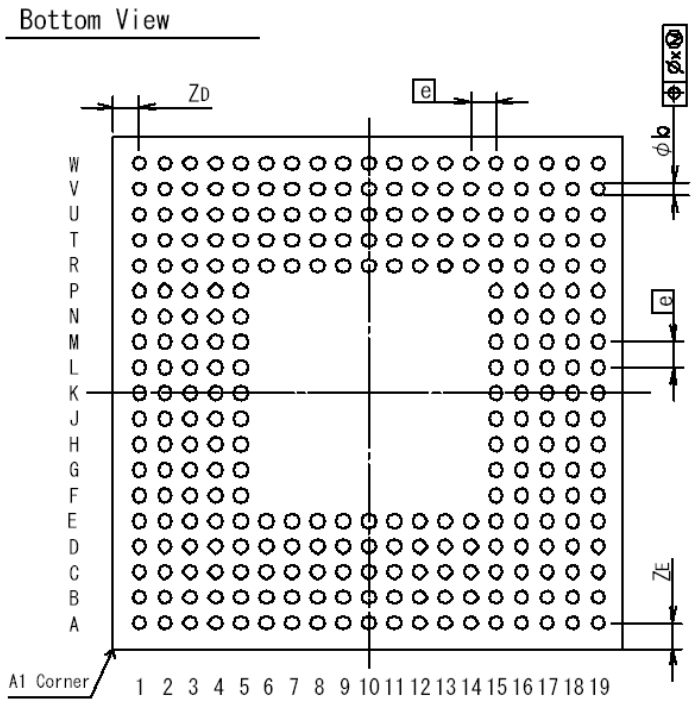
A connection example if S2S65A30 is used as slave device.



34. EXTERNAL DIMENSIONS

34.1 Plastic TFBGA 280pin Body size 16x16x1.2mm (PFBGA16U-280)





Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	16	—
E	—	16	—
A	—	—	1.2
A1	—	0.3	—
e	—	0.8	—
b	0.38	—	0.48
x	—	—	0.08
y	—	—	0.1
ZD	—	0.8	—
ZE	—	0.8	—

1 = 1mm

Figure 34.1 Package Dimensions (PFBGA16U-280PIN)

35. APPENDIX 1 S2S65A30 INTERNAL REGISTER LIST

Address (Hex)	Register Name		Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFD_1000	**IPC&INTIM2**		**IPC2**			
0xFFFD_1000	IPC Camera Input Mode Setup		INMODE	0x0000	R/W	16/8
0xFFFD_1010	IPC Camera Input Setting		INCONFIG	0x0001	R/W	16/8
0xFFFD_1108	IPC X-Direction Start Position Setting		XSTART	0x0001	R/W	16/8
0xFFFD_110C	IPC Y-Direction Start Position Setting/ ODD Field Start Position Setting		YSTART/ YSTART_O	0x0001	R/W	16/8
0xFFFD_1110	IPC EVEN Field Y-Direction Start Position Setting		YSTART_E	0x0001	R/W	16/8
0xFFFD_1140	IPC Interrupt Setting		INTSEL	0x0000	R/W	16/8
0xFFFD_1200	IPC Scaler Setting		CONTROL	0x0001	R/W	16/8
0xFFFD_1400	IPC Conversion Buffer SDRAM Start Address 1		IPCBUF_SADR_L	0x0000	R/W	16/8
0xFFFD_1404	IPC Conversion Buffer SDRAM Start Address 2		IPCBUF_SADR_H	0x0000	R/W	16/8
0xFFFD_1510	IPC Video Output X-Direction Effective Pixels		VOUT_HD	0x0280	R/W	16
0xFFFD_1520	IPC Video Output X-Direction Length Setting		VOUT_HT	0x02DA	R/W	16
0xFFFD_1534	IPC Video Output Vertical Blank Line Number		VOUT_VP	0x0001	R/W	16
0xFFFD_1540	IPC Video Output Y-Direction Effective Pixels		VOUT_VD	0x01E0	R/W	16
0xFFFD_1700	IPC Interlaced_to_Progressive Conversion Mode		IPC_MODE	0x0080	R/W	16/8
0xFFFD_1800	IPC Sync Signal Output Polarity Setting		OUTCONFIG	0x0003	R/W	16/8
0xFFFD_1804	IPC Image Correction Circuit Bypass Setting		BYPASS	0x0000	R/W	16/8
0xFFFD_1808	IPC Image Correction Setting Update Register		UPDATE	0x0000	R/W	16/8
0xFFFD_180C_ 19FC	Correction Value Setting Register Area					
0x FFFD_3000	**TIMB Related Register**		**TIMB**			
0x FFFD_3000	Timer-B Mode Control Register		TIMBMDC	0x0000	R/W	16(/32)
0x FFFD_3004	Timer-B Counter Control Register		TIMBCNTC	0x0000	R/W	16(/32)
0x FFFD_3008	Timer-B Status Register		TIMBSTS	0x0000	R/W	16(/32)
0x FFFD_300C	Timer-B Interrupt Enable Register		TIMBINTEN	0x0000	R/W	16(/32)
0x FFFD_3010	Timer-B Count Register		TIMBCNT	0x0000	R/W	16(/32)
0x FFFD_3014	Timer-B Common Control Register		TIMBCOMC	0x0000	R/W	16(/32)
0x FFFD_3018	Timer-B I/O Control Register		TIMBIO	0x0000	R/W	16(/32)
0x FFFD_301C	Timer-B Cycle Register		TIMBDUTY	0x0000	R/W	16(/32)
0x FFFD_3020	Timer-B COMMON_0 Register		TIMBCOM0	0x0000	R/W	16(/32)
0x FFFD_3024	Timer-B COMMON_1 Register		TIMBCOM1	0x0000	R/W	16(/32)
0x FFFD_3028	Timer-B COMMON_2 Register		TIMBCOM2	0x0000	R/W	16(/32)
0x FFFD_302C	Timer B COMMON_3 Register		TIMBCOM3	0x0000	R/W	16(/32)
0x FFFD_3030	Timer B COMINP_0 Register		TIMBINP0	0x0000	RO	16(/32)
0x FFFD_3034	Timer B COMINP_1 Register		TIMBINP1	0x0000	RO	16(/32)
0x FFFD_3038	Timer B COMINP_2 Register		TIMBINP2	0x0000	RO	16(/32)
0x FFFD_303C	Timer B COMINP_3 Register		TIMBINP3	0x0000	RO	16(/32)
0x FFFD_4000	**DLAB**	**UART2 Related Register**	**UART2**			
0x FFFD_4000	0	Receive Buffer Register	RBR	0x 00	RO	8 (/16/32)
0x FFFD_4000	0	Send Holding Register	THR	—	WO	8 (/16/32)
0x FFFD_4000	1	Divider Latch LSB Register	DLL	0x 00	R/W	8 (/16/32)
0x FFFD_4004	0	Interrupt Enable Register	IER	0x 00	R/W	8 (/16/32)
0x FFFD_4004	1	Divider Latch MSB Register	DLM	0x 00	R/W	8 (/16/32)
0x FFFD_4008	Interrupt Identification Register		IIR	0x 01	RO	8 (/16/32)
0x FFFD_4008	FIFO Control Register		FCR	—	WO	8 (/16/32)
0x FFFD_400C	Line Control Register		LCR	0x 60	R/W	8 (/16/32)
0x FFFD_4010	Modem Control Register		MCR	0x EX	R/W	8 (/16/32)

35. APPENDIX 1 S2S65A30 INTERNAL REGISTER LIST

Address (Hex)	Register Name		Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFD_4014	Line Status Register		LSR	0x 00	RO	8 (/16/32)
0x FFFD_4018	Modem Status Register		MSR	0x 00	RO	8 (/16/32)
0x FFFD_401C	Scratch Register		SCR	0x 00	R/W	8 (/16/32)
0x FFFD_4020	Test-0 Register		T0	0x 00	R/W	8 (/16/32)
0x FFFD_4024	Test-1 Register		T1	0x 00	R/W	8 (/16/32)
0x FFFD_4028	Test Status 0 Register		TS0	—	RO	8 (/16/32)
0x FFFD_402C	Test Status 1 Register		TS1	0x 01	RO	8 (/16/32)
0x FFFD_4030	Test Status 2 Register		TS2	0x 0F	RO	8 (/16/32)
0x FFFD_403C	Test Status 3 Register		TS3	0x 02	RO	8 (/16/32)
0x FFFD_5000	**DLAB**	**UART3 Related Register**	**UART3**			
0x FFFD_5000	0	Receive Buffer Register	RBR	0x 00	RO	8 (/16/32)
0x FFFD_5000	0	Send Holding Register	THR	—	WO	8 (/16/32)
0x FFFD_5000	1	Divider Latch LSB Register	DLL	0x 00	R/W	8 (/16/32)
0x FFFD_5004	0	Interrupt Enable Register	IER	0x 00	R/W	8 (/16/32)
0x FFFD_5004	1	Divider Latch MSB Register	DLM	0x 00	R/W	8 (/16/32)
0x FFFD_5008	Interrupt Identification Register		IIR	0x 01	RO	8 (/16/32)
0x FFFD_5008	FIFO Control Register		FCR	—	WO	8 (/16/32)
0x FFFD_500C	Line Control Register		LCR	0x 00	R/W	8 (/16/32)
0x FFFD_5010	Modem Control Register		MCR	0x 00	R/W	8 (/16/32)
0x FFFD_5014	Line Status Register		LSR	0x 60	RO	8 (/16/32)
0x FFFD_5018	Modem Status Register		MSR	0x EX	RO	8 (/16/32)
0x FFFD_501C	Scratch Register		SCR	0x 00	R/W	8 (/16/32)
0x FFFD_5020	Test-0 Register		T0	0x 00	R/W	8 (/16/32)
0x FFFD_5024	Test-1 Register		T1	0x 00	R/W	8 (/16/32)
0x FFFD_5028	Test Status 0 Register		TS0	—	RO	8 (/16/32)
0x FFFD_502C	Test Status 1 Register		TS1	0x 01	RO	8 (/16/32)
0x FFFD_5030	Test Status 2 Register		TS2	0x 0F	RO	8 (/16/32)
0x FFFD_503C	Test Status 3 Register		TS3	0x 02	RO	8 (/16/32)
0x FFFD_8000	**Camera-2 Interface Related Register**		**CAM2**			
0x FFFD_8000	Camera-2 Clock Cycle Setting Register			0x 0000	R/W	16
0x FFFD_8004	Camera-2 Signal Setting Register			0x 0000	R/W	16
0x FFFD_8008 to 0x FFFD_801C	Reserved			—	—	—
0x FFFD_8020	Camera-2 Mode Setting Register			0x 0000	R/W	16
0x FFFD_8024	Camera-2 Frame Control Register			0x 0000	R/W	16
0x FFFD_8028	Camera-2 Control Register			0x 0000	WO	16
0x FFFD_802C	Camera-2 Status Register			0x 0004	RO	16
0x FFFD_8030 to 0x FFFD_805C	Reserved			—	—	—
0x FFFD_9000	**JPEG2 Resize Related Register**		**RSZ2**			
0x FFFD_9060	Global Resizer Control Register			0x 0000	WO	16
0x FFFD_9064	Capture Control State Register			0x 0000	RO	16
0x FFFD_9068	Capture Data Setting Register			0x 0000	R/W	16
0x FFFD_9070 to 0x FFFD_907C	Reserved Register			—	—	—
0x FFFD_90C0	Capture Resize Control Register			0x 0000	R/W	16
0x FFFD_90C8	Capture Resize Start X-Coordinate Register			0x 0000	R/W	16
0x FFFD_90CC	Capture Resize Start Y-Coordinate Register			0x 0000	R/W	16
0x FFFD_90D0	Capture Resize End X-Coordinate Register			0x 027F	R/W	16
0x FFFD_90D4	Capture Resize End Y-Coordinate Register			0x 01DF	R/W	16
0x FFFD_90D8	Capture Resize Scaling Rate Register			0x 8080	R/W	16
0x FFFD_90DC	Capture Resize Scaling Mode Register			0x 0000	R/W	16

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFD_A000	**JPEG2 Module Register**	**JCTL2**			
0x FFFD_A000	JPEG Control Register		0x 0000	R/W	16
0x FFFD_A004	JPEG Status Flag Register		0x 8080	R/W	16
0x FFFD_A008	JPEG Raw Status Flag Register		0x 8080	RO	16
0x FFFD_A00C	JPEG Interrupt Control Register		0x 0000	R/W	16
0x FFFD_A010	Reserved Register		—	—	—
0x FFFD_A014	JPEG Codec Start/Stop Control Register		0x 0000	WO	16
0x FFFD_A018 to 0x FFFD_A01C	Reserved Register		—	—	—
0x FFFD_A020	Huffman Table Auto Setting Register		0x 0000	R/W	16
0x FFFD_A040	**JPEG2 FIFO Setting Register**	**JFIFO2**			
0x FFFD_A040	JPEG FIFO Control Register		0x 0000	R/W	16
0x FFFD_A044	JPEG FIFO Status Register		0x 8001	RO	16
0x FFFD_A048	JPEG FIFO Size Register		0x 003F	R/W	16
0x FFFD_A04C	JPEG FIFO Read/Write Port Register		0x 0000_0000	R/W	32
0x FFFD_A050 to 0x FFFD_A058	Reserved Register		—	—	—
0x FFFD_A060	Encode Size Limit Register 0		0x 0000	R/W	16
0x FFFD_A064	Encode Size Limit Register 1		0x 0000	R/W	16
0x FFFD_A068	Encode Size Result Register 0		0x 0000	RO	16
0x FFFD_A06C	Encode Size Result Register 1		0x 0000	RO	16
0x FFFD_A070 to 0x FFFD_A078	Reserved Register		—	—	—
0x FFFD_A080	**JPEG2 Line Buffer Setting Register**	**JLB2**			
0x FFFD_A080	JPEG Line Buffer Status Flag Register		0x 0000	R/W	16
0x FFFD_A084	JPEG Line Buffer Raw Status Flag Register		0x 0000	RO	16
0x FFFD_A088	JPEG Line Buffer Current Status Flag Register		0x X009	RO	16
0x FFFD_A08C	JPEG Line Buffer Interrupt Control Register		0x 0000	R/W	16
0x FFFD_A090 to 0x FFFD_A09C	Reserved Register		—	—	—
0x FFFD_A0A0	JPEG Line Buffer Horizontal Pixel Allowable Size Register		0x 2800	R/W	16
0x FFFD_A0A4	JPEG Line Buffer Memory Address Offset Register		0x 0020	R/W	16
0x FFFD_A0A8 to 0x FFFD_A0BC	Reserved Register		—	—	—
0x FFFD_A0C0	JPEG Line Buffer Read/Write Port Register		0x 0000	R/W	16
0x FFFD_B000	**JPEG2 Codec Register**	**JCOCEC2**			
0x FFFD_B000	Operation Mode Setting Register		0x 0000	R/W	16
0x FFFD_B004	Command Setting Register		Not applicable	WO	16
0x FFFD_B008	JPEG Operation Status Register		0x 0000	RO	16
0x FFFD_B00C	Quantization Table Number Register		0x 0000	R/W	16
0x FFFD_B010	Huffman Table Number Register		0x 0000	R/W	16
0x FFFD_B014	DRI Setting Register 0		0x 0000	R/W	16
0x FFFD_B018	DRI Setting Register 1		0x 0000	R/W	16
0x FFFD_B01C	Vertical Pixel Size Register 0		0x 0000	R/W	16
0x FFFD_B020	Vertical Pixel Size Register 1		0x 0000	R/W	16
0x FFFD_B024	Horizontal Pixel Size Register 0		0x 0000	R/W	16
0x FFFD_B028	Horizontal Pixel Size Register 1		0x 0000	R/W	16
0x FFFD_B02C to 0x FFFD_B034	Reserved Register		—	—	—
0x FFFD_B038	RST Marker Operation Setting Register		0x 0000	R/W	16

35. APPENDIX 1 S2S65A30 INTERNAL REGISTER LIST

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFD_B03C	RST Marker Operation Status Register		0x 0000	RO	16
0x FFFD_B040 to 0x FFFD_B0CC	Insertion Marker Data Register		0x 00FF	R/W	16
0x FFFD_B400 to 0x FFFD_B4FC	Quantization Table No. 0 Register		Not applicable	R/W	16
0x FFFD_B500 to 0x FFFD_B5FC	Quantization Table No.1 Register		Not applicable	R/W	16
0x FFFD_B800 to 0x FFFD_B83C	DC Huffman Table No. 0 Register 0		Not applicable	WO	16
0x FFFD_B840 to 0x FFFD_B86C	DC Huffman Table No. 0 Register 1		Not applicable	WO	16
0x FFFD_B880 to 0x FFFD_B8BC	AC Huffman Table No.0 Register 0		Not applicable	WO	16
0x FFFD_B8C0 to 0x FFFD_BB44	AC Huffman Table No.0 Register 1		Not applicable	WO	16
0x FFFD_BC00 to 0x FFFD_BC3C	DC Huffman Table No.1 Register 0		Not applicable	WO	16
0x FFFD_BC40 to 0x FFFD_BC6C	DC Huffman Table No.1 Register 1		Not applicable	WO	16
0x FFFD_BC80 to 0x FFFD_BCBC	AC Huffman Table No.1 Register 0		Not applicable	WO	16
0x FFFD_BCC0 to 0x FFFD_BF44	AC Huffman Table No.1 Register 1		Not applicable	WO	16
0x FFFD_C000	**ADC Related Register**	**ADC**			
0x FFFD_C000	ADC Data Register 0	ADCDT0	0x 0000	RO	16(/32)
0x FFFD_C004	ADC Data Register 1	ADCDT1	0x 0000	RO	16(/32)
0x FFFD_C008	ADC Data Register 2	ADCDT2	0x 0000	RO	16(/32)
0x FFFD_C00C	ADC Data Register 3	ADCDT3	0x 0000	RO	16(/32)
0x FFFD_C010	ADC Data Register 4	ADCDT4	0x 0000	RO	16(/32)
0x FFFD_C014	ADC Data Register 5	ADCDT5	0x 0000	RO	16(/32)
0x FFFD_C018	ADC Data Register 6	ADCDT6	0x 0000	RO	16(/32)
0x FFFD_C01C	ADC Data Register 7	ADCDT7	0x 0000	RO	16(/32)
0x FFFD_C020	ADC Control Register	ADCCTL	0x 00	RW	8(/16/32)
0x FFFD_C024	ADC Flag Register	ADCFLG	0x 0000	RW	16(/32)
0x FFFD_D000	**Reserved**				
0x FFFD_F000	**USB2.0 HS Device Control Related Register**	**USB**			
0x FFFD_F000	Main Interrupt Status	MainIntStat	0x 00	R/(W)	8(/16)
0x FFFD_F001	Reserved		—	—	
0x FFFD_F002	Reserved		—	—	8(/16)
0x FFFD_F003	CPU Interrupt Status	CPU_IntStat	0x 00	R/(W)	
0x FFFD_F004 to 0x FFFD_F005	Reserved		—	—	
0x FFFD_F006	Reserved		—	—	8(/16)
0x FFFD_F007	DMA Interrupt Status	DMA_IntStat	0x 00	R/(W)	
0x FFFD_F008 to 0x FFFD_F00F	Reserved		—	—	—
0x FFFD_F010	Main Interrupt Enable	MainIntEnb	0x 00	R/W	8(/16)
0x FFFD_F011	Reserved		—	—	
0x FFFD_F012	Reserved		—	—	8(/16)
0x FFFD_F013	CPU Interrupt Enable	CPU_IntEnb	0x 00	R/W	
0x FFFD_F014 to 0x FFFD_F015	Reserved		—	—	—

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFD_F016	Reserved		—	—	8(/16)
0x FFFD_F017	DMA Interrupt Enable	DMA_IntEnb	0x 00	R/W	
0x FFFD_F018 to 0x FFFD_F01F	Reserved		—	—	—
0x FFFD_F020	Power Management Control 0	PM_Control0	0x 00	R/W	8(/16)
0x FFFD_F021	Power Management Control 1	PM_Control1	0x 00	R	
0x FFFD_F022	Wakeup Time Low(BE)	WakeupTim_L	0x 00	R/W	8(/16)
0x FFFD_F023	Wakeup Time High(BE)	WakeupTim_H	0x 00	R/W	
0x FFFD_F024 to 0x FFFD_F02F	Reserved		—	—	—
0x FFFD_F030	Reserved		—	—	8(/16)
0x FFFD_F031	Macro Reset	MacroReset	0x XX	W	
0x FFFD_F032	Reserved		—	—	8(/16)
0x FFFD_F033	Mode Protection	ModeProtect	0x 56	R/W	
0x FFFD_F034	Reserved		—	—	8(/16)
0x FFFD_F035	Macro Configuration 0	MacroConfig0	0x 41	R/W	
0x FFFD_F036	Reserved		—	—	8(/16)
0x FFFD_F037	Macro Configuration 1	MacroConfig1	0x 06	R/W	
0x FFFD_F038	Reserved		—	—	—
0x FFFD_F039	Reserved		—	—	—
0x FFFD_F03A	Macro Type 0	MacroType0	0x 44	R	8(/16)
0x FFFD_F03B	Macro Type 1	MacroType1	0x 08	R	
0x FFFD_F03C	Macro Type 2	MacroType2	0x 02	R	8(/16)
0x FFFD_F03D	Macro Type 3	MacroType3	0x 30	R	
0x FFFD_F03E	FIFO Capacity Low(BE)	FIFO_CapacityL	0x 00	R	8(/16)
0x FFFD_F03F	FIFO Capacity High(BE)	FIFO_CapacityH	0x 12	R	
0x FFFD_F040	Reserved		—	—	8(/16)
0x FFFD_F041	DMA0 Configuration	DMA0_Config	0x 00	R/W	
0x FFFD_F042	DMA0 Control	DMA0_Control	0x 00	R/W	8(/16)-
0x FFFD_F043	Reserved		—	—	
0x FFFD_F044	DMA0 FIFO Remain Low(BE)	DMA0_RemainL	0x 00	R	8(/16)
0x FFFD_F045	DMA0 FIFO Remain High(BE)	DMA0_RemainH	0x 00	R	
0x FFFD_F046 to 0x FFFD_F047	Reserved		—	—	—
0x FFFD_F048	DMA0 Transfer Byte Counter High/Low(BE)	DMA0_Count_HL	0x 00	R/W	8(/16)
0x FFFD_F049	DMA0 Transfer Byte Counter High/High(BE)	DMA0_Count_HH	0x 00	R/W	
0x FFFD_F04A	DMA0 Transfer Byte Counter Low/Low(BE)	DMA0_Count_LL	0x 00	R/W	8(/16)
0x FFFD_F04B	DMA0 Transfer Byte Counter Low/High(BE)	DMA0_Count_LH	0x 00	R/W	
0x FFFD_F04C to 0x FFFD_F04F	Reserved		—	—	—
0x FFFD_F050	Reserved		—	—	8(/16)
0x FFFD_F051	DMA1 Configuration	DMA1_Config	0x 00	R/W	
0x FFFD_F052	DMA1 Control	DMA1_Control	0x 00	R/W	8(/16)
0x FFFD_F053	Reserved		—	—	
0x FFFD_F054	DMA1 FIFO Remain Low(BE)	DMA1_RemainL	0x 00	R	8(/16)
0x FFFD_F055	DMA1 FIFO Remain High(BE)	DMA1_RemainH	0x 00	R	
0x FFFD_F056 to 0x FFFD_F057	Reserved		—	—	—

35. APPENDIX 1 S2S65A30 INTERNAL REGISTER LIST

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFD_F058	DMA1 Transfer Byte Counter High/Low(BE)	DMA1_Count_HL	0x 00	R/W	8(/16)
0x FFFD_F059	DMA1 Transfer Byte Counter High/High(BE)	DMA1_Count_HH	0x 00	R/W	
0x FFFD_F05A	DMA1 Transfer Byte Counter Low/Low(BE)	DMA1_Count_LL	0x 00	R/W	8(/16)
0x FFFD_F05B	DMA1 Transfer Byte Counter Low/High(BE)	DMA1_Count_LH	0x 00	R/W	
0x FFFD_F05C to 0x FFFD_F05F	Reserved		—	—	—
0x FFFD_F060 to 0x FFFD_F07F	Reserved		—	—	—
0x FFFD_F080	Device Interrupt Status	DeviceIntStat	0x 00	R/W	8(/16)
0x FFFD_F081	Epr Interrupt Status	EprIntStat	0x 00	R	
0x FFFD_F082	SIE Interrupt Status	SIE_IntStat	0x 00	R/(W)	8(/16)
0x FFFD_F083	Reserved		—	—	
0x FFFD_F084	FIFO Interrupt Status	FIFO_IntStat	0x 00	R/(W)	8(/16)
0x FFFD_F085	Bulk Interrupt Status	BulkIntStat	0x 00	R/(W)	
0x FFFD_F086	Reserved		—	—	8(/16)
0x FFFD_F087	EP0 Interrupt Status	EP0IntStat	0x 00	R/(W)	
0x FFFD_F088	Epa Interrupt Status	EpaIntStat	0x 00	R/(W)	8(/16)
0x FFFD_F089	Epb Interrupt Status	EpbIntStat	0x 00	R/(W)	
0x FFFD_F08A	Epc Interrupt Status	EpcIntStat	0x 00	R/(W)	8(/16)
0x FFFD_F08B	Epd Interrupt Status	EpdIntStat	0x 00	R/(W)	
0x FFFD_F08C	Epe Interrupt Status	EpeIntStat	0x 00	R/(W)	8(/16)
0x FFFD_F08D	Epf Interrupt Status	EpfIntStat	0x 00	R/(W)	
0x FFFD_F08E	Epg Interrupt Status	EpgIntStat	0x 00	R/(W)	8(1/6)
0x FFFD_F08F	Eph Interrupt Status	EphIntStat	0x 00	R/(W)	
0x FFFD_F090	Device Interrupt Enable	DeviceIntEnb	0x 00	R/W	8(/16)
0x FFFD_F091	Epr Interrupt Enable	EprIntEnb	0x 00	R/W	
0x FFFD_F092	SIE Interrupt Enable	SIE_IntEnb	0x 00	R/W	8(/16)
0x FFFD_F093	Reserved		—	—	
0x FFFD_F094	FIFO Interrupt Enable	FIFO_IntEnb	0x 00	R/W	8(/16)
0x FFFD_F095	Bulk Interrupt Enable	BulkIntEnb	0x 00	R/W	
0x FFFD_F096	Reserved		—	—	8(/16)
0x FFFD_F097	EP0 Interrupt Enable	EP0IntEnb	0x 00	R/W	
0x FFFD_F098	Epa Interrupt Enable	EpaIntEnb	0x 00	R/W	8(/16)
0x FFFD_F099	Epb Interrupt Enable	EpbIntEnb	0x 00	R/W	
0x FFFD_F09A	Epc Interrupt Enable	EpcIntEnb	0x 00	R/W	8(/16)
0x FFFD_F09B	Epd Interrupt Enable	EpdIntEnb	0x 00	R/W	
0x FFFD_F09C	Epe Interrupt Enable	EpeIntEnb	0x 00	R/W	8(/16)
0x FFFD_F09D	Epf Interrupt Enable	EpfIntEnb	0x 00	R/W	
0x FFFD_F09E	Epg Interrupt Enable	EpgIntEnb	0x 00	R/W	8(/16)
0x FFFD_F09F	Eph Interrupt Enable	EphIntEnb	0x 00	R/W	
0x FFFD_F0A0	Reset DTM	ResetDTM	0x 01	R/W	8(/16)
0x FFFD_F0A1	Reserved		—	—	
0x FFFD_F0A2	Nego Control	NegoControl	0x 00	R/W	8(/16)
0x FFFD_F0A3	Reserved		—	—	
0x FFFD_F0A4	USB Status	USB_Status	0x XX	R/W	8(/16)
0x FFFD_F0A5	Xcvr Control	XcvrControl	0x 41	R/W	
0x FFFD_F0A6	USB Test	USB_Test	0x 00	R/W	8(/16)
0x FFFD_F0A7	Reserved		—	—	
0x FFFD_F0A8	Endpoint Control	EpnControl	0x XX	W	8(/16)

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFD_F0A9	Endpoint Clear	EPrFIFO_Clr	0x XX	W	
0x FFFD_F0AA	Clear All Epn Join	ClrAllEPnJoin	0x XX	W	8(/16)
0x FFFD_F0AB	Reserved		—	—	
0x FFFD_F0AC	BulkOnly Control	BulkOnlyControl	0x 00	R/W	8(/16)
0x FFFD_F0AD	BulkOnly Configuration	BulkOnlyConfig	0x 00	R/W	
0x FFFD_F0AE	Reserved		—	—	—
0x FFFD_F0AF	Reserved		—	—	—
0x FFFD_F0B0	EP0 SETUP 0	EP0SETUP_0	0x 00	R	8(/16)
0x FFFD_F0B1	EP0 SETUP 1	EP0SETUP_1	0x 00	R	
0x FFFD_F0B2	EP0 SETUP 2	EP0SETUP_2	0x 00	R	8(/16)
0x FFFD_F0B3	EP0 SETUP 3	EP0SETUP_3	0x 00	R	
0x FFFD_F0B4	EP0 SETUP 4	EP0SETUP_4	0x 00	R	8(/16)
0x FFFD_F0B5	EP0 SETUP 5	EP0SETUP_5	0x 00	R	
0x FFFD_F0B6	EP0 SETUP 6	EP0SETUP_6	0x 00	R	8(/16)
0x FFFD_F0B7	EP0 SETUP 7	EP0SETUP_7	0x 00	R	
0x FFFD_F0B8	USB Address	USB_Address	0x 00	R/(W)	8(/16)
0x FFFD_F0B9	Reserved		—	—	
0x FFFD_F0BA	SETUP Control	SETUP_Control	0x 00	R/W	8(/16)
0x FFFD_F0BB	Reserved		—	—	
0x FFFD_F0BC to 0x FFFD_F0BD	Reserved		—	—	—
0x FFFD_F0BE	FrameNumber Low	FrameNumber_L	0x 00	R	8(/16)
0x FFFD_F0BF	FrameNumber High	FrameNumber_H	0x 80	R	
0x FFFD_F0C0	EP0 Max Packet Size	EP0MaxSize	0x 40	R/W	8(/16)
0x FFFD_F0C1	EP0 Control	EP0Control	0x 00	R/W	
0x FFFD_F0C2	EP0 Control IN	EP0ControlIN	0x 00	R/W	8(/16)
0x FFFD_F0C3	EP0 Control OUT	EP0ControlOUT	0x 00	R/W	
0x FFFD_F0C4	Reserved		—	—	8(/16)
0x FFFD_F0C5	EP0 Join	EP0Join	0x 00	—	
0x FFFD_F0C6 to 0x FFFD_F0CF	Reserved		—	—	—
0x FFFD_F0D0	Epa Max Packet Size Low	EpaMaxSize_L	0x 00	R/W	8(/16)
0x FFFD_F0D1	Epa Max Packet Size High	EpaMaxSize_H	0x 00	R/W	
0x FFFD_F0D2	Epa Configuration	EpaConfig	0x 00	R/W	8(/16)
0x FFFD_F0D3	Reserved		—	—	
0x FFFD_F0D4	Epa Control	EpaControl	0x 00	R/W	8(/16)
0x FFFD_F0D5	Epa Join	EpaJoin	0x 00	R/W	
0x FFFD_F0D6	Reserved		—	—	—
0x FFFD_F0D7	Reserved		—	—	—
0x FFFD_F0D8	Epb Max Packet Size Low	EpbMaxSize_L	0x 00	R/W	8(/16)
0x FFFD_F0D9	Epb Max Packet Size High	EpbMaxSize_H	0x 00	R/W	
0x FFFD_F0DA	Epb Configuration	EpbConfig	0x 00	R/W	8(/16)
0x FFFD_F0DB	Reserved		—	—	
0x FFFD_F0DC	Epb Control	EpbControl	0x 00	R/W	8(/16)
0x FFFD_F0DD	Epb Join	EpbJoin	0x 00	R/W	
0x FFFD_F0DE	Reserved		—	—	—
0x FFFD_F0DF	Reserved		—	—	—
0x FFFD_F0E0	Epc Max Packet Size Low	EpcMaxSize_L	0x 00	R/W	8(/16)
0x FFFD_F0E1	Epc Max Packet Size High	EpcMaxSize_H	0x 00	R/W	
0x FFFD_F0E2	Epc Configuration	EpcConfig	0x 00	R/W	8(/16)
0x FFFD_F0E3	Reserved		—	—	
0x FFFD_F0E4	Epc Control	EpcControl	0x 00	R/W	8(/16)

35. APPENDIX 1 S2S65A30 INTERNAL REGISTER LIST

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFD_F0E5	Epc Join	EpcJoin	0x 00	R/W	
0x FFFD_F0E6	Reserved		—	—	—
0x FFFD_F0E7	Reserved		—	—	—
0x FFFD_F0E8	Epd Max Packet Size Low	EpdMaxSize_L	0x 00	R/W	8(/16)
0x FFFD_F0E9	Epd Max Packet Size High	EpdMaxSize_H	0x 00	R/W	
0x FFFD_F0EA	Epd Configuration	EpdConfig	0x 00	R/W	8(/16)
0x FFFD_F0EB	Reserved		—	—	
0x FFFD_F0EC	Epd Control	EpdControl	0x 00	R/W	8(/16)
0x FFFD_F0ED	Epd Join	EpdJoin	0x 00	R/W	
0x FFFD_F0EE	Reserved		—	—	—
0x FFFD_F0EF	Reserved		—	—	—
0x FFFD_F0F0	Epe Max Packet Size Low	EpeMaxSize_L	0x 00	R/W	8(/16)
0x FFFD_F0F1	Epe Max Packet Size High	EpeMaxSize_H	0x 00	R/W	
0x FFFD_F0F2	Epe Configuration	EpeConfig	0x 00	R/W	8(/16)
0x FFFD_F0F3	Reserved		—	—	
0x FFFD_F0F4	Epe Control	EpeControl	0x 00	R/W	8(/16)
0x FFFD_F0F5	Epe Join	EpeJoin	0x 00	R/W	
0x FFFD_F0F6	Reserved		—	—	—
0x FFFD_F0F7	Reserved		—	—	—
0x FFFD_F0F8	Epf Max Packet Size Low	EpfMaxSize_L	0x 00	R/W	8(/16)
0x FFFD_F0F9	Epf Max Packet Size High	EpfMaxSize_H	0x 00	R/W	
0x FFFD_F0FA	Epf Configuration	EpfConfig	0x 00	R/W	8(/16)
0x FFFD_F0FB	Reserved		—	—	
0x FFFD_F0FC	Epf Control	EpfControl	0x 00	R/W	8(/16)
0x FFFD_F0FD	Epf Join	EpfJoin	0x 00	R/W	
0x FFFD_F0FE	Reserved		—	—	—
0x FFFD_F0FF	Reserved		—	—	—
0x FFFD_F100	Epg Max Packet Size Low	EpgMaxSize_L	0x 00	R/W	8(/16)
0x FFFD_F101	Epg Max Packet Size High	EpgMaxSize_H	0x 00	R/W	
0x FFFD_F102	Epg Configuration	EpgConfig	0x 00	R/W	8(/16)
0x FFFD_F103	Reserved		—	—	
0x FFFD_F104	Epg Control	EpgControl	0x 00	R/W	8(/16)
0x FFFD_F105	Epg Join	EpgJoin	0x 00	R/W	
0x FFFD_F106	Reserved		—	—	—
0x FFFD_F107	Reserved		—	—	—
0x FFFD_F108	Eph Max Packet Size Low	EphMaxSize_L	0x 00	R/W	8(/16)
0x FFFD_F109	Eph Max Packet Size High	EphMaxSize_H	0x 00	R/W	
0x FFFD_F10A	Eph Configuration	EphConfig	0x 00	R/W	8(/16)
0x FFFD_F10B	Reserved		—	—	
0x FFFD_F10C	Eph Control	EphControl	0x 00	R/W	8(/16)
0x FFFD_F10D	Eph Join	EphJoin	0x 00	R/W	
0x FFFD_F10E	Reserved		—	—	—
0x FFFD_F10F	Reserved		—	—	—
0x FFFD_F110	Endpoint a Start Address Low	EpaStartAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F111	Endpoint a Start Address High	EpaStartAdrs_H	0x 00	R/W	
0x FFFD_F112	Endpoint b Start Address Low	EpbStartAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F113	Endpoint b Start Address High	EpbStartAdrs_H	0x 00	R/W	
0x FFFD_F114	Endpoint c Start Address Low	EpcStartAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F115	Endpoint c Start Address High	EpcStartAdrs_H	0x 00	R/W	
0x FFFD_F116	Endpoint d Start Address Low	EpdStartAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F117	Endpoint d Start Address High	EpdStartAdrs_H	0x 00	R/W	
0x FFFD_F118	Endpoint e Start Address Low	EpeStartAdrs_L	0x 00	R/W	8(/16)

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFD_F119	Endpoint e Start Address High	EpeStartAdrs_H	0x 00	R/W	
0x FFFD_F11A	Endpoint f Start Address Low	EpfStartAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F11B	Endpoint f Start Address High	EpfStartAdrs_H	0x 00	R/W	
0x FFFD_F11C	Endpoint g Start Address Low	EpgStartAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F11D	Endpoint g Start Address High	EpgStartAdrs_H	0x 00	R/W	
0x FFFD_F11E	Endpoint h Start Address Low	EphStartAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F11F	Endpoint h Start Address High	EphStartAdrs_H	0x 00	R/W	
0x FFFD_F120	Endpoint n End Address Low	EP_EndAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F121	Endpoint n End Address High	EP_EndAdrs_H	0x 12	R/W	
0x FFFD_F122	Reserved		—	—	—
0x FFFD_F123	Reserved		—	—	—
0x FFFD_F124	Descriptor Address Low	DescAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F125	Descriptor Address High	DescAdrs_H	0x 00	R/W	
0x FFFD_F126	Descriptor Size High	DescSize_L	0x 00	R/W	8(/16)
0x FFFD_F127	Descriptor Size Low	DescSize_H	0x 00	R/W	
0x FFFD_F128	DMA0 FIFO Control	DMA0_FIFO_ Control	0x 00	R/W	8(/16)
0x FFFD_F129	Reserved		—	—	
0x FFFD_F12A	DMA1 FIFO Control	DMA1_FIFO_ Control	0x 00	R/W	8(/16)
0x FFFD_F12B	Reserved		—	—	
0x FFFD_F12C to 0x FFFD_F12F	Reserved		—	—	—
0x FFFD_F130	FIFO Read 0	FIFO_Rd_0	0x XX	R	8(/16)
0x FFFD_F131	FIFO Read 1	FIFO_Rd_1	0x XX	R	
0x FFFD_F132	FIFO Write 0	FIFO_Wr_0	0x XX	W	8(/16)
0x FFFD_F133	FIFO Write 1	FIFO_Wr_1	0x XX	W	
0x FFFD_F134	FIFO Read Remain Low	FIFO_RdRemain _L	0x 00	R	8(/16)
0x FFFD_F135	FIFO Read Remain High	FIFO_RdRemain _H	0x 00	R	
0x FFFD_F136	FIFO Write Remain Low	FIFO_WrRemain _L	0x 00	R	8(/16)
0x FFFD_F137	FIFO Write Remain High	FIFO_WrRemain _H	0x 00	R	
0x FFFD_F138	FIFO Byte Read	FIFO_ByteRd	0x XX	R	8
0x FFFD_F139 to 0x FFFD_F13F	Reserved		—	—	—
0x FFFD_F140	RAM Read Address Low	RAM_RdAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F141	RAM Read Address High	RAM_RdAdrs_H	0x 00	R/W	
0x FFFD_F142	RAM Read Control	RAM_RdControl	0x 00	R/W	8(/16)
0x FFFD_F143	RAM Read Counter	RAM_RdCount	0x 00	R/W	
0x FFFD_F144	RAM Write Address Low	RAM_WrAdrs_L	0x 00	R/W	8(/16)
0x FFFD_F145	RAM Write Address High	RAM_WrAdrs_H	0x 00	R/W	
0x FFFD_F146	RAM Write Door 0	RAM_WrDoor_0	0x XX	W	8(/16)
0x FFFD_F147	RAM Write Door 1	RAM_WrDoor_1	0x XX	W	
0x FFFD_F148 to 0x FFFD_F14F	Reserved		—	—	—
0x FFFD_F150	RAM Read 00	RAM_Rd_00	0x XX	R	8(/16)
0x FFFD_F151	RAM Read 01	RAM_Rd_01	0x XX	R	
0x FFFD_F152	RAM Read 02	RAM_Rd_02	0x XX	R	8(/16)
0x FFFD_F153	RAM Read 03	RAM_Rd_03	0x XX	R	

35. APPENDIX 1 S2S65A30 INTERNAL REGISTER LIST

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFD_F154	RAM Read 04	RAM_Rd_04	0x XX	R	8(/16)
0x FFFD_F155	RAM Read 05	RAM_Rd_05	0x XX	R	
0x FFFD_F156	RAM Read 06	RAM_Rd_06	0x XX	R	8(/16)
0x FFFD_F157	RAM Read 07	RAM_Rd_07	0x XX	R	
0x FFFD_F158	RAM Read 08	RAM_Rd_08	0x XX	R	8(/16)
0x FFFD_F159	RAM Read 09	RAM_Rd_09	0x XX	R	
0x FFFD_F15A	RAM Read 0A	RAM_Rd_0A	0x XX	R	8(/16)
0x FFFD_F15B	RAM Read 0B	RAM_Rd_0B	0x XX	R	
0x FFFD_F15C	RAM Read 0C	RAM_Rd_0C	0x XX	R	8(/16)
0x FFFD_F15D	RAM Read 0D	RAM_Rd_0D	0x XX	R	
0x FFFD_F15E	RAM Read 0E	RAM_Rd_0E	0x XX	R	8(/16)
0x FFFD_F15F	RAM Read 0F	RAM_Rd_0F	0x XX	R	
0x FFFD_F160	RAM Read 10	RAM_Rd_10	0x XX	R	8(/16)
0x FFFD_F161	RAM Read 11	RAM_Rd_11	0x XX	R	
0x FFFD_F162	RAM Read 12	RAM_Rd_12	0x XX	R	8(/16)
0x FFFD_F163	RAM Read 13	RAM_Rd_13	0x XX	R	
0x FFFD_F164	RAM Read 14	RAM_Rd_14	0x XX	R	8(/16)
0x FFFD_F165	RAM Read 15	RAM_Rd_15	0x XX	R	
0x FFFD_F166	RAM Read 16	RAM_Rd_16	0x XX	R	8(/16)
0x FFFD_F167	RAM Read 17	RAM_Rd_17	0x XX	R	
0x FFFD_F168	RAM Read 18	RAM_Rd_18	0x XX	R	8(/16)
0x FFFD_F169	RAM Read 19	RAM_Rd_19	0x XX	R	
0x FFFD_F16A	RAM Read 1A	RAM_Rd_1A	0x XX	R	8(/16)
0x FFFD_F16B	RAM Read 1B	RAM_Rd_1B	0x XX	R	
0x FFFD_F16C	RAM Read 1C	RAM_Rd_1C	0x XX	R	8(/16)
0x FFFD_F16D	RAM Read 1D	RAM_Rd_1D	0x XX	R	
0x FFFD_F16E	RAM Read 1E	RAM_Rd_1E	0x XX	R	8(/16)
0x FFFD_F16F	RAM Read 1F	RAM_Rd_1F	0x XX	R	
0x FFFD_F170 to 0x FFFD_F2FF	Reserved		—	—	—
0x FFFE_0000	**APB Bridge Related Register**	**APB**			
0x FFFE_0000	APB WAIT0 Register	APBWAIT0	0x 0050_0500	R/W	32
0x FFFE_0004	APB WAIT1 Register	APBWAIT1	0x 0000_0000	R/W	32
0x FFFE_0008	APB WAIT2 Register	APBWAIT2	0x 0050_0000	R/W	32
0x FFFE_1000	**IPC&INTIM1**	**IPC1**			
0xFFFE_1000	IPC Camera Input Mode Setup	INMODE	0x0000	R/W	16/8
0xFFFE_1010	IPC Camera Input Setting	INCONFIG	0x0001	R/W	16/8
0xFFFE_1108	IPC X-Direction Start Position Setting	XSTART	0x0001	R/W	16/8
0xFFFE_110C	IPC Y-Direction Start Position Setting/ ODD Field Start Position Setting	YSTART/ YSTART_O	0x0001	R/W	16/8
0xFFFE_1110	IPC EVEN Field Y-Direction Start Position Setting	YSTART_E	0x0001	R/W	16/8
0xFFFE_1140	IPC Interrupt Setting	INTSEL	0x0000	R/W	16/8
0xFFFE_1200	IPC Scaler Setting	CONTROL	0x0001	R/W	16/8
0xFFFE_1400	IPC Conversion Buffer SDRAM Start Address 1	IPCBUF_SADR_L	0x0000	R/W	16/8
0xFFFE_1404	IPC Conversion Buffer SDRAM Start Address 2	IPCBUF_SADR_H	0x0000	R/W	16/8
0xFFFE_1510	IPC Video Output X-Direction Effective Pixels	VOUT_HD	0x0280	R/W	16
0xFFFE_1520	IPC Video Output X-Direction Length Setting	VOUT_HT	0x02DA	R/W	16
0xFFFE_1534	IPC Video Output Vertical Blank Line Number	VOUT_VP	0x0001	R/W	16
0xFFFE_1540	IPC Video Output Y-Direction Effective Pixels	VOUT_VD	0x01E0	R/W	16
0xFFFE_1700	IPC Interlaced_to_Progressive Conversion Mode	IPC_MODE	0x0080	R/W	16/8

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0xFFFE_1800	IPC Sync Signal Output Polarity Setting	OUTCONFIG	0x0003	R/W	16/8
0xFFFE_1804	IPC Image Correction Circuit Bypass Setting	BYPASS	0x0000	R/W	16/8
0xFFFE_1808	IPC Image Correction Setting Update Register	UPDATE	0x0000	R/W	16/8
0xFFFE_180C_ 19FC	Correction Value Setting Register Area				
0x FFFE_3000	**DMA Controller 1 Related Register**	**DMAC1**			
0x FFFE_3000	DMA Channel-0 Source Address Register	SAR0	0x XXXX_XXXX	R/W	32
0x FFFE_3004	DMA Channel-0 Destination Address Register	DAR0	0x XXXX_XXXX	R/W	32
0x FFFE_3008	DMA Channel-0 Transfer Count Register	TCR0	0x 00XX_XXXX	R/W	32
0x FFFE_300C	DMA Channel-0 Control Register	CTL0	0x 00XX_XXXX	R/W	32
0x FFFE_3010	DMA Channel-1 Source Address Register	SAR1	0x XXXX_XXXX	R/W	32
0x FFFE_3014	DMA Channel-1 Destination Address Register	DAR1	0x XXXX_XXXX	R/W	32
0x FFFE_3018	DMA Channel-1 Transfer Count Register	TCR1	0x 00XX_XXXX	R/W	32
0x FFFE_301C	DMA Channel-1 Control Register	CTL1	0x 00XX_XXXX	R/W	32
0x FFFE_3020	DMA Channel-2 Source Address Register	SAR2	0x XXXX_XXXX	R/W	32
0x FFFE_3024	DMA Channel-2 Destination Address Register	DAR2	0x XXXX_XXXX	R/W	32
0x FFFE_3028	DMA Channel-2 Transfer Count Register	TCR2	0x 00XX_XXXX	R/W	32
0x FFFE_302C	DMA Channel-2 Control Register	CTL2	0x 00XX_XXXX	R/W	32
0x FFFE_3030	DMA Channel-3 Source Address Register	SAR3	0x XXXX_XXXX	R/W	32
0x FFFE_3034	DMA Channel-3 Destination Address Register	DAR3	0x XXXX_XXXX	R/W	32
0x FFFE_3038	DMA Channel-3 Transfer Count Register	TCR3	0x 00XX_XXXX	R/W	32
0x FFFE_303C	DMA Channel-3 Control Register	CTL3	0x 00XX_XXXX	R/W	32
0x FFFE_3060	DMA Channel Operating Select Register	OPSR	0x 0000_0000	R/W	32
0x FFFE_6000	**CF Interface Control Related Register**	**CF**			
0x FFFE_6000	CF Card Interface Control Register	CFCTL	0x 1000	(R/W)	16(/32)
0x FFFE_6004	CF Card Pin Status Register	CFPINSTS	0x 0XXX	RO	16(/32)
0x FFFE_6008	CF Card IRQ Source & Clear Register	CFINTRSTS	0x 0XXX	R/W	16(/32)
0x FFFE_600C	CF Card IRQ Enable Register	CFINTMSTS	0x 0000	R/W	16(/32)
0x FFFE_6010	CF Card IRQ Status Register	CFINTSTS	0x 0000	RO	16(/32)
0x FFFE_6014	CF Card MISC Register	CFMISC	0x 0000	R/W	16(/32)
0x FFFE_7000	**ARS Control Register**	**ARS**			
0x FFFE_7000	ARS Control Register	ARSCTRL	0x0000_0080	R/W	32
0x FFFE_7004	ARS Area Select Register	ARSASEL	0x0000_0000	R/W	32
0x FFFE_700C	ARS Status Register	ARSSTAT	0x0000_0000	R/W	32
0x FFFE_7010	ARS Interrupt Cause Register	ARSINT	0x0000_0000	R/W	32
0x FFFE_7040	ARS Accumulation Register 0	ARSADD0	0x0000_0000	RO	32
0x FFFE_7044	ARS Accumulation Register 1	ARSADD1	0x0000_0000	RO	32
0x FFFE_7048	ARS Accumulation Register 2	ARSADD2	0x0000_0000	RO	32
0x FFFE_704C	ARS Accumulation Register 3	ARSADD3	0x0000_0000	RO	32
0x FFFE_7050	ARS Accumulation Register 4	ARSADD4	0x0000_0000	RO	32
0x FFFE_7054	ARS Accumulation Register 5	ARSADD5	0x0000_0000	RO	32
0x FFFE_7058	ARS Accumulation Register 6	ARSADD6	0x0000_0000	RO	32
0x FFFE_705C	ARS Accumulation Register 7	ARSADD7	0x0000_0000	RO	32
0x FFFE_7060	ARS Accumulation Register 8	ARSADD8	0x0000_0000	RO	32

35. APPENDIX 1 S2S65A30 INTERNAL REGISTER LIST

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFE_7064	ARS Accumulation Register 9	ARSADD9	0x0000_0000	RO	32
0x FFFE_7068	ARS Accumulation Register 10	ARSADD10	0x0000_0000	RO	32
0x FFFE_706C	ARS Accumulation Register 11	ARSADD11	0x0000_0000	RO	32
0x FFFE_7070	ARS Accumulation Register 12	ARSADD12	0x0000_0000	RO	32
0x FFFE_7074	ARS Accumulation Register 13	ARSADD13	0x0000_0000	RO	32
0x FFFE_7078	ARS Accumulation Register 14	ARSADD14	0x0000_0000	RO	32
0x FFFE_707C	ARS Accumulation Register 15	ARSADD15	0x0000_0000	RO	32
0x FFFE_8000	**Camera-1 Interface Related Register**	**CAM1**			
0x FFFE_8000	Camera-1 Clock Cycle Setting Register		0x 0000	R/W	16
0x FFFE_8004	Camera-1 Signal Setting Register		0x 0000	R/W	16
0x FFFE_8008 to 0x FFFE_801C	Reserved		—	—	—
0x FFFE_8020	Camera-1 Mode Setting Register		0x 0000	R/W	16
0x FFFE_8024	Camera-1 Frame Control Register		0x 0000	R/W	16
0x FFFE_8028	Camera-1 Control Register		0x 0000	WO	16
0x FFFE_802C	Camera-1 Status Register		0x 0004	RO	16
0x FFFE_8030 to 0x FFFE_805C	Reserved		—	—	—
0x FFFE_9000	**JPEG1 Resize Related Register**	**RSZ1**			
0x FFFE_9060	Global Resizer Control Register		0x 0000	WO	16
0x FFFE_9064	Capture Control State Register		0x 0000	RO	16
0x FFFE_9068	Capture Data Setting Register		0x 0000	R/W	16
0x FFFE_9070 to 0x FFFE_907C	Reserved Register		—	—	—
0x FFFE_90C0	Capture Resize Control Register		0x 0000	R/W	16
0x FFFE_90C8	Capture Resize Start X-Coordinate Register		0x 0000	R/W	16
0x FFFE_90CC	Capture Resize Start Y-Coordinate Register		0x 0000	R/W	16
0x FFFE_90D0	Capture Resize End X-Coordinate Register		0x 027F	R/W	16
0x FFFE_90D4	Capture Resize End Y-Coordinate Register		0x 01DF	R/W	16
0x FFFE_90D8	Capture Resize Scaling Rate Register		0x 8080	R/W	16
0x FFFE_90DC	Capture Resize Scaling Mode Register		0x 0000	R/W	16
0x FFFE_A000	**JPEG1 Module Register**	**JCTL1**			
0x FFFE_A000	JPEG Control Register		0x 0000	R/W	16
0x FFFE_A004	JPEG Status Flag Register		0x 8080	R/W	16
0x FFFE_A008	JPEG Raw Status Flag Register		0x 8080	RO	16
0x FFFE_A00C	JPEG Interrupt Control Register		0x 0000	R/W	16
0x FFFE_A010	Reserved Register		—	—	—
0x FFFE_A014	JPEG Codec Start/Stop Control Register		0x 0000	WO	16
0x FFFE_A018 to 0x FFFE_A01C	Reserved Register		—	—	—
0x FFFE_A020	Huffman Table Auto Setting Register		0x 0000	R/W	16
0x FFFE_A040	**JPEG1 FIFO Setting Register**	**JFIFO1**			
0x FFFE_A040	JPEG FIFO Control Register		0x 0000	R/W	16
0x FFFE_A044	JPEG FIFO Status Register		0x 8001	RO	16
0x FFFE_A048	JPEG FIFO Size Register		0x 003F	R/W	16
0x FFFE_A04C	JPEG FIFO Read/Write Port Register		0x 0000_0000	R/W	32
0x FFFE_A050 to 0x FFFE_A058	Reserved Register		—	—	—
0x FFFE_A060	Encode Size Limit Register 0		0x 0000	R/W	16
0x FFFE_A064	Encode Size Limit Register 1		0x 0000	R/W	16
0x FFFE_A068	Encode Size Result Register 0		0x 0000	RO	16
0x FFFE_A06C	Encode Size Result Register 1		0x 0000	RO	16

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFE_A070 to 0x FFFE_A078	Reserved Register		—	—	—
0x FFFE_A080	**JPEG1 Line Buffer Setting Register**	**JLB1**			
0x FFFE_A080	JPEG Line Buffer Status Flag Register		0x 0000	R/W	16
0x FFFE_A084	JPEG Line Buffer Raw Status Flag Register		0x 0000	RO	16
0x FFFE_A088	JPEG Line Buffer Current Status Flag Register		0x X009	RO	16
0x FFFE_A08C	JPEG Line Buffer Interrupt Control Register		0x 0000	R/W	16
0x FFFE_A090 to 0x FFFE_A09C	Reserved Register		—	—	—
0x FFFE_A0A0	JPEG Line Buffer Horizontal Pixel Allowable Size Register		0x 2800	R/W	16
0x FFFE_A0A4	JPEG Line Buffer Memory Address Offset Register		0x 0020	R/W	16
0x FFFE_A0A8 to 0x FFFE_A0BC	Reserved Register		—	—	—
0x FFFE_A0C0	JPEG Line Buffer Read/Write Port Register		0x 0000	R/W	16
0x FFFE_B000	**JPEG1 Codec Register**	**JCOCEC1**			
0x FFFE_B000	Operation Mode Setting Register		0x 0000	R/W	16
0x FFFE_B004	Command Setting Register		Not applicable	WO	16
0x FFFE_B008	JPEG Operation Status Register		0x 0000	RO	16
0x FFFE_B00C	Quantization Table Number Register		0x 0000	R/W	16
0x FFFE_B010	Huffman Table Number Register		0x 0000	R/W	16
0x FFFE_B014	DRI Setting Register 0		0x 0000	R/W	16
0x FFFE_B018	DRI Setting Register 1		0x 0000	R/W	16
0x FFFE_B01C	Vertical Pixel Size Register 0		0x 0000	R/W	16
0x FFFE_B020	Vertical Pixel Size Register 1		0x 0000	R/W	16
0x FFFE_B024	Horizontal Pixel Size Register 0		0x 0000	R/W	16
0x FFFE_B028	Horizontal Pixel Size Register 1		0x 0000	R/W	16
0x FFFE_B02C to 0x FFFE_B034	Reserved Register		—	—	—
0x FFFE_B038	RST Marker Operation Setting Register		0x 0000	R/W	16
0x FFFE_B03C	RST Marker Operation Status Register		0x 0000	RO	16
0x FFFE_B040 to 0x FFFE_B0CC	Insertion Marker Data Register		0x 00FF	R/W	16
0x FFFE_B400 to 0x FFFE_B4FC	Quantization Table No. 0 Register		Not applicable	R/W	16
0x FFFE_B500 to 0x FFFE_B5FC	Quantization Table No.1 Register		Not applicable	R/W	16
0x FFFE_B800 to 0x FFFE_B83C	DC Huffman Table No. 0 Register 0		Not applicable	WO	16
0x FFFE_B840 to 0x FFFE_B86C	DC Huffman Table No. 0 Register 1		Not applicable	WO	16
0x FFFE_B880 to 0x FFFE_B8BC	AC Huffman Table No.0 Register 0		Not applicable	WO	16
0x FFFE_B8C0 to 0x FFFE_BB44	AC Huffman Table No.0 Register 1		Not applicable	WO	16
0x FFFE_BC00 to 0x FFFE_BC3C	DC Huffman Table No.1 Register 0		Not applicable	WO	16
0x FFFE_BC40 to 0x FFFE_BC6C	DC Huffman Table No.1 Register 1		Not applicable	WO	16
0x FFFE_BC80 to 0x FFFE_BCBC	AC Huffman Table No.1 Register 0		Not applicable	WO	16

35. APPENDIX 1 S2S65A30 INTERNAL REGISTER LIST

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFE_BCC0 to 0x FFFE_BF44	AC Huffman Table No.1 Register 1		Not applicable	WO	16
0x FFFE_C000	**JPEG_DMAC Related Register**	**JDMA**			
0x FFFE_C000	DMA Channel 0 JPEG Source Address Register	JSAR0	0x XXXX_XXXX	R/W	32
0x FFFE_C004	DMA Channel 0 JPEG Destination Address Register	JDAR0	0x XXXX_XXXX	R/W	32
0x FFFE_C008	DMA Channel 0 JPEG Transfer Count Register	JTCR0	0x 0000_0000	R/W	32
0x FFFE_C00C	DMA Channel 0 JPEG Control Register	JCTL0	0x 0000_0000	R/W	32
0x FFFE_C010	DMA Channel 0 JPEG Block Count Register	JBCR0	0x 00XX_XXXX	R/W	32
0x FFFE_C014	DMA Channel 0 JPEG Destination Offset Address Register	JOFR0	0x 0000_0000	R/W	32
0x FFFE_C018	DMA Channel 0 JPEG Block End Count Register	JBER0	0x 00XX_XXXX	R/W	32
0x FFFE_C020	JPEG Source Address Register DMA Channel 1	JSAR1	0x XXXX_XXXX	R/W	32
0x FFFE_C024	DMA Channel 1 JPEG Destination Address Register	JDAR1	0x XXXX_XXXX	R/W	32
0x FFFE_C028	DMA Channel 1 JPEG Transfer Count Register	JTCR1	0x 0000_0000	R/W	32
0x FFFE_C02C	DMA Channel 1 JPEG Control Register	JCTL1	0x 0000_0000	R/W	32
0x FFFE_C030	DMA Channel 1 JPEG Block Count Register	JBCR1	0x 00XX_XXXX	R/W	32
0x FFFE_C034	DMA Channel 1 JPEG Destination Offset Address Register	JOFR1	0x 0000_0000	R/W	32
0x FFFE_C038	DMA Channel 1 JPEG Block End Count Register	JBER1	0x 00XX_XXXX	R/W	32
0x FFFE_C040	DMA Channel JPEG FIFO Data Select Mode Register	JFSM	0x 0000_0000	R/W	32
0x FFFE_C048	DMA Channel JPEG Expansion Register	JHID	0x 0000_0000	R/W	32
0x FFFE_D000	**I2C Related Register**	**I2C**			
0x FFFE_D000	I2C Send Data Register		0000 0000 b	R/W	8 (16/32)
0x FFFE_D004	I2C Receive Data Register		0000 0000 b	RO	8 (16/32)
0x FFFE_D008	I2C Control Register		0000 0000 b	R/W	8 (16/32)
0x FFFE_D00C	I2C Bus Status Register		00xx 0000 b	RO	8 (16/32)
0x FFFE_D010	I2C Error Status Register		0000 0000 b	RO	8 (16/32)
0x FFFE_D014	I2C Interrupt Control/Status Register		0000 0000 b	R/W	8 (16/32)
0x FFFE_D018	I2C-Bus Sample Clock Dividing Setting Register		0000 0000 b	R/W	8 (16/32)
0x FFFE_D01C	I2C SCL Clock Dividing Setting Register		0000 0000 b	R/W	8 (16/32)
0x FFFE_D020	I2C I/O Control Register		0000 0000 b	R/W	8 (16/32)
0x FFFE_D024	I2C DMA Mode Register		0000 0000 b	R/W	8 (16/32)
0x FFFE_D028	I2C DMA Counter Value (LSB) Register		0000 0000 b	R/W	8 (16/32)
0x FFFE_D02C	I2C DMA Counter Value (MSB) Register		0000 0000 b	R/W	8 (16/32)
0x FFFE_D030	I2C DMA Status Register		0000 1000 b	RO	8 (16/32)
0x FFFE_D034 to 0x FFFE_D038	Reserved		—	—	—
0x FFFE_E000	**I2S Related Register**	**I2S**			

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFE_E000	I2S0 Control Register		0x 0000	R/W	16(/32)
0x FFFE_E004	I2S0 Clock Dividing Register		0x 0000	R/W	16(/32)
0x FFFE_E008	I2S0 Transmission Port Register		—	R/W	8(/16/32)
0x FFFE_E010	I2S0 Interrupt Status Register		0x 0000	R/W	16(/32)
0x FFFE_E014	I2S0 Interrupt Raw Status Register		0x 0009	RO	16(/32)
0x FFFE_E018	I2S0 Interrupt Enable Register		0x 0000	R/W	16(/32)
0x FFFE_E01C	I2S0 Current Status Register		0x 0009	RO	16(/32)
0x FFFE_E040	I2S1 Control Register		0x 0000	R/W	16(/32)
0x FFFE_E044	I2S1 Clock Dividing Register		0x 0000	R/W	16(/32)
0x FFFE_E048	I2S1 Transmission Port Register		—	R/W	8(/16/32)
0x FFFE_E050	I2S1 Interrupt Status Register		0x 0000	R/W	16(/32)
0x FFFE_E054	I2S1 Interrupt Raw Status Register		0x 0009	RO	16(/32)
0x FFFE_E058	I2S1 Interrupt Enable Register		0x 0000	R/W	16(/32)
0x FFFE_E05C	I2S1 Current Status Register		0x 0009	RO	16(/32)
0x FFFF_1000	**GPIO Related Register**	**GPIO**			
0x FFFF_1000	GPIOA Data Register	GPIOA_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_1004	GPIOA Pin Function Register	GPIOA_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1008	GPIOB Data Register	GPIOB_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_100C	GPIOB Pin Function Register	GPIOB_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1010	GPIOC Data Register	GPIOC_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_1014	GPIOC Pin Function Register	GPIOC_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1018	GPIOD Data Register	GPIOD_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_101C	GPIOD Pin Function Register	GPIOD_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1020	GPIOE Data Register	GPIOE_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_1024	GPIOE Pin Function Register	GPIOE_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1028	GPIOF Data Register	GPIOF_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_102C	GPIOF Pin Function Register	GPIOF_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1030	GPIOG Data Register	GPIOG_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_1034	GPIOG Pin Function Register	GPIOG_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1038	GPIOH Data Register	GPIOH_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_103C	GPIOH Pin Function Register	GPIOH_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1040	GPIOI Data Register	GPIOI_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_1044	GPIOI Pin Function Register	GPIOI_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1048	GPIOJ Data Register	GPIOJ_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_104C	GPIOJ Pin Function Register	GPIOJ_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1050	GPIOK Data Register	GPIOK_DATA	0x 0000_0000	R/W	8 (/16/32)
0x FFFF_1054	GPIOK Pin Function Register	GPIOK_FNC	0x 0000_0000	R/W	16 (/32)
0x FFFF_1060	GPIOA&B IRQ Type Register	GPIOAB_ITYP	0x 0000_0000	R/W	16 (/32)
0x FFFF_1064	GPIOA&B IRQ Polarity Register	GPIOAB_IPOL	0x 0000_0000	R/W	16 (/32)
0x FFFF_1068	GPIOA&B IRQ Enable Register	GPIOAB_IEN	0x 0000_0000	R/W	16 (/32)
0x FFFF_106C	GPIOA&B IRQ Status & Clear Register	GPIOAB_ISTS	0x 0000_0000	R/W	16 (/32)
0x FFFF_2000	**SPI Related Register**	**SPI**			
0x FFFF_2000	SPI Receive Data Register		0x 0000_0000	RO	32
0x FFFF_2004	SPI Send Data Register		0x 0000_0000	R/W	32
0x FFFF_2008	SPI Control Register 1		0x 0000_0000	R/W	32
0x FFFF_200C	SPI Control Register 2		0x 0000_0000	R/W	32
0x FFFF_2010	SPI Wait Register		0x 0000_0000	R/W	32
0x FFFF_2014	SPI Status Register		0x 0000_0010	RO	32
0x FFFF_2018	SPI Interrupt Control Register		0x 0000_0000	R/W	32
0xFFFF_3000	**DMAC3**	**DMAC3**			
0xFFFF_3000	DMAC3 Transfer Source Address Register	SADR	0x0000_0000	R/W	32
0xFFFF_3004	DMAC3 Transfer Destination Address Register	DADR	0x0000_0000	R/W	32

35. APPENDIX 1 S2S65A30 INTERNAL REGISTER LIST

Address (Hex)	Register Name		Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0xFFFF_3008	DMAC3 Transfer Byte Count Register		TBYTE	0x0000_0000	R/W	32
0xFFFF_300C	DMAC3 Transfer Control Register		DCTRL	0x0000_0000	R/W	32
0xFFFF_3010	DMAC3 Operation Control Register		DOPSR	0x0000_0000	R/W	32
0x FFFF_5000	**DLAB**	**UART Related Register**	**UART**			
0x FFFF_5000	0	Receive Buffer Register	RBR	0x 00	RO	8 (/16/32)
0x FFFF_5000	0	Send Holding Register	THR	—	WO	8 (/16/32)
0x FFFF_5000	1	Divider Latch LSB Register	DLL	0x 00	R/W	8 (/16/32)
0x FFFF_5004	0	Interrupt Enable Register	IER	0x 00	R/W	8 (/16/32)
0x FFFF_5004	1	Divider Latch MSB Register	DLM	0x 00	R/W	8 (/16/32)
0x FFFF_5008	Interrupt Identification Register		IIR	0x 01	RO	8 (/16/32)
0x FFFF_5008	FIFO Control Register		FCR	—	WO	8 (/16/32)
0x FFFF_500C	Line Control Register		LCR	0x 00	R/W	8 (/16/32)
0x FFFF_5010	Modem Control Register		MCR	0x 00	R/W	8 (/16/32)
0x FFFF_5014	Line Status Register		LSR	0x 60	RO	8 (/16/32)
0x FFFF_5018	Modem Status Register		MSR	0x EX	RO	8 (/16/32)
0x FFFF_501C	Scratch Register		SCR	0x 00	R/W	8 (/16/32)
0x FFFF_5020	Test-0 Register		T0	0x 00	R/W	8 (/16/32)
0x FFFF_5024	Test-1 Register		T1	0x 00	R/W	8 (/16/32)
0x FFFF_5028	Test Status 0 Register		TS0	—	RO	8 (/16/32)
0x FFFF_502C	Test Status 1 Register		TS1	0x 01	RO	8 (/16/32)
0x FFFF_5030	Test Status 2 Register		TS2	0x 0F	RO	8 (/16/32)
0x FFFF_503C	Test Status 3 Register		TS3	0x 02	RO	8 (/16/32)
0x FFFF_8000	**RTC Related Register**		**RTC**			
0x FFFF_8000	RTC Run/Stop Control Register			xxx- --xx b	R/W	8(/16/32)
0x FFFF_8004	RTC Interrupt Register			0x xxxx	R/W	16(/32)
0x FFFF_8008	RTC Timer Dividing Register			xxxx xxxx b	R/(W)	8(/16/32)
0x FFFF_800C	RTC Second Counter Register			--xx xxxx b	R/W	8(/16/32)
0x FFFF_8010	RTC Minute Counter Register			--xx xxxx b	R/W	8(/16/32)
0x FFFF_8014	RTC Hour Counter Register			---x xxxx b	R/W	8(/16/32)
0x FFFF_8018	RTC Day Counter Register			---x xxxx b	R/W	8(/16/32)
0x FFFF_801C	RTC Month Counter Register			---- xxxx b	R/W	8(/16/32)
0x FFFF_8020	RTC Year Counter Register			-xxx xxxx b	R/W	8(/16/32)
0x FFFF_8024	RTC Alarm Minute Compare Register			--xx xxxx b	R/W	8(/16/32)
0x FFFF_8028	RTC Alarm Month Compare Register			---x xxxx b	R/W	8(/16/32)
0x FFFF_802C	RTC Alarm Day Compare Register			---x xxxx b	R/W	8(/16/32)
0x FFFF_8030	RTC Alarm Month Compare Register			---- xxxx b	R/W	8(/16/32)
0x FFFF_8034	RTC Alarm Year Compare Register			-xxx xxxx b	R/W	8(/16/32)
0x FFFF_8040	RTC Test Register			---x xxxx b	R/W	8(/16/32)
0x FFFF_8044	RTC Prescaler Register			-xxx xxxx b	R/(W)	8(/16/32)
0x FFFF_8048	RTC Test Clock Register			xxxx xxxx b	WO	8(/16/32)
0x FFFF_8060	RTC RAM0			xxxx xxxx b	R/W	8(/16/32)
0x FFFF_8064	RTC RAM1			xxxx xxxx b	R/W	8(/16/32)
0x FFFF_8068	RTC RAM2			xxxx xxxx b	R/W	8(/16/32)
0x FFFF_806C	RTC RAM3			xxxx xxxx b	R/W	8(/16/32)
0x FFFF_8070	RTC RAM4			xxxx xxxx b	R/W	8(/16/32)
0x FFFF_8074	RTC RAM5			xxxx xxxx b	R/W	8(/16/32)
0x FFFF_8078	RTC RAM6			xxxx xxxx b	R/W	8(/16/32)
0x FFFF_807C	RTC RAM7			xxxx xxxx b	R/W	8(/16/32)
0x FFFF_9000	**DMA Controller 2 Related Register**		**DMAC2**			
0x FFFF_9000	DMA Channel-0 Source Address Register		SAR0	0x XXXX_XXXX	R/W	32

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFF_9004	DMA Channel-0 Destination Address Register	DAR0	0x XXXX_XXXX	R/W	32
0x FFFF_9008	DMA Channel-0 Transfer Count Register	TCR0	0x 00XX_XXXX	R/W	32
0x FFFF_900C	DMA Channel-0 Control Register	CTL0	0x 0000_0000	R/W	32
0x FFFF_9010	DMA Channel-1 Source Address Register	SAR1	0x XXXX_XXXX	R/W	32
0x FFFF_9014	DMA Channel-1 Destination Address Register	DAR1	0x XXXX_XXXX	R/W	32
0x FFFF_9018	DMA Channel-1 Transfer Count Register	TCR1	0x 00XX_XXXX	R/W	32
0x FFFF_901C	DMA Channel-1 Control Register	CTL1	0x 0000_0000	R/W	32
0x FFFF_9020	DMA Channel-2 Source Address Register	SAR2	0x XXXX_XXXX	R/W	32
0x FFFF_9024	DMA Channel-2 Destination Address Register	DAR2	0x XXXX_XXXX	R/W	32
0x FFFF_9028	DMA Channel-2 Transfer Count Register	TCR2	0x 00XX_XXXX	R/W	32
0x FFFF_902C	DMA Channel-2 Control Register	CTL2	0x 0000_0000	R/W	32
0x FFFF_9030	DMA Channel-3 Source Address Register	SAR3	0x XXXX_XXXX	R/W	32
0x FFFF_9034	DMA Channel-3 Destination Address Register	DAR3	0x XXXX_XXXX	R/W	32
0x FFFF_9038	DMA Channel-3 Transfer Count Register	TCR3	0x 00XX_XXXX	R/W	32
0x FFFF_903C	DMA Channel-3 Control Register	CTL3	0x 0000_0000	R/W	32
0x FFFF_9060	DMA Channel Operating Select Register	OPSR	0x 0000_0000	R/W	32
0x FFFF_9064	DMA Channel MISC Register	MISC	0x 0000_0000	R/W	32
0x FFFF_9070	DMA Channel Transfer End Control Register	TECL	0x 0000_0000	R/W	32
0x FFFF_A000	**Memory Controller Related Register**	**MEMC**			
0x FFFF_A020	SRAM Device-0 Timing Register	RAMTMG0	0x 0000_1C7F	R/W	32
0x FFFF_A024	SRAM Device-0 Control Register	RAMCNTL0	0x 0000_0001	R/W	32
0x FFFF_A030	SRAM Device-1 Timing Register	RAMTMG1	0x 0000_1C7F	R/W	32
0x FFFF_A034	SRAM Device-1 Control Register	RAMCNTL1	0x 0000_0001	R/W	32
0x FFFF_A040	SRAM Device-2 Timing Register	RAMTMG2	0x 0000_1C7F	R/W	32
0x FFFF_A044	SRAM Device-2 Control Register	RAMCNTL2	0x 0000_0001	R/W	32
0x FFFF_A050	SRAM Device-3 Timing Register	RAMTMG3	0x 0000_1C7F	R/W	32
0x FFFF_A054	SRAM Device-3 Control Register	RAMCNTL3	0x 0000_0001	R/W	32
0x FFFF_A060	SDRAM Mode Register	SDMR	0x 0000_0032	R/W	16/32
0x FFFF_A064	Reserved	—	—	-/-	—
0x FFFF_A068	Reserved	—	—	-/-	—
0x FFFF_A070	SDRAM Setting Register	SDCNFG	0x 0600_C700	R/W	32
0x FFFF_A074	SDRAM Detailed Setting Register	SDADVCNFG	0x 000F_0300	R/W	32
0x FFFF_A080	Initialization Control Register	SDINIT	0x 0000_0000	R/W	16/32
0x FFFF_A090	SDRAM Refresh Timer Register	SDREF	0x 0000_00A0	R/W	16/32
0x FFFF_A0A0	SDRAM Status Register	SDSTAT	0x 0000_0202	RO	32
0x FFFF_B000	**TimerA Related Register**	**TIM**			
0x FFFF_B000	TimerA-0 Load Register	TM0LD	0x 0000	R/W	16 (/32)
0x FFFF_B004	TimerA-0 Count Register	TM0CNT	0x 0000	RO	16 (/32)
0x FFFF_B008	TimerA-0 Control Register	TM0CTRL	0x 0000	(R/W)	16 (/32)
0x FFFF_B00C	TimerA-0 IRQ Flag Clear Register	TM0IRQ	—	WO	8 (/16/32)
0x FFFF_B010	TimerA-0 Port Output Control Register	TM0POUT	0x 0000	(R/W)	8 (/16/32)
0x FFFF_B020	TimerA-1 Load Register	TM1LD	0x 0000	R/W	16 (/32)
0x FFFF_B024	TimerA-1 Count Register	TM1CNT	0x 0000	RO	16 (/32)
0x FFFF_B028	TimerA-1 Control Register	TM1CTRL	0x 0000	(R/W)	16 (/32)
0x FFFF_B02C	TimerA-1 IRQ Flag Clear Register	TM1IRQ	—	WO	8 (/16/32)

35. APPENDIX 1 S2S65A30 INTERNAL REGISTER LIST

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFF_B030	TimerA-1 Port Output Control Register	TM1POUT	0x 0000	(R/W)	8 (/16/32)
0x FFFF_B040	TimerA-2 Load Register	TM2LD	0x 0000	R/W	16 (/32)
0x FFFF_B044	TimerA-2 Count Register	TM2CNT	0x 0000	RO	16 (/32)
0x FFFF_B048	TimerA-2 Control Register	TM2CTRL	0x 0000	(R/W)	16 (/32)
0x FFFF_B04C	TimerA-2 IRQ Flag Clear Register	TM2IRQ	—	WO	8 (/16/32)
0x FFFF_B050	TimerA-2 Port Output Control Register	TM2POUT	0x 0000	(R/W)	8 (/16/32)
0x FFFF_B060 to 0x FFFF_B09C	Reserved	—	—	—	—
0x FFFF_B0A0	Prescaler 0 Control Register	PS0CTRL	0x 0000	(R/W)	16 (/32)
0x FFFF_B0A4	Prescaler 1 Control Register	PS1CTRL	0x 0000	(R/W)	16 (/32)
0x FFFF_B0B0	TimerA IRQ Status Register	TMAIRQSTS	0x 0000	RO	8 (/16/32)
0x FFFF_C000	**WDT Related Register**	**WDT**			
0x FFFF_C000	Watchdog Timer Load Register		0x 0000_FFFF	R/W	16 (/32)
0x FFFF_C004	Watchdog Timer Count Register		0x 0000_FFFF	RO	16 (/32)
0x FFFF_C008	Watchdog Timer Control Register		0x 0000_A500	R/W	16 (/32)
0x FFFF_D000	**System Controller Related Register**	**SYS**			
0x FFFF_D000	Chip ID Register	CHIPID	0x 065A_000X	RO	32
0x FFFF_D004	Chip Configuration Register	CHIPCFG	0x 0000_XXXX	RO	16 (/32)
0x FFFF_D008	PLL Setting Register 1	PLLSET1	0x 0421_84AE	R/W	32
0x FFFF_D00C	PLL Setting Register 2	PLLSET2	0x 0000_0000	(R/W)	16 (/32)
0x FFFF_D010	HALT Mode Clock Control Register	HALTMODE	0x 0000_0000	R/W	16 (/32)
0x FFFF_D014	IO Clock Control Register	IOCLKCTL	0x 0000_0000	R/W	16 (/32)
0x FFFF_D018	Clock Select Register	CLK_SEL	0x 0000_0000	R/W	16 (/32)
0x FFFF_D01C	HALT Control Register	HALTCTL	—	WO	16 (/32)
0x FFFF_D020	Memory Remap Register	REMAP	0x 0000_0000	R/W	16 (/32)
0x FFFF_D024	Software Reset Register	SOFTRST	—	WO	32
0x FFFF_D028	UART1 Clock Divider Register	UART1DIV	0x 0000_0000	R/W	16 (/32)
0x FFFF_D02C	UART2 Clock Divider Register	UART2DIV	0x 0000_0000	R/W	16 (/32)
0x FFFF_D030	UART3 Clock Divider Register	UART3DIV	0x 0000_0000	R/W	16 (/32)
0x FFFF_D034	Timer-B Clock Select Register	TIMBCKSEL	0x 0000_0000	R/W	16(/32)
0x FFFF_D040	MD Bus Pull-down Control Register	MDPLDCTL	0x 0000_0000	R/W	16 (/32)
0x FFFF_D044	SDD Bus Pull-down Control Register	SDDPLDCTL	0x 0000_0000	R/W	16(/32)
0x FFFF_D048	GPIOE Resistor Control Register	PORTERCTL	0x 0000_0000	R/W	16 (/32)
0x FFFF_D04C	GPIOF Resistor Control Register	PORTFRCTL	0x 0000_0000	R/W	16 (/32)
0x FFFF_D050	GPIOG Resistor Control Register	PORTGRCTL	0x 0000_0000	R/W	16 (/32)
0x FFFF_D054	GPIOH Resistor Control Register	PORTHRCTL	0x 0000_0000	R/W	16(/32)
0x FFFF_D058	GPIOI Resistor Control Register	PORTIRCTL	0x 0000_0000	R/W	16(/32)
0x FFFF_D05C	GPIOJ Resistor Control Register	PORTJRCTL	0x 0000_0000	R/W	16(/32)
0x FFFF_D060	GPIOK Resistor Control Register	PORTKRCTL	0x 0000_0000	R/W	16(/32)
0x FFFF_D064	Internal TEST Mode Register	ITESTM	0x 0000_0000	R/W	32
0x FFFF_D068	Embedded Memory Control Register	EMBMEMCTL	0x 0000_0000	R/W	32
0x FFFF_D06C	MISC Register	MISC	0x 0000_0000	R/W	32
0x FFFF_F000	**Interrupt Controller Related Register**	**INT**			
0x FFFF_F000	IRQ Status Register		0x 0000_0000	RO	32
0x FFFF_F004	Status Register Before IRQ Mask		0x 0000_0000	RO	32
0x FFFF_F008	IRQ Enable Register		0x 0000_0000	R/W	32
0x FFFF_F00C	IRQ Enable Clear Register		0x 0000_0000	WO	32
0x FFFF_F010	Software IRQ Register		0x 0000_0000	WO	32
0x FFFF_F020	IRQxx Status Register		0x 0000_0000	RO	32
0x FFFF_F024	Status Register Before IRQxx Mask		0x 0000_0000	RO	32
0x FFFF_F028	IRQxx Enable Register		0x 0000_0000	R/W	32
0x FFFF_F02C	IRQxx Enable Clear Register		0x 0000_0000	WO	32

Address (Hex)	Register Name	Register Abbreviation	Default (Hex) *1	R/W	Data Access Size (bits) *2
0x FFFF_F080	IRQ Level Register		0x 0000_0000	R/W	32
0x FFFF_F084	IRQ Polarity Register		0x FFFF_FFFF	R/W	32
0x FFFF_F088	IRQ Trigger Reset Register		0x 0000_0000	WO	32
0x FFFF_F0A0	IRQxx Level Register		0x 0000_0000	R/W	32
0x FFFF_F0A4	IRQxx Polarity Register		0x 0000_0FFF	R/W	32
0x FFFF_F0A8	IRQxx Trigger Reset Register		0x 0000_0000	WO	32
0x FFFF_F100	FIQ Status Register		0x 0000_0000	RO	32
0x FFFF_F104	Status Register Before FIQ Mask		0x 0000_0000	RO	32
0x FFFF_F108	FIQ Enable Register		0x 0000_0000	R/W	32
0x FFFF_F10C	FIQ Enable Clear Register		0x 0000_0000	WO	32
0x FFFF_F180	FIQ Level Register		0x 0000_0000	R/W	32
0x FFFF_F184	FIQ Polarity Register		0x 0000_0003	R/W	32
0x FFFF_F188	FIQ Trigger Reset Register		0x 0000_0000	WO	32

*1: The default value (or the initial value) is shown in hexadecimal notation and character “h” is added after the value. If character “b” is added after the value, it is a binary value.
Also, “X” represents the undefined hexadecimal value, and “x” represents the undefined binary value.

*2: The data access size is shown in bits which is equal to the register access size. Value 8 (or 16 or 32) is usually used to access to 8-bit data. If the 16- or 32-bit data access instruction is used, the 16- or 32-bit data can also be accessed. Similarly, value 16 (or 32) is usually used to access to 16-bit data but the 32-bit data can also be accessed. In these cases, only the low-order bits must be significant.

REVISION HISTORY

Appendix-1

Rev. No.	Date	Page	Type	Description of revisions (including contents of previous revisions) and reasons
Rev 1.0	2009/08	All pages	New	Newly established Added new register to Appendix register MAP.
Rev 1.2	2010/4/15	-	Add Revise	Revision of misentry Add the explanation for required SDRAM buffer area of IPC Add “IPC Video Output Vertical Blank Line Number” Register Add “ADC current” and “ADC input impedance” to Electric Characteristic Delete “ADC End Flag” Register Add the attention of power on timing
Rev 1.3	2011/11/18	Appendix1	Update	DAM control register channel 0/1/2/3 initial value 0x0000_0000 -> 0x00XX_XXXX JPEG line buffer current status flag register initial value 0x0009 -> 0xX009 UART 0/1/2/3 line status register initial value 0x00 -> 0x06 UART 0/1/2/3 modem status register initial value 0x00 -> 0xEX UART 0/1/2/3 test status register 1 initial value 0x00 -> 0x01 UART 0/1/2/3 test status register 2 initial value 0x00 -> 0x0F UART 0/1/2/3 test status register 3 initial value 0x00 -> 0x02 I2C I/O control register initial value 0x11 -> 0x00

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