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S1D14F57
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.0

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NOTICE

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1. Overview

The S1D14F57 is a two-level grayscale EPD passive panel driver IC. The device integrates drivers that are necessary for display updates of the EPD passive panel (segment (256 pins), top plane (4 pin) and back plane (4 pin)) and a control circuit for driver waveforms to one chip. The device also includes a Flash memory that stores output drive waveform data for the EPD passive panel drivers and a power supply circuit. The S1D14F57 can compose a two-level grayscale EPD passive panel display controller of a minimum number of parts.

2. Features

The S1D14F57 functions and features are shown below.

- Segment outputs : 256 pins
- Top plane output : 4 pin
- Back plane output : 4 pin
- EPD display waveform setting : 7 types (max.) can be stored in the built-in Flash memory.
  EPD display waveforms can be automatically selected with the automatic temperature detection function.
  One type can be set with the command interfaces.
  (32 phases max.)
- Built-in Flash memory : Capacity: 16k bits (storage for output drive waveform setting / initial setting)
  Erase-programming cycles: 10 times.
  Power supply for erase / programming (VPP): necessary
  You can reprogram the built-in Flash memory through the EPD microcontroller from Seiko Epson using the debug tool "ICDmini". note1
- Built-in temperature detection circuit : Temperature range -10 °C to 60 °C (±5°C)
  Temperature detection precision ±5°C
- Clock generator : 2 MHz (typ.) built-in oscillation circuit
- Power-on reset circuit : Built-in
- Command interfaces : I2C slave interface note2
  SPI interface
- Deep standby function : ≤ 1μA(25°C)
- Currently displayed data retention function : Built-in 257-bit register for V_{DD} power supply (ESEG0 to ESEG255, for storing currently displayed data for EBP)

- Boost power supply circuit : VOUT1 Booster
- EPD drive power supply : VEPD Booster = 9.15V/12.30V/15.45V
- Power supply for internal power supply circuit / power supply for logic signal I/O circuits
  : V_{DD} = 1.75V to 5.50V

- Expansion function for EPD drive pins of Seiko Epson EPD microcontrollers
- Multi-chip EPD drive function

- Shipment forms :Aluminum pad chip,
  Gold bump chip (T.B.D.)

Note1:For details about how to erase/reprogram the built-in Flash memory, contact our representatives.

Note2: The 10-bit address mode/general call address/HS mode are not supported.

3. Block Diagram

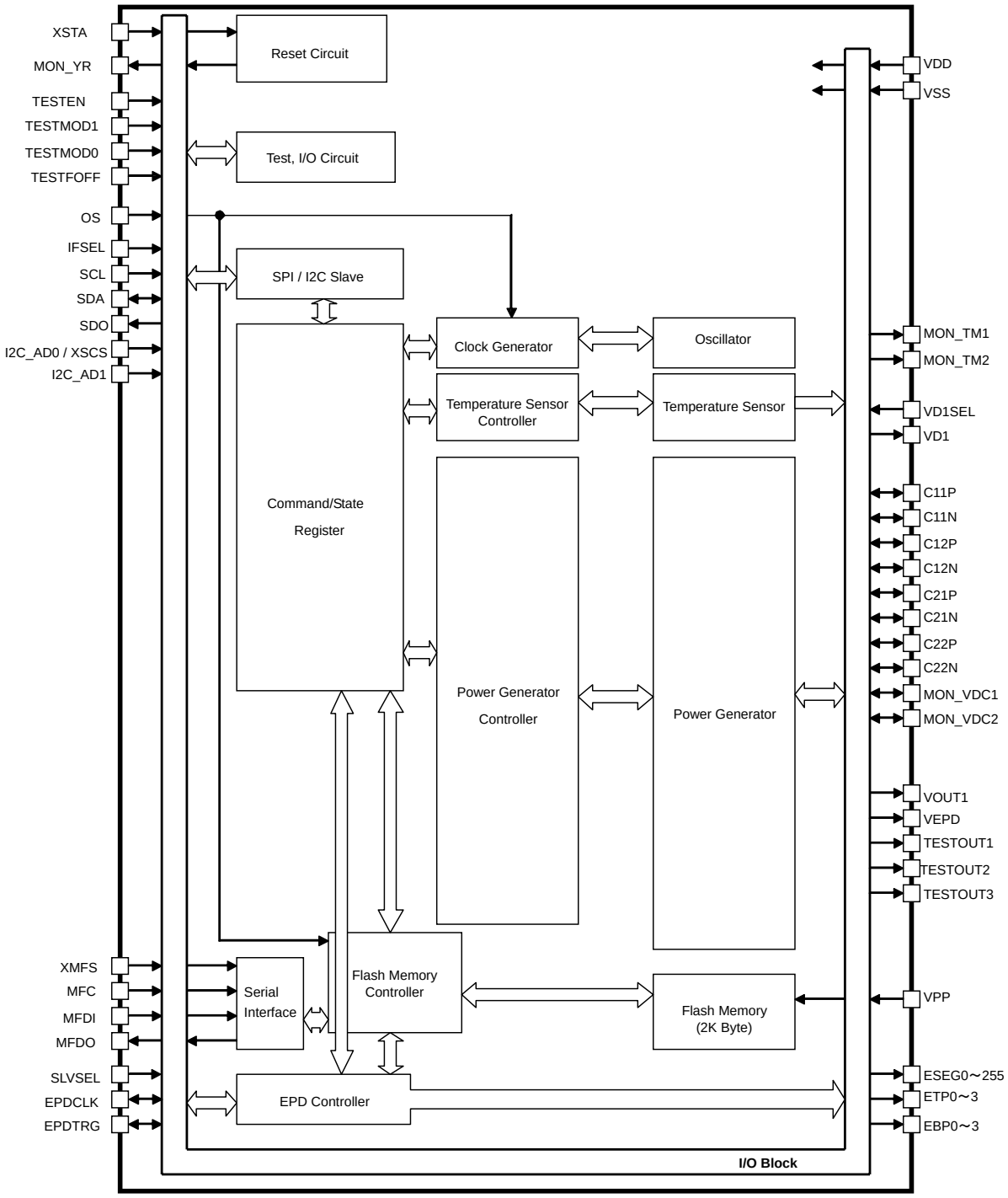

Figure 3.1 S1D14F57 block diagram

4. Chip Specifications

4.1 Chip Information

Table 4.1 Chip specifications

Item		Size		Unit
		X	Y	
Chip size		16.0	1.0	mm
Chip thickness		200 / 300 / 400		μm
Pad opening	No. 2 to 144, 147 to 342	70	96	μm
	No.1,145,146,343	66	96	μm
Minimum bump pitch		80		μm
Bump size	No. 2 to 144, 147 to 342	58	84	μm
	No.1,145,146,343	54	84	μm
Bump height		15		μm
Bump total area		1669752		μm^2

Note) Values are for reference, and not guaranteed.

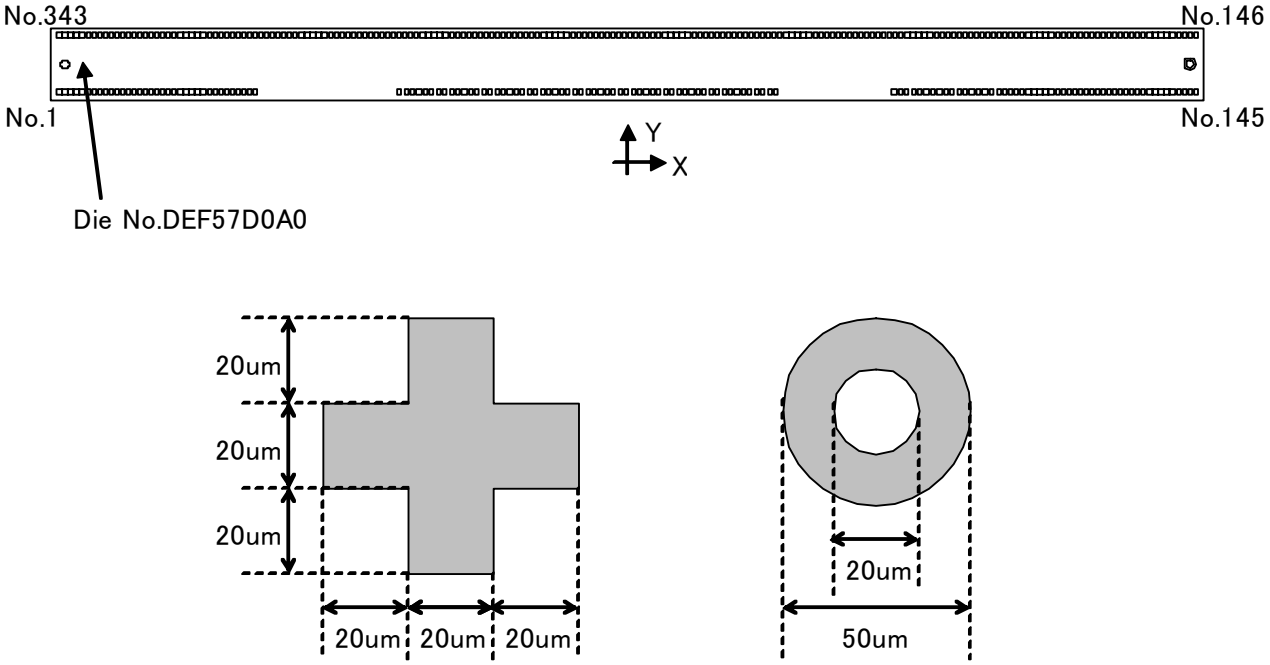

Figure 4.1 External view of the chip

4.2 Bump Center Coordinates

Table 4.2 Bump center coordinates

BUMP No.	Signal name	X-Coord (mm)	Y-Coord (mm)
1	Dummy	-7.878	-0.386
2	ESEG31	-7.800	-0.386
3	ESEG30	-7.720	-0.386
4	ESEG29	-7.640	-0.386
5	ESEG28	-7.560	-0.386
6	ESEG27	-7.480	-0.386
7	ESEG26	-7.400	-0.386
8	ESEG25	-7.320	-0.386
9	ESEG24	-7.240	-0.386
10	ESEG23	-7.160	-0.386
11	ESEG22	-7.080	-0.386
12	ESEG21	-7.000	-0.386
13	ESEG20	-6.920	-0.386
14	ESEG19	-6.840	-0.386
15	ESEG18	-6.760	-0.386
16	ESEG17	-6.680	-0.386
17	ESEG16	-6.600	-0.386
18	ESEG15	-6.520	-0.386
19	ESEG14	-6.440	-0.386
20	ESEG13	-6.360	-0.386
21	ESEG12	-6.280	-0.386
22	ESEG11	-6.200	-0.386
23	ESEG10	-6.120	-0.386
24	ESEG9	-6.040	-0.386
25	ESEG8	-5.960	-0.386
26	ESEG7	-5.880	-0.386
27	ESEG6	-5.800	-0.386
28	ESEG5	-5.720	-0.386
29	ESEG4	-5.640	-0.386
30	ESEG3	-5.560	-0.386
31	ESEG2	-5.480	-0.386
32	ESEG1	-5.400	-0.386
33	ESEG0	-5.320	-0.386
34	EBP0	-5.240	-0.386
35	ETP0	-5.160	-0.386
36	Dummy	-3.160	-0.386
37	Dummy	-3.070	-0.386
38	Vss	-2.980	-0.386
39	Vss	-2.890	-0.386
40	Vss	-2.800	-0.386

BUMP No.	Signal name	X-Coord (mm)	Y-Coord (mm)
173	ESEG199	5.720	0.386
174	ESEG198	5.640	0.386
175	ESEG197	5.560	0.386
176	ESEG196	5.480	0.386
177	ESEG195	5.400	0.386
178	ESEG194	5.320	0.386
179	ESEG193	5.240	0.386
180	ESEG192	5.160	0.386
181	ESEG191	5.080	0.386
182	ESEG190	5.000	0.386
183	ESEG189	4.920	0.386
184	ESEG188	4.840	0.386
185	ESEG187	4.760	0.386
186	ESEG186	4.680	0.386
187	ESEG185	4.600	0.386
188	ESEG184	4.520	0.386
189	ESEG183	4.440	0.386
190	ESEG182	4.360	0.386
191	ESEG181	4.280	0.386
192	ESEG180	4.200	0.386
193	ESEG179	4.120	0.386
194	ESEG178	4.040	0.386
195	ESEG177	3.960	0.386
196	ESEG176	3.880	0.386
197	ESEG175	3.800	0.386
198	ESEG174	3.720	0.386
199	ESEG173	3.640	0.386
200	ESEG172	3.560	0.386
201	ESEG171	3.480	0.386
202	ESEG170	3.400	0.386
203	ESEG169	3.320	0.386
204	ESEG168	3.240	0.386
205	ESEG167	3.160	0.386
206	ESEG166	3.080	0.386
207	ESEG165	3.000	0.386
208	ESEG164	2.920	0.386
209	ESEG163	2.840	0.386
210	ESEG162	2.760	0.386
211	ESEG161	2.680	0.386
212	ESEG160	2.600	0.386

BUMP No.	Signal name	X-Coord (mm)	Y-Coord (mm)
41	Dummy	-2.710	-0.386
42	TESTOUT1	-2.620	-0.386
43	MON_VDC2	-2.530	-0.386
44	MON_VDC1	-2.440	-0.386
45	VOUT1	-2.350	-0.386
46	VOUT1	-2.260	-0.386
47	VOUT1	-2.170	-0.386
48	VOUT1	-2.080	-0.386
49	C11P	-1.990	-0.386
50	C11P	-1.900	-0.386
51	C11P	-1.810	-0.386
52	C11N	-1.720	-0.386
53	C11N	-1.630	-0.386
54	C11N	-1.540	-0.386
55	C12P	-1.450	-0.386
56	C12P	-1.360	-0.386
57	C12P	-1.270	-0.386
58	C12N	-1.180	-0.386
59	C12N	-1.090	-0.386
60	C12N	-1.000	-0.386
61	Dummy	-0.910	-0.386
62	C21P	-0.820	-0.386
63	C21P	-0.730	-0.386
64	C21P	-0.640	-0.386
65	C21N	-0.550	-0.386
66	C21N	-0.460	-0.386
67	C21N	-0.370	-0.386
68	C22P	-0.280	-0.386
69	C22P	-0.190	-0.386
70	C22P	-0.100	-0.386
71	C22N	-0.010	-0.386
72	C22N	0.080	-0.386
73	C22N	0.170	-0.386
74	TESTOUT2	0.260	-0.386
75	VEPD	0.350	-0.386
76	VEPD	0.440	-0.386
77	VEPD	0.530	-0.386
78	TESTOUT3	0.620	-0.386
79	Dummy	0.710	-0.386
80	V_{DD}	0.800	-0.386
81	V_{DD}	0.890	-0.386
82	V_{DD}	0.980	-0.386
83	Dummy	1.070	-0.386

BUMP No.	Signal name	X-Coord (mm)	Y-Coord (mm)
213	ESEG159	2.520	0.386
214	ESEG158	2.440	0.386
215	ESEG157	2.360	0.386
216	ESEG156	2.280	0.386
217	ESEG155	2.200	0.386
218	ESEG154	2.120	0.386
219	ESEG153	2.040	0.386
220	ESEG152	1.960	0.386
221	ESEG151	1.880	0.386
222	ESEG150	1.800	0.386
223	ESEG149	1.720	0.386
224	ESEG148	1.640	0.386
225	ESEG147	1.560	0.386
226	ESEG146	1.480	0.386
227	ESEG145	1.400	0.386
228	ESEG144	1.320	0.386
229	ESEG143	1.240	0.386
230	ESEG142	1.160	0.386
231	ESEG141	1.080	0.386
232	ESEG140	1.000	0.386
233	ESEG139	0.920	0.386
234	ESEG138	0.840	0.386
235	ESEG137	0.760	0.386
236	ESEG136	0.680	0.386
237	ESEG135	0.600	0.386
238	ESEG134	0.520	0.386
239	ESEG133	0.440	0.386
240	ESEG132	0.360	0.386
241	ESEG131	0.280	0.386
242	ESEG130	0.200	0.386
243	ESEG129	0.120	0.386
244	ESEG128	0.040	0.386
245	ESEG127	-0.040	0.386
246	ESEG126	-0.120	0.386
247	ESEG125	-0.200	0.386
248	ESEG124	-0.280	0.386
249	ESEG123	-0.360	0.386
250	ESEG122	-0.440	0.386
251	ESEG121	-0.520	0.386
252	ESEG120	-0.600	0.386
253	ESEG119	-0.680	0.386
254	ESEG118	-0.760	0.386
255	ESEG117	-0.840	0.386

BUMP No.	Signal name	X-Coord (mm)	Y-Coord (mm)
84	MON_TM1	1.162	-0.386
85	MON_TM2	1.252	-0.386
86	MON_YR	1.342	-0.386
87	VD1	1.430	-0.386
88	Dummy	1.520	-0.386
89	TESTFOFF	1.610	-0.386
90	TESTMOD0	1.700	-0.386
91	TESTMOD1	1.790	-0.386
92	TESTEN	1.880	-0.386
93	Dummy	1.970	-0.386
94	VPP	2.060	-0.386
95	VD1SEL	3.696	-0.386
96	SLVSEL	3.786	-0.386
97	IFSEL	3.876	-0.386
98	OS	3.966	-0.386
99	XMFS	4.056	-0.386
100	MFC	4.146	-0.386
101	MFDI	4.236	-0.386
102	MFDO	4.326	-0.386
103	EPDCLK	4.416	-0.386
104	EPDTRG	4.506	-0.386
105	SCL	4.596	-0.386
106	SDA	4.686	-0.386
107	SDO	4.776	-0.386
108	I2C_AD0_XSCS	4.866	-0.386
109	I2C_AD1	4.956	-0.386
110	XSTA	5.046	-0.386
111	ETP3	5.160	-0.386
112	EBP3	5.240	-0.386
113	ESEG255	5.320	-0.386
114	ESEG254	5.400	-0.386
115	ESEG253	5.480	-0.386
116	ESEG252	5.560	-0.386
117	ESEG251	5.640	-0.386
118	ESEG250	5.720	-0.386
119	ESEG249	5.800	-0.386
120	ESEG248	5.880	-0.386
121	ESEG247	5.960	-0.386
122	ESEG246	6.040	-0.386
123	ESEG245	6.120	-0.386
124	ESEG244	6.200	-0.386
125	ESEG243	6.280	-0.386
126	ESEG242	6.360	-0.386

BUMP No.	Signal name	X-Coord (mm)	Y-Coord (mm)
256	ESEG116	-0.920	0.386
257	ESEG115	-1.000	0.386
258	ESEG114	-1.080	0.386
259	ESEG113	-1.160	0.386
260	ESEG112	-1.240	0.386
261	ESEG111	-1.320	0.386
262	ESEG110	-1.400	0.386
263	ESEG109	-1.480	0.386
264	ESEG108	-1.560	0.386
265	ESEG107	-1.640	0.386
266	ESEG106	-1.720	0.386
267	ESEG105	-1.800	0.386
268	ESEG104	-1.880	0.386
269	ESEG103	-1.960	0.386
270	ESEG102	-2.040	0.386
271	ESEG101	-2.120	0.386
272	ESEG100	-2.200	0.386
273	ESEG99	-2.280	0.386
274	ESEG98	-2.360	0.386
275	ESEG97	-2.440	0.386
276	ESEG96	-2.520	0.386
277	ESEG95	-2.600	0.386
278	ESEG94	-2.680	0.386
279	ESEG93	-2.760	0.386
280	ESEG92	-2.840	0.386
281	ESEG91	-2.920	0.386
282	ESEG90	-3.000	0.386
283	ESEG89	-3.080	0.386
284	ESEG88	-3.160	0.386
285	ESEG87	-3.240	0.386
286	ESEG86	-3.320	0.386
287	ESEG85	-3.400	0.386
288	ESEG84	-3.480	0.386
289	ESEG83	-3.560	0.386
290	ESEG82	-3.640	0.386
291	ESEG81	-3.720	0.386
292	ESEG80	-3.800	0.386
293	ESEG79	-3.880	0.386
294	ESEG78	-3.960	0.386
295	ESEG77	-4.040	0.386
296	ESEG76	-4.120	0.386
297	ESEG75	-4.200	0.386
298	ESEG74	-4.280	0.386

BUMP No.	Signal name	X-Coord (mm)	Y-Coord (mm)
127	ESEG241	6.440	-0.386
128	ESEG240	6.520	-0.386
129	ESEG239	6.600	-0.386
130	ESEG238	6.680	-0.386
131	ESEG237	6.760	-0.386
132	ESEG236	6.840	-0.386
133	ESEG235	6.920	-0.386
134	ESEG234	7.000	-0.386
135	ESEG233	7.080	-0.386
136	ESEG232	7.160	-0.386
137	ESEG231	7.240	-0.386
138	ESEG230	7.320	-0.386
139	ESEG229	7.400	-0.386
140	ESEG228	7.480	-0.386
141	ESEG227	7.560	-0.386
142	ESEG226	7.640	-0.386
143	ESEG225	7.720	-0.386
144	ESEG224	7.800	-0.386
145	Dummy	7.878	-0.386
146	Dummy	7.878	0.386
147	ETP2	7.800	0.386
148	EBP2	7.720	0.386
149	ESEG223	7.640	0.386
150	ESEG222	7.560	0.386
151	ESEG221	7.480	0.386
152	ESEG220	7.400	0.386
153	ESEG219	7.320	0.386
154	ESEG218	7.240	0.386
155	ESEG217	7.160	0.386
156	ESEG216	7.080	0.386
157	ESEG215	7.000	0.386
158	ESEG214	6.920	0.386
159	ESEG213	6.840	0.386
160	ESEG212	6.760	0.386
161	ESEG211	6.680	0.386
162	ESEG210	6.600	0.386
163	ESEG209	6.520	0.386
164	ESEG208	6.440	0.386
165	ESEG207	6.360	0.386
166	ESEG206	6.280	0.386
167	ESEG205	6.200	0.386
168	ESEG204	6.120	0.386
169	ESEG203	6.040	0.386

BUMP No.	Signal name	X-Coord (mm)	Y-Coord (mm)
299	ESEG73	-4.360	0.386
300	ESEG72	-4.440	0.386
301	ESEG71	-4.520	0.386
302	ESEG70	-4.600	0.386
303	ESEG69	-4.680	0.386
304	ESEG68	-4.760	0.386
305	ESEG67	-4.840	0.386
306	ESEG66	-4.920	0.386
307	ESEG65	-5.000	0.386
308	ESEG64	-5.080	0.386
309	ESEG63	-5.160	0.386
310	ESEG62	-5.240	0.386
311	ESEG61	-5.320	0.386
312	ESEG60	-5.400	0.386
313	ESEG59	-5.480	0.386
314	ESEG58	-5.560	0.386
315	ESEG57	-5.640	0.386
316	ESEG56	-5.720	0.386
317	ESEG55	-5.800	0.386
318	ESEG54	-5.880	0.386
319	ESEG53	-5.960	0.386
320	ESEG52	-6.040	0.386
321	ESEG51	-6.120	0.386
322	ESEG50	-6.200	0.386
323	ESEG49	-6.280	0.386
324	ESEG48	-6.360	0.386
325	ESEG47	-6.440	0.386
326	ESEG46	-6.520	0.386
327	ESEG45	-6.600	0.386
328	ESEG44	-6.680	0.386
329	ESEG43	-6.760	0.386
330	ESEG42	-6.840	0.386
331	ESEG41	-6.920	0.386
332	ESEG40	-7.000	0.386
333	ESEG39	-7.080	0.386
334	ESEG38	-7.160	0.386
335	ESEG37	-7.240	0.386
336	ESEG36	-7.320	0.386
337	ESEG35	-7.400	0.386
338	ESEG34	-7.480	0.386
339	ESEG33	-7.560	0.386
340	ESEG32	-7.640	0.386
341	EBP1	-7.720	0.386

BUMP No.	Signal name	X-Coord (mm)	Y-Coord (mm)
170	ESEG202	5.960	0.386
171	ESEG201	5.880	0.386
172	ESEG200	5.800	0.386

BUMP No.	Signal name	X-Coord (mm)	Y-Coord (mm)
342	ETP1	-7.800	0.386
343	Dummy	-7.878	0.386

5. Pin Descriptions

5.1 Power Supply Pins

5.1.1 External Power Supply Pins

Table 5.1.1 External power supply pin descriptions

Pin	I/O	Descriptions	Number of pins
V_{DD}	Power supply	Power supply for I/O circuits and the internal power supply circuit	3
V_{SS}	Power supply	Ground pin 0V pin connected to the system GND Base potential of this device	3

5.1.2 Internally Generated Power Supply

Table 5.1.2 Internally generated power supply pin descriptions

Pin	I/O	Descriptions	Number of pins
VD1	Power supply	Power supply for internal logic circuits and the built-in oscillation circuit Connect a stabilization capacitor (0.1μF).	1

5.1.3 VD1 Setting Pin (V_{DD} System I/O)

Table 5.1.3 VD1 setting pin descriptions

Pin	I/O	Descriptions	Number of pins
VD1SEL	I	Input pin to set the VD1 operation Make sure to fix this pin to High level (V_{DD}).	1

5.1.4 Boost Pins

Table 5.1.4 Boost pin descriptions

Pin	I/O	Descriptions	Number of pins
VOUT1	Power supply	VOUT1 boost circuit generation power supply output pin Connect a stabilization capacitor (0.1μF or 1.0μF) between V_{SS} and this pin.	4
VEPD	Power supply	EPD system power supply circuit output pin Connect a stabilization capacitor (0.1μF or 1.0μF) between V_{SS} and this pin.	3
C11P	Power supply	Connection pin for a flying capacitor positive electrode	3
C11N	Power supply	Connection pin for a flying capacitor negative electrode	3
C12P	Power supply	Connection pin for a flying capacitor positive electrode	3
C12N	Power supply	Connection pin for a flying capacitor negative electrode	3
C21P	Power supply	Connection pin for a flying capacitor positive electrode	3
C21N	Power supply	Connection pin for a flying capacitor negative electrode	3
C22P	Power supply	Connection pin for a flying capacitor positive electrode	3
C22N	Power supply	Connection pin for a flying capacitor negative electrode	3

5.2 Reset Pin (V_{DD} System I/O)

Table 5.2 Reset pin descriptions

Pin	I/O	Descriptions	Number of pins
XSTA	I	Deep standby control pin ・Low level: deep standby (VD1 off) state ・High level: standby (VD1 on) state	1

5.3 EPD Drive Pins (VEPD System I/O)

Table 5.3 EPD drive pin descriptions

Pin	I/O	Descriptions	Number of pins
ESEG	O	Output pins for the EPD segment (ESEG0 to ESEG255)	256
ETP	O	Output pin for the EPD top plane (ETP0 to ETP3)	4
EBP	O	Output pin for the EPD back plane (EBP0 to EBP3)	4

5.4 EPD_MCU EPD Driver Expansion Pin / Control Pin in Multi-chip Use (V_{DD} System I/O)

In deep stand-by mode, input/output for the pins listed in Table 5.4 are all disabled.

Table 5.4 EPD_MCU EPD driver expansion pin / control pin in multi-chip use descriptions

Pin	I/O	Descriptions	Number of pins
SLVSEL	I	Selection pin according to the purpose of using this device ・Low level: when this device is used alone / as a master IC in multi-chip use ・High level: when this device is used for MCU_EPD driver expansion / as a slave IC in multi-chip use	1
EPDCLK	I/O	Clock input / output pin to synchronize with EPD display updates ・SLVSEL pin = Low level: output state ・SLVSEL pin = High level: input state	1
EPDTRG	I/O	Starting trigger input / output pin to synchronize with EPD display updates ・SLVSEL pin = Low level: output state ・SLVSEL pin = High level: input state	1

5.5 Command Interface Pins (V_{DD} System I/O)

5.5.1 Command Interface Selection Pin

In deep stand-by mode, input for the pins listed in Table 5.5.1 are all disabled.

Table 5.5.1 Command interface selection pin descriptions

Pin	I/O	Descriptions	Number of pins
IFSEL	I	Command interface selection pin ・Low level: I2C slave interface ・High level: SPI slave interface	1

5.5.2 I2C/SPI Slave Interface Signal Pins (VDD System I/O)

In deep stand-by mode, input/output for the pins listed in Table 5.5.2 are all disabled.

Table 5.5.2 I2C/SPI slave interface signal pin descriptions

Pin	I/O	Descriptions		Number of pins
SCL	I	IFSEL pin = Low level	Serial clock input pin for the I2C slave interface control	1
		IFSEL pin = High level	Serial clock input pin for the SPI slave interface control	
SDA	I/O	IFSEL pin = Low level	Data input / output pin for the I2C slave interface control	1
		IFSEL pin = High level	Data input / output pin for the SPI slave interface control	
SDO	O	IFSEL pin = Low level	Make this pin to be open when the I2C slave interface is selected.	1
		IFSEL pin = High level	Data input / output pin for the SPI slave interface control	
I2C_AD0 / XSCS	I	IFSEL pin = Low level	If the I2C slave interface is selected, the input for this pin controls the value of the lowest bit of the slave address. You can set the pin input as required.	1
		IFSEL pin = High level	Chip-select input pin for the SPI slave interface control	
I2C_AD1	I	IFSEL pin = Low level	If the I2C slave interface is selected, the input for this pin controls the value of the second lowest bit of the slave address. You can set the pin input as required.	1
		IFSEL pin = High level	This pin may be open when the SPI slave interface is selected.	

5.6 Flash Memory System Pins

5.6.1 Flash Memory Power Supply Pin

Table 5.6.1 Flash memory power supply pin descriptions

Pin	I/O	Descriptions	Number of pins
VPP	Power supply	This is the power supply terminal that is used to program/erase the internal flash memory. Make it to be open in other operations.	1

5.6.2 Flash Memory Writer Pins (V_{DD} System I/O)

In deep stand-by mode, input/output for the pins listed in Table 5.6.2 are all disabled.

Table 5.6.2 Flash serial memory writer system pin descriptions

Pin	I/O	Descriptions	Number of pins
XMFS	I	Chip select pin for the Flash memory writer An internal pull-up resistor is connected always. You can set this pin to open.	1
MFC	I	Clock pin for the Flash memory writer XMFS pin = High level: You can set this pin to open.	1
MFDI	I	Data input pin for the Flash memory writer XMFS pin = High level: You can set this pin to open.	1
MFDO	O	Data output pin of the Flash memory writer XMFS pin = High level: high impedance	1
OS	I	Connect this pin to the Flash memory pin “MF_CK” directly. XMFS pin = High level: You can set this pin to open. XMFS pin = Low level: connect to the Flash memory clock directly.	1

5.7 Test System Pins

Table 5.7 Test system pin descriptions

Pin	I/O	Descriptions	Number of pins
TESTEN	I	Test pin Set to Low level.	1
TESTMOD 1-0	I	Test pin Set to Low level.	2
TESTFOFF	I	Test pin Set to Low level.	1
MON_TM1	I/O	Test pin Set to be open.	1
MON_TM2	I/O	Test pin Set to be open.	1
MON_YR	O	Test pin Set to be open.	1
MON_VDC1	O	Test pin Set to be open.	1
MON_VDC2	O	Test pin Set to be open.	1
TESTOUT1	O	Test pin Set to be open.	1
TESTOUT2	O	Test pin Set to be open.	1
TESTOUT3	O	Test pin Set to be open.	1

6. Recommended Values for External Parts

Table 6.1 Recommended Values for external parts

Symbol	Name	Recommended Values	Maximum Apply Voltage
C1	Capacitor between VD1 and Vss	0.1μF	1.95V
C2	Capacitor between C11P and C11N	0.1μF or 1.0μF	3.00V
C3	Capacitor between C12P and C12N		3.00V
C4	Capacitor between VOUT1 and Vss		6.0V
C5	Capacitor between C21P and C21N		5.5V
C6	Capacitor between C22P and C22N		5.5V
C7	Capacitor between VEPD and Vss		16.5V

Note: Use the same capacitance for the capacitors C2 through C7 listed in Table 6.1 Recommended Values for the External Components.

Possible combinations of the capacitance of the capacitors C2 through C7 listed in Table 6.1 "Recommended Values for the External Components", the VDD voltage, the frequencies of the step-up clocks, and the VEPD maximum load current are listed in Table 6.2 VEPD Maximum Load Current for Specified Conditions.

Table 6.2 VEPD Maximum Load Current for Specified Conditions *1

C2 to C7 capacitance	VDD voltage	VOUT1 step-up clock frequency *2	VEPD step-up clock frequency *3	VEPD maximum load current
0.1μF	1.75V to 3.60V	62.5KHz	32KHz	100μA
	3.00V to 5.50V	62.5KHz	32KHz	700μA
		32KHz	16KHz	500μA
		16KHz	8KHz	300μA
		8KHz	4KHz	100μA
1.0μF	1.75V to 3.60V	8KHz	4KHz	100μA
	3.00V to 5.50V	8KHz	4KHz	700μA

*1: Maximum load current that satisfies VEPD=9.00V, 12.00V, 15.00V±5%

*2: Specified by the POWCTL command parameter B25-B24 (VOUT1FREQ[1:0])

*3: Specified by the POWCTL command parameter B21-B20 (VEPDFREQ[1:0])

Choose the appropriate capacitance and setting based on Table 6.2 VEPD Maximum Load Current for Specified Conditions.

7. Functional Descriptions

7.1 Deep Standby Function

The device has the deep standby function that stops the power supply VD1 Regulator operation (refer to "7.3.3.1 VD1 Regulator") for the internal logic circuits / built-in oscillation circuit, while EPD display updates are not executed. This function can reduce the V_{DD} current consumption during the above period.

7.1.1 Deep Standby Outline

The deep standby outline is shown as follows.

- V_{DD} current consumption: ≤ 1μA(at 25°C)
- VD1 Regulator operation: stopped
- Issue from command interface: impossible

7.1.2 Deep Standby Control

The XSTA pin controls the deep standby state. The followings show the XSTA pin control.

- Low level: deep standby state
- High level: standby state (command issue: possible)

7.1.3 Transition to Deep Standby

When the XSTA pin is set to Low level, the device starts the transition to the deep standby state.

The device enters into the deep standby state by 1ms after the XSTA pin is set to Low level.

Note: Do not make a deep standby release during the deep standby transition (within 1ms)

Figure 7.1.3 shows the deep standby transition sequence.

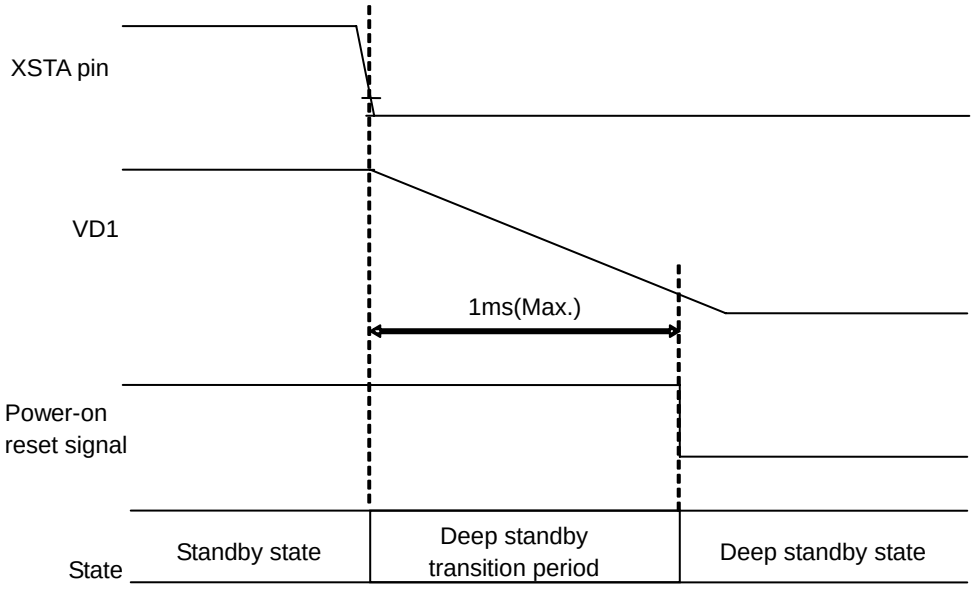

Figure 7.1.3 Deep standby state transition

7.1.4 Deep Standby Release

When the XSTA pin is set to High level, the deep standby state is released. After the release, the power-on reset circuit in this device releases the internal reset state.

After the deep standby state release, the device enters into the standby state.

Note: Be sure to set XSTA at a high level and wait at least 200 μs before issuing a command.

Figure 7.1.4 shows the deep standby release sequence.

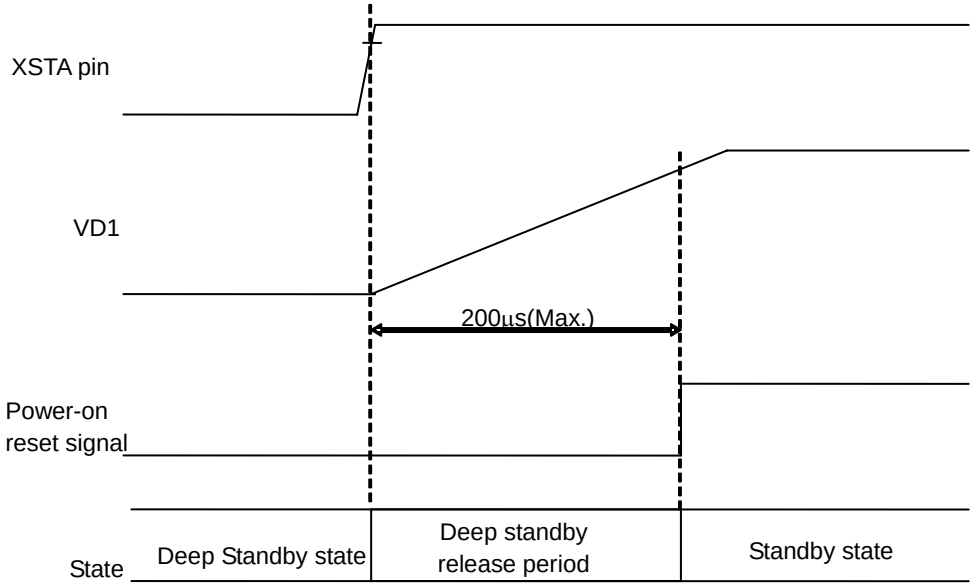

Figure 7.1.4 Deep standby state release

7.2 Command Interfaces

The device can select one from two command interfaces. The selection is done with the IFSEL pin connection. Refer to Table 7.2.

Table 7.2 Correspondence table of IFSEL pin and interface selection

IFSEL pin	Interface selection
Low level	I2C slave interface
High level	SPI slave interface

For descriptions of each command, refer to “8. Commands”.

7.2.1 I2C Slave Interface

This device has a built-in I2C slave interface module used for two-wire serial communication. This module is enabled when the IFSEL pin is low. This device operates as a slave device on the I2C bus and can communicate with the master device in compliance with I2C. The main functions and features of the I2C slave interface module are as follows.

- I2C bus slave device operation
- Supporting the standard mode (100kbps) and the fast mode (400kbps)
- 8-bit data length (MSB: first bit)
- 7-bit slave address (lower 2 bits: variable with pin setting)
- Detection of start, restart and stop condition

7.2.1.1 I2C Slave Interface Input / Output Pins

Table 7.2.1.1 shows the I2C slave interface pin list.

Table 7.2.1.1 I2C slave interface pin list

Pin	I/O	Descriptions	Number of pins
SCL	I	Clock input pin for the I2C slave interface module Inputs the SCL line state.	1
SDA	I/O	Data input / output pin for the I2C slave interface module Inputs serial data from the I2C bus. Outputs serial data to the I2C bus.	1

7.2.1.2 Slave Address Setting

The I2C slave interface module has a unique slave address to recognize each device. This module supports the 7-bit address mode (does not support the 10-bit address mode). Higher five bits of the 7-bit address are fixed to 0x0A. Lower two bits are set with connections of the I2C_AD1 pin and the I2C_AD0 / XSCS pin. Table 7.2.1.2 shows the 7-bit address list.

Table 7.2.1.2 7-bit address configuration

	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit
Slave address (7-bit)	Fixed to 0	Fixed to 1	Fixed to 0	Fixed to 1	Fixed to 0	I2C_AD1 pin	I2C_AD0 / XSCS pin

The lowest 2 bits of the slave address are 1 if the I2C_AD1 pin and the I2C_AD0 / XSCS pin are high and are 0 if those pins are low.

7.2.1.3 Transmitting / Receiving Data Control

Permission of Transmitting / Receiving Data

The startup of communication operations is allowed by detecting start conditions.

Start of Transmitting / Receiving Data

When the I2C slave interface module receives the slave address for this device from the master following the start condition, the module returns ACK (SDA pin = Low level output) to the master. And the module starts the receiving data operation (command issue / command parameter issue) or the transmitting data operation (command parameter output), according to the transfer direction bit (write / read selection bit) received concurrently with the address.

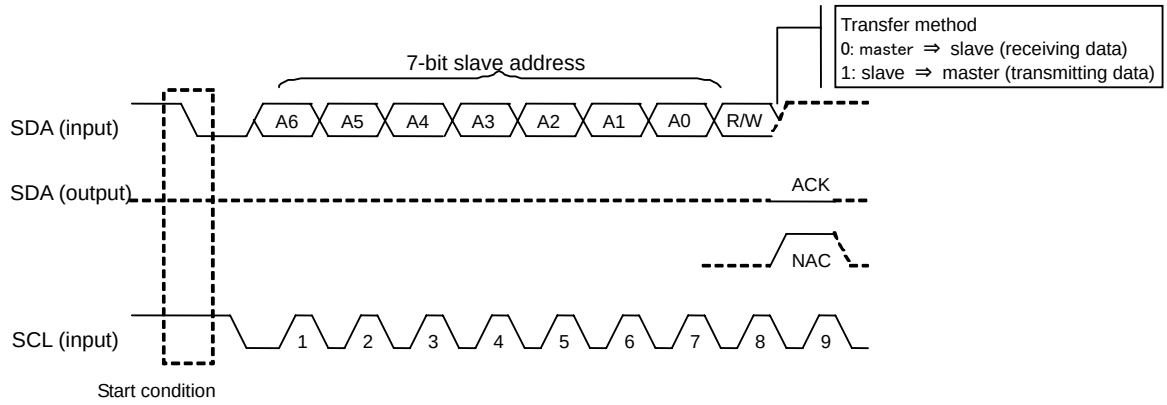

Figure 7.2.1.3.1 Receiving slave address and transfer direction bit

Termination of Transmitting / Receiving Data (Detection of Stop Condition)

When the master generates the stop condition, the data transfer terminates. The stop condition is generated with setting the SDA line to High level from Low level, while keeping the SCL line to High level.

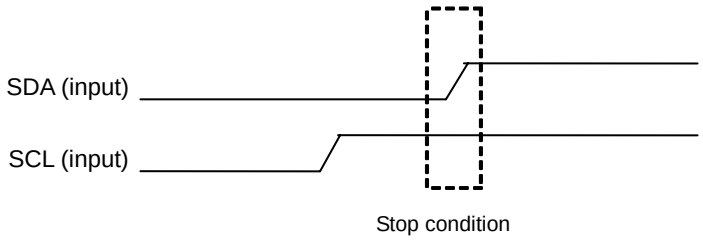

Figure 7.2.1.3.2 Stop condition

When the I2C slave interface module detects the stop condition, the module is initialized to wait for the next start condition.

Receiving Data Operation (Command Issue / Command Parameter Issue)

In the receiving data operation, a command is issued and command parameters are issued.

When the transfer direction bit (write / read selection bit) is 0, the I2C slave interface module starts the receiving operation. The receiving data is input from the SDA pin, synchronizing with the SCL input clock sent from the master. The module stores the 8-bit data (MSB: first bit) into the shift register, and returns ACK at the 9th bit.

The command is issued in the first 8-bit after the receiving data operation starts. Refer to Figure 7.2.1.3.3.

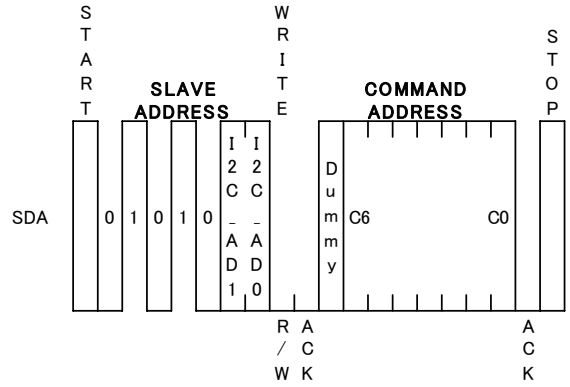

Figure 7.2.1.3.3 Command issue

For the command parameter issue, input the 8-bit data sequentially from the parameter 1 after the command is issued. Refer to Figure 7.2.1.3.4.

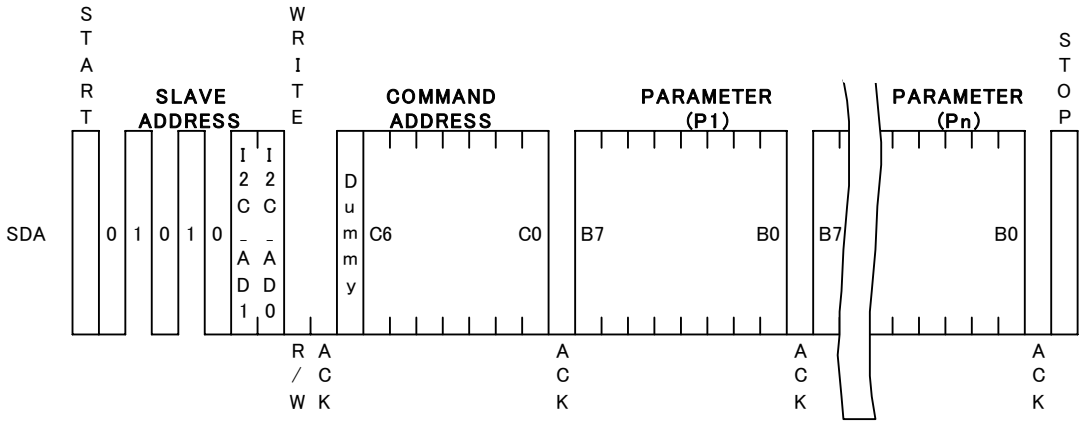

Figure 7.2.1.3.4 Command issue and command parameter issue

When issuing commands sequentially, generate the stop condition or the restart condition after one command / command parameter issue. After that, issue the next one. Refer to Figure 7.2.1.3.5.

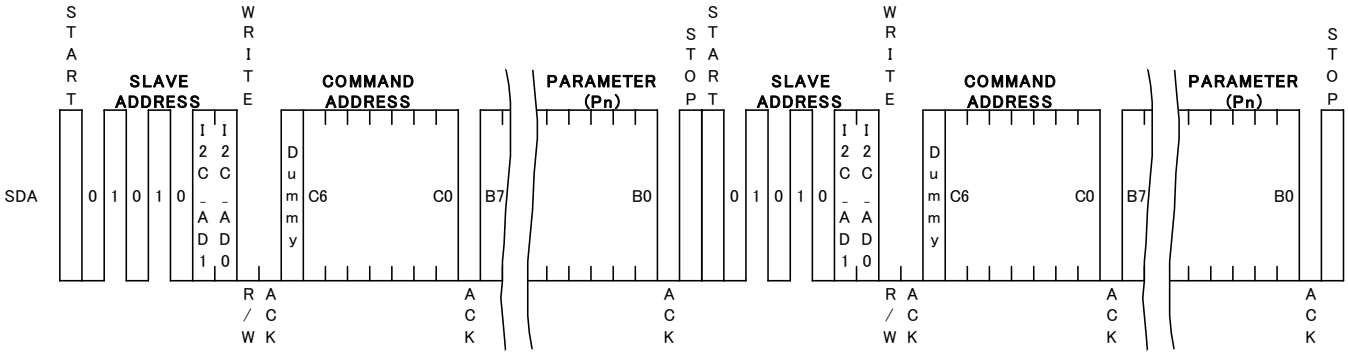

Figure 7.2.1.3.5 Sequential command issue

Transmitting Data Operation (Command Parameter Output)

Data transmission includes sending out the command parameters. Before the data is transmitted, the command address you want to send out to needs to be specified in the RDCOM command parameter B16-B10 (RDCOMAD[6:0]). For details about the RDCOM command, see Section 8.2.24 RDCOM: 0x30.

If the transmission direction bit (the write/read selection bit) is 1, the I2C slave interface module starts the transmission. The data is transmitted from the SDA pin and is synchronized with the SCL input clock from the master. 8-bit words (MSB first) are output starting from P1, and the device receives ACK or NAC from the master at the 9- bit clock cycle.

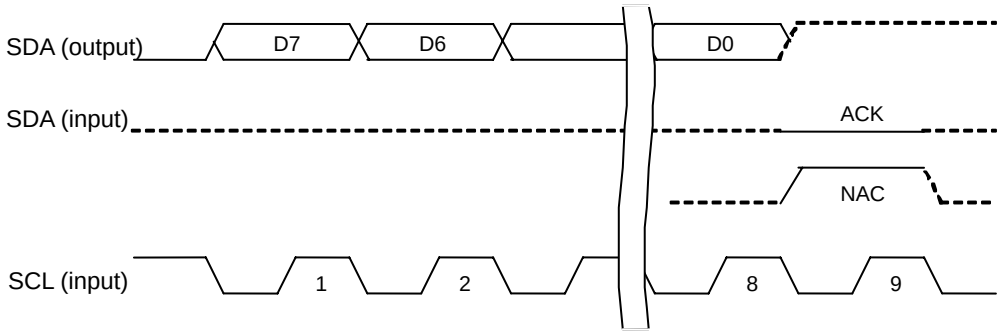

Figure 7.2.1.3.6 ACK and NAC in transmitting data

The ACK means that the master has received the data. It is also a transmission request for the data following to ACK. If the master has not received the data correctly or the master terminates the receiving data, NAC is returned. Refer to Figure 7.2.1.3.7.

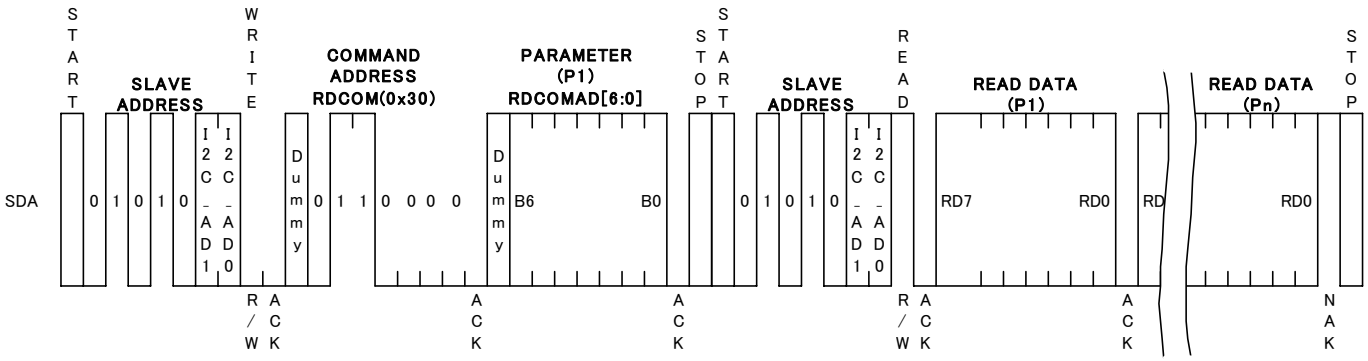

Figure 7.2.1.3.7 Command parameter transmission

7.2.2 SPI Slave Interface

This device has a built-in serial interface slave module (SPI). This module is enabled when the IFSEL pin is high. The main functions and features of the SPI slave module are as follows.

- Number of channel: 1 channel
- Supporting the slave mode, not supporting the master mode
- 8-bit data length (MSB: first bit)
- Built-in 1-byte receiving data buffer and 1-byte transmitting data buffer

7.2.2.1 SPI Slave Interface Input / Output Pins

Table 7.2.2.1 shows the SPI slave interface pin list.

Table 7.2.2.1 SPI slave interface pin list

Pin	I/O	Descriptions	Number of pins
SCL	I	Clock input pin for the SPI slave interface module	1
SDA	I	Data input pin for the SPI slave interface module Inputs serial data from the SPI bus.	1
SDO	O	Data output pin of the SPI slave interface module Outputs serial data to the SPI bus.	1
I2C_AD0 / XSCS	I	SPI slave selection (active Low) input pin When Low level is input to this pin, this SPI slave module is selected as a slave device.	1

7.2.2.2 SPI Clock Polarity and Phase

Figure 7.2.2.2 shows the SPI clock polarity and phase.

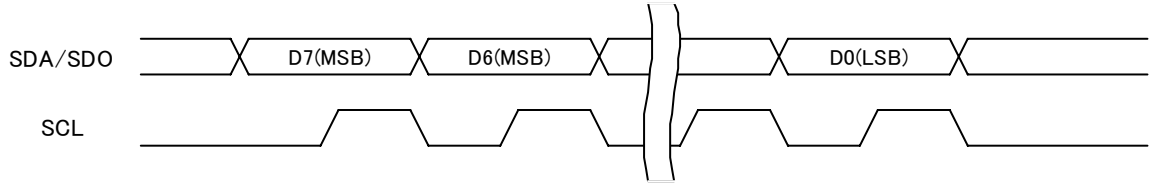

Figure 7.2.2.2 Clock and data transfer timing

7.2.2.3 Transmitting / Receiving Data

Permission of Transmitting / Receiving Data

The startup of communication operations is allowed by setting the I2C_AD0/XSCS terminal at a low level.

Start of Transmitting / Receiving Data

When the I2C_AD0 / XSCS pin is set to Low level and the SPI slave module receives the command address sent from the master, the module starts the receiving data operation (command parameter issue) or the transmitting data operation (command parameter output), according to the transfer direction bit (write / read selection bit) received concurrently with the command address.

Refer to Figure 7.2.2.3.1.

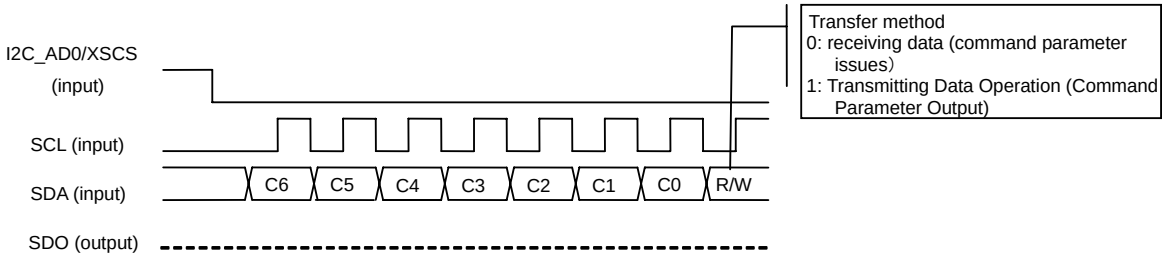

Figure 7.2.2.3.1 Receiving command address and transfer direction bit

Termination of Transmitting / Receiving Data

When the I2C_AD0 / XSCS pin is set to High level, the communication operation terminates and the SPI module is initialized.

Permission of Receiving Data

In the receiving data operation, command parameters are issued.

When the transfer direction bit (write / read selection bit) is 0, the SPI module starts the receiving operation. The receiving data is input from the SDA pin, synchronizing with the SCL input clock sent from the master. The module stores the 8-bit data (MSB: first bit) into the shift register.

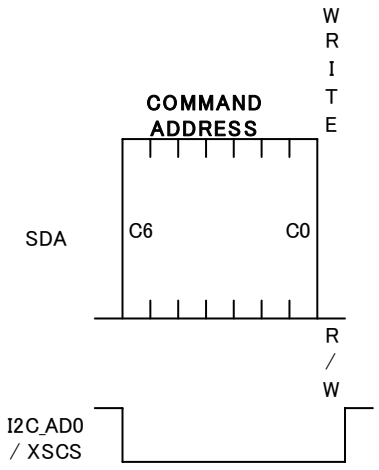

Figure 7.2.2.3.2 Command issue

When you issue command parameters, start the data reception process and enter the 8-bit parameters in succession starting from the parameter 1. See Figure 7.2.2.3.3.

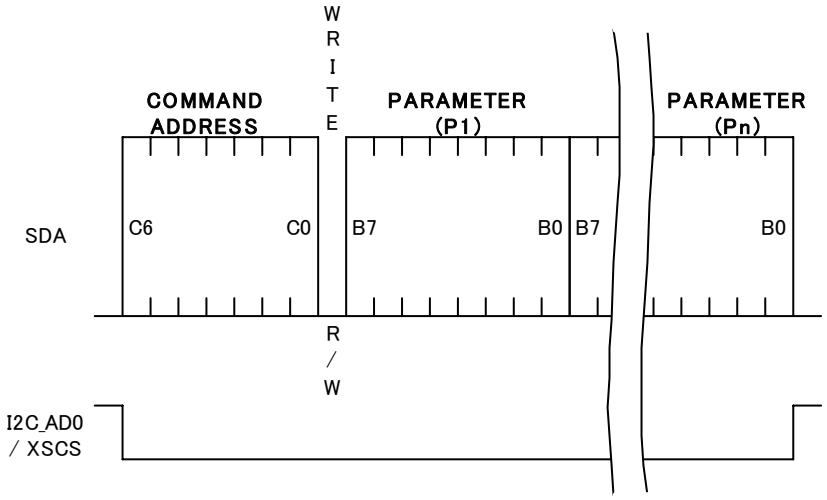

Figure 7.2.2.3.3 Command parameter issue

If you issue two commands back to back, after issuing the first command/command parameters is complete, set the I2C_AD0 / XSCS pin to high, and then issue the next command/command parameters. See Figure 7.2.2.3.4.

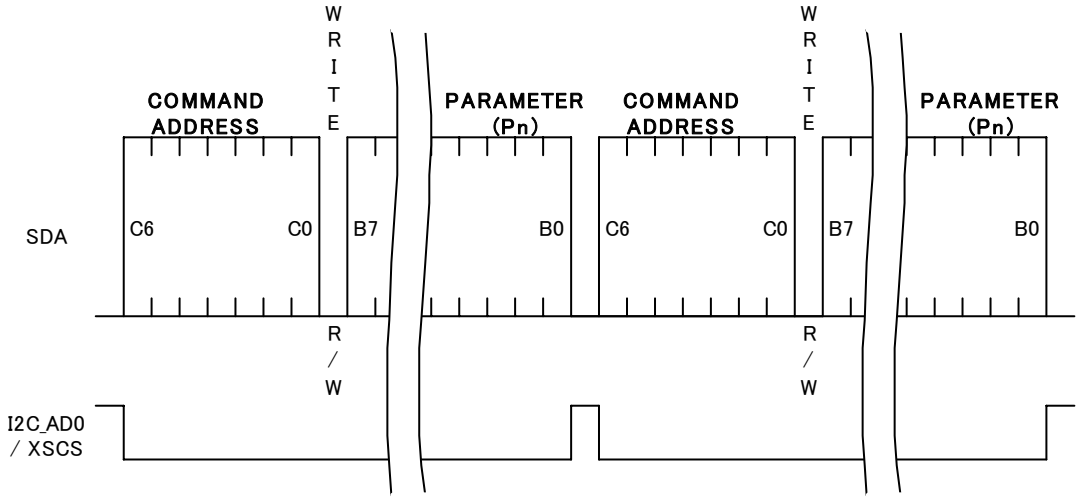

Figure 7.2.2.3.4 Sequential command issue

Transmitting Data (Command Parameter Output)

Data transmission includes sending out the command parameters. The command parameters of the command address that was issued when the data transmission/reception was started are transmitted.

When the transfer direction bit (write / read selection bit) is 1, the SPI slave interface module starts the transmission operation. The transmission data is output from the SDA pin, synchronizing with the SCL input clock sent from the master.The 8-bit data (MSB: first bit) is output from the parameter 1. Refer to Figure 7.2.2.3.5.

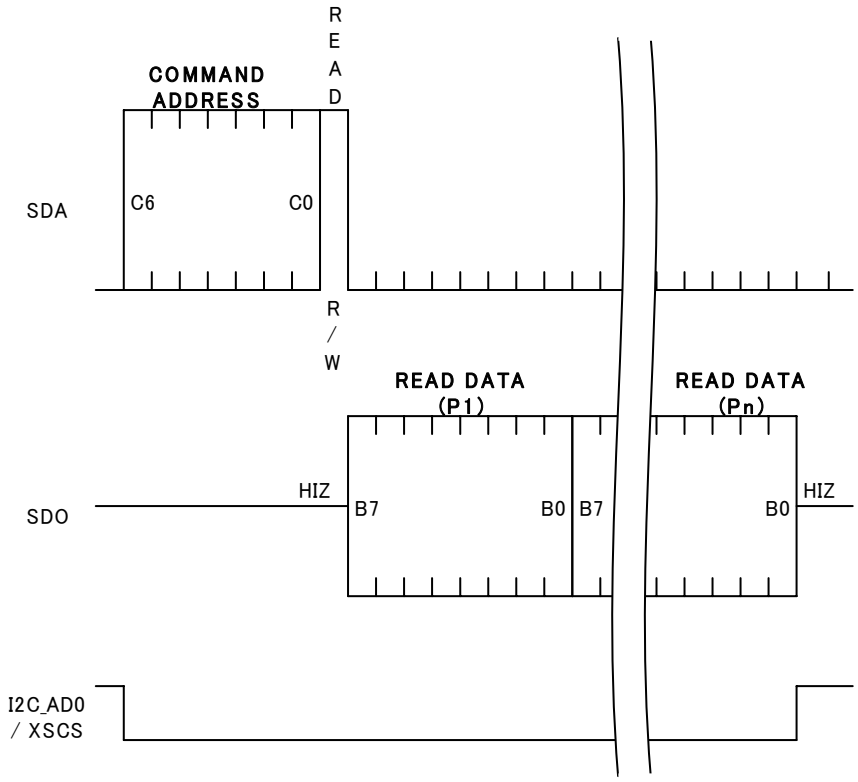

Figure 7.2.2.3.5 Command parameter transmission

7.3 Power Supplies

7.3.1 Power Supply Voltage (V_{DD})

The device operates with the power supply voltage supplied between V_{DD} to V_{SS}. Supply the voltage in the following range to V_{DD}, keeping the V_{SS} pin to the GND level.

- V_{DD} = 1.75V to 5.5V (V_{SS} = GND)

7.3.2 Power Supply for Flash Memory Programming (V_{PP})

This power voltage is used for erasing/reprogramming the built-in flash memory. When you erase/reprogram the flash memory, supply the following voltage to the V_{PP} pin where the V_{SS} is the GND level.

- V_{PP} = 7.0V(V_{SS} = GND)

Note: Make the V_{PP} pin to be open, in normal operation.

7.3.3 Internal Power Supply Circuit

The device integrates a circuit that generates the operation voltage for internal circuits.

Figure 7.3.3 shows the internal power supply circuit configuration.

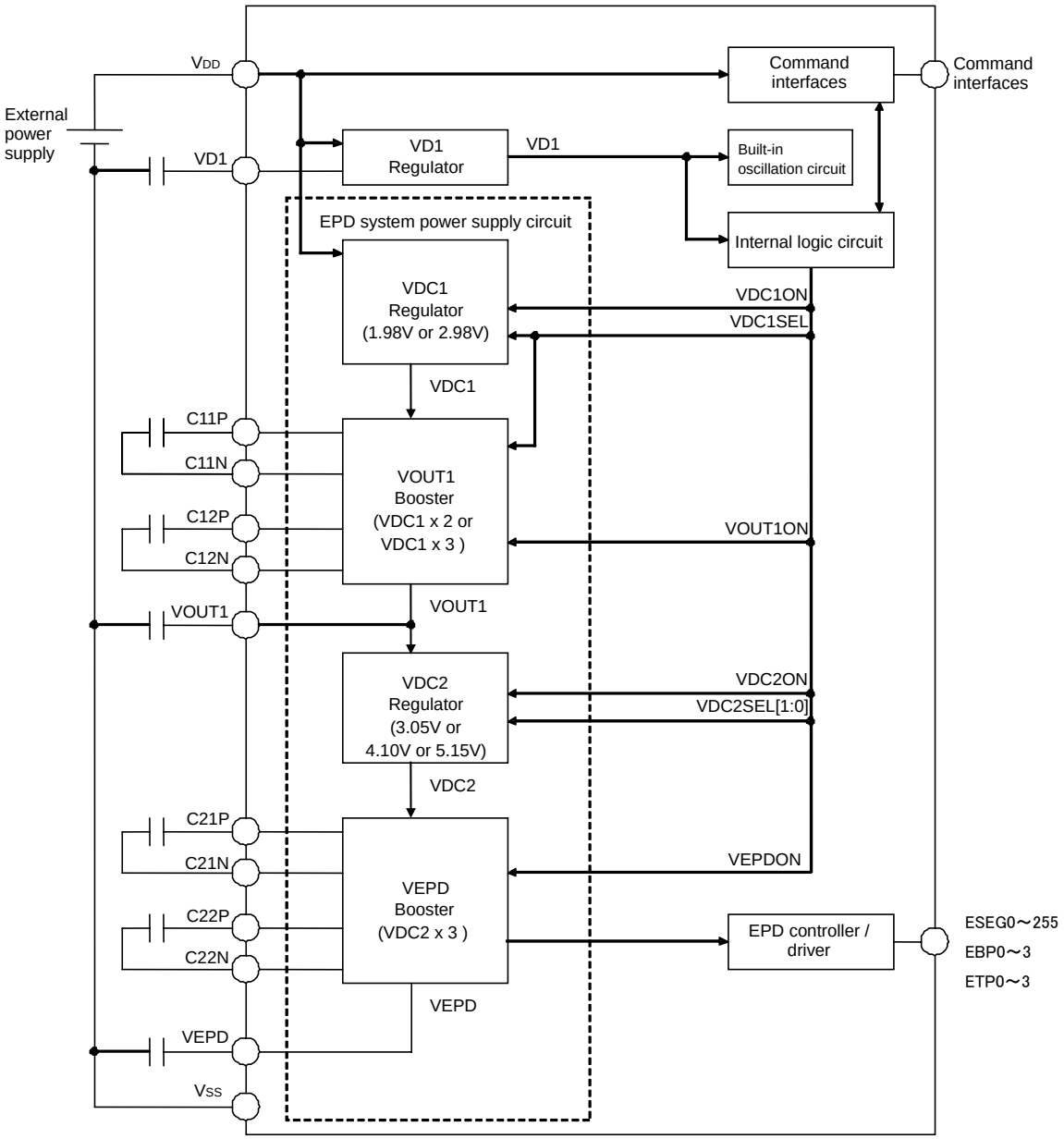

Figure 7.3.3 Internal power supply circuit configuration

The internal power supply circuit is composed of the VD1 Regulator and the EPD system power supply circuit.

7.3.3.1 VD1 Regulator

The VD1 Regulator generates the voltage required for the operation of the internal logic circuit, the built-in oscillation circuit, and the Flash memory. This power supply circuit operates when the XSTA pin is high.

7.3.3.2 EPD System Power Supply Circuit

The EPD system power supply circuit generates the EPD drive voltage VEPD. This voltage is transferred to the EPD drivers and used for generating the EPD drive waveforms.

The power supply circuits for the EPD system consist of the VDC1 Regulator, VOUT1 Booster, VDC2 Regulator, and VEPD Booster. It operates when the ATEPDWR 1 to 7 commands and the POWON command are issued. If you configure the POWCTL command parameter, you can perform voltage control and voltage

operation control on each power supply circuit.

VDC1 Regulator

The VDC1 Regulator generates the VOUT1 Booster reference voltage VDC1 from the power supply voltage VDD.

The VDC1 Regulator operation is selected with the POWCTL command parameter B10 (VDC1SEL), depending on the VDD value. For this functional descriptions, refer to Table 8.2.21.2 in "8.2.21 POWCTL Command: 0x24".

VOUT1 Booster

The VOUT1 Booster generates VOUT1, boosting VDC1 generated in the VDC1 Regulator to the double or triple level.

VOUT1 Booster uses the B10(VDC1SEL) parameter of the POWCTL command to switch the boost level between two and three times.

For information about this function, refer to Table 8.2.21.2 in Section 8.2.21, "POWCTL Command: 0x24".

VDC2 Regulator

The VDC2 Regulator generates the VDC2, VEPD Booster reference voltage, from the VOUT1 voltage.

According to the voltage you want the VEPD Booster to generate, you can configure the VDC2 Regulator by setting the POWCTL command parameter B15-B14 (VDC2SEL[1:0]). For information about this function, see Section 8.2.21 POWCTL command: 0x24 Table 8.2.21.1.

VEPD Booster

The VEPD Booster generates the VEPD, which is three times the voltage of the VDC2 generated by the VDC2 Regulator. The generated VEPD is supplied to the EPD driver and the EPD driving waveform is generated. For information about this function, see Section 8.2.21 POWCTL command: 0x24 Table 8.2.21.1.

VOUT1 Booster / VEPD Booster Clock

The VOUT1 Booster and the VEPD Booster use a clock for the boost operation. The boost clock is supplied at the same time as the boost operation start of both Boosters. The boost clocks are divided from the clock generated with the built-in oscillation circuit.

VOUT1 Booster Boost Clock Frequency Selection

The boost clock frequency of the VOUT1 Booster can be set separately under the following conditions.

- During the power supply startup period (refer to Section 7.7, "Status Transition")
- During operations other than the power supply startup period (refer to Section 7.7, "Status Transition")

The step-up clock frequency during the power warm-up period is controlled by the setting of the POWCTL command parameter B27-B26 (VOUT1SUFREQ[1:0]). For information about this function, see Section 8.2.21 POWCTL command: 0x24 Table 8.2.21.3.

The step-up clock frequency when the power circuit is active except during the power warm-up period is controlled by the setting of the POWCTL command parameter B25-B24 (VOUT1FREQ[1:0]). For information about this function, see Section 8.2.21 POWCTL command: 0x24 Table 8.2.21.4.

VEPD Booster Boost Clock Frequency Selection

The boost clock frequency of the VEPD Booster can be set separately under the following conditions.

- During the power supply startup period (refer to Section 7.7, “Status Transition”)
- During operations other than the power supply startup period (refer to Section 7.7, “Status Transition”)

The step-up clock frequency during the power warm-up period is controlled by the setting of the POWCTL command parameter B23-B22 (VEPDSUFREQ[1:0]). For information about this function, see Section 8.2.21 POWCTL command: 0x24 Table 8.2.21.5.

The step-up clock frequency when the power circuit is active except during the power warm-up period is controlled by the setting of the POWCTL command parameter B21-B20 (VEPDFREQ[1:0]). For information about this function, see Section 8.2.21 POWCTL command: 0x24 Table 8.2.21.6.

7.4 Temperature Detection Circuit

7.4.1 Temperature Detection Circuit Outline

This device has a built-in temperature detection circuit. The main functions of the temperature detection circuit are as follows.

- Temperature detection range: -10 °C to 60 °C
- Temperature detection time: 3.5ms (Max.)
- Temperature detection accuracy: ±5 °C
- Temperature detection operation: activated with TEMPSENSON command issue
- Offset function to temperature detection result
- Read function to temperature detection result (digital output value)
- Automatic temperature detection function at display updates

7.4.2 Temperature Detection Operation

When the temperature detection circuit issues the TEMPSENSON command, the circuit operates and starts the temperature detection operation. The temperature detection operation time takes 3.5ms (Max.).

For the TEMPSENSON command details, refer to “8.2.20 TEMPSENSON: 0x23”.

The temperature detection result of 7-bit digital value is stored in the register.

7.4.3 Digital Value of Temperature Detection Result

After the temperature detection, the temperature detection result is stored in the register as a digital value. Table 7.4.3 shows the correspondence table of the digital value and the temperature.

Table 7.4.3 Correspondence table of temperature and temperature detection result

Tempe-rature (°C)	Temperature detection result AD value (DEC)	Tempe-rature (°C)	Temperature detection result AD value (DEC)	Tempe-rature (°C)	Temperature detection result AD value (DEC)	Tempe-rature (°C)	Temperature detection result AD value (DEC)
Less-10	0 to 7	7.68	36	25.95	65	44.22	94
-9.96	8	8.31	37	26.58	66	44.85	95
-9.33	9	8.94	38	27.21	67	45.48	96
-8.7	10	9.57	39	27.84	68	46.11	97
-8.07	11	10.2	40	28.47	69	46.74	98
-7.44	12	10.83	41	29.1	70	47.37	99
-6.81	13	11.46	42	29.73	71	48	100
-6.18	14	12.09	43	30.36	72	48.63	101
-5.55	15	12.72	44	30.99	73	49.26	102
-4.92	16	13.35	45	31.62	74	49.89	103
-4.29	17	13.98	46	32.25	75	50.52	104
-3.66	18	14.61	47	32.88	76	51.15	105
-3.03	19	15.24	48	33.51	77	51.78	106
-2.4	20	15.87	49	34.14	78	52.41	107
-1.77	21	16.5	50	34.77	79	53.04	108
-1.14	22	17.13	51	35.4	80	53.67	109
-0.51	23	17.76	52	36.03	81	54.3	110
0.12	24	18.39	53	36.66	82	54.93	111
0.75	25	19.02	54	37.29	83	55.56	112
1.38	26	19.65	55	37.92	84	56.19	113
2.01	27	20.28	56	38.55	85	56.82	114
2.64	28	20.91	57	39.18	86	57.45	115
3.27	29	21.54	58	39.81	87	58.08	116
3.9	30	22.17	59	40.44	88	58.71	117
4.53	31	22.8	60	41.07	89	59.34	118
5.16	32	23.43	61	41.7	90	59.97	119
5.79	33	24.06	62	42.33	91	60 over	120 to 127
6.42	34	24.69	63	42.96	92		
7.05	35	25.32	64	43.59	93		

7.4.4 Offset to Temperature Detection Result

This function is for customer environments where the temperature detection result is not suitable. The function can select any offset value from ±0/2/4/6 to the temperature detection result of digital value. The offset value is selected with setting of the POWCTL command parameter B72 - B70 (TEMPOFFSET [2:0]). For details of this function, refer to Table 8.2.21.8 in “8.2.21 POWXTL: 0x24”.

7.4.5 Temperature Detection Result Reading

The temperature detection result is read with the command interface.

The temperature detection result is 7-bit data, and the command interface outputs 8-bit data. As a result, the temperature detection result is output in lower 7-bit of 8-bit data (MSB: first bit). Refer to “8.2.20 TEMPSENSON: 0x23”, for details.

7.4.6 Automatic Temperature Detection Function

For details of the automatic temperature detection function, refer to the B30 ATTEMPON in “8.2.21 POWCTL: 0x24”.

7.5 Flash Memory

7.5.1 Flash Memory Map

Figure 7.5.1 shows the memory map of this device.

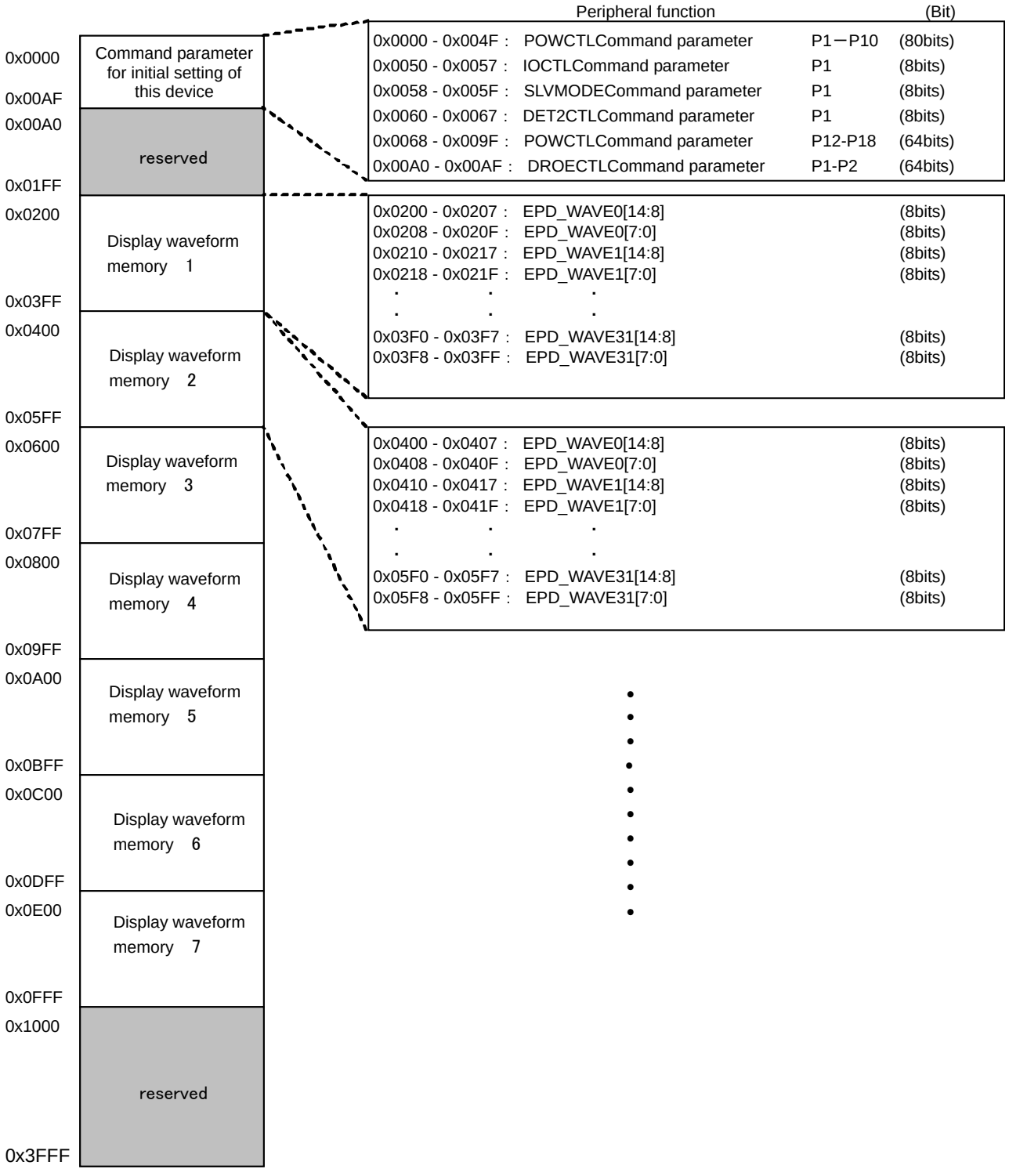

Figure 7.5.1 Flash Memory Map

7.5.2 Flash Memory Initial Setting Data

The device can store the following initial setting data in the Flash memory.

- POWCTL command parameter : P1 to P10,P12 to P18 (refer to “8.2.21 POWCTL: 0x24”)
- IOCTL command parameter : P1 (refer to “8.2.22 IOCTL: 0x25”)
- SLVMODE command parameter : P1 (refer to “8.2.23 SLVMODE: 0x26”)
- DET2CTL command parameter : P1 (refer to “8.2.26 DET2CTL: 0x32”)
- DROECTL command parameter : P1 to P2 (refer to “8.2.27 DROECTL: 0x33”)

By setting the B10 (FMDISB) parameter of the FMDISB command to “0”, the above command parameter is set to the default settings data of the flash memory that is automatically read before the VOUT1 Booster and VEPD Booster are started. For details on the FMDISB command, refer to Section 8.2.11, “FMDISB: 0x0B”.

If the POWCTL / IOCTL / SLVMODE / DET2CTL / DROECTL command parameter is issued with the command interface, the Flash memory initial setting data is given to priority.

7.5.3 Flash Memory Display Waveform Data

The device can store seven types (max.) display waveforms in the Flash memory.

With setting the FMDISB command B10 (FMDISB) to 0 the display waveform data to be used is read automatically. At this time, the WFSET command (refer to “8.2.10 WFSET: 0x0A”) becomes invalid.

The display memory 1 to 7 store 32 (max.) timing sets (timing set 0 to timing set 31). A timing set is composed of 15-bit. Refer to “7.6.6 Display Waveform Data”, for details of the display waveform data.

7.5.4 Flash Memory Programming

You can erase/reprogram the built-in Flash memory through the EPD microcontroller from Seiko Epson using the debug tool “ICDmini”. For details about how to erase/reprogram the built-in Flash memory, contact our representatives.

When you use the Flash memory, make sure that the following pins can be controlled from the outside.

- XMFS pin
- MFC pin
- MFDI pin
- MFDO pin
- OS pin
- VPP pin

7.5.5 Flash Memory Functions of Data Stored in Each Bit Address

Figure 7.5.1 shows the outline of the Flash memory map. This section describes the relations between the data stored in each bit address of the Flash memory and the initial setting command parameter / display waveform data 1 to 7.

7.5.5.1 Initial Setting Command Parameter

Table 7.5.5.1 shows the correspondence table of each bit address of the Flash memory and the initial setting data.

Table 7.5.5.1 Correspondence table of each bit address and initial setting data

MF_A[13:2]	MF_A[1:0]				Initial setting command	Parameter
	0x3	0x2	0x1	0x0		
0x000	—	—	B15	B14	POWCTL	P1
0x001	—	—	—	B10		
0x002	0(Fix)	0(Fix)	B25	B24		P2
0x003	0(Fix)	0(Fix)	B21	B20		
0x004	—	—	—	0(Fix)		P3
0x005	—	—	—	B30		
0x006	B47	B46	B45	B44		P4
0x007	B43	B42	B41	B40		
0x008	B57	B56	B55	B54		P5
0x009	B53	B52	B51	B50		
0x00A	B67	B66	B65	B64		P6
0x00B	B63	B62	B61	B60		
0x00C	—	—	—	—		P7
0x00D	—	B72	B71	B70		
0x00E	0(Fix)	0(Fix)	0(Fix)	0(Fix)		P8
0x00F	1(Fix)	1(Fix)	1(Fix)	1(Fix)		
0x010	0(Fix)	0(Fix)	1(Fix)	1(Fix)		P9
0x011	0(Fix)	0(Fix)	0(Fix)	0(Fix)		
0x012	0(Fix)	0(Fix)	0(Fix)	0(Fix)		P10
0x013	0(Fix)	1(Fix)	0(Fix)	0(Fix)		
0x014	—	—	—	—	IOCTL	P1
0x015	—	—	—	B10		
0x016	—	—	—	—	SLVMODE	P1
0x017	—	—	—	B10		
0x018	—	—	0(Fix)	—	DET2CTL	P1
0x019	—	B12	B11	1(Fix)		
0x01A	0(Fix)	0(Fix)	1(Fix)	0(Fix)	POWCTL	P12
0x01B	1(Fix)	1(Fix)	0(Fix)	1(Fix)		
0x01C	0(Fix)	0(Fix)	0(Fix)	0(Fix)		P13
0x01D	0(Fix)	0(Fix)	0(Fix)	1(Fix)		
0x01E	0(Fix)	0(Fix)	0(Fix)	0(Fix)		P14
0x01F	1(Fix)	0(Fix)	0(Fix)	0(Fix)		
0x020	0(Fix)	0(Fix)	0(Fix)	1(Fix)		P15
0x021	0(Fix)	0(Fix)	0(Fix)	0(Fix)		
0x022	0(Fix)	0(Fix)	0(Fix)	1(Fix)		P16
0x023	1(Fix)	0(Fix)	0(Fix)	0(Fix)		
0x024	1(Fix)	0(Fix)	1(Fix)	0(Fix)		P17
0x025	0(Fix)	0(Fix)	0(Fix)	1(Fix)		
0x026	0(Fix)	0(Fix)	0(Fix)	1(Fix)		P18
0x027	1(Fix)	1(Fix)	1(Fix)	1(Fix)		
0x028	B17	B16	B15	B14	DROECTL	P1
0x029	B13	B12	B11	B10		
0x02A	—	—	—	—		P2
0x02B	—	—	B21	B20		

For the initial setting command parameter of each bit, refer to the followings.

- POWCTL command parameter : P1 to P10, P12 to P18 (refer to “8.2.21 POWCTL: 0x24”)
- IOCTL command parameter : P1 (refer to “8.2.22 IOCTL: 0x25”)
- SLVMODE command parameter : P1 (refer to “8.2.23 SLVMODE: 0x26”)
- DET2CTL command parameter : P1 (refer to “8.2.26 DET2CTL: 0x32”)
- DROECTL command parameter : P1 to P2 (refer to “8.2.27 DROECTL: 0x33”)

7.5.5.2 Display Waveform Data

The display waveform data is stored up to seven types in the built-in Flash memory.

Table 7.5.5.2.1 shows the correspondence table of each bit address of the Flash memory and the display data 1 timing set.

Table 7.5.5.2.1 Correspondence table of each bit address and the display data 1 timing set

MF_A[13:2]	MF_A[1:0]				Timing set
	0x3	0x2	0x1	0x0	
0x080	EOW	—	HIZ	TP	0
0x081	BB	BW	WB	WW	
0x082	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x083	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x084	EOW	—	HIZ	TP	1
0x085	BB	BW	WB	WW	
0x086	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x087	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
• •	• •	• •	• •	• •	• •
0x0F8	EOW	—	HIZ	TP	30
0x0F9	BB	BW	WB	WW	
0x0FA	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x0FB	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x0FC	EOW	—	HIZ	TP	31
0x0FD	BB	BW	WB	WW	
0x0FE	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x0FF	INTV[3]	INTV[2]	INTV[1]	INTV[0]	

For the display waveform data descriptions, refer to “7.6.6 Display Waveform Memory”.

Table 7.5.5.2.2 shows the correspondence table of each bit address of the Flash memory and the display data 2 timing set.

Table 7.5.5.2.2 Correspondence table of each bit address and the display data 2 timing set

MF_A[13:2]	MF_A[1:0]				Timing set
	0x3	0x2	0x1	0x0	
0x100	EOW	—	HIZ	TP	0
0x101	BB	BW	WB	WW	
0x102	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x103	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x104	EOW	—	HIZ	TP	1
0x105	BB	BW	WB	WW	
0x106	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x107	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
• •	• •	• •	• •	• •	• •
0x178	EOW	—	HIZ	TP	30
0x179	BB	BW	WB	WW	
0x17A	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x17B	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x17C	EOW	—	HIZ	TP	31
0x17D	BB	BW	WB	WW	
0x17E	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x17F	INTV[3]	INTV[2]	INTV[1]	INTV[0]	

For the display waveform data descriptions, refer to “7.6.6 Display Waveform Memory”.

Table 7.5.5.2.3 shows the correspondence table of each bit address of the Flash memory and the display data 3 timing set.

Table 7.5.5.2.3 Correspondence table of each bit address and the display data 3 timing set

MF_A[13:2]	MF_A[1:0]				Timing set
	0x3	0x2	0x1	0x0	
0x180	EOW	—	HIZ	TP	0
0x181	BB	BW	WB	WW	
0x182	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x183	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x184	EOW	—	HIZ	TP	1
0x185	BB	BW	WB	WW	
0x186	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x187	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
• •	• •	• •	• •	• •	• •
0x1F8	EOW	—	HIZ	TP	30
0x1F9	BB	BW	WB	WW	
0x1FA	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x1FB	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x1FC	EOW	—	HIZ	TP	31
0x1FD	BB	BW	WB	WW	
0x1FE	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x1FF	INTV[3]	INTV[2]	INTV[1]	INTV[0]	

For the display waveform data descriptions, refer to “7.6.6 Display Waveform Memory”.

Table 7.5.5.2.4 shows the correspondence table of each bit address of the Flash memory and the display data 4 timing set.

Table 7.5.5.2.4 Correspondence table of each bit address and the display data 4 timing set

MF_A[13:2]	MF_A[1:0]				Timing set
	0x3	0x2	0x1	0x0	
0x200	EOW	—	HIZ	TP	0
0x201	BB	BW	WB	WW	
0x202	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x203	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x204	EOW	—	HIZ	TP	1
0x205	BB	BW	WB	WW	
0x206	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x207	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
• •	• •	• •	• •	• •	• •
0x278	EOW	—	HIZ	TP	30
0x279	BB	BW	WB	WW	
0x27A	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x27B	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x27C	EOW	—	HIZ	TP	31
0x27D	BB	BW	WB	WW	
0x27E	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x27F	INTV[3]	INTV[2]	INTV[1]	INTV[0]	

For the display waveform data descriptions, refer to “7.6.6 Display Waveform Memory”.

Table 7.5.5.2.5 shows the correspondence table of each bit address of the Flash memory and the display data 5 timing set.

Table 7.5.5.2.5 Correspondence table of each bit address and the display data 5 timing set

MF_A[13:2]	MF_A[1:0]				Timing set
	0x3	0x2	0x1	0x0	
0x280	EOW	—	HIZ	TP	0
0x281	BB	BW	WB	WW	
0x282	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x283	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x284	EOW	—	HIZ	TP	1
0x285	BB	BW	WB	WW	
0x286	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x287	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
• •	• •	• •	• •	• •	• •
0x2F8	EOW	—	HIZ	TP	30
0x2F9	BB	BW	WB	WW	
0x2FA	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x2FB	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x2FC	EOW	—	HIZ	TP	31
0x2FD	BB	BW	WB	WW	
0x2FE	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x2FF	INTV[3]	INTV[2]	INTV[1]	INTV[0]	

For the display waveform data descriptions, refer to “7.6.6 Display Waveform Memory”.

Table 7.5.5.2.6 shows the correspondence table of each bit address of the Flash memory and the display data 6 timing set.

Table 7.5.5.2.6 Correspondence table of each bit address and the display data 6 timing set

MF_A[13:2]	MF_A[1:0]				Timing set
	0x3	0x2	0x1	0x0	
0x300	EOW	—	HIZ	TP	0
0x301	BB	BW	WB	WW	
0x302	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x303	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x304	EOW	—	HIZ	TP	1
0x305	BB	BW	WB	WW	
0x306	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x307	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
• •	• •	• •	• •	• •	• •
0x378	EOW	—	HIZ	TP	30
0x379	BB	BW	WB	WW	
0x37A	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x37B	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x37C	EOW	—	HIZ	TP	31
0x37D	BB	BW	WB	WW	
0x37E	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x37F	INTV[3]	INTV[2]	INTV[1]	INTV[0]	

For the display waveform data descriptions, refer to “7.6.6 Display Waveform Memory”.

Table 7.5.5.2.7 shows the correspondence table of each bit address of the Flash memory and the display data 7 timing set.

Table 7.5.5.2.7 Correspondence table of each bit address and the display data 7 timing set

MF_A[13:2]	MF_A[1:0]				Timing set
	0x3	0x2	0x1	0x0	
0x380	EOW	—	HIZ	TP	0
0x381	BB	BW	WB	WW	
0x382	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x383	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x384	EOW	—	HIZ	TP	1
0x385	BB	BW	WB	WW	
0x386	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x387	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
• •	• •	• •	• •	• •	• •
0x3F8	EOW	—	HIZ	TP	30
0x3F9	BB	BW	WB	WW	
0x3FA	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x3FB	INTV[3]	INTV[2]	INTV[1]	INTV[0]	
0x3FC	EOW	—	HIZ	TP	31
0x3FD	BB	BW	WB	WW	
0x3FE	INTV[7]	INTV[6]	INTV[5]	INTV[4]	
0x3FF	INTV[3]	INTV[2]	INTV[1]	INTV[0]	

For the display waveform data descriptions, refer to “7.6.6 Display Waveform Memory”.

7.5.5.3 Flash Memory Unused Memory Address

Data (either of 0 / 1) in unused addresses of the Flash memory shown in Figure 7.5.1 do not affect the operations.

7.6 EPD Controller / Driver

7.6.1 EPD Module Outline

The device integrates an EPD controller / driver (EPD) module that achieves the EPD display function.
Major functions are as follows.

- Number of driver outputs: 256 segments +4 back plane +4 top plane
- EPD drive voltage: two values of VEPD and Vss
- Built-in EPD display waveform memory
- Reverse, all white and all black display functions
- Synchronization for EPD display updates is available with the trigger signal and clock generated in the EPD_MCU, for the EPD drive pin expansion for the Seiko Epson EPD_MCU.
- Multi-chip use is available with the SEIKO EPSON EPD drivers.

7.6.2 EPD Module Input / Output Pins

Table 7.6.2 shows the EPD pin list.

Table 7.6.2 EPD module pin list

Pin	I/O	Descriptions	Number of pins
ESEG0 to ESEG255	O	EPD segment output pin Outputs the segment drive waveform.	256
ETP0 to ETP3	O	EPD top plane output pin	4
EBP0 to EBP 3	O	EPD back plane output pin	4
EPDTRG	I/O	EPD trigger input / output pin When the device is used for the EPD_MCU driver expansion or as a slave device in multi-chip use: input pin When the device is used alone or as a master device in multi-chip use: output pin	1
EPDCLK	I/O	EPD clock input / output pin When the device is used for the EPD_MCU driver expansion or as a slave device in multi-chip use: input pin When the device is used alone or as a master device in multi-chip use: output pin	1
SLVSEL	I	Master device / slave device switching pin When the device is used for the EPD_MCU driver expansion or as a slave device in multi-chip use: High level When the device is used alone or as a master device in multi-chip use: Low level	1

By setting the B17-B10(ESEGOENCTL[7:0]) parameter of the DROECTL command, it is possible to select whether to use ESEG0 to ESEG255 in 32 terminal units. For details on this function, refer to Section 8.2.27, “DROECTL: 0x33”.

By setting the B21-B20(ETBPOENCTL[1:0]) parameter of the DROECTL command, it is possible to select whether to use ETP0 to ETP3/EBP0 to EBP3 in 2 terminal units. For details on this function, refer to Section 8.2.27, “DROECTL: 0x33”.

7.6.3 Power Supply for EPD Drivers

The VEPD, power voltage for the EPD driver, is generated by the built-in power supply circuits for the EPD system. This voltage does not need to be supplied from the outside. For details about the EPD power supply circuits, see 7.3 Power Supply Circuit.

When multiple chips are used, a slave device can use the VEPD voltage generated by the master device supplied to the VEPD pin of the slave device by setting the SLVMODE command parameter B10 (SLVMODE) to 0. For details about this function, see Section 8.2.23 SLVMODE: 0x26. If you use this function, supply the VOUT1 voltage generated by the master devise to the VOUT1 pin of the slave device

7.6.4 EPD Clock

The EPD module of the device is controlled with the EPD clock (base clock for the drive waveform generation).

When it is used as a master device (SLVSEL pin = Low level), the internal EPDCLK generated internally is used as the EPD clock. The followings show the internal EPDCLK cycle and frequency.

- Cycle: 4.096ms (Typ.)
- Frequency: 244.14Hz (Typ.)

These cycle and frequency are not variable.

The internal EPDTRG is output from the EPDCLK pin, with setting the IOCTL command parameter B10 (EPDTRGSIG) to 1. For details of this function, refer to “8.2.22 IOCTL: 0x25”. In multi-chip use, make sure to connect the master device EPDCLK pin to the slave device EPDCLK pin.

When it is used as a slave device (SLVSEL pin = High level), the clock supplied externally (external EPDCLK) is used as the EPD clock. The limitations of cycle and frequency of the clock that can be supplied to the EPDCLK pin are shown below.

- Cycle: $\leq$ 31.25µs
- Frequency: $\geq$ 32KHz

7.6.5 EPD Controller

When a trigger for EPD display updates is applied, the EPD controller outputs the drive waveforms programmed in the display waveform memory. For the display waveform setting, refer to “7.6.6”.

7.6.6 Display Waveform Memory

The display waveform memory is used to store the drive waveform setting generated with EPD controller.

In the display waveform memory, up to 32 timing sets are stored (timing set 0 to timing set 31). Each set is composed of 15-bit. The timing set 0 stores the state and the period that are output first after a display update trigger is applied. Following this, each waveform change state is stored sequentially as the timing set 1 to n (Max.31).

Table 7.6.6.1 shows one timing set configuration.

Table 7.6.6.1 Timing set configuration

Bit name	Contents
EOW(End Of Wave)	The bit defines the waveform end point. The waveform generation terminates with a timing set setting EOW to 1. And the output keeps high impedance to the next display update trigger. During the waveform generation, all timing sets are necessary to set EOW to 0.
HIZ(High Impedance)	The bit sets segment pins and the back plane pin to high impedance. When the bit is set to 1, segment outputs and the back plane output keeps high impedance in the period of that timing set (the assignment of BB / BW / WB / WW is invalid). When set to 0, these outputs keep the level assigned with BB / BW / WB / WW.
TP(Top Plane)	The bit defines the top plane pin output waveform. The top plane output keeps VEPD level with setting to 1, and Vss level with setting to 0, in the period of that timing set.
BB(Black to Black)	The bit defines output waveforms for segments pins and the back plane pin, when the display keeps black to black at display updates. These outputs keep VEPD level with setting to 1, and Vss level with setting to 0, in the period of that timing set.
BW(Black to White)	The bit defines output waveforms for segment pins and the back plane pin, when display changes from black to white at display updates. These outputs keep VEPD level with setting to 1, and Vss level with setting to 0, in the period of that timing set.
WB(White to Black)	The bit defines output waveforms for segment pins and the back plane pin, when display changes from white to black at display updates. These outputs keep VEPD level with setting to 1, and Vss level with setting to 0, in the period of that timing set.
WW(White to White)	The bit defines output waveforms for segment pins and the back plane pin, when display changes from white to white at display updates. These outputs keep VEPD level with setting to 1, and Vss level with setting to 0, in the period of that timing set.
INTV[7:0](Interval)	The bit defines the timing set period with the number of EPDCLK clocks. Time (s) = (INTV [7:0] +1) / EPDCLK frequency

For the display waveform memory, up to seven types (max.) are stored in the register, which stores the WFSET command parameter P1 - P64 (refer to “8.2.10 WFSET: 0x0A”), and the Flash memory.

The display waveform data is set in the EPD_WAVE0 to EPD_WAVE31 registers prepared for each timing set. Each register is composed of bits with the above name.

The correspondence table of the timing set setting contents and the generated waveform is shown below, for a simple example.

Table 7.6.6.2 Timing set setting example

Timing set No. (register)	EOW	HIZ	TP	BB	BW	WB	WW	INTV[7:0]
0(EPD_WAVE0)	0	0	0	0	0	0	0	0x01
1(EPD_WAVE1)	0	0	1	0	1	0	1	0x02
2(EPD_WAVE2)	0	0	0	0	0	1	1	0x00
3(EPD_WAVE3)	0	1	1	*	*	*	*	0x01
4(EPD_WAVE4)	1	0	0	0	0	0	0	0x03

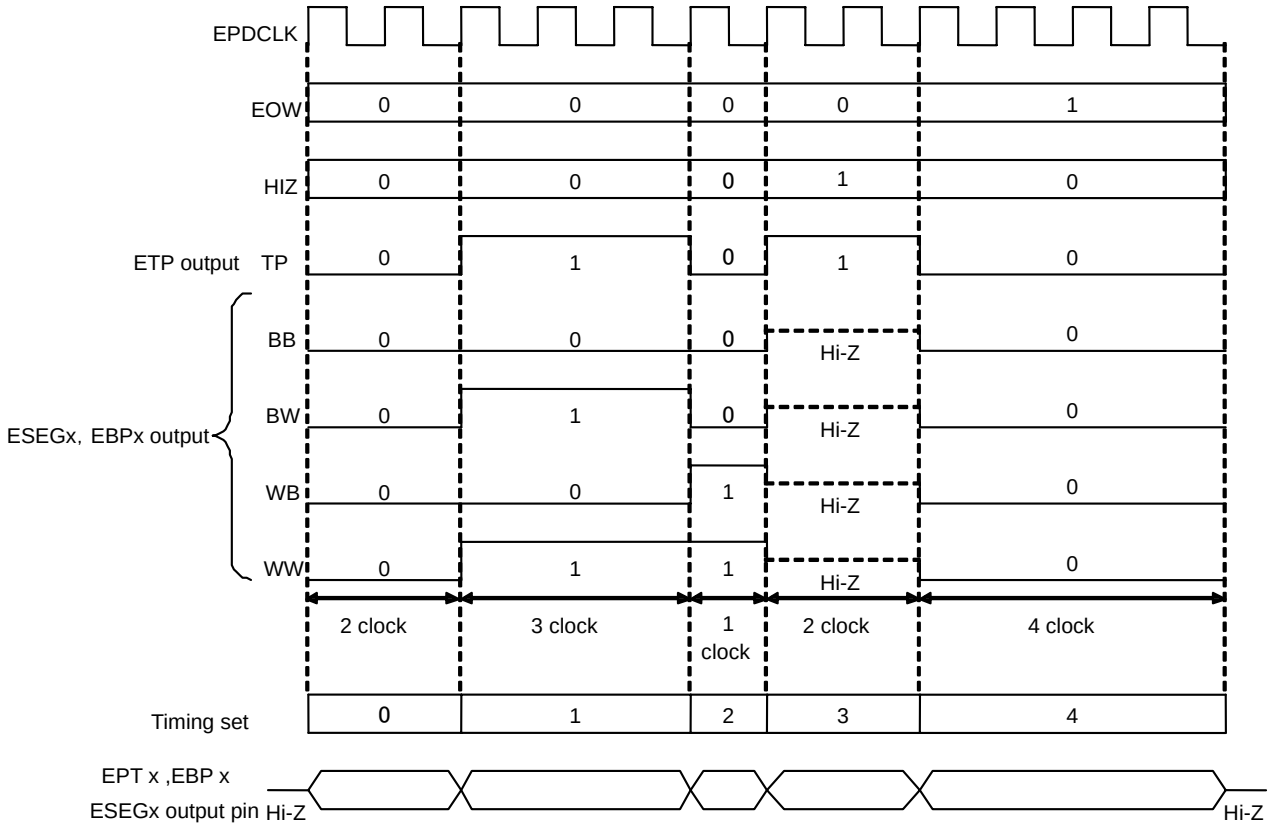

Figure 7.6.6.1 Display waveform example (corresponding to the setting in Table 7.6.6.2)

Note: Table 7.6.6.2 and Figure 7.6.6.1 are examples only for describing the relation between settings and waveforms, not used for the actual EPD drive.

7.6.7 Display Data Memories

The device integrates two display data memories (one display memory: 256-bit (for segment outputs) + 1-bit (for the back plane). One display data memory is for the display data before the EPD display update (current display data). Another one is for the display data to be updated (display data).

The current display memory is set with the following command parameters.

- EPD display segment output data : CURSDT command parameter P1-P32(CSEGDT[255:0]) (refer to "8.2.1 CURSDT: 0x01")
- Back plane output data : CURBDT command parameter B10 (CBPDT) (refer to "8.2.2 CURBDT: 0x02")

When storing 1 in the current display data memory, a black display is set. And when 0, a white display is set. When the EPDDCTL command B13-B12 (DSPMOD) is 0x1 or 0x3, storing 0 sets a white display and 1 sets a black. For details of this function, refer to "8.2.18 EPDDCTL: 0x21".

VDD power display memory is incorporated to hold currently displayed data in a deep standby state.

If EPD display/update operations are first performed after VDD power supply is turned on, a device that controls this device needs to set the currently displayed data in the currently displayed data memory. The currently displayed data must always be set before EPD display/update operations start. Otherwise, segment display waveforms cannot be guaranteed.

After the update of the EPD display is complete, the display data is automatically saved to the current display data memory. Setup is necessary only when the EPD display is updated for the first time after VDD power on. No setup is necessary for the second time and after. For the data transition of the current display data memory, see Figure 7.6.7.

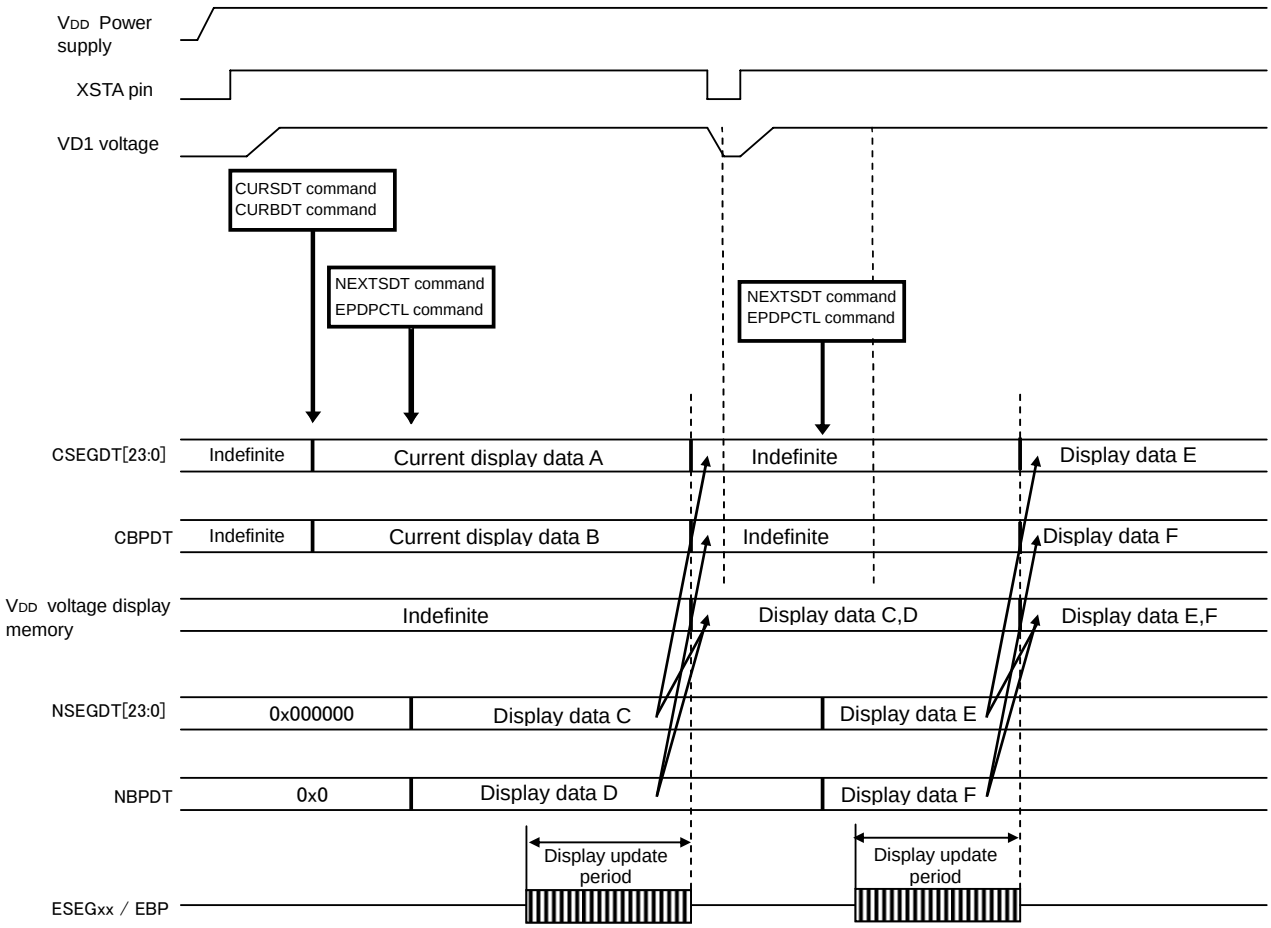

Figure 7.6.7 Data transition in current display data memory

The display data memories are set with the following command parameters.

- EPD display segment output data : NEXTSDT command parameter P1-P32(NSEGDT[255:0]) (refer to "8.2.13 NEXTSDT: 0x10")
- Back plane output data : EPDPCTL command parameter B10(NBPDT) (refer to "8.2.17 EPDPCTL: 0x20")

When 1 is stored in the display data memory, a black display is set. And when 0, a white display is set. The contents in the display data memory are reflected to the outputs, when the display update trigger (described later) is applied.

At reset, display data memories are cleared to 0.

Reverse, all white and all black display control

The displays of reverse, all white and all black are available, without rewriting the display data memories. These are set with the EPDDCTL command parameter B13-B12 (DSPMOD). For details of this function, refer to "8.2.18 EPDDCTL: 0x21".

7.6.8 Display Waveform Memory Selection

For Automatic EPD Display Update Sequence

When the automatic EPD display update sequence (ATEPDWR 1 to 7 commands) is issued, the display waveform memory, for the display waveform data at the EPD display update, is selected with settings of the FMDISB command B10 (FMDISB) / SLVSEL pin / POWCTL command B30 (ATTEMPON). For details of this function, refer to the following.

- ATEPDWR1 command issue: refer to "8.2.3 ATEPDWR1: 0x03"
- ATEPDWR2 command issue: refer to "8.2.4 ATEPDWR2: 0x04"
- ATEPDWR3 command issue: refer to "8.2.5 ATEPDWR3: 0x05"
- ATEPDWR4 command issue: refer to "8.2.6 ATEPDWR4: 0x06"
- ATEPDWR5 command issue: refer to "8.2.7 ATEPDWR5: 0x07"
- ATEPDWR6 command issue: refer to "8.2.8 ATEPDWR6: 0x08"
- ATEPDWR7 command issue: refer to "8.2.9 ATEPDWR7: 0x09"

For EPD Display Update Sequence

For the waveform selection using the EPD display update sequence (POWON / EPDWR / POWOFF commands), refer to "8.2.19 WFSEL: 0x22".

7.6.9 Automatic Temperature Detection Function

The automatic temperature detection function is as follows: detects a temperature with temperature detection circuit before the EPD display update, and automatically selects the display waveform data stored in the Flash memory, based on the above detection result.

This function is activated with the following settings.

- FMDISB command parameter B10(FMDISB) : 0 (refer to "8.2.11 FMDISB: 0x0B")
- POWCTL command parameter B30(ATTEMPON) : 1 (refer to "8.2.21 POWCTL: 0x24")

Note: When this device is used as a slave device IC (SLVSEL pin = High level), this function is not activated with the above settings.

The function automatically reads out the initial setting data (refer to "7.5.2 Flash Memory Initial Setting Data") stored in the Flash memory, before the EPD display update. The POWCTL command parameter issued with the command interface before the EPD display update overwrites data stored in the Flash memory. Make sure to program the initial setting data in the Flash memory.

For this functional descriptions, refer to the B30 ATTEMPON in "8.2.21 POWCTL: 0x24".

7.6.10 Display Update Control

Before the display update, all the following settings are necessary.

- EPD display update data is stored in the display data memory.
- When FMDISB command B10 (FMDISB) is 1 (Flash memory is not used), the display waveform is set to the WFSET command parameter.
- For the EPD display update after the deep standby release, the current display data is set to the CURSDT command parameter P1 - P32 (CSEGDT [255:0]), and the back plane output data is set to the CURBDT command parameter B10 (CBPDT).
- EPDDCTL command parameter B13 - B12 (DSPMOD) is set.
- The power supplies are stable. Refer to "7.7 State Transitions".

Master Device Display Control

When the device is used as a master device (SLVSEL pin = Low level), the display control changes at the ATEPDWR 1 to 7 commands (refer to "8.2.3 ATEPDWR 1") issue and the POWON / EPDWR / POWOFF commands issue.

At the ATEPDWR 1 to 7 Commands Issue

(1) When power supplies become stable, the display update trigger is automatically issued. The EPD drive waveform generation circuit outputs the drive waveforms programmed in the display waveform memory from the pins of segments, top plane and back plane, according to the display data memory contents and the current display data.

(2) After the display update, the display data memory contents are automatically stored in the current display memory.

(3) Then, the device enters into the power supply falling period.

At the POWON / EPDWR / POWOFF Commands Issue

(1) When power supplies become stable, issue the EPDWR command (refer to "8.2.16 EPDWR: 0x13"). After the EPDWR command issue, the display update trigger (EPDTRG) is issued. The EPD drive waveform generation circuit outputs the drive waveforms programmed in the display waveform memory from the pins of segments, top plane and back plane, according to the display data memory contents and the current display data.

(2) After the display update, the display data memory contents are automatically stored in the current display memory.

(3) The device returns to the power supply stable period.

The EPDTRG signal generated in the master device is output from the EPDTRG pin, with setting the IOCTL command parameter B10 (EPDTRGSIG) to 1. In multi-chip use, make sure to connect the EPDTRG pins of the master device and the slave device, mutually.

Slave Device Display Control

When the device is used as a slave device (SLVSEL pin = High level), the display control changes at the ATEPDWR 1 to 7 commands (refer to "8.2.3 ATEPDWR 1") issue and the POWON / EPDWR / POWOFF commands issue.

At the ATEPDWR 1 to 7 Commands Issue

(1) When power supplies become stable, the device waits the display update trigger (EPDTRG) input from the EPDTRG pin. After detecting the display update trigger with the EPDTRG pin, the EPD drive waveform generation circuit outputs the drive waveforms programmed in the display waveform memory from the pins of segments, top plane and back plane, according to the display data memory contents and the current display data.

(2) After the display update, the display data memory contents are automatically stored in the current display memory.

(3) Then, the device enters into the power supply falling period.

At the POWON / EPDWR / POWOFF Commands Issue

(1) When power supplies become stable, the device waits the display update trigger (EPDTRG) input from the EPDTRG pin. After detecting the display update trigger with the EPDTRG pin, the EPD drive waveform generation circuit outputs the drive waveforms programmed in the display waveform memory from the pins of segments, top plane and back plane, according to the display data memory contents and the current display data.

(2) After the display update, the display data memory contents are automatically stored in the current display memory.

(3) The device returns to the power supply stable period.

7.7 State Transitions

The states and the periods of this device are as follows.

- Deep standby state
- Standby state
- Internal oscillation start-up period
- Readout period of initial setting data in Flash memory
- Readout period of display waveform data in Flash memory
- Automatic temperature detection period
- Power supply start-up period
- Power supply stable period
- EPD display update period
- Power supply falling period

Table 7.7 describes each state / period.

Table 7.7 Descriptions of each state / period

State / period	Descriptions
Deep standby state	In the state, the VD1 Regulator is stopped. The command issue is impossible with the command interface. Refer to “7.1 Deep Standby”, for details.
Standby state	In the state, the built-in oscillation circuit and the VOUT1 Booster / VEPD Booster are stopped. The command issue is possible with the command interface.
Internal oscillation start-up period	In the period, the built-in oscillation circuit starts operation. The VOUT1 Booster / VEPD Booster are stopped.
Readout period of initial setting data in Flash memory	In the period, the POWCTL / IOCTL / SLVMODE / DET2CTL / DROECTL commands in the Flash memory are readout and reflected to the device.
Readout period of display waveform data in Flash memory	In the period one of seven (max.) waveform data in the Flash memory is readout and reflected to the device.
Automatic temperature detection period	In the period the temperature detection is automatically done before the EPD display update, and one of seven (max.) display waveform data in the Flash memory is readout and reflected to the device
Power supply start-up period	In the period, the VOUT1 Booster / VEPD Booster start operations and generate the VOUT1 voltage / VEPD voltage.
Power supply stable period	In the period, the VOUT1 voltage / VEPD voltage are stable. Or the EPD display update is available with the EPD display update start trigger.
EPD display update period	In the period, the EPD display update is done.
Power supply falling period	In the period, the VOUT1 Booster / VEPD Booster and the built-in oscillation circuit are stopped. After this period, the device enters into the standby state.

For the EPD display update, there are mainly two types of state transition as follows.

- Automatic EPD display update sequence (at ATEPDWR 1 to 7 commands issue)
  Note: For the ATEPDWR1 to 7 commands, the sequence starts after all the parameters are sent the number of which is set by the SEGDLEN command parameter setting (see Section 8.2.12 SEGDLEN: 0x0C).

- EPD display update sequence (at POWON / EPDWR / POWON commands issue)

For the above two types of state transition, the operations are changed with the following settings.

- SLVSEL pin
  Low level: the device is used alone or as a master device IC in multi-chip use.
  High level: the device is used for the EPD_MCU driver expansion or as a slave device IC in multi-chip use.
- FMDISB command parameter B10 (FMDISB)
  Set to 0: Flash memory data is used.

Set to 1: Flash memory data is unused.

Note: If setting values are not programmed in the Flash memory, make sure to set to 1.

- POWCTL command parameter B30 (ATTEMPON)
  Set to 0: automatic temperature detection function is invalid.
  Set to 1: automatic temperature detection function is valid.
  Note: Under the following conditions, the automatic temperature detection function is forced to be invalid.
  - **This device is used for the EPD_MCU driver expansion or as a slave device in multi-chip use.**
  - **Flash memory data is unused.**
- SLVMODE command parameter B10 (SLVMODE)
  Set to 0: the device is used as a slave device in multi-chip use.
  Set to 1: the device is used for the EPD_MCU driver expansion.
  Note: The SLVMODE command parameter B10 (SLVMODE) is valid only when the SLVSEL pin = High level.

Each state transition is described here.

7.7.1 Automatic EPD Display Update Sequence

When the ATEPDWR1 to 7 commands are issued, the automatic EPD display update sequence makes a series of operations necessary for the EPD display update from the standby state. After the completion of this sequence, the device automatically returns to the standby state.

7.7.1.1 When Used Alone or as a Master Device IC

When this device is used alone or as a master device IC in multi-chip use (SLVSEL pin = Low level), the state transition is changed with the following settings.

- Flash memory data is unused.
- When using Flash memory data / invalid automatic temperature detection function
- When using Flash memory data / valid automatic temperature detection function

Flash memory data is unused

Figure 7.7.1.1.1 shows the automatic EPD display update sequence, when the Flash memory data is unused.

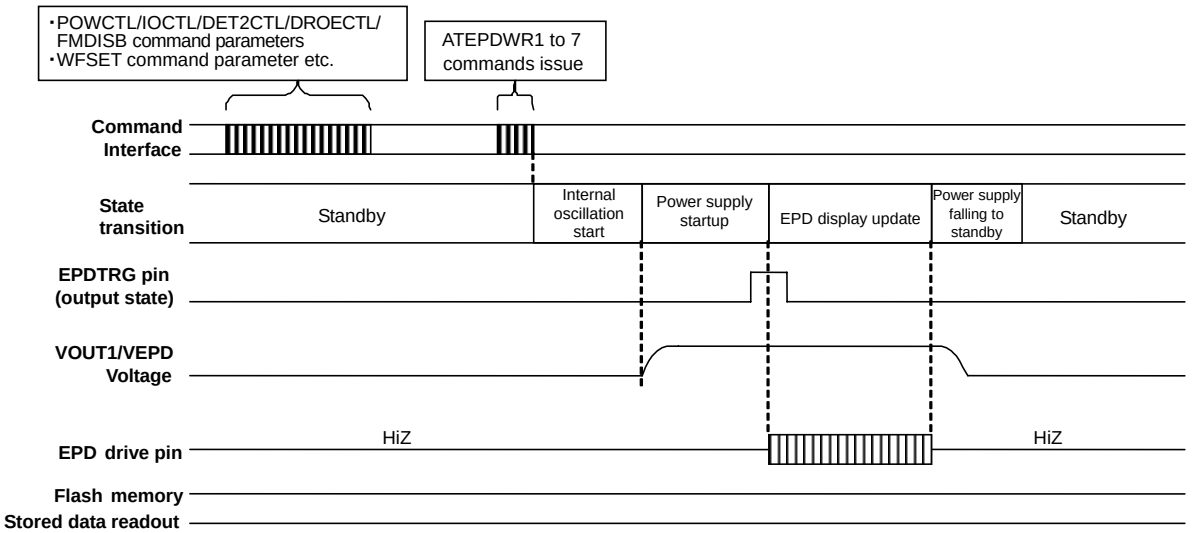

Figure 7.7.1.1.1 Flash memory data is unused

During the standby state, issue the POWCTL / IOCTL / DET2CTL / DROECTL / WFSET command parameters, with setting the FMDISB command parameter B10 (FMDISB) to 1 from the command interface.

After the ATEPDWR 1 to 7 commands are issued, the automatic EPD display update sequence starts.

As the Flash memory data is unused, the display waveform data in the Flash memory selected with the ATEPDWR 1 to 7 commands is invalid. The display waveform data, which is set with the WFSET command parameter, is used at the EPD display update.

After the EPD display update is completed, the device automatically enters into the power supply falling period and returns to the standby state.

When Using Flash Memory Data / Invalid Automatic Temperature Detection Function

Figure 7.7.1.1.2 shows the automatic EPD display update sequence, when the Flash memory data is used and the automatic temperature detection function is invalid.

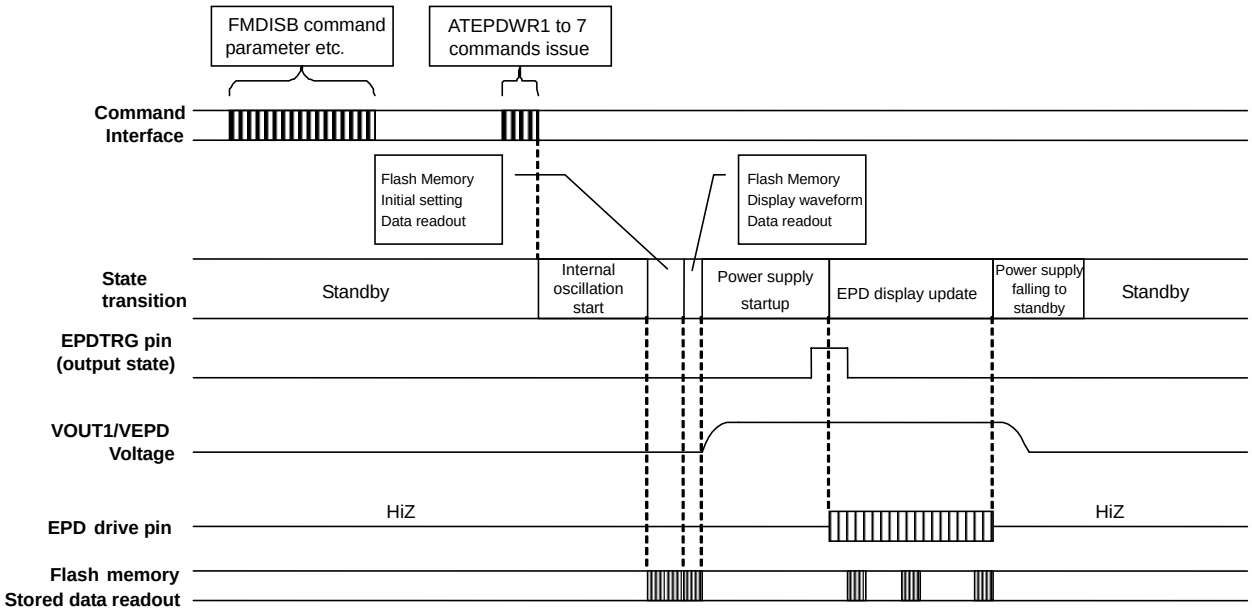

Figure 7.7.1.1.2 When the Flash memory data is used and the automatic temperature detection function is invalid

During the standby state, set the FMDISB command parameter B10 (FMDISB) to 0 from the command interface. The issue of the POWCTL / IOCTL / DET2CTL /DROECTL / WFSET command parameters is not necessary.

After the ATEPDWR 1 to 7 commands are issued, the automatic EPD display update sequence starts.

The display waveform data in the Flash memory selected with the ATEPDWR 1 to 7 commands is used at the EPD display update.

After the EPD display update is completed, the device automatically enters into the power supply falling period and returns to the standby state.

When Using Flash Memory Data / Invalid Automatic Temperature Detection Function

Figure 7.7.1.1.3 shows the automatic EPD display update sequence, when the Flash memory data is used and the automatic temperature detection function is invalid.

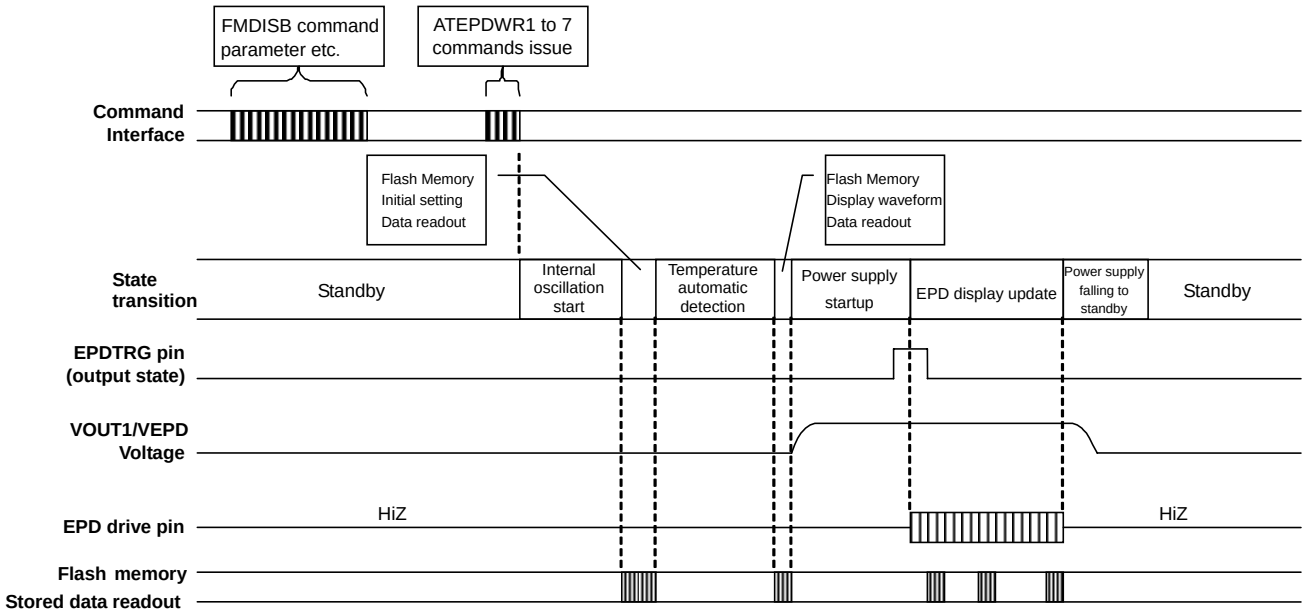

Figure 7.7.1.1.3 When the Flash memory data is used and the automatic temperature detection function is valid

During the standby state, set the FMDISB command parameter B10 (FMDISB) to 0 from the command interface. The issue of the POWCTL / IOCTL / DET2CTL / DROECTL / WFSET command parameters is not necessary.

After the ATEPDWR 1 to 7 commands are issued, the automatic EPD display update sequence starts.

As the automatic temperature detection function is valid, the display waveform data in the Flash memory selected with the ATEPDWR 1 to 7 commands is invalid. The display waveform data in the Flash memory is automatically selected with the automatic temperature detection result, and used at the EPD display update. For the details of the automatic temperature detection function, refer to B30 ATTEMPON in “8.2.21 POWCTL: 0x24”.

After the EPD display update is completed, the device automatically enters into the power supply falling period and returns to the standby state.

7.7.1.2 When Used for the EPD_MCU Driver Expansion or as a Slave Device IC

When this device is used for the EPD_MCU driver expansion or as a slave device IC in multi-chip use (SLVSEL pin = High level), the state transition is changed with the following settings.

- Flash memory data is unused.
  - When used for the EPD_MCU driver expansion
  - When used as a slave device IC
- When using Flash memory data
  - When used for the EPD_MCU driver expansion
  - When used as a slave device IC

Flash memory data is unused

- **When used for the EPD_MCU driver expansion**

Figure 7.7.1.2.1 shows the automatic EPD display update sequence, when the Flash memory data is unused and this device is used for the EPD_MCU driver expansion.

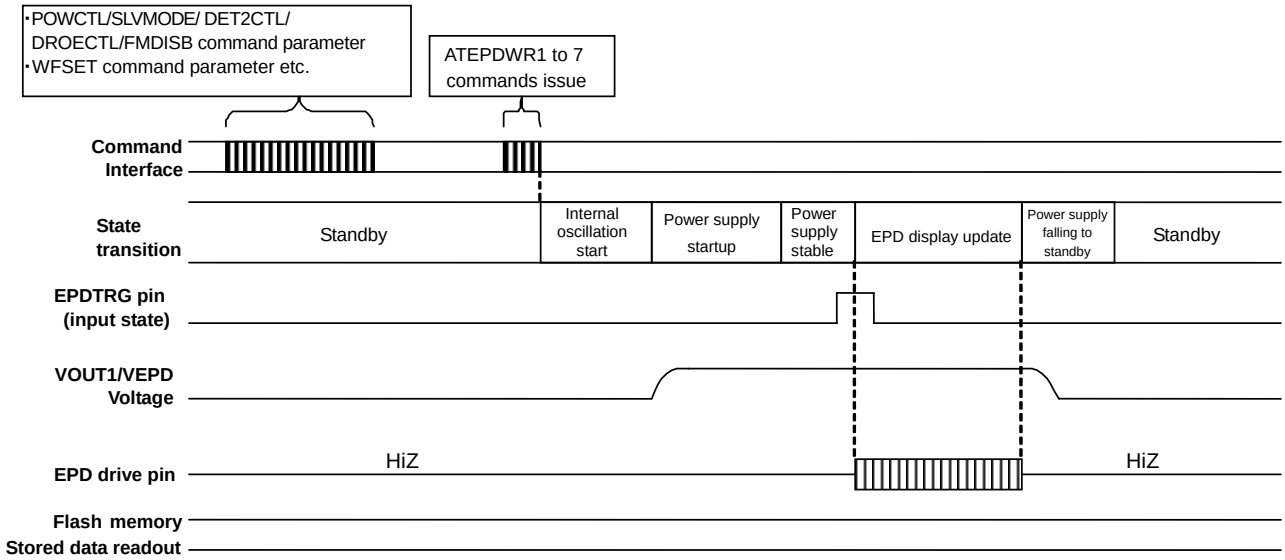

Figure 7.7.1.2.1 When not using Flash memory / used for the EPD_MCU driver expansion

During the standby state, issue the POWCTL / DET2CTL / DROECTL / WFSET command parameters, with setting the FMDISB command parameter B10 (FMDISB) to 1 and the SLVMODE command parameter B10 (SLVMODE) to 1 from the command interface.

After the ATEPDWR 1 to 7 commands are issued, the automatic EPD display update sequence starts.

As the Flash memory data is unused, the display waveform data in the Flash memory selected with the ATEPDWR 1 to 7 commands is invalid. The display waveform data, which is set with the WFSET command parameter, is used at the EPD display update.

The EPD display update start timing is synchronized with the EPD display update start of EPD_MCU. The timing is determined with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in EPD_MCU. For precautions when the device is used for the EPD_MCU driver expansion, refer to “7.8 EPD_MCU Driver Expansion Function”.

After the EPD display update is completed, the device automatically enters into the power supply falling period and returns to the standby state.

• **When Used as a Slave Device IC**

Figure 7.7.1.2.2 shows the automatic EPD display update sequence, when the Flash memory data is unused and this device is used as a slave device IC in multi-chip use.

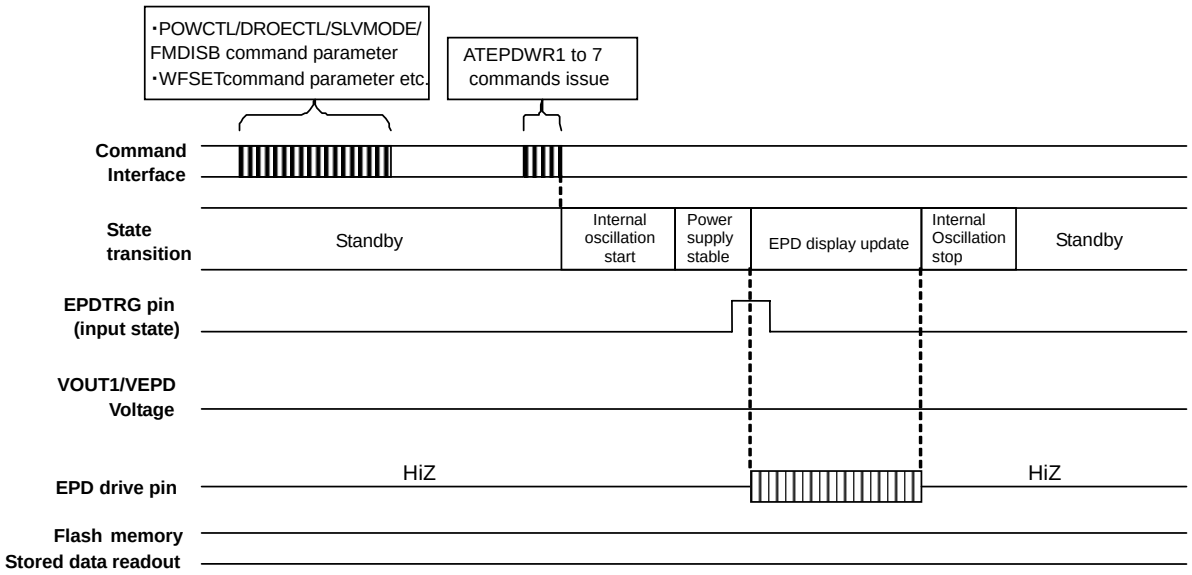

Figure 7.7.1.2.2 When not using Flash memory / used as a slave device IC

During the standby state, issue the POWCTL / DET2CTL / DROECTL / WFSET command parameters, with setting the FMDISB command parameter B10 (FMDISB) to 1 and the SLVMODE command parameter B10 (SLVMODE) to 0 from the command interface.

After the ATEPDWR 1 to 7 commands are issued, the automatic EPD display update sequence starts.

As the Flash memory data is unused, the display waveform data in the Flash memory selected with the ATEPDWR 1 to 7 commands is invalid. The display waveform data, which is set with the WFSET command parameter, is used at the EPD display update.

The EPD display update start timing is synchronized with the EPD display update start of the master device IC. The timing is determined with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in the master device IC. For precautions when the device is used in multi-chip use, refer to “7.9 Multi-chip Function”.

As the slave device IC uses the VOUT1 / VEPD power supplies generated in the master device IC, for the VOUT1 / VEPD power supplies, the device enters into the power supply stable period after the internal oscillation start-up period.

The VOUT1/VEPD power supply for the slave device IC uses the VOUT1/VEPD power supply generated by the master device IC, so when the built-in oscillator operation start period finishes, it will transition to the stable power supply period.

After EPD display/update operations finish, the built-in oscillator will stop automatically, and the state will transition to a standby state.

When Using Flash Memory Data

• **When used for the EPD_MCU driver expansion**

Figure 7.7.1.2.3 shows the automatic EPD display update sequence, when the Flash memory data is used and this device is used for the EPD_MCU driver expansion.

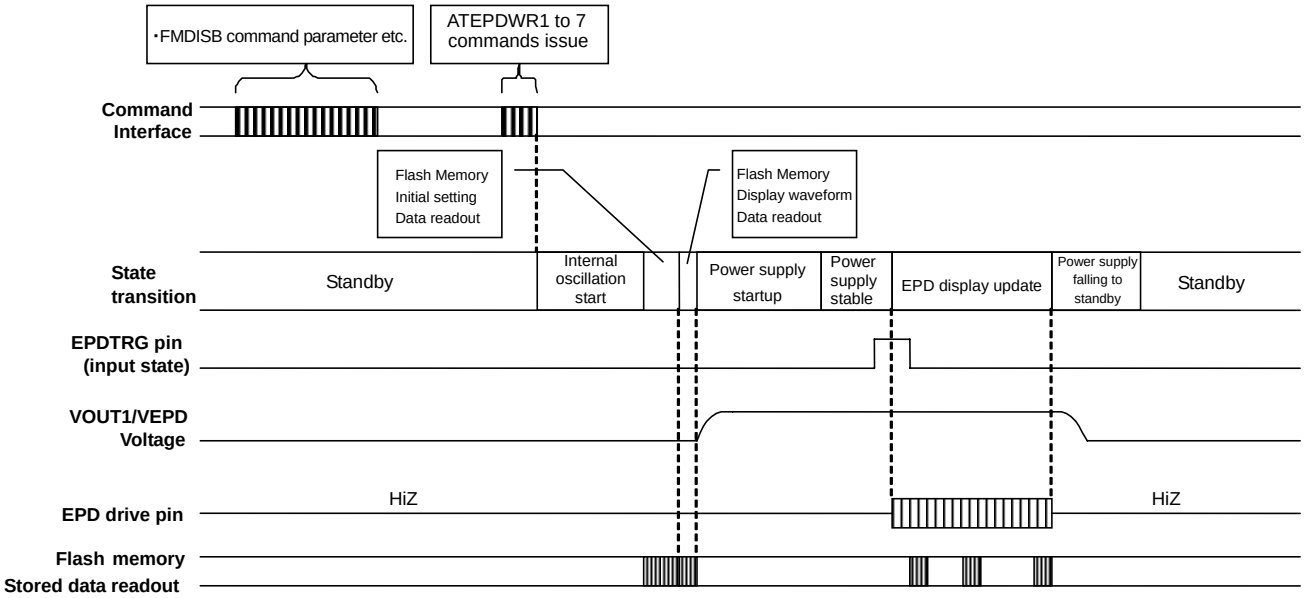

Figure 7.7.1.2.3 When using Flash memory data / used for the EPD_MCU driver expansion

While in a standby state, use the command interface to set the B10(FMDISB) parameter of the FMDISB command to “0”. There is no need to issue POWCTL / SLVMODE / DET2CTL / DROECTL / WFSET command parameters. Use the ATEPDWR1 to ATEPDWR7 commands to select display waveform data 1 to 7 for the Flash memory.

After the ATEPDWR 1 to 7 commands are issued, the automatic EPD display update sequence starts.

The display waveform data in the Flash memory selected with the ATEPDWR 1 to 7 commands is used at the EPD display update.

The EPD display update start timing is synchronized with the EPD display update start of EPD_MCU. The timing is determined with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in EPD_MCU. For precautions when the device is used for the EPD_MCU driver expansion, refer to “7.8 EPD_MCU Driver Expansion Function”.

After the EPD display update is completed, the device automatically enters into the power supply falling period and returns to the standby state.

• **When Used as a Slave Device IC**

Figure 7.7.1.2.4 shows the automatic EPD display update sequence, when the Flash memory data is used and this device is used as a slave device IC in multi-chip use.

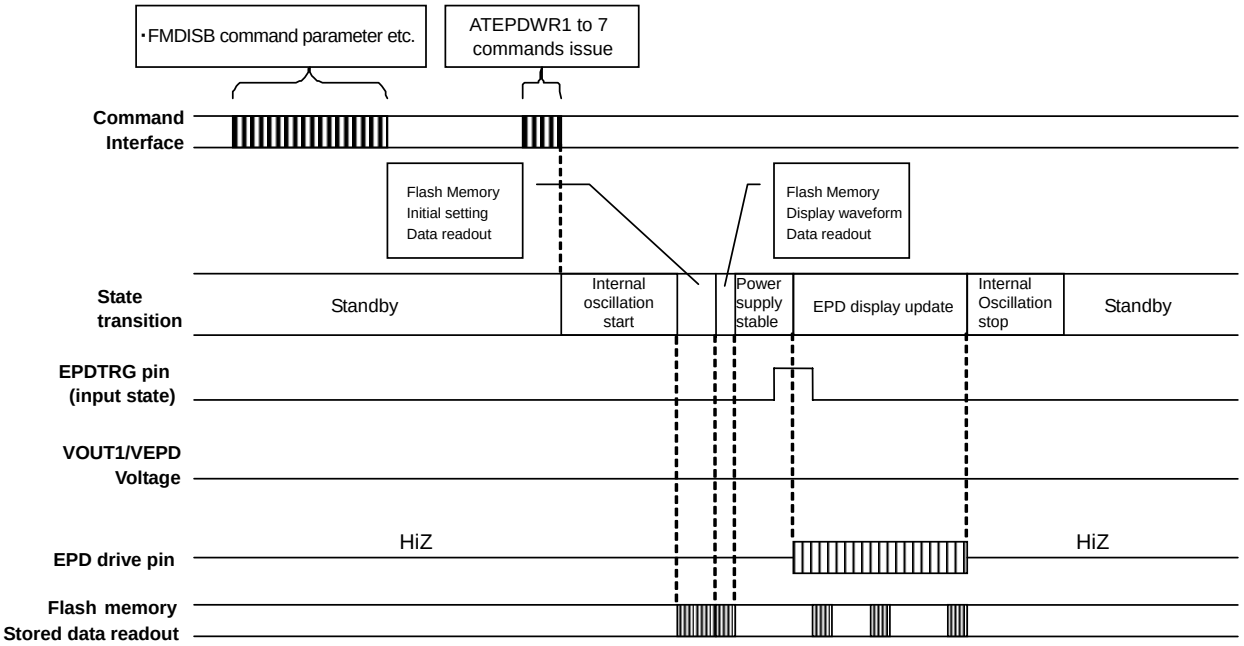

Figure 7.7.1.2.4 When using Flash memory data / used as a slave device IC

While in a standby state, use the command interface to set the B10(FMDISB) parameter of the FMDISB command to “0”. There is no need to issue POWCTL / SLVMODE / DET2CTL / DROECTL / WFSET command parameters. Use the ATEPDWR1 to ATEPDWR7 commands to select display waveform data 1 to 7 for the Flash memory.

After the ATEPDWR 1 to 7 commands are issued, the automatic EPD display update sequence starts.

The display waveform data in the Flash memory selected with the ATEPDWR 1 to 7 commands is used at the EPD display update.

The EPD display update start timing is synchronized with the EPD display update start of the master device IC. The timing is determined with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in the master device IC. For precautions when the device is used in multi-chip use, refer to “7.9 Multi-chip Function”.

As the slave device IC uses the VOUT1 / VEPD power supplies generated in the master device IC, for the VOUT1 / VEPD power supplies, the device enters into the power supply stable period after the internal oscillation start-up period.

After the EPD display update is completed, the internal oscillation automatically stops and the device enters into the standby state.

7.7.2 EPD Display Update Sequence

The EPD display update sequence issues the POWON / EPDWR / POWOFF commands individually, and controls the timings of the power supply start-up / EPD display update / power supply falling sequences with the command interface.

7.7.2.1 When Used Alone or as a Master Device IC

The state transition is changed with the following settings.

- Flash memory data is unused.
- When using Flash memory data / invalid automatic temperature detection function
- When using Flash memory data / valid automatic temperature detection function

Flash memory data is unused

Figure 7.7.2.1.1 shows the EPD display update sequence, when the Flash memory data is unused.

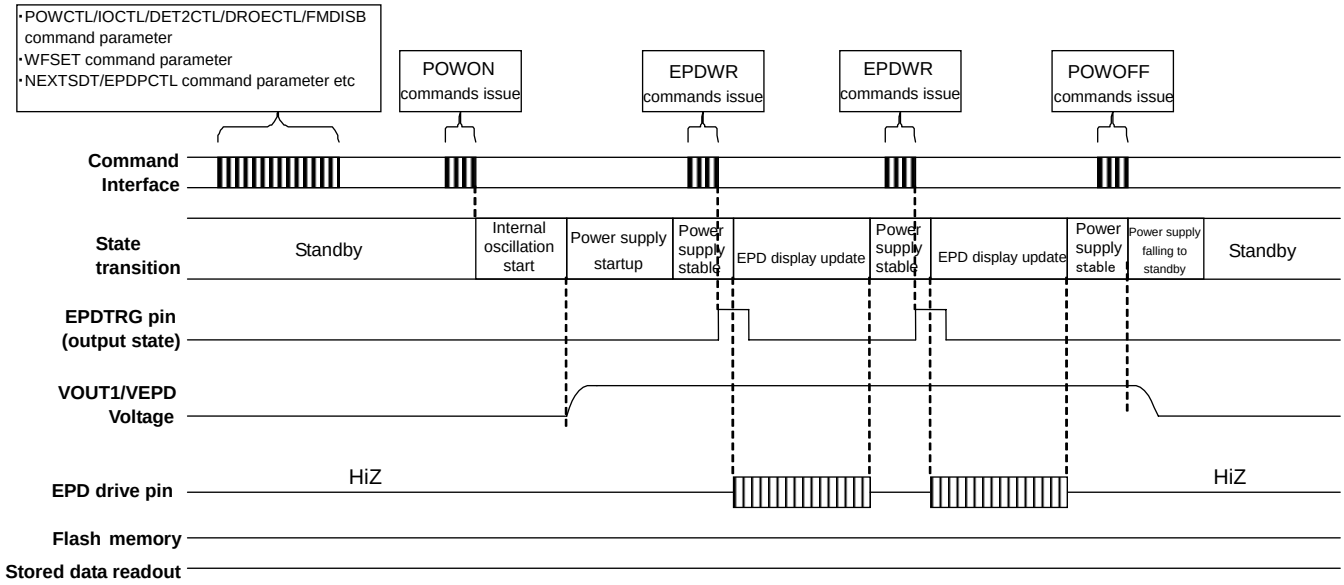

Figure 7.7.2.1.1 When not using Flash memory

During the standby state, issue the POWCTL / IOCTL / DET2CTL / DROECTL / WFSET command parameters, with setting the FMDISB command parameter B10 (FMDISB) to 1 from the command interface.

When the POWON command is issued, the device enters in to the power supply stable period from the internal oscillation start-up period (refer to Figure 7.7.2.1.1).

As the Flash memory data is unused, the display waveform data in the Flash memory selected with the WFSEL command parameter B12-B10 (WFSEL [2:0]) is invalid. The display waveform data, which is set with the WFSET command parameter, is used at the EPD display update.

When the EPDWR command is issued in the power supply stable period, the EPD display update is done. After the completion, the device returns to the power supply stable period. If the following command parameter is issued again in the power supply stable period, the EPD display update is done any number of times with issuing the EPDWR command. The command parameter shown below can be issued in this period.

- SEGDLEN command parameter (refer to “8.2.12 SEGDLEN: 0x0C”)
- NEXTSDT command parameter (refer to “8.2.13 NEXTSDT: 0x10”)
- EPDPCTL command parameter (refer to “8.2.17 EPDPCTL: 0x20”)
- EPDDCTL command parameter (refer to “8.2.18 EPDDCTL: 0x21”)
- TEMPSENSON command (refer to “8.2.20 TEMPSENSON: 0x23”)
- WFSET command parameter (refer to “8.2.10 WFSET: 0x0A”)
- EPDWR command parameter (refer to “8.2.16 EPDWR: 0x13”)
- POWOFF command parameter (refer to “8.2.15 POWOFF: 0x12”)

When the POWOFF command is issued in the power supply stable period, the device enters into the power supply falling period and returns to the standby state.

When Using Flash Memory Data / Invalid Automatic Temperature Detection Function

Figure 7.7.2.1.2 shows the EPD display update sequence, when the Flash memory data is used and the automatic temperature detection function is invalid.

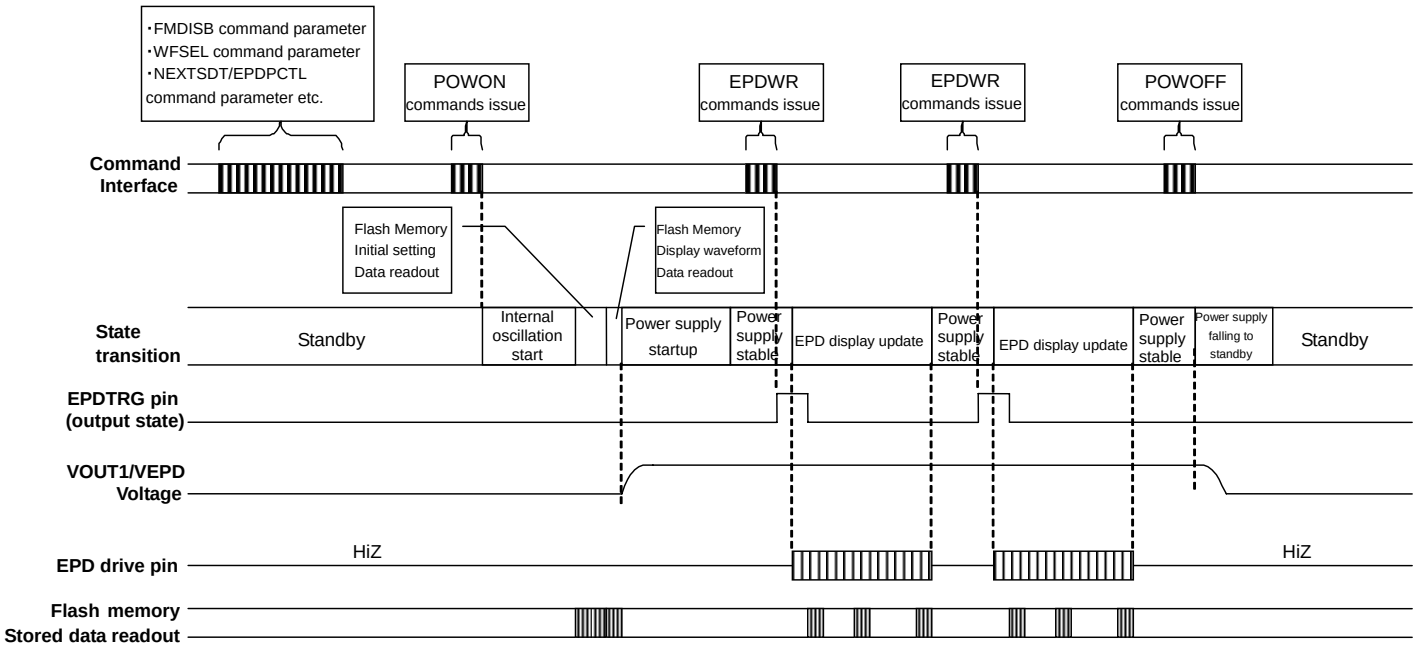

Figure 7.7.2.1.2 When using flash memory data / Invalid automatic temperature detection function

During the standby state, set the FMDISB command parameter B10 (FMDISB) to 0 from the command interface. The issue of the POWCTL / IOCTL / DET2CTL / DROECTL / WFSET command parameters is not necessary.

When the POWON command is issued, the device enters into the power supply stable period from the internal oscillation start-up period (refer to Figure 7.7.2.1.2).

The display waveform data in the Flash memory selected with the WFSEL command parameter B12-B10 (WFSEL [2:0]) is used at the EPD display update.

When the EPDWR command is issued in the power supply stable period, the EPD display update is done. After the completion, the device returns to the power supply stable period. If the following command parameter is issued again in the power supply stable period, the EPD display update is done any number of times with issuing the EPDWR command. The command parameter shown below can be issued in this period.

- SEGDLEN command parameter (refer to “8.2.12 SEGDLEN: 0x0C”)
- NEXTSDT command parameter (refer to “8.2.13 NEXTSDT: 0x10”)
- EPDPCTL command parameter (refer to “8.2.17 EPDPCTL: 0x20”)
- EPDDCTL command parameter (refer to “8.2.18 EPDDCTL: 0x21”)
- TEMPSENSON command (refer to “8.2.20 TEMPSENSON: 0x23”)
- WFSET command parameter (refer to “8.2.10 WFSET: 0x0A”)
- EPDWR command parameter (refer to “8.2.16 EPDWR: 0x13”)
- POWOFF command parameter (refer to “8.2.15 POWOFF: 0x12”)

When the POWOFF command is issued in the power supply stable period, the device enters into the power supply falling period and returns to the standby state.

When Using Flash Memory Data / Valid Automatic Temperature Detection Function

Figure 7.7.2.1.3 shows the EPD display update sequence, when the Flash memory data is used and the automatic temperature detection function is valid.

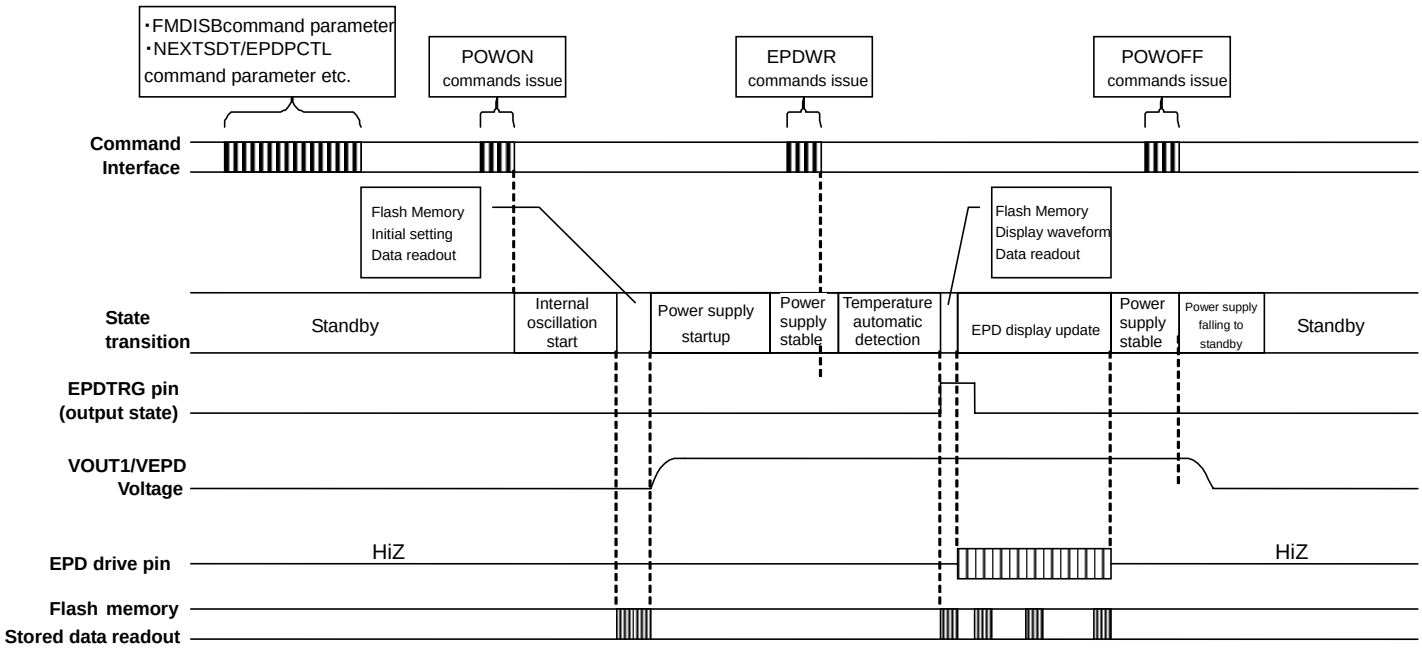

Figure 7.7.2.1.3 When using flash memory data / Valid automatic temperature detection function

During the standby state, set the FMDISB command parameter B10 (FMDISB) to 0 from the command interface. The issue of the POWCTL / IOCTL / DET2CTL / DROECTL / WFSET command parameters is not necessary.

When the POWON command is issued, the device enters into the power supply stable period from the internal oscillation start-up period (refer to Figure 7.7.2.1.3).

As the automatic temperature detection function is valid, the display waveform data in the Flash memory selected with the WFSEL command parameter B12-B10 (WFSEL [2:0]) is invalid. The display waveform data in the Flash memory is automatically selected with the automatic temperature detection result, and used at the EPD display update.

When the EPDWR command is issued in the power supply stable period, the EPD display update is done. After the completion, the device returns to the power supply stable period. If the following command parameter is issued again in the power supply stable period, the EPD display update is done any number of times with issuing the EPDWR command. The command parameter shown below can be issued in this period.

- SEGDLEN command parameter (refer to “8.2.12 SEGDLEN: 0x0C”)
- NEXTSDT command parameter (refer to “8.2.13 NEXTSDT: 0x10”)
- EPDPCTL command parameter (refer to “8.2.17 EPDPCTL: 0x20”)
- EPDDCTL command parameter (refer to “8.2.18 EPDDCTL: 0x21”)
- TEMPSENSON command (refer to “8.2.20 TEMPSENSON: 0x23”)
- WFSET command parameter (refer to “8.2.10 WFSET: 0x0A”)
- EPDWR command parameter (refer to “8.2.16 EPDWR: 0x13”)
- POWOFF command parameter (refer to “8.2.15 POWOFF: 0x12”)

When the POWOFF command is issued in the power supply stable period, the device enters into the power supply falling period and returns to the standby state.

7.7.2.2 When Used for the EPD_MCU Driver Expansion or as a Slave Device IC

When this device is used for the EPD_MCU driver expansion or as a slave device IC in multi-chip use (SLVSEL pin = High level), the state transition is changed with the following settings.

- Flash memory data is unused.
  - When used for the EPD_MCU driver expansion
  - When used as a slave device IC
- When using Flash memory data
  - When used for the EPD_MCU driver expansion
  - When used as a slave device IC

Flash memory data is unused.

- **When used for the EPD_MCU driver expansion**

Figure 7.7.2.2.1 shows the EPD display update sequence, when the Flash memory data is unused and the device is used for the EPD_MCU driver expansion.

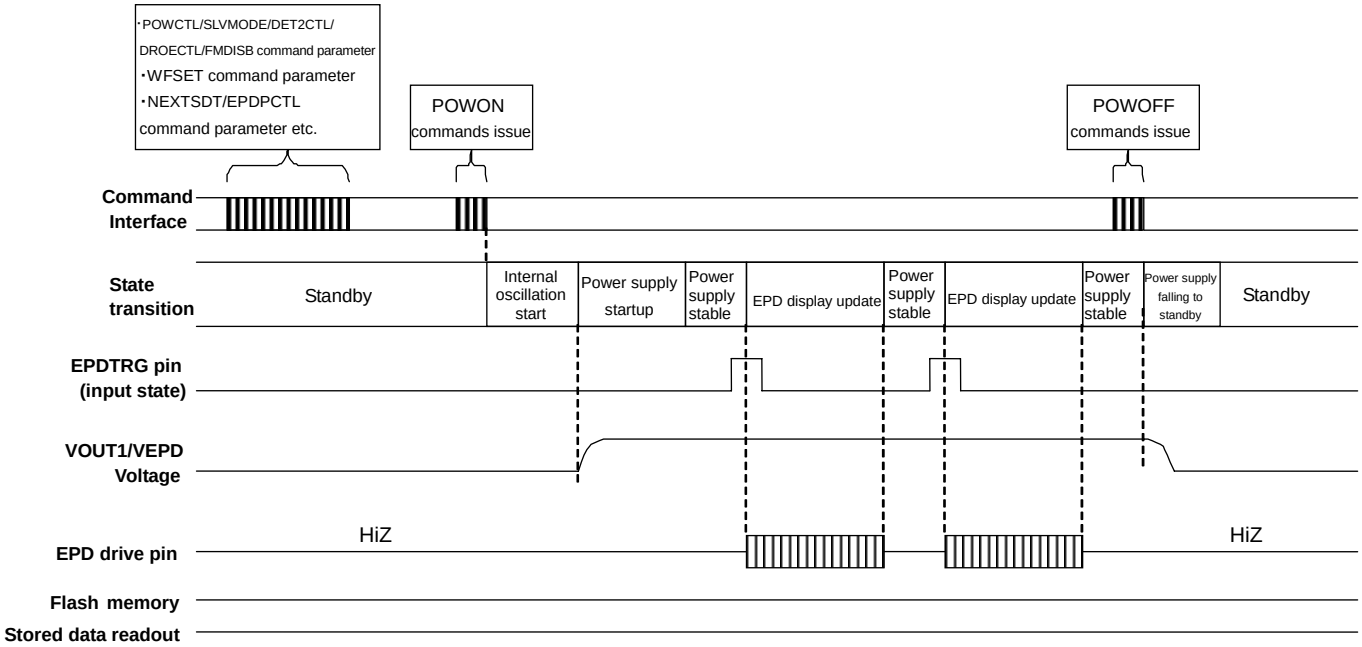

Figure 7.7.2.2.1 When not using Flash memory / used for EPD_MCU driver expansion

During the standby state, issue the POWCTL / DET2CTL / DROECTL / WFSET command parameters, with setting the FMDISB command parameter B10 (FMDISB) to 1 and the SLVMODE command parameter B10 (SLVMODE) to 1 from the command interface.

When the POWON command is issued, the device enters into the power supply stable period from the internal oscillation start-up period (refer to Figure 7.7.2.2.1).

As the Flash memory data is unused, the display waveform data in the Flash memory selected with the WFSEL command parameter B12-B10 (WFSEL [2:0]) is invalid. The display waveform data, which is set with the WFSET command parameter, is used at the EPD display update.

The EPD display update start timing is synchronized with the EPD display update start of EPD_MCU. The timing is determined with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in EPD_MCU. The EPDWR command is invalid. For precautions when the device is used for the EPD_MCU driver expansion, refer to “7.8 EPD_MCU Driver Expansion Function”.

After the EPD display update completion, the device returns to the power supply stable period. If the following command parameter is issued again in the power supply stable period, the EPD display update is done any number of times with issuing the EPD display update start trigger (EPDTRG) command. The

command parameter shown below can be issued in this period.

- SEGDLEN command parameter (refer to “8.2.12 SEGDLEN: 0x0C”)
- NEXTSDT command parameter (refer to “8.2.13 NEXTSDT: 0x10”)
- EPDPCTL command parameter (refer to “8.2.17 EPDPCTL: 0x20”)
- EPDDCTL command parameter (refer to “8.2.18 EPDDCTL: 0x21”)
- TEMPSENSON command (refer to “8.2.20 TEMPSENSON: 0x23”)
- WFSET command parameter (refer to “8.2.10 WFSET: 0x0A”)
- EPDWR command parameter (refer to “8.2.16 EPDWR: 0x13”)
- POWOFF command parameter (refer to “8.2.15 POWOFF: 0x12”)

When the POWOFF command is issued in the power supply stable period, the device enters into the power supply falling period and returns to the standby state.

• **When Used as a Slave Device IC**

Figure 7.7.2.2.2 shows the EPD display update sequence, when the Flash memory data is unused and the device is used as a slave device IC in multi-chip use.

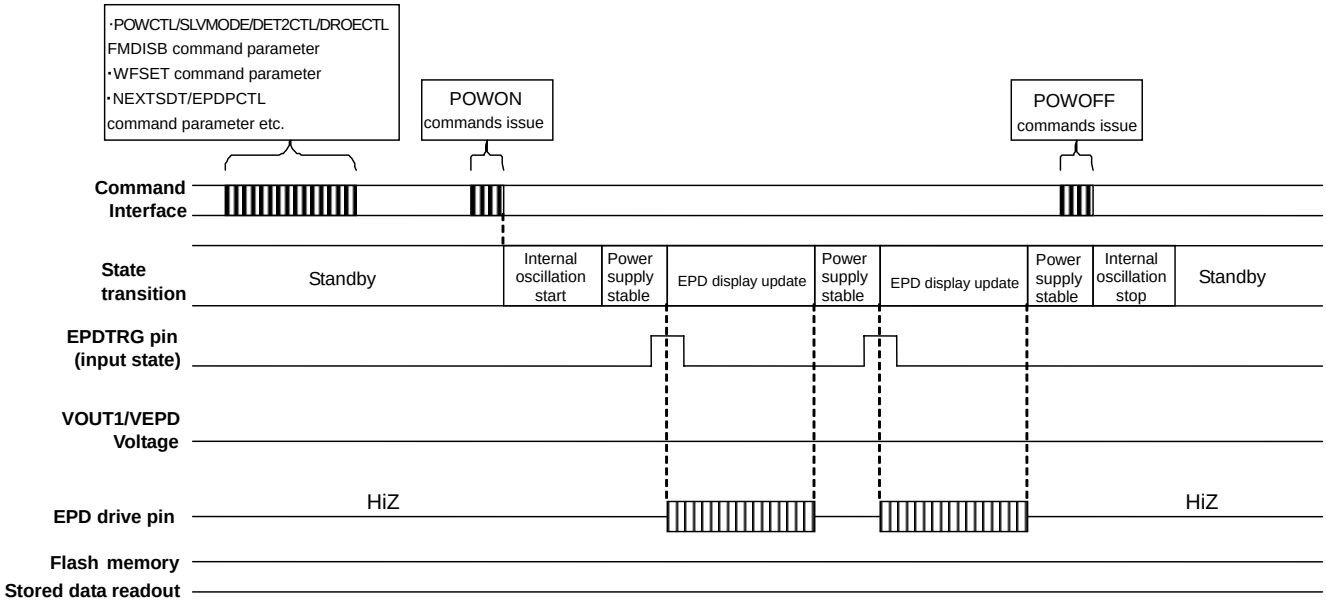

Figure 7.7.2.2.2 When not using Flash memory / used as a slave device IC

During the standby state, issue the POWCTL / DET2CTL / DROECTL / WFSET command parameters, with setting the FMDISB command parameter B10 (FMDISB) to 1 and the SLVMODE command parameter B10 (SLVMODE) to 0 from the command interface.

When the POWON command is issued, the device enters in to the power supply stable period from the internal oscillation start-up period (refer to Figure 7.7.2.2.2).

As the Flash memory data is unused, the display waveform data in the Flash memory selected with the WFSEL command parameter B12-B10 (WFSEL [2:0]) is invalid. The display waveform data, which is set with the WFSET command parameter, is used at the EPD display update.

The EPD display update start timing is synchronized with the EPD display update start of the master device IC. The timing is determined with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in the master device IC. For precautions when the device is used in multi-chip use, refer to “7.9 Multi-chip Function”.

After the EPD display update completion, the device returns to the power supply stable period. If the following command parameter is issued again in the power supply stable period, the EPD display update is done any number of times with issuing the EPD display update start trigger (EPDTRG) command. The command parameter shown below can be issued in this period.

- SEGDLEN command parameter (refer to “8.2.12 SEGDLEN: 0x0C”)
- NEXTSDT command parameter (refer to “8.2.13 NEXTSDT: 0x10”)
- EPDPCTL command parameter (refer to “8.2.17 EPDPCTL: 0x20”)
- EPDDCTL command parameter (refer to “8.2.18 EPDDCTL: 0x21”)
- TEMPSENSON command (refer to “8.2.20 TEMPSENSON: 0x23”)
- WFSET command parameter (refer to “8.2.10 WFSET: 0x0A”)
- EPDWR command parameter (refer to “8.2.16 EPDWR: 0x13”)
- POWOFF command parameter (refer to “8.2.15 POWOFF: 0x12”)

As the slave device IC uses the VOUT1 / VEPD power supplies generated in the master device IC, for the VOUT1 / VEPD power supplies, the device enters into the power supply stable period after the internal oscillation start-up period.

When the POWOFF command is issued in the power supply stable period, the device enters into the power supply falling period and returns to the standby state.

When Using Flash Memory Data

• **When used for the EPD_MCU driver expansion**

Figure 7.7.2.2.3 shows the EPD display update sequence, when the Flash memory data is used and the device is used for the EPD_MCU driver expansion.

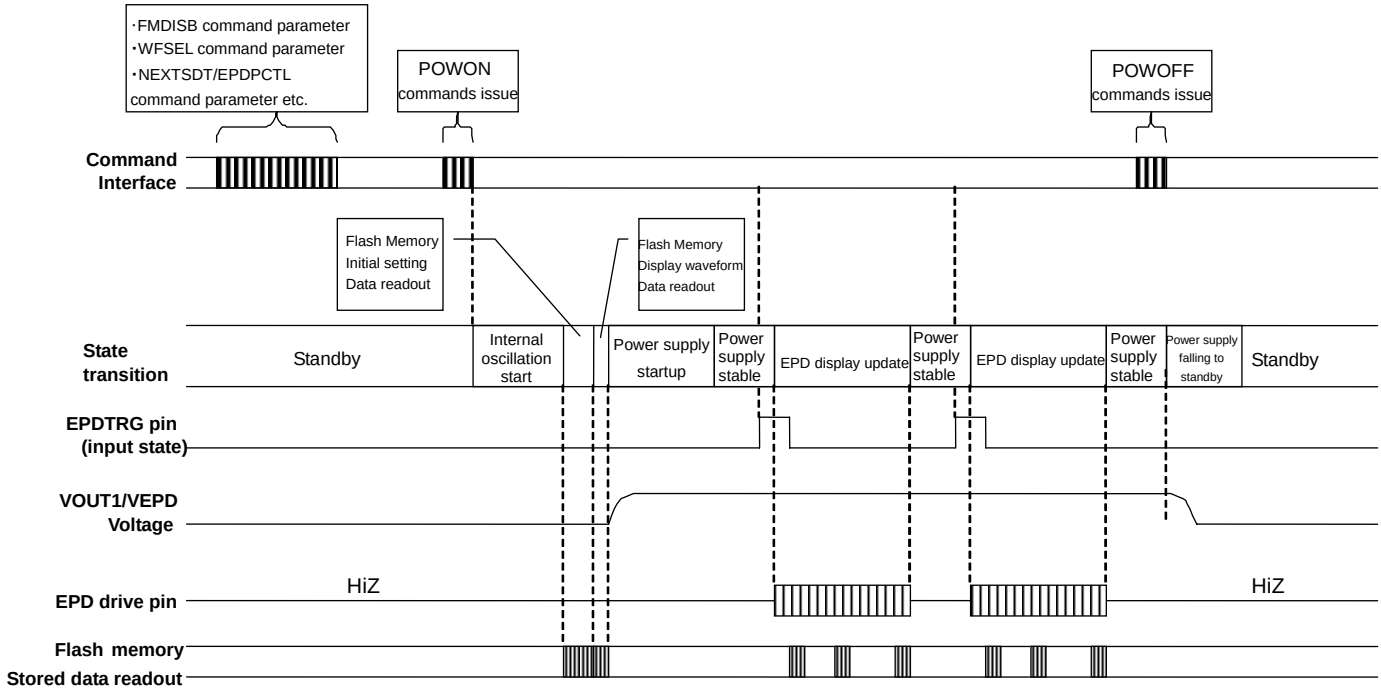

Figure 7.7.2.2.3 When using Flash memory / used for EPD_MCU driver expansion

During the standby state, set the FMDISB command parameter B10 (FMDISB) to 0 from the command interface. The issue of the POWCTL / SLVMODE / DET2CTL / DROECTL / WFSEL command parameters is not necessary.

When the POWON command is issued, the device enters into the power supply stable period from the internal oscillation start-up period (refer to Figure 7.7.2.2.3).

The display waveform data in the Flash memory selected with the WFSEL command parameter B12-B10 (WFSEL [2:0]) is used at the EPD display update.

The EPD display update start timing is synchronized with the EPD display update start of EPD_MCU. The timing is determined with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in EPD_MCU. EPDWR command is invalid. For precautions when the device is used for the EPD_MCU driver expansion, refer to “7.8 EPD_MCU Driver Expansion Function”.

After the EPD display update completion, the device returns to the power supply stable period. If the following command parameter is issued again in the power supply stable period, the EPD display update is done any number of times with issuing the EPD display update start trigger (EPDTRG) command. The command parameter shown below can be issued in this period.

- SEGDLEN command parameter (refer to "8.2.12 SEGDLEN: 0x0C")
- NEXTSDT command parameter (refer to "8.2.13 NEXTSDT: 0x10")
- EPDPCTL command parameter (refer to "8.2.17 EPDPCTL: 0x20")
- EPDDCTL command parameter (refer to "8.2.18 EPDDCTL: 0x21")
- TEMPSENSON command (refer to "8.2.20 TEMPSENSON: 0x23")
- WFSET command parameter (refer to "8.2.10 WFSET: 0x0A")
- EPDWR command parameter (refer to "8.2.16 EPDWR: 0x13")
- POWOFF command parameter (refer to "8.2.15 POWOFF: 0x12")

When the POWOFF command is issued in the power supply stable period, the device enters into the power supply falling period and returns to the standby state.

• **When Used as a Slave Device IC**

Figure 7.7.2.2.4 shows the EPD display update sequence, when the Flash memory data is used and the device is used as a slave device IC in multi-chip use.

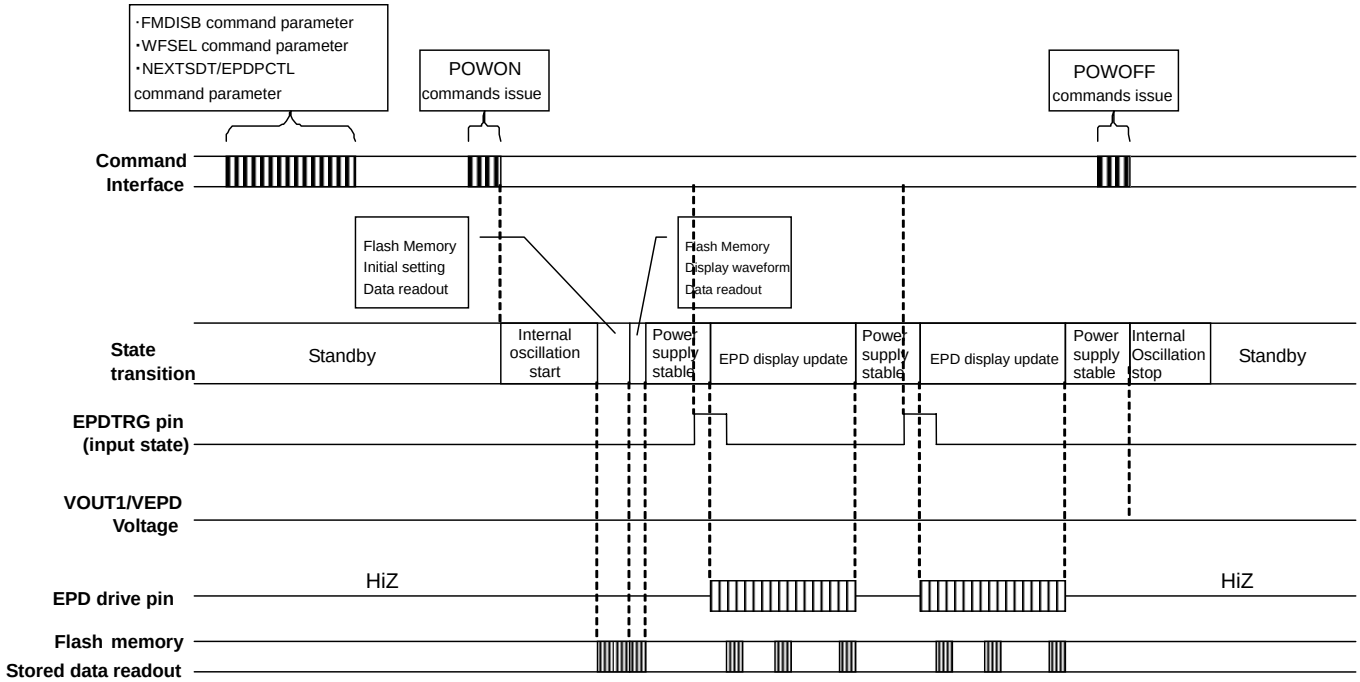

Figure 7.7.2.2.4 When using Flash memory / used as a slave device IC

During the standby state, set the FMDISB command parameter B10 (FMDISB) to 0 from the command interface. The issue of the POWCTL / SLVMODE / DET2CTL / DROECTL / WFSEL command parameters is not necessary.

When the POWON command is issued, the device enters into the power supply stable period from the internal oscillation start-up period (refer to Figure 7.7.2.2.4).

The display waveform data in the Flash memory selected with the WFSEL command parameter B12-B10 (WFSEL [2:0]) is used at the EPD display update.

The EPD display update start timing is synchronized with the EPD display update start of the master device IC. The timing is determined with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in the master device IC. For precautions when the device is used in multi-chip use, refer to "7.9 Multi-chip Function".

After the EPD display update completion, the device returns to the power supply stable period. If the

following command parameter is issued again in the power supply stable period, the EPD display update is done any number of times with issuing the EPD display update start trigger (EPDTRG) command. The command parameter shown below can be issued in this period.

- SEGDLEN command parameter (refer to "8.2.12 SEGDLEN: 0x0C")
- NEXTSDT command parameter (refer to "8.2.13 NEXTSDT: 0x10")
- EPDPCTL command parameter (refer to "8.2.17 EPDPCTL: 0x20")
- EPDDCTL command parameter (refer to "8.2.18 EPDDCTL: 0x21")
- TEMPSENSON command (refer to "8.2.20 TEMPSENSON: 0x23")
- WFSET command parameter (refer to "8.2.10 WFSET: 0x0A")
- EPDWR command parameter (refer to "8.2.16 EPDWR: 0x13")
- POWOFF command parameter (refer to "8.2.15 POWOFF: 0x12")

When the POWOFF command is issued in the power supply stable period, the device enters into the power supply falling period and returns to the standby state.

7.8 EPD_MCU Driver Expansion Function

7.8.1 EPD_MCU Driver Expansion Function Outline

The device can be used for the EPD driver expansion of Seiko Epson EPD microcontroller (EPD_MCU). The number of EPD driver pins of the Seiko Epson EPD_MCU can be extended, with this function. Major functions are as follows.

- The VEPD voltage generated with the boost circuit in this device is supplied to VEPD and VE5 pins of EPD_MCU.
- The EPD display update synchronization is available with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in EPD_MCU.
- The display waveforms, which are common for EPD_MCU, are stored.

7.8.2 Settings for EPD_MCU driver expansion

When the device is used for the Seiko Epson EPD_MCU driver expansion, settings of pin / command parameter are as follows.

- SLVSEL pin: High level
- SLVMODE command parameter B10 (SLVMODE): 1 (refer to "8.2.23 SLVMODE: 0x26")

7.8.3 Display Synchronization for the EPD_MCU driver expansion

When used for the EPD_MCU driver expansion, the EPD display update synchronization between this device and EPD_MCU is necessary to execute the EPD display update correctly.

This EPD display update synchronization is made possible at the EPD display update, with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in EPD_MCU. This function is effective with the following connections.

- EPDCLK pin: connect to the EPDCLK pin of EPD_MCU
- EPDTRG pin: connect to the EPDTRG pin of EPD_MCU

The EPDCLK clock phase is active High. When the EPDTRG signal of High level is input with the EPDCLK signal, the EPD display update starts. Refer to Figure 7.8.3.

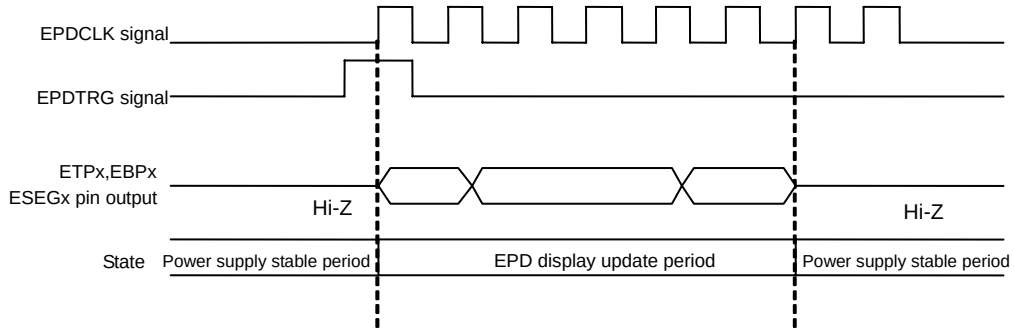

Figure 7.8.3 Relation of EPDCLK signal and EPDTRG signal

The EPDCLK signal specifications are as follows.

- Cycle: ≥ 31.25 μs
- Frequency: ≤ 32KHz

7.8.4 Display Waveform Data for the EPD_MCU Driver Expansion

When the device is used for the EPD_MCU driver expansion, it is necessary to use the same display waveform data as EPD_MCU (refer to "7.6.6 Display Waveform Memory"). As the display waveform memory configurations of EPD_MCU and this device are same, the EPD display update is available with common settings. If the display waveform data is different, the EPD display update is not guaranteed.

7.8.5 Connecting Diagram for EPD_MCU Driver Expansion

For a connection diagram example used for the EPD_MCU driver expansion, refer to Figure 11.3 in "11.3 Example of Connecting Diagram for EPD_MCU Driver Expansion".

7.9 Multi-chip Function

7.9.1 Multi-chip Function Outline

The device can be used in multi-chip use. This function makes the EPD drive pin expansion available. Major functions are as follows.

- The VOUT1 voltage generated with the boost circuit in the master device IC (of this device) is supplied to the VOUT1 pin of the slave device IC (of this device).
- The VEPD voltage generated with the boost circuit in the master device IC (of this device) is supplied to the VEPD pin of the slave device IC (of this device).
- The EPD display update synchronization is available with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in the master device IC.

7.9.2 Settings in Multi-chip Use

In multi-chip use, the settings of pin / command parameter of the master device IC are as follows.

- SLVSEL pin: Low level
- IOCTL command parameter B10 (EPDTRGSIG): 1 (refer to "8.2.22 IOCTL: 0x25")

The settings of pin / command parameter of the slave device IC are as follows.

- SLVSEL pin: High level
- SLVMODE command parameter B10 (SLVMODE): 0 (refer to "8.2.23 SLVMODE: 0x26")

7.9.3 Display Synchronization in Multi-chip Use

In multi-chip use, the EPD display update synchronization between the master device IC and the slave device IC is necessary to execute the EPD display update correctly.

This EPD display update synchronization is made possible at the EPD display update, with the EPD display update start trigger (EPDTRG) and the EPD display update base clock (EPDCLK) generated in the master device IC. This function is effective with the following connections.

- Connect the EPDCLK pins of the master device IC and the slave device IC mutually.
- Connect the EPDTRG pins of the master device IC and the slave device IC mutually.

The EPDCLK clock phase is active High. When the EPDTRG signal of High level is input with the EPDCLK signal, the EPD display update starts. Refer to Figure 7.9.3.

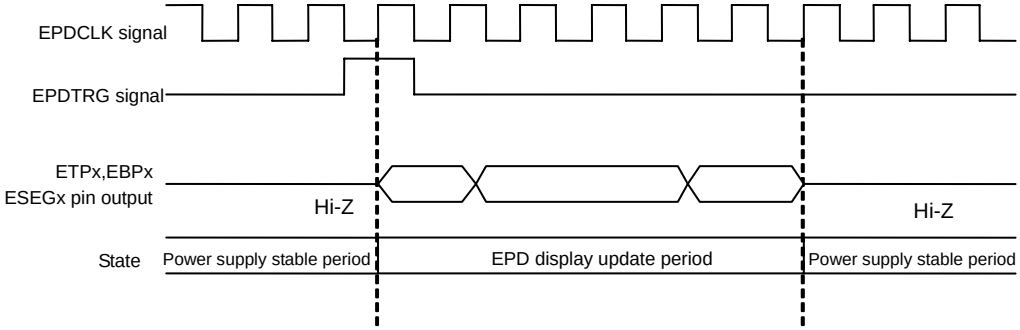

Figure 7.9.3 Relation of EPDCLK signal and EPDTRG signal

The cycle / frequency of EPDCLK signal are as follows

- Cycle: 4.096ms (Typ.) fixed
- Frequency: 244Hz (Typ.) fixed

7.9.4 Display Waveform Data in Multi-chip Use

When the device is used in multi-chip use, it is necessary that both the master device IC and the slave device IC use the same display waveform data (refer to “7.6.6 Display Waveform Memory”. If the display waveform data is different, the EPD display update is not guaranteed.

7.9.5 Connecting Diagram in Multi-chip Use

For a connection diagram example in multi-chip use, refer to Figure 11.4 in “11.4 Connecting Diagram Example”.

8. Commands

8.1 List of Commands

◇ Command address table

Table 8.1.1 Command address table

No.	Name	Code	Description	Type	P-Num	P-Res	F-Mem
1	CURSDT	0x01	Current Segment Data	WR1	32	No	No
2	CURBDT	0x02	Current Back Plane Data	WR1	1	No	No
3	ATEPDWR1	0x03	Auto EPD Write 1	WR2	32	Yes	No
4	ATEPDWR2	0x04	Auto EPD Write 2	WR2	32	Yes	No
5	ATEPDWR3	0x05	Auto EPD Write 3	WR2	32	Yes	No
6	ATEPDWR4	0x06	Auto EPD Write 4	WR2	32	Yes	No
7	ATEPDWR5	0x07	Auto EPD Write 5	WR2	32	Yes	No
8	ATEPDWR6	0x08	Auto EPD Write 6	WR2	32	Yes	No
9	ATEPDWR7	0x09	Auto EPD Write 7	WR2	32	Yes	No
10	WFSET	0x0A	Waveform Timing Setting	WR1	64	Yes	No
11	FMDISB	0x0B	Flash Memory Disable	WR1	1	Yes	No
12	SEGDLEN	0x0C	Seg Data Length	WR1	2	Yes	No
13	NEXTSDT	0x10	Next Segment Data	WR1	32	Yes	No
14	POWON	0x11	Power On	CMD	—	—	—
15	POWOFF	0x12	Power Off	CMD	—	—	—
16	EPDWR	0x13	EPD Write	CMD	—	—	—
17	EPDPCTL	0x20	EPD Back Plane Control	WR1	1	Yes	No
18	EPDDCTL	0x21	EPD Display Control	WR1	1	Yes	No
19	WFSEL	0x22	WaveForm Select	WR1	1	Yes	No
20	TEMPSENSON	0x23	Temperature Sensor Sensing On	CMD	—	—	—
21	POWCTL	0x24	Power Control	WR1	18	Yes	Yes
22	IOCTL	0x25	I/O Cell Control	WR1	1	Yes	Yes
23	SLVMODE	0x26	Slave mode	WR1	1	Yes	Yes
24	RDCOM	0x30	Read Command Address	WR1	1	Yes	No
25	RDSTATE	0x31	Read status	RD	3	Yes	No
26	Reserved	0x32	Detector2 Control	WR1	1	Yes	Yes
27	DROECTL	0x33	Driver Output Enable Control	WR1	2	Yes	Yes
28	SWRESET	0x4A	Software Reset	CMD	—	—	—

No. : Command No.
Name : Command name
Code : Command code
Description : Command description
Type : Command type
- CMD - A command type which controls operation by means of a command input
- WR1 - A command type which writes parameters that control operation
- WR2 - command type which writes parameters that control operation, and starts operation after the parameters have been input.
- RD - A command type which reads the internal status, for example.

P-Num : Parameter number (byte units)
P-Res : Parameter reset
- Yes - The parameters are reset to the default values during a power-on reset or a software reset.
- No - The parameters are not reset to the default values during a power-on reset or a software reset.

F-Mem : Parameters stored in the Flash memory
- Yes - Parameters can be stored.
- No - Parameters cannot be stored.

8.2 Command Details

8.2.1 CURSDT: 0x01

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
CURSDT	—	0	0	0	0	0	0	1	Current Segment Data
P1	B17	B16	B15	B14	B13	B12	B11	B10	CSEGDT[7:0]
P2	B27	B26	B25	B24	B23	B22	B21	B20	CSEGDT[15:8]
P3	B37	B36	B35	B34	B33	B32	B31	B30	CSEGDT[23:16]
P4	B47	B46	B45	B44	B43	B42	B41	B40	CSEGDT[31:24]
P5	B57	B56	B55	B54	B53	B52	B51	B50	CSEGDT[39:32]
P6	B67	B66	B65	B64	B63	B62	B61	B60	CSEGDT[47:40]
P7	B77	B76	B75	B74	B73	B72	B71	B70	CSEGDT[55:48]
P8	B87	B86	B85	B84	B83	B82	B81	B80	CSEGDT[63:56]
P9	B97	B96	B95	B94	B93	B92	B91	B90	CSEGDT[71:64]
P10	B107	B106	B105	B104	B103	B102	B101	B100	CSEGDT[79:72]
P11	B117	B116	B115	B114	B113	B112	B111	B110	CSEGDT[87:80]
P12	B127	B126	B125	B124	B123	B122	B121	B120	CSEGDT[95:88]
P13	B137	B136	B135	B134	B133	B132	B131	B130	CSEGDT[103:96]
P14	B147	B146	B145	B144	B143	B142	B141	B140	CSEGDT[111:104]
P15	B157	B156	B155	B154	B153	B152	B151	B150	CSEGDT[119:112]
P16	B167	B166	B165	B164	B163	B162	B161	B160	CSEGDT[127:120]
P17	B177	B176	B175	B174	B173	B172	B171	B170	CSEGDT[135:128]
P18	B187	B186	B185	B184	B183	B182	B181	B180	CSEGDT[143:136]
P19	B197	B196	B195	B194	B193	B192	B191	B190	CSEGDT[151:144]
P20	B207	B206	B205	B204	B203	B202	B201	B200	CSEGDT[159:152]
P21	B217	B216	B215	B214	B213	B212	B211	B210	CSEGDT[167:160]
P22	B227	B226	B225	B224	B223	B222	B221	B220	CSEGDT[175:168]
P23	B237	B236	B235	B234	B233	B232	B231	B230	CSEGDT[183:176]
P24	B247	B246	B245	B244	B243	B242	B241	B240	CSEGDT[191:184]
P25	B257	B256	B255	B254	B253	B252	B251	B250	CSEGDT[199:192]
P26	B267	B266	B265	B264	B263	B262	B261	B260	CSEGDT[207:200]
P27	B277	B276	B275	B274	B273	B272	B271	B270	CSEGDT[215:208]
P28	B287	B286	B285	B284	B283	B282	B281	B280	CSEGDT[223:216]
P29	B297	B296	B295	B294	B293	B292	B291	B290	CSEGDT[231:224]
P30	B307	B306	B305	B304	B303	B302	B301	B300	CSEGDT[239:232]
P31	B317	B316	B315	B314	B313	B312	B311	B310	CSEGDT[247:240]
P32	B327	B326	B325	B324	B323	B322	B321	B320	CSEGDT[255:248]

This command can be issued in any state other than during EPD display/update operations (refer to Section 7.7, “Status Transition”).

The first and last command parameter numbers to be issued can be set in the following command parameters:

- Setting for the first parameter number to be issued: Parameter B14-B10(SEGDSTAD[4:0]) of the SEGDLEN command
- Setting for the last parameter number to be issued: Parameter B24-B20(SEGDENDAD[4:0]) of the SEGDLEN command

Be sure to issue all the parameters up to the last parameter number specified by the B24-B20(SEGDENDAD[4:0]) parameter of the SEGDLEN command. For details on the SEGDLEN command, refer to Section 8.2.12, “SEGDLEN:0x0C”.

After setting the SEGDLEN command parameters, issue this command.

P1-P32 CSEGDT[255:0]: Current Segment Data (Default value: None)

This parameter stores the data of each segment that is currently displayed before EPD display/update operations are performed. The stored data is not reset by resetting the power-on status or the software.

If EPD display/update operations are first performed after V_{DD} power supply is turned on, a device that

controls this device needs to set the currently displayed data in this parameter. The currently displayed data must always be set before EPD display/update operations start. Otherwise, segment display waveforms cannot be guaranteed.

After EPD display/update operations have finished, display/update data for each segment is automatically stored. The currently displayed data need not to be set when the second or subsequent EPD display/update operations are performed after V_{DD} power supply is turned on.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0 or 0x2, black is displayed if 1 is written before the display update and white is displayed if 0. If the EPDDCTL command B13-B12 (DSPMOD) is 0x1 or 0x3, 0 is set for the parameter and white is displayed if 1 is written before the display update and 1 is set and black is displayed if 0.

Refer to Table 8.2.1 for the correspondence between CSEGDT[255:0] and segments.

Table 8.2.1 CSEGDT [255:0] applicable segment table

Bit	CSEGDT[23:0]	Applicable segment	Bit	CSEGDT[23:0]	Applicable segment
B10	CSEGDT[0]	ESEG0	B170	CSEGDT[128]	ESEG128
B11	CSEGDT[1]	ESEG1	B171	CSEGDT[129]	ESEG129
B12	CSEGDT[2]	ESEG2	B172	CSEGDT[130]	ESEG130
B13	CSEGDT[3]	ESEG3	B173	CSEGDT[131]	ESEG131
B14	CSEGDT[4]	ESEG4	B174	CSEGDT[132]	ESEG132
B15	CSEGDT[5]	ESEG5	B175	CSEGDT[133]	ESEG133
B16	CSEGDT[6]	ESEG6	B176	CSEGDT[134]	ESEG134
B17	CSEGDT[7]	ESEG7	B177	CSEGDT[135]	ESEG135
B20	CSEGDT[8]	ESEG8	B180	CSEGDT[136]	ESEG136
B21	CSEGDT[9]	ESEG9	B181	CSEGDT[137]	ESEG137
B22	CSEGDT[10]	ESEG10	B182	CSEGDT[138]	ESEG138
B23	CSEGDT[11]	ESEG11	B183	CSEGDT[139]	ESEG139
B24	CSEGDT[12]	ESEG12	B184	CSEGDT[140]	ESEG140
B25	CSEGDT[13]	ESEG13	B185	CSEGDT[141]	ESEG141
B26	CSEGDT[14]	ESEG14	B186	CSEGDT[142]	ESEG142
B27	CSEGDT[15]	ESEG15	B187	CSEGDT[143]	ESEG143
B30	CSEGDT[16]	ESEG16	B190	CSEGDT[144]	ESEG144
B31	CSEGDT[17]	ESEG17	B191	CSEGDT[145]	ESEG145
B32	CSEGDT[18]	ESEG18	B192	CSEGDT[146]	ESEG146
B33	CSEGDT[19]	ESEG19	B193	CSEGDT[147]	ESEG147
B34	CSEGDT[20]	ESEG20	B194	CSEGDT[148]	ESEG148
B35	CSEGDT[21]	ESEG21	B195	CSEGDT[149]	ESEG149
B36	CSEGDT[22]	ESEG22	B196	CSEGDT[150]	ESEG150
B37	CSEGDT[23]	ESEG23	B197	CSEGDT[151]	ESEG151
B40	CSEGDT[24]	ESEG24	B200	CSEGDT[152]	ESEG152
B41	CSEGDT[25]	ESEG25	B201	CSEGDT[153]	ESEG153
B42	CSEGDT[26]	ESEG26	B202	CSEGDT[154]	ESEG154
B43	CSEGDT[27]	ESEG27	B203	CSEGDT[155]	ESEG155
B44	CSEGDT[28]	ESEG28	B204	CSEGDT[156]	ESEG156
B45	CSEGDT[29]	ESEG29	B205	CSEGDT[157]	ESEG157
B46	CSEGDT[30]	ESEG30	B206	CSEGDT[158]	ESEG158
B47	CSEGDT[31]	ESEG31	B207	CSEGDT[159]	ESEG159
B50	CSEGDT[32]	ESEG32	B210	CSEGDT[160]	ESEG160
B51	CSEGDT[33]	ESEG33	B211	CSEGDT[161]	ESEG161
B52	CSEGDT[34]	ESEG34	B212	CSEGDT[162]	ESEG162
B53	CSEGDT[35]	ESEG35	B213	CSEGDT[163]	ESEG163
B54	CSEGDT[36]	ESEG36	B214	CSEGDT[164]	ESEG164
B55	CSEGDT[37]	ESEG37	B215	CSEGDT[165]	ESEG165
B56	CSEGDT[38]	ESEG38	B216	CSEGDT[166]	ESEG166
B57	CSEGDT[39]	ESEG39	B217	CSEGDT[167]	ESEG167
B60	CSEGDT[40]	ESEG40	B220	CSEGDT[168]	ESEG168
B61	CSEGDT[41]	ESEG41	B221	CSEGDT[169]	ESEG169
B62	CSEGDT[42]	ESEG42	B222	CSEGDT[170]	ESEG170
B63	CSEGDT[43]	ESEG43	B223	CSEGDT[171]	ESEG171
B64	CSEGDT[44]	ESEG44	B224	CSEGDT[172]	ESEG172
B65	CSEGDT[45]	ESEG45	B225	CSEGDT[173]	ESEG173

Bit	CSEGDT[23:0]	Applicable segment	Bit	CSEGDT[23:0]	Applicable segment
B66	CSEGDT[46]	ESEG46	B226	CSEGDT[174]	ESEG174
B67	CSEGDT[47]	ESEG47	B227	CSEGDT[175]	ESEG175
B70	CSEGDT[48]	ESEG48	B230	CSEGDT[176]	ESEG176
B71	CSEGDT[49]	ESEG49	B231	CSEGDT[177]	ESEG177
B72	CSEGDT[50]	ESEG50	B232	CSEGDT[178]	ESEG178
B73	CSEGDT[51]	ESEG51	B233	CSEGDT[179]	ESEG179
B74	CSEGDT[52]	ESEG52	B234	CSEGDT[180]	ESEG180
B75	CSEGDT[53]	ESEG53	B235	CSEGDT[181]	ESEG181
B76	CSEGDT[54]	ESEG54	B236	CSEGDT[182]	ESEG182
B77	CSEGDT[55]	ESEG55	B237	CSEGDT[183]	ESEG183
B80	CSEGDT[56]	ESEG56	B240	CSEGDT[184]	ESEG184
B81	CSEGDT[57]	ESEG57	B241	CSEGDT[185]	ESEG185
B82	CSEGDT[58]	ESEG58	B242	CSEGDT[186]	ESEG186
B83	CSEGDT[59]	ESEG59	B243	CSEGDT[187]	ESEG187
B84	CSEGDT[60]	ESEG60	B244	CSEGDT[188]	ESEG188
B85	CSEGDT[61]	ESEG61	B245	CSEGDT[189]	ESEG189
B86	CSEGDT[62]	ESEG62	B246	CSEGDT[190]	ESEG190
B87	CSEGDT[63]	ESEG63	B247	CSEGDT[191]	ESEG191
B90	CSEGDT[64]	ESEG64	B250	CSEGDT[192]	ESEG192
B91	CSEGDT[65]	ESEG65	B251	CSEGDT[193]	ESEG193
B92	CSEGDT[66]	ESEG66	B252	CSEGDT[194]	ESEG194
B93	CSEGDT[67]	ESEG67	B253	CSEGDT[195]	ESEG195
B94	CSEGDT[68]	ESEG68	B254	CSEGDT[196]	ESEG196
B95	CSEGDT[69]	ESEG69	B255	CSEGDT[197]	ESEG197
B96	CSEGDT[70]	ESEG70	B256	CSEGDT[198]	ESEG198
B97	CSEGDT[71]	ESEG71	B257	CSEGDT[199]	ESEG199
B100	CSEGDT[72]	ESEG72	B260	CSEGDT[200]	ESEG200
B101	CSEGDT[73]	ESEG73	B261	CSEGDT[201]	ESEG201
B102	CSEGDT[74]	ESEG74	B262	CSEGDT[202]	ESEG202
B103	CSEGDT[75]	ESEG75	B263	CSEGDT[203]	ESEG203
B104	CSEGDT[76]	ESEG76	B264	CSEGDT[204]	ESEG204
B105	CSEGDT[77]	ESEG77	B265	CSEGDT[205]	ESEG205
B106	CSEGDT[78]	ESEG78	B266	CSEGDT[206]	ESEG206
B107	CSEGDT[79]	ESEG79	B267	CSEGDT[207]	ESEG207
B110	CSEGDT[80]	ESEG80	B270	CSEGDT[208]	ESEG208
B111	CSEGDT[81]	ESEG81	B271	CSEGDT[209]	ESEG209
B112	CSEGDT[82]	ESEG82	B272	CSEGDT[210]	ESEG210
B113	CSEGDT[83]	ESEG83	B273	CSEGDT[211]	ESEG211
B114	CSEGDT[84]	ESEG84	B274	CSEGDT[212]	ESEG212
B115	CSEGDT[85]	ESEG85	B275	CSEGDT[213]	ESEG213
B116	CSEGDT[86]	ESEG86	B276	CSEGDT[214]	ESEG214
B117	CSEGDT[87]	ESEG87	B277	CSEGDT[215]	ESEG215
B120	CSEGDT[88]	ESEG88	B280	CSEGDT[216]	ESEG216
B121	CSEGDT[89]	ESEG89	B281	CSEGDT[217]	ESEG217
B122	CSEGDT[90]	ESEG90	B282	CSEGDT[218]	ESEG218
B123	CSEGDT[91]	ESEG91	B283	CSEGDT[219]	ESEG219
B124	CSEGDT[92]	ESEG92	B284	CSEGDT[220]	ESEG220
B125	CSEGDT[93]	ESEG93	B285	CSEGDT[221]	ESEG221
B126	CSEGDT[94]	ESEG94	B286	CSEGDT[222]	ESEG222
B127	CSEGDT[95]	ESEG95	B287	CSEGDT[223]	ESEG223
B130	CSEGDT[96]	ESEG96	B290	CSEGDT[224]	ESEG224
B131	CSEGDT[97]	ESEG97	B291	CSEGDT[225]	ESEG225
B132	CSEGDT[98]	ESEG98	B292	CSEGDT[226]	ESEG226
B133	CSEGDT[99]	ESEG99	B293	CSEGDT[227]	ESEG227
B134	CSEGDT[100]	ESEG100	B294	CSEGDT[228]	ESEG228
B135	CSEGDT[101]	ESEG101	B295	CSEGDT[229]	ESEG229
B136	CSEGDT[102]	ESEG102	B296	CSEGDT[230]	ESEG230
B137	CSEGDT[103]	ESEG103	B297	CSEGDT[231]	ESEG231
B140	CSEGDT[104]	ESEG104	B300	CSEGDT[232]	ESEG232
B141	CSEGDT[105]	ESEG105	B301	CSEGDT[233]	ESEG233
B142	CSEGDT[106]	ESEG106	B302	CSEGDT[234]	ESEG234
B143	CSEGDT[107]	ESEG107	B303	CSEGDT[235]	ESEG235
B144	CSEGDT[108]	ESEG108	B304	CSEGDT[236]	ESEG236

Bit	CSEGDT[23:0]	Applicable segment	Bit	CSEGDT[23:0]	Applicable segment
B145	CSEGDT[109]	ESEG109	B305	CSEGDT[237]	ESEG237
B146	CSEGDT[110]	ESEG110	B306	CSEGDT[238]	ESEG238
B147	CSEGDT[111]	ESEG111	B307	CSEGDT[239]	ESEG239
B150	CSEGDT[112]	ESEG112	B310	CSEGDT[240]	ESEG240
B151	CSEGDT[113]	ESEG113	B311	CSEGDT[241]	ESEG241
B152	CSEGDT[114]	ESEG114	B312	CSEGDT[242]	ESEG242
B153	CSEGDT[115]	ESEG115	B313	CSEGDT[243]	ESEG243
B154	CSEGDT[116]	ESEG116	B314	CSEGDT[244]	ESEG244
B155	CSEGDT[117]	ESEG117	B315	CSEGDT[245]	ESEG245
B156	CSEGDT[118]	ESEG118	B316	CSEGDT[246]	ESEG246
B157	CSEGDT[119]	ESEG119	B317	CSEGDT[247]	ESEG247
B160	CSEGDT[120]	ESEG120	B320	CSEGDT[248]	ESEG248
B161	CSEGDT[121]	ESEG121	B321	CSEGDT[249]	ESEG249
B162	CSEGDT[122]	ESEG122	B322	CSEGDT[250]	ESEG250
B163	CSEGDT[123]	ESEG123	B323	CSEGDT[251]	ESEG251
B164	CSEGDT[124]	ESEG124	B324	CSEGDT[252]	ESEG252
B165	CSEGDT[125]	ESEG125	B325	CSEGDT[253]	ESEG253
B166	CSEGDT[126]	ESEG126	B326	CSEGDT[254]	ESEG254
B167	CSEGDT[127]	ESEG127	B327	CSEGDT[255]	ESEG255

8.2.2 CURBDT: 0x02

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
CURBDT	—	0	0	0	0	0	1	0	Current Back Plane Data
P1	—	—	—	—	—	—	—	B10	CBPDT

This command can be issued in any state other than during EPD display/update operations (refer to Section 7.7, “Status Transition”).

B17-B11 Reserved

B10 CBPDT: Current Back Plane Data (Default value: None)

This parameter stores the data of each segment that is currently displayed before EPD display/update operations are performed. The stored data is not reset by resetting the power-on status or the software.

If EPD display/update operations are first performed after V_{DD} power supply is turned on, a device that controls this device needs to set the currently displayed data in this parameter. The currently displayed data must always be set before EPD display/update operations start. Otherwise, backplane display waveforms cannot be guaranteed.

After EPD display/update operations have finished, display/update data for each backplane is automatically stored. The currently displayed data need not to be set when the second or subsequent EPD display/update operations are performed after V_{DD} power supply is turned on.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0 or 0x2, black is displayed if 1 is written before the display update and white is displayed if 0. If the EPDDCTL command B13-B12 (DSPMOD) is 0x1 or 0x3, 0 is set for the parameter and white is displayed if 1 is written before the display update and 1 is set and black is displayed if 0.

8.2.3 ATEPDWR1: 0x03

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
ATEPDWR1	—	0	0	0	0	0	1	1	Auto EPD Write 1
P1	B17	B16	B15	B14	B13	B12	B11	B10	NSEGDT[7:0]
P2	B27	B26	B25	B24	B23	B22	B21	B20	NSEGDT[15:8]
P3	B37	B36	B35	B34	B33	B32	B31	B30	NSEGDT[23:16]
P4	B47	B46	B45	B44	B43	B42	B41	B40	NSEGDT[31:24]
P5	B57	B56	B55	B54	B53	B52	B51	B50	NSEGDT[39:32]
P6	B67	B66	B65	B64	B63	B62	B61	B60	NSEGDT[47:40]
P7	B77	B76	B75	B74	B73	B72	B71	B70	NSEGDT[55:48]
P8	B87	B86	B85	B84	B83	B82	B81	B80	NSEGDT[63:56]
P9	B97	B96	B95	B94	B93	B92	B91	B90	NSEGDT[71:64]
P10	B107	B106	B105	B104	B103	B102	B101	B100	NSEGDT[79:72]
P11	B117	B116	B115	B114	B113	B112	B111	B110	NSEGDT[87:80]
P12	B127	B126	B125	B124	B123	B122	B121	B120	NSEGDT[95:88]
P13	B137	B136	B135	B134	B133	B132	B131	B130	NSEGDT[103:96]
P14	B147	B146	B145	B144	B143	B142	B141	B140	NSEGDT[111:104]
P15	B157	B156	B155	B154	B153	B152	B151	B150	NSEGDT[119:112]
P16	B167	B166	B165	B164	B163	B162	B161	B160	NSEGDT[127:120]
P17	B177	B176	B175	B174	B173	B172	B171	B170	NSEGDT[135:128]
P18	B187	B186	B185	B184	B183	B182	B181	B180	NSEGDT[143:136]
P19	B197	B196	B195	B194	B193	B192	B191	B190	NSEGDT[151:144]
P20	B207	B206	B205	B204	B203	B202	B201	B200	NSEGDT[159:152]
P21	B217	B216	B215	B214	B213	B212	B211	B210	NSEGDT[167:160]
P22	B227	B226	B225	B224	B223	B222	B221	B220	NSEGDT[175:168]
P23	B237	B236	B235	B234	B233	B232	B231	B230	NSEGDT[183:176]
P24	B247	B246	B245	B244	B243	B242	B241	B240	NSEGDT[191:184]
P25	B257	B256	B255	B254	B253	B252	B251	B250	NSEGDT[199:192]
P26	B267	B266	B265	B264	B263	B262	B261	B260	NSEGDT[207:200]
P27	B277	B276	B275	B274	B273	B272	B271	B270	NSEGDT[215:208]
P28	B287	B286	B285	B284	B283	B282	B281	B280	NSEGDT[223:216]
P29	B297	B296	B295	B294	B293	B292	B291	B290	NSEGDT[231:224]
P30	B307	B306	B305	B304	B303	B302	B301	B300	NSEGDT[239:232]
P31	B317	B316	B315	B314	B313	B312	B311	B310	NSEGDT[247:240]
P32	B327	B326	B325	B324	B323	B322	B321	B320	NSEGDT[255:248]

If this command issues parameters until the following conditions are met, an automatic EPD display/update sequence (refer to Section 7.7.1, “Automatic EPD Display/Update Sequence”) will start.

- Setting for the first parameter number to be issued: Parameter B14-B10(SEGDSTAD[4:0]) of the SEGDLEN command
- Setting for the last parameter number to be issued: Parameter B24-B20(SEGDENDAD[4:0]) of the SEGDLEN command

For details on the SEGDLEN command, refer to Section 8.2.12, “SEGDLEN:0x0C”. After setting the SEGDLEN command, issue this command.

The display waveform memory used during EPD display/update operations will change with the following settings.

- FMDISB command parameter B10(FMDISB) : Refer to “8.2.11 FMDISB: 0x0B”.
- SLVSEL pin : Refer to “5.4 EPD_MCU Driver Expansion EPD Drive Pin Extension/Control Pin for a Multi-chip.”
- POWCTL command parameter B30(ATTEMPON) : Refer to “8.2.21 POWCTL: 0x24”.

The relationship between the above settings and the display waveforms is shown in Table 8.2.3.1.

Table 8.2.3.1 Display waveform memory selection table

FMDISB	SLVSEL pin	ATTEMPON	Status	Selected display waveform memory
1	—	—	When Flash memory is not used	WFSET (Command parameter)
0	1	—	When Flash memory is used In the case of the slave IC	Display waveform 1 (Flash memory)
0	0	0	When Flash memory is used In the case of the master IC When automatic temperature detection is OFF	Display waveform 1 (Flash memory)
0	0	1	When Flash memory is used In the case of the master IC When automatic temperature detection is ON	Selected from the result of automatic temperature detection (Flash memory)

This command can only be issued while in a standby state (refer to Section 7.7, “Status Transition”).

P1-P32 NSEGDT[255:0]: Next Segment Data

(Default value:0x0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000)

This parameter stores the display data for each segment that is subject to EPD display/update operations.

Each bit corresponds to one segment.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0, black is displayed if 1 is written, and white if 0.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x1, white is displayed if 1 is written, and black if 0.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x2, white is displayed regardless of whether 0 or 1 is written.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x3, black is displayed regardless of whether 0 or 1 is written.

For the correspondence between NSEGDT [255:0] and the segments, refer to Table 8.2.3.2.

Table 8.2.3.2 NSEGDT[255:0] applicable segment table

Bit	NSEGDT[23:0]	Applicable segment	Bit	NSEGDT[23:0]	Applicable segment
B10	NSEGDT[0]	ESEG0	B170	NSEGDT[128]	ESEG128
B11	NSEGDT[1]	ESEG1	B171	NSEGDT[129]	ESEG129
B12	NSEGDT[2]	ESEG2	B172	NSEGDT[130]	ESEG130
B13	NSEGDT[3]	ESEG3	B173	NSEGDT[131]	ESEG131
B14	NSEGDT[4]	ESEG4	B174	NSEGDT[132]	ESEG132
B15	NSEGDT[5]	ESEG5	B175	NSEGDT[133]	ESEG133
B16	NSEGDT[6]	ESEG6	B176	NSEGDT[134]	ESEG134
B17	NSEGDT[7]	ESEG7	B177	NSEGDT[135]	ESEG135
B20	NSEGDT[8]	ESEG8	B180	NSEGDT[136]	ESEG136
B21	NSEGDT[9]	ESEG9	B181	NSEGDT[137]	ESEG137
B22	NSEGDT[10]	ESEG10	B182	NSEGDT[138]	ESEG138
B23	NSEGDT[11]	ESEG11	B183	NSEGDT[139]	ESEG139
B24	NSEGDT[12]	ESEG12	B184	NSEGDT[140]	ESEG140
B25	NSEGDT[13]	ESEG13	B185	NSEGDT[141]	ESEG141
B26	NSEGDT[14]	ESEG14	B186	NSEGDT[142]	ESEG142
B27	NSEGDT[15]	ESEG15	B187	NSEGDT[143]	ESEG143
B30	NSEGDT[16]	ESEG16	B190	NSEGDT[144]	ESEG144
B31	NSEGDT[17]	ESEG17	B191	NSEGDT[145]	ESEG145
B32	NSEGDT[18]	ESEG18	B192	NSEGDT[146]	ESEG146
B33	NSEGDT[19]	ESEG19	B193	NSEGDT[147]	ESEG147
B34	NSEGDT[20]	ESEG20	B194	NSEGDT[148]	ESEG148
B35	NSEGDT[21]	ESEG21	B195	NSEGDT[149]	ESEG149
B36	NSEGDT[22]	ESEG22	B196	NSEGDT[150]	ESEG150
B37	NSEGDT[23]	ESEG23	B197	NSEGDT[151]	ESEG151
B40	NSEGDT[24]	ESEG24	B200	NSEGDT[152]	ESEG152

Bit	NSEGDT[23:0]	Applicable segment	Bit	NSEGDT[23:0]	Applicable segment
B41	NSEGDT[25]	ESEG25	B201	NSEGDT[153]	ESEG153
B42	NSEGDT[26]	ESEG26	B202	NSEGDT[154]	ESEG154
B43	NSEGDT[27]	ESEG27	B203	NSEGDT[155]	ESEG155
B44	NSEGDT[28]	ESEG28	B204	NSEGDT[156]	ESEG156
B45	NSEGDT[29]	ESEG29	B205	NSEGDT[157]	ESEG157
B46	NSEGDT[30]	ESEG30	B206	NSEGDT[158]	ESEG158
B47	NSEGDT[31]	ESEG31	B207	NSEGDT[159]	ESEG159
B50	NSEGDT[32]	ESEG32	B210	NSEGDT[160]	ESEG160
B51	NSEGDT[33]	ESEG33	B211	NSEGDT[161]	ESEG161
B52	NSEGDT[34]	ESEG34	B212	NSEGDT[162]	ESEG162
B53	NSEGDT[35]	ESEG35	B213	NSEGDT[163]	ESEG163
B54	NSEGDT[36]	ESEG36	B214	NSEGDT[164]	ESEG164
B55	NSEGDT[37]	ESEG37	B215	NSEGDT[165]	ESEG165
B56	NSEGDT[38]	ESEG38	B216	NSEGDT[166]	ESEG166
B57	NSEGDT[39]	ESEG39	B217	NSEGDT[167]	ESEG167
B60	NSEGDT[40]	ESEG40	B220	NSEGDT[168]	ESEG168
B61	NSEGDT[41]	ESEG41	B221	NSEGDT[169]	ESEG169
B62	NSEGDT[42]	ESEG42	B222	NSEGDT[170]	ESEG170
B63	NSEGDT[43]	ESEG43	B223	NSEGDT[171]	ESEG171
B64	NSEGDT[44]	ESEG44	B224	NSEGDT[172]	ESEG172
B65	NSEGDT[45]	ESEG45	B225	NSEGDT[173]	ESEG173
B66	NSEGDT[46]	ESEG46	B226	NSEGDT[174]	ESEG174
B67	NSEGDT[47]	ESEG47	B227	NSEGDT[175]	ESEG175
B70	NSEGDT[48]	ESEG48	B230	NSEGDT[176]	ESEG176
B71	NSEGDT[49]	ESEG49	B231	NSEGDT[177]	ESEG177
B72	NSEGDT[50]	ESEG50	B232	NSEGDT[178]	ESEG178
B73	NSEGDT[51]	ESEG51	B233	NSEGDT[179]	ESEG179
B74	NSEGDT[52]	ESEG52	B234	NSEGDT[180]	ESEG180
B75	NSEGDT[53]	ESEG53	B235	NSEGDT[181]	ESEG181
B76	NSEGDT[54]	ESEG54	B236	NSEGDT[182]	ESEG182
B77	NSEGDT[55]	ESEG55	B237	NSEGDT[183]	ESEG183
B80	NSEGDT[56]	ESEG56	B240	NSEGDT[184]	ESEG184
B81	NSEGDT[57]	ESEG57	B241	NSEGDT[185]	ESEG185
B82	NSEGDT[58]	ESEG58	B242	NSEGDT[186]	ESEG186
B83	NSEGDT[59]	ESEG59	B243	NSEGDT[187]	ESEG187
B84	NSEGDT[60]	ESEG60	B244	NSEGDT[188]	ESEG188
B85	NSEGDT[61]	ESEG61	B245	NSEGDT[189]	ESEG189
B86	NSEGDT[62]	ESEG62	B246	NSEGDT[190]	ESEG190
B87	NSEGDT[63]	ESEG63	B247	NSEGDT[191]	ESEG191
B90	NSEGDT[64]	ESEG64	B250	NSEGDT[192]	ESEG192
B91	NSEGDT[65]	ESEG65	B251	NSEGDT[193]	ESEG193
B92	NSEGDT[66]	ESEG66	B252	NSEGDT[194]	ESEG194
B93	NSEGDT[67]	ESEG67	B253	NSEGDT[195]	ESEG195
B94	NSEGDT[68]	ESEG68	B254	NSEGDT[196]	ESEG196
B95	NSEGDT[69]	ESEG69	B255	NSEGDT[197]	ESEG197
B96	NSEGDT[70]	ESEG70	B256	NSEGDT[198]	ESEG198
B97	NSEGDT[71]	ESEG71	B257	NSEGDT[199]	ESEG199
B100	NSEGDT[72]	ESEG72	B260	NSEGDT[200]	ESEG200
B101	NSEGDT[73]	ESEG73	B261	NSEGDT[201]	ESEG201
B102	NSEGDT[74]	ESEG74	B262	NSEGDT[202]	ESEG202
B103	NSEGDT[75]	ESEG75	B263	NSEGDT[203]	ESEG203
B104	NSEGDT[76]	ESEG76	B264	NSEGDT[204]	ESEG204
B105	NSEGDT[77]	ESEG77	B265	NSEGDT[205]	ESEG205
B106	NSEGDT[78]	ESEG78	B266	NSEGDT[206]	ESEG206
B107	NSEGDT[79]	ESEG79	B267	NSEGDT[207]	ESEG207
B110	NSEGDT[80]	ESEG80	B270	NSEGDT[208]	ESEG208
B111	NSEGDT[81]	ESEG81	B271	NSEGDT[209]	ESEG209
B112	NSEGDT[82]	ESEG82	B272	NSEGDT[210]	ESEG210
B113	NSEGDT[83]	ESEG83	B273	NSEGDT[211]	ESEG211
B114	NSEGDT[84]	ESEG84	B274	NSEGDT[212]	ESEG212
B115	NSEGDT[85]	ESEG85	B275	NSEGDT[213]	ESEG213
B116	NSEGDT[86]	ESEG86	B276	NSEGDT[214]	ESEG214
B117	NSEGDT[87]	ESEG87	B277	NSEGDT[215]	ESEG215

Bit	NSEGDT[23:0]	Applicable segment	Bit	NSEGDT[23:0]	Applicable segment
B120	NSEGDT[88]	ESEG88	B280	NSEGDT[216]	ESEG216
B121	NSEGDT[89]	ESEG89	B281	NSEGDT[217]	ESEG217
B122	NSEGDT[90]	ESEG90	B282	NSEGDT[218]	ESEG218
B123	NSEGDT[91]	ESEG91	B283	NSEGDT[219]	ESEG219
B124	NSEGDT[92]	ESEG92	B284	NSEGDT[220]	ESEG220
B125	NSEGDT[93]	ESEG93	B285	NSEGDT[221]	ESEG221
B126	NSEGDT[94]	ESEG94	B286	NSEGDT[222]	ESEG222
B127	NSEGDT[95]	ESEG95	B287	NSEGDT[223]	ESEG223
B130	NSEGDT[96]	ESEG96	B290	NSEGDT[224]	ESEG224
B131	NSEGDT[97]	ESEG97	B291	NSEGDT[225]	ESEG225
B132	NSEGDT[98]	ESEG98	B292	NSEGDT[226]	ESEG226
B133	NSEGDT[99]	ESEG99	B293	NSEGDT[227]	ESEG227
B134	NSEGDT[100]	ESEG100	B294	NSEGDT[228]	ESEG228
B135	NSEGDT[101]	ESEG101	B295	NSEGDT[229]	ESEG229
B136	NSEGDT[102]	ESEG102	B296	NSEGDT[230]	ESEG230
B137	NSEGDT[103]	ESEG103	B297	NSEGDT[231]	ESEG231
B140	NSEGDT[104]	ESEG104	B300	NSEGDT[232]	ESEG232
B141	NSEGDT[105]	ESEG105	B301	NSEGDT[233]	ESEG233
B142	NSEGDT[106]	ESEG106	B302	NSEGDT[234]	ESEG234
B143	NSEGDT[107]	ESEG107	B303	NSEGDT[235]	ESEG235
B144	NSEGDT[108]	ESEG108	B304	NSEGDT[236]	ESEG236
B145	NSEGDT[109]	ESEG109	B305	NSEGDT[237]	ESEG237
B146	NSEGDT[110]	ESEG110	B306	NSEGDT[238]	ESEG238
B147	NSEGDT[111]	ESEG111	B307	NSEGDT[239]	ESEG239
B150	NSEGDT[112]	ESEG112	B310	NSEGDT[240]	ESEG240
B151	NSEGDT[113]	ESEG113	B311	NSEGDT[241]	ESEG241
B152	NSEGDT[114]	ESEG114	B312	NSEGDT[242]	ESEG242
B153	NSEGDT[115]	ESEG115	B313	NSEGDT[243]	ESEG243
B154	NSEGDT[116]	ESEG116	B314	NSEGDT[244]	ESEG244
B155	NSEGDT[117]	ESEG117	B315	NSEGDT[245]	ESEG245
B156	NSEGDT[118]	ESEG118	B316	NSEGDT[246]	ESEG246
B157	NSEGDT[119]	ESEG119	B317	NSEGDT[247]	ESEG247
B160	NSEGDT[120]	ESEG120	B320	NSEGDT[248]	ESEG248
B161	NSEGDT[121]	ESEG121	B321	NSEGDT[249]	ESEG249
B162	NSEGDT[122]	ESEG122	B322	NSEGDT[250]	ESEG250
B163	NSEGDT[123]	ESEG123	B323	NSEGDT[251]	ESEG251
B164	NSEGDT[124]	ESEG124	B324	NSEGDT[252]	ESEG252
B165	NSEGDT[125]	ESEG125	B325	NSEGDT[253]	ESEG253
B166	NSEGDT[126]	ESEG126	B326	NSEGDT[254]	ESEG254
B167	NSEGDT[127]	ESEG127	B327	NSEGDT[255]	ESEG255

8.2.4 ATEPDWR2: 0x04

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
ATEPDWR2	—	0	0	0	0	1	0	0	Auto EPD Write 2
P1	B17	B16	B15	B14	B13	B12	B11	B10	NSEGDT[7:0]
P2	B27	B26	B25	B24	B23	B22	B21	B20	NSEGDT[15:8]
P3	B37	B36	B35	B34	B33	B32	B31	B30	NSEGDT[23:16]
P4	B47	B46	B45	B44	B43	B42	B41	B40	NSEGDT[31:24]
P5	B57	B56	B55	B54	B53	B52	B51	B50	NSEGDT[39:32]
P6	B67	B66	B65	B64	B63	B62	B61	B60	NSEGDT[47:40]
P7	B77	B76	B75	B74	B73	B72	B71	B70	NSEGDT[55:48]
P8	B87	B86	B85	B84	B83	B82	B81	B80	NSEGDT[63:56]
P9	B97	B96	B95	B94	B93	B92	B91	B90	NSEGDT[71:64]
P10	B107	B106	B105	B104	B103	B102	B101	B100	NSEGDT[79:72]
P11	B117	B116	B115	B114	B113	B112	B111	B110	NSEGDT[87:80]
P12	B127	B126	B125	B124	B123	B122	B121	B120	NSEGDT[95:88]
P13	B137	B136	B135	B134	B133	B132	B131	B130	NSEGDT[103:96]
P14	B147	B146	B145	B144	B143	B142	B141	B140	NSEGDT[111:104]
P15	B157	B156	B155	B154	B153	B152	B151	B150	NSEGDT[119:112]
P16	B167	B166	B165	B164	B163	B162	B161	B160	NSEGDT[127:120]
P17	B177	B176	B175	B174	B173	B172	B171	B170	NSEGDT[135:128]
P18	B187	B186	B185	B184	B183	B182	B181	B180	NSEGDT[143:136]
P19	B197	B196	B195	B194	B193	B192	B191	B190	NSEGDT[151:144]
P20	B207	B206	B205	B204	B203	B202	B201	B200	NSEGDT[159:152]
P21	B217	B216	B215	B214	B213	B212	B211	B210	NSEGDT[167:160]
P22	B227	B226	B225	B224	B223	B222	B221	B220	NSEGDT[175:168]
P23	B237	B236	B235	B234	B233	B232	B231	B230	NSEGDT[183:176]
P24	B247	B246	B245	B244	B243	B242	B241	B240	NSEGDT[191:184]
P25	B257	B256	B255	B254	B253	B252	B251	B250	NSEGDT[199:192]
P26	B267	B266	B265	B264	B263	B262	B261	B260	NSEGDT[207:200]
P27	B277	B276	B275	B274	B273	B272	B271	B270	NSEGDT[215:208]
P28	B287	B286	B285	B284	B283	B282	B281	B280	NSEGDT[223:216]
P29	B297	B296	B295	B294	B293	B292	B291	B290	NSEGDT[231:224]
P30	B307	B306	B305	B304	B303	B302	B301	B300	NSEGDT[239:232]
P31	B317	B316	B315	B314	B313	B312	B311	B310	NSEGDT[247:240]
P32	B327	B326	B325	B324	B323	B322	B321	B320	NSEGDT[255:248]

If this command issues parameters until the following conditions are met, an automatic EPD display/update sequence (refer to Section 7.7.1, “Automatic EPD Display/Update Sequence”) will start.

- Setting for the first parameter number to be issued: Parameter B14-B10(SEGDSTAD[4:0]) of the SEGDLEN command
- Setting for the last parameter number to be issued: Parameter B24-B20(SEGDENDAD[4:0]) of the SEGDLEN command

For details on the SEGDLEN command, refer to Section 8.2.12, “SEGDLEN:0x0C”. After setting the SEGDLEN command, issue this command.

The display waveform memory which is used when the display is being updated changes according to the settings shown below.

- FMDISB command parameter B10(FMDISB) : Refer to “8.2.11 FMDISB: 0x0B”.
- SLVSEL pin : Refer to “5.4 EPD_MCU Driver Expansion EPD Drive Pin Extension/Control Pin for a Multi-chip.”
- POWCTL command parameter B30(ATTEMPON) : Refer to “8.2.21 POWCTL: 0x24”.

The relationship between the above settings and the display waveforms is shown in Table 8.2.4.

Table 8.2.4 Display waveform memory selection table

FMDISB	SLVSEL pin	ATTEMPON	Status	Selected display waveform memory
1	—	—	When Flash memory is not used	WFSET (Command parameter)
0	1	—	When Flash memory is used In the case of the slave IC	Display waveform 2 (Flash memory)
0	0	0	When Flash memory is used In the case of the master IC When automatic temperature detection is OFF	Display waveform 2 (Flash memory)
0	0	1	When Flash memory is used In the case of the master IC When automatic temperature detection is ON	Selected from the result of automatic temperature detection (Flash memory)

This command can only be issued while in a standby state (refer to Section 7.7, “Status Transition”).

P1-P32 NSEGDT[255:0]: Next Segment Data

(Default value:0x0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000)

This parameter stores the display data for each segment that is subject to EPD display/update operations.

Each bit corresponds to one segment.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0, black is displayed if 1 is written, and white if 0.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x1, white is displayed if 1 is written, and black if 0.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x2, white is displayed regardless of whether 0 or 1 is written.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x3, black is displayed regardless of whether 0 or 1 is written.

For the correspondence between NSEGDT[255:0] and the segments, refer to Table 8.2.3.2.

8.2.5 ATEPDWR3: 0x05

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
ATEPDWR3	—	0	0	0	0	1	0	1	Auto EPD Write 3
P1	B17	B16	B15	B14	B13	B12	B11	B10	NSEGDT[7:0]
P2	B27	B26	B25	B24	B23	B22	B21	B20	NSEGDT[15:8]
P3	B37	B36	B35	B34	B33	B32	B31	B30	NSEGDT[23:16]
P4	B47	B46	B45	B44	B43	B42	B41	B40	NSEGDT[31:24]
P5	B57	B56	B55	B54	B53	B52	B51	B50	NSEGDT[39:32]
P6	B67	B66	B65	B64	B63	B62	B61	B60	NSEGDT[47:40]
P7	B77	B76	B75	B74	B73	B72	B71	B70	NSEGDT[55:48]
P8	B87	B86	B85	B84	B83	B82	B81	B80	NSEGDT[63:56]
P9	B97	B96	B95	B94	B93	B92	B91	B90	NSEGDT[71:64]
P10	B107	B106	B105	B104	B103	B102	B101	B100	NSEGDT[79:72]
P11	B117	B116	B115	B114	B113	B112	B111	B110	NSEGDT[87:80]
P12	B127	B126	B125	B124	B123	B122	B121	B120	NSEGDT[95:88]
P13	B137	B136	B135	B134	B133	B132	B131	B130	NSEGDT[103:96]
P14	B147	B146	B145	B144	B143	B142	B141	B140	NSEGDT[111:104]
P15	B157	B156	B155	B154	B153	B152	B151	B150	NSEGDT[119:112]
P16	B167	B166	B165	B164	B163	B162	B161	B160	NSEGDT[127:120]
P17	B177	B176	B175	B174	B173	B172	B171	B170	NSEGDT[135:128]
P18	B187	B186	B185	B184	B183	B182	B181	B180	NSEGDT[143:136]
P19	B197	B196	B195	B194	B193	B192	B191	B190	NSEGDT[151:144]
P20	B207	B206	B205	B204	B203	B202	B201	B200	NSEGDT[159:152]
P21	B217	B216	B215	B214	B213	B212	B211	B210	NSEGDT[167:160]
P22	B227	B226	B225	B224	B223	B222	B221	B220	NSEGDT[175:168]
P23	B237	B236	B235	B234	B233	B232	B231	B230	NSEGDT[183:176]
P24	B247	B246	B245	B244	B243	B242	B241	B240	NSEGDT[191:184]
P25	B257	B256	B255	B254	B253	B252	B251	B250	NSEGDT[199:192]
P26	B267	B266	B265	B264	B263	B262	B261	B260	NSEGDT[207:200]
P27	B277	B276	B275	B274	B273	B272	B271	B270	NSEGDT[215:208]
P28	B287	B286	B285	B284	B283	B282	B281	B280	NSEGDT[223:216]
P29	B297	B296	B295	B294	B293	B292	B291	B290	NSEGDT[231:224]
P30	B307	B306	B305	B304	B303	B302	B301	B300	NSEGDT[239:232]
P31	B317	B316	B315	B314	B313	B312	B311	B310	NSEGDT[247:240]
P32	B327	B326	B325	B324	B323	B322	B321	B320	NSEGDT[255:248]

If this command issues parameters until the following conditions are met, an automatic EPD display/update sequence (refer to Section 7.7.1, “Automatic EPD Display/Update Sequence”) will start.

- Setting for the first parameter number to be issued: Parameter B14-B10(SEGDSTAD[4:0]) of the SEGDLEN command
- Setting for the last parameter number to be issued: Parameter B24-B20(SEGDENDAD[4:0]) of the SEGDLEN command

For details on the SEGDLEN command, refer to Section 8.2.12, “SEGDLEN:0x0C”. After setting the SEGDLEN command, issue this command.

The display waveform memory used during EPD display/update operations will change with the following settings.

- FMDISB command parameter B10(FMDISB) : Refer to “8.2.11 FMDISB: 0x0B”.
- SLVSEL pin : Refer to “5.4 EPD_MCU Driver Expansion EPD Drive Pin Extension/Control Pin for a Multi-chip.”
- POWCTL command parameter B30(ATTEMPON) : Refer to “8.2.21 POWCTL: 0x24”.

The relationship between the above settings and the display waveforms is shown in Table 8.2.5.

Table 8.2.5 Display waveform memory selection table

FMDISB	SLVSEL pin	ATTEMPON	Status	Selected display waveform memory
1	—	—	When Flash memory is not used	WFSET (Command parameter)
0	1	—	When Flash memory is used In the case of the slave IC	Display waveform 3 (Flash memory)
0	0	0	When Flash memory is used In the case of the master IC When automatic temperature detection is OFF	Display waveform 3 (Flash memory)
0	0	1	When Flash memory is used In the case of the master IC When automatic temperature detection is ON	Selected from the result of automatic temperature detection (Flash memory)

This command can be issued only when the system is in a standby status (Refer to “7.7 Status Transition”).

P1-P32 NSEGDT[255:0]: Next Segment Data

(Default value:0x0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000)

This parameter stores the display data for each segment that is subject to EPD display/update operations.

Each bit corresponds to one segment.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0, black is displayed if 1 is written, and white if 0.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x1, white is displayed if 1 is written, and black if 0.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x2, white is displayed regardless of whether 0 or 1 is written.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x3, black is displayed regardless of whether 0 or 1 is written.

For the correspondence between NSEGDT[255:0] and the segments, refer to Table 8.2.3.2.

8.2.6 ATEPDWR4: 0x06

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
ATEPDWR4	—	0	0	0	0	1	1	0	Auto EPD Write 4
P1	B17	B16	B15	B14	B13	B12	B11	B10	NSEGDT[7:0]
P2	B27	B26	B25	B24	B23	B22	B21	B20	NSEGDT[15:8]
P3	B37	B36	B35	B34	B33	B32	B31	B30	NSEGDT[23:16]
P4	B47	B46	B45	B44	B43	B42	B41	B40	NSEGDT[31:24]
P5	B57	B56	B55	B54	B53	B52	B51	B50	NSEGDT[39:32]
P6	B67	B66	B65	B64	B63	B62	B61	B60	NSEGDT[47:40]
P7	B77	B76	B75	B74	B73	B72	B71	B70	NSEGDT[55:48]
P8	B87	B86	B85	B84	B83	B82	B81	B80	NSEGDT[63:56]
P9	B97	B96	B95	B94	B93	B92	B91	B90	NSEGDT[71:64]
P10	B107	B106	B105	B104	B103	B102	B101	B100	NSEGDT[79:72]
P11	B117	B116	B115	B114	B113	B112	B111	B110	NSEGDT[87:80]
P12	B127	B126	B125	B124	B123	B122	B121	B120	NSEGDT[95:88]
P13	B137	B136	B135	B134	B133	B132	B131	B130	NSEGDT[103:96]
P14	B147	B146	B145	B144	B143	B142	B141	B140	NSEGDT[111:104]
P15	B157	B156	B155	B154	B153	B152	B151	B150	NSEGDT[119:112]
P16	B167	B166	B165	B164	B163	B162	B161	B160	NSEGDT[127:120]
P17	B177	B176	B175	B174	B173	B172	B171	B170	NSEGDT[135:128]
P18	B187	B186	B185	B184	B183	B182	B181	B180	NSEGDT[143:136]
P19	B197	B196	B195	B194	B193	B192	B191	B190	NSEGDT[151:144]
P20	B207	B206	B205	B204	B203	B202	B201	B200	NSEGDT[159:152]
P21	B217	B216	B215	B214	B213	B212	B211	B210	NSEGDT[167:160]
P22	B227	B226	B225	B224	B223	B222	B221	B220	NSEGDT[175:168]
P23	B237	B236	B235	B234	B233	B232	B231	B230	NSEGDT[183:176]
P24	B247	B246	B245	B244	B243	B242	B241	B240	NSEGDT[191:184]
P25	B257	B256	B255	B254	B253	B252	B251	B250	NSEGDT[199:192]
P26	B267	B266	B265	B264	B263	B262	B261	B260	NSEGDT[207:200]
P27	B277	B276	B275	B274	B273	B272	B271	B270	NSEGDT[215:208]
P28	B287	B286	B285	B284	B283	B282	B281	B280	NSEGDT[223:216]
P29	B297	B296	B295	B294	B293	B292	B291	B290	NSEGDT[231:224]
P30	B307	B306	B305	B304	B303	B302	B301	B300	NSEGDT[239:232]
P31	B317	B316	B315	B314	B313	B312	B311	B310	NSEGDT[247:240]
P32	B327	B326	B325	B324	B323	B322	B321	B320	NSEGDT[255:248]

If this command issues parameters until the following conditions are met, an automatic EPD display/update sequence (refer to Section 7.7.1, “Automatic EPD Display/Update Sequence”) will start.

- Setting for the first parameter number to be issued: Parameter B14-B10(SEGDSTAD[4:0]) of the SEGDLEN command
- Setting for the last parameter number to be issued: Parameter B24-B20(SEGDENDAD[4:0]) of the SEGDLEN command

For details on the SEGDLEN command, refer to Section 8.2.12, “SEGDLEN:0x0C”. After setting the SEGDLEN command, issue this command.

The display waveform memory which is used when the display is being updated changes according to the settings shown below.

- FMDISB command parameter B10(FMDISB) : Refer to “8.2.11 FMDISB: 0x0B”.
- SLVSEL pin : Refer to “5.4 EPD_MCU Driver Expansion EPD Drive Pin Extension/Control Pin for a Multi-chip.”
- POWCTL command parameter B30(ATTEMPON) : Refer to “8.2.21 POWCTL: 0x24”.

The relationship between the above settings and the display waveforms is shown in Table 8.2.6.

Table 8.2.6 Display waveform memory selection table

FMDISB	SLVSEL pin	ATTEMPON	Status	Selected display waveform memory
1	—	—	When Flash memory is not used	WFSET (Command parameter)
0	1	—	When Flash memory is used In the case of the slave IC	Display waveform 4 (Flash memory)
0	0	0	When Flash memory is used In the case of the master IC When automatic temperature detection is OFF	Display waveform 4 (Flash memory)
0	0	1	When Flash memory is used In the case of the master IC When automatic temperature detection is ON	Selected from the result of automatic temperature detection (Flash memory)

This command can only be issued while in a standby state (refer to Section 7.7, “Status Transition”).

P1-P32 NSEGDT[255:0]: Next Segment Data

(Default value:0x0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000)

This parameter stores the display data for each segment that is subject to EPD display/update operations.

Each bit corresponds to one segment.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0, black is displayed if 1 is written, and white if 0.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x1, white is displayed if 1 is written, and black if 0.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x2, white is displayed regardless of whether 0 or 1 is written.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x3, black is displayed regardless of whether 0 or 1 is written.

For the correspondence between NSEGDT [255:0] and the segments, refer to Table 8.2.3.2.

8.2.7 ATEPDWR5: 0x07

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
ATEPDWR5	—	0	0	0	0	1	1	1	Auto EPD Write 5
P1	B17	B16	B15	B14	B13	B12	B11	B10	NSEGDT[7:0]
P2	B27	B26	B25	B24	B23	B22	B21	B20	NSEGDT[15:8]
P3	B37	B36	B35	B34	B33	B32	B31	B30	NSEGDT[23:16]
P4	B47	B46	B45	B44	B43	B42	B41	B40	NSEGDT[31:24]
P5	B57	B56	B55	B54	B53	B52	B51	B50	NSEGDT[39:32]
P6	B67	B66	B65	B64	B63	B62	B61	B60	NSEGDT[47:40]
P7	B77	B76	B75	B74	B73	B72	B71	B70	NSEGDT[55:48]
P8	B87	B86	B85	B84	B83	B82	B81	B80	NSEGDT[63:56]
P9	B97	B96	B95	B94	B93	B92	B91	B90	NSEGDT[71:64]
P10	B107	B106	B105	B104	B103	B102	B101	B100	NSEGDT[79:72]
P11	B117	B116	B115	B114	B113	B112	B111	B110	NSEGDT[87:80]
P12	B127	B126	B125	B124	B123	B122	B121	B120	NSEGDT[95:88]
P13	B137	B136	B135	B134	B133	B132	B131	B130	NSEGDT[103:96]
P14	B147	B146	B145	B144	B143	B142	B141	B140	NSEGDT[111:104]
P15	B157	B156	B155	B154	B153	B152	B151	B150	NSEGDT[119:112]
P16	B167	B166	B165	B164	B163	B162	B161	B160	NSEGDT[127:120]
P17	B177	B176	B175	B174	B173	B172	B171	B170	NSEGDT[135:128]
P18	B187	B186	B185	B184	B183	B182	B181	B180	NSEGDT[143:136]
P19	B197	B196	B195	B194	B193	B192	B191	B190	NSEGDT[151:144]
P20	B207	B206	B205	B204	B203	B202	B201	B200	NSEGDT[159:152]
P21	B217	B216	B215	B214	B213	B212	B211	B210	NSEGDT[167:160]
P22	B227	B226	B225	B224	B223	B222	B221	B220	NSEGDT[175:168]
P23	B237	B236	B235	B234	B233	B232	B231	B230	NSEGDT[183:176]
P24	B247	B246	B245	B244	B243	B242	B241	B240	NSEGDT[191:184]
P25	B257	B256	B255	B254	B253	B252	B251	B250	NSEGDT[199:192]
P26	B267	B266	B265	B264	B263	B262	B261	B260	NSEGDT[207:200]
P27	B277	B276	B275	B274	B273	B272	B271	B270	NSEGDT[215:208]
P28	B287	B286	B285	B284	B283	B282	B281	B280	NSEGDT[223:216]
P29	B297	B296	B295	B294	B293	B292	B291	B290	NSEGDT[231:224]
P30	B307	B306	B305	B304	B303	B302	B301	B300	NSEGDT[239:232]
P31	B317	B316	B315	B314	B313	B312	B311	B310	NSEGDT[247:240]
P32	B327	B326	B325	B324	B323	B322	B321	B320	NSEGDT[255:248]

If this command issues parameters until the following conditions are met, an automatic EPD display/update sequence (refer to Section 7.7.1, “Automatic EPD Display/Update Sequence”) will start.

- Setting for the first parameter number to be issued: Parameter B14-B10(SEGDSTAD[4:0]) of the SEGDLEN command
- Setting for the last parameter number to be issued: Parameter B24-B20(SEGDENDAD[4:0]) of the SEGDLEN command

For details on the SEGDLEN command, refer to Section 8.2.12, “SEGDLEN:0x0C”. After setting the SEGDLEN command, issue this command.

The display waveform memory used during EPD display/update operations will change with the following settings.

- FMDISB command parameter B10(FMDISB) : Refer to “8.2.11 FMDISB: 0x0B”.
- SLVSEL pin : Refer to “5.4 EPD_MCU Driver Expansion EPD Drive Pin Extension/Control Pin for a Multi-chip.”
- POWCTL command parameter B30(ATTEMPON) : Refer to “8.2.21 POWCTL: 0x24”.

The relationship between the above settings and the display waveforms is shown in Table 8.2.7.

Table 8.2.7 Display waveform memory selection table

FMDISB	SLVSEL pin	ATTEMPON	Status	Selected display waveform memory
1	—	—	When Flash memory is not used	WFSET (Command parameter)
0	1	—	When Flash memory is used In the case of the slave IC	Display waveform 5 (Flash memory)
0	0	0	When Flash memory is used In the case of the master IC When automatic temperature detection is OFF	Display waveform 5 (Flash memory)
0	0	1	When Flash memory is used In the case of the master IC When automatic temperature detection is ON	Selected from the result of automatic temperature detection (Flash memory)

This command can only be issued while in a standby state (refer to Section 7.7, “Status Transition”).

P1-P32 NSEGDT[255:0]: Next Segment Data

(Default value:0x0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000)

This parameter stores the display data for each segment that is subject to EPD display/update operations.

Each bit corresponds to one segment.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0, black is displayed if 1 is written, and white if 0.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x1, white is displayed if 1 is written, and black if 0.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x2, white is displayed regardless of whether 0 or 1 is written.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x3, black is displayed regardless of whether 0 or 1 is written.

For the correspondence between NSEGDT [255:0] and the segments, refer to Table 8.2.3.2.

8.2.8 ATEPDWR6: 0x08

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
ATEPDWR6	—	0	0	0	1	0	0	0	Auto EPD Write 6
P1	B17	B16	B15	B14	B13	B12	B11	B10	NSEGDT[7:0]
P2	B27	B26	B25	B24	B23	B22	B21	B20	NSEGDT[15:8]
P3	B37	B36	B35	B34	B33	B32	B31	B30	NSEGDT[23:16]
P4	B47	B46	B45	B44	B43	B42	B41	B40	NSEGDT[31:24]
P5	B57	B56	B55	B54	B53	B52	B51	B50	NSEGDT[39:32]
P6	B67	B66	B65	B64	B63	B62	B61	B60	NSEGDT[47:40]
P7	B77	B76	B75	B74	B73	B72	B71	B70	NSEGDT[55:48]
P8	B87	B86	B85	B84	B83	B82	B81	B80	NSEGDT[63:56]
P9	B97	B96	B95	B94	B93	B92	B91	B90	NSEGDT[71:64]
P10	B107	B106	B105	B104	B103	B102	B101	B100	NSEGDT[79:72]
P11	B117	B116	B115	B114	B113	B112	B111	B110	NSEGDT[87:80]
P12	B127	B126	B125	B124	B123	B122	B121	B120	NSEGDT[95:88]
P13	B137	B136	B135	B134	B133	B132	B131	B130	NSEGDT[103:96]
P14	B147	B146	B145	B144	B143	B142	B141	B140	NSEGDT[111:104]
P15	B157	B156	B155	B154	B153	B152	B151	B150	NSEGDT[119:112]
P16	B167	B166	B165	B164	B163	B162	B161	B160	NSEGDT[127:120]
P17	B177	B176	B175	B174	B173	B172	B171	B170	NSEGDT[135:128]
P18	B187	B186	B185	B184	B183	B182	B181	B180	NSEGDT[143:136]
P19	B197	B196	B195	B194	B193	B192	B191	B190	NSEGDT[151:144]
P20	B207	B206	B205	B204	B203	B202	B201	B200	NSEGDT[159:152]
P21	B217	B216	B215	B214	B213	B212	B211	B210	NSEGDT[167:160]
P22	B227	B226	B225	B224	B223	B222	B221	B220	NSEGDT[175:168]
P23	B237	B236	B235	B234	B233	B232	B231	B230	NSEGDT[183:176]
P24	B247	B246	B245	B244	B243	B242	B241	B240	NSEGDT[191:184]
P25	B257	B256	B255	B254	B253	B252	B251	B250	NSEGDT[199:192]
P26	B267	B266	B265	B264	B263	B262	B261	B260	NSEGDT[207:200]
P27	B277	B276	B275	B274	B273	B272	B271	B270	NSEGDT[215:208]
P28	B287	B286	B285	B284	B283	B282	B281	B280	NSEGDT[223:216]
P29	B297	B296	B295	B294	B293	B292	B291	B290	NSEGDT[231:224]
P30	B307	B306	B305	B304	B303	B302	B301	B300	NSEGDT[239:232]
P31	B317	B316	B315	B314	B313	B312	B311	B310	NSEGDT[247:240]
P32	B327	B326	B325	B324	B323	B322	B321	B320	NSEGDT[255:248]

If this command issues parameters until the following conditions are met, an automatic EPD display/update sequence (refer to Section 7.7.1, “Automatic EPD Display/Update Sequence”) will start.

- Setting for the first parameter number to be issued: Parameter B14-B10(SEGDSTAD[4:0]) of the SEGDLEN command
- Setting for the last parameter number to be issued: Parameter B24-B20(SEGDENDAD[4:0]) of the SEGDLEN command

For details on the SEGDLEN command, refer to Section 8.2.12, “SEGDLEN:0x0C”. After setting the SEGDLEN command, issue this command.

The display waveform memory used during EPD display/update operations will change with the following settings.

- FMDISB command parameter B10(FMDISB) : Refer to “8.2.11 FMDISB: 0x0B”.
- SLVSEL pin : Refer to “5.4 EPD_MCU Driver Expansion EPD Drive Pin Extension/Control Pin for a Multi-chip.”
- POWCTL command parameter B30(ATTEMPON) : Refer to “8.2.21 POWCTL: 0x24”.

The relationship between the above settings and the display waveforms is shown in Table 8.2.8.

Table 8.2.8 Display waveform memory selection table

FMDISB	SLVSEL pin	ATTEMPON	Status	Selected display waveform memory
1	—	—	When Flash memory is not used	WFSET (Command parameter)
0	1	—	When Flash memory is used In the case of the slave IC	Display waveform 6 (Flash memory)
0	0	0	When Flash memory is used In the case of the master IC When automatic temperature detection is OFF	Display waveform 6 (Flash memory)
0	0	1	When Flash memory is used In the case of the master IC When automatic temperature detection is ON	Selected from the result of automatic temperature detection (Flash memory)

This command can only be issued while in a standby state (refer to Section 7.7, “Status Transition”).

P1-P32 NSEGDT[255:0]: Next Segment Data

(Default value:0x0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000)

This parameter stores the display data for each segment that is subject to EPD display/update operations.

Each bit corresponds to one segment.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0, black is displayed if 1 is written, and white if 0.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x1, white is displayed if 1 is written, and black if 0.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x2, white is displayed regardless of whether 0 or 1 is written.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x3, black is displayed regardless of whether 0 or 1 is written.

For the correspondence between NSEGDT [255:0] and the segments, refer to Table 8.2.3.2.

8.2.9 ATEPDWR7: 0x09

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
ATEPDWR7	—	0	0	0	1	0	0	1	Auto EPD Write 7
P1	B17	B16	B15	B14	B13	B12	B11	B10	NSEGDT[7:0]
P2	B27	B26	B25	B24	B23	B22	B21	B20	NSEGDT[15:8]
P3	B37	B36	B35	B34	B33	B32	B31	B30	NSEGDT[23:16]
P4	B47	B46	B45	B44	B43	B42	B41	B40	NSEGDT[31:24]
P5	B57	B56	B55	B54	B53	B52	B51	B50	NSEGDT[39:32]
P6	B67	B66	B65	B64	B63	B62	B61	B60	NSEGDT[47:40]
P7	B77	B76	B75	B74	B73	B72	B71	B70	NSEGDT[55:48]
P8	B87	B86	B85	B84	B83	B82	B81	B80	NSEGDT[63:56]
P9	B97	B96	B95	B94	B93	B92	B91	B90	NSEGDT[71:64]
P10	B107	B106	B105	B104	B103	B102	B101	B100	NSEGDT[79:72]
P11	B117	B116	B115	B114	B113	B112	B111	B110	NSEGDT[87:80]
P12	B127	B126	B125	B124	B123	B122	B121	B120	NSEGDT[95:88]
P13	B137	B136	B135	B134	B133	B132	B131	B130	NSEGDT[103:96]
P14	B147	B146	B145	B144	B143	B142	B141	B140	NSEGDT[111:104]
P15	B157	B156	B155	B154	B153	B152	B151	B150	NSEGDT[119:112]
P16	B167	B166	B165	B164	B163	B162	B161	B160	NSEGDT[127:120]
P17	B177	B176	B175	B174	B173	B172	B171	B170	NSEGDT[135:128]
P18	B187	B186	B185	B184	B183	B182	B181	B180	NSEGDT[143:136]
P19	B197	B196	B195	B194	B193	B192	B191	B190	NSEGDT[151:144]
P20	B207	B206	B205	B204	B203	B202	B201	B200	NSEGDT[159:152]
P21	B217	B216	B215	B214	B213	B212	B211	B210	NSEGDT[167:160]
P22	B227	B226	B225	B224	B223	B222	B221	B220	NSEGDT[175:168]
P23	B237	B236	B235	B234	B233	B232	B231	B230	NSEGDT[183:176]
P24	B247	B246	B245	B244	B243	B242	B241	B240	NSEGDT[191:184]
P25	B257	B256	B255	B254	B253	B252	B251	B250	NSEGDT[199:192]
P26	B267	B266	B265	B264	B263	B262	B261	B260	NSEGDT[207:200]
P27	B277	B276	B275	B274	B273	B272	B271	B270	NSEGDT[215:208]
P28	B287	B286	B285	B284	B283	B282	B281	B280	NSEGDT[223:216]
P29	B297	B296	B295	B294	B293	B292	B291	B290	NSEGDT[231:224]
P30	B307	B306	B305	B304	B303	B302	B301	B300	NSEGDT[239:232]
P31	B317	B316	B315	B314	B313	B312	B311	B310	NSEGDT[247:240]
P32	B327	B326	B325	B324	B323	B322	B321	B320	NSEGDT[255:248]

If this command issues parameters until the following conditions are met, an automatic EPD display/update sequence (refer to Section 7.7.1, “Automatic EPD Display/Update Sequence”) will start.

- Setting for the first parameter number to be issued: Parameter B14-B10(SEGDSTAD[4:0]) of the SEGDLEN command
- Setting for the last parameter number to be issued: Parameter B24-B20(SEGDENDAD[4:0]) of the SEGDLEN command

For details on the SEGDLEN command, refer to Section 8.2.12, “SEGDLEN:0x0C”. After setting the SEGDLEN command, issue this command.

The display waveform memory used during EPD display/update operations will change with the following settings.

- FMDISB command parameter B10(FMDISB) : Refer to “8.2.11 FMDISB: 0x0B”.
- SLVSEL pin : Refer to “5.4 EPD_MCU Driver Expansion EPD Drive Pin Extension/Control Pin for a Multi-chip.”
- POWCTL command parameter B30(ATTEMPON) : Refer to “8.2.21 POWCTL: 0x24”.

The relationship between the above settings and the display waveforms is shown in Table 8.2.9.

Table 8.2.9 Display waveform memory selection table

FMDISB	SLVSEL pin	ATTEMPON	Status	Selected display waveform memory
1	—	—	When Flash memory is not used	WFSET (Command parameter)
0	1	—	When Flash memory is used In the case of the slave IC	Display waveform 7 (Flash memory)
0	0	0	When Flash memory is used In the case of the master IC When automatic temperature detection is OFF	Display waveform 7 (Flash memory)
0	0	1	When Flash memory is used In the case of the master IC When automatic temperature detection is ON	Selected from the result of automatic temperature detection (Flash memory)

This command can only be issued while in a standby state (refer to Section 7.7, “Status Transition”).

P1-P32 NSEGDT[255:0]: Next Segment Data

(Default value:0x0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000)

This parameter stores the display data for each segment that is subject to EPD display/update operations.

Each bit corresponds to one segment.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0, black is displayed if 1 is written, and white if 0.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x1, white is displayed if 1 is written, and black if 0.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x2, white is displayed regardless of whether 0 or 1 is written.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x3, black is displayed regardless of whether 0 or 1 is written.

For the correspondence between NSEGDT [255:0] and the segments, refer to Table 8.2.3.2.

8.2.10 WFSET: 0x0A

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
WFSET	—	0	0	0	1	0	1	0	Waveform Timing Set
P1	B17	—	B15	B14	B13	B12	B11	B10	EPD_WAVE0[14:8]
P2	B27	B26	B25	B24	B23	B22	B21	B20	EPD_WAVE0[7:0]
P3	B37	-	B35	B34	B33	B32	B31	B30	EPD_WAVE1[14:8]
P4	B47	B46	B45	B44	B43	B42	B41	B40	EPD_WAVE1[7:0]
. .	. .	. .	. .	. .	. .	. .	. .	. .	. .
P61	B617	—	B615	B614	B613	B612	B611	B610	EPD_WAVE30[14:8]
P62	B627	B626	B625	B624	B623	B622	B621	B620	EPD_WAVE30[7:0]
P63	B637	—	B635	B634	B633	B632	B631	B630	EPD_WAVE31[14:8]
P64	B647	B646	B645	B644	B643	B642	B641	B640	EPD_WAVE31[7:0]

This command can be issued in any state other than during EPD display/update operations (refer to Section 7.7, “Status Transition”).

For details on this command, refer to Section 7.6.6, “Display Waveform Memory”.

8.2.11 FMDISB: 0x0B

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
FMDISB	—	0	0	0	1	0	1	1	Flash Memory Disable
P1	—	—	—	—	—	—	—	B10	FMDISB

This command can be issued at all times.

B17-B11 Reserved

B10 FMDISB: Flash Memory Disable Bit (Default value:0x0)

This parameter is used to select whether to use the default settings data and display waveform settings stored in Flash memory.

1: Flash memory data is unused.

0: The data in the Flash memory is used. (Default values)

If 1 is set, the following command parameters must be set before the ATEPDWR1 to 7 commands and the POWON command are issued.

- POWCTL command parameters
- IOCTL command parameters
- SLVSEL command parameters
- DET2CTL command parameters
- DROECTL command parameters
- WFSET command parameters

If 0 is to be set, the above command parameter settings in the Flash memory must be programmed in advance. If the settings are not programmed, system operation cannot be guaranteed.

8.2.12 SEGDLEN: 0x0C

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
SEGDLEN	—	0	0	0	1	1	0	0	Seg Data Length
P1	—	—	—	B14	B13	B12	B11	B10	SEGDSTAD[4:0]
P2	—	—	—	B24	B23	B22	B21	B20	SEGDENDAD[4:0]

This command can be issued at all times. Be sure to set any desired parameter before issuing the CURSDT, ATEPDWR1 to ATEPDWR7, or NEXTSDT command parameters.

Set this parameter when not all segments are used or when EPD display/update operations are partially performed.

B17-B15 Reserved

B14-B10 SEGDSTAD[4:0]: Segment Data Start Address Bits(Default value:0x00)

Set the input start address for the CURSDT, ATEPDWR1 to ATEPDWR7, or NEXTSDT command parameters.

Table 8.2.12.1 SEGDSTAD[4:0] input start address

SEGDSTAD[4:0]	Input start address
0x00	P1 (default value)
0x01 ~ 0x1F	P (setting value + 1)

The following are notes on this parameter.

- SEGDSTAD[4:0] ≦ SEGENDAD[4:0]

B27-B25 Reserved

B24-B20 SEGDENDAD[4:0]: Segment Data End Address Bits(Default value:0x00)

Set the input end address for the CURSDT, ATEPDWR1 to ATEPDWR7 command parameters. This setting does not work with the NEXTSDT command parameters.

Table 8.2.12.2 SEGDSTAD[4:0] input start address

SEGDENDAD[4:0]	Input start address
0x00	P1 (default value)
0x01 ~ 0x1F	P (setting value + 1)

The following are notes on this parameter.

- SEGDSTAD[4:0] ≦ SEGENDAD[4:0]

Unless the above notes are observed, normal operations cannot be guaranteed.

If the ATEPDWR1 to ATEPDWR7 command parameters have been entered, an automatic EPD display/update sequence will start as soon as issuing all parameters up to this parameter has finished.

8.2.13 NEXTSDT: 0x10

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
NEXTSDT	—	0	0	1	0	0	0	0	Next Segment Data
P1	B17	B16	B15	B14	B13	B12	B11	B10	NSEGDT[7:0]
P2	B27	B26	B25	B24	B23	B22	B21	B20	NSEGDT[15:8]
P3	B37	B36	B35	B34	B33	B32	B31	B30	NSEGDT[23:16]
P4	B47	B46	B45	B44	B43	B42	B41	B40	NSEGDT[31:24]
P5	B57	B56	B55	B54	B53	B52	B51	B50	NSEGDT[39:32]
P6	B67	B66	B65	B64	B63	B62	B61	B60	NSEGDT[47:40]
P7	B77	B76	B75	B74	B73	B72	B71	B70	NSEGDT[55:48]
P8	B87	B86	B85	B84	B83	B82	B81	B80	NSEGDT[63:56]
P9	B97	B96	B95	B94	B93	B92	B91	B90	NSEGDT[71:64]
P10	B107	B106	B105	B104	B103	B102	B101	B100	NSEGDT[79:72]
P11	B117	B116	B115	B114	B113	B112	B111	B110	NSEGDT[87:80]
P12	B127	B126	B125	B124	B123	B122	B121	B120	NSEGDT[95:88]
P13	B137	B136	B135	B134	B133	B132	B131	B130	NSEGDT[103:96]
P14	B147	B146	B145	B144	B143	B142	B141	B140	NSEGDT[111:104]
P15	B157	B156	B155	B154	B153	B152	B151	B150	NSEGDT[119:112]
P16	B167	B166	B165	B164	B163	B162	B161	B160	NSEGDT[127:120]
P17	B177	B176	B175	B174	B173	B172	B171	B170	NSEGDT[135:128]
P18	B187	B186	B185	B184	B183	B182	B181	B180	NSEGDT[143:136]
P19	B197	B196	B195	B194	B193	B192	B191	B190	NSEGDT[151:144]
P20	B207	B206	B205	B204	B203	B202	B201	B200	NSEGDT[159:152]
P21	B217	B216	B215	B214	B213	B212	B211	B210	NSEGDT[167:160]
P22	B227	B226	B225	B224	B223	B222	B221	B220	NSEGDT[175:168]
P23	B237	B236	B235	B234	B233	B232	B231	B230	NSEGDT[183:176]
P24	B247	B246	B245	B244	B243	B242	B241	B240	NSEGDT[191:184]
P25	B257	B256	B255	B254	B253	B252	B251	B250	NSEGDT[199:192]
P26	B267	B266	B265	B264	B263	B262	B261	B260	NSEGDT[207:200]
P27	B277	B276	B275	B274	B273	B272	B271	B270	NSEGDT[215:208]
P28	B287	B286	B285	B284	B283	B282	B281	B280	NSEGDT[223:216]
P29	B297	B296	B295	B294	B293	B292	B291	B290	NSEGDT[231:224]
P30	B307	B306	B305	B304	B303	B302	B301	B300	NSEGDT[239:232]
P31	B317	B316	B315	B314	B313	B312	B311	B310	NSEGDT[247:240]
P32	B327	B326	B325	B324	B323	B322	B321	B320	NSEGDT[255:248]

This command can be issued in any state other than during EPD display/update operations (refer to Section 7.7, “Status Transition”).

The first command parameter number to be issued can be set in the following command parameter:

- Setting for the first parameter number to be issued: Parameter B14-B10(SEGDSTAD[4:0]) of the SEGDLEN command

Setting for the last parameter number to be issued: This command is not related to the

B24-B20(SEGDENDAD[4:0]) parameter of the SEGDLEN command. Finish issuing the parameters with the last parameter number to be issued. All the parameters that have been issued will be applied.

For details on the SEGDLEN command, refer to Section 8.2.12, “SEGDLEN:0x0C”. After setting the SEGDLEN command, issue this command.

P1-P32 NSEGDT[255:0]: Next Segment Data

(Default value:0x0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000)

This parameter stores the display data for each segment that is subject to EPD display/update operations when EPD display/update operations are performed using the POWON, EPDWR or POWOFF command. There is no need to set this parameter if EPD display/update operations are performed by issuing the ATEPDWR1 to ATEPDWR7 commands.

Each bit corresponds to one segment.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0, black is displayed if 1 is written, and white if 0.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x1, white is displayed if 1 is written, and black if 0.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x2, white is displayed regardless of whether 0 or 1 is written.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x3, black is displayed regardless of whether 0 or 1 is written.

For the correspondence between NSEGDT [255:0] and the segments, refer to Table 8.2.3.2.

8.2.14 POWON: 0x11

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
POWON	—	0	0	1	0	0	0	1	Power On

This command can be issued all the time.

If you want to control the power on / EPD display update / power off individually, use this command to do the following:

- Starting the built-in oscillation circuit
- Starting power warm-up for the VOUT1/VEPD Boosters. Those power supplies are required for the EPD display update.

If the B34 (DCDCSEL) is 1, the built-in Cap booster is used. In this case, if you want to control the power-on / EPD display update / power-off individually, use this command to do the following.

- Starting the built-in oscillation circuit
- Starting power warm-up for the VOUT1/VOUT2/HVREG power supplies. Those power supplies are required for the EPD display update.

After this command is issued, it takes 200 msfor the power warm-up to finish. When the power worm-up is finished and the power is stabilized, EPD display update can be started by issuing the EPDWR command if the device is a master IC (the SLVSEL pin is low) or by detecting the EPDTRG pin is high at a rising edge of the EPDCLK pin if the device is a slave IC (the SLVSEL pin is high).

After EPD display update is finished, the VOUT1/VEPD are not turned off automatically. When the power is stabilized, EPD display update can be started by issuing the EPDWR command if the device is a master IC or by detecting the EPDTRG pin is high at a rising edge of the EPDCLK pin if the device is a slave IC.

8.2.15 POWOFF: 0x12

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
POWOFF	—	0	0	1	0	0	1	0	Power Off

This command can be issued during the stable power supply period (refer to Section 7.7, “Status Transition”).

If this command is issued when power startup, EPD display update, and power shutdown are controlled separately, the following operations will take place.

- Transition to the power supply shutdown sequence (Refer to “7.7 Transition Status”)
- VOUT1/VEPD power supply shutdown
- Shutdown of the built-in oscillation circuit
- Transition to a standby status (Refer to “7.7 Transition Status”)

If the B34 (DCDCSEL) is 1, the built-in Cap booster is used. If you want to control the power-on / EPD display update / power-off individually, use this command to do the following.

- Starting the power off sequence (see Section 7.7 State Transition)
- Turning off the VOUT1/VOUT2/HVREG power supplies
- Stopping the built-in oscillation circuit
- Entering stand-by mode (see Section 7.7 State Transition).

8.2.16 EPDWR: 0x13

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
EPDWR	—	0	0	1	0	0	1	1	EPD Write

This command can be issued during the stable power supply period (refer to Section 7.7, “Status Transition”). It can also be issued when the master IC is used (the SLVSEL terminal is set at a low level).

This command can be issued during the power supply stable period (Refer to “7.7 Transition Status”). It can also be issued in the case of the master IC (SLVSEL pin = Low level).

If this command is issued when power startup, EPD display update, and power shutdown are controlled separately, the following operations will take place.

- Commencement of EPD display update (Refer to “7.7 Transition Status”)

This command cannot be used in the case of the slave IC (SLVSEL pin = High level). If the High level status of the EPDTRG pin is acquired during the rise of the EPDCLK pin, the EPD display update sequence will start.

8.2.17 EPDPCTL: 0x20

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
EPDPCTL	—	0	1	0	0	0	0	0	EPD Back Plane Control
P1	—	—	—	—	—	—	—	B10	NBPDT

This command can be issued in any state other than during EPD display/update operations (refer to Section 7.7, “Status Transition”).

B17-B11 Reserved

B10 NBPDT: Next Back Plane Data Bit (Default value:0x0)

This parameter stores display data on the backplane for which EPD display/update operations are to be performed.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x0, black is displayed if 1 is written, and white if 0.

If the EPDDCTL command B13-B12 (DSPMOD) is 0x1, white is displayed if 1 is written, and black if 0.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x2, white is displayed

regardless of whether 0 or 1 is written.

When the B13-B12(DSPMOD) parameter of the EPDDCTL command is set to 0x3, black is displayed regardless of whether 0 or 1 is written.

8.2.18 EPDDCTL: 0x21

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
EPDDCTL	—	0	1	0	0	0	0	1	EPD Display Control
P1	—	—	—	—	B13	B12	—	—	DSPMOD[1:0]

This command can be issued in any state other than during EPD display/update operations (refer to Section 7.7, “Status Transition”).

B17-B14 Reserved

B13-B12 DSPMOD[1:0]: Next Back Plane Bits (Default value:0x0)

This parameter is used to select a mode of EPD display/update operations.

Table 8.2.18 DSPMOD[2:0] display waveform selection table

DSPMOD[1:0]	Display mode
0x3	All-black display
0x2	All-white display
0x1	Reverse display
0x0	Normal display

If EPD display/update operations are performed by setting this parameter, display colors can be reversed or the entire screen can be displayed in white or black. This display control does not directly affect the “NEXTSDT[255:0]” or “NEXTBDT” EPD display/update data.

To make a normal display, set these parameters to 0x0, and update the EPD display.

B11-B10 Reserved

8.2.19 WFSEL: 0x22

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
WFSEL	—	0	1	0	0	0	1	0	Waveform Select
P1	—	—	—	—	—	B12	B11	B10	WFSEL[2:0]

This command can be issued in any state other than during EPD display/update operations (refer to Section 7.7, “Status Transition”).

B17-B13 Reserved

B12-B10 WFSEL[2:0]:Waveform Select Bits (Default value:0x1)

This parameter selects from the seven display waveform modes stored in the Flash memory when the EPD display is updated if you control the power-on / EPD display update / power-off individually. See Table 8.2.18.1.

Table 8.2.19.1 WFSEL[2:0] display waveform selection

WFSEL[2:0]	Selection display waveform
0x0	Setting prohibited
0x1	Display waveform 1 (default value)
0x2	Display waveform 2
0x3	Display waveform 3
0x4	Display waveform 4
0x5	Display waveform 5
0x6	Display waveform 6
0x7	Display waveform 7

The display waveform memory which is used when the display is being updated changes according to the settings shown below.

- FMDISB command parameter B10(FMDISB) : Refer to “8.2.11 FMDISB: 0x0B”.
- SLVSEL pin : Refer to “5.4 EPD_MCU Driver Expansion EPD Drive Pin Extension/Control Pin for a Multi-chip.”
- POWCTL command parameter B30(ATTEMPON) : Refer to “8.2.21 POWCTL: 0x24”.

The relationship between the above settings and the display waveforms is shown in Table 8.2.19.2.

Table 8.2.19.2 Display waveform memory selection table

FMDISB	SLVSEL pin	ATTEMPON	Status	Selected display waveform memory
1	—	—	When Flash memory is not used	WFSET (Command parameter)
0	1	—	When Flash memory is used In the case of the slave IC	WFSEL[2:0] (Flash memory)
0	0	0	When Flash memory is used In the case of the master IC When automatic temperature detection is OFF	WFSEL[2:0] (Flash memory)
0	0	1	When Flash memory is used In the case of the master IC When automatic temperature detection is ON	Selected from the result of automatic temperature detection (Flash memory)

8.2.20 TEMPSENSON: 0x23

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
TEMPSENSON	—	0	1	0	0	0	1	1	Temperature Sensor Sensing On

This command can be issued while in a standby state or during the stable power supply period (refer to Section 7.7, “Status Transition”).

When it is issued, the temperature detection circuit detects the temperature. Temperature detection is completed 3.5 ms after the command is issued. Do not operate the command interface or update the EPD display during this interval.

The result (AD value) of temperature detection can be stored in a register, and read from the command interface as a 7-bit digital value. For the readout procedure in the case of the I2C slave interface, refer to Figure 8.2.20.1. For the readout procedure in the case of the SPI slave interface, refer to Figure 8.2.20.2.

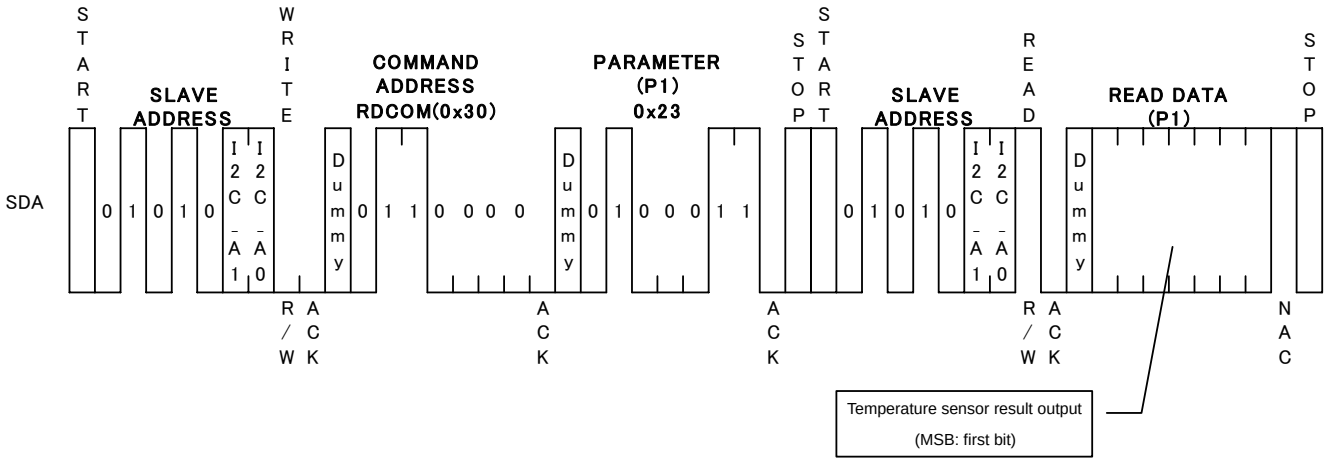

Figure 8.2.20.1 I2C Reading of AD value in the case of a slave interface

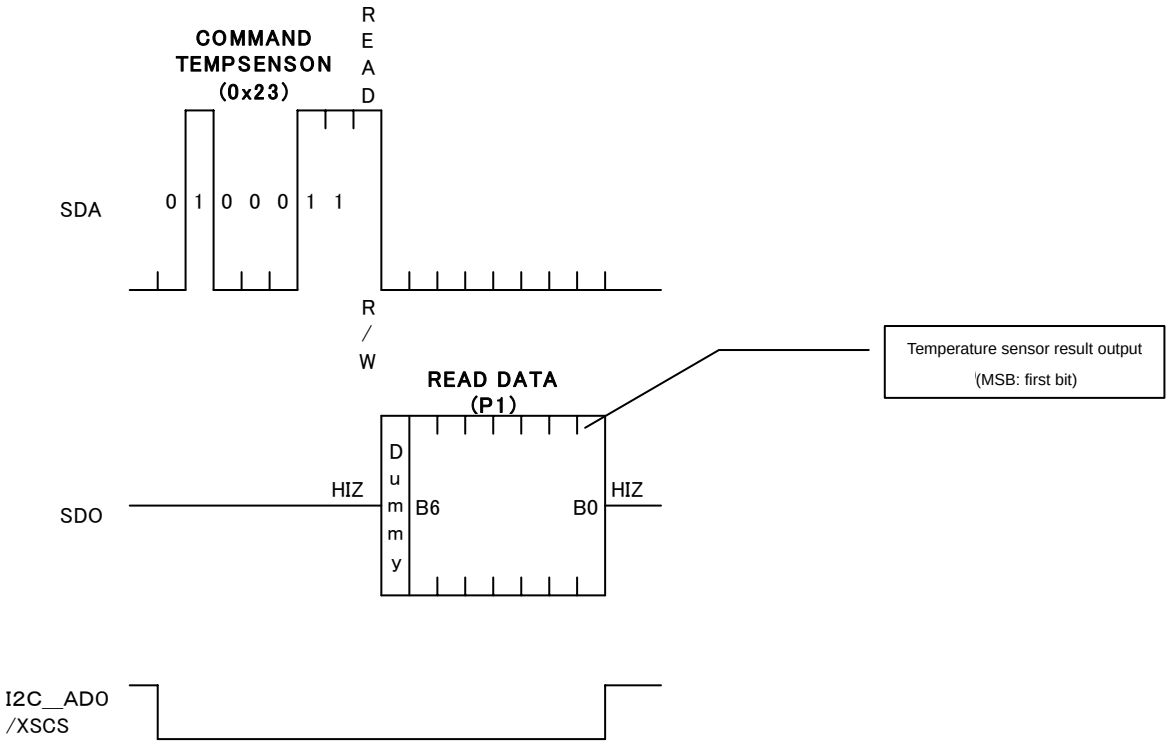

Figure 8.2.20.2 SPI Readout of AD value in the case of a slave interface

8.2.21 POWCTL: 0x24

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
POWCTL	—	0	1	0	0	1	0	0	Power Control
P1	—	—	B15	B14	—	—	—	B10	VDC2SEL[1:0] VDC1SEL
P2	B27	B26	B25	B24	B23	B22	B21	B20	VOUTSU1FREQ[1:0] VOUT1FREQ[1:0] VEPDSUFREQ[1:0] VEPDFREQ[1:0]
P3	—	—	—	—	—	—	—	B30	ATTEMPON
P4	B47	B46	B45	B44	B43	B42	B41	B40	FM2SETWAVE TMPTW1W2 [2:0] FM3SETWAVE TMPTW2W3 [2:0]
P5	B57	B56	B55	B54	B53	B52	B51	B50	FM4SETWAVE TMPTW3W4[2:0] FM5SETWAVE TMPTW4W5 [2:0]
P6	B67	B66	B65	B64	B63	B62	B61	B60	FM6SETWAVE TMPTW5W6 [2:0] FM7SETWAVE TMPTW6W7 [2:0]
P7	—	—	—	—	—	B72	B71	B70	TEMPOFFSET[2:0]
P8	0	0	0	0	1	1	1	1	Fix
P9	0	0	1	1	0	0	0	0	Fix
P10	0	0	0	0	0	1	0	0	Fix
P11	0	0	0	0	0	0	0	0	Fix
P12	0	0	1	0	1	1	0	1	Fix
P13	0	0	0	0	0	0	0	1	Fix
P14	0	0	0	0	1	0	0	0	Fix
P15	0	0	0	1	0	0	0	0	Fix
P16	0	0	0	1	1	0	0	0	Fix
P17	1	0	1	0	0	0	0	1	Fix
P18	0	0	0	1	1	1	1	1	Fix

This command can be issued while in a standby state (refer to Section 7.7, “Status Transition”). There is no need to issue this command parameter when the B10(FMDISB) parameter of the FMDISB command is set to “0”.

B17-B16 Reserved

B15-B14 VDC2SEL[1:0]: VDC2 Voltage Select Bits (Default value:0x3)

This parameter is used to select the VDC2 voltage for the standard power supply for the VEPD Booster. See Table 8.2.21.1 for the settings correspondence table. The VEPD voltage is three times the VDC2 voltage.

Table 8.2.21.1 VDC2SEL [1:0] and VDC2 voltage correspondence table

VDC2SEL[1:0]	VDC2 voltage	VEPD voltage (VDC2 voltage × 3)
0x0	Prohibited setting	Prohibited setting
0x1	3.05V	9.15V
0x2	4.1V	12.3V
0x3	5.15V (Default value)	15.45V

Select the DET2CTL command parameter B12-B11 (DET2SEL[1:0]) according to the setting of this parameter. See Section 8.2.26 DET2CTL:0x32 Table 8.2.26.

B13-B11 Reserved

B10 VDC1SEL: VDC1 Voltage Select Bit (Default value:0x0)

This parameter sets the VDC1 voltage for the standard power supply for the VOUT1 Booster. See Table 8.2.21.2 for the settings correspondence table.

Table 8.2.21.2 VDC1SEL and VDC1 voltage correspondence table

VDC1SEL	VDC1 voltage	VOUT1 voltage
0x0	1.98V(Default value)	5.94V(VDC1 voltage x 3)
0x1	2.98V	5.96V(VDC1 voltage x 2)

If this device is used as a multi-chip, the master device (SLVSEL pin = Low level) must be set to 1. By setting this device to 1, the clock and display start timing that are necessary for updating the EPD display will be output to the slave IC. The slave device (SLVSEL pin = High level) is unrelated to this parameter.

When this device is used on its own, by setting it to 0 the output from the EPDCLK and EPDTRG pins will be fixed at 0(Vss), thus enabling unnecessary consumption of current to be suppressed.

B27-B26 VOUT1SUFREQ[1:0]: VOUT1 Start Up Dcdc Frequency Select Bits (Default value:0x0)

This parameter is used to select the boost clock frequency during the power supply startup period (refer to Section 7.7, “Status Transition”) for the VOUT1 Booster. See Table 8.2.21.3 for the settings correspondence table.

Table 8.2.21.3 VOUT1SUFREQ[1:0] and VOUT1 voltage booster clock frequency correspondence table

VOUT1SUFREQ[1:0]	VOUT1 voltage booster clock frequency
0x0	62.5KHz (Default value)
0x1	32KHz
0x2	16KHz
0x3	8KHz

Set this parameter to 0x0 in normal usage.

B25-B24 VOUT1FREQ: VOUT1 Dcdc Frequency Select Bits (Default value:0x0)

This parameter is used to select the boost clock frequency for the VOUT1 Booster. This setting is for when the VOUT1 Booster is operating during any period other than the power supply startup period (refer to Section 7.7, “Status Transition”). See Table 8.2.21.4 for the settings correspondence table.

Table 8.2.21.4 VOUT1FREQ [1:0] and VOUT1 voltage booster clock frequency correspondence table

VOUT1FREQ[1:0]	VOUT1 voltage booster clock frequency
0x0	64KHz (Default value)
0x1	32KHz
0x2	16KHz
0x3	8KHz

When you configure this parameter, see Section 6 Recommended Values for the External Components.

B23-B22 VEPDSUFREQ[1:0]: VEPD Start Up Dcdc Frequency Select Bits (Default value:0x0)

This parameter is used to select the boost clock frequency for the VOUT1 Booster. See Table 8.2.21.5 for the settings correspondence table.

Table 8.2.21.5 VEPDSUFREQ[1:0] and VEPD voltage booster clock frequency correspondence table

VEPDSUFREQ[1:0]	VEPD voltage booster clock frequency
0x0	64KHz (Default value)
0x1	16KHz
0x2	8KHz
0x3	4KHz

Set this parameter to 0x0 in normal usage.

B21-B20 VEPDFREQ: VEPD Dcdc Frequency Select Bits (Default value:0x0)

This parameter is used to select the boost clock frequency for the VEPD Booster. This setting is for when the VEPD Booster is operating during any period other than the power supply startup period (refer to Section 7.7, "Status Transition"). See Table 8.2.21.6 for the settings correspondence table.

Table 8.2.21.6 VEPDFREQ [1:0] and VEPD voltage boosting clock frequency correspondence table

VEPDFREQ[1:0]	VEPD voltage boosting clock frequency
0x0	32KHz (Default value)
0x1	16KHz
0x2	8KHz
0x3	4KHz

When you configure this parameter, see Section 6 Recommended Values for the External Components.

B37-B35 Reserved

B34 Fixed 0 Bit

Fix this parameter to 0x0.

B33-B31 Reserved

B30 ATTEMPON: Auto Temperature Sensing On Bit (Default value:0x0)

This function automatically detects the temperature prior to updating of the EPD display, and based on the result it selects one of the display waveforms stored in the Flash memory (Refer to "7.7 Transition Status"). These parameters are effective only for making the following settings.

- The SLVSEL terminal is set at a low level (when the master IC is used), and the B10(FMDISB) parameter of the FMDISB command is set to "0" (where flash memory data is used).

If the automatic detection function is valid, be sure to set parameters P4-P6. If this function is invalid, there is no need to set parameters P4-P6.

The function automatically reads out the initial setting data (refer to "7.5.2 Flash Memory Initial Setting Data) stored in the Flash memory, before the EPD display update. The POWCTL command parameter issued with the command interface before the EPD display update overwrites data stored in the Flash memory. Make sure to program the initial setting data in the Flash memory.

Setting the number of items of display waveform data stored in the Flash memory

The POWCTL parameter which sets the number of items of display waveform data stored in the Flash memory to 1 is shown below.

- Two types of display waveform data: B47(FM2SETWAVE)
- Three types of display waveform data: B43(FM3SETWAVE)
- Four types of display waveform data: B57(FM4SETWAVE)
- Five types of display waveform data: B53(FM5SETWAVE)
- Six types of display waveform data: B67(FM6SETWAVE)
- Seven types of display waveform data: B63(FM7SETWAVE)

Be sure to set 1 in the parameter applicable to the above. If it is not set, operation of the system cannot be guaranteed.

Temperature boundary value and display waveform data

The temperature boundary value is the value which automatically selects a maximum of seven items of display waveform data stored in the Flash memory depending upon the temperature change, based on the result of automatic temperature detection. For details of the method of setting the display waveform data, refer to "7.5.1 Flash Memory Map."

The setting of the temperature boundary value corresponds to the POWCTL command parameter shown below.

- Temperature boundary value setting for display data 1 and 2: B46-B44(TMPTW1W2[2:0])
- Temperature boundary value setting for display data 2 and 3: B42-B40 (TMPTW2W3[2:0])
- Temperature boundary value setting for display data 3 and 4: B56-B54(TMPTW3W4[2:0])
- Temperature boundary value setting for display data 4 and 5: B52-B50(TMPTW4W5[2:0])
- Temperature boundary value setting for display data 5 and 6: B66-B64(TMPTW5W6[2:0])
- Temperature boundary value setting for display data 6 and 7: B62-B60(TMPTW6W7[2:0])

The relationship between the above set value and the temperature boundary value is shown in Table 8.2.21.7. (The accuracy of the temperature detection circuit is ±5 °C.)

Table 8.2.21.7 Set value and temperature boundary value correspondence table

Set value	Temperature boundary value
0x0	0.1 °C (Default value)
0x1	10.2°C
0x2	20.3 °C
0x3	29.7 °C
0x4	39.8 °C
0x5	49.9 °C
0x6,0x7	Prohibited setting

The precautions concerning the setting of the temperature boundary value are set out below.

- TMPTW1W2[2:0]<TMPTW2W3[2:0]<TMPTW3W4[2:0]<TMPTW4W5[2:0]<TMPTW5W6[2:0]< TMPTW6W7[2:0]
  (Note, however, that there is no need to make more items of display waveform data than the number of items of display data stored in the Flash memory. If additional items are set, operation will be unaffected.)

Figure 8.2.21.1 shows an example of the temperature boundary value, the display waveform memory, and the automatically detected result for the case where seven kinds of display waveform data are stored in the display waveform memory.

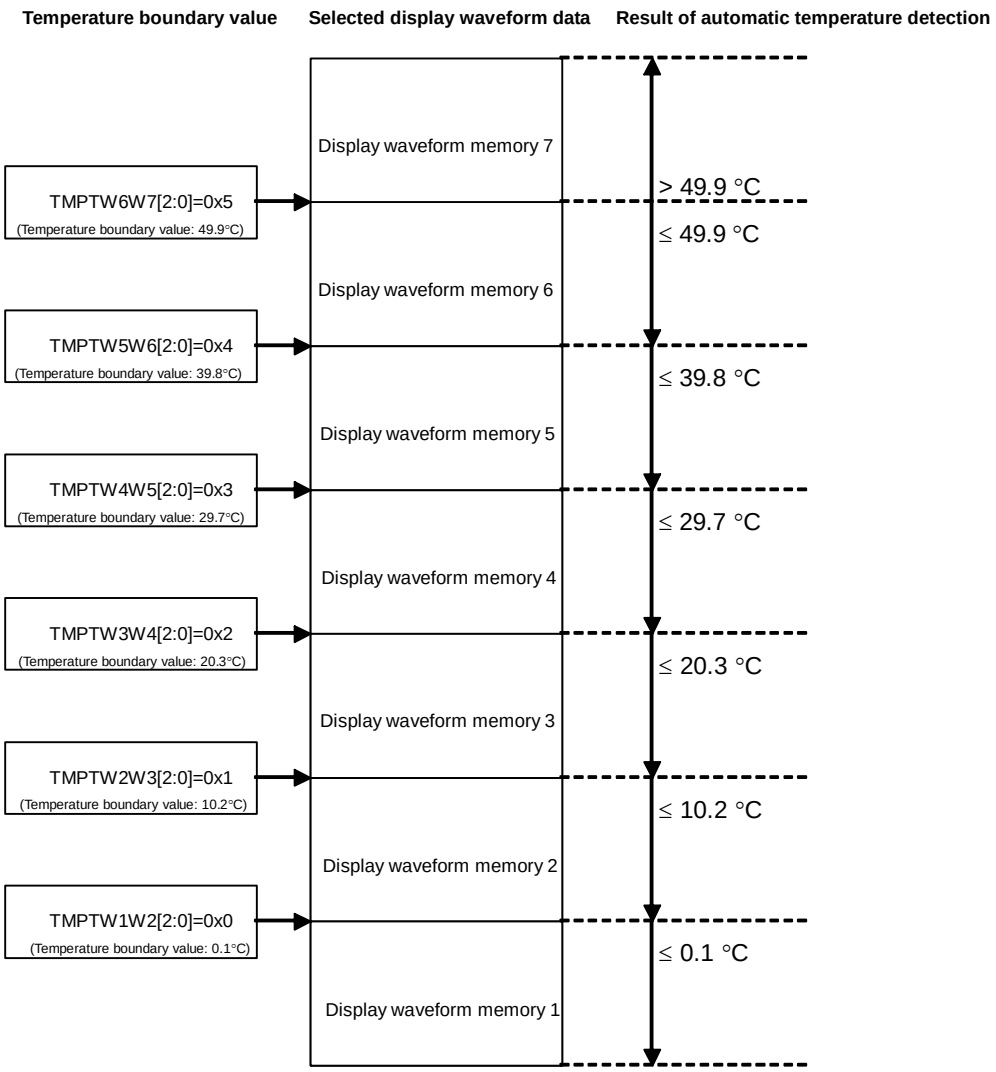

Figure 8.2.21.1 Example of display waveform (seven items of display waveform data)

Figure 8.2.21.2 shows an example of the temperature boundary value, the display waveform memory, and the automatic temperature detection result for the case where three kinds of display waveform data are stored in the display waveform memory.

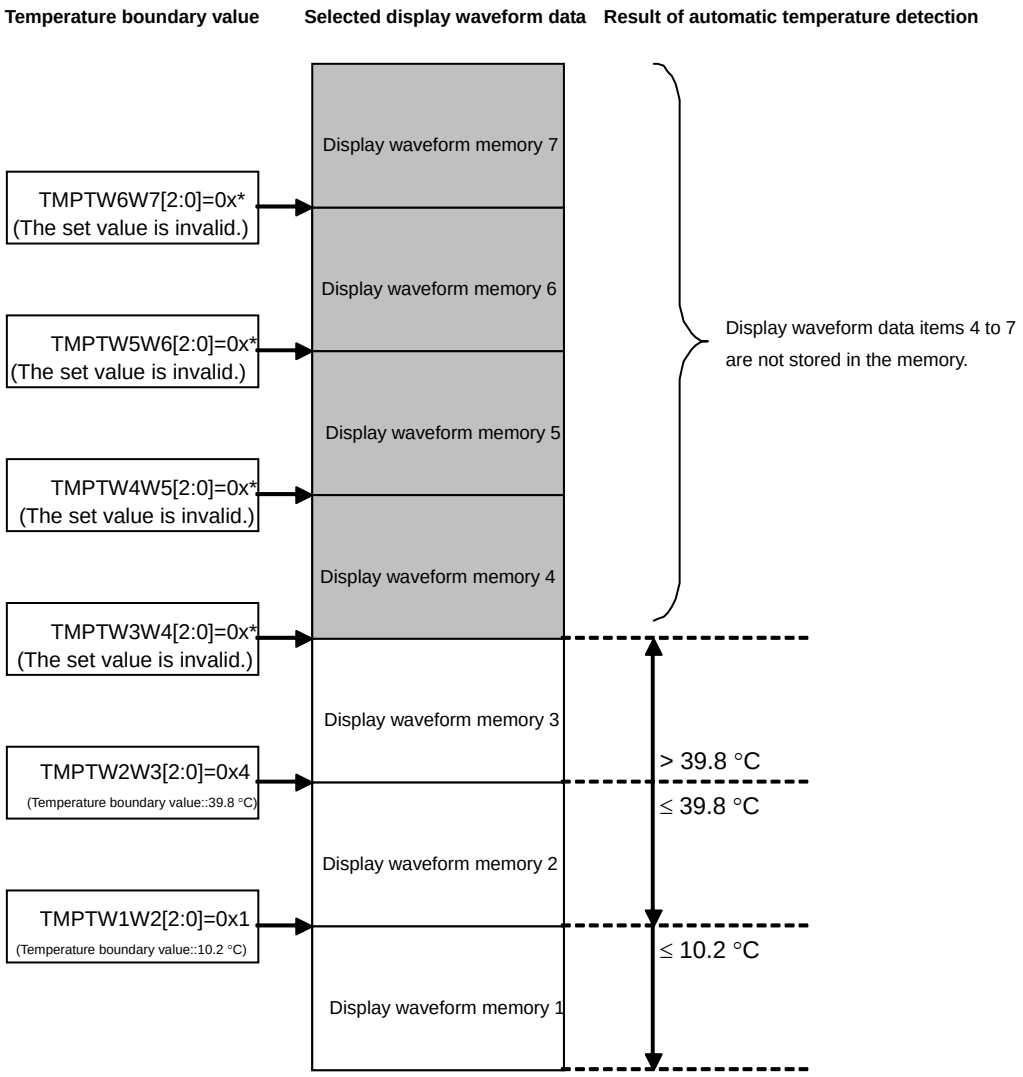

Figure 8.2.21.2 Example of display waveform (three kinds of display waveform data)

B47 FM2SETWAVE: Flash Memory 2 Setting Waveform Bit (Default value:0x0)

This parameter indicates whether two types of display waveform are stored in Flash memory.

1: Two kinds of display wavefore data are stored in the Flash memory.

0: One kind or at least three kinds of display data are stored in the Flash memory. (Default value)

Set this parameter when all of the following settings are satisfied.

- When setting B30 (ATTEMPON) to 1
- In the case of the master IC (SLVSEL pin = Low level)
- The Flash memory data is used (The FMDISB command B10 (FMDISB) is set to 0).

This parameter is invalid when settings other than the above are made.

B46-B44 TMPTW1W2[2:0]: Temperature Point between Waveform 1 and Waveform 2 Bits (Default value:0x0)

This parameter sets the temperature boundary values for which display waveform data 1 and display waveform data 2 stored in Flash memory are to be selected, and determines which waveform to select according to the automatic temperature detection results. See Table 8.2.21.7 for the relationship between set values and temperature boundary values.

B43 FM3SETWAVE: Flash Memory 3 Setting Waveform Bit (Default value:0x0)

This parameter indicates whether three types of display waveform are stored in Flash memory.

1: Three kinds of display waveform data are stored in the Flash memory.

0: Two or fewer kinds or at least four kinds of display waveform data are stored in the Flash memory. (Default value)

Set this parameter when all of the following settings are satisfied.

- When setting B30 (ATTEMPON) to 1
- In the case of the master IC (SLVSEL pin = Low level)
- The Flash memory data is used (The FMDISB command B10 (FMDISB) is set to 0).

This parameter is invalid when settings other than the above are made.

B42-B40 TMPTW2W3[2:0]: Temperature Point between Waveform 2 and Waveform 3 Bits (Default value:0x1)

This parameter sets the temperature boundary values for which display waveform data 2 and display waveform data 3 stored in flash memory are to be selected, and determines which waveform to select according to the automatic temperature detection results. See Table 8.2.21.7 for the relationship between set values and temperature boundary values.

B57 FM4SETWAVE: Flash Memory 4 Setting Waveform Bit (Default value:0x0)

This parameter indicates whether four types of display waveform are stored in Flash memory.

1: Four kinds of display waveform data are stored in the Flash memory.

0: Three or fewer kinds or at least five kinds of display waveform data are stored in the Flash memory. (Default value)

Set this parameter when all of the following settings are satisfied.

- When setting B30 (ATTEMPON) to 1
- In the case of the master IC (SLVSEL pin = Low level)
- The Flash memory data is used (The FMDISB command B10 (FMDISB) is set to 0).

This parameter is invalid when settings other than the above are made.

B56-B54 TMPTW3W4[2:0]: Temperature Point between Waveform 3 and Waveform 4 Bits (Default value:0x2)

This parameter sets the temperature boundary values for which display waveform data 3 and display waveform data 4 stored in flash memory are to be selected, and determines which waveform to select according to the automatic temperature detection results. See Table 8.2.21.7 for the relationship between set values and temperature boundary values.

B53 FM5SETWAVE: Flash Memory 5 Setting Waveform Bit (Default value:0x0)

This parameter indicates whether four types of display waveform are stored in Flash memory.

1: Five kinds of display waveform data are stored in the Flash memory.

0: Four or fewer kinds or at least six kinds of display waveform are stored in the Flash memory. (Default value)

Set this parameter when all of the following settings are satisfied.

- When setting B30 (ATTEMPON) to 1
- In the case of the master IC (SLVSEL pin = Low level)
- The Flash memory data is used (The FMDISB command B10 (FMDISB) is set to 0).

This parameter is invalid when settings other than the above are made.

B52-B50 TMPTW4W5[2:0]: Temperature Point between Waveform 4 and Waveform 5 Bits (Default value:0x3)

This parameter sets the temperature boundary values for which display waveform data 4 and display waveform data 5 stored in Flash memory are to be selected, and determines which waveform to select according to the automatic temperature detection results. See Table 8.2.21.7 for the relationship between set values and temperature boundary values.

B67 FM6SETWAVE: Flash Memory 6 Setting Waveform Bit (Default value:0x0)

This parameter indicates whether six types of display waveform are stored in flash memory.

1: Six kinds of display waveform data are stored in the Flash memory.

0: Five or fewer kinds or seven kinds of display waveform data are stored in the Flash memory. (Default value)

Set this parameter when all of the following settings are satisfied.

- When setting B30 (ATTEMPON) to 1
- In the case of the master IC (SLVSEL pin = Low level)
- The Flash memory data is used (The FMDISB command B10 (FMDISB) is set to 0).

This parameter is invalid when settings other than the above are made.

B66-B64 TMPTW5W6[2:0]: Temperature Point between Waveform 5 and Waveform 6 Bits (Default value:0x4)

This parameter sets the temperature boundary values for which display waveform data 5 and display waveform data 6 stored in Flash memory are to be selected, and determines which waveform to select according to the automatic temperature detection results. See Table 8.2.21.7 for the relationship between set values and temperature boundary values.

B63 FM7SETWAVE: Flash Memory 7 Setting Waveform Bit (Default value:0x1)

This parameter indicates whether seven types of display waveform are stored in flash memory.

1: Seven kinds of display waveform data are stored in the Flash memory. (default value)

0: Six or fewer kinds of display waveform data are stored in the Flash memory.

Set this parameter when all of the following settings are satisfied.

- When setting B30 (ATTEMPON) to 1
- In the case of the master IC (SLVSEL pin = Low level)
- The Flash memory data is used (The FMDISB command B10 (FMDISB) is set to 0).

This parameter is invalid when settings other than the above are made.

B62-B60 TMPTW6W7[2:0]: Temperature Point between Waveform 6 and Waveform 7 Bits (Default value:0x5)

This parameter sets the temperature boundary values for which display waveform data 6 and display waveform data 7 stored in Flash memory are to be selected, and determines which waveform to select according to the automatic temperature detection results. See Table 8.2.21.7 for the relationship between set values and temperature boundary values.

B77-B73 Reserved

B72-B70 TEMPOFFSET[2:0]: Temperature Sensing Result Offset Bits (Default value:0x0)

This value offsets the temperature detection result (AD value). See Table 8.2.21.8 for the amount of offset.

Table 8.2.21.8 TEMPOFFSET [2:0] and offset value correspondence table

TEMPOFFSET[2:0]	Temperature sensing result (AD value) offset	Temperature value offset
0x0	AD value + 0(default value)	+0 °C
0x1	AD value + 2	+1.26 °C
0x2	AD value + 4	+2.52 °C
0x3	AD value + 6	+3.78 °C
0x4	AD value - 0	-0 °C
0x5	AD value - 2	-1.26 °C
0x6	AD value - 4	-2.52 °C
0x7	AD value - 6	-3.78 °C

When these parameters are set, the result of calculating the offset is output to the temperature detection result (AD value).

The temperature detection result (AD value) is 7 bits (AD value: 0x0 – 0x7F). If the calculated value of the offset is less than 0, the temperature detection result will be 0x0. If the calculated value is 0x128 or higher, the temperature detection result will be 0x127.

B87-B80 Set this parameter to 0x0F.

B97-B90 Set this parameter to 0x30.

B107-B100 Set this parameter to 0x04.

B117-B110 Set this parameter to 0x00.

B127-B120 Set this parameter to 0x2D.

B137-B130 Set this parameter to 0x01.

B147-B140 Set this parameter to 0x08.

B157-B150 Set this parameter to 0x10.

B167-B160 Set this parameter to 0x18.

B177-B170 Set this parameter to 0xA1.

B187-B180 Set this parameter to 0x1F.

8.2.22 IOCTL: 0x25

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
IOCTL	—	0	1	0	0	1	0	1	I/O Cell Control
P1	—	—	—	—	—	—	—	B10	EPDCTLSIG

This command can be issued while in a standby state (refer to Section 7.7, “Status Transition”). There is no need to issue this command parameter when the B10(FMDISB) parameter of the FMDISB command is set to “0”.

B17-B11 Reserved

B10 EPDTRGSIG: Epd Trigger Signal Bit (Default value:0x0)

This parameter determines whether the EPDCLK and EPDTRG signals that internally generate EPD display/update timing will be output from the EPDCLK and EPDTRG terminals when the SLVSEL terminal is set at a low level.

0x1: Output the slave IC control signals

(EPDCLK signal = EPDCLK pin. EPDTRG signal = EPDTRG pin.)

0x0: 0 (VSS) output fixed (default)

When this device is used in the multiple-chip configuration, this parameter needs to be set to 0x1for the master device (SLVSEL pin = Low). By setting this parameter to 0x1, the clock required for the EPD display update and the display start timing are output to the slave IC. If the device is configured as a slave device (SLVSEL pin = High), this parameter is ignored.

When this device is used in the single-chip configuration, by setting this parameter to 0x0, the EPDCLK pin and the EPDTRG pin are tied to the low output level (VSS) and unnecessary current consumption can be avoided.

8.2.23 SLVMODE: 0x26

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
SLVMODE	—	0	1	0	0	1	1	0	Slave Mode
P1	—	—	—	—	—	—	—	B10	SLVMODE

This command can be issued while in a standby state (refer to Section 7.7, “Status Transition”). There is no need to issue this command parameter when the B10(FMDISB) parameter of the FMDISB command is set to “0”.

B17-B11 Reserved

B10 SLVMODE: Slave Mode Bit (Default value:0x0)

This parameter sets whether the slave device (where the SLVSEL terminal is set at a high level) will be used with multiple chips or with EPD microcomputer extensions.

0x1: When used for the EPD_MCU driver expansion

0x0: In the case of a multi-chip (default value)

If this device is configured as a slave IC in the multiple-chip configuration, you need to set this parameter to 0x0. By setting this parameter to 0x 0, the device can recognize that the device is used as a slave IC in the multiple-chip configuration and can use the VOUT1/VEPD voltages generated by the master IC.

If this device is used in the EPD microcontroller extension, you need to set this parameter to 0x1. By setting this parameter to 0x1, the device can recognize that the device is used in the EPD microcontroller extension and generate the VOUT1/VEPD voltages to supply them to the EPD microcontroller.

Note: it is necessary to set the EPD_MCU driver to a status that enables the VOUT1/VEPD power supply to be applied from an external source.

8.2.24 RDCOM: 0x30

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
RDCOM	—	0	1	1	0	0	0	0	Read Command Address
P1	—	B16	B15	B14	B13	B12	B11	B10	RDCOMAD

This command can be issued at all times.

B17 Reserved

B16-B10 RDCOMAD: Read Command Address Bits (Default value:0x31)

This parameter is used to select the address of the command parameter to be read when the command interface is an I2C slave interface (when the IFSEL terminal is set at a low level). Be sure to set this parameter before reading a command parameter. Table 8.2.24 shows the correspondence between read command addresses and commands.

Table 8.2.24 Read command addresses and selected commands

RDCOM[6:0]	Selected command
0x01	CURSDT
0x02	CURBDT
0x03	ATEPDWR1
0x04	ATEPDWR2
0x05	ATEPDWR3
0x06	ATEPDWR4
0x07	ATEPDWR5
0x08	ATEPDWR6
0x09	ATEPDWR7
0x0A	WFSET
0x0B	FMDISB
0x0C	SEGDLEN
0x10	NEXTSDT
0x20	EPDPCTL
0x21	EPDDCTL
0x22	WFSEL
0x23	TEMPSENON
0x24	POWCTL
0x25	IOCTL
0x26	SLVMODE
0x30	RDCOM
0x31	RDSTATE
0x32	DET2CTL
0x33	DROECTL

This parameter is invalid when the SPI slave interface is used (when the IFSEL terminal is set at a high level).

8.2.25 RDSTATE: 0x31

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
RDSTATE	—	0	1	1	0	0	0	1	Read Status
P1(RD)	—	B16	B15	B14	B13	B12	B11	B10	RDSTATE[15:8]
P2(RD)	—	B26	B25	B24	B23	B22	B21	B20	RDSTATE [7:0]

This command reads the state condition flag, display waveform selection status and revision data for this device. See Table 8.2.25 for the correspondence between each bit.

Table 8.2.25 RDSTATE bit table

Bit	Read Flag	0 Output	1 Output
B17	Unused	Fix 0	
B16	Standby status	No	Yes(default)
B15	ATEPDWR1 – 7 operation flag	No(default)	Yes
B14	Internal oscillation operation flag	No(default)	Yes
B13	Power supply startup sequence period flag	No(default)	Yes
B12	Power supply stable period/EPD display update flag 0x0/0x1: Power supply stable period/Other than the EPD display update period 0x2: During the power supply stable period 0x3: During the EPD display update period	0x0 to 0x3 (default:0x0)	
B11			
B10	Temperature sensing period	No(default)	Yes
B27	Unused	Fix 0	
B26	Selected display waveform Flash memory 0x0: Not selected / 0x1: Display waveform 1 / 0x2: Display waveform 2 / 0x3: Display waveform 3 / 0x4: Display waveform 4 / 0x5: Display waveform 5 / 0x6 Display waveform 6 / 0x7: Display waveform 7	0x0 to 0x7 (default:0x0)	
B25			
B24			
B23	Unused	Fix 0	
B22	This device Revision	Fix 0x1	
B21			
B20			

8.2.26 Reserved: 0x32

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
DET2CTL	—	0	1	1	0	0	1	0	Detector2 Control
P1	—	—	B15	—	—	B12	B11	B10	TESTOUT DET2SEL[1:0] DETVEPDON

This command can be issued in stand-by mode (see Section 7.7 State Transition). If the FMDISB command B10 (FMDISB) is 0, issuing this command parameter is not necessary.

B17-B16 Reserved

B15 TESTOUT: Test Out Bit Default value:0x0)

This function is for testing. Set this parameter to 0x0 in normal usage

B14-B13 Reserved

B12-B11 DET2SEL[1:0]: Detector2 Voltage Select Bits (Default value:0x0)

Select this parameter according to the setting of the POWCTL command parameter B15-B14 (VDC2SEL[1:0]). For the relationship between this parameter and the VDC2SEL[1:0], see Table 8.2.26.

Table 8.2.26 DET2SEL[1:0] Selection Table

VDC2SEL[1:0]	DET2SEL[1:0]
0x0	0x0
0x1	0x1
0x2	0x2
0x3	0x3

B10 DET2ON: Detector2 On Bit (Default value:0x0)

Set this parameter to 0x1 in normal usage.

8.2.27 DROECTL: 0x33

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
DROECTL	—	0	1	1	0	0	1	1	Driver Output Enable Control
P1	B17	B16	B15	B14	B13	B12	B11	B10	ESEGOENCTL[7:0]
P2	—	—	—	—	—	—	B21	B20	ETBPOENCTL[1:0]

This command can be issued while in a standby state (refer to Section 7.7, “Status Transition”). There is no need to issue this command parameter when the B10(FMDISB) parameter of the FMDISB command is set to “0”.

Unused terminals can be always set to Hi-Z when there are unused segments, top-planes, or backplanes. (Units for segments: 32 terminals; Units for top-planes/backplanes: 2 terminals)

B17-B10 ESEGOENCTL[7:0]: Epd Segment Output Enable Control Bits(Default value:0x00)

This parameter sets the output status of segments in 32 terminal units. See Table 8.2.27.1 for the correspondence between this parameter and ESEG.

Table 8.2.27.1 ESEGOENCTL[7:0] ESEG Correspondence table

Bit	Corresponding segment	Setting 0	Setting 1
ESEGOENCTL[0]	ESEG0 to ESEG31	Always set to Hi-Z	Output when display/update is performed
ESEGOENCTL[1]	ESEG32 to ESEG63	Always set to Hi-Z	Output when display/update is performed
ESEGOENCTL[2]	ESEG64 to ESEG95	Always set to Hi-Z	Output when display/update is performed
ESEGOENCTL[3]	ESEG96 to ESEG127	Always set to Hi-Z	Output when display/update is performed
ESEGOENCTL[4]	ESEG128 to ESEG159	Always set to Hi-Z	Output when display/update is performed
ESEGOENCTL[5]	ESEG160 to ESEG191	Always set to Hi-Z	Output when display/update is performed
ESEGOENCTL[6]	ESEG192 to ESEG223	Always set to Hi-Z	Output when display/update is performed
ESEGOENCTL[7]	ESEG224 to ESEG255	Always set to Hi-Z	Output when display/update is performed

B27-B22 Reserved

B21-B20 ETBPOENCTL [1:0]: Epd Tp Bp Output Enable Control Bits(Default value:0x0)

This parameter sets the output status of the top-plane or backplane in two terminal units. See Table 8.2.27.2 for the correspondence between ETP and EBP.

Table 8.2.27.2 ETBPCTL[1:0] ETP and EBP Correspondence table

Bit	Corresponding top-plane/ backplane	Setting 0	Setting 1
ETBPOENCTL[0]	ETP0,ETP3,EBP0,EBP3	Always set to Hi-Z	Output when display/update is performed
ETBPOENCTL[1]	ETP1,ETP1,EBP2,EBP2	Always set to Hi-Z	Output when display/update is performed

8.2.28 SWRESET: 0x4A

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
SWRESET	—	0	1	0	1	0	1	0	Software Reset

This command can be issued at all times.

By issuing this command, the internal logic circuit for this device can be initialized from the command interface. After the command is issued, the following operations will be performed.

- Initialization of the command parameters (other than the CURSDT/CURBDT command parameter)
- The system goes into a standby status.

After issuing this command, set the necessary command parameters from the command interface and perform EPD display/update operations.

9. Absolute Maximum Ratings

Table 9 Absolute Maximum Ratings

Item	Symbol	Rating Value		Unit
Power supply voltage (1)	V_{DD}		-0.3 to +7.0	V
Power supply voltage (2)	VD1		-0.3 to +2.5	V
Flash programming voltage	VPP		-0.2 to +8.0	V
EPD drive voltage 1	VOUT1		-0.3 to +7.0	V
EPD drive voltage 2	VEPD		-0.3 to +23.0	V
Input voltage	VI		-0.3 to V_{DD}+0.3	V
Output voltage	VO		-0.3 to V_{DD}+0.3	V
High level output current	IOH	1 pin	-5	mA
		Total for all pins	-20	mA
Low level output current	IOL	1 pin	5	mA
		Total for all pins	20	mA
Allowable loss	VO		200	mW
Working temperature	Ta		-20 to 70	°C
Storage temperature	Tstg		-65 to 150	°C
Soldering temperature and time	Tsol		260 °C, 10 sec (leads)	

- All of the voltages are based on V_{SS} = 0 V.
- If the LSI is used when any of the above absolute maximum ratings is exceeded, the LSI may be destroyed. During normal operation, it is desirable that the LSI be used under conditions that match its electrical characteristics. If these conditions are exceeded, the LSI may malfunction and also its reliability may be adversely affected.
- The value of the storage temperature applies to the bare chip condition.
- The operation of the IC is guaranteed when the IC is operated under conditions that match its electrical characteristics.
- Insert a bypass capacitor near the power supply pins as a noise countermeasure.

10. Electrical Characteristics

10.1 DC Characteristics

Table 10.1 DC characteristics

If not specified V_{DD}=1.75V to 5.50V, Ta=-20 °C to 70 °C

Item	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage (1)	V_{DD}	—	1.75	—	5.50	V
Flash programming voltage	V_{PP}	—	6.80	7.00	7.20	V
EPD drive voltage 1	VOUT1	—	5.20	—	6.00	V
EPD drive voltage 2-1	VEPD1	—	—	9.15	—	V
EPD drive voltage 2-2	VEPD2	—	—	12.30	—	V
EPD drive voltage 2-3	VEPD3	—	—	15.45	—	V
High level input voltage	VIH	XSTA,VD1SEL pin	0.7V_{DD}	—	V_{DD}	V
Low level input voltage	VIL	XSTA,VD1SEL pin	V_{SS}	—	0.3V_{DD}	V
High level Schmitt input Threshold voltage	VT+	*Note1	0.5V_{DD}	—	0.9V_{DD}	V
Low level Schmitt input Threshold voltage	VT-	*Note1	0.1V_{DD}	—	0.5V_{DD}	V
Current flowing through input pull-up resistor	RIN	VIL=0V XMFS pin	—	—	-50	μA
High level output voltage	VOH	IOH=-300μA *Note2	V_{DD}-0.2	—	V_{DD}	V
Low level output voltage	VOL	IOL=300μA *Note2	V_{SS}	—	V_{SS}+0.2	V
Standby current 1	IDDQ1	Ta=25°C Deep Standby （XSTA=L）	—	0.06	1.00	μA
Standby current 2	IDDQ2	Standby （XSTA=H）	—	40	60	μA
Operation current 1	IDDOP1	*Note4	—	410	550	μA
Operation current 2	IDDOP2	*Note5	—	380	570	μA
Operation current 3	IDDOP3	*Note6	—	330	400	μA
Operation current 4	IDDOP4	*Note7	—	290	400	μA
Input current	ILI	V_{SS}≦VIN≦V_{DD} *Note3	-100	—	100	nA
Input capacity	CI	Frequency=1MHz Ta=25°C individual chip *Note3	—	—	15	pF
Output capacity	CO	Frequency=1MHz Ta=25°C,individual chip *Note8	—	—	15	pF
Internal oscillation	FOSC	—	1.90	2.00	2.10	MHz
Temperature detect circuit precision	TEMP	-10°C to 60°C	-5	—	5	°C

Table 10.2 Inrush Current

Ta=25°C

Item	Symbol	Condition	Typ	Unit
Inrush Current(during booster warm-up 1)	INRUSHDCDC1	*Note4	25	mA
Inrush Current(during booster warm-up 2)	INRUSHDCDC2	*Note5	25	mA
Inrush Current(during booster warm-up 3)	INRUSHDCDC3	*Note6	30	mA
Inrush Current(during booster warm-up 4)	INRUSHDCDC4	*Note7	40	mA

*Note1 : Applicable input pin — SLVSEL, IFSEL, OS, XMFS, MFC, MFDI, EPDCLK, EPDTRG, SCL, SDA, I2C_AD0 / XSCS, I2C_AD1

*Note2 : Applicable input pin — MFDO,EPDCLK,EPDTRG,SDO,SDA

*Note3 : Applicable input pin — XSTA, VD1SEL, SLVSEL, IFSEL, OS, XMFS, MFC, MFDI, EPDCLK, EPDTRG, SCL, SDA, I2C_AD0 / XSCS, I2C_AD1, TESTEN, TESTMOD0, TESTMODE1, TESTFOFF

*Note4 : Operation conditions — Current consumption during the EPD display/update period

V_{DD}=1.75V to 3.60V. Primary boost: Set to three times the original voltage. Secondary boost: Boosted to three times the original voltage (15.45V).

Connect a flying capacitor (0.1 μF) between C11P and C11N, between C12P and C12N, between C11P and C11N, between C12P and C12N, and between VOUT1 and V_{SS}, and between VEPD and V_{SS}.

Stabilizing capacitors (0.1μF) are placed between VOUT1-V_{SS} and between VEPD-V_{SS}.

Primary step-up clock frequency: 62.5KHz. Secondary step-up clock frequency: 32KHz.

Current consumption when the IC itself has no load

*Note5 : Operation conditions — Current consumption during the EPD display/update period

V_{DD}=3.00V to 5.50V. Primary boost: Set to two times the original voltage. Secondary boost: Boosted to three times the original voltage (15.45V).

Connect a flying capacitor (0.1 μF) between C11P and C11N, between C12P and C12N, between C11P and C11N, between C12P and C12N, and between VOUT1 and V_{SS}, and between VEPD and V_{SS}.

Stabilizing capacitors (0.1uF) are placed between VOUT1-V_{SS} and between VEPD-V_{SS}.

Primary step-up clock frequency: 62.5KHz. Secondary step-up clock frequency: 32KHz.

Current consumption when the IC itself has no load

*Note6 : Operation conditions — Current consumption during the EPD display/update period

V_{DD}=1.75V to 3.60V. Primary boost: Set to three times the original voltage. Secondary boost: Boosted to three times the original voltage (15.45V).

	Connect a flying capacitor (0.1 μF) between C11P and C11N, between C12P and C12N, between C11P and C11N, between C12P and C12N, and between VOUT1 and VSS, and between VEPD and VSS.
	Stabilizing capacitors (0.1uF) are placed between VOUT1-VSS and between VEPD-VSS.
	Primary step-up clock frequency: 62.5KHz. Secondary step-up clock frequency: 32KHz.
	Current consumption when the IC itself has no load
*Note7 : Operation conditions	Current consumption during the EPD display/update period
	VDD=3.00V to 5.50V. Primary boost: Set to two times the original voltage. Secondary boost: Boosted to three times the original voltage (15.45V).
	Connect a flying capacitor (0.1 μF) between C11P and C11N, between C12P and C12N, between C11P and C11N, between C12P and C12N, and between VOUT1 and VSS, and between VEPD and VSS.
	Stabilizing capacitors (0.1uF) are placed between VOUT1-VSS and between VEPD-VSS.
	Primary step-up clock frequency: 62.5KHz. Secondary step-up clock frequency: 32KHz.
	Current consumption when the IC itself has no load
*Note8 : Applicable output pin	MFDO,EPDCLK,EPDTRG,SDO,ESEG0-255,EBP0-3,ETP0-3

10.2 AC Characteristics

10.2.1 I2C Slave Interface

Table 10.2.1 I2C slave interface AC characteristics [Note 1]

Item	Symbol	100KHz access (Standard-Mode)		400KHz access (Fast-Mode)		Unit
		Min.	Max.	Min.	Max.	
SCL clock time	f_{SCL}	—	100	—	400	kHz
SCL LOW time	f_{LOW}	4.7	—	1.3	—	µs
SCL HIGH time	t_{HIGH}	4.0	—	0.6	—	µs
Startup condition setup time	$t_{SU;STA}$	4.7	—	0.6	—	µs
Startup condition hold time	$t_{HD;STA}$	4.0	—	0.6	—	µs
Shutdown condition setup time	$t_{SU;STO}$	4.0	—	0.6	—	µs
Data setup time	$t_{SU;DAT}$	250	—	100	—	ns
Data hold time	$t_{HD;DAT}$	0	—	0	—	µs
SDA fall time [Note 2]	t_f [Note 2]	—	0.3	—	0.3	µs
Bus-free time between the startup conditions and the shutdown conditions	t_{BUF}	4.7	—	1.3	—	µs

Note 1: V_{DD} = 1.75 V to 5.50 V, Ta = -20 °C to 70 °C.

The timing of input signals is set to 30% and 70% of the voltage between V_{DD} and V_{SS} as reference points.

The timing of output signals is set to 20% and 80% of the voltage between V_{DD} and V_{SS} as reference points.

The rise time of SCL/SDA is as follows.

- For 100KHz access (Standard-Mode) : Within 1.0 µs
- For 400KHz access (fast-Mode) : Within 0.3 µs

The fall time of SCL/SDA of the master device IC is as follows.

- For 100KHz access (Standard-Mode) : Within 0.3 µs
- For 400KHz access (fast-Mode) : Within 0.3 µs

Note 2: Specifications under the condition capacitance: 220pF, pull-up resistor: 3.3KΩ.

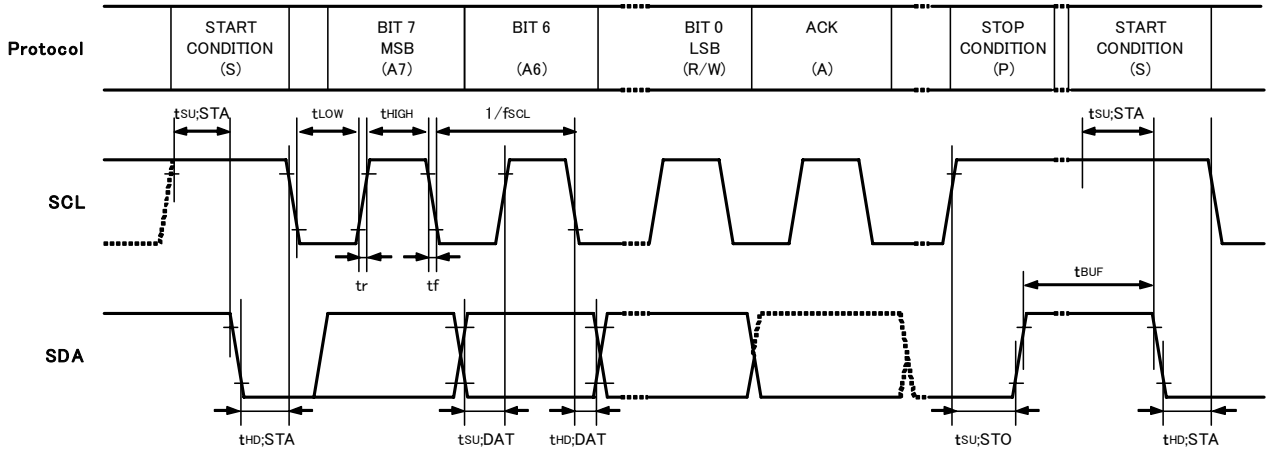

Figure 10.2.1 I2C slave interface AC characteristics diagram

10.2.2 SPI Slave Interface

Table 10.2.2 SPI slave interface AC characteristics [Note]

Item	Symbol	Min.	Max.	Unit
XSCS setup time	tSCSS	100	—	ns
XSCS hold time	tSCSH	100	—	ns
XSCS HIGH time	tSCSW	100	—	ns
SCL clock time (write)	tSCLCYCW	200	—	ns
SCL HIGH time (write)	tSCLHW	50	—	ns
SCL LOW time (write)	tSCLLW	50	—	ns
SCL clock time (read)	tSCLCYCR	200	—	ns
SCL HIGH time (read)	tSCLHR	100	—	ns
SCL LOW time (read)	tSCLLR	100	—	ns
Data setup time	tSDAS	50	—	ns
Data hold time	tSDAH	50	—	ns
Data output time [Note 2]	tSACC [Note 2]	—	100	ns

Note 1: V_{DD}=1.75V to 5.50V, Ta=-20 °C to 70 °C

The rise time (tr) and fall time (tf) of the input signal are stipulated as 15 ns or less.

The timing is specified based on 30% and 70% of V_{DD}-V_{SS}.

Note 2: When the terminal itself has no load

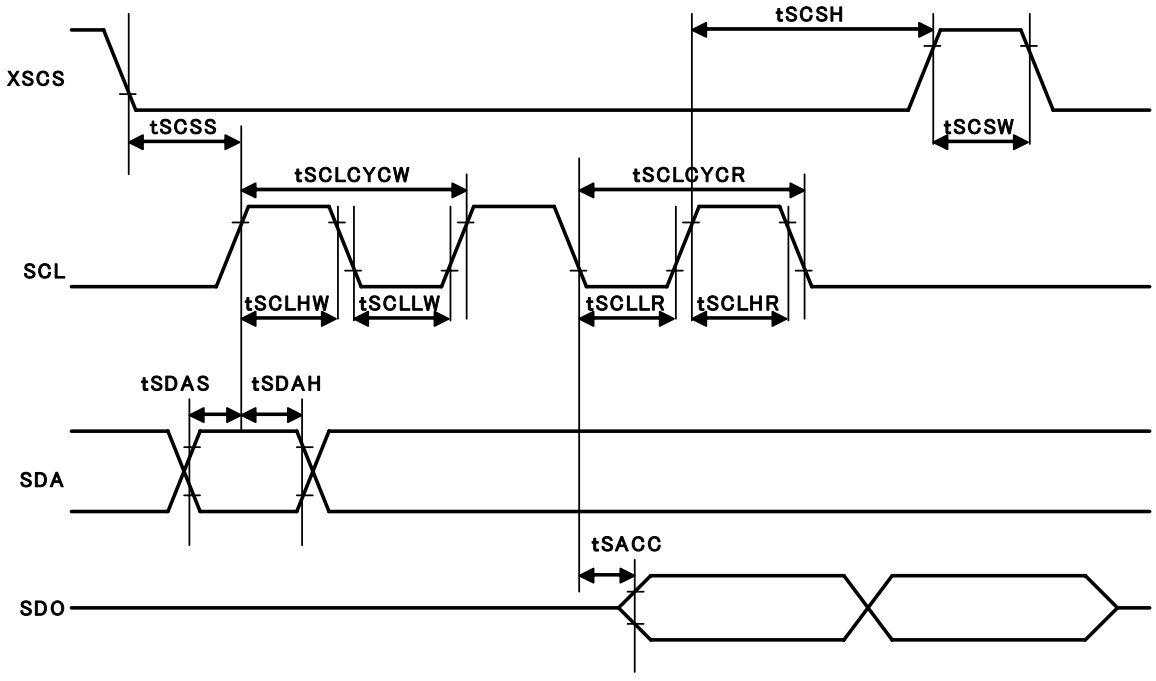

Figure 10.2.2 SPI slave interface AC characteristics diagram

10.2.3 Deep Standby Control

Table 10.2.3 Deep standby control AC characteristics [Note 1]

Item	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
XSTA	tXSTALW	XSTA Low Pulse Width	1	—	—	ms	
	tPORC	Power On Reset Cancel Time	200	—	—	µs	

Note 1: V_{DD}=1.75V to 5.50V, Ta=-20 °C to 70 °C

The rise time (tr) and fall time (tf) of the input signal are stipulated as 15 ns or less.

The timing is stipulated based on 30% and 70% of V_{DD}-V_{SS}.

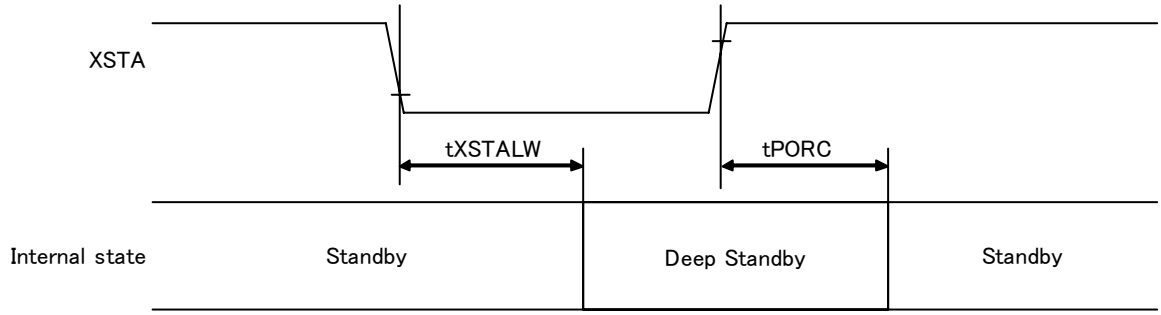

Figure 10.2.3 Deep standby control AC characteristics diagram

10.2.4 ESEG Output Delay

Table 10.2.4 ESEG output delay [Note 1]

Item	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
ESEGxxx	tESEGST	ESEG Out Setting Time	—	—	500	ns	

Note 1: VDD=1.75V to 5.50V, VEPD=9.0 to 15.45V, Ta=-20 °C to 70 °C

The timing of EPDCLK is stipulated based on 30% and 70% of VDD-VSS.

The ESEG0 to 255 timing is stipulated based on 20% and 80% of VEPD-VSS.

Note 2: When the terminal itself has no load

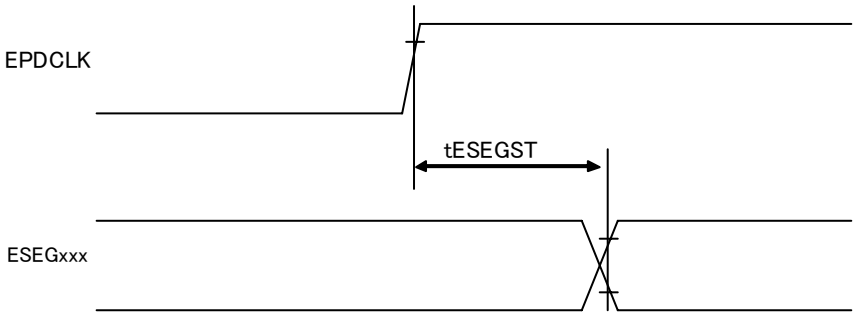

Figure 10.2.4 ESEGxx output delay diagram

10.2.5 ETP Output Delay

Table 10.2.5 ETP output delay [Note 1]

Item	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
ETPx	tETPT	ETP Out Setting Time	—	—	500	ns	

Note 1: VDD=1.75V to 5.50V, VEPD=9.0 to 15.45V, Ta=-20 °C to 70 °C

The timing of EPDCLK is stipulated based on 30% and 70% of VDD-VSS.

The ETP0 to 3 timing is stipulated based on 20% and 80% of VEPD-VSS.

When the terminal itself has no load

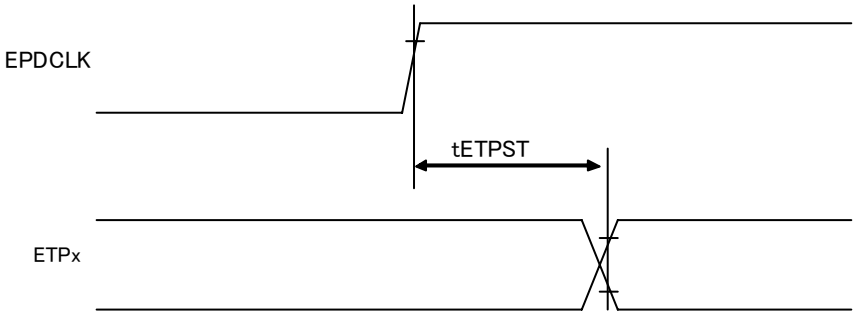

Figure 10.2.5 ETP output delay diagram

10.2.6 EBP Output Delay

Table 10.2.6 EBP output delay [Note 1]

Item	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
EBPx	tEBPT	EBP Out Setting Time	—	—	500	ns	

Note 1: VDD=1.75V to 5.50V, VEPD=9.0 to 15.45V, Ta=-20 °C to 70 °C

The timing of EPDCLK is stipulated based on 30% and 70% of VDD-VSS.

The EBP0 to 3 timing is stipulated based on 20% and 80% of VEPD-VSS.

When the terminal itself has no load

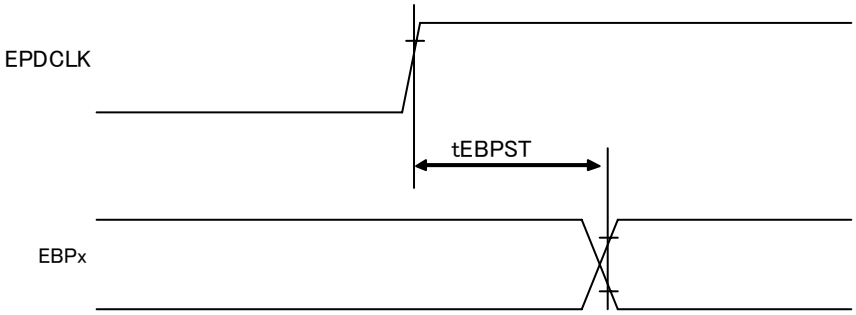

Figure 10.2.6 EBP output delay diagram

10.2.7 EPDCLK,EPDTRG Output Delay

Table 10.2.7 EPDTRG,EPDCLK output delay [Note1]

Item	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
EPDTRG	tEPDCLK	EPDCLK Out Settling Time	—	—	100	ns	
EPDCLK	tEPDTRG	EPDTRG Out Settling Time	—	—	100	ns	

Note 1: VDD=1.75V to 5.50V, Ta=-20 °C to 70 °C

The timing of input signals is set to 30% and 70% of the voltage between VDD and VSS as reference points.

The timing of output signals is set to 20% and 80% of the voltage between VDD and VSS as reference points.

When the terminal itself has no load

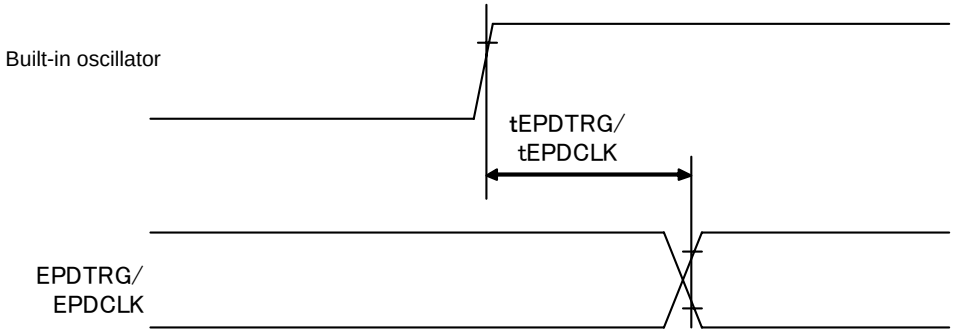

Figure 10.2.7 EPDCLK, EPDTRG output delay diagram

11. Basic External Connecting Diagram

11.1 Example of a connecting diagram when this device stands alone (When all ESEG terminals are used)

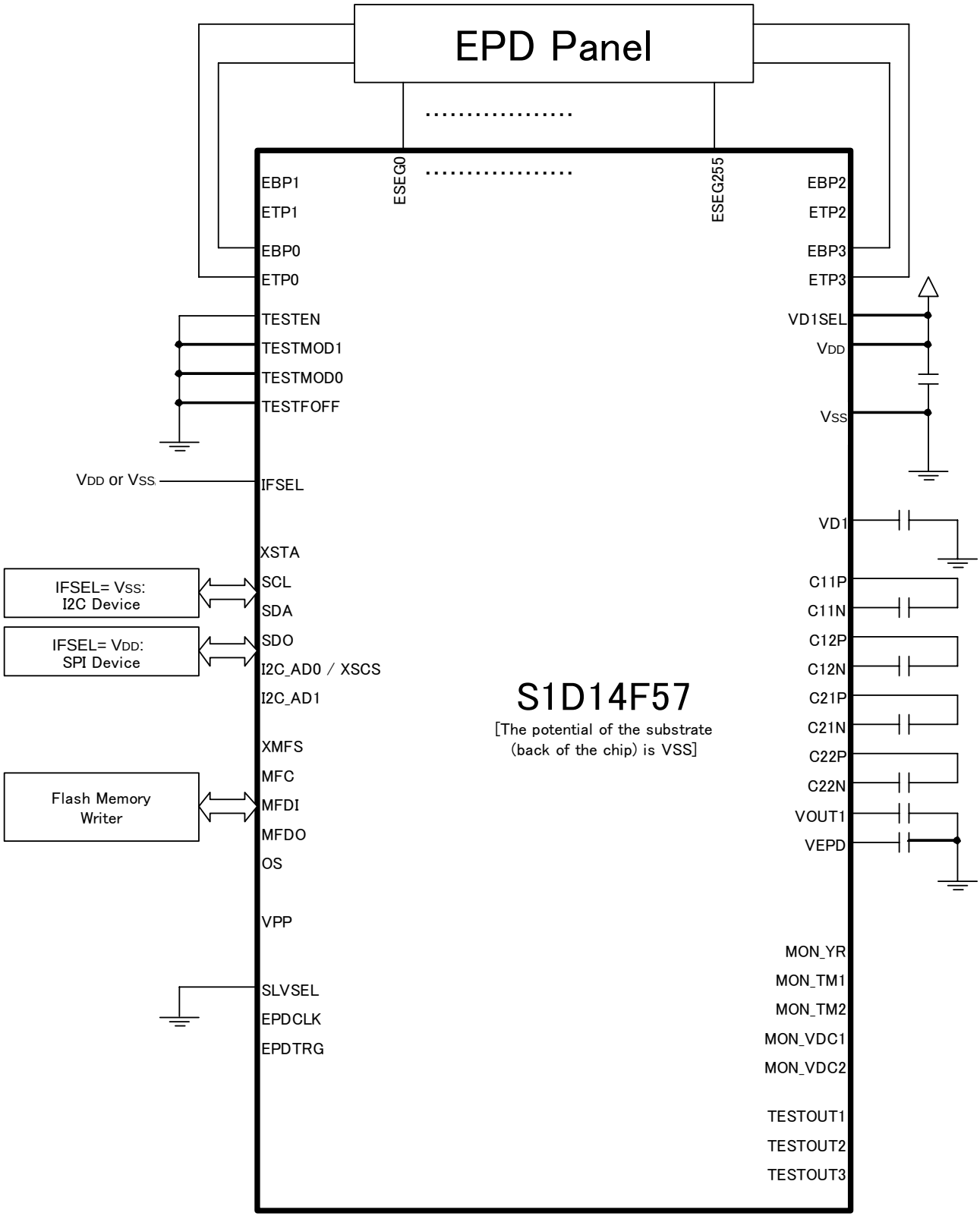

Figure 11.1 Sample wiring diagram when this device is used alone (ESEG256)

11.2 Example of Connecting Diagram for EPD_MCU Driver Expansion (When the ESEG 192 terminal is used)

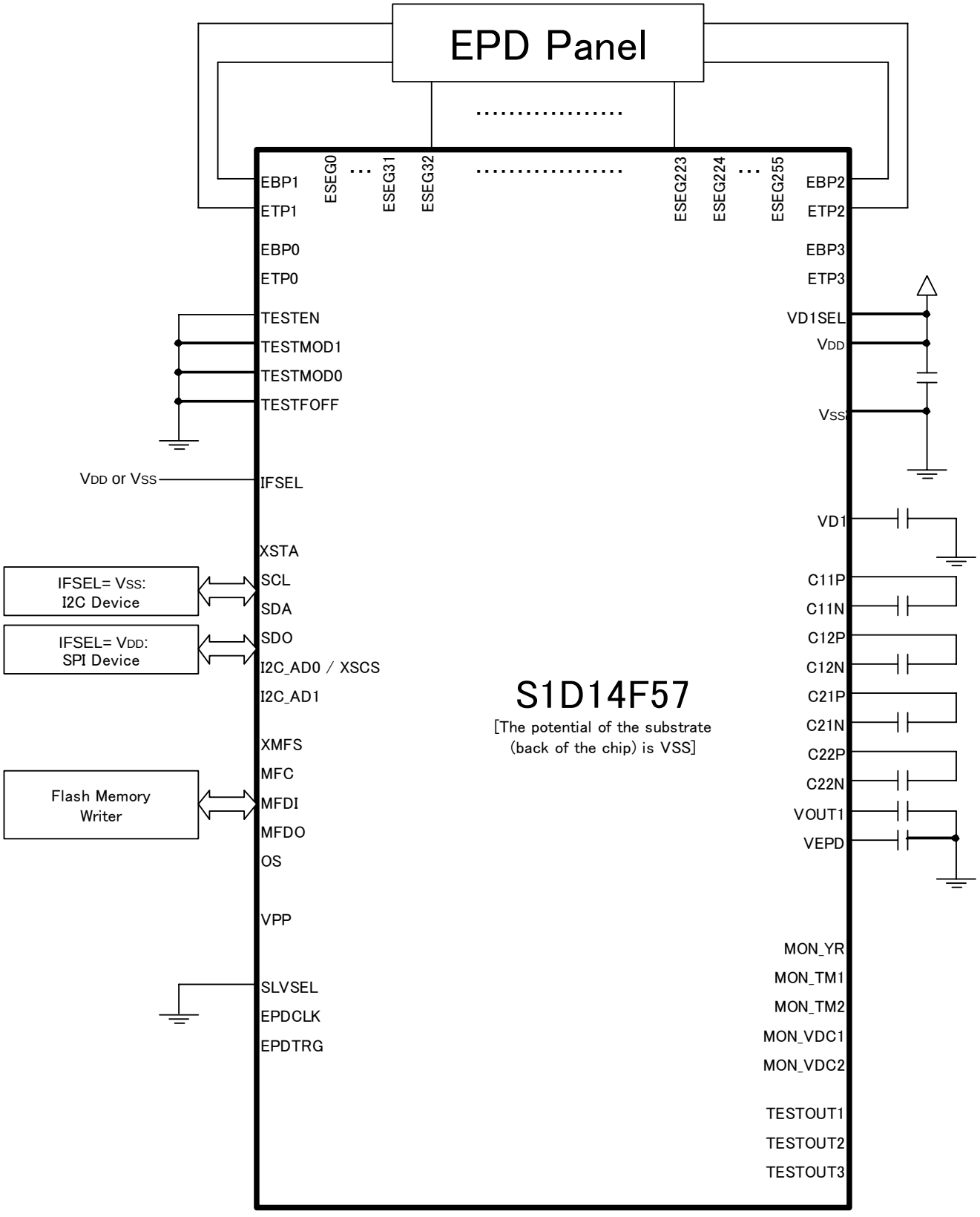

Figure 11.2 Sample wiring diagram when this device is used alone (ESEG192)

11.3 Sample wiring diagram when the EPD microcomputer is extended

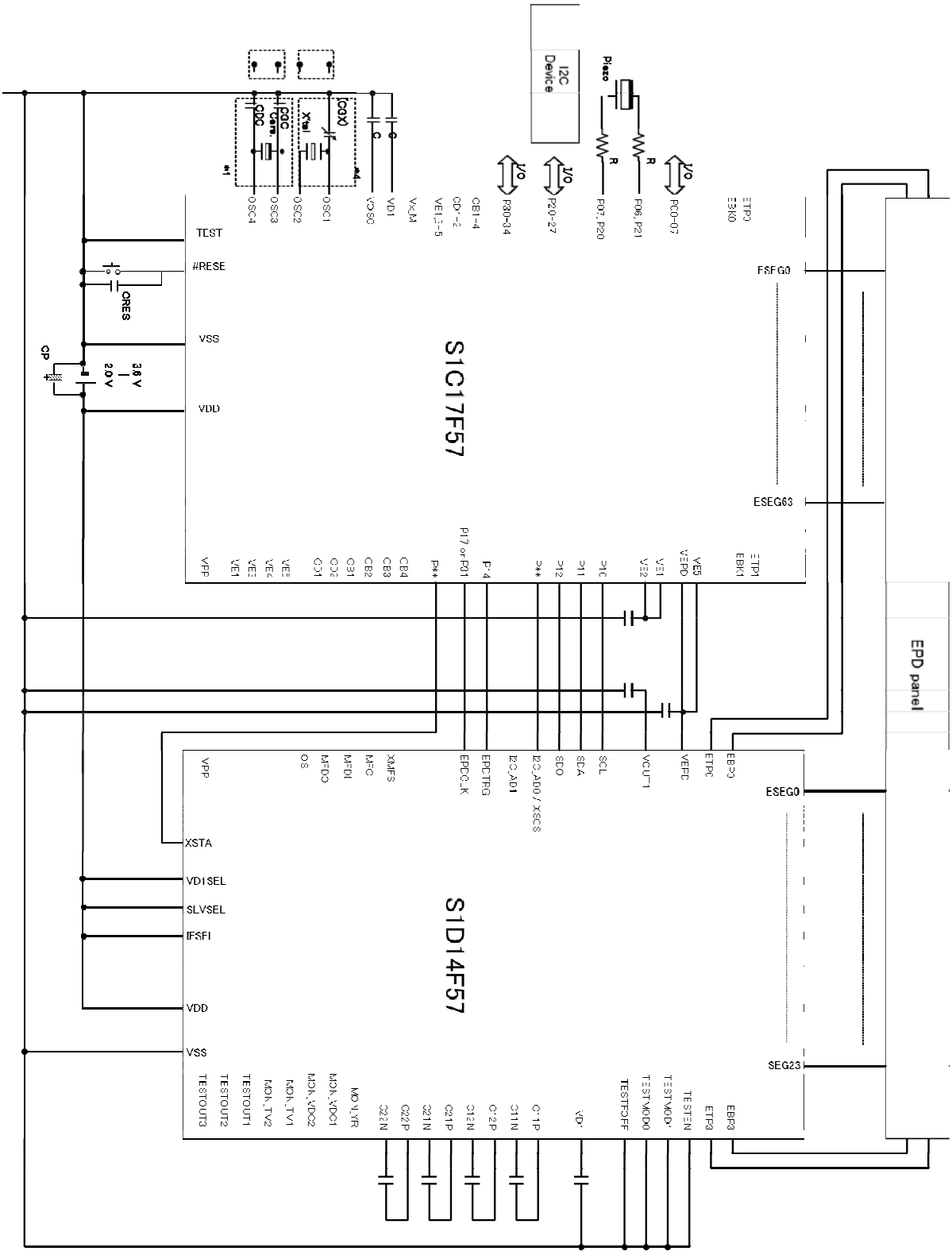

Figure 11.3 Sample wiring diagram when the EPD microcomputer is extended

Note: This is a sample wiring diagram for when Seiko Epson's EPD microcomputer S1C17F57 is used.

11.4 Sample wiring diagram when the device multichip is extended

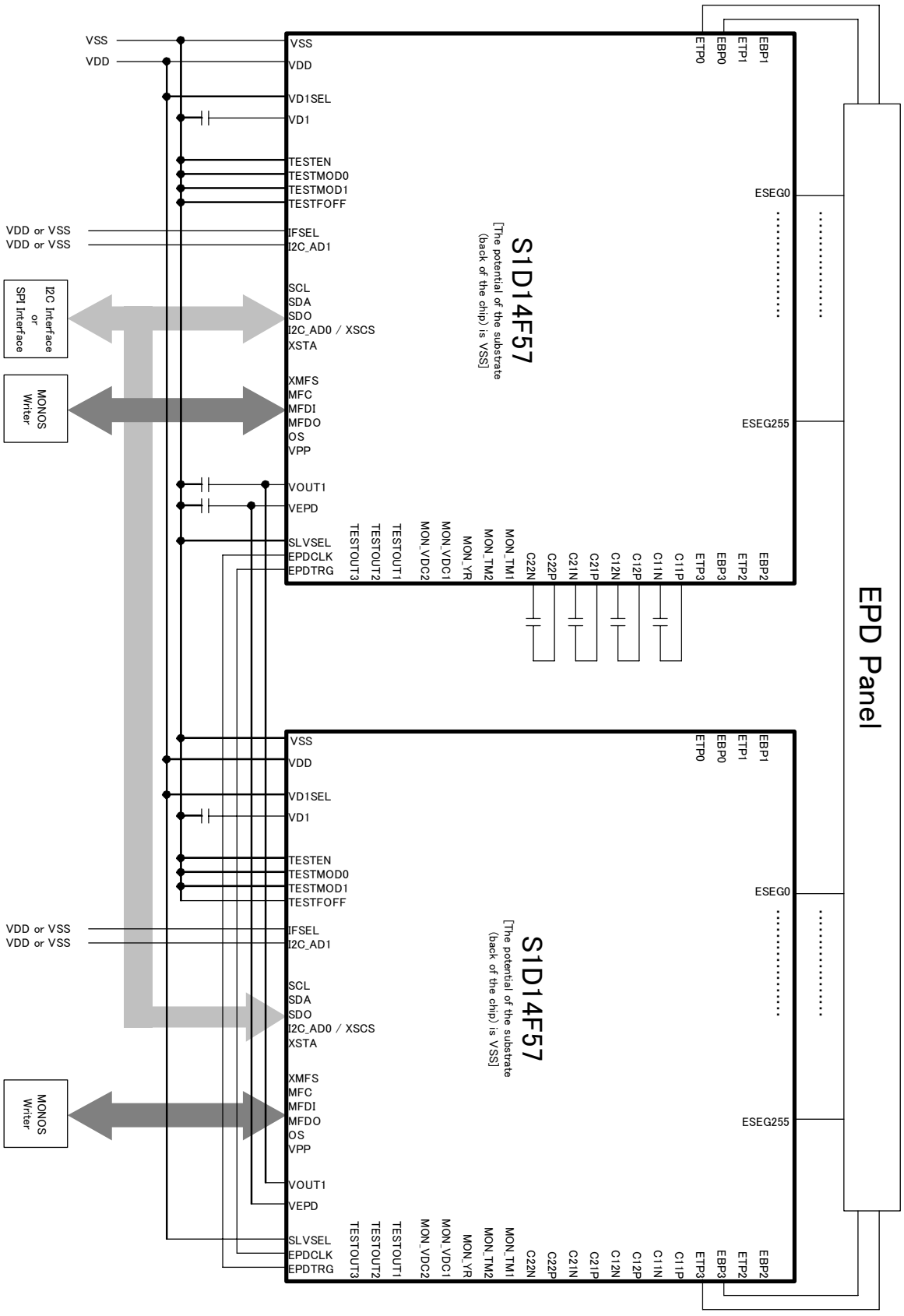

Figure 11.4 Sample wiring diagram when the device multichip is extended

Revision History

Attachment-1

Rev. No.	Date	Page	Category	Contents
Rev.1.0	2011/06/01	All	New	

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