

S1C31D50/51/41 (rev3.01)

EPSON

32-bit Single Chip **Sound Microcontroller**

- Arm® 32-bit RISC CPUcore Cortex®-M0+
- D50:192K / D51:192K / D41:96K bytes Embedded Flash memory
- D50:8K / D51:10K / D41:8K bytes embedded RAM
- Provide Voice Guidance on a buzzer in addition to a speaker
- "Voice/Audio Play"(2ch mixing play, Voice Speed Conversion w/o CPU resource)
- Voice Pitch Conversion Function(only S1C31D41)
- ±1%(@Ta=0 to 85℃) 16MHzinternal Oscillator (only S1C31D41)

arm

■ DESCRIPTIONS

The S1C31D51/D50/D41 is a 32-bit Arm® Cortex®-M0+ MCU which integrates a specific hardware block called the HW Processor, 2type Embedded Flash size 192K(D50/D51)/96K(D41) bytes is supported. Normally, the buzzer does not provide sufficient voice quality and sound pressure, but our newly developed algorithm allows the buzzer to play the voice, and even devices that could not be equipped with a speaker and voice guidance can generate an error or warning, and can improve usability for the end user. The HW Processor can perform 2ch Voice/Audio Play, Voice Speed Conversion, and Self Memory Check without using any CPU resource, and the S1C31D51/D50/D41 is suitable for home electronics, white goods, and battery-based products which require voice and audio playback. In addition, the audio playback format uses a high-compression, high-quality sound algorithm, which makes it possible to install multiple languages. Furthermore, the EPSON Voice Creation PC tool makes development without studio recording easy

■ FEATURES

Model	S1C31D50	S1C31D51	S1C31D41
CPU			
CPU core	Arm® 32-bit RISC CPU core Cortex®-M0+		
Other	Serial-wire debug ports (SW-DP) and a micro trace buffer (MTB) included		
Embedded Flash memory			
Capacity(for Program&SoundROM)	192K bytes		96K bytes
Erase/program count	1,000 times (min.) * When being programmed by the dedicated flash loader		
Other	On-board programming function Flash programming voltage can be generated internally.		
Embedded RAMs			
General-purpose RAM (under HW Processor is not active)	8K bytes (+ 14K bytes)	10K bytes (+ 12K bytes)	8K bytes (+ 18K bytes)
Instruction cache	-		512 bytes
HW Processor	ver1.00	ver2.00	ver3.00
Sound Play FUNCTION			
Voice/Audio Algorithm	EPSON high quality & High compress algorithm		
Play channels	2ch mixing support(suitable for background music + Voice play)		
Sampling Frequency	15.625kHz, (suitable for Back Ground Music + Voice play)		
Bitrate	EOV:16/24/32/40 kbps		EOV:16/24 kbps
Multi-SoundROM	supported		
Gapless play	supported		
Volume setting	Supported(0db to -63.0db:0.5db step, silence)		
Repeat time setting	Supported(1time to 255times, repeat until stop command receive)		
Voice Speed Conversion	Ver1.00	Ver2.00 75% - 125% (5% step)	
Voice Pitch Conversion	-		75% - 125% (5% step)
Tone Generation	-		supported
Electromagnetic/Piezoelectric buzzer Voice/Melody	-		supported
Self Memory Check FUNCTION			
On Chip RAM Check	W/R Check, MARCH-C		
On Chip Flash check	Checksum, CRC		
External SPI-Flash Check	Checksum, CRC		
Sound DAC			
Sampling Frequency	15.625kHz		
External Differential Circuit Speaker DAC/Electromagnetic Buzzer DAC/Piezoelectric buzzer DAC			
Sampling Frequency (requires to use 16bit PWM Timer(T16B)1ch)	-		15.625kHz

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Model	S1C31D50	S1C31D51	S1C31D41
Serial interfaces			
UART (UART3)	3 channels Baud-rate generator included, IrDA1.0 supported Open drain output, signal polarity, and baud rate division ratio are configurable. Infrared communication carrier modulation output function		
Synchronous serial interface (SPIA)	3 channels 2 to 16-bit variable data length The 16-bit timer (T16) can be used for the baud-rate generator in master mode.		
Quad synchronous serial interface (QSPI)	1 channel Supports single, dual, and quad transfer modes. Low CPU overhead memory mapped access mode that can directly read data from the external flash memory with XIP (eXecute-In-Place) mode.		
I ² C (I2C)*1	3 channels Baud-rate generator included		
DMA Controller (DMAC)			
Number of channels	4 channels		
Data transfer path	Memory to memory, memory to peripheral, and peripheral to memory		
Transfer mode	Basic, ping-pong, scatter-gather		
DMA trigger source	UART3, SPIA, QSPI, I2C, T16B, ADC12A, and software		
Clock generator (CLG)			
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)		
System clock frequency (operating frequency)	V _{D1} voltage mode = mode0: 16.0MHz (max.) V _{D1} voltage mode = mode1: 1.8MHz (max.)		
IOSC oscillator circuit (boot clock source)	V _{D1} voltage mode = mode0: 8/2/1MHz (typ.) software selectable V _{D1} voltage mode = mode1: 1.9/0.9 MHz (typ.) software selectable 10 μs (max.) starting time (time from cancelation of SLEEP state to vector table)		
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator 32kHz (typ.) embedded oscillator Oscillation stop detection circuit included		
OSC3 oscillator circuit	16 MHz (max.) crystal/ceramic oscillator 16/8/4MHz(typ) embedded oscillator		16/8/4MHz(typ) embedded oscillator(8/4MHz:divie16MHz) ±1%@T_a=0~85°C
EXOSC clock input	16 MHz (max.) square or sine wave input		
Other	Configurable system clock division ratio Configurable system clock used at wake up from SLEEP state Operating clock frequency for the CPU and all peripheral circuits is selectable.		
I/O port (PPORT)			
Number of general-purpose I/O ports	PKG48pin : 39bit(max.) PKG64pin : 55bit(max.) PKG80pin : 71bit(max.) PKG100pin : 91bit (max.) Pins are shared with the peripheral I/O.		PKG32pin : 25bit(max.) PKG48pin : 39bit(max.) PKG64pin : 55bit(max.)
Number of input interrupt ports	PKG48pin : 33bit(max.) PKG64pin : 49bit(max.) PKG80pin : 65bit(max.) PKG100pin : 85bit (max.)		PKG32pin : 21bit(max.) PKG48pin : 35bit(max.) PKG64pin : 51bit(max.)
Number of ports that support universal port multiplexer (UPMUX)	PKG48pin : 16bit(max.) PKG64pin : 24bit(max.) PKG80pin : 27bit(max.) PKG100pin : 32bit (max.) A peripheral circuit I/O function selected via software can be assigned to each port.		PKG32pin : 9bit(max.) PKG48pin : 20bit(max.) PKG64pin : 32bit(max.)
Timers			
Watchdog timer (WDT2)	Generates NMI or watchdog timer reset. Programmable NMI/reset generation cycle		
Real-time clock (RTCA)	128–1 Hz counter, second/minute/hour/day/day of the week/month/year counters Theoretical regulation function for 1-second correction Alarm and stopwatch functions		
16-bit timer (T16)	8 channels Generates the SPIA and QSPI master clocks, and the ADC12A operating clock/		
16-bit PWM timer (T16B)	2 channels Event counter/capture function PWM waveform generation function Number of PWM output or capture input ports: 4 ports/channel		
12-bit A/D converter (ADC12A)			
Conversion method	Successive approximation type		
Resolution	12 bits		
Number of conversion channels	1 channel		
Number of analog signal inputs	8 ports/channel (max)		

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Model	S1C31D50	S1C31D51	S1C31D41
Supply voltage detector (SVD3)			
Number of channels	1 channel		
Detection voltage	V _{DD} or an external voltage (2 external detection ports are available.)		
Detection level	V _{DD} : 28 levels (1.8 to 5.0 V)/external voltage: 32 levels (1.2 to 5.0 V)		
Other	Intermittent operation mode Generates an interrupt or reset according to the detection level evaluation.		
Temperature sensor/reference voltage generator (TSRVR)			
Temperature sensor circuit	-		Sensor output can be measured using ADC12A.
Reference voltage generator	-		Reference voltage for ADC12A is selectable from 2.0 V, 2.5 V, V _{DD} , and external input.
R/F converter (RFC)			
Conversion method	CR oscillation type 24-bit counters		
Number of conversion channels	1 channel		
Supported sensors	DC bias resistive sensors		
IR remote controller (REMC3)			
Number of transmitter channels	1 channel		
Other	EL lamp drive waveform can be generated (by the hardware) for an application example. Output inversion function		
Reset			
#RESET pin	Reset when the reset pin is set to low.		
Power-on reset	Reset at power on.		
Brown-out reset	Reset when the power supply voltage drops (when V _{DD} ≤ 1.45 V (typ.) is detected).		
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).		
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/		
Interrupt			
Non-maskable interrupt	6 systems (Reset, NMI, HardFault, SVCALL, PendSV, SysTic)		
Programmable interrupt	External interrupt: 3 systems Internal interrupt: 27 systems		
Power supply voltage			
V _{DD} operating voltage	1.8 to 5.5 V * If V _{DD} > 3.6 V, the V _{D1} voltage mode must be mode0.		
V _{DD} operating voltage for Flash programming	2.4 ~ 5.5 V		2.2 ~ 5.5 V
SPI-Flash interface power supply VDDQSPI	3.0 to 3.6V(possible to set main VDD:5v, SPI-Flash power supply :3.3v)		
Operating temperature			
Operating temperature range	-40 to 85 °C		
Current consumption (Typ. value)			
SLEEP mode *2	IOSC = OFF, OSC1 = OFF, OSC3 = OFF		
	0.46 μA		0.34 μA
	IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OSC3 = OFF, RTCA = ON		0.9 μA
HALT mode *3	IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OSC3 = OFF		
	1.8 μA		1.5 μA
RUN mode	V _{D1} voltage mode = mode0, CPU = OSC3 (16MHz)		
	243 μA/MHz		215 μA/MHz
	V _{D1} voltage mode = mode1, CPU = IOSC (2MHz)		
	155 μA/MHz		130 μA/MHz
Shipping form *4			
1	-		P-TQFP032-0707-0.80 (7mm x 7mm, 0.8mm pitch)
2	P-TQFP048-0707-0.50 (7mm x 7mm, 0.5mm pitch)		
3	P-LQFP064-1010-0.50 (10mm x 10mm, 0.5mm pitch)		
4	P-LQFP080-1212-0.50 (12mm x 12mm, 0.5mm pitch)		-
5	P-LQFP100-1414-0.50 (14mm x 14mm, 0.5mm pitch)		-

*1 The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns.

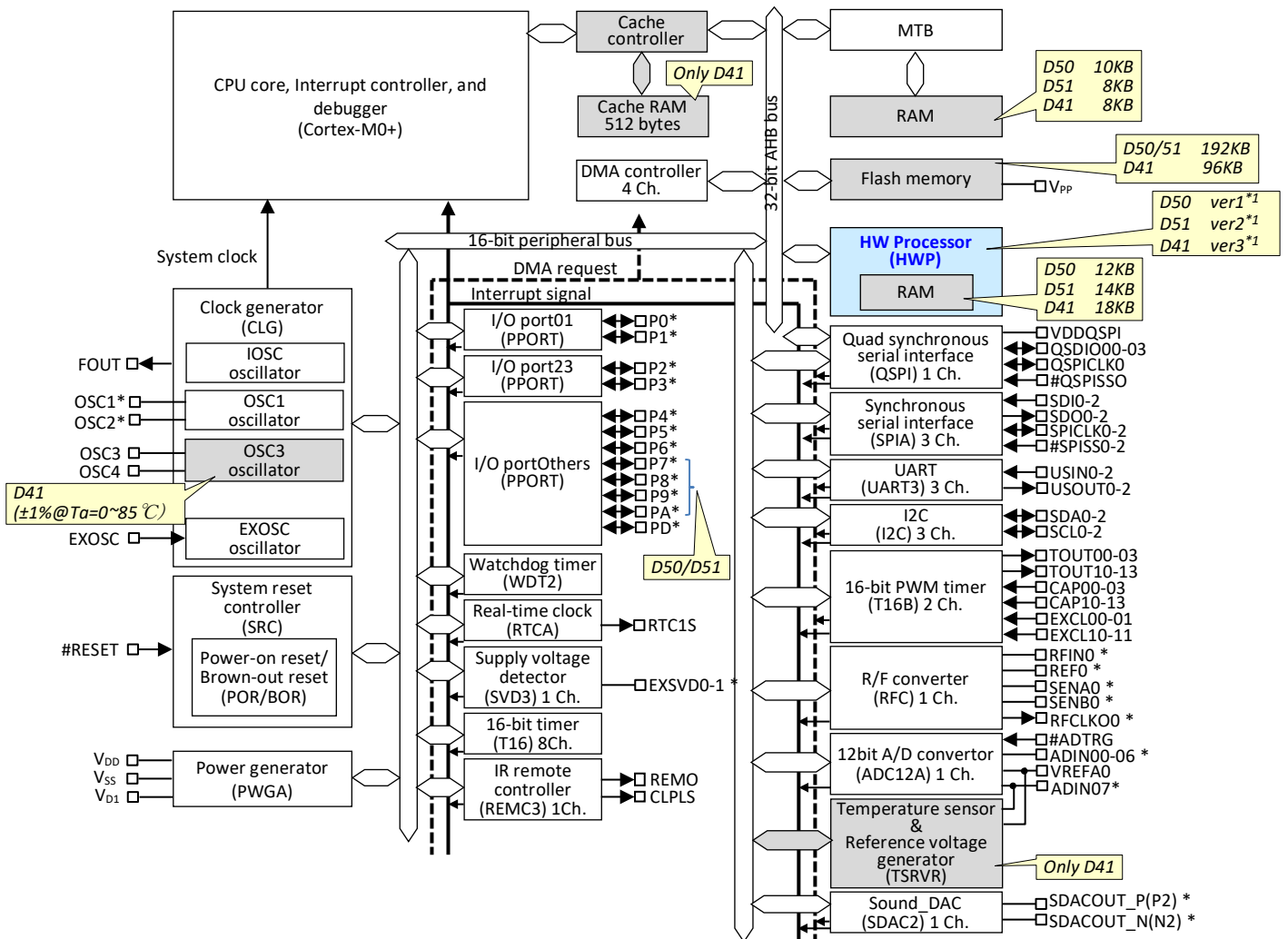
*2 SLEEP mode refers to deep sleep mode in the Cortex®-M0+ processor.

*3 HALT mode refers to sleep mode in the Cortex®-M0+ processor.

*4 Shown in parentheses are JEITA package names.

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Block Diagram



* The pin configuration depends on the package. For detailed information, refer to Section "Pins."

*1 HW Processor Specification

•Sound Play Function

Model	HWP version	2ch Sound Play	Multi-SoundROM	Volume Setting	Repeat Setting	Voice Speed Conversion	Gapless Play	Buzzer Voice/Melody	Voice Pitch Conversion	Tone Generation
S1C31D50	1.00	✓	✓	✓	✓	√(ver1.00)	-	-	-	-
S1C31D51	2.00					√(ver2.00)	✓	✓	✓	✓
S1C31D41	3.00								✓	✓

•Memory Check Function

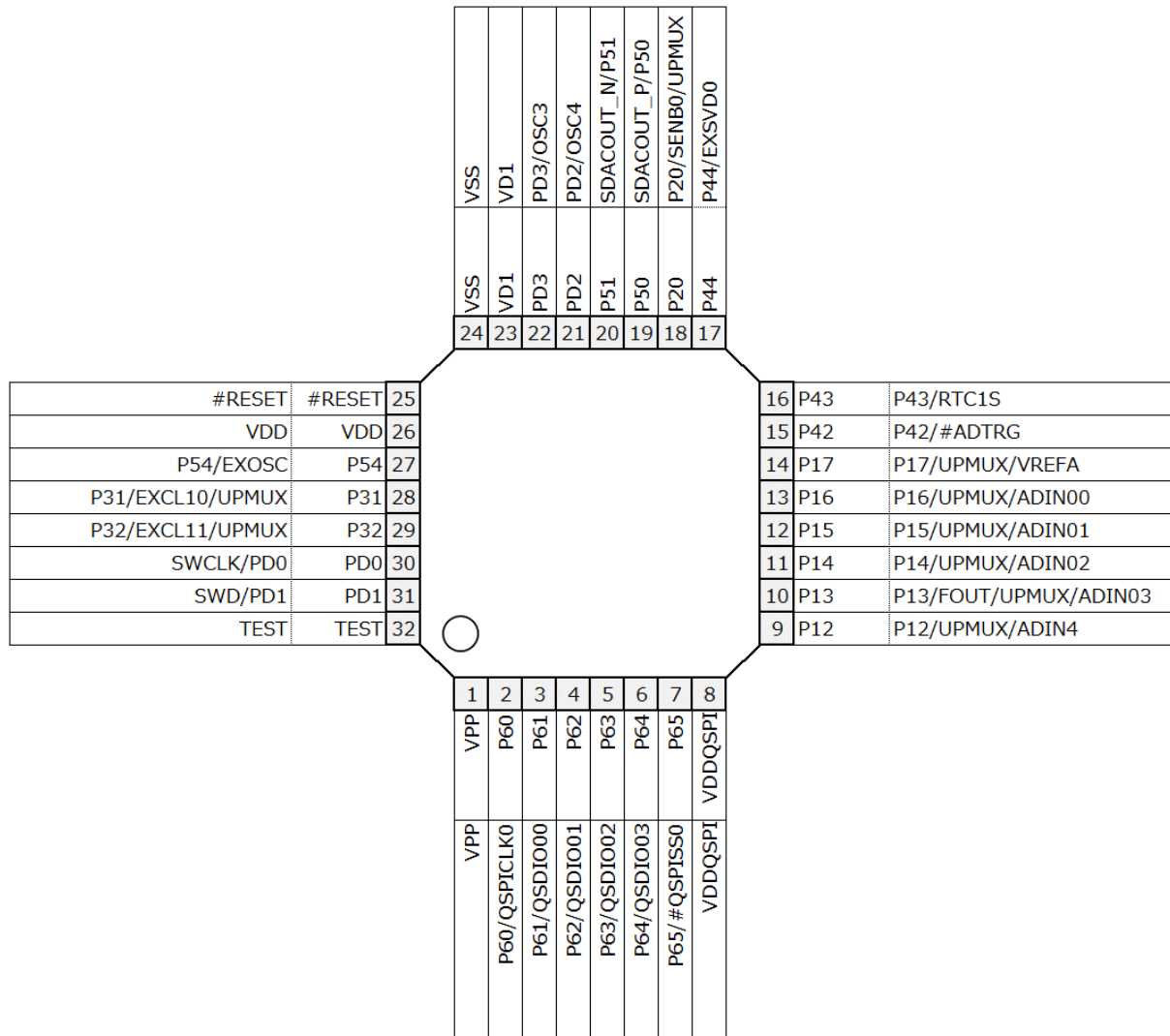
Model	HWP version	Embedded Flash		External SPI-Flash		Embedded RAM	
		CRC	Checksum	CRC	Checksum	March-C	R/W Check
S1C31D50	1.00						
S1C31D51	2.00	✓	✓	✓	✓	✓	✓
S1C31D41	3.00						

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■ Pin Configuration Diagram

P-TQFP032-0707-0.80(32pin, 7mm x 7mm, 0.8mm pitch)

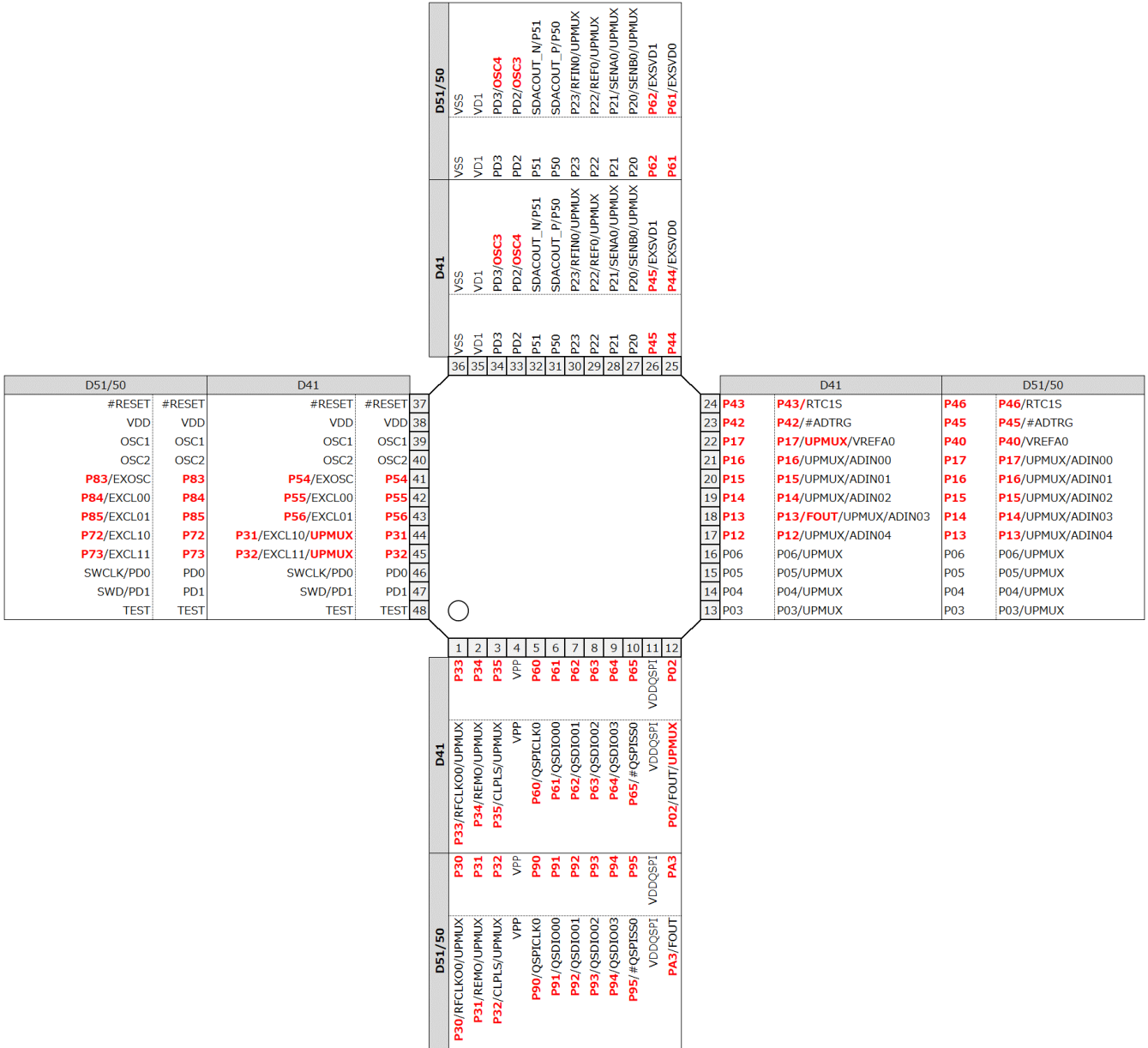
✓ S1C31D41



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P-TQFP048-0707-0.50(48pin, 7mm x 7mm, 0.5mm pitch)

✓ S1C31D51/50/41

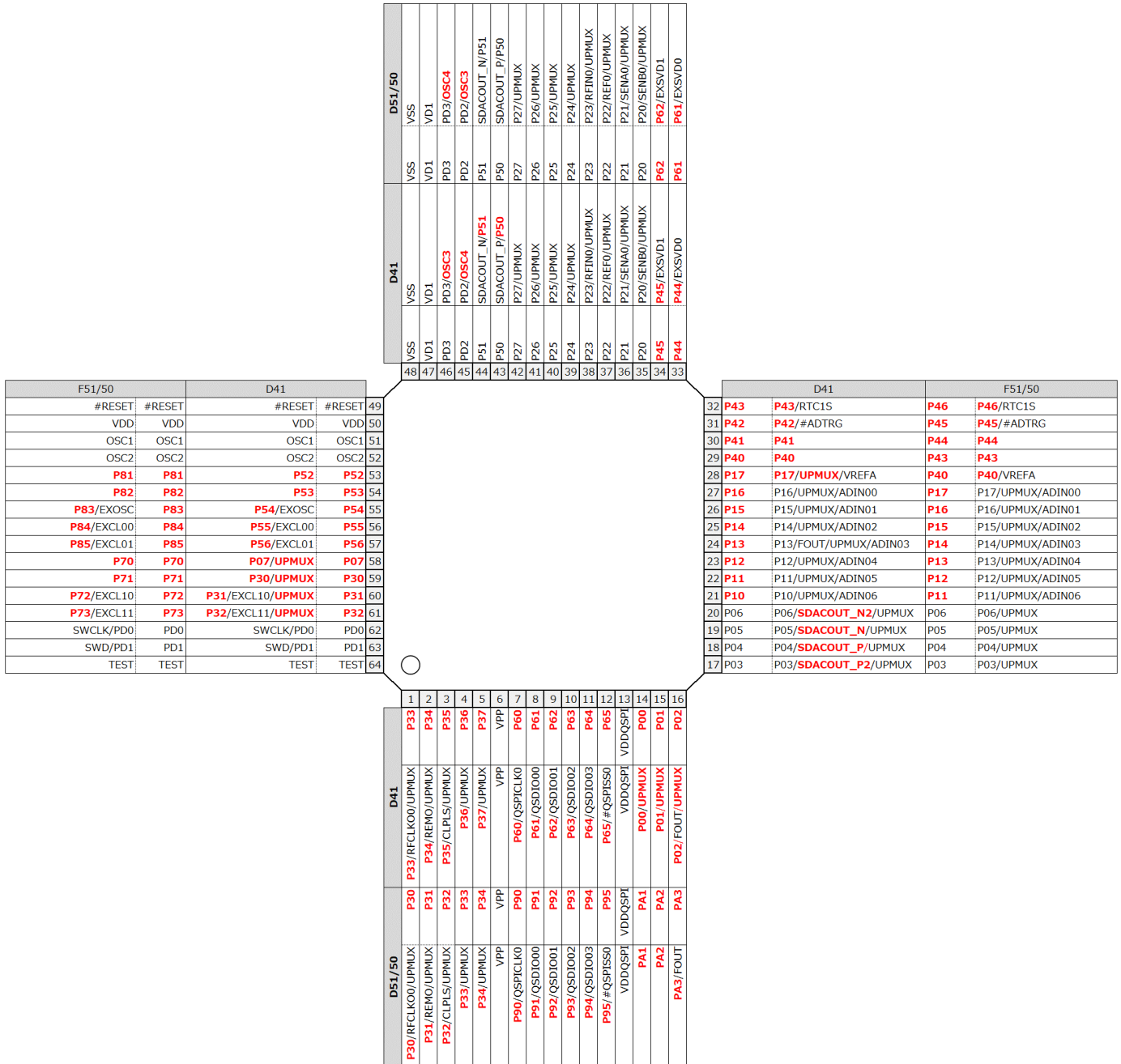


Note) Basically, Pin Compatible for D50/D51/D41 is achievable, if software deal with Port Pins differential.
 Red Pins : differential between D50/D51 and D41.

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P-LQFP064-1010-0.50(64pin, 10mm x 10mm, 0.5mm pitch)

✓ S1C31D51/50/41



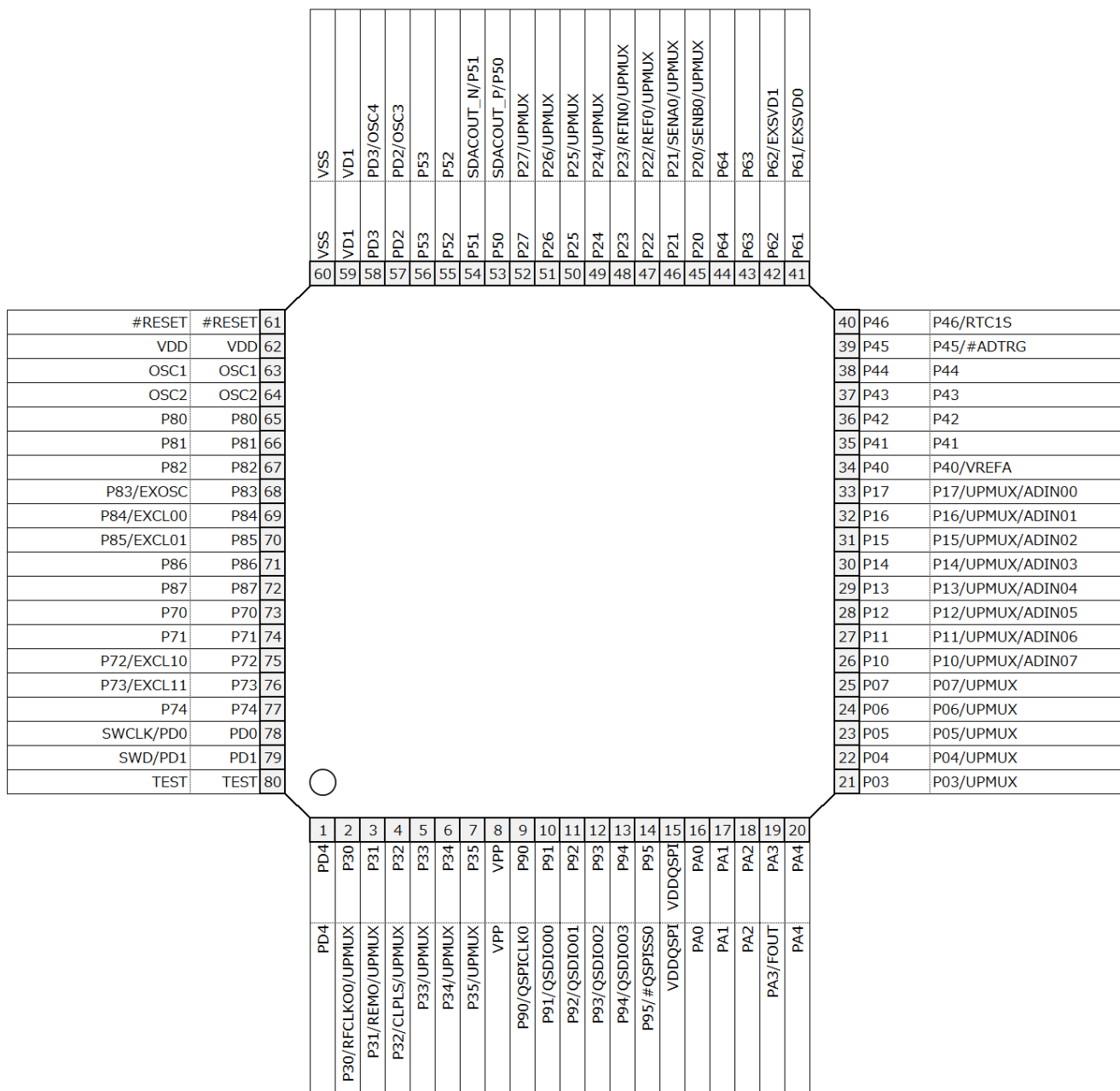
Note) Basically, Pin Compatible for D50/D51/D41 is achievable, if software deal with Port Pins differential.

Red Pins : differential between D50/D51 and D41.

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P-LQFP080-1212-0.50(80pin, 12mm x 12mm, 0.5mm pitch)

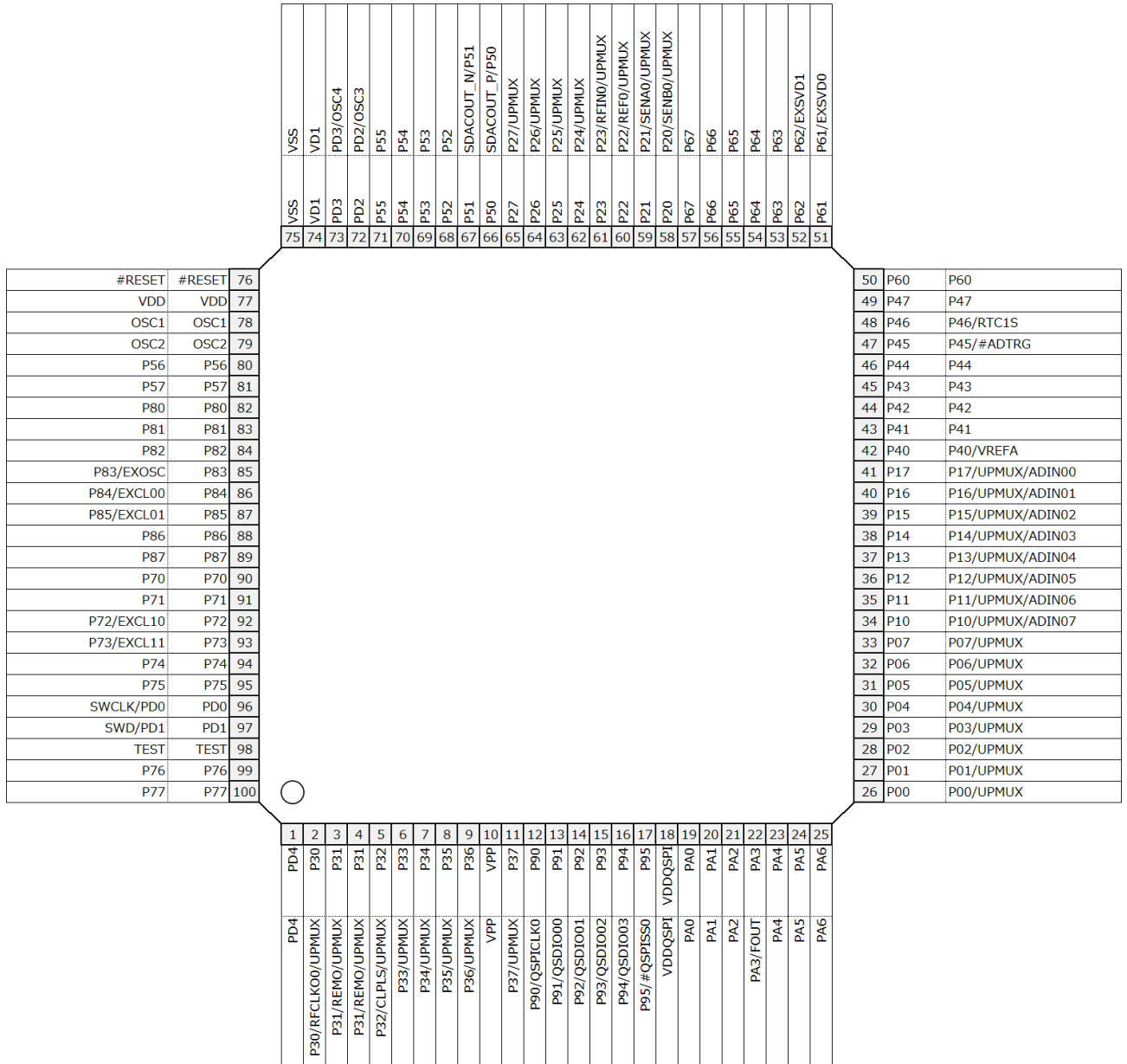
✓ S1C31D51/50



S1C31D50/51/41

P-LQFP100-1414-0.50(100pin, 14mm x 14mm, 0.5mm pitch)

✓ S1C31D51/50



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■ Pin Descriptions

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the “I/O Ports” chapter).

I/O:	I	= Input
	O	= Output
	I/O	= Input/Output
	P	= Power supply
	A	= Analog signal
	Hi-Z	= High impedance state
Initial state:	I (Pull-up)	= Input with pulled up
	I (Pull-down)	= Input with pulled down
	Hi-Z	= High impedance state
	O (H)	= High level output
	O (L)	= Low level output
Tolerant fail-safe structure:	✓	= Over voltage tolerant fail-safe type I/O cell included

Red Pins : differential between D50/D51 and D41.

Pin name	Pin function	I/O	Initial	Tolerant fail-safe structure	Description	D41			D51/50				
						32pin	48pin	64pin	48pin	64pin	80pin	100pin	
VDD	VDD	P	-	-	Power(+)	✓	✓	✓	✓	✓	✓	✓	
VSS	VSS	P	-	-	GND	✓	✓	✓	✓	✓	✓	✓	
VPP	VPP	P	-	-	Flash Programing Power	✓	✓	✓	✓	✓	✓	✓	
VD1	VD1	A	-	-	VD1 Regulator output	✓	✓	✓	✓	✓	✓	✓	
VDDQSPI	VDDQSPI	P	-	-	QSPI Interface/ P9 Port group power Supply(D50/51)/ P6 Port group power Supply (D41)	✓	✓	✓	✓	✓	✓	✓	
OSC1	OSC1	A	-	-	OSC1 oscillator input	-	✓	✓	✓	✓	✓	✓	
OSC2	OSC2	A	-	-	OSC1 oscillator output	-	✓	✓	✓	✓	✓	✓	
TEST	TEST	I	I(Pull-down)	-	Test mode enable	✓	✓	✓	✓	✓	✓	✓	
#RESET	#RESET	I	I(Pull-up)	-	Reset input	✓	✓	✓	✓	✓	✓	✓	
P00	P00	I/O	Hi-Z	✓	I/O port	-	-	✓	-	-	-	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	-	✓	-	-	-	✓	
P01	P01	I/O	Hi-Z	✓	I/O port	-	-	✓	-	-	-	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	-	✓	-	-	-	✓	
P02	P02	I/O	Hi-Z	✓	I/O port	-	✓	✓	-	-	-	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	✓	✓	-	-	-	✓	
P03	P03	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓	✓	✓	✓	
	SDACOUT_P2	D41			O	Buzzer sound DAC positive output 2	-	✓	✓	-	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	✓	✓	✓	✓	✓	✓	
P04	P04	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓	✓	✓	✓	
	SDACOUT_P	D41			O	Buzzer sound DAC positive output 1	-	✓	✓	-	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	✓	✓	✓	✓	✓	✓	
P05	P05	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓	✓	✓	✓	
	SDACOUT_N	D41			O	Buzzer sound DAC negative output 1	-	✓	✓	-	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	✓	✓	✓	✓	✓	✓	
P06	P06	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓	✓	✓	✓	
	SDACOUT_N2	D41			O	Buzzer sound DAC negative output 2	-	✓	✓	-	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	✓	✓	✓	✓	✓	✓	
P07	P07	I/O	Hi-Z	✓	I/O port	-	-	✓	-	-	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	-	✓	-	-	✓	✓	

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Pin name	Pin function	I/O	Initial	Tolerant fail-safe structure	Description	D41			D51/50				
						32pin	48pin	64pin	48pin	64pin	80pin	100pin	
P10	P10	I/O	Hi-Z	-	I/O port	-	-	✓	-	-	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	-	✓	-	-	✓	✓	
	ADIN06	D41			A	12-bit A/D converter Ch.0 analog signal input6	-	-	✓	-	-	-	-
	ADIN07	D50/D51			A	12-bit A/D converter Ch.0 analog signal input7	-	-	-	-	-	✓	✓
P11	P11	I/O	Hi-Z	-	I/O port	-	-	✓	-	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	-	✓	-	✓	✓	✓	
	ADIN05	D41			A	12-bit A/D converter Ch.0 analog signal input5	-	-	✓	-	-	-	-
	ADIN06	D50/D51			A	12-bit A/D converter Ch.0 analog signal input6	-	-	-	-	✓	✓	✓
P12	P12	I/O	Hi-Z	-	I/O port	✓	✓	✓	-	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	✓	✓	✓	-	✓	✓	✓	
	ADIN04	D41			A	12-bit A/D converter Ch.0 analog signal input4	✓	✓	✓	-	-	-	-
	ADIN05	D50/D51			A	12-bit A/D converter Ch.0 analog signal input5	-	-	-	-	✓	✓	✓
P13	P13	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓	✓	✓	✓	
	FOUT	D41			O	Clock external output	✓	✓	✓	-	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	✓	✓	✓	✓	✓	✓	✓	
	ADIN03	D41			A	12-bit A/D converter Ch.0 analog signal input3	✓	✓	✓	-	-	-	-
	ADIN04	D50/D51			A	12-bit A/D converter Ch.0 analog signal input4	-	-	-	✓	✓	✓	✓
P14	P14	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	✓	✓	✓	-	-	-	-	
	ADIN02	D41			A	12-bit A/D converter Ch.0 analog signal input2	✓	✓	✓	-	-	-	-
	ADIN03	D50/D51			A	12-bit A/D converter Ch.0 analog signal input3	-	-	-	✓	✓	✓	✓
P15	P15	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	✓	✓	✓	-	-	-	-	
	ADIN01	D41			A	12-bit A/D converter Ch.0 analog signal input1	✓	✓	✓	-	-	-	-
	ADIN02	D50/D51			A	12-bit A/D converter Ch.0 analog signal input2	-	-	-	✓	✓	✓	✓
P16	P16	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	✓	✓	✓	-	-	-	-	
	ADIN00	D41			A	12-bit A/D converter Ch.0 analog signal input0	✓	✓	✓	-	-	-	-
	ADIN01	D50/D51			A	12-bit A/D converter Ch.0 analog signal input1	-	-	-	✓	✓	✓	✓
P17	P17	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	✓	✓	✓	-	-	-	-	
	VREFA0	D41			A	12-bit A/D converter Ch.0 reference voltage input	✓	✓	✓	-	-	-	-
	ADIN00	D50/D51			A	12-bit A/D converter Ch.0 analog signal input0	-	-	-	✓	✓	✓	✓

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Pin name	Pin function	I/O	Initial	Tolerant fail-safe structure	Description	D41			D51/50				
						32pin	48pin	64pin	48pin	64pin	80pin	100pin	
P20	P20	I/O	Hi-Z	✓	I/O port								
	SENB0	A			R/F converter Ch.0 sensor B oscillator pin	✓	✓	✓	✓	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)								
P21	P21	I/O	Hi-Z	✓	I/O port								
	SENA0	A			R/F converter Ch.0 sensor A oscillator pin	-	✓	✓	✓	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)								
P22	P22	I/O	Hi-Z	✓	I/O port								
	REF0	A			R/F converter Ch.0 reference oscillator pin	-	✓	✓	✓	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)								
P23	P23	I/O	Hi-Z	✓	I/O port								
	RFIN0	A			R/F converter Ch.0 oscillation input	-	✓	✓	✓	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)								
P24	P24	I/O	Hi-Z	✓	I/O port	-	-	✓	-	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)								
P25	P25	I/O	Hi-Z	✓	I/O port	-	-	✓	-	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)								
P26	P26	I/O	Hi-Z	✓	I/O port	-	-	✓	-	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)								
P27	P27	I/O	Hi-Z	✓	I/O port	-	-	✓	-	✓	✓	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)								
P30	P30	I/O	Hi-Z	✓	I/O port	-	-	✓					
	RFCLK00	D50/D51			O	R/F converter Ch.0 clock monitor output	-	-	-	✓	✓	✓	✓
	UPMUX				I/O	User-selected I/O(universal port multiplexer)	-	-	✓				
P31	P31	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓	✓	✓	✓	
	EXCL10	D41			I	16-bit PWM timer Ch.1 event counter input 0	✓	✓	✓	-	-	-	-
	REMO	D50/D51			O	IR remote controller transmit data output	-	-	-	✓	✓	✓	✓
	UPMUX				I/O	User-selected I/O(universal port multiplexer)	✓	✓	✓	✓	✓	✓	✓
P32	P32	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓	✓	✓	✓	
	EXCL11	D41			I	16-bit PWM timer Ch.1 event counter input 1	✓	✓	✓	-	-	-	-
	CLPLS	D50/D51			O	IR remote controller clear pulse output	-	-	-	✓	✓	✓	✓
	UPMUX				I/O	User-selected I/O(universal port multiplexer)	✓	✓	✓	✓	✓	✓	✓
P33	P33	I/O	Hi-Z	✓	I/O port				-	✓	✓	✓	
	RFCLK00	D41			O	R/F converter Ch.0 clock monitor output	-	✓	✓	-	-	-	-
	UPMUX				I/O	User-selected I/O(universal port multiplexer)				-	✓	✓	✓
P34	P34	I/O	Hi-Z	✓	I/O port				-	✓	✓	✓	
	REMO	D41			O	IR remote controller transmit data output	-	✓	✓	-	-	-	-
	UPMUX				I/O	User-selected I/O(universal port multiplexer)				-	✓	✓	✓
P35	P35	I/O	Hi-Z	✓	I/O port				-	-	✓	✓	
	CLPLS	D41			O	IR remote controller clear pulse output	-	✓	✓	-	-	-	-
	UPMUX				I/O	User-selected I/O(universal port multiplexer)				-	-	✓	✓
P36	P36	I/O	Hi-Z	✓	I/O port	-	-	✓	-	-	-	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)								
P37	P37	I/O	Hi-Z	✓	I/O port	-	-	✓	-	-	-	✓	
	UPMUX	I/O			User-selected I/O(universal port multiplexer)								

S1C31D50/51/41

Pin name	Pin function		I/O	Initial	Tolerant fail-safe structure	Description	D41			D51/50			
							32pin	48pin	64pin	48pin	64pin	80pin	100pin
P40	P40		I/O	Hi-Z	-	I/O port	-	-	✓				
	VREFA	D50/D51	A			12-bit A/D converter Ch.0 reference voltage input	-	-	-	✓	✓	✓	✓
P41	P41		I/O	Hi-Z	✓	I/O port	-	-	✓	-	-	✓	✓
P42	P42		I/O	Hi-Z	✓*1	I/O port	✓	✓	✓	-	-	✓	✓
	#ADTRG0	D41	I			12-bit A/D converter Ch.0 trigger input	-	-	-	-	-	-	
P43	P43		I/O	Hi-Z	✓*1	I/O port	✓	✓	✓	-	✓	✓	✓
	RTC1S	D41	O			Real-time clock 1-second cycle pulse output	-	-	-	-	-		
P44	P44		I/O	Hi-Z	✓	I/O port	✓	✓	✓	-	✓	✓	✓
	EXSVD0	D41	A			Supply voltage detector external voltage detection input 0	-	-	-	-	-		
P45	P45		I/O	Hi-Z	✓	I/O port	-	✓	✓				
	EXSVD1	D41	A			Supply voltage detector external voltage detection input 1	✓	✓	✓	✓	✓	✓	
	#ADTRG0	D50/D51	I			12-bit A/D converter Ch.0 trigger input	-	-	-	-	-		
P46	P46		I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	RTC1S	D50/D51	O			Real-time clock 1-second cycle pulse output	-	-	-	-	-		
P47	P47		I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	
P50	SDACOUT_P		O	O(L)	✓	Sound DAC positive output	✓	✓	✓	✓	✓	✓	✓
	P50		I/O			I/O port							
P51	SDACOUT_N		O	O(L)	✓	Sound DAC negative output	✓	✓	✓	✓	✓	✓	✓
	P51		I/O			I/O port							
P52	P52		I/O	Hi-Z	✓	I/O port	-	-	✓	-	-	✓	✓
P53	P53		I/O	Hi-Z	✓	I/O port	-	-	✓	-	-	✓	✓
P54	P54		I/O	Hi-Z	✓	I/O port	✓	✓	✓	-	-	-	✓
	EXOSC	D41	I			Clock generator external clock input	-	-	-	-	-		
P55	P55		I/O	Hi-Z	✓	I/O port	-	✓	✓	-	-	-	✓
	EXCL00	D41	I			16-bit PWM timer Ch.0 event counter input 0	-	-	-	-	-		
P56	P56		I/O	Hi-Z	✓	I/O port	-	✓	✓	-	-	-	✓
	EXCL01	D41	I			16-bit PWM timer Ch.0 event counter input 1	-	-	-	-	-		
P57	P57		I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	
P60	P60		I/O	Hi-Z	✓	I/O port	✓	✓	✓	-	-	-	✓
	QSPICLK0	D41	I/O			Quad synchronous serial interface Ch.0 clock input/output	-	-	-	-	-		
P61	P61		I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓	✓	✓	✓
	QSDIO00	D41	I/O			Quad synchronous serial interface Ch.0 data input/output	-	-	-	-	-		
	EXSVD0	D50/D51	A			Supply voltage detector external voltage detection input 0	-	-	-	✓	✓	✓	✓
P62	P62		I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓	✓	✓	✓
	QSDIO01	D41	I/O			Quad synchronous serial interface Ch.0 data input/output	-	-	-	-	-		
	EXSVD1	D50/D51	A			Supply voltage detector external voltage detection input 1	-	-	-	✓	✓	✓	✓
P63	P63		I/O	Hi-Z	✓	I/O port	✓	✓	✓	-	-	✓	✓
	QSDIO02	D41	I/O			Quad synchronous serial interface Ch.0 data input/output	-	-	-	-	-		
P64	P64		I/O	Hi-Z	✓	I/O port	✓	✓	✓	-	-	✓	✓
	QSDIO03	D41	I/O			Quad synchronous serial interface Ch.0 data input/output	-	-	-	-	-		
P65	P65		I/O	Hi-Z	✓	I/O port	✓	✓	✓	-	-	-	✓
	#QSDISS0	D41	I/O			Quad synchronous serial interface Ch.0 slave-select input/output	-	-	-	-	-		
P66	P66		I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	
P67	P67		I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	

* 1 : D41 unsupported

S1C31D50/51/41

Pin name	Pin function	I/O	Initial	Tolerant fail-safe structure	Description	D41			D51/50				
						32pin	48pin	64pin	48pin	64pin	80pin	100pin	
P70	P70	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	✓	✓	✓
P71	P71	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	✓	✓	✓
P72	P72	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	EXCL10		I			16-bit PWM timer Ch.1 event counter input 0							
P73	P73	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	EXCL11		I			16-bit PWM timer Ch.1 event counter input 1							
P74	P74	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	✓	✓	✓
P75	P75	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	✓
P76	P76	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	✓
P77	P77	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	✓
P80	P80	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	✓
P81	P81	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	✓	✓	✓
P82	P82	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	✓	✓	✓
P83	P83	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	EXOSC		I			Clock generator external clock input							
P84	P84	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	EXCL00		I			16-bit PWM timer Ch.0 event counter input 0							
P85	P85	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	EXCL01		I			16-bit PWM timer Ch.0 event counter input 1							
P86	P86	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	✓	✓	✓
P87	P87	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	-	✓	✓	✓
P90	P90	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	QSPICLK0		I/O			Quad synchronous serial interface Ch.0 clock input/output							
P91	P91	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	QSDIO00		I/O			Quad synchronous serial interface Ch.0 data input/output							
P92	P92	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	QSDIO01		I/O			Quad synchronous serial interface Ch.0 data input/output							
P93	P93	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	QSDIO02		I/O			Quad synchronous serial interface Ch.0 data input/output							
P94	P94	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	QSDIO03		I/O			Quad synchronous serial interface Ch.0 data input/output							
P95	P95	<u>D50/D51</u>	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓
	#QSPISS0		I/O			Quad synchronous serial interface Ch.0 slave-select input/output							

S1C31D50/51/41

Pin name	Pin function		I/O	Initial	Tolerant fail-safe structure	Description	D41			D51/50										
							32pin	48pin	64pin	48pin	64pin	80pin	100pin							
PA0	PA0	D50/D51	I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	✓							
PA1	PA1	D50/D51	I/O	Hi-Z	✓	I/O port	-	-	-	-	✓	✓	✓							
PA2	PA2	D50/D51	I/O	Hi-Z	✓	I/O port	-	-	-	-	✓	✓	✓							
PA3	PA3	D50/D51	I/O	Hi-Z	✓	I/O port	-	-	-	✓	✓	✓	✓							
	FOUT		O			Clock external output														
PA4	PA4	D50/D51	I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	✓							
PA5	PA5	D50/D51	I/O	Hi-Z	✓	I/O port	-	-	-	-	-	-	✓							
PA6	PA6	D50/D51	I/O	Hi-Z	✓	I/O port	-	-	-	-	-	-	✓							
PD0	SWCLK		I	I (Pull-up)	✓	Serial-wire debugger clock input	✓	✓	✓	✓	✓	✓	✓							
	PD0		I/O			I/O port														
PD1	SWD		I/O	I (Pull-up)	✓	Serial-wire debugger data input/output	✓	✓	✓	✓	✓	✓	✓							
	PD1		I/O			I/O port														
PD2	PD2		I/O	Hi-Z	-	I/O port	✓	✓	✓	✓	✓	✓	✓							
	OSC4	D41	A			OSC4 oscillator circuit output								✓	✓	✓	-	-	-	-
	OSC3	D50/D51	A			OSC3 oscillator circuit input								-	-	-	✓	✓	✓	✓
PD3	PD3		I/O	Hi-Z	-	I/O port	✓	✓	✓	✓	✓	✓	✓							
	OSC3	D41	A			OSC3 oscillator circuit input								✓	✓	✓	-	-	-	-
	OSC4	D50/D51	A			OSC4 oscillator circuit output								-	-	-	✓	✓	✓	✓
PD4	PD4	D50/D51	I/O	Hi-Z	✓	I/O port	-	-	-	-	-	✓	✓							
PD5	PD5	D50/D51	I/O	Hi-Z	✓	I/O port	-	-	-	-	-	-	✓							

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

Peripheral circuit	Signal to be assigned	I/O	Channel number n	Function
I ² C (I2C)	SCLn	I/O	n=0~2	I2C Ch.n clock input/output
	SDAn	I/O		I2C Ch.n data input/output
UART (UART3)	USINn	I	n=0~2	UART3 Ch.n data input
	USOUTn	O		UART3 Ch.n data output
Synchronous serial interface (SPIA)	SDIn	I	n=0~2	SPIA Ch.n data input
	SDOn	O		SPIA Ch.n data output
	SPICLKn	I/O		SPIA Ch.n clock input/output
	#SPISSn	I		SPIA Ch.n slave-select input
16-bit PWM timer (T16B)	TOUTn0/CAPn0	I/O	n=0,1	T16B Ch.n PWM output/capture input 0
	TOUTn1/CAPn1	I/O		T16B Ch.n PWM output/capture input 1
	TOUTn2/CAPn2	I/O		T16B Ch.n PWM output/capture input 2
	TOUTn3/CAPn3	I/O		T16B Ch.n PWM output/capture input 3

Note) Do not assign a function to two or more pins simultaneously.

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■ EPSON Voice Creation PC Tool

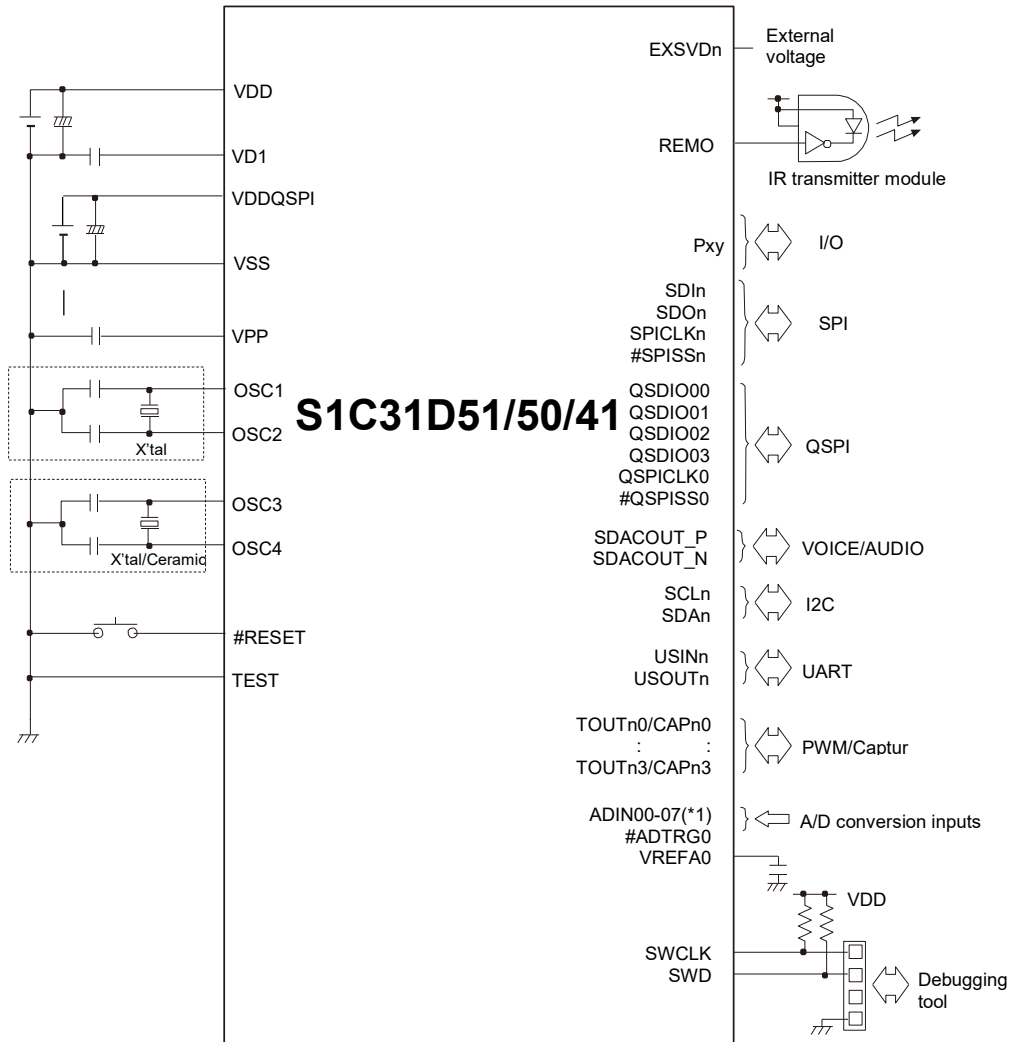
EPSON Voice creation PC tool makes voice related development easy because of no-studio recording, no narrator arrangement. This tool supports languages in the table below (all female voice), and easily creation, modification can be done, by "wav file" import function, existing wav file can be used.

Asia	America	Europe
Chinese	American English	British English
Korean	American Spanish	German
Japanese	Canadian French	French
—	—	Spanish
—	—	Italian
—	—	Russian



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■ Basic External Connection Diagram



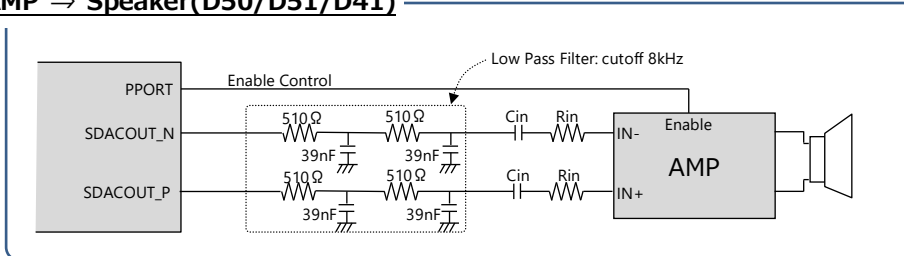
*1) S1C31D41 ADIN07 is connected internal TSRVR signal.

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■ Basic Speaker/Buzzer External Connection Diagram

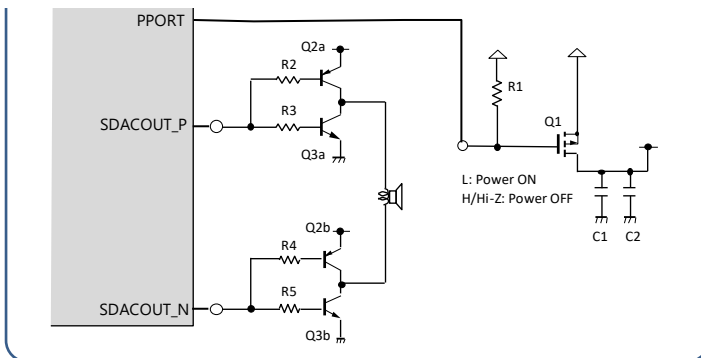
Please see the circuit in D50/D51/D41 Evaluation Board manual to the details.

1. AMP ⇒ Speaker(D50/D51/D41)



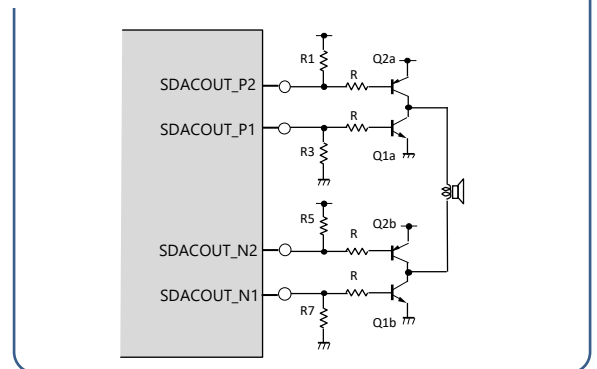
2.1. differential circuit ⇒

Speaker/Electromagnetic Buzzer(D51/D41)



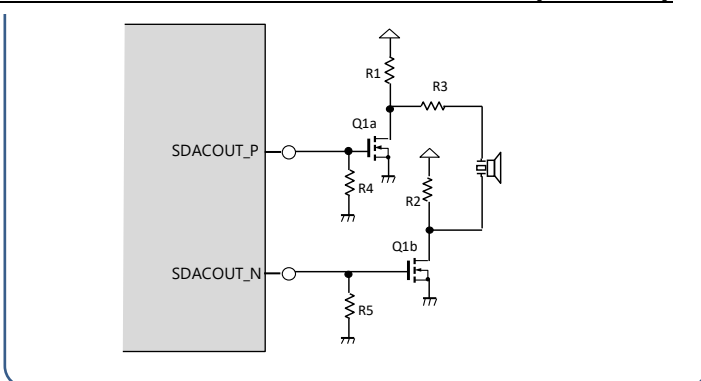
2.2. differential circuit ⇒

Speaker/Electromagnetic Buzzer(D41)



note) Resistance value depends on the power supply for the buzzer, please check each evaluation manual.

3. differential circuit ⇒ Piezoelectric buzzer (D51/D41)



note) Resistance value depends on the power supply for the buzzer, please check each evaluation manual.

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■ Revision History

Contents				
Date	Rev.	Page	Type	Details
2018/7/30	1.00	All	New	New release
2020/6/30	2.00	All	Changed	Added S1C31D51
2020/12/15	2.01	All	Changed	Deleted "FEAUTURES" – Embedded RAMS – Instruction cache Modified "Basic External Connection Diagram"
2021/2/15	2.02	p.13	Changed	Corrected "Basic External Connection Diagram"
2022/6/2	3.00	All	Changed	Added S1C31D41
2023/8/1	3.01	p.3,8	Changed	Changed "P-TQFP080" to "P-LQFP080"

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