

S2R72A21

Data Sheet

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1. Description

S2R72A21 is the Re-Synchronization IC which re-synchronizes the HS packet of USB 2.0 (Universal Serial Bus Specification Revision 2.0).

S2R72A21 monitors the Bus condition on the basis of USB 2.0 standards once this device is inserted in between the Bus of USB port of the SoC and the USB Type-A receptacle. It automatically switches the Bus path to HS Synchronizer during HS connection and to Bus Switch during non-HS connection. Unlike the Hub, there is no directional limitation such as Upstream / Downstream, so the S2R72A21 can maintain the Bus path when the Host is connected to either port.

The HS Synchronizer would surely receive the HS packet from one port, re-synchronize using its own clock, and transmit to the other port. Herewith, the S2R72A21 would reduce the jitters of the HS signal waveform along with controlling its aperture. This realizes a stable longer connection using various USB applications, such as car navigation / car display audio to the smart phone / portable audio player.

S2R72A21 is complying with the automotive level grade quality and support the max temperature range up to 105°C.

2. Features

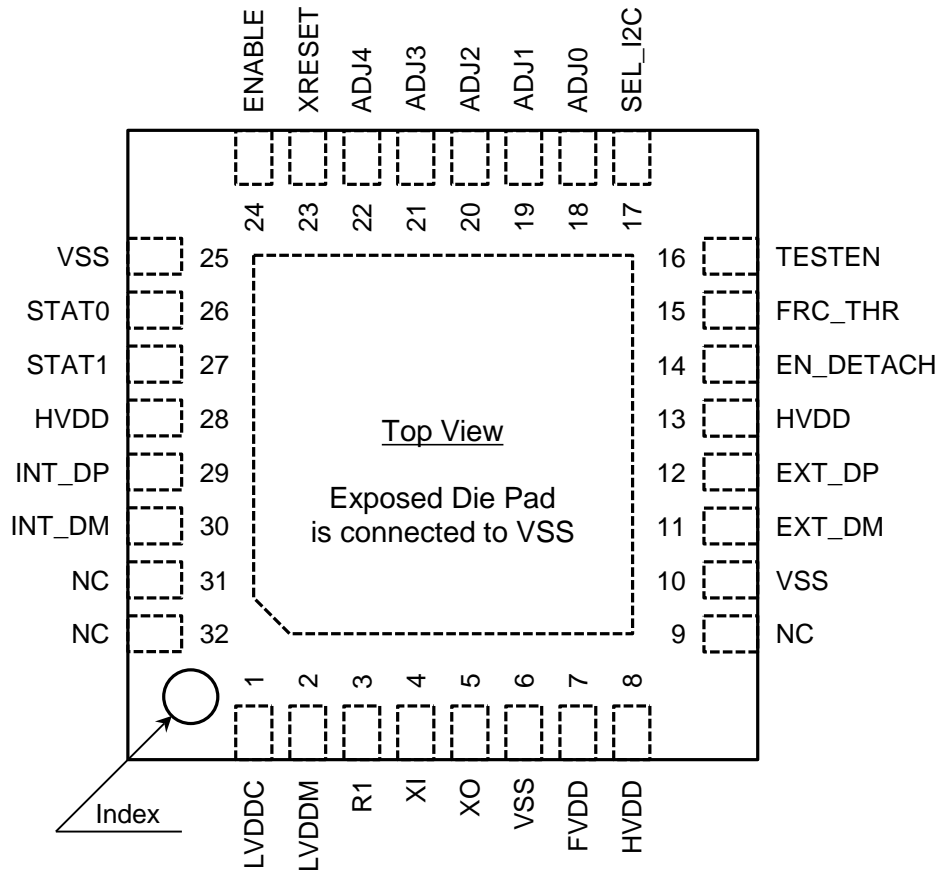
- AEC-Q100 certified
- Excellent data communication characteristics (HS 480Mbps)
 - HS transmission: Transmission waveform with low jitter
 - Support HS transmission current control
 - HS reception: High reception tolerance
- Automatic USB line monitor and control function
 - HS communication: Re-synchronize with HS Synchronizer
 - Except for HS communication: Passes through with analog switch
- Wide temperature range
 - Operating temperature range is -40°C to +105°C
- Other features
 - Supports 24MHz crystal oscillator (with built-in oscillator circuit and feedback resistor)
 - Power supply voltage: 3.3V
 - Built-in Regulator to generate voltage (1.8V) for the internal core and PLL/OSC
 - Built-in Charge Pump for Analog Switch

Table 2.1 Product list

Model number	Package	Packing
S2R72A21F05E600	SQFN5-32PIN-W*	Tray
S2R72A21F05E60B		Tape & reel

*: SQFN5-32PIN-W (Wettable Flank, 32pin, 5mm square, 0.5mm pitch)

3. Pin Layout



Note: Please connect the Exposed Die pad to the VSS.

Figure 3.1 Pin Layout

4. Pin Assignment

4.1 Reset Pin (HVDD level I/O)

Pin	Description	I/O	Pin Assignment
23	XRESET	IN	Reset Signal Pin 0: Reset 1: Reset release

4.2 Control Pin (HVDD level I/O)

Pin	Description	I/O	Pin Assignment	
24	ENABLE	IN	Bus connection condition notification pin. 0: Disconnect 1: Connect During ENABLE=0: Bus Monitor is reset, and the connection between INT_DP/DM - EXT_DP/DM would be connected by Bus Switch. During ENABLE=1: Bus Monitor becomes valid / Then it would monitor the condition of the Bus and automatically do the path switching of Bus Switch / HS Synchronizer.	
14	EN_DETACH	IN	DETACH State valid pin. 0: DETACH State invalid 1: DETACH state valid Please stable it either with "0" or "1" on the board.	
15	FRC_THR	IN	Force through setting pin. 0: Normal 1: Force through Case FRC_THR=1: The Bus Switch would forcibly connect between the INT-EXT. Please stable it either with "0" or "1" on the board.	
17	SEL_I2C	IN	I2C validation setting pin. 0: I2C Invalid 1: I2C Valid This pin setting would have an influence of the setting method (Transmission waveform shaping function) as following Case SEL_I2C=0: Set up via ADJ0-4 pins Case SEL_I2C=1: Set up via I2C register Please stable it either with "0" or "1" on the board.	
22	ADJ4	IN/OUT	Case SEL_I2C=0 : <u>RSV1</u> Reserved pin 1. Please stable "0" on the board.	Case SEL_I2C=1: <u>I2C_SDA</u> Data pin of I2C (bidirectional). Please connect the pull up resistor between HVDD.
21	ADJ3	IN	Case SEL_I2C=0 : <u>RSV0</u> Reserved pin 0. Please stable "0" on the board.	Case SEL_I2C=1: <u>I2C_SCL</u> CLK pin of I2C. Please connect the pull up resistor between HVDD.
20	ADJ2	IN	Case SEL_I2C=0: <u>EXT_CUR[3]</u> Third bit (MSB) HS transmit current setting pin for EXT port. Please stable either "0" or "1" on the board.	Case SEL_I2C=1: <u>I2C_OADR[2]</u> The second bit (MSB) I2C slave address setting pin. Please stable either "0" or "1" on the board.
19	ADJ1	IN	Case SEL_I2C=0: <u>EXT_CUR[2]</u> Second bit HS transmit current setting pin for EXT port. Please stable either "0" or "1" on the board.	Case SEL_I2C=1: <u>I2C_OADR[1]</u> The first bit I2C slave address setting pin. Please stable either "0" or "1" on the board.
18	ADJ0	IN	Case SEL_I2C=0: <u>EXT_CUR[1]</u> First bit HS transmit current setting pin for EXT port. Please stable either "0" or "1" on the board.	Case SEL_I2C=1: <u>I2C_OADR[0]</u> Zero bit (LSB) I2C slave address setting pin. Please stable either "0" or "1" on the board.
27	STAT1	OUT	The first bit Status signal output pin. Output of this pin is open drain during default. Initial condition is HiZ.	

			It is feasible to select the output signal via I2C registers.
26	STAT0	OUT	Zero bit Status signal output pin. Output of this pin is open drain during default. Initial condition is HiZ. It is feasible to select the output signal via I2C registers.

4.3 USB Pin

Pin	Description	I/O	Pin Assignment
29	INT_DP	IN/OUT	Internal Side : USB Data line (INT Port) Data + Connection pin
30	INT_DM	IN/OUT	Internal Side : USB Data line (INT Port) Data – Connection pin
12	EXT_DP	IN/OUT	External Side : USB Data line (EXT Port) Data + Connection pin
11	EXT_DM	IN/OUT	External Side : USB Data line (EXT Port) Data – Connection pin

4.4 Reference pin

Pin	Description	I/O	Pin Assignment
4	XI	IN	Internal OSC input pin (24MHz)
5	XO	OUT	Internal OSC output pin (24MHz)
3	R1	IN	The reference voltage setting terminal Please connect 6.04kΩ ± 1% in between VSS.

4.5 Power Pin

4.5.1 External Power pin

Pin	Description	Voltage	Pin Assignment
8, 13, 28	HVDD	3.3V	External power connection pin of S2R72A21 Please connect all pins on the board with external power.
6, 10, 25, EP	VSS	0V	GND Pin EP stands for Exposed Die Pad. Please connect the Exposed Die pad to the VSS.

4.5.2 Internal Power pin

Pin	Description	Voltage	Pin Assignment
7	FVDD	2.2V	Intermediate power Please connect 10uF + 0.1uF in between VSS.
1	LVDDC	1.8V	Internal Core 1.8V power Please connect 10uF + 0.1uF in between VSS.
2	LVDDM	1.8V	USB 1.8V power Please connect 10uF + 0.1uF in between VSS.

4.6 Test Pin

Pin	Description	I/O	Pin Assignment
16	TESTEN	IN	Test pin Please connect to VSS on the board.

4.7 NC pin

Pin	Description	I/O	Pin Assignment
9,31, 32	NC	-	Not Used Please keep this OPEN on the board.

5. Block diagram

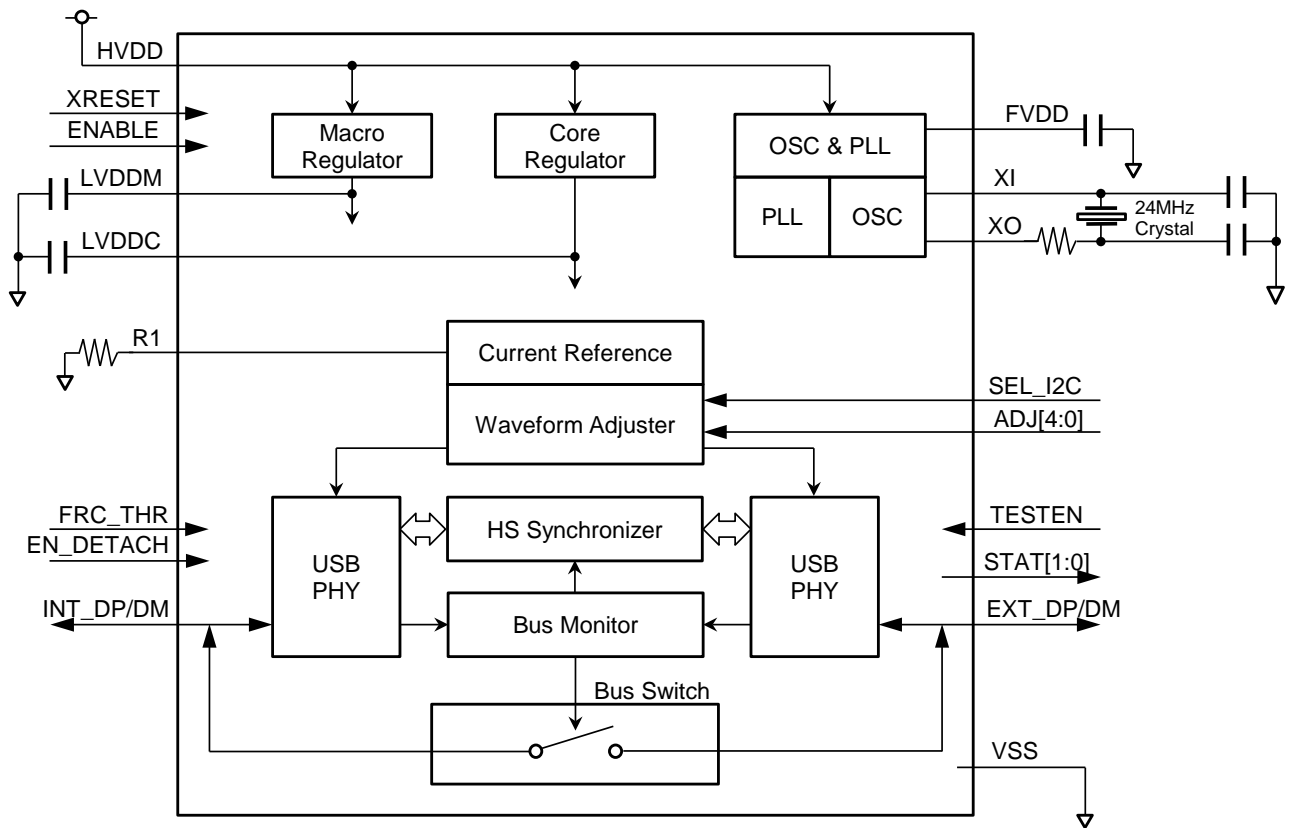


Figure 5.1 Block diagram

6. Feature Description

6.1 Operation

The S2R72A21 has 2 USB signal paths which are “Bus Switch” and “HS Synchronizer”.

The Bus Switch connects INT_DP/DM and EXT_DP/DM electrically. The LS/FS or BC signal would pass as it is.

The HS Synchronizer re-synchronizes the HS signal which has been received via either by INT_DP/DM or EXT_DP/DM. And it transmits to the other ports.

The switch of these 2 paths would be done automatically by the built-in Bus Monitor.

6.1.1 State transition

Please refer to figure 6.1.1.1 for the state transition diagram.

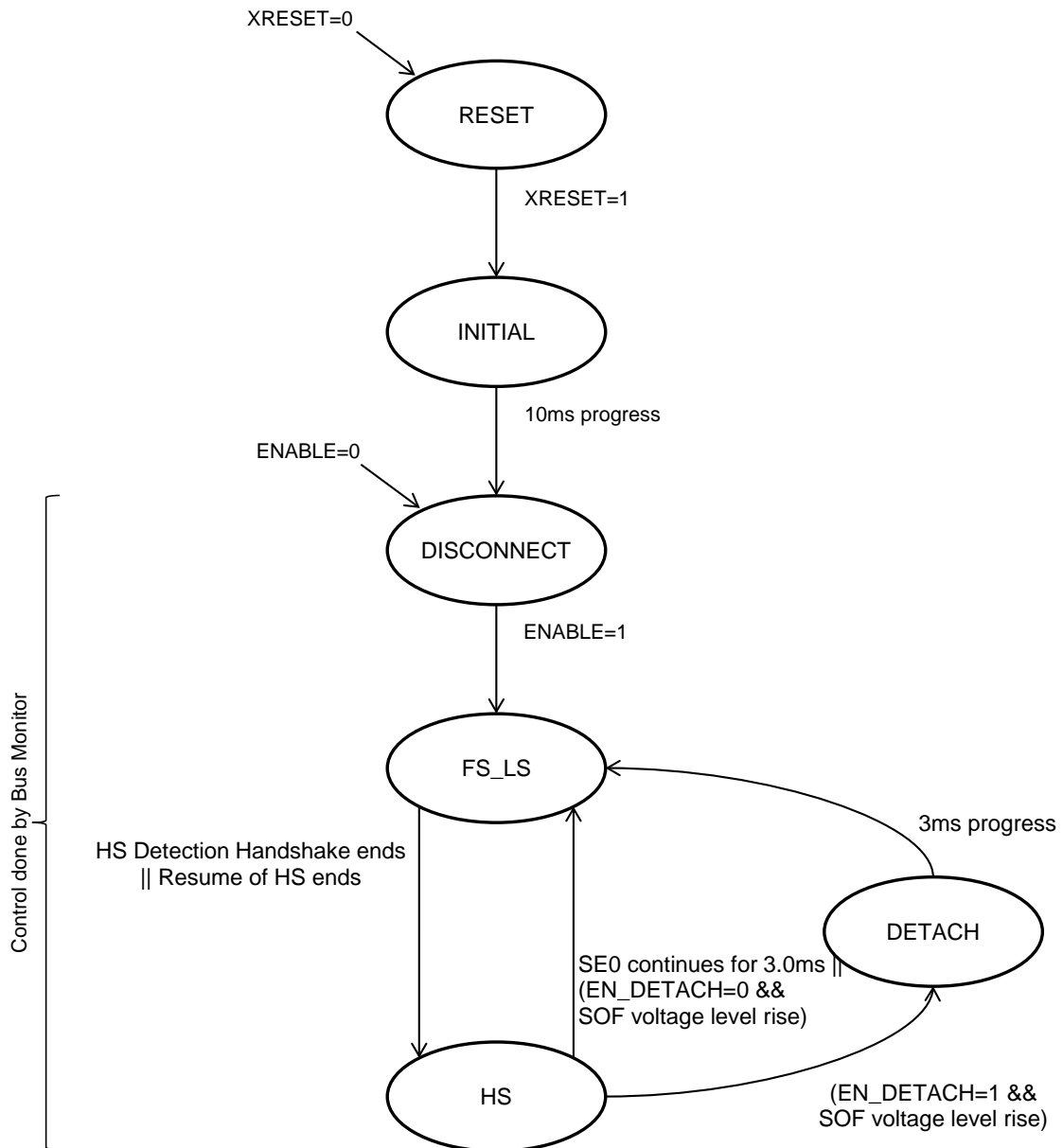


Figure 6.1.1.1 S2R72A21 state transition diagram

6.1.2 Each state and circuit operation

Table 6.1.2.1 indicates the condition of the circuit operation (each state) in case FRC_THR=0. Any pass of HS signal besides the HS state is not guaranteed.

Table 6.1.2.1 Circuit operation in each state (Case FRC_THR=0)

State	Bus Switch	HS Synchronizer	Regulator	OSC / PLL
RESET	OFF	Stopped	Activated	Stopped
INITIAL	ON ^{Note}	Stopped	Activated	Activated
DISCONNECT	ON	Stopped	Activated	Activated
FS_LS	ON	Stopped	Activated	Activated
HS	OFF	Activated	Activated	Activated
DETACH	OFF	Stopped	Activated	Activated

Note: During INITIAL state, the Bus Switch would be "ON" but it would only pass by the BC related signals.

Furthermore, in case FRC_THR=1, the HS synchronizer would be invalid and the Bus Switch would connect INT - EXT port. HS Signal Pass is not guaranteed here.

Table 6.1.2.2 Circuit operation in each state (Case FRC_THR=1)

State	Bus Switch	HS Synchronizer	Regulator	OSC / PLL
RESET	OFF	Stopped	Activated	Stopped
INITIAL	ON ^{Note}	Stopped	Activated	Activated
Other	ON	Stopped	Activated	Activated

Note: During INITIAL state, the Bus Switch would be ON and it would only pass by the BC related signals.

6.1.2.1 RESET State

The RESET state is a RESET condition (XRESET=0) of S2R72A21. The Bus Switch is off and it is under the condition where the Regulator is only active.

The transition to the INITIAL state would occur when XRESET is set up to "1".

6.1.2.2 INITIAL State

The INITIAL state means initial condition (after Reset condition) of S2R72A21. The Bus Switch is not fully operating but in between INT port – EXT port are connected and the BC signal passes through.

From this state, when it pass through 10ms, it would make a transition to DISCONNECT state.

6.1.2.3 DISCONNECT State

DISCONNECT state means the condition when the USB connection via the S2R72A21 is disconnected. In between INT port - EXT port would be connected by the Bus Switch.

From this state, if the ENABLE =1 is detected, the transition to the FS_LS state would be done.

6.1.2.4 FS_LS State

FS_LS state is a condition where the Host and Device connected to INT port and EXT port for each are connected in FS or LS. Bus Switch would connect INT – EXT port.

From this state, the transition to the HS state would be done when the HS detection handshake ends or the HS Resume ends. The transition to the DISCONNECT state would be done when the ENABLE pin is set up to "0".

6.1.2.5 HS State

HS state is a condition where the Host and Device connected to INT port and EXT port for each are connected in HS. The HS packet which is received from either port would be re-synchronized and sent out to the other port by the HS Synchronizer.

In case of EN_DETACH=0, the transition to FS_LS state would be done when the detection of either SOF voltage level rise (HS Device detach) or SE0 over 3ms continuously (HS Reset/Suspend).

In case of EN_DETACH=1, the transition to DETACH state would be done when the detection of SOF voltage level rise (HS Device detach). And the transition to FS_LS state would be done when the detection of SE0 over 3ms continuously (HS Reset/Suspend).

The detach detection should be evaluated on the actual board since it is dependent on the system (detection circuit of the Host, the cable length, etc.).

6.1.2.6 DETACH state

DETACH State is a condition where the S2R72A21 has detected the HS Device detach. In case of EN_DETACH=1, transition to this state is done. When the HS Device detach is detected, the HS Synchronizer of S2R72A21 would be stopped and the Bus Switch is controlled to be OFF. Due to this, Host can detect the Detach more easily when the cable which is connected to the INT port side and EXT port side is longer in total.

Within this condition, after 3ms passes, it would transit to the FS_LS state.

The detach detection should be evaluated on the actual board since it is dependent on the system (detection circuit of the Host, the cable length, etc.).

6.1.3 Flow of operation

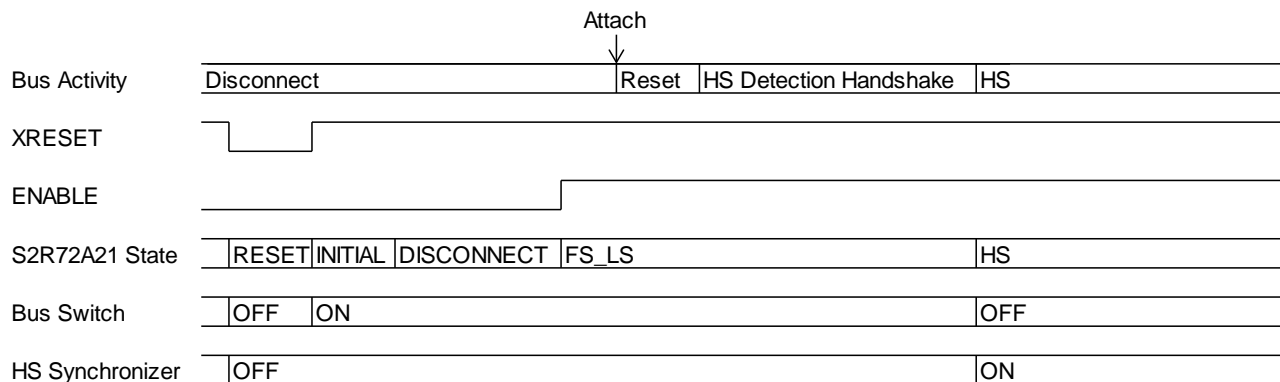
We would like to explain 2 cases of operation flow of S2R72A21 from Attach to Detach of a Device: DETACH state validation (EN_DETACH=1) and DETACH state invalidation (EN_DETACH=0).

6.1.3.1 In case of DETACH state validation (EN_DETACH=1)

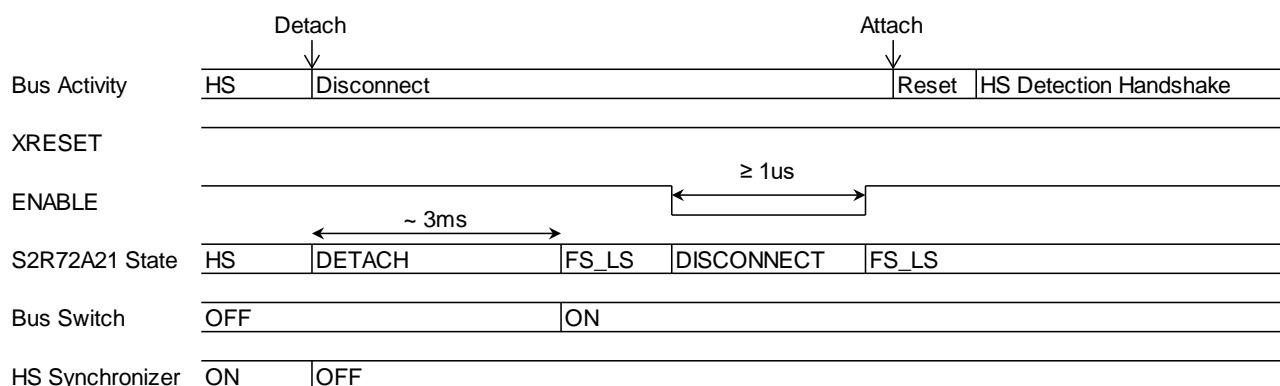
2 cases are shown below: ENABLE pin controlled and ENABLE pin stabled with 1.

- **Case ENABLE pin controlled**

Figure 6.1.3.1.1 shows the operation flow of DETACH state validation (EN_DETACH=1) and ENABLE pin controlled.



a) From Reset to Attach and HS communication condition



b) From Detach on HS Communication condition to Re-Attach

Figure 6.1.3.1.1 Operation flow (DETACH state Validation and ENABLE pin controlled)

Figure 6.1.3.1.1 a) shows the flow from Reset to Attach and HS communication condition. During XRESET=0, S2R72A21 would be RESET state, and the Bus Switch would be OFF. It would be INITIAL state after XRESET rises to 1 and the connection between INT port – EXT port would be done by the Bus Switch. Within this period the BC signal would pass through. From this condition, it would become DISCONNECT state if there are 10ms passes over. Furthermore, the transition to FS_LS state would occur when ENABLE=1 is detected and the Attach would be acceptable. When the HS Detection Handshake which starts from the Reset ends under this condition, it would become HS state and the HS communication would be possible since the HS Synchronizer would be ON.

Figure 6.1.3.1.1 b) shows the flow from Device Detach on the HS communication condition to Re-Attach. When the S2R72A21 detects the Device Detach within HS state, the transition towards DETACH state would start and the HS Synchronizer would be off as long as Bus Switch off condition continues for 3ms. Please detect the Detach externally. After 3ms passes, the transition to the FS_LS state would be done and the Bus Switch would connect INT port – EXT port. When the Detach is detected, notification of the Detach detection is done to the S2R72A21 by ENABLE=0. In this way the S2R72A21 would transit to DISCONNECT state. If ENABLE is set

to 1 then the S2R72A21 would make a transit to FS_LS state, and it would allow to accept Re-Attach. Within this process please maintain the low pulse width of the ENABLE signal over 1us.

Please refer to “S2R72A21 Application Note” for detailed ENABLE pin control.

Each operation’s timing is described on section 6.2.

- **Case ENABLE pin stabled with 1**

Figure 6.1.3.1.2 shows the operation flow of DETACH state validation (EN_DETACH=1) and ENABLE pin stabled with 1.

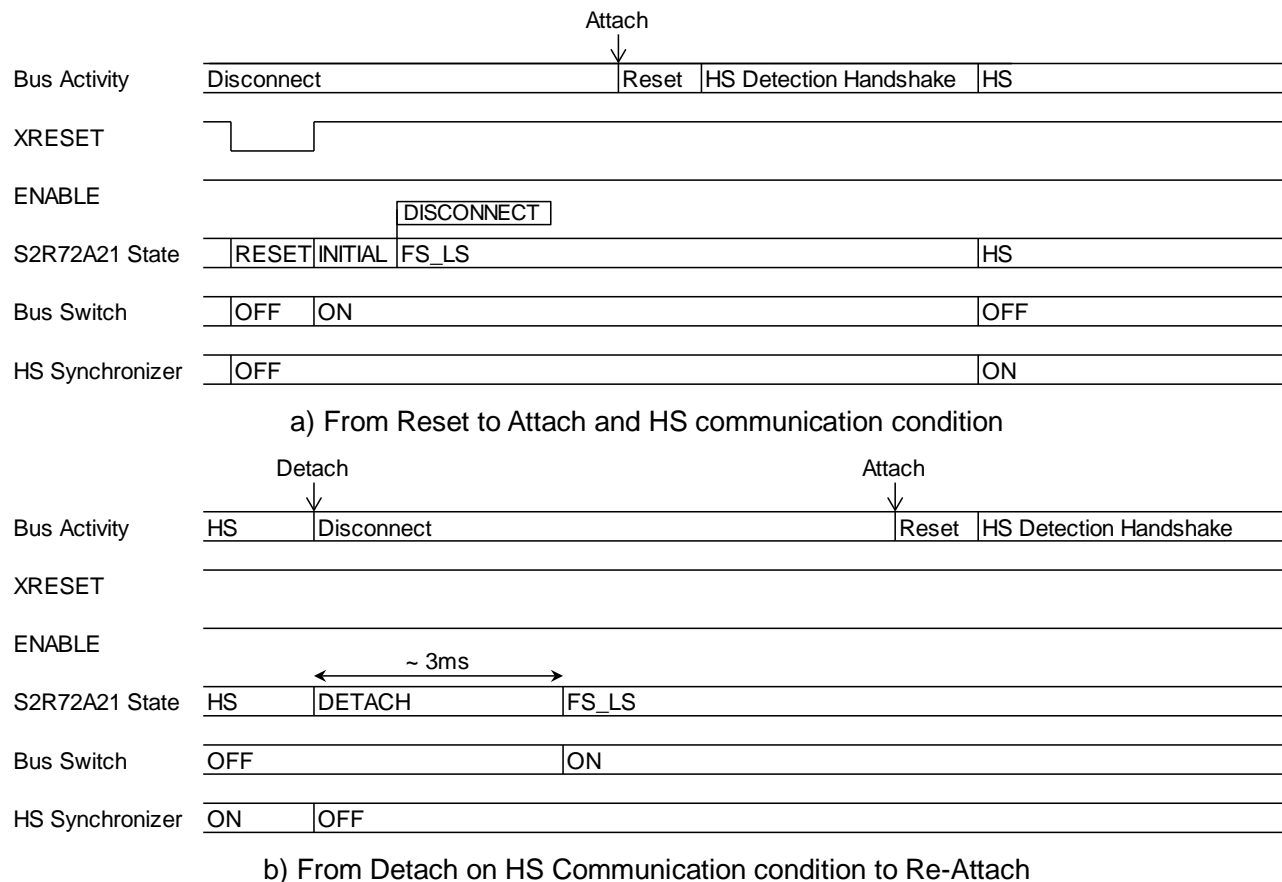


Figure 6.1.3.1.2 Operation flow (DETACH state Validation and ENABLE pin stabled 1)

Figure 6.1.3.1.2 a) shows the flow from Reset to Attach and HS communication condition. During XRESET=0, S2R72A21 would be RESET state, and the Bus Switch would be OFF. It would be INITIAL state after XRESET rises to 1 and the connection between INT port – EXT port would be done by the Bus Switch. Within this period the BC signal would pass through. From this condition, it would become DISCONNECT state if there are 10ms passes over, but the transition to FS_LS state would occur immediately since ENABLE=1 is detected. And the Attach would be acceptable. When the HS Detection Handshake which starts from the Reset ends under this condition, it would become HS state and the HS communication would be possible since the HS Synchronizer would be ON.

Figure 6.1.3.1.2 b) shows the flow from Device Detach on HS communication condition to Re-Attach. When the S2R72A21 detects the Device Detach within HS state, the transition towards DETACH state would start and the HS Synchronizer would be off as long as Bus Switch off condition continues for 3ms. Please detect the Detach externally. After 3ms passes, the transition to the FS_LS state would be done and the Bus Switch would connect INT port – EXT port. And the S2R72A21 would allow to accept Re-Attach.

Please refer to “S2R72A21 Application Note” for detailed information for the case ENABLE pin stabled with 1.

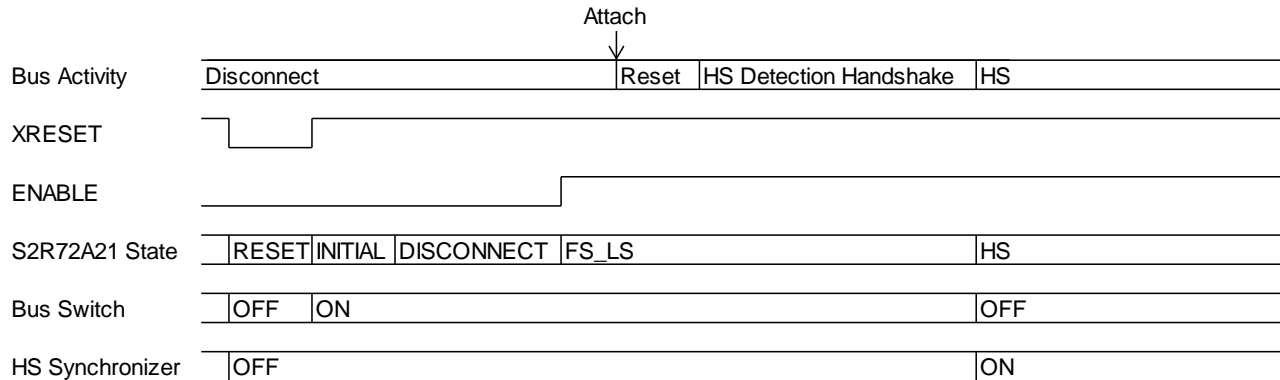
Each operation's timing is described on section 6.2.

6.1.3.2 In case of DETACH state invalidation (EN_DETACH=0)

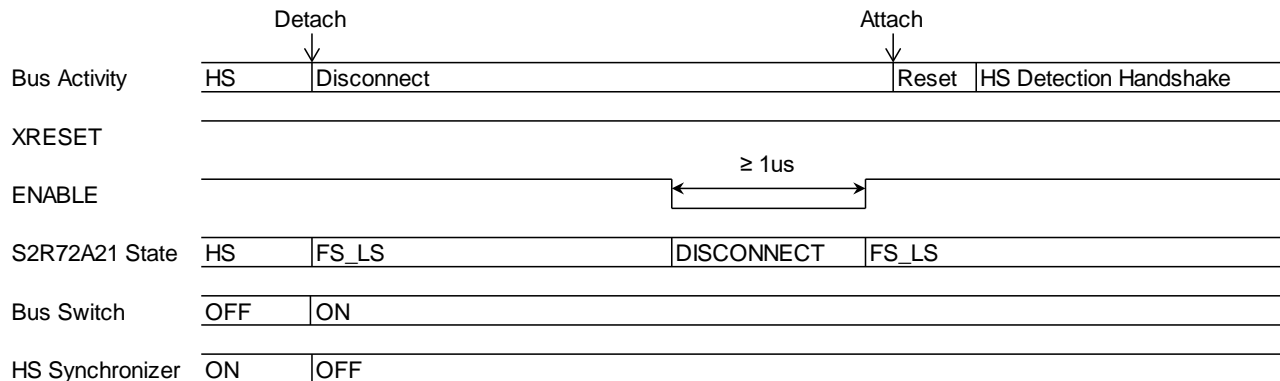
2 cases are shown below: ENABLE pin controlled and ENABLE pin stabled with 1.

- **Case ENABLE pin controlled**

Figure 6.1.3.2.1 shows the operation flow of DETACH state invalidation (EN_DETACH=0) and ENABLE pin controlled.



a) From reset to Attach and HS communication condition



b) From Detach on HS communication condition to Re-Attach

Figure 6.1.3.2.1 Operation flow (DETACH state Invalidation and ENABLE pin controlled)

Figure 6.1.3.2.1 a) shows the flow from Reset to Attach and HS communication condition. During XRESET=0 the S2R72A21 would be RESET state, and the Bus Switch would be OFF. It would be INITIAL state after XRESET rises to 1 and the connection between INT port – EXT port would be done by the Bus Switch. Within this period the BC signal would pass through. From this condition, it would become DISCONNECT state if there are 10ms passes over. Furthermore, the transition to FS_LS state would occur when ENABLE=1 is detected and the Attach would be acceptable. When the HS Detection Handshake which starts from the Reset ends under this condition, it would become HS state and the HS communication would be possible since the HS Synchronizer would be ON.

Figure 6.1.3.2.1 b) shows the flow from Device Detach on the HS communication condition to Re-Attach. When the S2R72A21 detects the Device Detach within HS state, the transition to FS_LS state would be done and the Bus switch would connect INT port – EXT port. From this the detection of Device Detach can be done externally. When the Detach is detected, notification of the Detach detection is done to the S2R72A21 by EN_DETACH=0. In this way the S2R72A21 would transit to DISCONNECT state. If ENABLE is set to 1, then the S2R72A21 would

make a transit to FS_LS state, and it would allow to accept Re-Attach. Within this process please maintain the low pulse width of the ENABLE signal over 1 μ s.

Please refer to “S2R72A21 Application Note” for detailed ENABLE pin control.

Each operation’s timing is described on section 6.2.

- **Case ENABLE pin stabled with 1**

Figure 6.1.3.2.2 shows the operation flow of DETACH state invalidation (EN_DETACH=0) and ENABLE pin stabled 1.

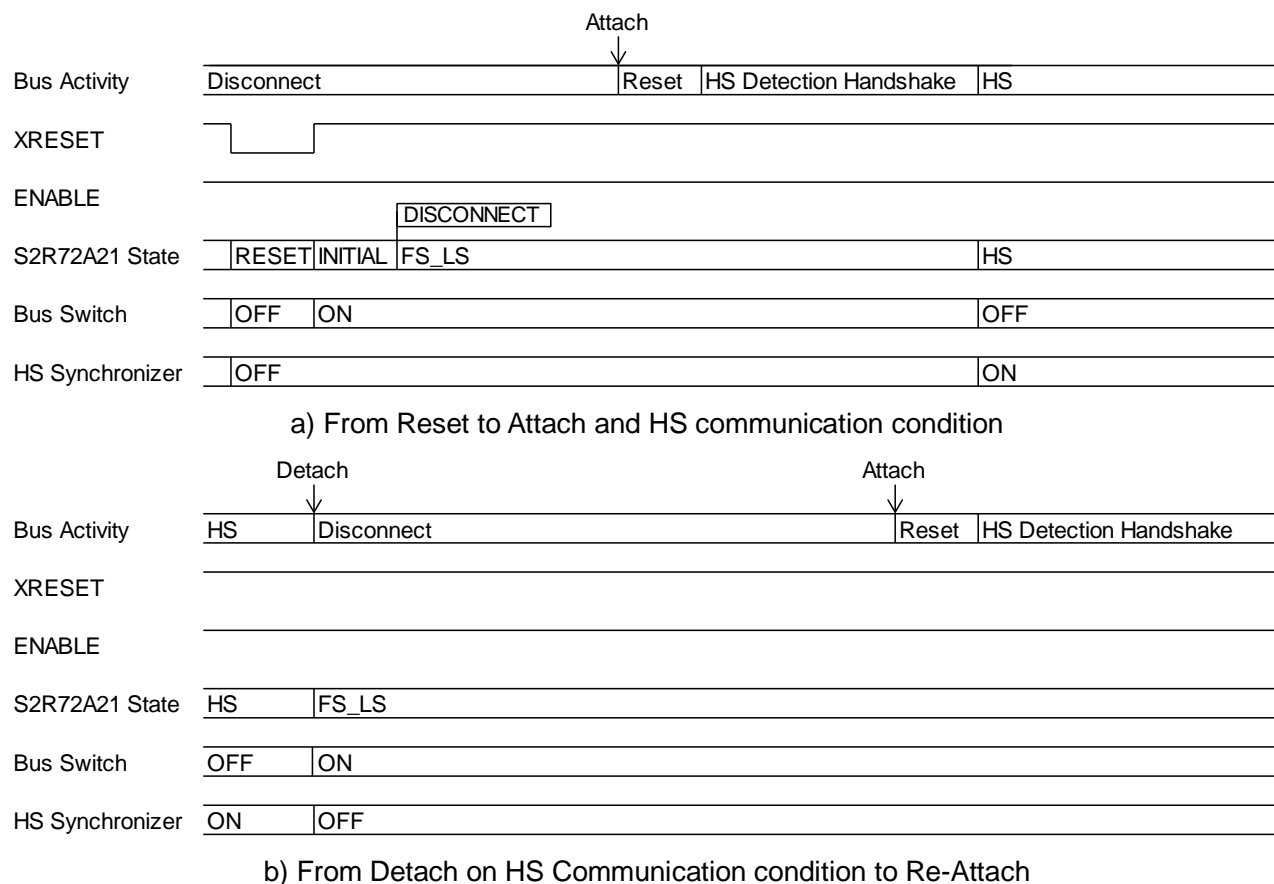


Figure 6.1.3.2.2 Operation flow (DETACH state Invalidation and ENABLE pin stabled 1)

Figure 6.1.3.2.2 a) shows the flow from Reset to Attach and HS communication condition. During XRESET=0, S2R72A21 would be RESET state, and the Bus Switch would be OFF. It would be INITIAL state after XRESET rises to 1 and the connection between INT port – EXT port would be done by the Bus Switch. Within this period the BC signal would pass through. From this condition, it would become DISCONNECT state if there are 10ms passes over, but the transition to FS_LS state would occur immediately since ENABLE=1 is detected. And the Attach would be acceptable. When the HS Detection Handshake which starts from the Reset ends under this condition, it would become HS state and the HS communication would be possible since the HS Synchronizer would be ON.

Figure 6.1.3.2.2 b) shows the flow of Device Detach from the HS communication condition to Re-Attach. When the S2R72A21 detects the Device Detach within HS state, the transition to the FS_LS state would be done and the Bus Switch would connect INT port – EXT port. From this the detection of Device Detach can be done externally. And the S2R72A21 would allow to accept Re-Attach.

Please refer to “S2R72A21 Application Note” for detailed information for the case ENABLE pin stabled with 1.

Each operation’s timing is described on section 6.2.

6.2 Operation timing

6.2.1 Reset release

It would take the Bus Switch around 10ms until it is fully operated after the reset is released. Within this period, Only the BC signal would pass through. After 10ms progresses, the FS/LS signal of the USB would start passing through.

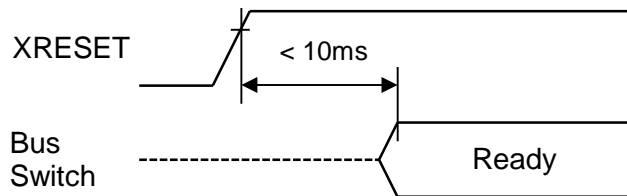


Figure 6.2.1.1 Reset Release

6.2.2 Connection / Disconnection

ENABLE pin is controlled to connect or disconnect the USB connection via the S2R72A21. To start the USB connection, please set ENABLE pin = 1. ENABLE pin is controlled to 0 in case when the host detect a Detach (USB connection).

Please refer to the below figure for the timings from ENABLE pin condition change to Bus Switch condition change.

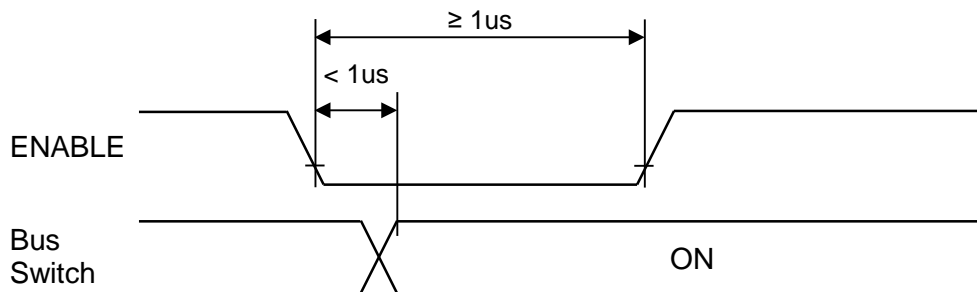


Figure 6.2.2.1 Bus Switch condition change by ENABLE pin

Please refer to “S2R72A21 Application Note” for detailed ENABLE pin control.

Regarding the HS Device Detach detection, we would make a separate explanation for the case the DETACH state is valid (when EN_DETACH=1) and the case DETACH state is invalid (when EN_DETACH=0).

6.2.2.1 In case DETACH state valid (in case EN_DETACH=1)

The HS Device Detach detection would be done with the following steps.

1. S2R72A21 would detect HS Device disconnection by SOF voltage level raise which is following to the Device side port. (Transition from HS state to DETACH state)
2. HS Synchronizer stop
Host would detect the disconnection.
3. Bus Switch would connect the INT and EXT port after 3ms (Transition from DETACH state to FS_LS state)

The timing is the following.

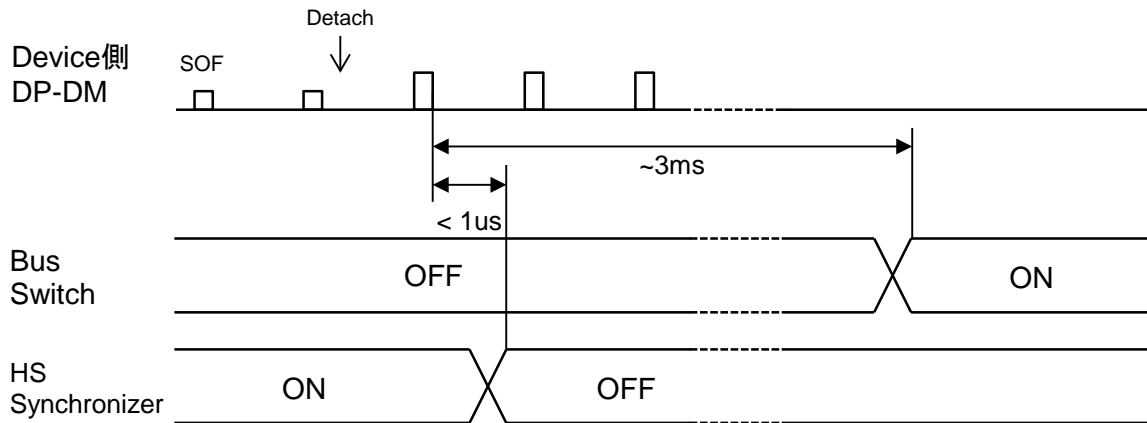


Figure 6.2.2.1.1 HS Device Detach detection (in case DETACH state valid)

6.2.2.2 In case DETACH state invalid (in case EN_DETACH=0)

The HS Device Detach detection would be done with the following steps.

1. S2R72A21 would detect HS Device disconnection by SOF voltage level raise which is following to the Device side port. (Transition from HS state to FS_LS state)
2. HS Synchronizer stop, Bus Switch connects INT port and EXT port
The Host detect the disconnection

The following is the timing.

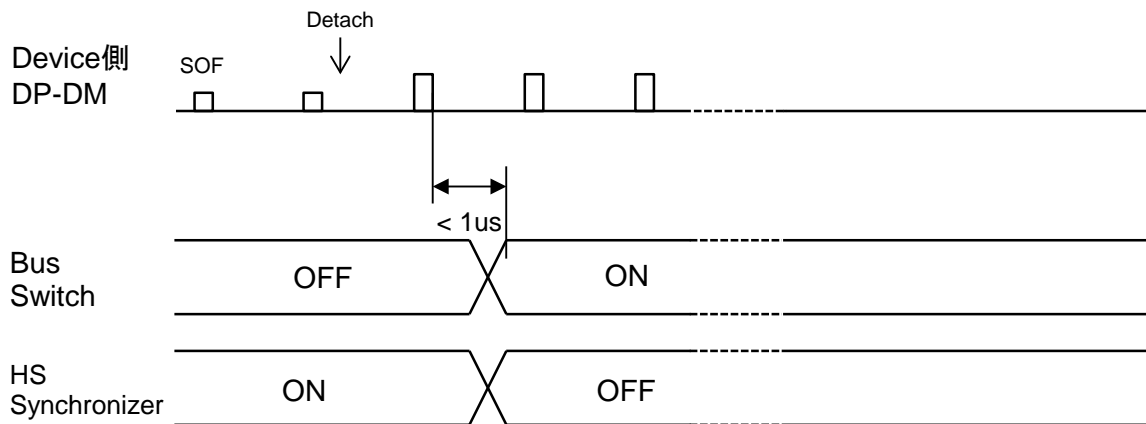


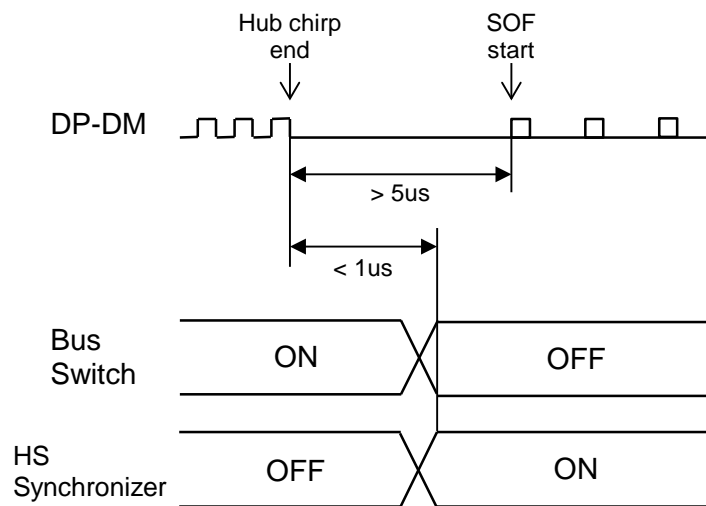
Figure 6.2.2.2.1 HS Device Detach detection (in case, DETACH state invalid)

6.2.3 Transition from FS_LS state to HS state

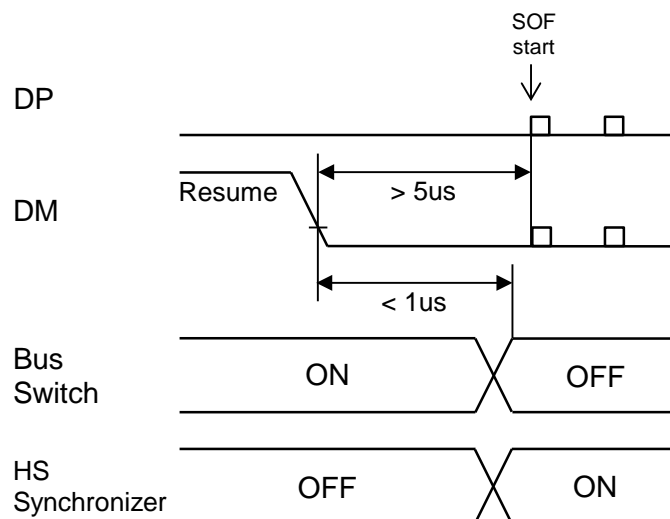
This section would explain the transition from the FS_LS state (section 6.1.2.4) to the HS state (section 6.1.2.5).

The transition to the HS state would operate when the ending of HS Detection Handshake or Resume of HS within the FS_LS state has been detected. Please refer to the following figure.

In addition, please maintain over 5 μs from Hub chirp ending to SOF transmit start up. Also please maintain over 5 μs from Resume of HS ending to SOF transmit start up.



a) HS Detection Handshake ending



b) Resume of HS ending

Figure 6.2.3.1 Transition from FS_LS state to HS state

6.2.4 Transition from HS state to FS_LS state

This section would explain the transition from HS state (section 6.1.2.5) to FS_LS state (section 6.1.2.4) in case of Reset or Suspend (3ms continuation of SE0). For the case of the HS Device Detach detection (DETACH state invalid), please refer to section 6.2.2.2.

The transition to the FS_LS state (from HS state) would operate when the detection of SE0 for 3ms (Reset or Suspend detection) on the INT/EXT port. Please refer to the following diagram for the transition timing. The Bus Switch would be ON until 3.0ms after Bus activity stop. In addition, please do not transmit the packet after 2.95 ms has passed from the Bus activity stop.

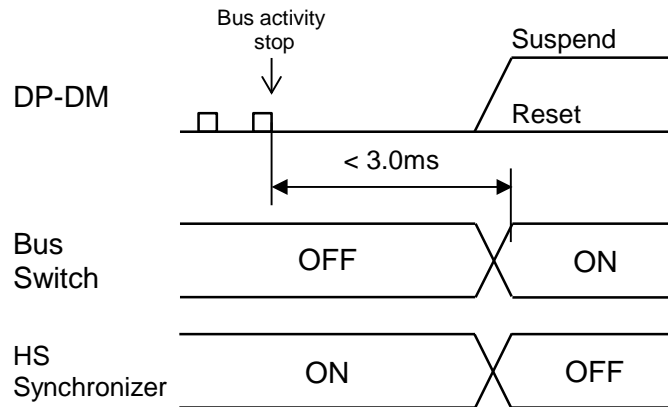


Figure 6.2.4.1 Reset / Suspend from HS

6.3 HS Synchronizer

HS Synchronizer would be activated during S2R72A21 HS state, and it would Re-Synchronize the HS packet received via either INT or EXT port and transmit to the other port.

HS Synchronizer would compensate the SYNC field to 32bit and send out.

The packet delay from Receive to Transmit would be the following diagram.

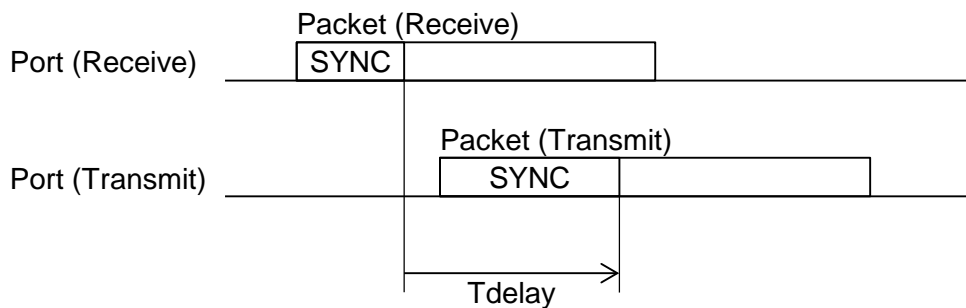


Figure 6.3.1 Packet delay by HS Synchronizer

The Max amount of Tdelay is as follows.

Received packet with 32bit SYNC: 40 bit time

Received packet with 12bit SYNC*: 60 bit time

*: The maximum hub-tier on the S2R72A21 inserted bus line is up to 4. Supported hub-tier is dependent on the host.

6.4 Transmission waveform shaping

S2R72A21 has a transmission waveform shaping which is HS transmit current control. The USB transmit signal quality (Eye Pattern) can be improved by controlling the current amount of HS transmission.

As for the setting of this feature, ADJ pin or I2C register is used. When using the I2C register, it is feasible to set up both INT/EXT port's current setting amount in details. When using the ADJ pin, it can only control the upper bit of the current setting amount of the EXT port. Please set "1" for I2C register setting and "0" for ADJ pin setting (Level of SEL_I2C pin).

Table 6.4.1 Settings of transmission waveform shaping function

Feature	Port	Case ADJ pin setting SEL_I2C=0	Case I2C register setting SEL_I2C=1
HS Tx current control	INT	Stabilize the base current amount (Level 0)	Feasible to control (in detail)
	EXT	Feasible to control	

When using this feature, please evaluate this function within your system to confirm the performance at the end.

6.4.1 HS transmission current control

HS transmission current control is a feature which controls the current used for transmitting from either INT or EXT port during HS connection. By this feature, it enables to control the amplitude of the USB signal. The control value is 4bit which corresponds to each INT port and EXT port.

With the controlling via the I2C register, it is feasible to set up 4bit (Internal control value) to each INT port and EXT port side. Please use and set up the INT_CUR bit of INT_ADJ register at the INT port side and EXT_CUR bit of the EXT_ADJ register at the EXT port side. Please refer to section 6.5.2 for I2C register map.

Within the control done by ADJ pin, it is feasible to set up 3pins (ADJ2, ADJ1 and ADJ0) with upper 3bit (4bit Internal control value) at the EXT port side. The least significant bit would be fixed with “0”. The INT port side’s control value is fixed with “0” (level 0).

Please refer to table 6.4.1.1 and table 6.4.1.2 for the relationship between setting values and the HS transmit current level. The transmit current is increased approx. 0.5mA per level. The signal level can reach disconnect detection threshold if the transmit current is increased too much. Therefore the recommended maximum HS transmit current level is limited to level 6 for the EXT port, level 2 for the INT port.

Table 6.4.1.1 EXT port HS transmit current (Setting value and transmitting current)

ADJ pin setting (SEL_I2C=0)	I2C register setting (SEL_I2C=1)	HS transmit current level	
{ADJ2, ADJ1, ADJ0}	EXT_CUR[3:0]		
{0, 0, 0}	0x0	Level 0	Min (Standard)
-	0x1	Level 1	
{0, 0, 1}	0x2	Level 2	
-	0x3	Level 3	
{0, 1, 0}	0x4	Level 4	
-	0x5	Level 5	
{0, 1, 1}	0x6	Level 6	Recommended Max
-	0x7	Caution ^{Note1}	
{1, 0, 0}	0x8		
-	0x9		
{1, 0, 1}	0xA		
-	0xB		
{1, 1, 0}	0xC		
-	0xD		
{1, 1, 1}	0xE		
-	0xF		

Table 6.4.1.2 INT port HS transmit current (Setting value and transmitting current)

I2C register setting (SEL_I2C=1) ^{Note2}	HS transmit current level
INT_CUR[3:0]	
0x0	Level 0 Min (Standard)
0x1	Level 1
0x2	Level 2 Recommended Max
0x3	Caution ^{Note1}
0x4	
0x5	
0x6	
0x7	
0x8	
0x9	
0xA	
0xB	
0xC	
0xD	
0xE	
0xF	

Note1: These settings can result in exceeding the HS disconnect detection level. Therefore, the HS disconnect detection can be provoked though the USB device is still connected. Evaluation on the actual system should be done carefully. HS signal amplitude can also exceed the voltage level of the provided eye pattern template. Please refer to "S2R72A21 Application Note"

Note2: In case the control done by ADJ pin (SEL_I2C=0), the setting is fixed to level 0 regardless of the ADJ pin setting.

6.5 I2C

S2R72A21 has an I2C slave interface for setting up each feature.

The objective I2C is 7bit address. 10bit address, General Call address, repeated START condition and Clock stretching are not supported. The Bus speeds are Standard-mode (Max 100kbps) and Fast-mode (max 400kbps).

In case when I2C would be used, please set up SEL_I2C="1".

The following is protocol of I2C and the register map.

6.5.1 I2C Protocol

6.5.1.1 Slave Address

Within the 7bit Slave address (I2C_OADR) of S2R72A21, the upper 4 bit is fixed with "4'b1010". The lower 3 bit is possible to set up by the ADJ2/1/0 pins. Please refer to the following table.

Table 6.5.1.1.1 Slave address

	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2C_OADR	1	0	1	0	ADJ2	ADJ1	ADJ0

6.5.1.2 Writing timing

The Writing towards the I2C register is done with the following procedures.

1. Issue the START condition
2. Attach and transmit R/W bit=1'b0 (WRITE) to the S2R72A21's Slave address (OADR[6:0])
3. Transmit the address "RADR[7:0]" of I2C register which is plan to be written
4. Transmit the written values (DATA[7:0]) to the I2C register
5. Issue STOP condition

Please refer to the following timing chart (writing).

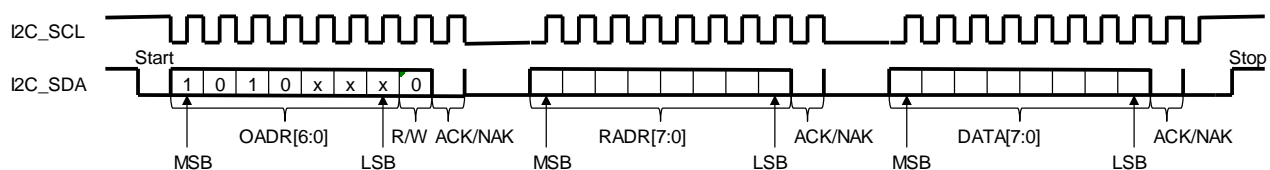


Figure 6.5.1.2.1 Writing Timing

6.5.1.3 Read out timing

The Read out from the I2C register is done with 2 phases. As for the 1st phase, write down the I2C's address RADR which is wished to be read out (WRITE). As for the 2nd phase, read out the register value (READ). The following shows the procedures.

1st phase : RADR write down

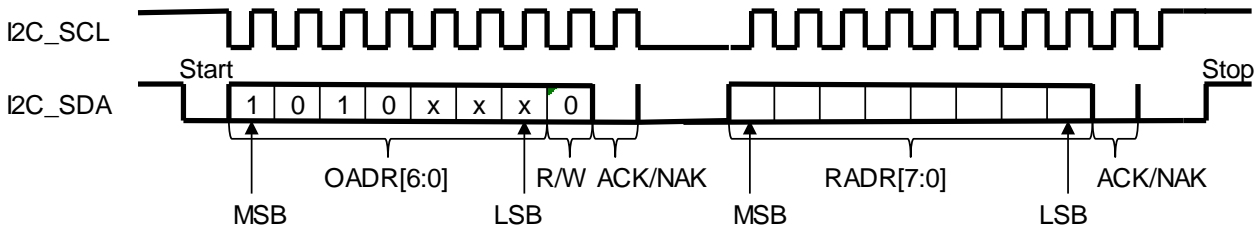
1. Issue the START condition
2. Attach and transmit R/W bit=1'b0 (WRITE) to the S2R72A21's Slave address (OADR[6:0])
3. Transmit the address "RADR[7:0]" of I2C register which is plan to be read out
4. Issue the STOP condition

2nd phase : Read out of the register value

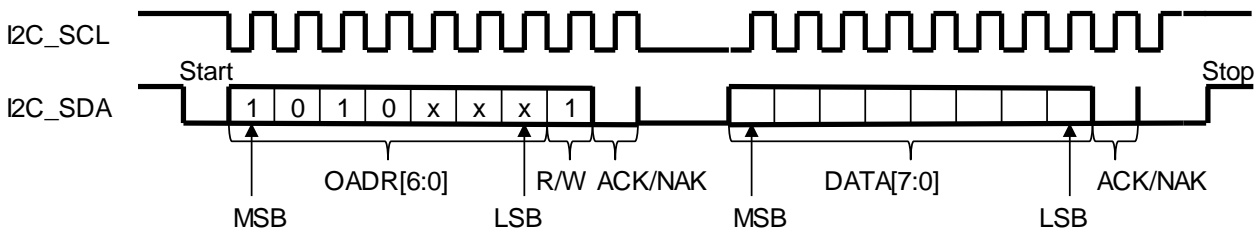
1. Issue the START condition.
2. Attach and transmit R/W bit=1'b1 (READ) to the S2R72A21's Slave address OADR[6:0]

3. Receive the register value DATA[7:0]
4. Issue the STOP condition

Please refer to the following diagrams for each timing.



a) 1st phase: RADR write down



b) 2nd phase: Register value read out

Figure 6.5.1.3.1 Read out timing

6.5.1.4 ACK / NAK

S2R72A21 would return the ACK or NAK after the Master has transmitted the OADR, RADR and DATA.

The case when the S2R72A21 returns the NAK is the followings

- When the OADR which is transmitted does not match with the Slave address, the NAK is returned after OADR transmit.
- When the RADR is beyond the specified domain, the NAK is returned after RADR transmit.

In other cases, ACK is returned.

After the Master receives the Data (after the 3rd step of the 2nd phase), please transmit either ACK or NAK to S2R72A21.

6.5.2 I2C register map

The following is the I2C register map.

All register would be reset to initial value via XRESET="0". All registers are feasible to read/write in case SEL_I2C="1".

These register configurations cannot be changed dynamically. Please write registers as initial configuration after S2R72A21 reset is released and before S2R72A21 transits to HS state, and do not change values afterward. And the initial values must be written to the Reserved bits.

Table 6.5.2.1 I2C register map

RADR	Reg name	Bit	Bit name	Init	R/W	Description
0x00	EXT_ADJ	7	-	0x0	R	-
		6-4	Reserved	0x0	R/W	Reserved
		3-0	EXT_CUR[3:0]	0x0	R/W	HS transmission current amount setting (EXT port side)
0x01	INT_ADJ	7	-	0x0	R	-
		6-4	Reserved	0x0	R/W	Reserved
		3-0	INT_CUR[3:0]	0x0	R/W	HS transmission current amount setting (INT port side)
0x02	STAT_SEL	7	STAT1_MODE	0x1	R/W	STAT1 pin output mode setting 0: Push-Pull 1: Open drain
		6	STAT1_INV	0x1	R/W	STAT1 pin output inversion setting 0: Do not invert 1: Invert
		5-4	STAT1_SEL[1:0]	0x1	R/W	Internal status selection which outputs to the STAT1 pin 0: HS 1: HostExt 2: State[0] 3: State[1]
		3	STAT0_MODE	0x1	R/W	STAT0 pin output mode setting 0: Push-Pull 1: Open drain
		2	STAT0_INV	0x1	R/W	STAT1 pin output inversion setting 0: Do not Invert 1: Invert
		1-0	STAT0_SEL[1:0]	0x0	R/W	Internal status selection which outputs to the STAT0 pin 0: HS 1: HostExt 2: State[0] 3: State[1]
0x03	REV_NO	7-0	-	-	R	IC revision 0xE4: S2R72A21F05E6

The signal which is selected by the registers STAT1_SEL and STAT0_SEL are explained in Section 6.6.

6.6 STAT pin output

STAT1 and STAT0 pins would output the internal status of the S2R72A21.

The following is the 3 types of status which can be output.

Table 6.6.1 Status which is output via STAT pin

Status	Description
HS	USB connection condition via S2R72A21 0: Condition besides HS connection (besides HS state) 1: HS connection (HS state)
HostExt	Port connected to the Host 0: INT port (SOF detection at the INT port during HS) 1: EXT port (SOF detection at the EXT port during HS)
State[1:0]	S2R72A21 state 0: DISCONNECT 1: DETACH 2: FS_LS 3: HS

Output signal from the STAT0 pin can be selected by the STAT0_SEL register (I2C). Same as that, the output signal from the STAT1 pin can be selected by the STAT1_SEL register (I2C).

The signal output from the STAT pins can be selected from push-pull (VSS or HVDD level output) or open drain done by the I2C's STATx_MODE register. Also the output level can be inverted by the STATx_INV register. Within each setting, the output level of the STAT pin vs. Status value is decided as following.

Table 6.6.2 Signal level output from the STAT pin

STATx_MODE	STATx_INV	Status value	STATx pin output
0	0	0	VSS level
		1	HVDD level
	1	0	HVDD level
		1	VSS level
1 (default)	0	0	VSS level
		1	HiZ
	1 (default)	0	HiZ
		1	VSS level

In case when the I2C is not used (SEL_I2C="0"), the STAT1 and STAT0 pin would be invert output (Open Drain), same as the above table's default setting. In this case, as for the status signal, the STAT1 would output the HostExt and STAT0 would output the HS.

7. Electrical Characteristics

7.1 Absolute maximum ratings

(V_{SS}=0V)

Contents	Symbol	Rating	Unit
Power supply voltage	HVDD	V _{SS} -0.3 ~ 4.0	V
Input Voltage	HVI	V _{SS} -0.3 ~ HVDD+0.5	V
	LVI ^{Note1}	V _{SS} -0.3 ~ 2.35	V
Output Voltage	HVO	V _{SS} -0.3 ~ HVDD+0.5	V
	LVO ^{Note2}	V _{SS} -0.3 ~ 2.35	V
Storage Temperature	Tstg	-65 ~ 150	°C

Note1: XI

Note2: XO

7.2 Recommended Operation Condition

(V_{SS}=0V)

Contents	Symbol	MIN	TYP	MAX	Unit
Power supply voltage	HVDD	3.00	3.30	3.60	V
Input Voltage	HVI	V _{SS} -0.3	-	HVDD+0.3	V
	LVI ^{Note1}	V _{SS} -0.3	-	2.15	V
Ambient Temperature	Ta	-40	25	105	°C

Note1: XI

7.3 DC Characteristics

HVDD=3.3V unless otherwise specified.

7.3.1 Power consumption

Contents		Symbol	Condition	MIN	TYP	MAX	unit
Standby current ^{Note1}							
Standby Current	HVDD	IDD1	Ta=25°C	-	20	30	mA
HS_IDLE current ^{Note2}							
HS_IDLE Current	HVDD	IDD2	Ta=25°C	-	32	-	mA
Operation current ^{Note3}							
Operation current	HVDD	IDD3	Ta=25°C	-	65	100	mA
Input Leak Pin: INT_DP / INT_DM, EXT_DP / EXT_DM							
Input leak current		IL		-	-	10	μA

Note1: This is the average current consumption after XRESET rises via Epson's measurement environment. Please refer to this value as for reference when evaluating power consumption.

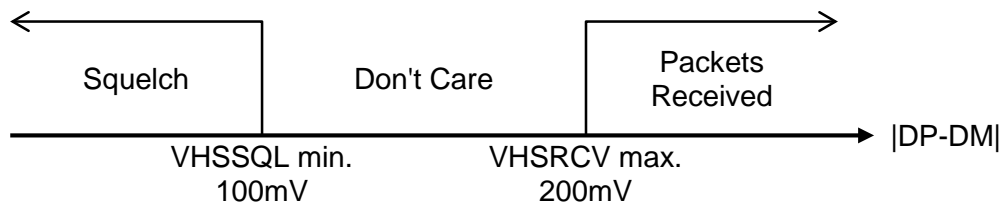
Note2: This is the average current consumption when the SOF packet (once every 125us) is re-synchronized from INT port to EXT port continuously within HS state. HS transmit current is level 0.

Note3: This is the average current consumed when the Test_Packet (Bus occupancy: 85.6%) is re-synchronized from INT port to EXT port continuously within HS state. HS transmit current is level 0. Please refer to this value as for reference when evaluating power supply capability of the power circuit.

7.3.2 Input Characteristics

(V_{SS}=0V)

Contents	Symbol	Condition	MIN	TYP	MAX	Unit
Input Characteristic (Schmitt)	PIN:	XRESET, ENABLE, EN_DETACH, FRC_THR, SEL_I2C, ADJ4, ADJ3, ADJ2, ADJ1, ADJ0, TESTEN				
Positive trigger voltage	VT1+	HVDD = 3.6V	1.2	-	2.52	V
Negative trigger voltage	VT1-	HVDD = 3.0V	0.75	-	1.98	V
Hysteresis voltage	ΔV1	HVDD = 3.0V	0.30	-	-	V



(V_{SS}=0V)

Contents	Symbol	Condition	MIN	TYP	MAX	Unit
USB input characteristics (HS Squelch)	PIN:	INT_DP / INT_DM(Pair), EXT_DP / EXT_DM(Pair)				
HS Squelch detection threshold voltage	VHSSQL		100	-	-	mV
USB input characteristics (HS Receiver)	PIN:	INT_DP / INT_DM(Pair), EXT_DP / EXT_DM(Pair)				
HS Receiver sensitivity threshold voltage	VHSRCV		-	-	200	mV
USB input characteristics (HS disconnection detection)	PIN:	INT_DP / INT_DM(Pair), EXT_DP / EXT_DM(Pair)				
Disconnection detection	VHSDSC		525	-	-	mV

7.3.3 Output Characteristics

(V_{SS}=0V)

Contents	Symbol	Condition	MIN	TYP	MAX	Unit
Output Characteristics	PIN:	STAT1, STAT0				
“L” Level output voltage	VOL1	HVDD = 3.0V IOL = 4mA	-	-	V _{SS} +0.4	V
Output Characteristics	PIN:	ADJ4 (I2C_SDA)				
“L” Level output voltage	VOL2	HVDD = 3.0V IOL = 1mA	-	-	V _{SS} +0.4	V

(V_{SS}=0V)

Contents	Symbol	Condition	MIN	TYP	MAX	Unit
USB output Characteristics (HS)	PIN:	EXT_DP / EXT_DM				
Transmission current (GND basis) ^{Note}	IOUHE		-19.5	-	-17.5	mA
USB output Characteristics (HS)	PIN:	INT_DP / INT_DM				
Transmission current (GND basis) ^{Note}	IOUHI		-21.5	-	-19.5	mA
USB output Characteristics (HS)	PIN:	INT_DP / INT_DM, EXT_DP / EXT_DM				
Termination resistance (GND basis)	ROUH		40.5	-	49.5	Ω

Note: In case when the HS transmission control function is not under usage (HS transmit current level 0)

7.3.4 Pin Capacitance

Contents	Symbol	Condition	MIN	TYP	MAX	Unit
Terminal capacity	PIN:	Input pin besides USB				
Input terminal capacity	CI	f = 1MHz	-	-	15	pF
Terminal capacity	PIN:	Output pin besides USB				
Output terminal capacity	CO	f = 1MHz	-	-	15	pF
Terminal capacity	PIN:	INT_DP / INT_DM, EXT_DP / EXT_DM				
Input and output terminal capacity (USB)	CBUH	f = 1MHz	-	-	20	pF

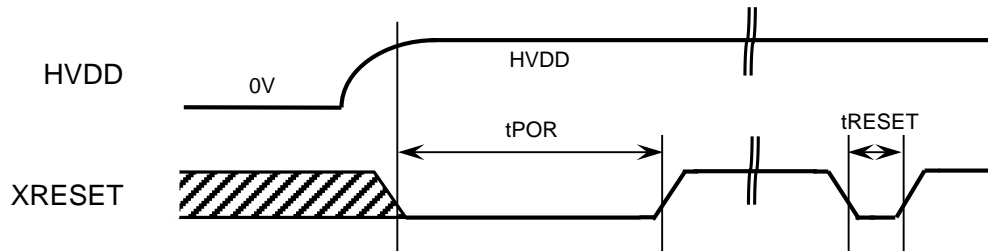
7.3.5 Bus Switch Characteristics

Contents	Symbol	Condition	MIN	TYP	MAX	Unit
Bus Switch Characteristics	PIN:	Between INT_DP and EXT_DP, between INT_DM and EXT_DM				
ON-resistance	RON	HVDD = 3.3V	-	6	-	Ω

7.4 AC characteristics

HVDD=3.3V unless otherwise specified.

7.4.1 RESET timings



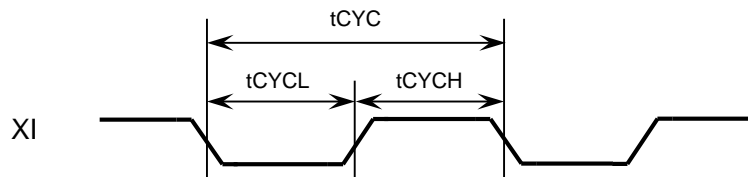
Symbol	Description	MIN	TYP	MAX	Unit
tPOR	Reset release during Power on ^{Note1}	100	–	–	us
tRESET	Reset pulse width ^{Note2}	400	–	–	ns

Note1: Period between HVDD start up to 90% and releasing period of XRESET (Low to High)

Note2: When tRESET is less than its minimum value, the RESET validation / invalidation is not guaranteed.

The base of XRESET pin level are 20% of HVDD-VSS.

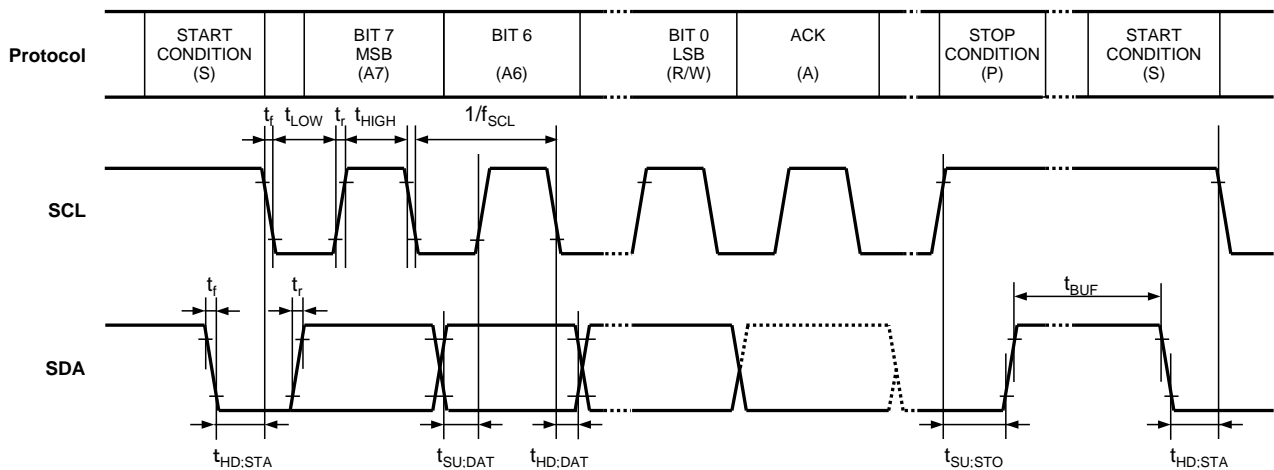
7.4.2 Clock timings



Symbol	Description	MIN	TYP	MAX	Unit
tCYC	Clock cycle	–	24.000	–	MHz
tCYCL tCYCH	Clock duty	–	50	–	%

Note: Epson recommends using Crystal OSC with a Frequency accuracy to be below ± 100 ppm.

7.4.3 I2C timings

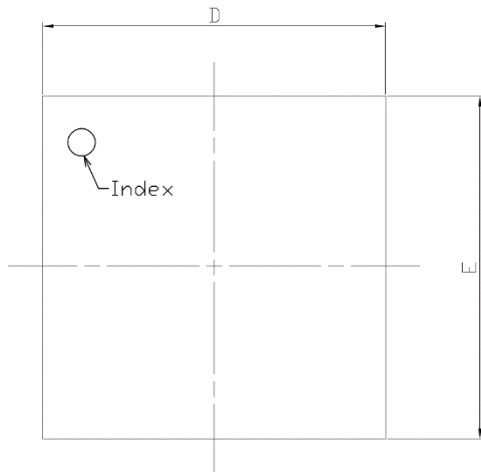


Signal	Description	100 kHz access (Standard-Mode)		400 kHz access (Fast-Mode)		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	-	100	-	400	kHz
$t_{HD,STA}$	hold time START condition	4.0	-	0.6	-	us
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	us
$t_{HD,DAT}$	data hold time	0	-	0	-	us
$t_{SU,DAT}$	data set-up time	250	-	100	-	ns
t_r	rise time of both SDA and SCL signals	-	1000	-	300	ns
t_f	fall time of both SDA and SCL signals	-	300	-	300	ns
$t_{SU,STO}$	set-up time for STOP condition	4.0	-	0.6	-	us
t_{BUF}	bus free time between a STOP and START condition	4.7	-	1.3	-	us

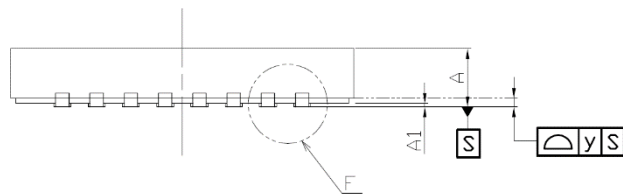
The base level of SCL pin and SDA pins are specified 30% and 70% of HVDD-VSS.

8. Dimensions

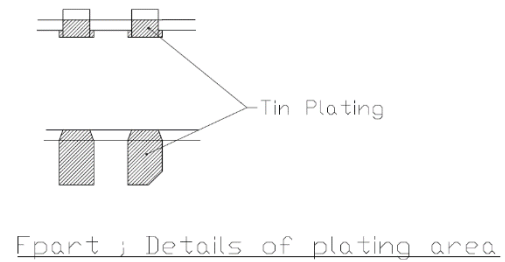
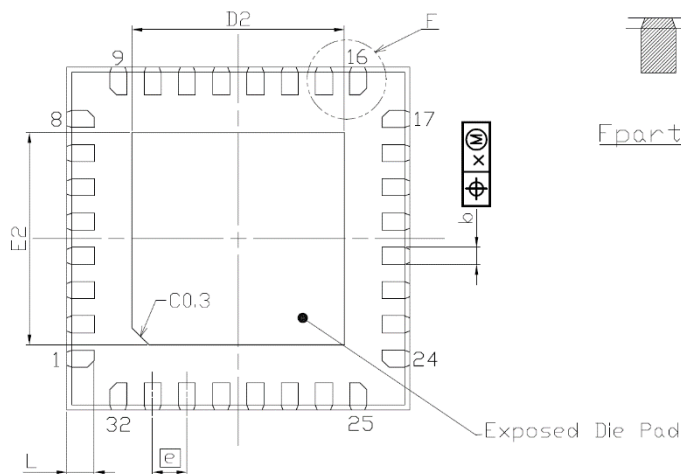
Top View



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.90	5.00	5.10
E	4.90	5.00	5.10
A	0.80	0.85	1.00
A_1	0.00	0.035	0.05
b	0.20	0.25	0.30
e	0.45	0.50	0.55
L	0.35	0.40	0.45
D_2	3.00	3.10	3.20
E_2	3.00	3.10	3.20
x	-	-	0.10
y	-	-	0.08



Bottom View



1 = 1mm

Note1: This dimension drawing may change without notification.

Note2: Exposed Die pad should be connected to VSS.

Figure 8.1 SQFN5-32PIN-W dimensions

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