S2D13515 Display Controller

Interfacing the Sharp LQ043xxx 480x272 TFT Panel

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NOTICE

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Chapter 1 Interfacing the Sharp LQ043xxx 480x272 TFT Panel

This document describes the hardware and software environment required to interface the S2D13515 Display Controller and Sharp LQ043xxxx 480x272 TFT Panel.

The designs described in this document are presented only as examples of how such interfaces might be implemented.

In the following example, the Sharp LQ043xxx panel is connected to FP2IO LCD interface of S2D13515.

1.1 Overview

The S2D13515 directly supports the Sharp LQ043xxx and requires no additional hardware and minimal programming. The S2D13515 register settings and electrical interface is described in the following sections.
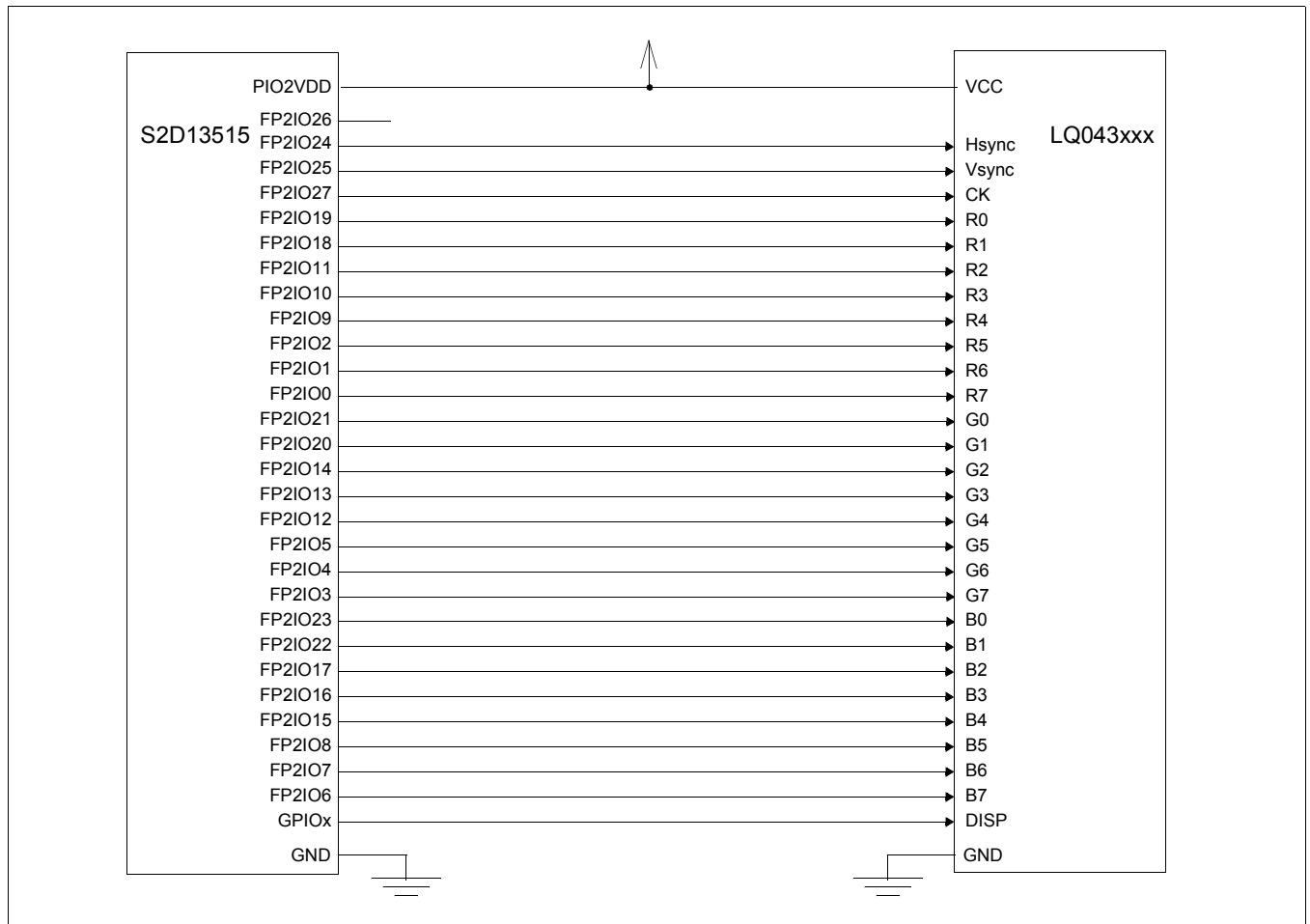

Figure 1-1: S2D13515 to Sharp LQ043xxx Connection Diagram

1.1.1 Electrical Interface

Table 1-1: Pin Mapping

S2D13515 Pin Name	LQ043xxxx Pin Name
FP2IO24	Hsync
FP2IO25	Vsync
FP2IO27	CK
FP2IO26	-
FP2IO19	R0
FP2IO18	R1
FP2IO11	R2
FP2IO10	R3
FP2IO9	R4
FP2IO2	R5
FP2IO1	R6
FP2IO0	R7
FP2IO21	G0
FP2IO20	G1
FP2IO14	G2
FP2IO13	G3
FP2IO12	G4
FP2IO5	G5
FP2IO4	G6
FP2IO3	G7
FP2IO23	B0
FP2IO22	B1
FP2IO17	B2
FP2IO16	B3
FP2IO15	B4
FP2IO8	B5
FP2IO7	B6
FP2IO6	B7
GPIOx (any GPIO pin)	DISP

The same power must be connected to PIO2VDD pins of S2D13515 and to VCC pins of Sharp LQ043xxx panel.

Display ON/OFF signal is provided by one of S2D13515 GPIO pins and it is under application software control. The LCD2 VNDP Status bit can be used to comply with the Sharp LQ043xxx requirement that DISP signal does not change while Vsync is low.

1.1.2 S2D13515 Register Settings for Sharp LQ043xxx, 480x272 TFT Panel

The registers listed below are only those associated with panel specific timing issues. All other registers are not shown here.

Table 1-2: Example Register Settings for Sharp LQ043xxx 480x272 TFT Panel

Register	Value	Comment
REG[0031h]	31h	set LCD2PCLK divide, LCD2PCLK = 8MHz assuming LCDCLK=80MHz
REG[4000h]	0Xh	LCD2 RGB8:8:8), generic RGB
REG[4001h]	BXh	Display data is latched on falling edge of PCLK, 24-bit panel
REG[4020h]	0Ch	Hsync period = 525 pixels
REG[4021h]	02h	
REG[4022h]	EFh	horizontal display period = 480 pixels
REG[4023h]	00	
REG[4024h]	2Ah	horizontal display period start position = 43 pixels
REG[4025h]	00h	
REG[4026h]	28h	Hsync width = 41 pixels, active low pulse
REG[4027h]	00h	
REG[4028h]	00h	Hsync start position = 0 pixels
REG[4029h]	00h	
REG[402Ah]	1Dh	Vsync period = 286 lines
REG[402Bh]	01h	
REG[402Ch]	0Fh	vertical display period = 272 lines
REG[402Dh]	01h	
REG[402Eh]	0Ch	vertical display period start position = 12 lines
REG[402Fh]	00h	
REG[4030h]	09h	Vsync width = 10 lines
REG[4031h]	00h	Vsync active low
REG[4032h]	00h	Vsync start position = 0 lines
REG[4033h]	00h	
REG[4070h]	01h	enable LCD2 output

The above values are intended as examples. This example assumes that CLKI = 20MHz and that the PLL2 is used to generate LCDCLK. Actual settings can vary and still remain within the LCD panel timing requirements.

Chapter 2 Change Record

X83A-A-001-01   Revision 1.1 - Issued: March 28, 2018

• updated Sales and Technical Support Section

• updated some formatting

X83A-A-001-01   Revision 1.0 - Issued: June 11, 2008

• all changes from the last revision are highlighted in Red

• initial release

Chapter 3 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

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