REG[00h] Revision Code Register [1] IO address = 1FFE0h [2], RO

Product Code = 001001						Revision Code = 00	
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 1	Bit 0

REG[01h] Mode Register 0 IO address = 1FFE1h, RW

TFT/STN	Dual/Single	Color/Mono [3]	FPLine Polarity	FPFrame Polarity	Mask FPSHIFT	Data Width [4]	
						Bit 1	Bit 0

REG[02h] Mode Register 1 IO address = 1FFE2h, RW

Bit-Per-Pixel [3]		High [5] Performance	Input Clock Div (CLKI/2)	Display Blank	Frame Repeat	Hw Video Invert Enable	Software Video Invert
Bit 1	Bit 0						

REG[03h] Mode Register 2 IO address = 1FFE3h, RW

						Sw Power Save [6]	
n/a	n/a	n/a	n/a	LCDPWR Override	Hardware PS Enable	Bit 1	Bit 0

REG[04h] Horizontal Panel Size Register IO address = 1FFE4h, RW

	Horizontal Panel Size = 8(REG + 1)						
n/a	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[05h] Vertical Panel Size Register (LSB) IO address = 1FFE5h, RW

Vertical Panel Size = (REG[05h], REG[06h]) + 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[06h] Vertical Panel Size Register (MSB) IO address = 1FFE6h, RW

						Vertical Panel Size	
n/a	n/a	n/a	n/a	n/a	n/a	Bit 9	Bit 8

REG[07h] FPLine Start Position IO address = 1FFE7h, RW

			FPLine Start Position = 8(REG[07h] + 2)				
n/a	n/a	n/a	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[08h] Horizontal Non-Display Period IO address = 1FFE8h, RW

			Horizontal Non-Display Period = 8(REG + 4)				
n/a	n/a	n/a	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[09h] FPFrame Start Position IO address = 1FFE9h, RW

		FPFrame Start Position					
n/a	n/a	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[0Ah] Vertical Non-Display Period Register IO address = 1FFEAh, RW

Vert Non-Disp Status	n/a	Vertical Non-Display Period					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[0Bh] MOD Rate Register IO address = 1FFEBh, RW

		MOD Rate					
n/a	n/a	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[0Ch] Screen 1 Start Word Address Register (LSB) IO address = 1FFECh, RW

Screen 1 Start Word Address = (REG[0Ch], REG[0Dh], REG[10] bit 1)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[0Dh] Screen 1 Start Word Address Register (MSB) IO address = 1FFEDh, RW

Screen 1 Start Word Address							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[0Eh] Screen 2 Start Word Address Register (LSB) IO address = 1FFEEh, RW

Screen 2 Start Word Address = (REG[0E], REG[0Fh], REG[10] bit 4)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[0Fh] Screen 2 Start Word Address Register (MSB) IO address = 1FFEFh, RW

Screen 2 Start Word Address							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[10h] Screen Start Address Overflow Register) IO address = 1FFF0h, RW

			Screen 2 Start Add Bit 16				Screen 1 Start Add Bit 16

REG[11h] Memory Address Offset Register IO address = 1FFF1h, RW

Memory Address Offset							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[12h] Screen 1 Vertical Size Register (LSB) IO address = 1FFF2h, RW

Screen 1 Vertical Size = (REG[12h], REG[13h])							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[13h] Screen 1 Vertical Size Register (MSB) IO address = 1FFF3h, RW

						Screen 1 Vertical Size	
n/a	n/a	n/a	n/a	n/a	n/a	Bit 9	Bit 8

REG[15h] Look-Up Table Address Register IO address = 1FFF5h, RW

Look-Up Table Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[17h] Look-Up Table Data Register IO address = 1FFF7h, RW

Look-Up Table Data							
Bit 3	Bit 2	Bit 1	Bit 0	n/a	n/a	n/a	n/a

REG[18h] GPIO Configuration Control Register IO address = 1FFF8h, RW

n/a	n/a	n/a	GPIO4 Pin IO Config	GPIO3 Pin IO Config	GPIO2 Pin IO Config	GPIO1 Pin IO Config	GPIO0 Pin IO Config

REG[19h] GPIO Status / Control Register IO address = 1FFF9h, RW

n/a	n/a	n/a	GPIO4 Pin IO Status	GPIO3 Pin IO Status	GPIO2 Pin IO Status	GPIO1 Pin IO Status	GPIO0 Pin IO Status

REG[1Ah] Scratch Pad Register IO address = 1FFFAh, RW

Scratch Pad Register							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[1Bh] SwivelView Mode Register IO address = 1FFFBh, RW

SwivelView Mode En.	SwivelView Mode Sel.	n/a	n/a	n/a	reserved	SwivelView PCLK Select	
						Bit 1	Bit 0

REG[1Ch] Line Byte Count Register IO address = 1FFFCh, RW

Line Byte Count							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Notes

1 These bits are used to identify the S1D13705 at power on / reset.

2 IO addresses are relative to the beginning of display memory.

3 Gray Shade/Color Mode Selection

Color/Mono REG[01] bit 5	Bit-Per-Pixel Bit 1 REG[02] bit 7	Bit-Per-Pixel Bit 0 REG[02] bit 6	Display Mode	
1	0	0	2 Colors	1 Bit-Per-Pixel
		1	4 Colors	2 Bit-Per-Pixel
	1	0	16 Colors	4 Bit-Per-Pixel
		1	256 Colors	8 Bit-Per-Pixel
0	0	0	2 Gray Shade	1 Bit-Per-Pixel
		1	4 Gray Shade	2 Bit-Per-Pixel
	1	0	16 Gray Shade	4 Bit-Per-Pixel
		1	reserved	

4 Panel Data Format

TFT/STN REG[01] bit 7	Color/ Mono REG[01] bit 5	Dual/ Single REG[01] bit 6	Data Width Bit 1 REG[01] bit 1	Data Width Bit 0 REG[01] bit 0	Function
0	0	0	0	0	Mono Single 4-bit LCD
				1	Mono Single 8-bit LCD
			1	0	reserved
				1	reserved
		1	0	0	reserved
				1	Mono Dual 8-bit LCD
			1	0	reserved
				1	reserved
	1	0	0	0	Color Single 4-bit LCD
				1	Color Single 8-bit LCD Format 1
			1	0	reserved
				1	Color Single 8-bit LCD Format 2
		1	0	0	reserved
				1	Color Dual 8-bit LCD
			1	0	reserved
				1	reserved
1	don't care			0	9 bit TFT Panel
				1	12 bit TFT Panel

5 High Performance Selection

High Performance	Bit-Per-Pixel Bit 1 REG[02] bit 7	Bit-Per-Pixel Bit 0 REG[02] bit 6	Display Modes	
0	0	0	MClk = PClk/8	1 bit-per-pixel
		1	MClk = PClk/4	2 bit-per-pixel
	1	0	MClk = PClk/2	4 bit-per-pixel
		1	MClk = PClk	8 bit-per-pixel
1	X	X	MClk = PClk	

6 Power Save Mode Selection

Power Save Bit 1	Power Save Bit 0	Mode
0	0	Power Save Mode 1
0	1	reserved
1	0	reserved
1	1	Normal Operation