REG[00h] Revision Code Register [1] — RO

Product Code = 001010						Revision Code = 00	
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 1	Bit 0

REG[01h] Display Buffer Size Register — RW

Display Buffer Size							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[02h] Configuration Readback Register — RO

CNF7 Status	CNF6 Status	CNF5 Status	CNF4 Status	CNF3 Status	CNF2 Status	CNF1 Status	CNF0 Status

REG[04h] Memory Clock Configuration Register [2] — RW

n/a	n/a	MCLK Divide Select		n/a	n/a	n/a	Reserved
		bit 1	bit 0				

REG[05h] Pixel Clock Configuration Register [3,4] — RW

n/a	PCLK Divide Select			n/a	n/a	PCLK Source Select	
	Bit 2	Bit 1	Bit 0			Bit 1	Bit 0

REG[08h] Look-Up Table Blue Write Data Register — WO

LUT Blue Write Data							
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	n/a	n/a

REG[09h] Look-Up Table Green Write Data Register — WO

LUT Green Write Data							
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	n/a	n/a

REG[0Ah] Look-Up Table Red Write Data Register — WO

LUT Red Write Data							
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	n/a	n/a

REG[0Bh] Look-Up Table Write Address Register — WO

LUT Write Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[0Ch] Look-Up Table Blue Read Data Register — RO

LUT Blue Read Data							
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	n/a	n/a

REG[0Dh] Look-Up Table Green Read Data Register — RO

LUT Green Read Data							
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	n/a	n/a

REG[0Eh] Look-Up Table Red Read Data Register — RO

LUT Red Write Data							
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	n/a	n/a

REG[0Fh] Look-Up Table Read Address Register — WO

LUT Read Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[10h] Panel Type Register [5,6] — RW

Panel Data Format Select	Color/Mono Panel Select	Panel Data Width		Active Panel Res. Select	n/a	Panel Type	
		Bit 1	Bit 0			Bit 1	Bit 0

REG[11h] MOD Rate Register — RW

n/a	n/a	MOD Rate					
		bit 5	bit 4	bit 3	bit 2	bit1	bit 0

REG[12h] Horizontal Total Register — RW

n/a	Horizontal Total						
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[14h] Horizontal Display Period Register — RW

n/a	Horizontal Display Period						
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[16h] Horizontal Display Period Start Position Register 0 — RW

Horizontal Display Period Start Position							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

REG[17h] Horizontal Display Period Start Position Register 1 — RW

n/a	n/a	n/a	n/a	n/a	n/a	Horizontal Display Period Start Position	
						bit 9	bit 8

REG[18h] Vertical Total Register 0 — RW

Vertical Total							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[19h] Vertical Total Register 1 — RW

n/a	n/a	n/a	n/a	n/a	n/a	Vertical Total	
						Bit 9	Bit 8

REG[1Ch] Vertical Display Period Register 0 — RW

Vertical Display Period							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[1Dh] Vertical Display Period Register 1 — RW

n/a	n/a	n/a	n/a	n/a	n/a	Vertical Display Period	
						Bit 9	Bit 8

REG[1Eh] Vertical Display Period Start Position Register 0 — RW

Vertical Display Period Start Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[1Fh] Vertical Display Period Start Position Register 1 — RW

n/a	n/a	n/a	n/a	n/a	n/a	Vertical Display Period Start Position	
						bit 9	bit 8

REG[20h] FPLINE Pulse Width Register — RW

FPLINE Pulse Polarity	FPLINE Pulse Width						
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[22h] FPLINE Pulse Start Position Register 0 — RW

FPLINE Pulse Start Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[23h] FPLINE Pulse Start Position Register 1 — RW

n/a	n/a	n/a	n/a	n/a	n/a	FPLINE Pulse Start Position	
						Bit 9	Bit 8

REG[24h] FPFRAME Pulse Width Register — RW

FPFRAME Pulse Polarity	n/a	n/a	n/a	n/a	FPFRAME Pulse Width		
					Bit 2	Bit 1	Bit 0

REG[26h] FPFRAME Pulse Start Position Register 0 — RW

FPFRAME Pulse Start Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[27h] FPFRAME Pulse Start Position Register 1 — RW

n/a	n/a	n/a	n/a	n/a	n/a	FPFRAME Pulse Start Position	
						Bit 9	Bit 8

REG[28h] D-TFD GCP Index Register — RW

n/a	n/a	n/a	D-TFD GCP Index				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[2Ch] D-TFD GCP Data Register — RW

D-TFD GCP Data							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[70h] Display Mode Register [7] — RW

Display Blank	Dithering Disable	Hardware Video Invert Enable	Software Video Invert	n/a	Bit-per-pixel Select		
					Bit 2	Bit 1	Bit 0

REG[71h] Special Effects Register [8] — RW

Display Data Word Swap	Display Data Byte Swap	n/a	Sub-Window Enable	n/a	n/a	SwivelView™ Mode Select	
						Bit 1	Bit 0

REG[74h] Main Window Display Start Address Register 0 — RW

Main Window Display Start Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[75h] Main Window Display Start Address Register 1 — RW

Main Window Display Start Address							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[76h] Main Window Display Start Address Register 2 — RW

n/a	n/a	n/a	n/a	n/a	n/a	n/a	Main Window Display Start Address Bit 16

REG[78h] Main Window Line Address Offset Register 0 — RW

Main Window Line Address Offset							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[79h] Main Window Line Address Offset Register 1 — RW

n/a	n/a	n/a	n/a	n/a	n/a	Main Window Line Address Offset	
						Bit 9	Bit 8

REG[7Ch] Sub-Window Display Start Address Register 0 — RW

Sub-Window Display Start Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[7Dh] Sub-Window Display Start Address Register 1 — RW

Sub-Window Display Start Address							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[7Eh] Sub-Window Display Start Address Register 2 — RW

n/a	n/a	n/a	n/a	n/a	n/a	n/a	Sub-Window Display Start Address Bit 16

REG[80h] Sub-Window Line Address Offset Register 0 — RW

Sub-Window Line Address Offset							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[81h] Sub-Window Line Address Offset Register 1 — RW

n/a	n/a	n/a	n/a	n/a	n/a	Sub-Window Line Address Offset	
						Bit 9	Bit 8

REG[84h] Sub-Window X Start Position Register 0 — RW

Sub-Window X Start Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[85h] Sub-Window X Start Position Register 1 — RW

n/a	n/a	n/a	n/a	n/a	n/a	Sub-Window X Start Position	
						Bit 9	Bit 8

REG[88h] Sub-Window Y Start Position Register 0 — RW

Sub-Window Y Start Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[89h] Sub-Window Y Start Position Register 1							RW
n/a	n/a	n/a	n/a	n/a	n/a	Sub-Window Y Start Position	
						Bit 9	Bit 8

REG[8Ch] Sub-Window X End Position Register 0							RW
Sub-Window X End Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[8Dh] Sub-Window X End Position Register 1							RW
n/a	n/a	n/a	n/a	n/a	n/a	Sub-Window X End Position	
						Bit 9	Bit 8

REG[90h] Sub-Window Y End Position Register 0							RW
Sub-Window Y End Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[91h] Sub-Window Y End Position Register 1							RW
n/a	n/a	n/a	n/a	n/a	n/a	Sub-Window Y End Position	
						Bit 9	Bit 8

REG[A0h] Power Save Configuration Register							RW
VNDP Status (RO)	n/a	n/a	n/a	Memory Controller Power Save Status (RO)	n/a	n/a	Power Save Mode Enable

REG[A1h] Reserved							RW
n/a	n/a	n/a	n/a	n/a	n/a	n/a	Reserved

REG[A2h] Software Reset Register							RW
Reserved	n/a	n/a	n/a	n/a	n/a	n/a	Software Reset (WO)

REG[A3h] Reserved							RW
Reserved	n/a	n/a	n/a	n/a	n/a	n/a	n/a

REG[A4h] Scratch Pad Register 0							RW
Scratch Pad							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[A5h] Scratch Pad Register 1							RW
Scratch Pad							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[A8h] General Purpose IO Pins Configuration Register 0							RW
n/a	GPIO6 Pin IO Config	GPIO5 Pin IO Config	GPIO4 Pin IO Config	GPIO3 Pin IO Config	GPIO2 Pin IO Config	GPIO1 Pin IO Config	GPIO0 Pin IO Config

REG[A9h] General Purpose IO Pins Configuration Register 1							RW
GPIO Pin Input Enable	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

REG[ACh] General Purpose IO Pins Status/Control Register 0							RW
n/a	GPIO6 Pin IO Status	GPIO5 Pin IO Status	GPIO4 Pin IO Status	GPIO3 Pin IO Status	GPIO2 Pin IO Status	GPIO1 Pin IO Status	GPIO0 Pin IO Status

REG[ADh] General Purpose IO Pins Status/Control Register 1							RW
GPO Control	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

REG[B0h] PWM Clock / CV Pulse Control Register							RW
PWM Clock Force High	n/a	n/a	PWM Clock Enable	CV Pulse Force High	CV Pulse Burst Status (RO)	CV Pulse Burst Start	CV Pulse Enable

REG[B1h] PWM Clock / CV Pulse Configuration Register [9,10]							RW
PWM Clock Divide Select				CV Pulse Divide Select			PWMCLK Source Select
Bit 3	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	

REG[B2h] CV Pulse Burst Length Register								RW
CV Pulse Burst Length								
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

REG[B3h] PWMOUT Duty Cycle Register [11]								RW
PWMOUT Duty Cycle								
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Notes

1 REG[00h] These bits are used to identify the S1D13706. For the S1D13706, the product code should be 10.

2 REG[04h] Memory Clock Configuration Register

MCLK Divide Select Bits	BCLK to MCLK Frequency Ratio
00	1:1
01	2:1
10	3:1
11	4:1

3 REG[05h] Pixel Clock Configuration Register

PCLK Divide Select Bits	PCLK Source to PCLK Frequency Ratio
000	1:1
001	2:1
010	3:1
011	4:1
1XX	8:1

4 REG[05h] Pixel Clock Configuration Register

PCLK Source Select Bits	PCLK Source
00	MCLK
01	BCLK
10	CLKI
11	CLKI2

5 REG[10h] Panel Type Register

Panel Data Width Bits [1:0]	Passive LCD Panel Data Width Size	Active Panel Data Width Size
00	4-bit	9-bit
01	8-bit	12-bit
10	16-bit	18-bit
11	Reserved	Reserved

6 REG[10h] Panel Type Register

REG[10h] Bits[1:0]	Panel Type
00	STN
01	TFT
10	HR-TFT
11	D-TFD

7 REG[70h] Display Mode Register

Bit-per-pixel Select Bits [1:0]	Color Depth (bpp)	Maximum Number of Colors/Shades		Max. No. Of Simultaneously Displayed Colors/ Shades
		Passive Panel (Dithering On)	TFT Panel	
000	1 bpp	256K/64	256K/64	2/2
001	2 bpp	256K/64	256K/64	4/4
010	4 bpp	256K/64	256K/64	16/16
011	8 bpp	256K/64	256K/64	256/64
100	16 bpp	64K/64	64K/64	64K/64
101, 110, 111	Reserved	n/a	n/a	n/a

8 REG[71h] Special Effects Register

SwivelView™ Mode Select Bits	SwivelView™ Orientation
00	Normal
01	90°
10	180°
11	270°

9 REG[B1h] PWM Clock / CV Pulse Configuration Register

PWM Clock Divide Select Bits [3:0]	PWM Clock Divide Amount
0h	1
1h	2
2h	4
3h	8
...	...
Ch	4096
Dh-Fh	Reserved

10 REG[B1h] PWM Clock / CV Pulse Configuration Register

CV Pulse Divide Select Bits [2:0]	CV Pulse Divide Amount
0h	1
1h	2
2h	4
3h	8
...	...
7h	128

11 REG[B3h] PWMOUT Duty Cycle Register

PWMOUT Duty Cycle [7:0]	PWMOUT Duty Cycle
00h	Always Low
01h	High for 1 out of 256 clock periods
02h	High for 2 out of 256 clock periods
...	...
FFh	High for 255 out of 256 clock periods