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S1D13781

Power Consumption

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SEIKO EPSON CORPORATION

Rev.1.4

NOTICE

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1 S1D13781 Power Consumption

S1D13781 power consumption is affected by many system design variables.

- Memory clock frequency (MCLK): CPU performance to memory, and other functions – the higher the frequency, the higher the performance and power consumption.
- Pixel clock frequency (PCLK): determines the LCD frame-rate – the higher the frequency, the higher the frame-rate and power consumption.
- V_{DD} voltage level: the voltage level affects power consumption – the higher the voltage, the higher the power consumption.
- Display mode: the resolution and color depth affect power consumption – the higher the resolution/color depth, the higher the power consumption.
- Layer Rotation: using a layer rotation option of either 90 or 270 degrees, will be higher power consumption than 0 or 180 degrees.
- Look Up Table: if a LUT is used, then power consumption will be higher.

The S1D13781 supports software initiated power save modes. The power consumption in power save modes is affected by various system design variables.

- Clock states during the power save mode: disabling the clocks during power save mode has substantial power savings.

1.1 Conditions

The following table provides examples of typical configurations for some 320x240 panels and their effects on power consumption. The following conditions apply.

- All tests were run with a static full color palette display.
- All tests were done using the Direct 16-bit Mode 1 host bus interface.
- All tests set the PLL/MCLK for 60MHz, from a CLKI of 24MHz.

Table 1-1: S1D13781 Total Power Consumption for 320x240 panels

Test Condition *$COREV_{DD}$ and $PLLV_{DD}$ = 1.5V and IOV_{DD} = 3.3V*							**Current Consumption (mA)** **S1D13781 Active**		
Resolution	**Panel Type**	**Frame Rate**	**Clocks (MHz) Other Consideration**	**Rotation**	**LUT**	**Color Depth**	**CORE**	**PLL**	**IO**
320x240	18-bit TFT	57	CLKI = 24.0 MHz POCLK/MCLK = 60.0 MHz PCLK = MCLK / 7	0	Yes	24	3.977	0.530	2.195
		57		90	Yes	24	4.789	0.530	1.927
		0	CLKI = 24.0 MHz POCLK/MCLK = 60.0 MHz PCLK = MCLK / 7 Power Save Enabled = PSM1	0	Yes	24	2.150	0.530	0.101
		0	CLKI = STOPPED POCLK/MCLK = 0.0 MHz PCLK = MCLK / 7 Power Save Enabled = PSM0	0	Yes	24	0.005	0	0.071
	Color STN 8-bit Format 2	68		0	Yes	24	4.290	0.530	1.347
		68		90	Yes	24	5.260	0.530	1.347
	Mono STN 8-bit	70		0	Yes	8 for Mono	3.353	0.532	0.999

The following table provides an example of a 480x272 24-bit TFT panel and the effects on power consumption for specific environments. The following conditions apply.

- All tests were run with a static full color palette display, **except the test where the 2D BitBLT engine was running**.
- All tests were done using the Direct 16-bit Mode 1 host bus interface.

Table 1-2: S1D13781 Total Power Consumption for 480x272 panels

Test Condition *$COREV_{DD}$ and $PLLV_{DD}$ = 1.5V and IOV_{DD} = 3.3V*							**Current Consumption (mA)** **S1D13781 Active**		
Resolution	**Panel Type**	**Frame Rate**	**Clocks (MHz) Other Consideration**	**Rotation**	**LUT**	**Color Depth**	**CORE**	**PLL**	**IO**
480x272	24-bit TFT	57	CLKI = 24.0 MHz POCLK/MCLK = 60.0 MHz PCLK = MCLK / 7	0	Yes	8	4.605	0.532	3.793
		57		0	Yes	16	3.982	0.532	2.719
		57		0	Yes	24	4.815	0.532	3.794
		57		0	No	RGB888	4.605	0.532	3.793
		57		90	Yes	24	6.201	0.532	2.556
		57	CLKI = 24.0 MHz POCLK/MCLK = 60.0 MHz PCLK = MCLK / 7 2D BitBLT engine running[1]	0	Yes	24	9.689	0.532	6.333
		0	CLKI = STOPPED POCLK/MCLK = 0.0 MHz PCLK = MCLK / 7 Power Save Enabled = PSM0	0	Yes	24	0.005	0	0.071

1. This test has the 2D BitBLT engine performing a constant BitBLT writes, requires a high-level of CPU activity and a rapidly updating display.

2 Summary

The system design variables in **Error! Reference source not found.** and in the included comparison tables, show that S1D13781 power consumption depends on the specific implementation. When the S1D13781 is running, power consumption depends on the desired performance and LCD frame-rate. Power save mode consumption depends on the Clock state.

In a typical design environment, the S1D13781 can be configured to be an extremely power-efficient Simple LCD Controller with high performance and flexibility.

3 Change Record

X00A-G-008-01 Revision 1.4 - Issued: March 29, 2018

- Updated address/contact page
- Minor formatting changes

X00A-G-008-01 Revision 1.3 - Issued: February 26, 2015

- Re-format.
- Changed PSM1 mode power consumption inTable 1-1: S1D13781 Total Power Consumption for 320x240 panels and changed connective LCD panels

X94A-G-003-01 Revision 1.0 - Issued: April 06, 2011

- Re-format and edit document for release

4 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

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