READ-ONLY CONFIGURATION REGISTERS

Product Information Register
REG[00h] Default = 2Dxx402Dh Read Only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Product Code						Revision Code		n/a	CNF[6:0] Status						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Display Buffer Size								Product Code						Revision Code	

CLOCK CONFIGURATION REGISTERS

Memory Clock Configuration Register
REG[04h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a										MCLK Divide Select		n/a			BCLK Source Select

Pixel Clock Configuration Register
REG[08h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									PCLK Divide Select			n/a		PCLK Source Select	

PANEL CONFIGURATION REGISTERS

Panel Type & MOD Rate Register
REG[0Ch] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a							FPSHIFT Invert	n/a		MOD Rate					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a							HR-TFT PS Mode	Panel Data Format Select	Color/ Mono Panel Select	Panel Data Width		Reserved	n/a	Panel Type	

Display Settings Register
REG[10h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						Pixel Doubling Vertical	Pixel Doubling Horiz.	Display Blank	Dithering Disable	Display Blank Polarity	SW Video Invert	PIP+ Window Enable	n/a	SwivelView Mode Select	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a											Bits-per-pixel Select (actual value: 1, 2, 4, 8, 16 bpp)				

Power Save Configuration Register
REG[14h] Default = 00000010h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								VNDP Status (RO)	Memory Power Save Status (RO)	n/a	Power Save Enable	n/a			Reserved

LOOK-UP TABLE REGISTERS

Look-Up Table Write Register
REG[18h] Default = 00000000h Write Only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LUT Write Address								LUT Red Write Data						n/a	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LUT Green Write Data						n/a		LUT Blue Write Data						n/a	

Look-Up Table Read Register
REG[1Ch] Default = 00000000h Write Only (bits 31-24)/Read Only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LUT Read Address (write only)								LUT Red Read Data						n/a	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LUT Green Read Data						n/a		LUT Blue Read Data						n/a	

DISPLAY MODE REGISTERS

Horizontal Total Register
REG[20h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									Horizontal Total bits 6-0						

Horizontal Display Period Register
REG[24h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									Horizontal Display Period bits 6-0						

Horizontal Display Period Start Position Register
REG[28h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						Horizontal Display Period Start Position bits 9-0										

FPLINE Register
REG[2Ch] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a								FPLINE Polarity	FPLINE Pulse Width bits 6-0						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						FPLINE Pulse Start Position bits 9-0										

Vertical Total Register
REG[30h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						Vertical Total bits 9-0									

Vertical Display Period Register
REG[34h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						Vertical Display Period bits 9-0									

Vertical Display Period Start Position Register
REG[38h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						Vertical Display Period Start Position bits 9-0									

FPFRAME Register
REG[3Ch] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a								FPFRAME Polarity	n/a				FPFRAME Pulse Width bits 2-0		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						FPFRAME Pulse Start Position bits 9-0									

Main Window Display Start Address Register
REG[40h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															bit 16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Main Window Display Start Address bits 15-0															

Main Window Line Address Offset Register
REG[44h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						Main Window Line Address Offset bits 9-0									

Extended Panel Type Register
REG[48h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a							Data Compare Invert Enable	n/a				Extended Panel Type bits 3-0			

PICTURE-IN-PICTURE PLUS (PIP+) REGISTERS

PIP+ Display Start Address Register
REG[50h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															bit 16
PIP+ Window Display Start Address bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

PIP+ Window Line Address Offset Register
REG[54h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
n/a						PIP+ Window Line Address Offset bits 9-0										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

PIP+ Window X Positions Register
REG[58h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						PIP+ Window X End Position bits 9-0									
n/a						PIP+ Window X Start Position bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

PIP+ Window Y Positions Register
REG[5Ch] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						PIP+ Window Y End Position bits 9-0									
n/a						PIP+ Window Y Start Position bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

MISCELLANEOUS REGISTERS

Reserved REG[60h]								Default = 00000000h							Read/Write
n/a								Reserved							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						Reserved	Reserved	Reserved	Reserved	Reserved	n/a		Reserved	n/a	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO Status and Control Register REG[64h]								Default = 20000000h							Read/Write
GPIO7 Input Enable	GPIO6 Input Enable	GPIO5 Input Enable	GPIO4 Input Enable	GPIO3 Input Enable	GPIO2 Input Enable	GPIO1 Input Enable	GPIO0 Input Enable	GPIO7 IO Config	GPIO6 IO Config	GPIO5 IO Config	GPIO4 IO Config	GPIO3 IO Config	GPIO2 IO Config	GPIO1 IO Config	GPIO0 IO Config
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a								GPIO7 IO Control/ Status	GPIO6 IO Control/ Status	GPIO5 IO Control/ Status	GPIO4 IO Control/ Status	GPIO3 IO Control/ Status	GPIO2 IO Control/ Status	GPIO1 IO Control/ Status	GPIO0 IO Control/ Status
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPO Control Register REG[68h]								Default = 00000000h							Read/Write
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a					GPO10 Control	GPO9 Control	GPO8 Control	GPO7 Control	GPO6 Control	GPO5 Control	GPO4 Control	GPO3 Control	GPO2 Control	GPO1 Control	GPO0 Control
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Brightness (PWM) Configuration Register REG[70h]								Default = 00000000h							Read/Write
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a								PWM Clock Divide Select bits 3-0				PWM Clock Force High	PWMCLK Source Select bits 1-0		PWM Clock Enable
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Brightness (PWM) Duty Cycle Register REG[74h]								Default = 00000000h							Read/Write
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a								PWMOUT Duty Cycle bits 7-0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Scratch Pad A Register REG[80h]								Default = not applicable							Read/Write
Scratch Pad A bits 31-24															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Scratch Pad A bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Scratch Pad B Register REG[84h]								Default = not applicable							Read/Write
Scratch Pad B bits 31-24															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Scratch Pad B bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Scratch Pad C Register REG[88h]								Default = not applicable							Read/Write
Scratch Pad C bits 31-24															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Scratch Pad C bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

EXTENDED PANEL REGISTERS

HR-TFT Mode 2 CLS Width Register
REG[A0h] Default = 0000012Ch Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a							CLS Pulse Width bits 8-0								

HR-TFT Mode 2 PS1 Rising Edge Register
REG[A4h] Default = 00000032h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a										PS1 Rising Edge bits 5-0					

HR-TFT Mode 2 PS2 Rising Edge Register
REG[A8h] Default = 00000064h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								PS2 Rising Edge bits 7-0							

HR-TFT Mode 2 PS2 Toggle Width Register
REG[ACh] Default = 0000000Ah Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									PS2 Toggle Width bits 6-0						

HR-TFT Mode 2 PS3 Signal Width Register
REG[B0h] Default = 00000064h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									PS3 Signal Width bits 6-0						

HR-TFT Mode 2 REV Toggle Point Register
REG[B4h] Default = 0000000Ah Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a											REV Toggle Point bits 4-0				

HR-TFT Mode 2 PS1/2 End Register
REG[B8h] Default = 00000007h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a													PS1/2 End bits 7-0		

Type 2 TFT Configuration Register
REG[BCh] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POL Type	n/a	AP Pulse Width bits 2-0			n/a	AP Rising Position bits1-0		n/a			VCLK Hold bits 1-0		n/a	VCLK Setup bits 1-0	

Casio TFT Timing Register
REG[C0h] Default = 09180E09h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a		GPCK Rising Edge to STH Pulse bits 5-0						n/a	GRES Falling Edge to FRP Toggle Point bits 6-0						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a		GRES Falling Edge to GPCK Rising Edge bits 5-0						n/a		GPCK Rising Edge to GRES Rising Edge bits 5-0					

Type 3 TFT Configuration Register 0
REG[D8h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POL Toggle Position bits 7-0								OE Pulse Width bits 7-0							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OE Rising Edge Position bits 7-0								n/a							

Type 3 TFT Configuration Register 1
REG[DCh] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
XOEV Falling Edge Position bits 7-0								XOEV Rising Edge Position bits 7-0							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPV Pulse Width bits 7-0								VCOM Toggle Position bits 7-0							

Type 3 TFT PCLK Divide Register
REG[E0h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a										PCLK2 Divide Rate bits 1-0		PCLK1 Divide Rate bits 3-0			

Type 3 TFT Partial Mode Display Area Control Register
REG[E4h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a		Partial Mode Display Refresh Cycle bits 5-0						n/a			Partial Mode Display Enable	Partial Mode Display Type Select	Area 2 Display Enable	Area 1 Display Enable	Area 0 Display Enable

Type 3 TFT Partial Area 0 Positions Register
REG[E8h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a		Partial Area 0 Y End Position bits 5-0						n/a		Partial Area 0 X End Position bits 5-0					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a		Partial Area 0 Y Start Position bits 5-0						n/a		Partial Area 0 X Start Position bits 5-0					

Type 3 TFT Partial Area 1 Positions Register
REG[ECh] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a		Partial Area 1 Y End Position bits 5-0						n/a		Partial Area 1 X End Position bits 5-0					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a		Partial Area 1 Y Start Position bits 5-0						n/a		Partial Area 1 X Start Position bits 5-0					

Type 3 TFT Partial Area 2 Positions Register
REG[F0h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a		Partial Area 2 Y End Position bits 5-0						n/a		Partial Area 2 X End Position bits 5-0					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a		Partial Area 2 Y Start Position bits 5-0						n/a		Partial Area 2 X Start Position bits 5-0					

Type 3 TFT Command Store Register
REG[F4h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a				Command 1 Store bits 11-0											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a				Command 0 Store bits 11-0											

Type 3 TFT Miscellaneous Register
REG[F8h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						Source Driver IC Number bits 1-0		n/a							Command Send Request

USB REGISTERS

Control Register
REG[4000h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								USBClk Enable	Software EOT	USB Enable	Endpoint 4 Stall	Endpoint 3 Stall	USB Setup	Reserved	Reserved

Interrupt Enable Register 0
REG[4002h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Suspend Request Interrupt Enable	SOF Interrupt Enable	Reserved	Endpoint 4 Interrupt Enable	Endpoint 3 Interrupt Enable	Endpoint 2 Interrupt Enable	Endpoint 1 Interrupt Enable	n/a

Interrupt Status Register 0
REG[4004h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Suspend Request Interrupt Status	SOF Interrupt Status	Reserved	Endpoint 4 Interrupt Status	Endpoint 3 Interrupt Status	Endpoint 2 Interrupt Status	Endpoint 1 Interrupt Status	Upper Interrupt Active (read only)

Interrupt Enable Register 1
REG[4006h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a														Transmit FIFO Almost Empty Interrupt Enable	Receive FIFO Almost Full Interrupt Enable

Interrupt Status Register 1
REG[4008h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a														Transmit FIFO Almost Empty Status	Receive FIFO Almost Full Status

Endpoint 1 Index Register
REG[4010h] Default = 00h Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a													Endpoint 1 Index bits 2-0		

Endpoint 1 Receive Mailbox Data Register
REG[4012h] Default = 00h Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Endpoint 1 Receive Mailbox Data bits 7-0							

Endpoint 2 Index Register
REG[4018h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a													Endpoint 2 Index bits 2-0		

Endpoint 2 Transmit Mailbox Data Register
REG[401Ah] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Endpoint 2 Transmit Mailbox Data bits 7-0							

Endpoint 2 Interrupt Polling Interval Register
REG[401Ch] Default = FFh Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Endpoint 2 Interrupt Polling Interval bits 7-0							

Endpoint 3 Receive FIFO Data Register
REG[4020h] Default = 00h Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Endpoint 3 Receive FIFO Data bits 7-0							

Endpoint 3 Receive FIFO Count Register
REG[4022h] Default = 00h Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Endpoint 3 Receive FIFO Count bits 7-0							

Endpoint 3 Receive FIFO Status Register
REG[4024h] Default = 01h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a											Receive FIFO Flush	Receive FIFO Overflow	Receive FIFO Underflow	Receive FIFO Full (read only)	Receive FIFO Empty (read only)

Endpoint 3 Maximum Packet Size Register
REG[4026h] Default = 08h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Endpoint 3 Max Packet Size bits 7-0							

Endpoint 4 Transmit FIFO Data Register
REG[4028h] Default = 00h Write Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Endpoint 4 Transmit FIFO Data bits 7-0							

Endpoint 4 Transmit FIFO Count Register
REG[402Ah] Default = 00h Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Endpoint 4 Transmit FIFO Count bits 7-0							

Endpoint 4 Transmit FIFO Status Register
REG[402Ch] Default = 01h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a										Transmit FIFO Valid	Transmit FIFO Flush	Transmit FIFO Overflow	Reserved	Transmit FIFO Full (read only)	Transmit FIFO Empty (read only)

Endpoint 4 Maximum Packet Size Register
REG[402Eh] Default = 08h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Endpoint 4 Max Packet Size bits 7-0							

Revision Register
REG[4030h] Default = 01h Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Chip Revision bits 7-0							

USB Status Register
REG[4032h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Suspend Control	USB Endpoint 4 STALL	USB Endpoint 4 NAK	USB Endpoint 4 ACK	USB Endpoint 3 STALL	USB Endpoint 3 NAK	USB Endpoint 3 ACK	Endpoint 2 Valid

Frame Counter MSB Register
REG[4034h] Default = 00h Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a													Frame Counter bits 10-8		

Frame Counter LSB Register
REG[4036h] Default = 00h Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Frame Counter bits 7-0							

Extended Register Index
REG[4038h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Extended Register Index bits 7-0							

Extended Register Data
REG[403Ah] Default = 04h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Extended Register Data bits 7-0							

Vendor ID MSB
REG[403Ah], Index[00h] Default = 04h Read/Write

7	6	5	4	3	2	1	0
Vendor ID bits 15-8							

Vendor ID LSB
REG[403Ah], Index[01h] Default = B8h Read/Write

7	6	5	4	3	2	1	0
Vendor ID bits 7-0							

Product ID MSB
REG[403Ah], Index[02h] Default = 88h Read/Write

7	6	5	4	3	2	1	0
Product ID bits 15-8							

Product ID LSB
REG[403Ah], Index[03h] Default = 21h Read/Write

7	6	5	4	3	2	1	0
Product ID bits 7-0							

Release Number MSB
REG[403Ah], Index[04h] Default = 01h Read/Write

7	6	5	4	3	2	1	0
Release Number bits 15-8							

Release Number LSB
REG[403Ah], Index[05h] Default = 00h Read/Write

7	6	5	4	3	2	1	0
Release Number bits 7-0							

Receive FIFO Almost Full Threshold
REG[403Ah], Index[06h] Default = 3Ch Read/Write

7	6	5	4	3	2	1	0
n/a		Receive FIFO Almost Full Threshold bits 5-0					

Transmit FIFO Almost Empty Threshold
REG[403Ah], Index[07h] Default = 04h Read/Write

7	6	5	4	3	2	1	0
n/a		Transmit FIFO Almost Empty Threshold bits 5-0					

USB Control
REG[403Ah], Index[08h] Default = 01h Read/Write

7	6	5	4	3	2	1	0
n/a							USB String Enable

Maximum Power Consumption
REG[403Ah], Index[09h] Default = FAh Read/Write

7	6	5	4	3	2	1	0
Maximum Current bits 7-0							

Packet Control
REG[403Ah], Index[0Ah] Default = 00h Read/Write

7	6	5	4	3	2	1	0
EP4 Data Toggle	EP3 Data Toggle	EP2 Data Toggle	EP1 Data Toggle	Reserved	Reserved	n/a	Reserved

Reserved
REG[403Ah], Index[0Bh] Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a							Reserved

FIFO Control
REG[403Ah], Index[0Ch] Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a							Transmit FIFO Valid Mode

USBFC Input Control Register
REG[4040h] Default = 0Dh Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									USCMPEN	Reserved	Reserved	ISO	WAKEUP	Reserved	Reserved

Reserved
REG[4042h] Default = 1Dh Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a											Reserved				

Pin Input Status / Pin Output Data Register
REG[4044h] Default = depends on USB input pin state Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a														USBDETECT Input Pin Status (read only)	USBPUP Output Pin Status

Interrupt Control Enable Register 0
REG[4046h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									USB Host Connected	Reserved	Reserved	Reserved	Reserved	USBRESET	Reserved

Interrupt Control Enable Register 1
REG[4048h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									USB Host Disconnect	Reserved	Device Configured	Reserved	Reserved	Reserved	INT

Interrupt Control Status/Clear Register 0
REG[404Ah] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									USB Host Connected	Reserved	Reserved	Reserved	Reserved	USBRESET	Reserved

Interrupt Control Status/Clear Register 1
REG[404Ch] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									USB Host Disconnect	Reserved	Device Configured	Reserved	Reserved	Reserved	INT

Interrupt Control Masked Status Register 0
REG[404Eh] Default = 00h Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									USB Host Connected	Reserved	Reserved	Reserved	Reserved	USBRESET	Reserved

Interrupt Control Masked Status Register 1
REG[4050h] Default = 00h Read Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									USB Host Disconnect	Reserved	Device Configured	Reserved	Reserved	Reserved	INT

USB Software Reset Register
REG[4052h] Default = 00h Write Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								USB Software Reset (Code = 10100100) bits 7-0							

USB Wait State Register
REG[4054h] Default = 00h Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								n/a						USB Wait State bits 1-0	

2D ACCELERATION (BitBLT) REGISTERS

BitBLT Control Register
REG[8000h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a													Color Format Select	Dest Linear Select	Source Linear Select
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a															BitBLT Enable (WO)

BitBLT Status Register
REG[8004h] Default = 00000000h Read Only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a			Number of Used FIFO Entries					n/a		Number of Free FIFO Entries (0 means full)					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a									FIFO Not Empty	FIFO Half Full	FIFO Full Status	n/a			BitBLT Busy Status

BitBLT Command Register
REG[8008h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a												BitBLT ROP Code bits 3-0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a												BitBLT Operation bits 3-0			

BitBLT Source Start Address Register
REG[800Ch] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a											BitBLT Source Start Address bits 20-16				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BitBLT Source Start Address bits 15-0															

BitBLT Destination Start Address Register
REG[8010h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a											BitBLT Destination Start Address bits 20-16				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BitBLT Destination Start Address bits 15-0															

BitBLT Memory Address Offset Register
REG[8014h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a					BitBLT Memory Address Offset bits 10-0										

BitBLT Width Register
REG[8018h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						BitBLT Width bits 9-0									

BitBLT Height Register
REG[801Ch] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						BitBLT Height bits 9-0									

BitBLT Background Color Register
REG[8020h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BitBLT Background Color bits 15-0															

BitBLT Foreground Color Register
REG[8024h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BitBLT Foreground Color bits 15-0															

2D Accelerator (BitBLT) Data Memory Mapped Region Register
AB16-AB0 = 10000h-1FFFEh, even addressesRead/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BitBLT Data bits 31-16															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BitBLT Data bits 15-0															