

**S1D13L01 Display Controller**

# **S5U13L01P00C100 Evaluation Board User Manual**

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## Chapter 1 Introduction

This manual describes the setup and operation of the S5U13L01P00C100 Evaluation Board. The evaluation board is designed as an evaluation platform for the S5U13L01 Display Controller.

The S5U13L01P00C100 evaluation board can also connect to the S5U13U00P00C100 USB Adapter board so that it can be used with a laptop or desktop computer, via USB 2.0. The S5U13L01P00C100 evaluation board can be used with many native platforms via the host connector which provides the appropriate signals to support a variety of CPUs. However, if you do not use the S5U13U00P00C100 USB Adapter board, there is prepare the land for the other host interface. Please use the land to host interface.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at [vdc.epson.com](http://vdc.epson.com).

We appreciate your comments on our documentation. Please contact us via email at [vdc-documentation@ea.epson.com](mailto:vdc-documentation@ea.epson.com).

# Chapter 2 Features

The S5U13L01P00C100 Evaluation Board includes the following features:

- QFP 128pin S1D13L01F00A100 Display Controller
- Headers for connection to the S5U13U00P00C100 USB Adapter board

### Note

The SPI interface is not available when the S5U13L01P00C100 evaluation board is used with the S5U13U00P00C100 USB adapter board.

- Headers for connection to various host interface

### Note

These headers are not mounted. There is only land.

- Headers for connection to various LCD panels
- On-board 24MHz crystal (EPSON SG-210)
- On-board voltage regulator with 1.5V output, for CORE/PLLVDD
- On-board voltage regulator with adjustable 1.5~3.8V output, for IOVDD
- On-board voltage regulator with 3.3V output, for on-board OSC
- On-board voltage regulator with adjustable 38V/60mA max, to provide power for LED back-light of LCD panels.

## Chapter 3 Installation and Configuration

The S5U13L01P00C100 evaluation board incorporates a DIP switch, jumpers, and 0 ohm resistors which allow it to be used with a variety of different configurations.

### 3.1 CNF[2:0] Configuration

The S1D13L01 has 3 configuration inputs CNF[2:0], which are used to configure the S1D13L01 host interface type through DIP switch SW1. Depending on the CNF[2:0] setting, some host interface pins will not be used. Those pins should be terminated by SW2 and SW3.

Table 3-1: Host Interface Pin Mapping

S1D13L01 Pin Name	Direct 16-bit Mode 1	Direct 16-bit Mode 2	Indirect 16-bit Mode 1	Indirect 16-bit Mode 2	Direct 8-bit	Indirect 8-bit	SPI
CNF[2:0]	000	001	010	011	100	101	111
CS#	CS#	CS#	CS#	CS#	CS#	CS#	CS#
WR#	WR#	RDU#	WR#	RDU#	WR#	WR#	SCK
RD#	RD#	RDL#	RD#	RDL#	RD#	RD#	SW2-3=On
UB#	UB#	WRU#	UB#	WRU#	SW2-1=On	SW2-1=On	SW2-1=On
LB#	LB#	WRL#	LB#	WRL#	SW2-2=On	SW2-2=On	SW2-2=On
AB0	TE (JP108 2-3)	TE (JP108 2-3)	TE (JP108 2-3)	TE (JP108 2-3)	AB0	TE (JP108 2-3)	TE (JP108 2-3)
AB1	AB1	AB1	P/C#	P/C#	AB1	P/C#	Low
AB[18:2]	AB[18:2]	AB[18:2]	Low	Low	AB[18:2]	Low	Low
DB0	DB0	DB0	DB0	DB0	DB0	DB0	SI
DB1	DB1	DB1	DB1	DB1	DB1	DB1	SO
DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	SW2-5~10=On
DB8	DB8	DB8	DB8	DB8	TE (JP108 3-4)	SW3-1=On	SW3-1=On
DB[15:9]	DB[15:9]	DB[15:9]	DB[15:9]	DB[15:9]	SW3-2~8=On	SW3-2~8=On	SW3-2~8=On

#### Note


1. For SW2~3, the setting must be Off if there is no suggestion in table.
2. For JP105~109, the setting must be 1-2 if there is no suggestion in table.
3. Low means internal pull-down for address bus active.
4. The SPI interface is not available when the S5U13L01P00C100 evaluation board is used with the S5U13U00P00C100 USB adapter board.

## 3.2 Configuration Switches

The S5U13L01P00C100 evaluation board includes the following switch blocks which control the functions described in Table 3-2: “Switch Settings”. For jumper locations on the evaluation board, see Figure 3-1: “Configuration Switch and Jumper Locations (Red)” on page 10.

Table 3-2: Switch Settings

Switch	bit	On	Off	Comment
SW1	1	CNF0 is Pull Up (1)	CNF0 is Pull Down (0)	CNF[2:0] configuration. See Table 3-1: “Host Interface Pin Mapping”
	2	CNF1 is Pull Up (1)	CNF1 is Pull Down (0)	
	3	CNF2 is Pull Up (1)	CNF2 is Pull Down (0)	
	4	not used	not used	
SW2	1	UB# is Pull Up	UB# is not tied	Host interface pin termination when not used pin. See Table 3-1: “Host Interface Pin Mapping”
	2	LB# is Pull Up	LB# is not tied	
	3	RD# is Pull Up	RD# is not tied	
	4	not used	not used	
	5	DB2 is Pull Down	DB2 is not tied	
	6	DB3 is Pull Down	DB3 is not tied	
	7	DB4 is Pull Down	DB4 is not tied	
	8	DB5 is Pull Down	DB5 is not tied	
	9	DB6 is Pull Down	DB6 is not tied	
	10	DB7 is Pull Down	DB7 is not tied	
SW3	1	DB8 is Pull Down	DB8 is not tied	
	2	DB9 is Pull Down	DB9 is not tied	
	3	DB10 is Pull Down	DB10 is not tied	
	4	DB11 is Pull Down	DB11 is not tied	
	5	DB12 is Pull Down	DB12 is not tied	
	6	DB13 is Pull Down	DB13 is not tied	
	7	DB14 is Pull Down	DB14 is not tied	
	8	DB15 is Pull Down	DB15 is not tied	

 = suggested settings



### 3.3 Configuration Jumpers

The S5U13L01P00C100 evaluation board includes the following 2-pin, 3-pin, 5-pin and 8-pin jumper blocks which control the functions described in Table 3-3: “2-Pin Jumper Settings”, Table 3-4: “3-Pin Jumper Settings”, Table 3-5: “5-Pin Jumper Settings” and Table 3-6: “8-Pin Jumper Setting”. For jumper locations on the evaluation board, see Figure 3-1: “Configuration Switch and Jumper Locations (Red)” on page 10.

Table 3-3: 2-Pin Jumper Settings

Jumper	Position 1-2	No Jumper (Open)
JP101	Connect COREVDD Power Supply	Connect a current meter for power measurement
JP102 <small>NOTE</small>	Connect IOVDD Power Supply to S5U13U00P00C100	No IOVDD Power Supply to S5U13U00P00C100
JP104	Connect PLLVDD Power Supply	Connect a current meter for power measurement

= suggested settings

**Note**

For normal S5U13L01P00C100 operation, JP102 should be in Position 1-2. Also, when using the S5U13L01P00C100 with the S5U13U00P00C100, JP102 should be in Position 1-2 (JP1 on the S5U13U00P00C100 must be in Position 1-2). For IOVDD current measurement, JP102 should be removed.

Table 3-4: 3-Pin Jumper Settings

Jumper	Position 1-2	Position 2-3	Off
JP105	WR# is from P1 and CN3	WR# is from P2	WR# is not connected
JP106	DB0 is from P1 and CN3	DB0 is from P2	DB0 is not connected
JP107	DB1 is from P1 and CN3	DB1 is from P2	DB1 is not connected

= suggested settings

Table 3-5: 5-Pin Jumper Settings

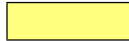
Jumper	Position		Function
JP108	Position 1-2	Position 2-3	Position 1-2: AB0 is AB0 (only for Direct 8bit mode) Position 2-3: AB0 is TE
	Position 3-4	Position 4-5	Position 3-4: DB8 is TE (only for Direct 8bit mode) Position 4-5: DB8 is DB8

= suggested settings

# Installation and Configuration

Table 3-6: 8-Pin Jumper Setting

Jumper	Position		Function
JP503	Position 1-2	No Jumper	In connect case, TPS61161A is Enable
	Position 3-4	No Jumper	In connect case, Vout = 20mA
	Position 5-6	No Jumper	In connect case, Vout = 40mA (add connect Position 3-4)
	Position 7-8	No Jumper	In connect case, Vout = 60mA (add connect Position3-4 and Position5-6)

 = suggested settings

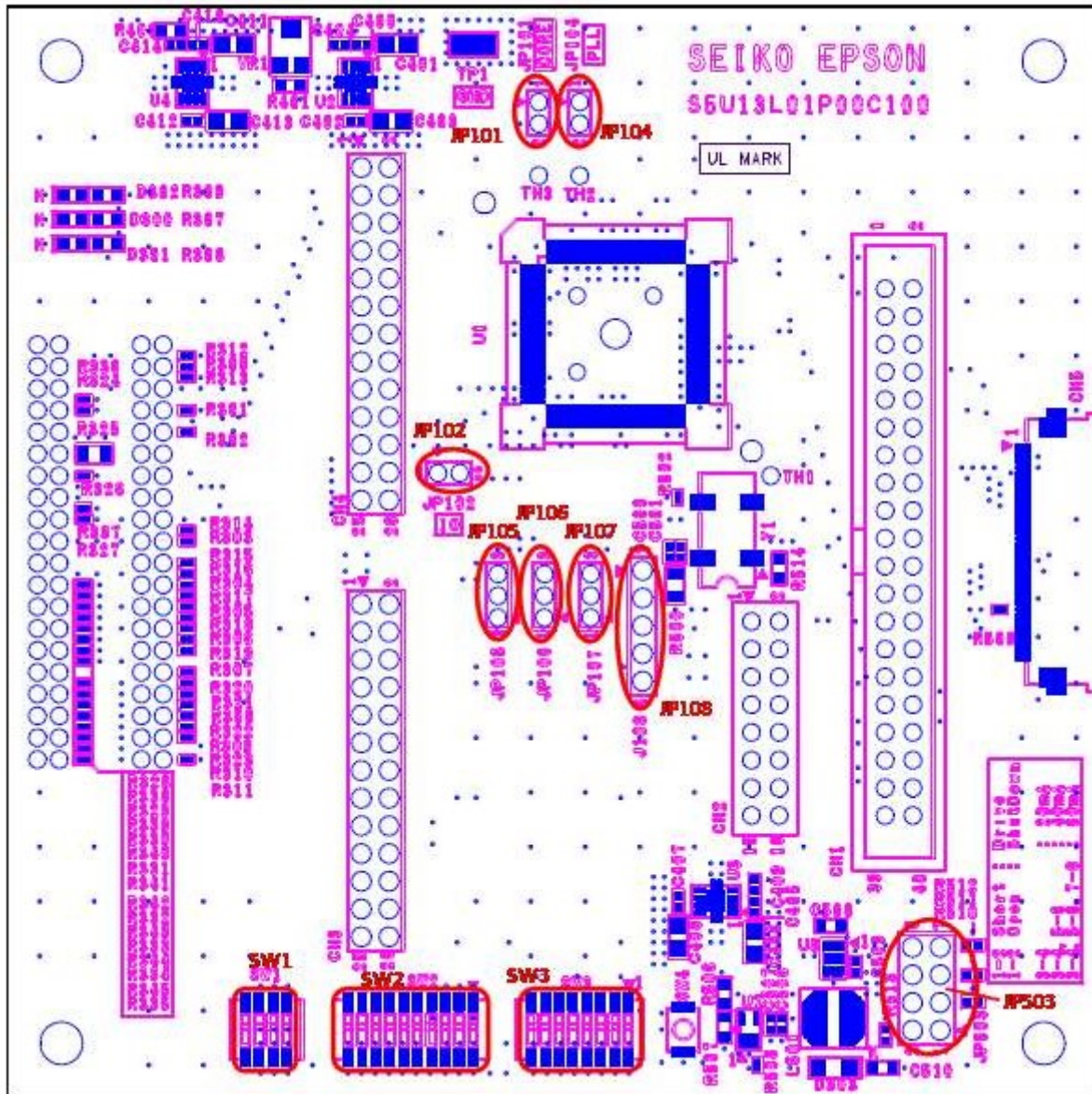


Figure 3-1: Configuration Switch and Jumper Locations (Red)

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## 3.4 Zero Ohm Resistor Configuration

Between the S5U13U00P00C100 connector (P1, P2) and the S1D13L01 there are zero ohm resistors.

## 3.5 Power Requirements

### 3.5.1 IOVDD, COREVDD, PLLVDD

The S5U13L01P00C100 evaluation board is designed to generate COREVDD, PLLVDD and IOVDD from 5V via the S5U13U00P00C100 USB adapter board or connector CN4. Since PLLVDD and COREVDD must be same, these two voltages are generated by one voltage regulator, separated by an inductance. 5V must be supplied from the S5U13U00P00C100 or CN4. IOVDD for the S5U13U00P00C100 should be supplied from the S5U13L01P00C100 (both JP102 on the S5U13L01P00C100 evaluation board and JP1 on the S5U13U00P00C100 USB adapter board should be set to position 1-2). These power supplies are adjustable. See Table 3-7: “S5U13L01P00C100 Power Mapping” for detail.

**Note**

Connector CN4 is only land.

### 3.5.2 3.3V

The S5U13L01P00C100 evaluation board is designed to generate 3.3V for on board OSC from 5V via the S5U13U00P00C100 USB adapter board or connector CN4. 5V must be supplied from the S5U13U00P00C100 or CN4. The 3.3V power supply is fixed output. See Table 3-7: “S5U13L01P00C100 Power Mapping” for detail.

**Note**

Connector CN4 is only land.

### 3.5.3 Backlight Power Supply for LCD Panel

The S5U13L01P00C100 evaluation board is designed to generate backlight power supply for LCD panel from 5V via the S5U13U00P00C100 USB adapter board or connector CN4. The 5V must be supplied from the S5U13U00P00C100 or CN4. This power supply is adjustable. It is possible to change the current value by the connection of JP503. See Table 3-6: “8-PinJumper Setting” and Table 3-7: “S5U13L01P00C100 Power Mapping”for detail.

**Note**

Connector CN4 is only land.

Table 3-7: S5U13L01P00C100 Power Mapping

Name	Purpose	Adj.	Range
COREVDD	S1D13L01 COREVDD 1.5V Fixed	—	1.5V
PLLVDD	S1D13L01 PLLVDD 1.5V Fixed		
IOVDD\	S1D13L01 IOVDD 1.8/3.3V Typical	VR1	1.5~3.8V
3.3V	SG-210 VDD 3.3V Fixed	—	3.3V
LED+	Backlight for panel, 38V/60mA max	JP503	12~38V

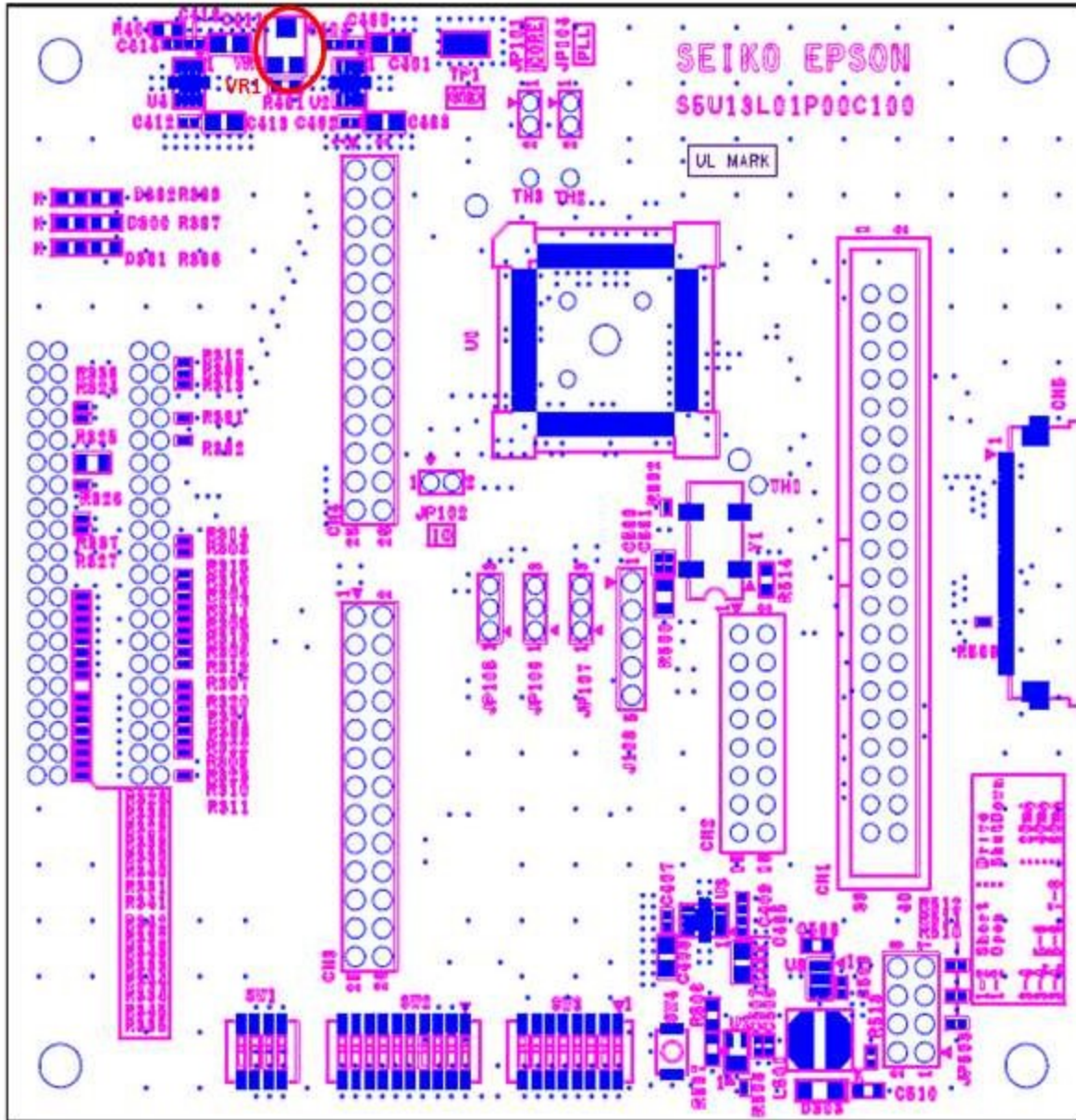


Figure 3-2: Voltage Adjustment Locations (Red)

### 3.6 LED Status Indicators

The S5U13L01P00C100 evaluation board has 3 LED status indicators which provide a quick visual status of the following conditions as described in Table 3-8: “LED Status Indicators”.

**Note**

Connector CN4 is only land.

Table 3-8: LED Status Indicators

LED	Color	Signal	Comment
HB	RED	HEARTBEAT	HEARTBEAT from the S5U13U00P00C100
ENUM	RED	ENUMARETED	ENUMARETED from the S5U13U00P00C100
POWER	RED	5V	5.0V is present from the S5U13U00P00C100 or CN4

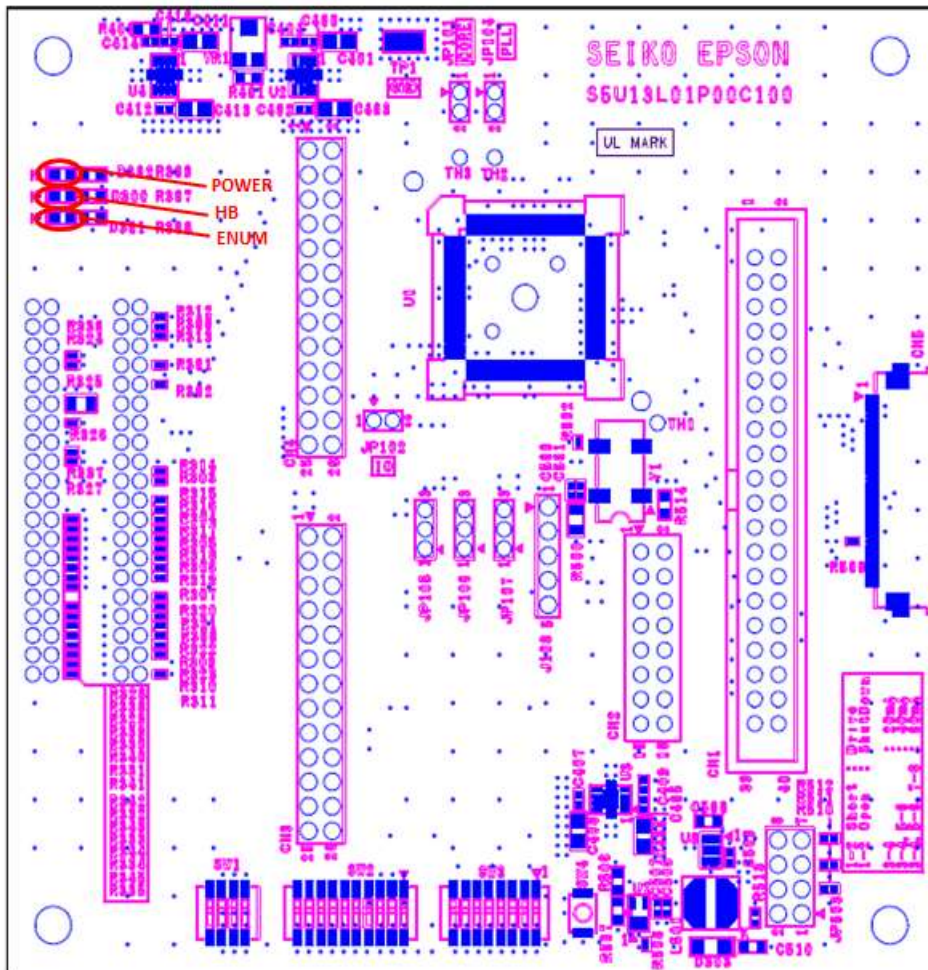


Figure 3-3: LED Locations (Red)

# Chapter 4 Connectors

## 4.1 CN1, CN2, CN5 Panel Interface Connector

The LCD interface uses the VS, HS, DE, PCLK and PDT[23:0] pins. All signals on these pins are available on connectors CN1, CN2 and CN5.

Connectors CN1 and CN2 and CN5 are 0.1" x 0.1", 40-pin headers (20 x 2) for CN1, 16-pin headers (8 x 2) for CN2, 0.5mm pitch, 40-pin FPC Connector for CN5. See Figure 4-1: "Host and Panel Bus Connector Location (CN1, CN2, CN3, CN4, CN5)" on page 15 for the location of these connectors. For the pinout of connectors CN1, CN2 and CN5, see Section Chapter 7, "Schematic Diagrams" on page 23.

### Note

Connector CN1 and CN2 are only land.

## 4.2 CN3, CN4 Host Bus Interface Connector

All S1D13L01 host interface pins are available on connectors CN3 and CN4. This allows the S5U13L01P00C100 evaluation board to be connected to a variety of development platforms. For S1D13L01 host interface pin mapping, see Table 3-1: "Host Interface Pin Mapping," on page 7.

See Figure 4-1: "Host and Panel Bus Connector Location (CN1, CN2, CN3, CN4, CN5)" on page 15 for the location of host bus connectors CN3 and CN4. CN3 and CN4 are 0.1" x 0.1" 26-pin header (13x2). For the pinout of connectors CN3 and CN4, see Section Chapter 7, "Schematic Diagrams" on page 23.

### Note

Connector CN3 and CN4 are only land.

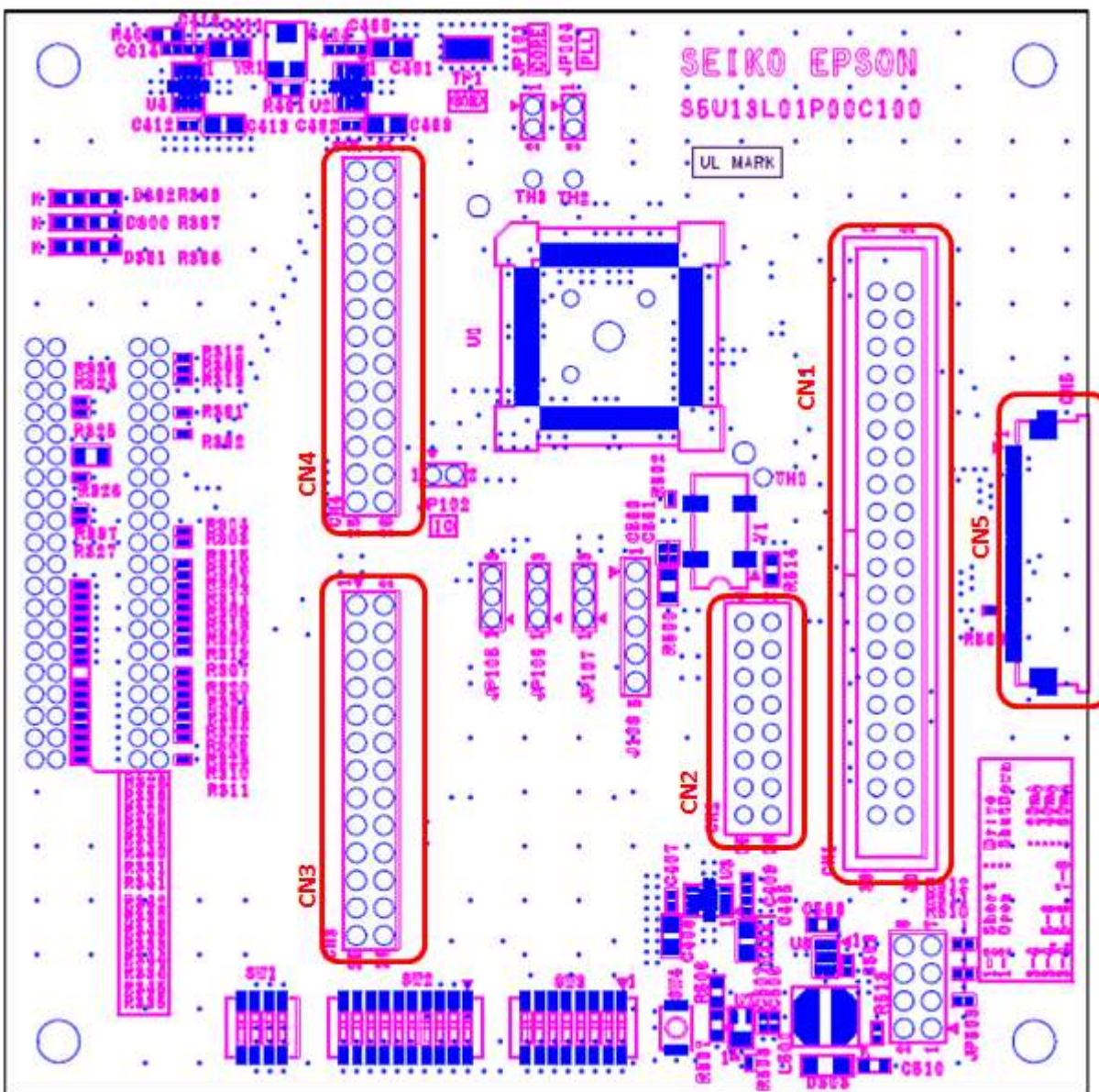


Figure 4-1: Host and Panel Bus Connector Location (CN1, CN2, CN3, CN4, CN5)

### 4.3 P1, P2 Connecting to the Epson S5U13U00P00C100 USB Adapter Board

The S5U13L01P00C100 evaluation board is designed to connect to a S5U13U00P00C100 USB Adapter Board. The USB adapter board provides a simple connection to any computer via a USB 2.0 connection. The S5U13L01P00C100 directly connects to the USB adapter board through connectors P1 and P2.

#### **Note**

The SPI interface is not available when the S5U13L01P00C100 evaluation board is used with the S5U13U00P00C100 USB adapter board.

The S5U13U00P00C100 USB adapter board supplies the 5V power required by the S5U13L01P00C100 evaluation board. The S5U13L01P00C100 evaluation board then supplies the IOVDD for the S5U13U00P00C100 USB adapter board. Therefore, both JP102 on the S5U13L01P00C100 evaluation board and JP1 on the S5U13U00P00C100 USB adapter board should be set to position 1-2.

When the S5U13L01P00C100 is connected to the S5U13U00P00C100 USB Adapter board, there are 2 LEDs on the S5U13L01P00C100 which provide a quick visual status of the USB adapter. HB (D300) blinks to indicate that the USB adapter board is active. ENUM (D301) turns on to indicate that the USB has been enumerated by the PC.



The following diagram shows the location of connectors P1 and P2. P1 and P2 are 2mm x 2mm, 40-pin headers (20 x 2) located on the underside of the board.

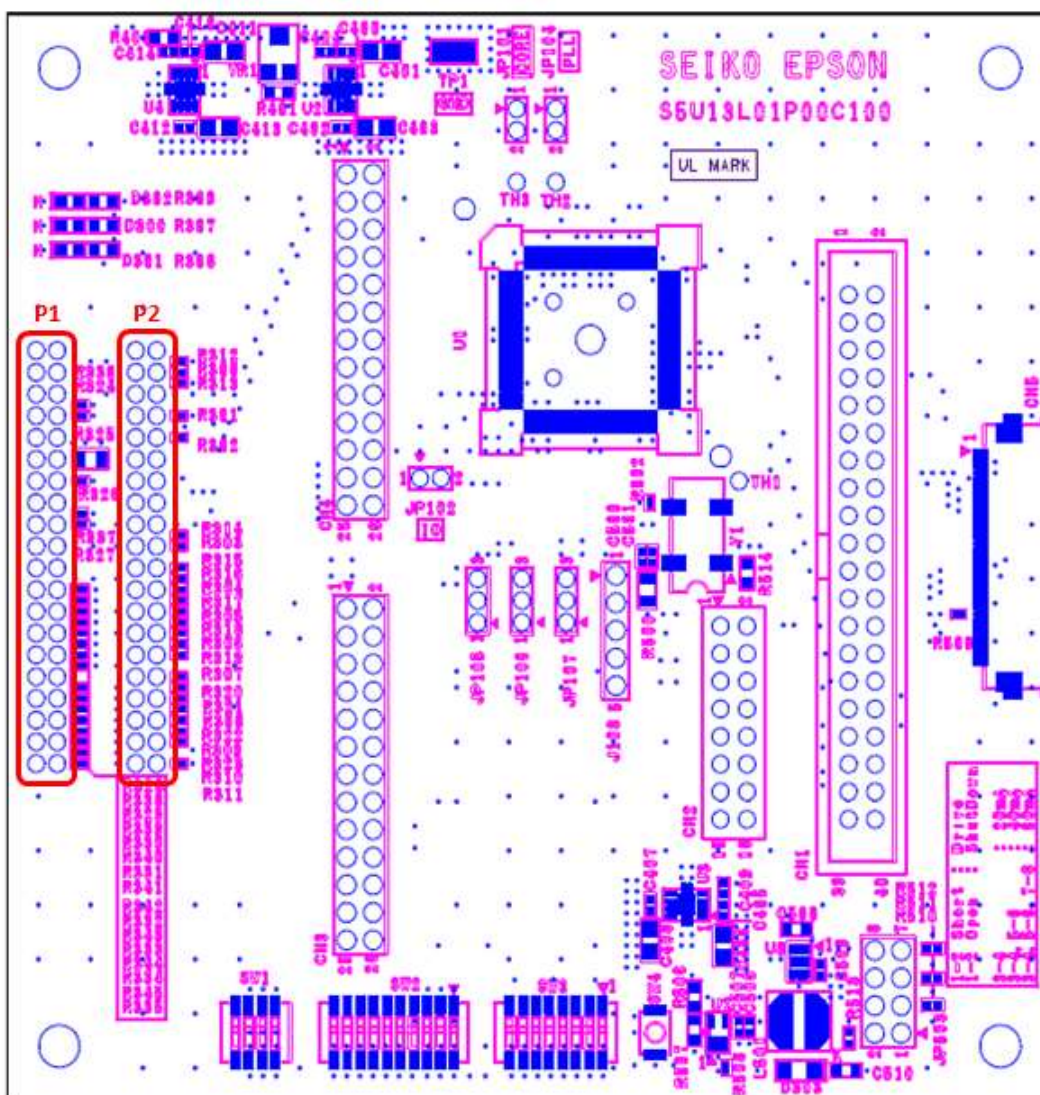


Figure 4-2: USB Adapter Connector Locations (P1, P2)

For the pinout of connectors P1 and P2, see Section Chapter 7, “Schematic Diagrams” on page 23.

**Note**

A windows driver must be installed on the PC when the S5U13L01P00C100 is used with the S5U13U00P00C100 USB Adapter Board. The S1D13xxxUSB driver is available at [vdc.epson.com](http://vdc.epson.com).

# Chapter 5 Technical Description

## 5.1 Current Measurement

Current measurement can be performed individually for the following S1D13L01 power supplies: COREVDD, PLLVDD, IOVDD. For a details on which jumper block is used for each power supply, refer to Table 3-3: “2-Pin Jumper Settings,” on page 9.

To measure current for a particular S1D13L01 power supply, remove the corresponding jumper shunt and place an ammeter on the jumper terminals to measure the current draw. Use the lowest possible range for the measurement to minimize loading from the ammeter.

For IOVDD current measurement, shunts for JP102 should be removed and an ammeter connected across JP102. JP1 on S5U13U00P00C100 must be set to position 2-3.

### Note

Attaching an ammeter while doing other tests can cause a voltage drop across the ammeter and may produce invalid test results.

## 5.2 Oscillator Support for CLKI input

The S5U13L01P00C100 evaluation board has an on-board 24MHz oscillator (Y1) which drives the input for the S1D13L01 CLKI pin.



## Chapter 6 Parts List

Table 6-1 : S5U13L01P00C100 Parts List

Item	Qty	Reference	Part	Description	Manufacture Part No. / Comments
1	1	U1	S1D13L01	LCD Controller QFP15-128 0.5mm Pitch	EPSON S1D13L01F
2	1	U2	TPS73615DRB	Single Channel LDO Fixed	TI TPS73615DRB
3	1	U3	TPS73633DRB	Single Channel LDO Fixed	TI TPS73633DRB
4	1	U4	TPS73601DRB	Single Channel LDO Adjustable	TI TPS73601DRB
5	1	U7	TPS3801-01DCKR	SUPPLY VOLTAGE SUPERVISORS Vref 1.14V Delay 200ms	TI TPS3801-01DCKR
6	1	U8	TPS61161ADRVT	White LED Driver with Digital and PWM Brightness Control	TI TPS61161ADRVT
7	1	C123	GRM155B11H 102KA01D	cap 1000p 1005	MURATA
8	3	C404, C409, C414	GRM155B11E103KA0 1D	cap 10n 1005	MURATA
9	12	C102, C104, C106, C108, C110, C112, C114, C116, C118, C120, C501, C507	GRM155B11E103KA0 1D	cap 0.01u 1005	MURATA
10	20	C101, C103, C105, C107, C109, C111, C113, C115, C117, C119, C121, C400, C402, C405, C407, C410, C412, C500, C506, C509	GRM155R71C104KA8 8D	cap 0.1u 1005	MURATA
11	7	C122, C401, C403, C406, C408, C411, C413	GRM21BB31C106KE 15L	cap 10u 16v 2012	MURATA
12	1	C508		cap 0.22u/50V	
13	1	C510		cap 1.0u/50V	

Table 6-1 : S5U13L01P00C100 Parts List

Item	Qty	Reference	Part	Description	Manufacture Part No. / Comments
14	46	R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R310, R311, R312, R314, R315, R316, R317, R318, R319, R320, R321, R322, R323, R324, R326, R327, R328, R329, R330, R331, R332, R333, R334, R335, R336, R337, R338, R339, R340, R341, R342, R343, R344, R345, R508, R509	ERJ-1GE0R00C	res 0 0603	Panasonic
15	2	R325, R500	RK73Z2ATTD	res 0 2012	KOA
16	2	R367, R368	RK73B1JTDD 331J	res 330 1608	KOA
17	1	R369	RK73B1JTDD 621J	res 620 1608	KOA
18	20	R101, R102, R103, R350, R351, R352, R353, R354, R355, R356, R357, R358, R359, R360, R361, R362, R363, R364, R365, R366	ERJ-1GEJ102C	res 1k 0603	Panasonic
19	1	R401	RK73B1JTDD 223J	res 22k 1608	KOA
20	4	R104, R105, R106, R400	RK73B1JTDD 473J	res 47k 1608	KOA
21	1	R502	MCR006YZPF33R0	res 33 1% 0603	ROHM
22	1	R506	RK73H1JTDD 5621F	res 5.62k 1% 1608	KOA
23	1	R507	RK73H1JTDD 4532F	res 45.3k 1% 1608	KOA
24	1	R313	NM	res NM 0603	not mounted
25	3	R510, R511, R512		res 10	
26	1	R513		res 10k	
27	1	VR1	ST32ETA204	SMD Trimming Potentiometer 200k	COPAL ST32ETA204CT-ND
28	3	D300, D301, D302	SML-310VTT86	LED red 1608	ROHM SML-310VT

## Parts List

Table 6-1 : S5U13L01P00C100 Parts List

Item	Qty	Reference	Part	Description	Manufacture Part No. / Comments
29	1	D303	CRS04		TOSHIBA
30	2	L101, L102	BLM21P	FERRITE CHIP 220 OHM 2000mA 0805	MURATA BLM21P
31	1	Y1	SG-210SCB 24MHz	CRYSTAL OSCILLATOR 24MHz	EPSON SG-210SCB 24MHz
32	1	CN1	NM	Box Connector 2.54mm 40pin	not mounted
33	1	CN2	NM	Pin Header 2.54mm 16pin	not mounted
34	2	CN4, CN3	NM	Pin Header 2.54mm 26pin SMD	not mounted
35	1	CN5	WM3436CT-ND	FPC Connector	Molex
36	3	JP101, JP102, JP104		2.54mm 2 pos Jumper	SULLINS
37	5	JP105, JP106, JP107, JP108, JP109		2.54mm 3 pos Jumper	SULLINS
38	1	JP503	67997-108HLF	2.54mm 4x2 pos Jumper	FCI
39	2	P1, P2	151240-8422-RB	Pin Header 2mm 40pin SMD	3M
40	1	SW1	CHS-04A	Slide Switch 4bit	COPAL
41	1	SW2	CHS-10A	Slide Switch 8bit	COPAL
42	1	SW3	CHS-08A	Slide Switch 10bit	COPAL
43	1	SW4	SKRKAEE010	SMD Tactile Switches 3.9x2.9x2.0mm	ALPS
44	3	TH1, TH2, TH3	0.9mm dia	Through Hole 0.9mm dia	-
45	4	TP1, TP2, TP3, TP4	HK-2-S	Test Point	MAC8
46	12	SH101, SH102, SH104, SH105, SH106, SH107, SH108, SH109, SH503, SH504, SH505, SH506	SPN02SYBN-RC	.079 in. Jumper Shunt	SULLINS
47	2	-	EP-6	Spacer M3x6mm	MAC8
48	2	-	3M-5	Screw M3x5mm	MAC8

# Chapter 7 Schematic Diagrams

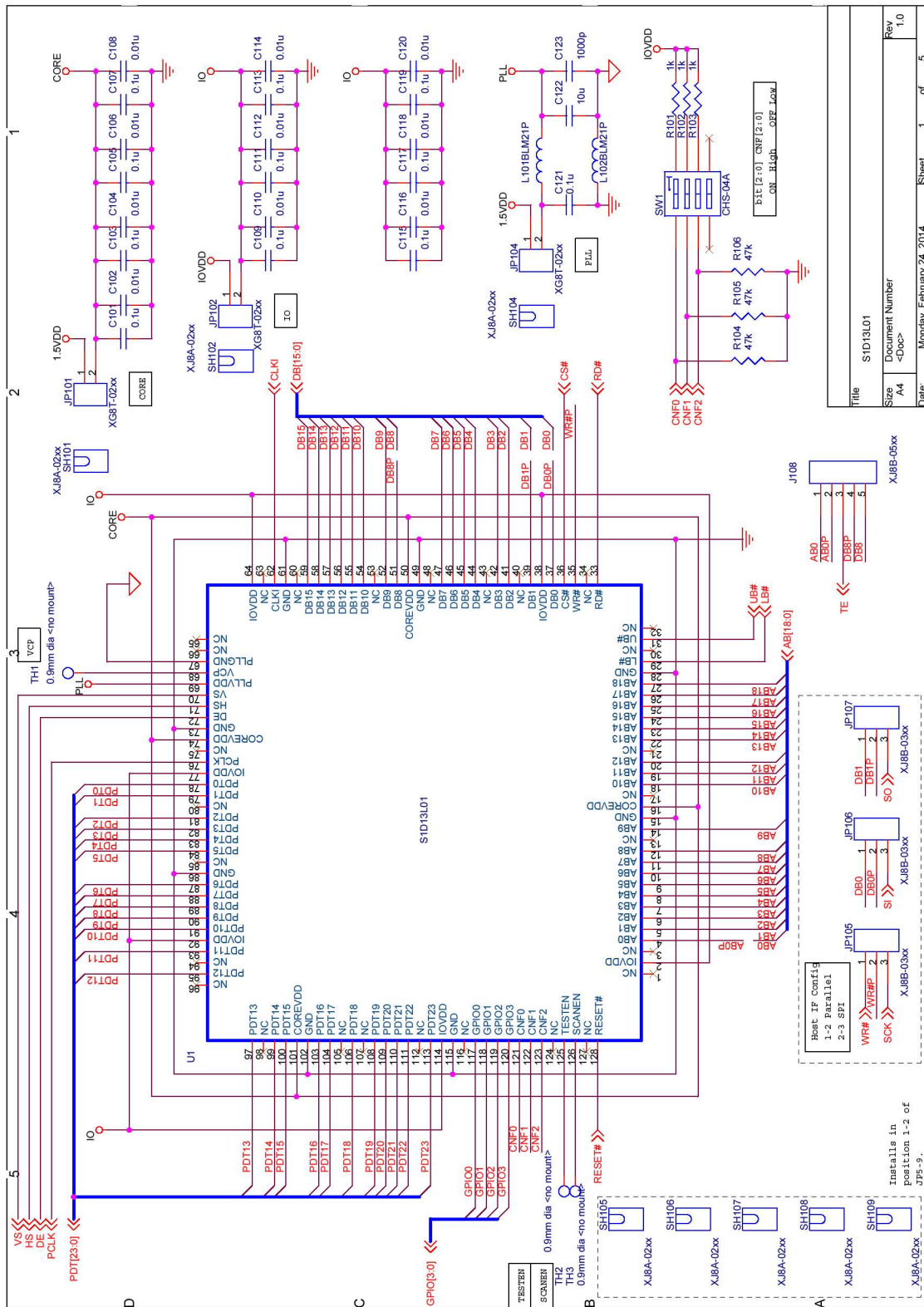
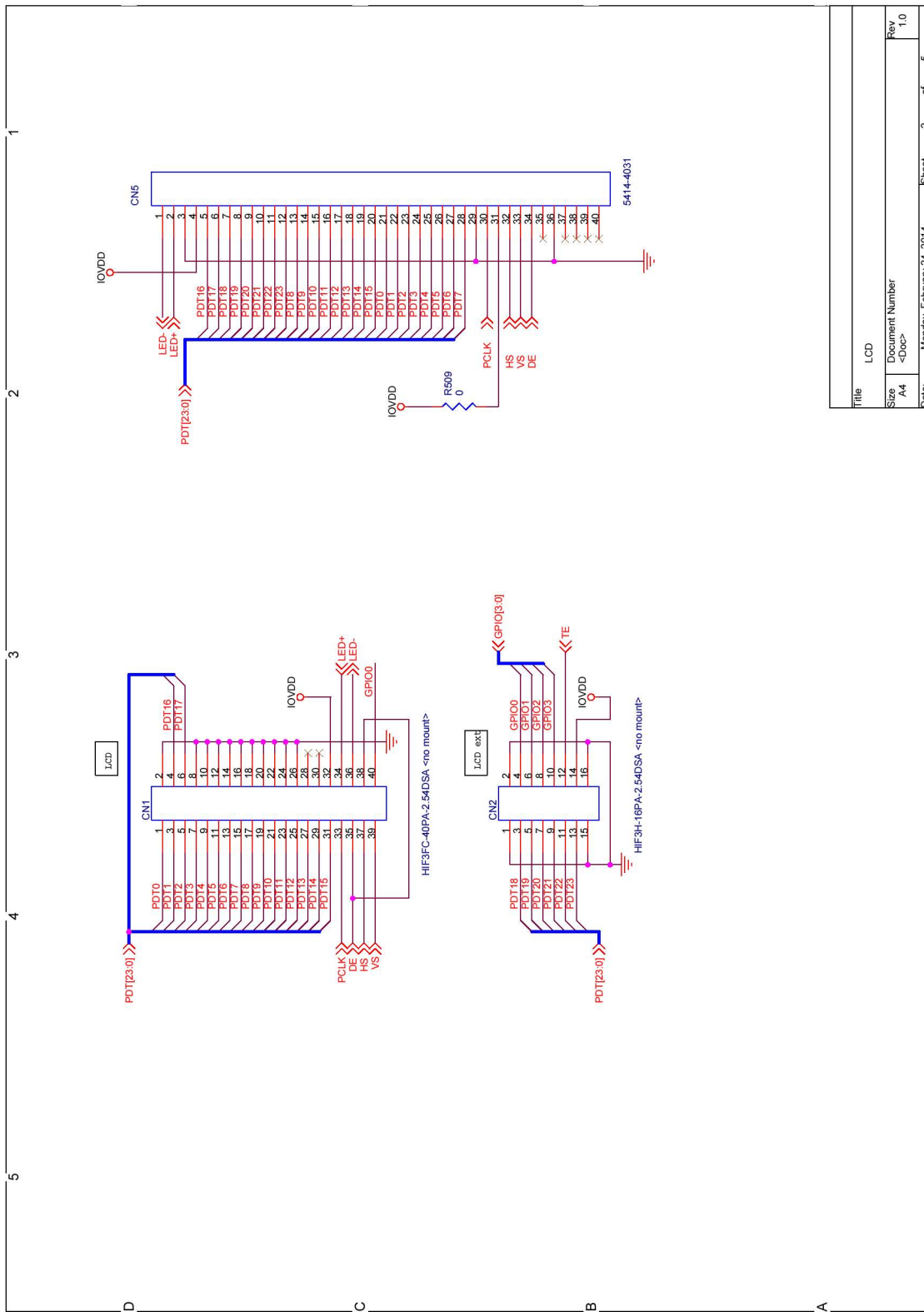


Figure 7-1: S5U13L01P00C100 Schematics (1 of 5)



Title	LCD
Size	A4
Document Number	<Doc>
Rev	1.0
Date	Monday, February 24, 2014
Sheet	2 of 5

Figure 7-2: S5U13L01P00C100 Schematics (2 of 5)



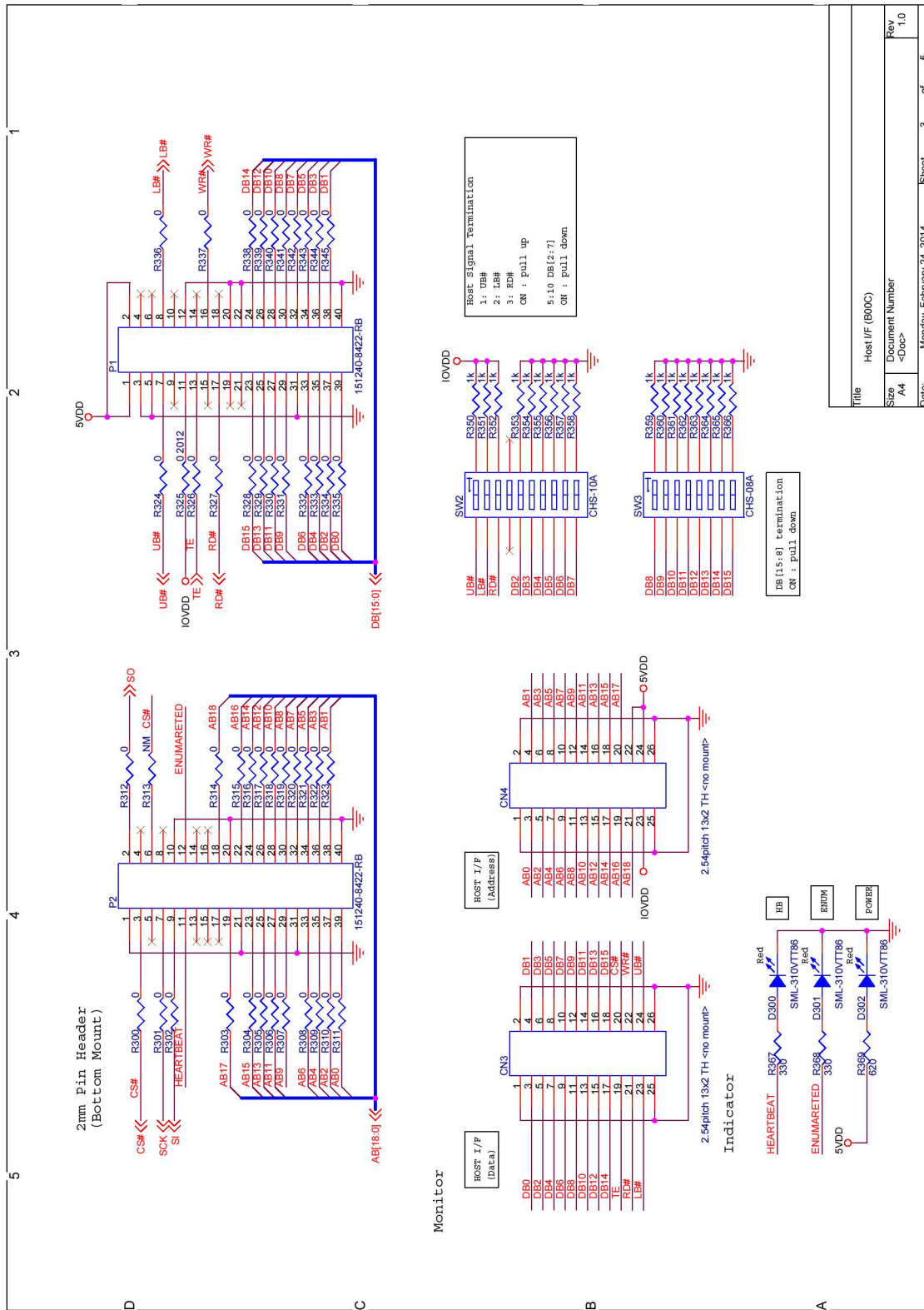


Figure 7-3: S5U13L01P00C100 Schematics (3 of 5)

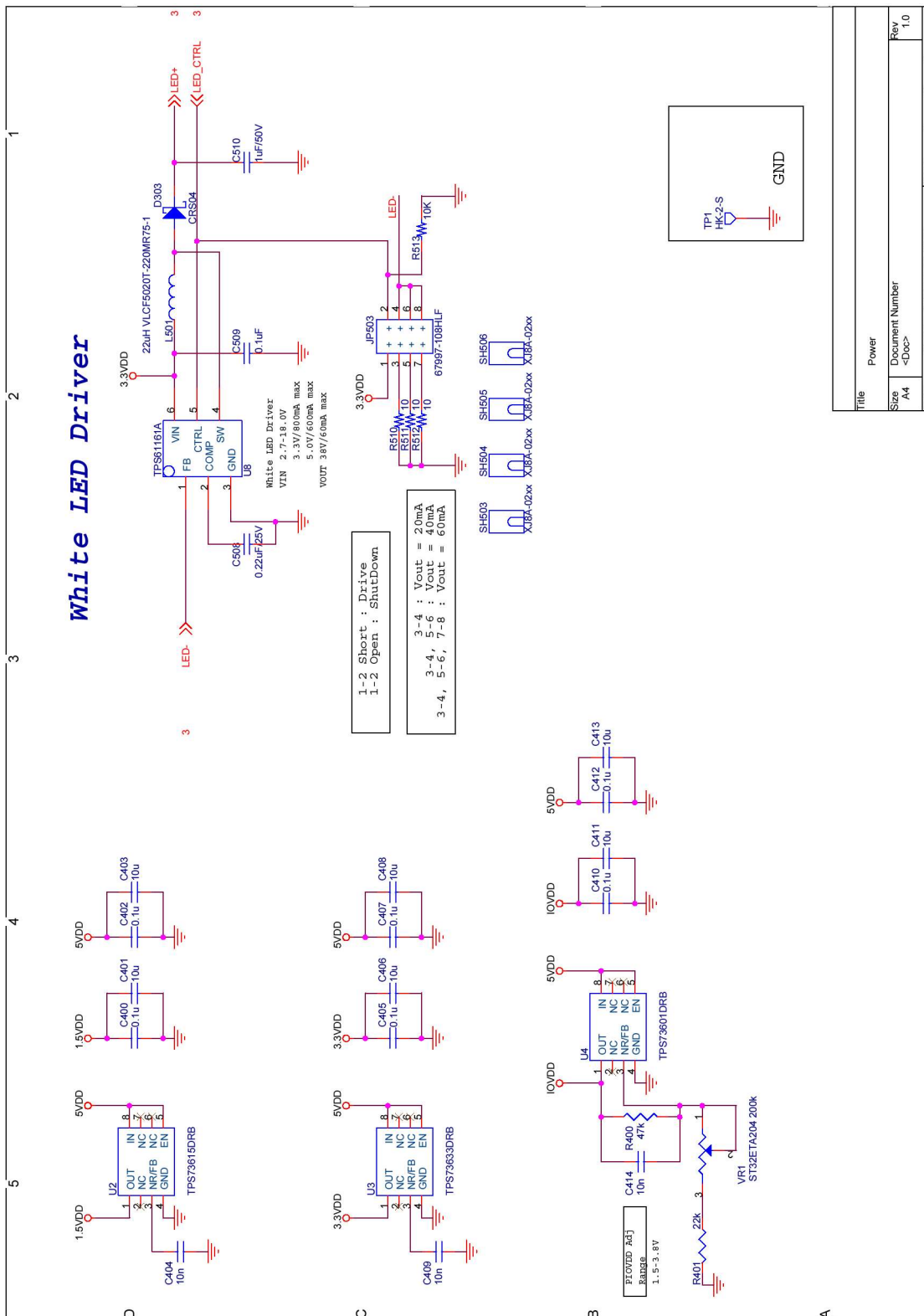
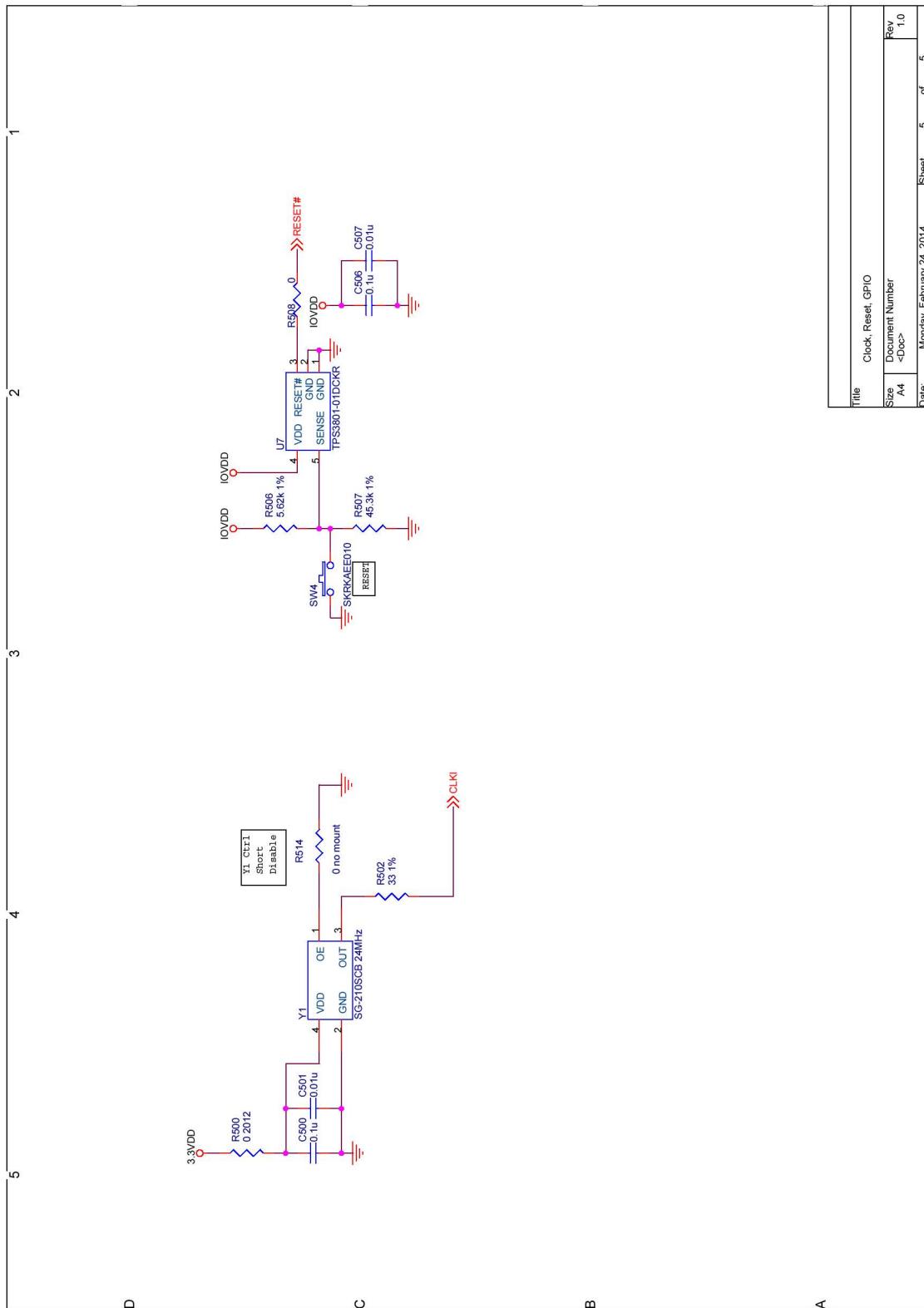


Figure 7-4: S5U13L01P00C100 Schematics (4 of 5)

Title	Power
Size	Document Number
A4	<Doc>
Date:	Monday, February 24, 2014
Sheet	4 of 5
Rev	1.0



Title	Clock, Reset, GPIO
Size	A4
Document Number	<Doc>
Rev	1.0
Date	Monday, February 24, 2014
Sheet	5 of 5

Figure 7-5: S5U13L01P00C100 Schematics (5 of 5)

# Chapter 8 Board Layout

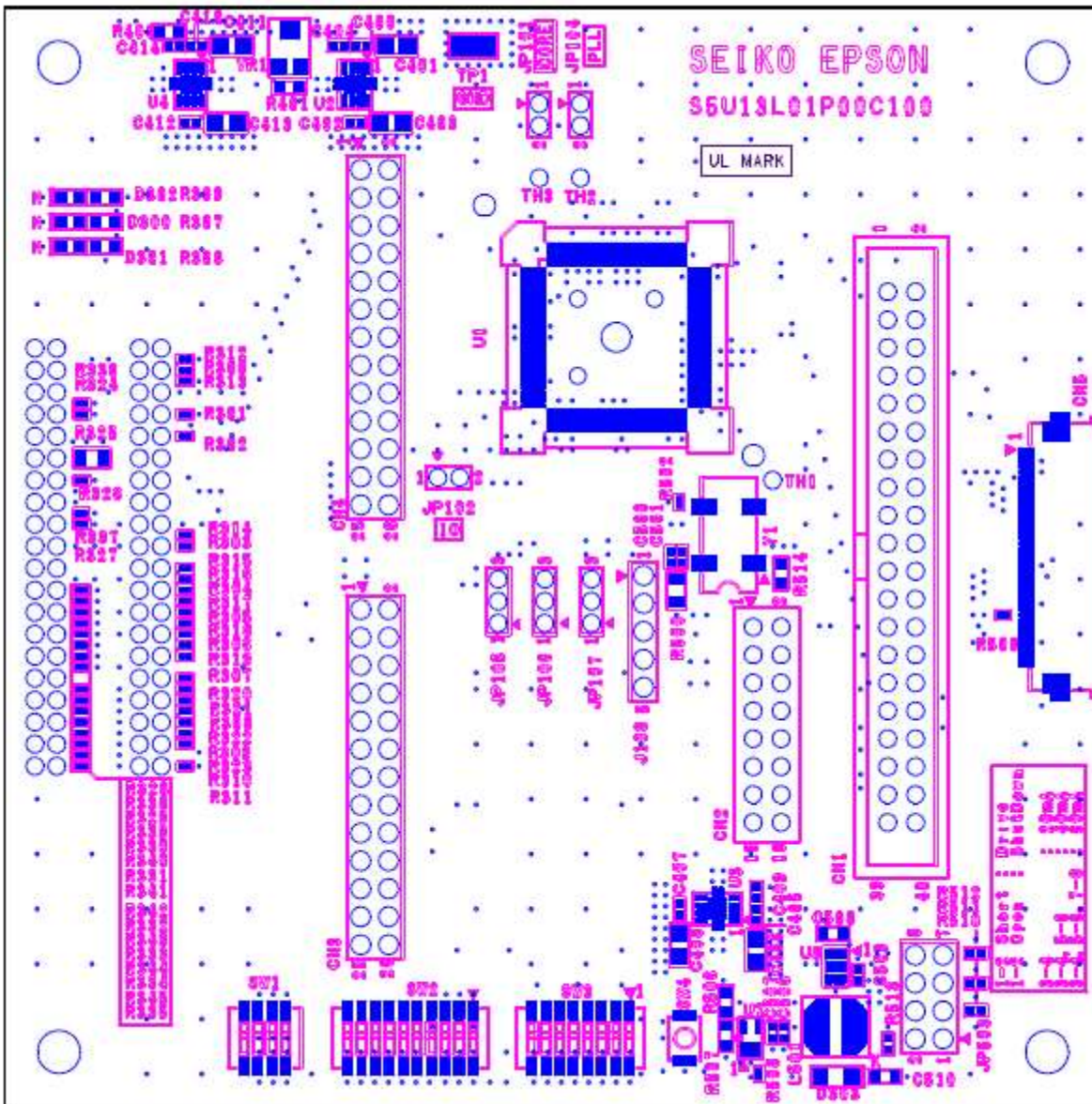


Figure 8-1: S5U13L01P00C100 Board Layout - Top View

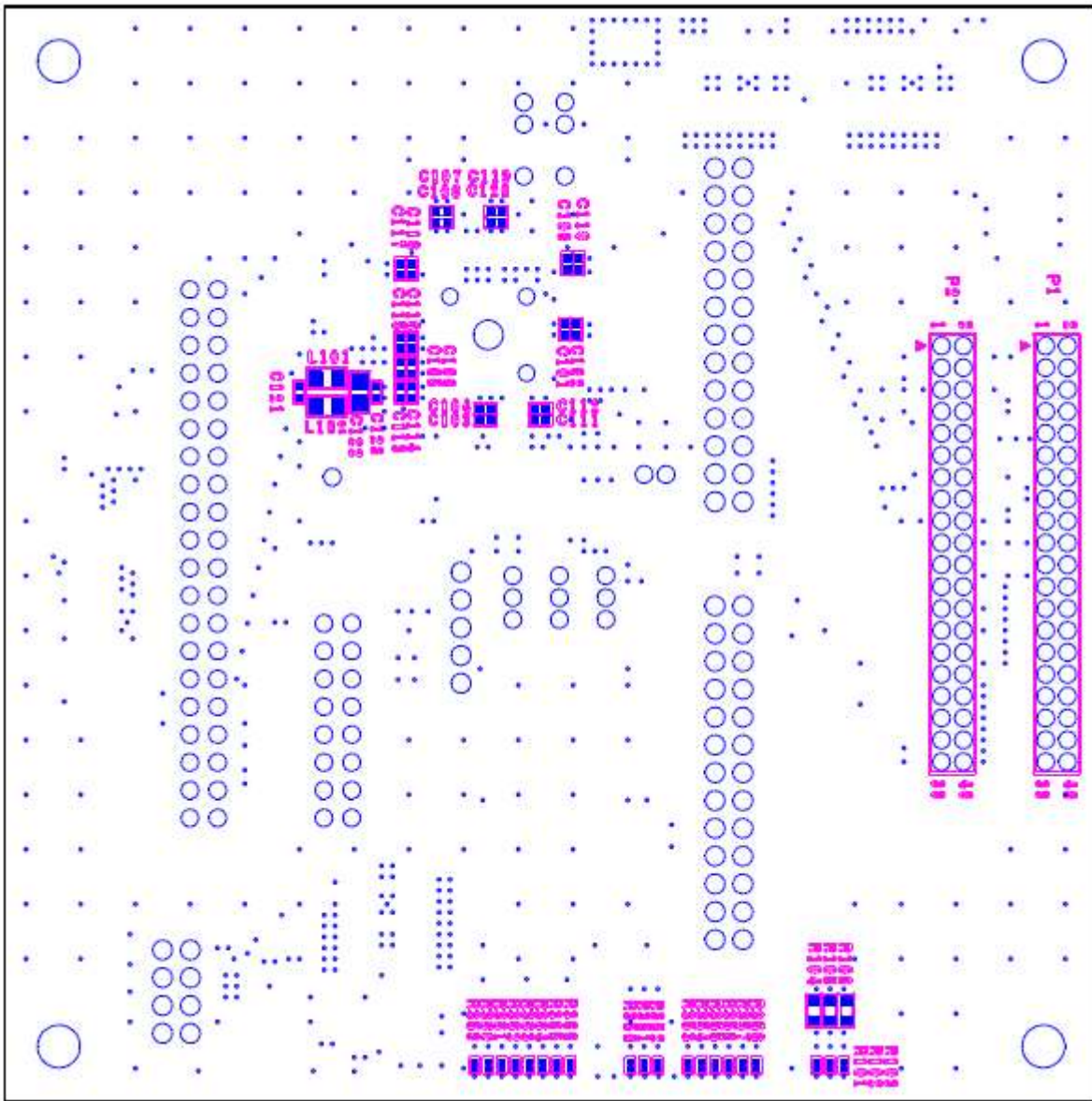


Figure 8-2: S5U13L01P00C100 Board Layout - Bottom View

# Chapter 9 Change Record

### **XA9A-G-001 Rev. 1.3 issued April 09, 2018**

- Updated address/contact page
- Updated Epson web page and email address
- Minor formatting changes

### **XA9A-G-001 Rev. 1.2 issued December 5, 2014**

- Corrected cropped board schematics.

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## Chapter 10 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

[https://global.epson.com/products\\_and\\_drivers/semicon/products/display\\_controllers/](https://global.epson.com/products_and_drivers/semicon/products/display_controllers/)



For Sales and Technical Support, contact the Epson representative for your region.

[https://global.epson.com/products\\_and\\_drivers/semicon/information/support.html](https://global.epson.com/products_and_drivers/semicon/information/support.html)

