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S1D13L02 LCDC

Hardware Functional Specification

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SEIKO EPSON CORPORATION

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Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13L02 LCD controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

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1.2 Overview Description

The S1D13L02 is a low cost, low power LCD controller providing LCD support for embedded and mobile products requiring up to WVGA resolution. Supporting up to three display layers, the S1D13L02 provides the Host processor with flexibility in handling multiple image sources. It's ability to receive high speed Host writes, combined with it's support for a wide variety of LCD panels, makes the S1D13L02 an excellent choice for a multitude of LCD applications.

The S1D13L02 includes a pixel doubling feature which allows easy migration to larger panel sizes using existing image data. The feature set includes independent resizing of PIP window image data, scrolling control for each layer,and LCD output manipulation such as gamma control and optional dithering. This allows the Host processor to provide image data, but off-loads the image processing requirement from the Host. The S1D13L02 contains 1024K bytes of embedded SRAM which is used to store image data for up to three layers for LCD. This feature set provides a low cost, low power single chip solution to meet the demands of embedded markets requiring up to WVGA resolution, such as Mobile Communications devices.

1.3 Abbreviations and Acronyms

The following abbreviations and acronyms are used in this document:

All numbers are in decimal unless marked otherwise (b for binary, h for hexadecimal)
K = 2^{10} = 1024 when used with regards to memory
b = bit
B = Byte
bpp = bits-per-pixel
msb = Most Significant bit
lsb = Least Significant bit
IO = Input/Output
LUT = Look-Up Table
NC = No Connection
VDP = Vertical Display Period
VNDP = Vertical Non-display Period
POUT = PLL Output

2 Features

2.1 Memory

- Embedded 1024k bytes of SRAM can be used for:
  - Main Window frame buffer
  - PIP1 Window frame buffer
  - PIP2 Window frame buffer

2.2 Registers

- Registers are memory mapped
- Asynchronous/synchronous registers (asynchronous registers are accessible during power save mode)

2.3 Host Interface

- 16-bit Indirect Host interface
  - Allows high speed writes (1 write cycle = 3 internal system clocks)
  - Integrated Host interface Write Controller (HWC) supports:
    - Rectangular Write Mode
    - Rotation Write Mode
    - Mirror Write Mode

2.4 Input Format

- Host can input image data as RGB 5:6:5

2.5 LCD Interface

- LCD interface supports the following panel types:
  - 16/18/24-bit RGB interface panels
    - Generic TFT interface

2.6 Display Functions

- Three layers which support Transparency and Alpha Blending functions:
  - Main Layer:
    - Image data can be stored as RGB 5:6:5
    - Pixel Doubling which doubles the size of the display image (independent horizontal/vertical)
  - PIP1 Layer:
    - Image data can be stored as RGB 5:6:5
    - Includes Bi-Cubic Scaler
    - Supports Edge Enhancement
  - PIP2 Layer:
    - Image data can be stored as RGB 5:6:5
    - Includes Bi-Cubic Scaler
    - Supports Edge Enhancement
    - Includes LUT (Look-Up Table) for independent gamma control of PIP2 window
- Independent Display Scrolling for each Layer (Main, PIP1, PIP2)
- LUT (Look-Up Table) for gamma control of the LCD output
- Dithering options for the LCD output

2.7 Miscellaneous

- Internal PLL or digital clock input (CLKI)
- Software initiated power save mode
- Available general purpose IO pins
- QFP22 208-pin package
  - 28mm (length) x 28mm (width) x 1.4mm(thickness), Pitch 0.5mm

3 Typical System Diagrams

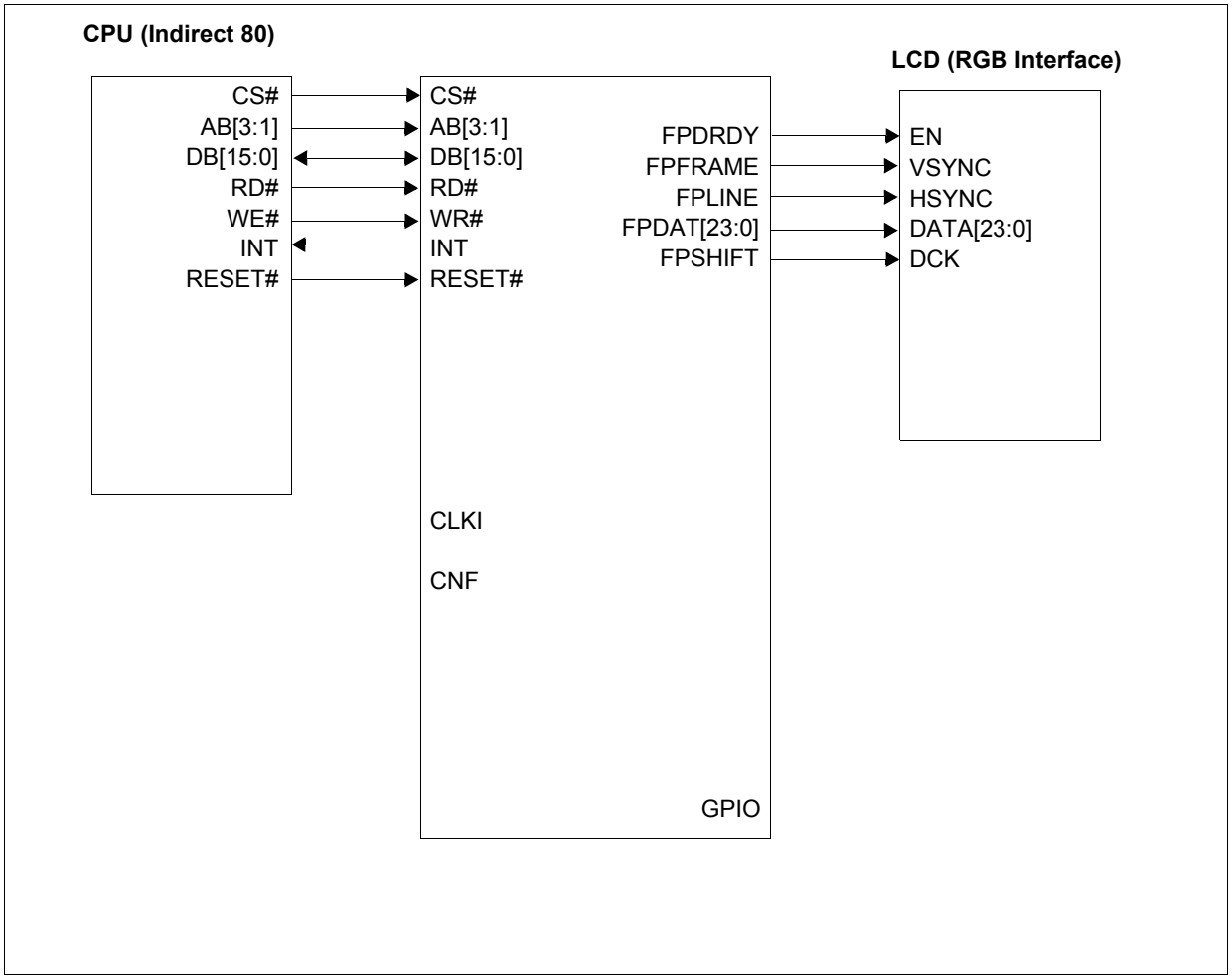


Figure 3-1: System Diagram 1

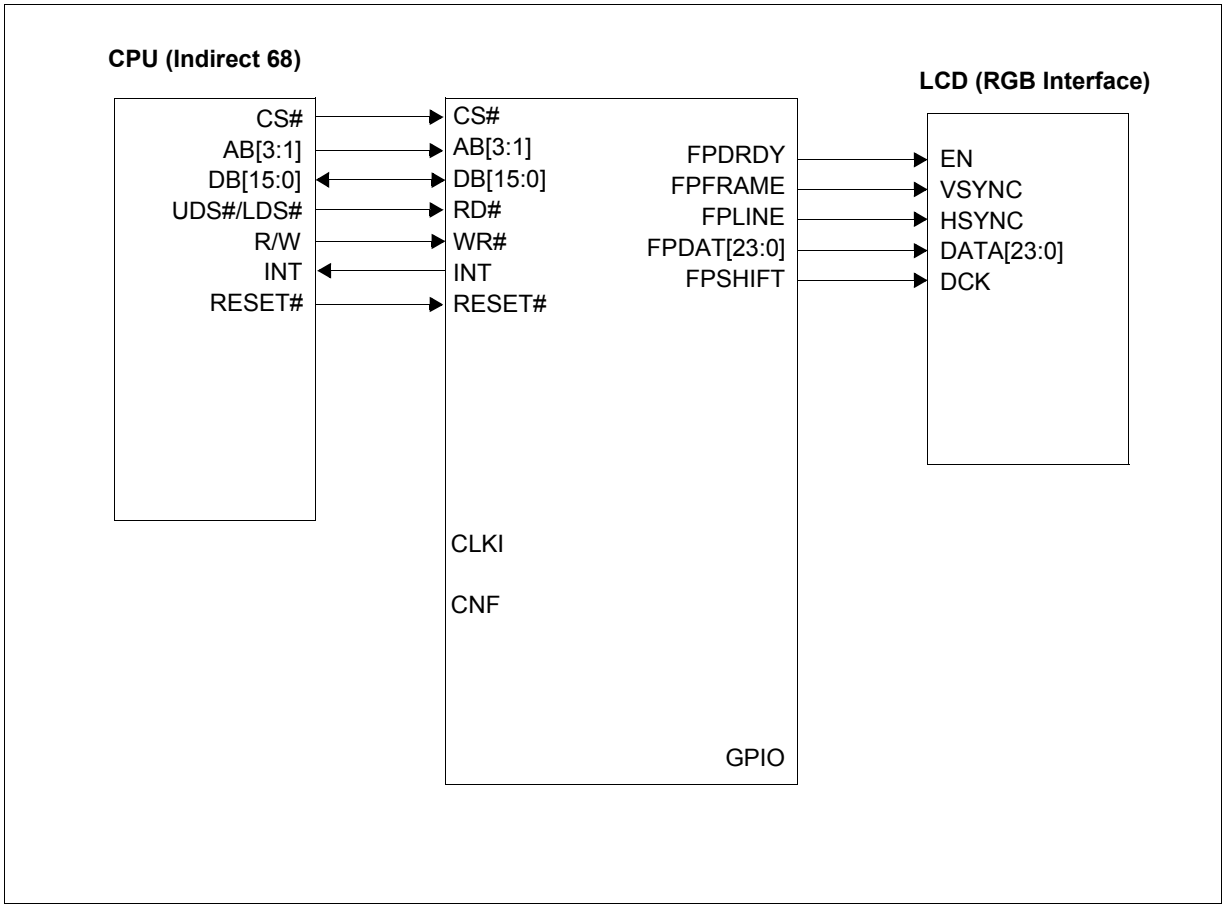


Figure 3-2: System Diagram 2

4 Block Diagram

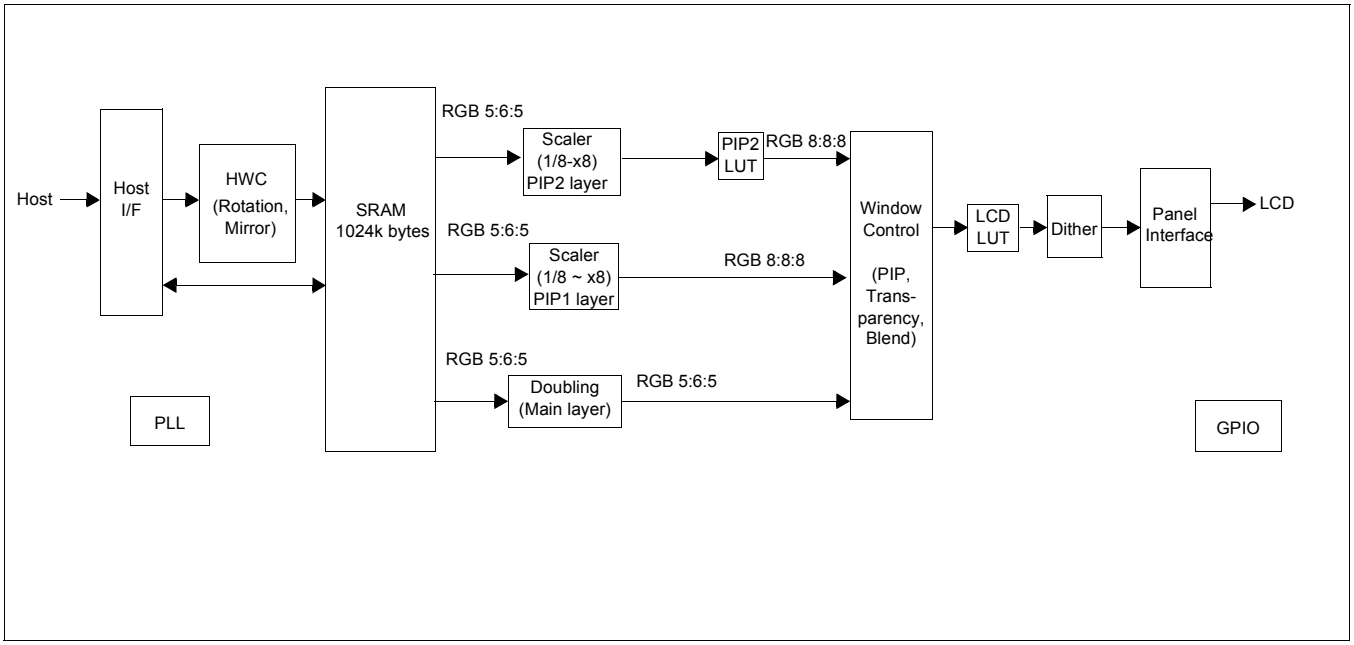


Figure 4-1: S1D13L02 Block Diagram

5 Pins

5.1 Pin Diagrams

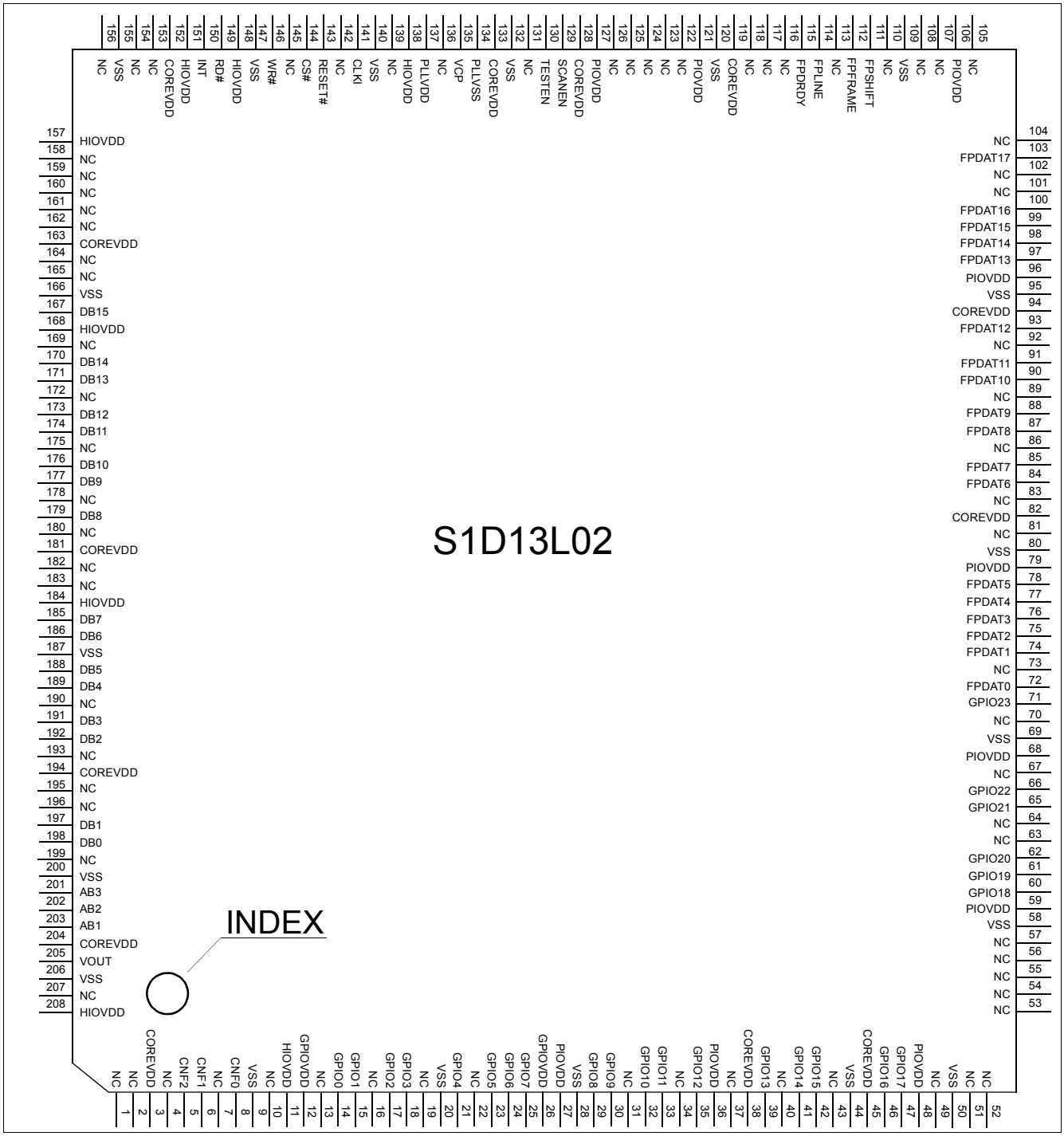


Figure 5-1: S1D13L02 QFP22-208-Pin Mapping(Top View)

5.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# States

H	=	High level output
L	=	Low level output
Z	=	High Impedance (Hi-Z)
1	=	Pull-up resistor on input
0	=	Pull-down resistor on input
#	=	Active low level

Table 5-1: Cell Descriptions

Item	Description
IC	CMOS input
ICD	CMOS input with pull-down resistor
ICU	CMOS input with pull-up resistor
IS	Schmitt input
ISD2	Schmitt input with pull-down resistor
ISG	Schmitt input with gated control
OB	Output buffer
BC	CMOS input bi-directional buffer
BCD	CMOS input bi-directional buffer with pull-down resister
ITD	Test mode control input with pull-down resistor
LIN	Low Voltage Transparent Input

5.2.1 Host Interface Pins

Some of the Host interface pins have different functions depending on the setting of CNF1. For a summary of host interface pin mapping, see Table 5-8: "Host Interface Pin Mapping," on page 23.

Table 5-2: Host Interface Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
AB[3:1]	I	201-203	IC	HIOVDD	—	Host interface address bus. These input pins are used to index the Indirect Interface Register Ports (see Section 14.1.1, "Indirect Addressing Register Ports" on page 156).
DB[15:0]	IO	167,170,171, 173,174,176, 177,179,185, 186,188,189, 191,192,197, 198	BC	HIOVDD	Hi-Z	Host interface data bus pins 15-0.
CS#	I	144	IC	HIOVDD	—	This input pin inputs the chip select signal.
RD#	I	149	IC	HIOVDD	—	This input pin is the read enable signal. • For Indirect 80 (CNF1 = 0), this pin is RD#. • For Indirect 68 (CNF1 = 1), this pin is UDS#/LDS#.
WR#	I	146	IC	HIOVDD	—	This input pin is the write enable signal. • For Indirect 80 (CNF1 = 0), this pin is WE#. • For Indirect 68 (CNF1 = 1), this pin is R/W#.
INT	O	150	OB	HIOVDD	L	Interrupt output. When an internal interrupt occurs, this output pin is driven high. If the Host CPU clears the internal interrupt, this pin is driven low.
RESET#	I	143	IS	HIOVDD	—	This active low input sets all internal registers to their default state and forces all signals to their inactive states.
VOUT	O	205	OB	HIOVDD	L	This output pin is the FPFRAME (VSYNC) signal for the host interface. For further information on configuring this pin, see REG[0198h] VOUT Configuration Register on page 78.

5.2.2 LCD Interface Pins

Many of the LCD interface pins have different functions depending on the configured panel interface mode. For details on the pin mapping for each mode, see Table 5-9: "LCD Interface Pin Mapping," on page 24.

For further information on the panel interface modes, see the bit description for REG[0032h] bits 1-0.

Table 5-3: LCD Interface Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
GPIO[23:18]	IO	71,66,65,62-60	BCD	PIOVDD	0	These input/output pins have multiple functions. • 24-bit RGB interfaces, these pins are the RGB data outputs (FPDAT[23:18]). • For LCD interfaces less than 24-bit, these pins are general purpose IO pins.
FPDAT[17:0]	IO	103,100-97,93,91,90,88,87,85,84,78-74,72	BCD	PIOVDD	L	These input/output pins are the LCD interface data pins and have multiple functions. These pins are the LCD RGB data outputs.
FPFRAME	O	112	OB	PIOVDD	L	This output pin has multiple functions. This pin is the LCD frame pulse output (VSYNC).
FPLINE	O	114	OB	PIOVDD	L	This output pin has multiple functions. This pin is the LCD line pulse output
FPSHIFT	O	111	OB	PIOVDD	L	This output pin has multiple functions. This pin is the LCD pixel clock output (DCK/CLK).
FPDRDY	O	115	OB	PIOVDD	L	This output pin has multiple functions. This pin is the LCD DRDY output (ENAB).
GPIO[17:10]	IO	47,46,42,41,39,35,33,32	BCD	PIOVDD	0	These pins are general purpose IO pins.
GPIO9	IO	30	BCD	PIOVDD	0	This pin is a general purpose IO pin.
GPIO8	IO	29	BCD	PIOVDD	0	This pin is a general purpose IO pin.

5.2.3 Clock Input Pin

Table 5-4: Clock Input Pin Description

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
CLKI	I	141	ISG	HIOVDD	—	This input clock has multiple functions. • When the internal PLL is used, this pin is the input reference clock for the internal PLL. • When the PLL is bypassed, this pin is the digital clock input for the system clock (SYSCLK). **Note:** When REG[0012h] bit 8 = 1b, the CLKI input can be left high impedance.

5.2.4 Miscellaneous Pins

Table 5-5: Miscellaneous Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
GPIO[7:0]	IO	25-23,21,18,17,15,14	BCD	GPIOVDD	0	These input/output pins are general purpose IO pins.
CNF[2:1]	I	5,6	IC	HIOVDD	—	These input pins are used for configuring the S1D13L02 and must be connected to either HIOVDD or VSS. The states of these pins are latched at RESET#. For more information, see Table 5-7: “Summary of Power-On Configurations,” on page 22.
CNF0	I	8	IC	HIOVDD	—	This configuration pin is Reserved and must be connected to VSS.
VCP	O	135	LIN	PLLVDD	—	Production test pin. For normal operations, this pin must be left unconnected.
TESTEN	I	130	ITD	COREVDD	—	Production test pin. For normal operations, this pin should be connected to VSS.
SCANEN	I	129	ISD2	COREVDD	—	Production test pin. For normal operations, this pin should be connected to VSS.

Table 5-5: Miscellaneous Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
NC	—	1,2,4,7,10,13,16,19,22,31,34,37,40,43,49,51-57,63,64,67,70,73,81,83,86,89,92,101,102,104,105,107,108,110,113,116-118,122-126,131,136,139,142,145,153,154,156,158-162,164,165,169,172,175,178,180,182,183,190,193,195,196,199,207	—	—	—	This pin must be left unconnected.

5.2.5 Power and Ground Pins

Table 5-6: Power and Ground Pin Descriptions

Pin Name	Type	QFP Pin#	Power	RESET# State	Description
HIOVDD	P	11,138,148,151,157,168,184,208	P	—	IO power supply for the host interface.
PIOVDD	P	27,36,48,59,68,79,96,106,121,127,	P	—	IO power supply for the panel interface.
GPIOVDD	P	12,26	P	—	IO power supply for the general purpose IO interface.
COREVDD	P	3,38,45,82,94,119,128,133,152,163,181,194,204	P	—	Core power supply
VSS	P	9,20,28,44,50,58,69,80,95,109,120,132,140,147,155,166,187,200,206	P	—	GND for HIOVDD, PIOVDD, GPIOVDD and COREVDD
PLLVDD	P	137	P	—	PLL power supply
PLLVSS	P	134	P	—	GND for PLLVDD

5.3 Summary of Configuration Options

These pins are used for configuration of the chip and must be connected directly to HIOVDD or VSS. The state of CNF[2:0] are latched on the rising edge of RESET#. Changed state at any other time has no effect.

Table 5-7: Summary of Power-On Configurations

CNF[2:0] Input	Power-On/Reset State	
	1 (connected to HIOVDD)	0 (connected to VSS)
CNF2	Big Endian	Little Endian
CNF1	Indirect 68	Indirect 80
CNF0	Reserved. Must be connected to VSS.	

5.4 Host Interface Pin Mapping

The Host interface is selected using the CNF1 pin. When CNF1=0, the Indirect 80 interface is selected. When CNF1=1, the indirect 68 interface is selected. For details on the pins, refer to Section 5.2.1, “Host Interface Pins” on page 17.

Table 5-8: Host Interface Pin Mapping

Pin Name	Indirect 80	Indirect 68
AB[3:1]	AB[3:1]	AB[3:1]
DB[15:0]	DB[15:0]	DB[15:0]
CS#	CS#	CS#
RD#	RD#	UDS#/LDS#
WR#	WE#	R/W#
INT	Interrupt Signal	
RESET#	RESET#	
SCS#	—	—
SCK	—	—
SA0	—	—
SI	—	—

5.5 LCD Interface Pin Mapping

The LCD panel interface mode is selected using the Panel Interface bits, REG[0032h] bit 1-0. For details on the specific data formats used for each panel type and panel width, refer to Section 15, “LCD Interface” on page 174.

Table 5-9: LCD Interface Pin Mapping

Pin Name	LCD Panel (RGB Interface) Generic TFT
FPFRAME	VSYNC
FPLINE	HSYNC
FPSHIFT	DCK
FPDRDY	ENAB
FPDAT0	R7
FPDAT1	R6
FPDAT2	R5
FPDAT3	G7
FPDAT4	G6
FPDAT5	G5
FPDAT6	B7
FPDAT7	B6
FPDAT8	B5
FPDAT9	R4
FPDAT10	R3
FPDAT11	R2
FPDAT12	G4
FPDAT13	G3
FPDAT14	G2
FPDAT15	B4
FPDAT16	B3
FPDAT17	B2
GPIO18 (FPDAT18)	R1
GPIO19 (FPDAT19)	R0
GPIO20 (FPDAT20)	G1
GPIO21 (FPDAT21)	G0
GPIO22 (FPDAT22)	B1
GPIO23 (FPDAT23)	B0

6 D.C. Characteristics

6.1 Absolute Maximum Ratings

Table 6-1: Absolute Maximum Ratings (VSS = 0V)

Symbol	Parameter	Rating	Units
HIOVDD[1]	Supply Voltage	VSS - 0.3 ~ 4.0	V
PIOVDD[2]		VSS - 0.3 ~ 4.0	V
GPIOVDD[3]		VSS - 0.3 ~ 4.0	V
COREVDD		VSS - 0.3 ~ 2.0	V
PLLVDD		VSS - 0.3 ~ 2.0	V
HVI	Input Voltage	VSS - 0.3 ~ HIOVDD + 0.5	V
		VSS - 0.3 ~ PIOVDD + 0.5	V
		VSS - 0.3 ~ GPIOVDD + 0.5	V
LVI		VSS - 0.3 ~ COREVDD + 0.5	V
		VSS - 0.3 ~ PLLVDD + 0.5	V
HVO	Output Voltage	VSS - 0.3 ~ HIOVDD + 0.5	V
		VSS - 0.3 ~ PIOVDD + 0.5	V
		VSS - 0.3 ~ GPIOVDD + 0.5	V
LVO		VSS - 0.3 ~ COREVDD + 0.5	V
		VSS - 0.3 ~ PLLVDD + 0.5	V
IOUT	Output Current	± 10	mA
Tstg	Storage Temperature	-65 ~ 150	°C

Note

1. HIOVDD ≥ COREVDD / PLLVDD
2. PIOVDD ≥ COREVDD / PLLVDD
3. GPIOVDD ≥ COREVDD / PLLVDD

6.2 Recommended Operating Conditions

Table 6-2: Recommended Operating Conditions 1

Symbol	Parameter	Condition	Min	Typ	Max	Units
HIOVDD	Host IO Supply Voltage	V_{SS} = 0 V	3.00	3.30	3.60	V
PIOVDD	Panel IO Supply Voltage	V_{SS} = 0 V	3.00	3.30	3.60	V
GPIOVDD	GPIO Supply Voltage	V_{SS} = 0 V	3.00	3.30	3.60	V
COREVDD	Core Supply Voltage	V_{SS} = 0 V	1.35	1.50	1.65	V
PLLVDD	PLL Supply Voltage	V_{SS} = 0 V	1.35	1.50	1.65	V
HVI	Input Voltage	—	-0.3	—	HIOVDD + 0.3	V
			-0.3	—	PIOVDD + 0.3	V
			-0.3	—	GPIOVDD + 0.3	V
LVI		—	-0.3	—	COREVDD + 0.3	V
			-0.3	—	PLLVDD + 0.3	V
Ta	Operating Temperature	—	-40	25	85	°C
tr	CMOS Input Rise Time[1]	—	—	—	50	ns
tf	CMOS Input Fall Time[1]	—	—	—	50	ns
tr	Schmitt Input Rise Time[1]	—	—	—	5	ms
tf	Schmitt Input Fall Time[1]	—	—	—	5	ms

Note

1. This time is the change time from 10% to 90% of VDD.

Table 6-3: Recommended Operating Conditions 2

Symbol	Parameter	Condition	Min	Typ	Max	Units
HIOVDD	Host IO Supply Voltage	V_{SS} = 0 V	2.66	2.80	2.94	V
PIOVDD	Panel IO Supply Voltage	V_{SS} = 0 V	2.66	2.80	2.94	V
GPIOVDD	GPIO Supply Voltage	V_{SS} = 0 V	2.66	2.80	2.94	V
COREVDD	Core Supply Voltage	V_{SS} = 0 V	1.35	1.50	1.65	V
PLLVDD	PLL Supply Voltage	V_{SS} = 0 V	1.35	1.50	1.65	V
HVI	Input Voltage	—	-0.3	—	HIOVDD + 0.3	V
			-0.3	—	PIOVDD + 0.3	V
			-0.3	—	GPIOVDD + 0.3	V
LVI		—	-0.3	—	COREVDD + 0.3	V
			-0.3	—	PLLVDD + 0.3	V
Ta	Operating Temperature	—	-40	25	85	°C
tr	CMOS Input Rise Time[1]	—	—	—	50	ns
tf	CMOS Input Fall Time[1]	—	—	—	50	ns
tr	Schmitt Input Rise Time[1]	—	—	—	5	ms
tf	Schmitt Input Fall Time[1]	—	—	—	5	ms

Note

1. This time is the change time from 10% to 90% of VDD.

Table 6-4: Recommended Operating Conditions 3

Symbol	Parameter	Condition	Min	Typ	Max	Units
HIOVDD	Host IO Supply Voltage	V_{SS} = 0 V	1.62	1.80	1.98	V
PIOVDD	Panel IO Supply Voltage	V_{SS} = 0 V	1.62	1.80	1.98	V
GPIOVDD	GPIO Supply Voltage	V_{SS} = 0 V	1.62	1.80	1.98	V
COREVDD	Core Supply Voltage	V_{SS} = 0 V	1.35	1.50	1.65	V
PLLVDD	PLL Supply Voltage	V_{SS} = 0 V	1.35	1.50	1.65	V
HVI	Input Voltage	—	-0.3	—	HIOVDD + 0.3	V
			-0.3	—	PIOVDD + 0.3	V
			-0.3	—	GPIOVDD + 0.3	V
LVI		—	-0.3	—	COREVDD + 0.3	V
			-0.3	—	PLLVDD + 0.3	V
Ta	Operating Temperature	—	-40	25	85	°C
tr	CMOS Input Rise Time[1]	—	—	—	50	ns
tf	CMOS Input Fall Time[1]	—	—	—	50	ns
tr	Schmitt Input Rise Time[1]	—	—	—	5	ms
tf	Schmitt Input Fall Time[1]	—	—	—	5	ms

Note

1. This time is the change time from 10% to 90% of VDD.

6.3 Electrical Characteristics

The following characteristics are for:
HIOVDD = PIOVDD = GPIOVDD, VSS = 0V, Ta = -40 - 85°C, CNF1 = 0.

The following table applies for HIOVDD = PIOVDD = GPIOVDD = 3.30V.

Table 6-5: Electrical Characteristics 1

Symbol	Parameter	Condition	Min	Typ	Max	Units
IL	Input Leakage Current	—	-5	—	5	μA
IOZ	Output Leakage Current	—	-5	—	5	μA
IQcore	Quiescent Current on COREVDD	—	—	200	—	μA
IQpll	Quiescent Current on PLLVDD	—	—	7	—	μA
IQio	Quiescent Current on HIOVDD, PIOVDD, GPIOVDD	—	—	34	—	μA
VIH1H	CMOS High Level Input Voltage	HIOVDD, PIOVDD = Max	2.20	—	HIOVDD, PIOVDD + 0.3	V
VIL1H	CMOS Low Level Input Voltage	HIOVDD, PIOVDD = Min	-0.3	—	0.75	V
VT1+	Schmitt Positive Trigger Voltage	HIOVDD, PIOVDD = Max	1.20	—	2.52	V
VT1-	Schmitt Negative Trigger Voltage	HIOVDD, PIOVDD = Min	0.75	—	1.98	V
ΔV1	Schmitt Hysteresis Voltage	HIOVDD, PIOVDD = Min	0.30	—	—	V
VT2+	Schmitt Positive Trigger Voltage	COREVDD = Max	0.54	—	1.15	V
VT2-	Schmitt Negative Trigger Voltage	COREVDD = Min	0.41	—	0.99	V
ΔV2	Schmitt Hysteresis Voltage	COREVDD = Min	0.14	—	—	V
RPLU1H	Pull-Up Resistance	VI = VSS	20	50	120	kΩ
RPLD1H	Pull-Down Resistance	VI = HIOVDD, PIOVDD	20	50	120	kΩ
RPLD1L	Pull-Down Resistance	VI = COREVDD	27	75	183	kΩ
VOH2H	High Level Output Voltage	HIOVDD, PIOVDD = min IOH = -1.8mA	HIOVDD, PIOVDD - 0.4	—	—	V
VOL2H	Low Level Output Voltage	HIOVDD, PIOVDD = min IOH = 1.8mA	—	—	VSS + 0.4	V
VOH4H	High Level Output Voltage	HIOVDD, PIOVDD = min IOH = -5.4mA	HIOVDD, PIOVDD - 0.4	—	—	V
VOL4H	Low Level Output Voltage	HIOVDD, PIOVDD = min IOH = 5.4mA	—	—	VSS + 0.4	V

The following table applies for HIOVDD = PIOVDD = GPIOVDD = 2.80V.

Table 6-6: Electrical Characteristics 2

Symbol	Parameter	Condition	Min	Typ	Max	Units
IL	Input Leakage Current	—	-5	—	5	µA
IOZ	Output Leakage Current	—	-5	—	5	µA
IQcore	Quiescent Current on COREVDD	—	—	200	—	µA
IQpll	Quiescent Current on PLLVDD	—	—	7	—	µA
IQio	Quiescent Current on HIOVDD, PIOVDD, GPIOVDD	—	—	9.2	—	µA
VIH1H	CMOS High Level Input Voltage	HIOVDD, PIOVDD = Max	1.85	—	HIOVDD, PIOVDD + 0.3	V
VIL1H	CMOS Low Level Input Voltage	HIOVDD, PIOVDD = Min	-0.3	—	0.75	V
VT1+	Schmitt Positive Trigger Voltage	HIOVDD, PIOVDD = Max	0.94	—	1.91	V
VT1-	Schmitt Negative Trigger Voltage	HIOVDD, PIOVDD = Min	0.67	—	1.61	V
ΔV1	Schmitt Hysteresis Voltage	HIOVDD, PIOVDD = Min	0.27	—	—	V
VT2+	Schmitt Positive Trigger Voltage	COREVDD = Max	0.54	—	1.15	V
VT2-	Schmitt Negative Trigger Voltage	COREVDD = Min	0.41	—	0.99	V
ΔV2	Schmitt Hysteresis Voltage	COREVDD = Min	0.14	—	—	V
RPLU1H	Pull-Up Resistance	VI = VSS	22	55	132	kΩ
RPLD1H	Pull-Down Resistance	VI = HIOVDD, PIOVDD	22	55	132	kΩ
RPLD1L	Pull-Down Resistance	VI = COREVDD	27	75	183	kΩ
VOH2H	High Level Output Voltage	HIOVDD, PIOVDD = min IOH = -1.8mA	HIOVDD, PIOVDD - 0.4	—	—	V
VOL2H	Low Level Output Voltage	HIOVDD, PIOVDD = min IOH = 1.8mA	—	—	VSS + 0.4	V
VOH4H	High Level Output Voltage	HIOVDD, PIOVDD = min IOH = -5.4mA	HIOVDD, PIOVDD - 0.4	—	—	V
VOL4H	Low Level Output Voltage	HIOVDD, PIOVDD = min IOH = 5.4mA	—	—	VSS + 0.4	V

The following table applies for HIOVDD = PIOVDD = GPIOVDD = 1.80V.

Table 6-7: Electrical Characteristics 3

Symbol	Parameter	Condition	Min	Typ	Max	Units
IL	Input Leakage Current	—	-5	—	5	µA
IOZ	Output Leakage Current	—	-5	—	5	µA
IQcore	Quiescent Current on COREVDD	—	—	200	—	µA
IQpll	Quiescent Current on PLLVDD	—	—	7	—	µA
IQio	Quiescent Current on HIOVDD, PIOVDD, GPIOVDD	—	—	6.44	—	µA
VIH1H	CMOS High Level Input Voltage	HIOVDD, PIOVDD = Max	1.29	—	HIOVDD, PIOVDD + 0.3	V
VIL1H	CMOS Low Level Input Voltage	HIOVDD, PIOVDD = Min	-0.3	—	0.56	V
VT1+	Schmitt Positive Trigger Voltage	HIOVDD, PIOVDD = Max	0.65	—	1.38	V
VT1-	Schmitt Negative Trigger Voltage	HIOVDD, PIOVDD = Min	0.49	—	1.18	V
ΔV1	Schmitt Hysteresis Voltage	HIOVDD, PIOVDD = Min	0.17	—	—	V
VT2+	Schmitt Positive Trigger Voltage	COREVDD = Max	0.54	—	1.15	V
VT2-	Schmitt Negative Trigger Voltage	COREVDD = Min	0.41	—	0.99	V
ΔV2	Schmitt Hysteresis Voltage	COREVDD = Min	0.14	—	—	V
RPLU1H	Pull-Up Resistance	VI = VSS	36	100	244	kΩ
RPLD1H	Pull-Down Resistance	VI = HIOVDD, PIOVDD	36	100	244	kΩ
RPLD1L	Pull-Down Resistance	VI = COREVDD	27	75	183	kΩ
VOH2H	High Level Output Voltage	HIOVDD, PIOVDD = min IOH = -1.8mA	HIOVDD, PIOVDD - 0.4	—	—	V
VOL2H	Low Level Output Voltage	HIOVDD, PIOVDD = min IOH = 1.8mA	—	—	VSS + 0.4	V
VOH4H	High Level Output Voltage	HIOVDD, PIOVDD = min IOH = -5.4mA	HIOVDD, PIOVDD - 0.4	—	—	V
VOL4H	Low Level Output Voltage	HIOVDD, PIOVDD = min IOH = 5.4mA	—	—	VSS + 0.4	V

7 AC Characteristics

Conditions for HIOVDD = PIOVDD = GPIOVDD = 1.62 ~ 1.98V

- T_A = -40° C to 85° C
- Output Driver = 5.4mA (REG[0004h] bits 15-13 = 111b)
- T_{rise} and T_{fall} for all inputs except CLKI must be < 50 ns (10% ~ 90%)
- C_L = 30pF (Host Interface)
- C_L = 30pF (LCD Interface)
- C_L = 30pF (GPIO Interface)

Conditions for HIOVDD = PIOVDD = GPIOVDD = 2.66 ~ 2.94V

- T_A = -40° C to 85° C
- Output Driver = 3.6mA (REG[0004h] bits 15-13 =000b)
- T_{rise} and T_{fall} for all inputs except CLKI must be < 50 ns (10% ~ 90%)
- C_L = 30pF (Host Interface)
- C_L = 30pF (LCD Interface)
- C_L = 30pF (GPIO Interface)

Conditions for HIOVDD = PIOVDD = GPIOVDD = 3.00 ~ 3.60V

- T_A = -40° C to 85° C
- Output Driver = 4.0mA (REG[0004h] bits 15-13 =000b)
- T_{rise} and T_{fall} for all inputs except CLKI must be < 50 ns (10% ~ 90%)
- C_L = 30pF (Host Interface)
- C_L = 30pF (LCD Interface)
- C_L = 30pF (GPIO Interface)

7.1 Clock Timing

7.1.1 Input Clock Timing

The following timing information specifies the input requirements when CLKI will be used as the PLL reference clock (REG[0012h] bit 0 = 0b). For details on configuring the PLL, refer to Section 10.4.2, "Clock Configuration Registers" on page 57. For more information on the clock structure of the S1D13L02, refer to Section 9.1, "Clock Diagram" on page 50.

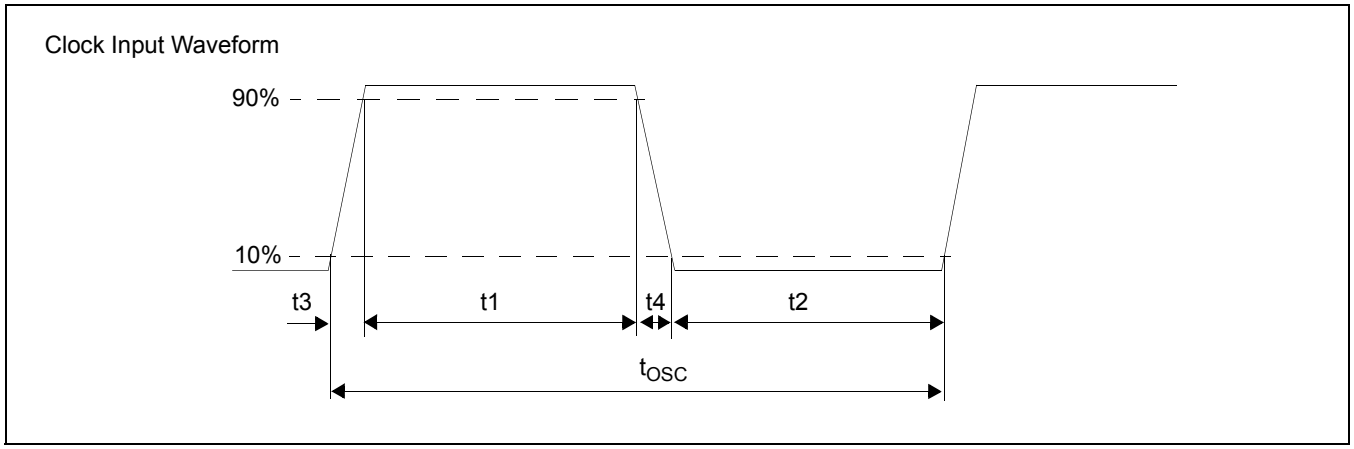


Figure 7-1: Clock Input Requirements (CLKI when PLL Used)

Table 7-1: Clock Input Requirements (CLKI when PLL Used)

Symbol	Parameter	Min	Typ	Max	Units
f_{OSCI}	Input Clock Frequency (CLKI)	1	—	33	MHz
T_{OSC}	Input Clock period (CLKI)	$1/f_{OSC}$	—	—	ns
t1	Input Clock Pulse Width High (CLKI)	$0.4t_{OSC}$	—	$0.6t_{OSC}$	us
t2	Input Clock Pulse Width Low (CLKI)	$0.4t_{OSC}$	—	$0.6t_{OSC}$	us
t3	Input clock rising time (10% - 90%)	—	—	10	ns
t4	Input clock falling time (10% - 90%)	—	—	10	ns

The following timing information specifies the input requirements when CLKI will be used as the source for the system clock (SYSCLK), bypassing the PLL (REG[0012h] bit 0 = 1b). For details on the clock structure of the S1D13L02, refer to Section 9.1, "Clock Diagram" on page 50.

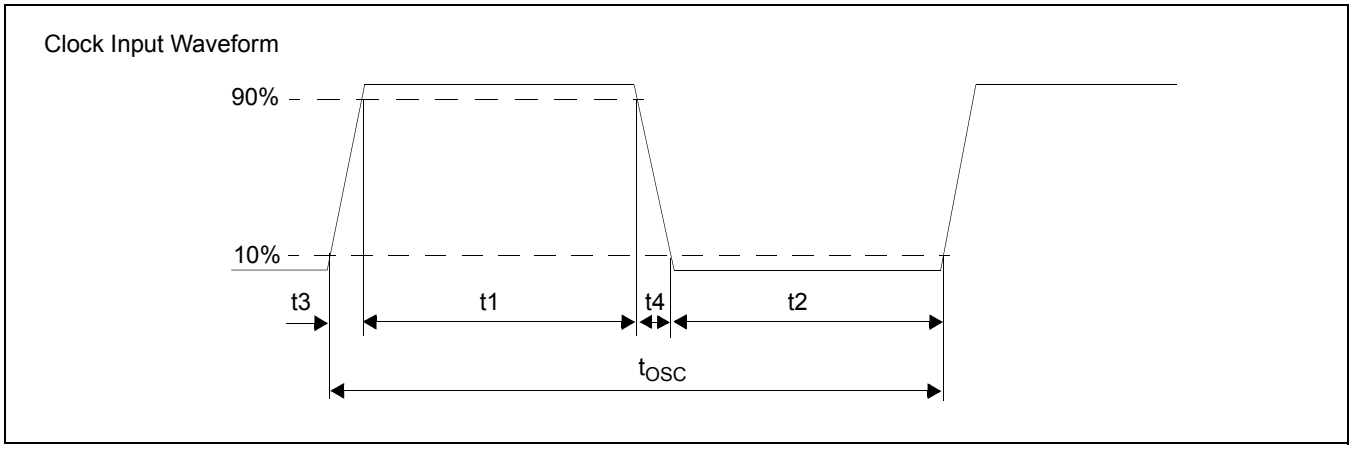


Figure 7-2: Clock Input Requirements (CLKI when PLL Bypassed)

Table 7-2: Clock Input Requirements (CLKI when PLL Bypassed)

Symbol	Parameter	Min	Typ	Max	Units
f_{OSCI}	Input Clock Frequency (CLKI)	—	—	58	MHz
T_{OSC}	Input Clock period (CLKI)	$1/f_{OSC}$	—	—	ns
t1	Input Clock Pulse Width High (CLKI)	$0.4t_{OSC}$	—	$0.6t_{OSC}$	us
t2	Input Clock Pulse Width Low (CLKI)	$0.4t_{OSC}$	—	$0.6t_{OSC}$	us
t3	Input clock rising time (10% - 90%)	—	—	10	ns
t4	Input clock falling time (10% - 90%)	—	—	10	ns

7.1.2 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

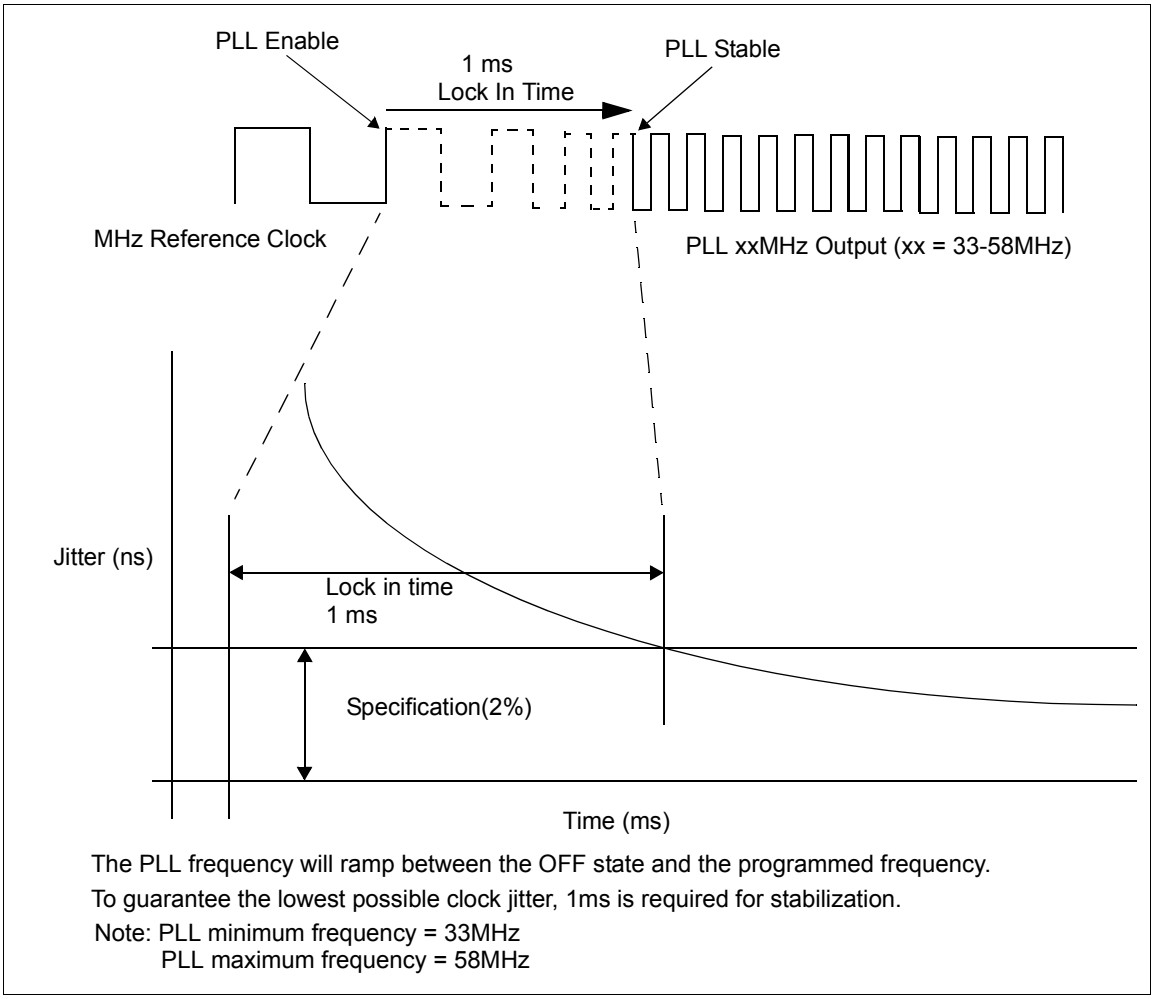


Figure 7-3: PLL Start-Up Time

7.2 Power Supply Sequence

7.2.1 Power-On Sequence

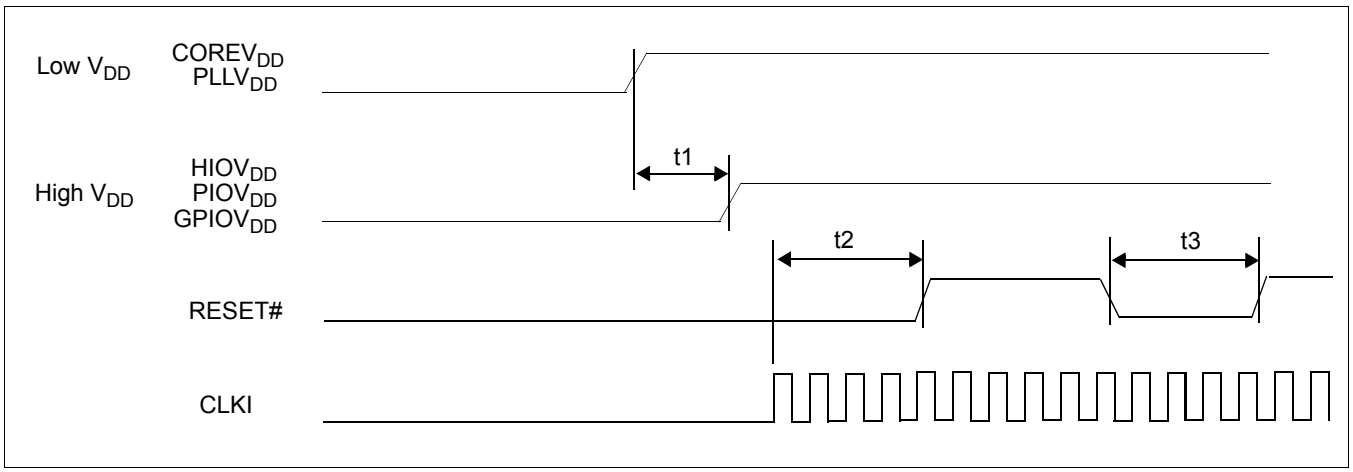


Figure 7-4: Power-On Sequence

Table 7-3: Power-On Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	High VDD on delay from low VDD on	0	10	ms
t2	RESET# hold time	2	—	Tck (Note 1)
t3	RESET# active width	2	—	Tck

1. Tck = CLKI Clock Period

7.2.2 Power-Off Sequence

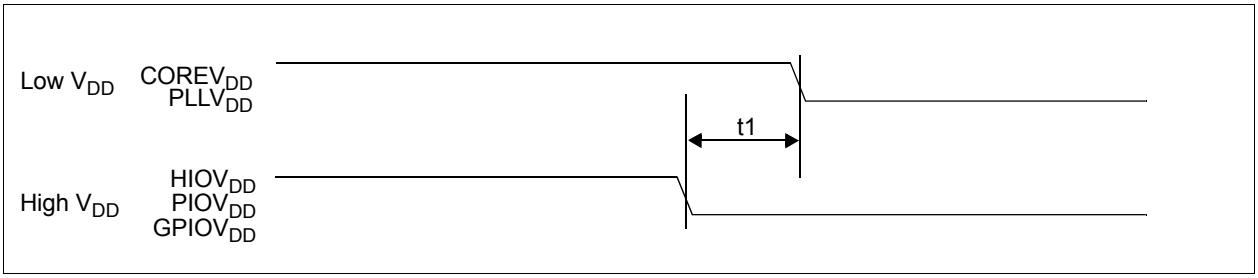


Figure 7-5: Power-Off Sequence

Table 7-4: Power-Off Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	High V_{DD} off delay from Low V_{DD} off	0	10	ms

7.3 Host Bus Interface Timing

7.3.1 Indirect 80 Timing

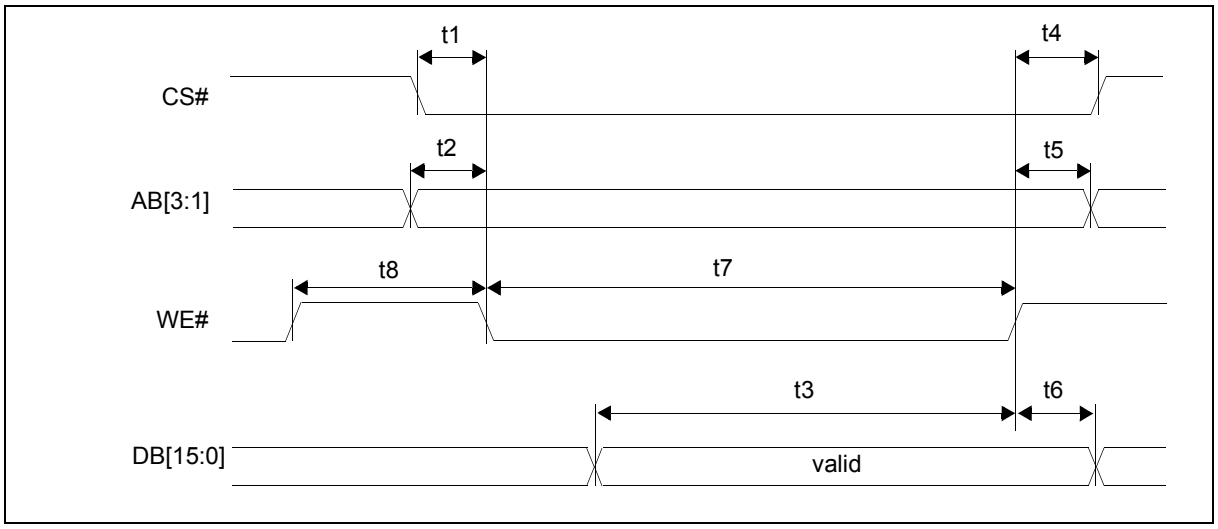


Figure 7-6: Indirect 80 Write Cycle Single Access Timing

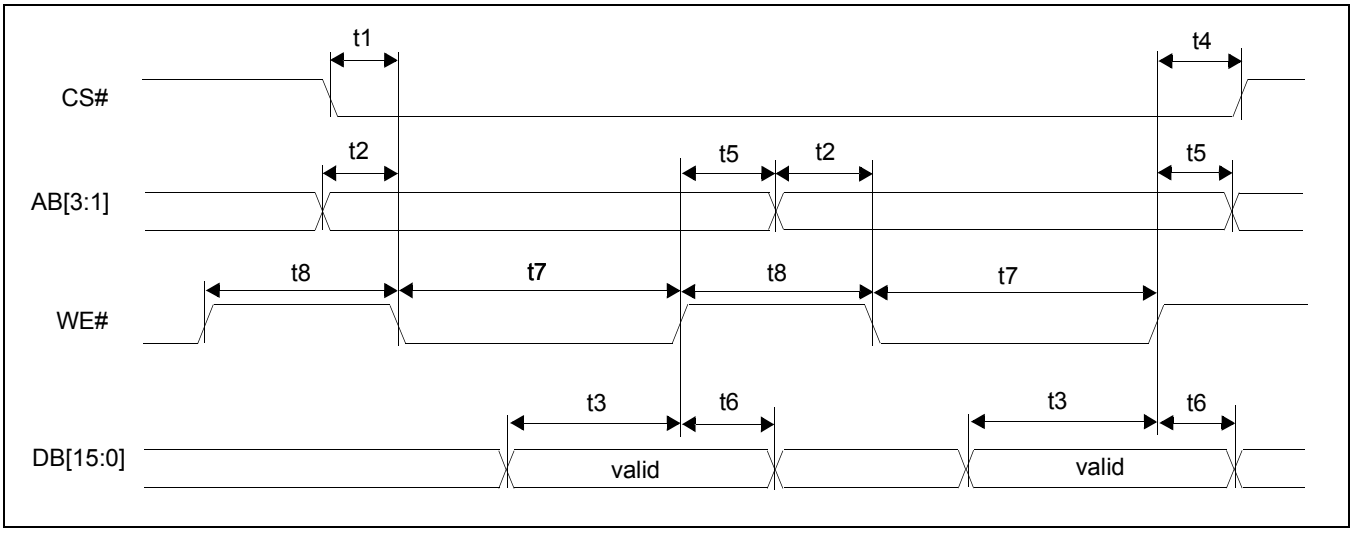


Figure 7-7: Indirect 80 Write Cycle Burst Access Timing

Note
The Indirect 80 interface write cycle timing included in this specification is preliminary and subject to change.

Table 7-5: Indirect 80 Write Cycle Timing

Symbol	Parameter	HIOVDD = 1.8V		HIOVDD = 2.8V or 3.3V		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	AB[3:1] setup time	5	—	5	—	ns
t3	DB[15:0] setup time to WE# rising edge	5	—	5	—	ns
t4	CS# hold time from WE# rising edge	5	—	5	—	ns
t5	AB[3:1] hold time from WE# rising edge	5	—	5	—	ns
t6	DB[15:0] hold time from WE# rising edge	5	—	5	—	ns
t7	WE# pulse active time	2	—	2	—	Ts (Note 1)
t8	WE# pulse inactive time	1	—	1	—	Ts

1. Ts = System Clock Period

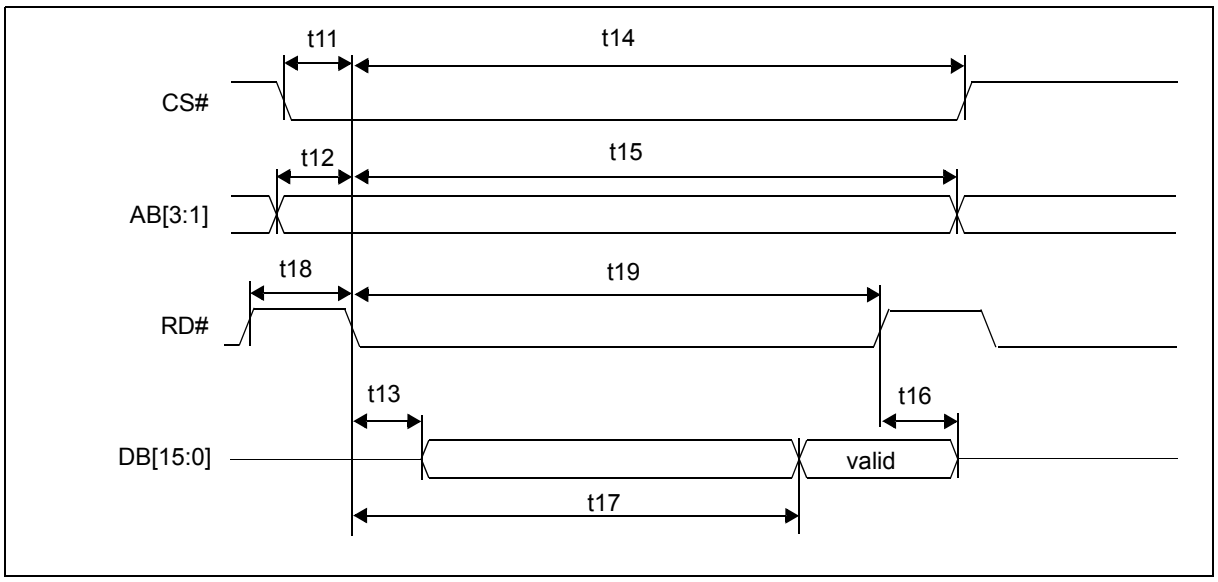


Figure 7-8: Indirect 80 Read Cycle Single Access Timing

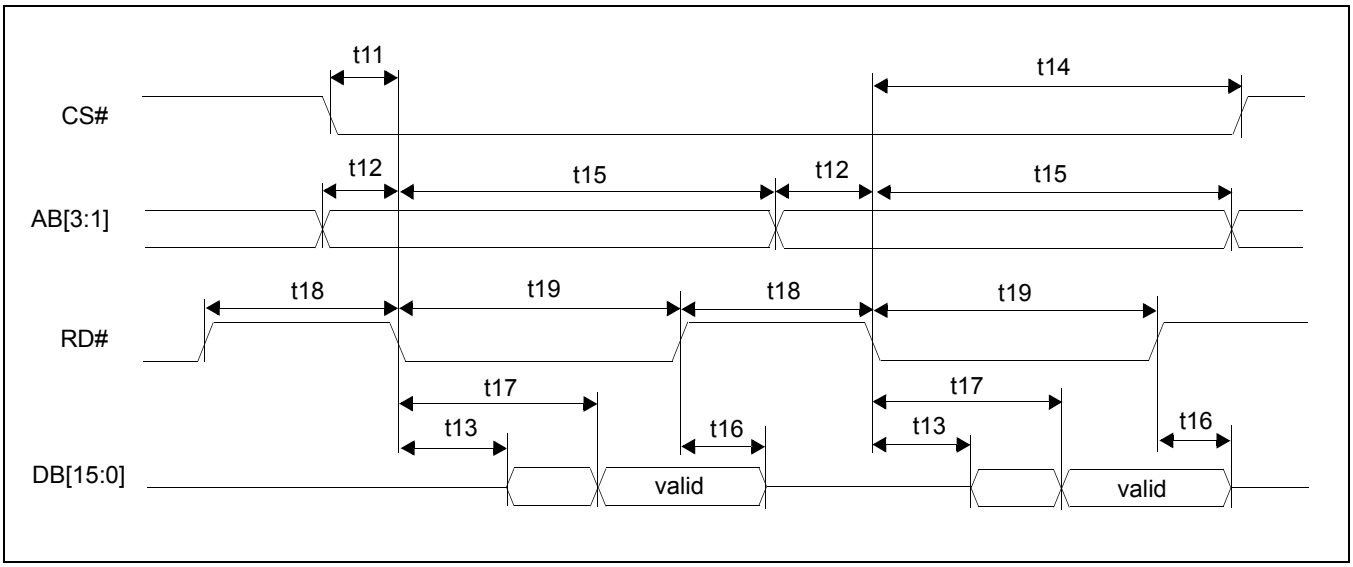


Figure 7-9: Indirect 80 Read Cycle Burst Access Timing

Note

The Indirect 80 interface read cycle timing included in this specification is preliminary and subject to change.

Table 7-6: Indirect 80 Read Cycle Timing

Symbol	Parameter	HIOVDD = 1.8V		HIOVDD = 2.8V or 3.3V		Units
		Min	Max	Min	Max	
t11	CS# setup time	5	—	5	—	ns
t12	AB[3:1] setup time	5	—	5	—	ns
t13	RD# falling edge to DB[15:0] driven	4	—	3	—	ns
t14	CS# hold time from RD# falling edge	1	—	1	—	Ts (Note 1)
t15	AB[3:1] hold time from RD# falling edge	1	—	1	—	Ts
t16	DB[15:0] hold time from RD# rising edge	2	11	2	10	ns
t17	RD# falling edge to valid data	—	27	—	22	ns
t18	RD# pulse inactive time	1	—	1	—	Ts
t19	RD# pulse active time	2	—	2	—	Ts

1. Ts = System Clock Period

7.3.2 Indirect 68 Timing

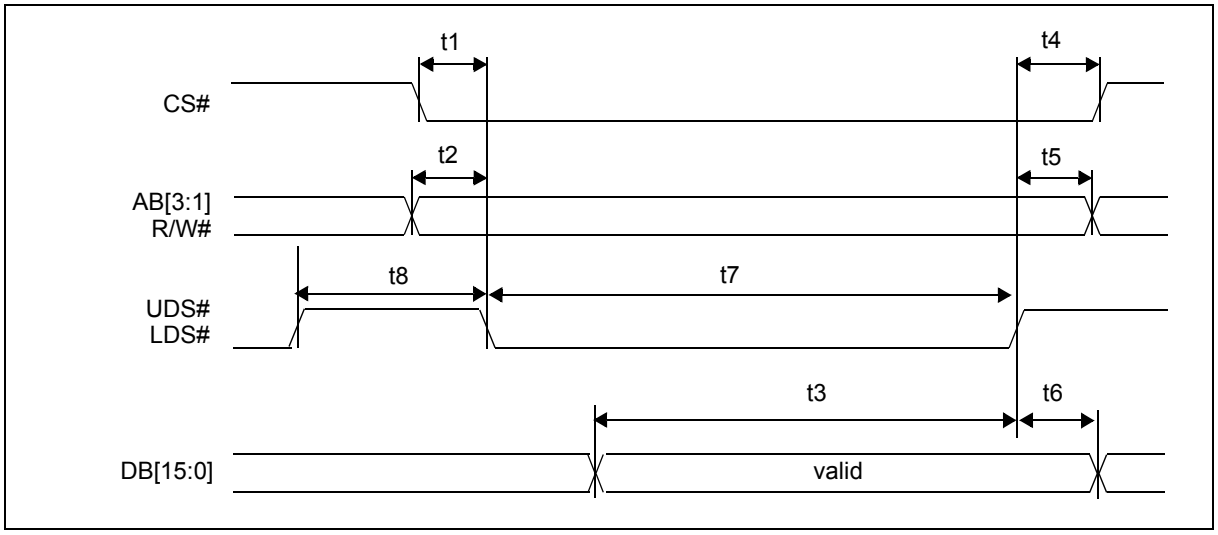


Figure 7-10: Indirect 68 Write Cycle Single Access Timing

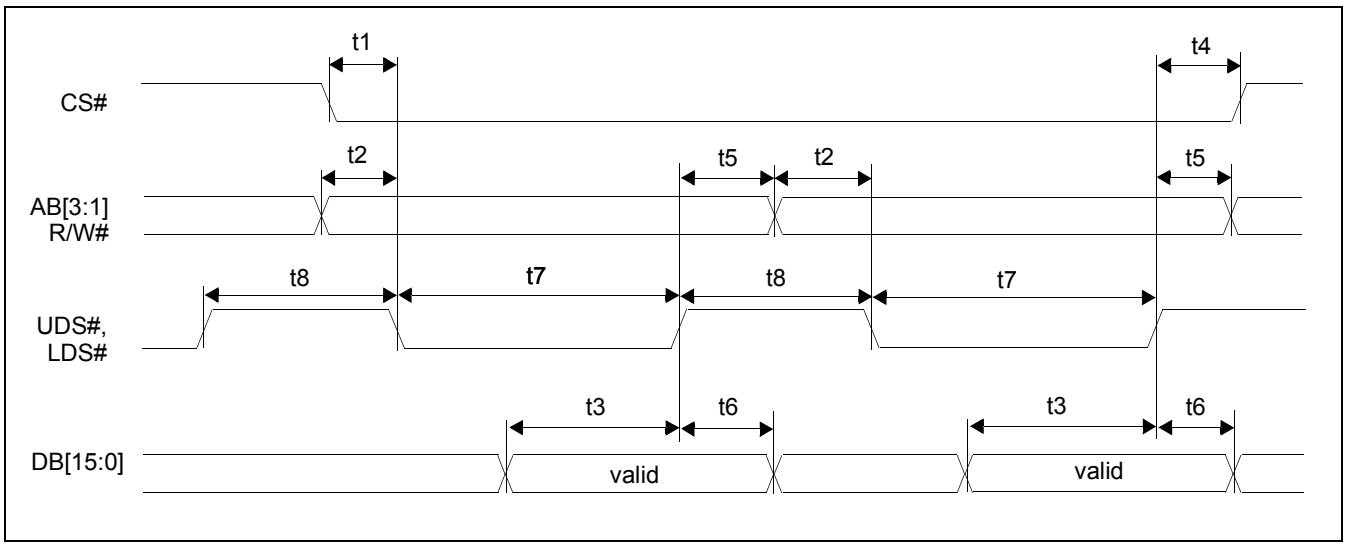


Figure 7-11: Indirect 68 Write Cycle Burst Access Timing

Note

The Indirect 68 interface write cycle timing included in this specification is preliminary and subject to change.

Table 7-7: Indirect 68 Write Cycle Timing

Symbol	Parameter	HIOVDD = 1.8V		HIOVDD = 2.8V or 3.3V		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	AB[3:1], R/W# setup time	5	—	5	—	ns
t3	DB[15:0] setup time to UDS#, LDS# rising edge	5	—	5	—	ns
t4	CS# hold time from UDS#, LDS# rising edge	5	—	5	—	ns
t5	AB[3:1], R/W# hold time from UDS#, LDS# rising edge	5	—	5	—	ns
t6	DB[15:0] hold time from UDS#, LDS# rising edge	5	—	5	—	ns
t7	UDS#, LDS# pulse active time	2	—	2	—	Ts (Note 1)
t8	UDS#, LDS# pulse inactive time	1	—	1	—	Ts

1. Ts = System Clock Period

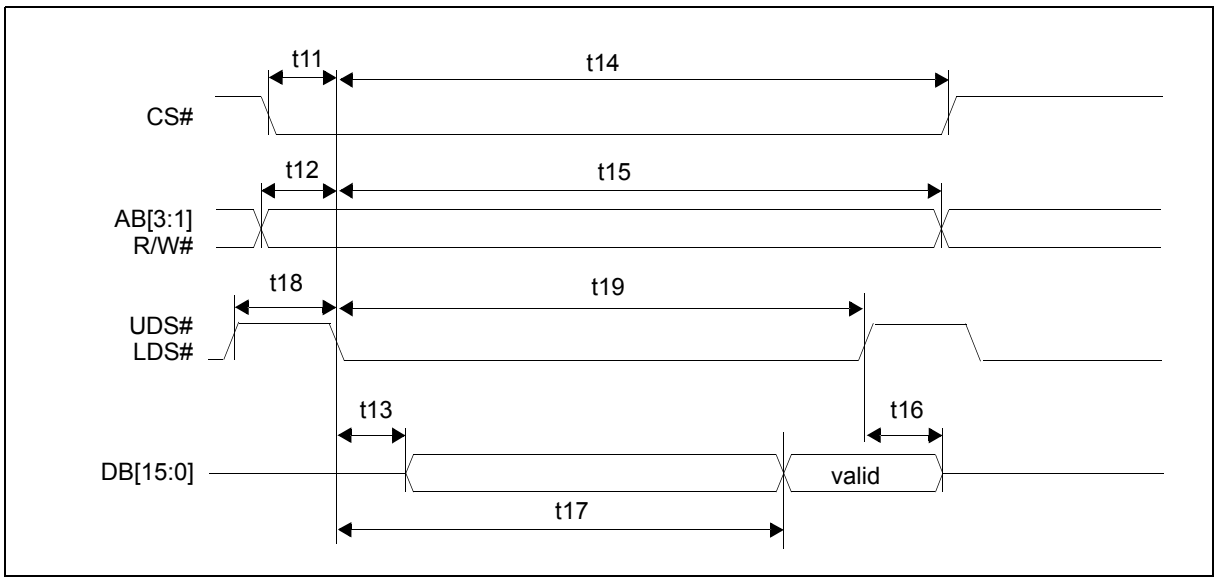


Figure 7-12: Indirect 68 Read Cycle Single Access Timing

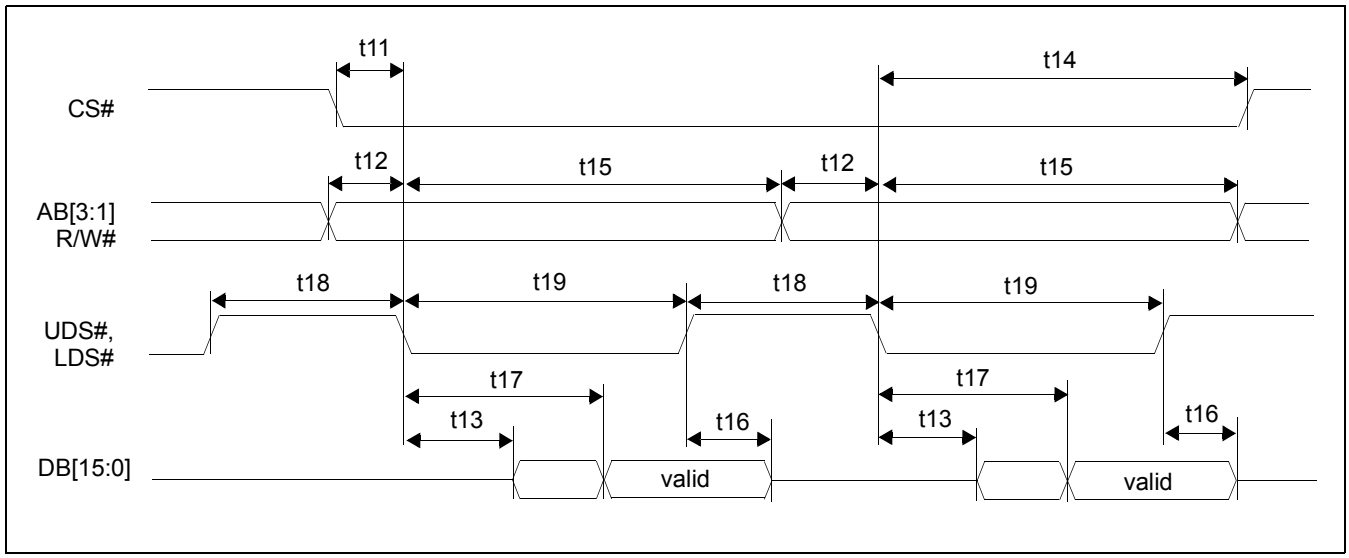


Figure 7-13: Indirect 68 Read Cycle Burst Access Timing

Note

The Indirect 68 interface read cycle timing included in this specification is preliminary and subject to change.

Table 7-8: Indirect 68 Read Cycle Timing

Symbol	Parameter	HIOVDD = 1.8V		HIOVDD = 2.8V or 3.3V		Units
		Min	Max	Min	Max	
t11	CS# setup time	5	—	5	—	ns
t12	AB[3:1], R/W# setup time	5	—	5	—	ns
t13	UDS#, LDS# falling edge to DB[15:0] driven	4	—	3	—	ns
t14	CS# hold time from UDS#, LDS# falling edge	1	—	1	—	Ts (Note 1)
t15	AB[3:1], R/W# hold time from UDS#, LDS# falling edge	1	—	1	—	Ts
t16	DB[15:0] hold time from UDS#, LDS# rising edge	2	11	2	10	ns
t17	UDS#, LDS# falling edge to valid data	—	27	—	22	ns
t18	UDS#, LDS# pulse inactive time	1	—	1	—	Ts
t19	UDS#, LDS# pulse active time	2	—	2	—	Ts

1. Ts = System Clock Period

7.4 LCD Interface Timing

7.4.1 Generic TFT Panel Timing

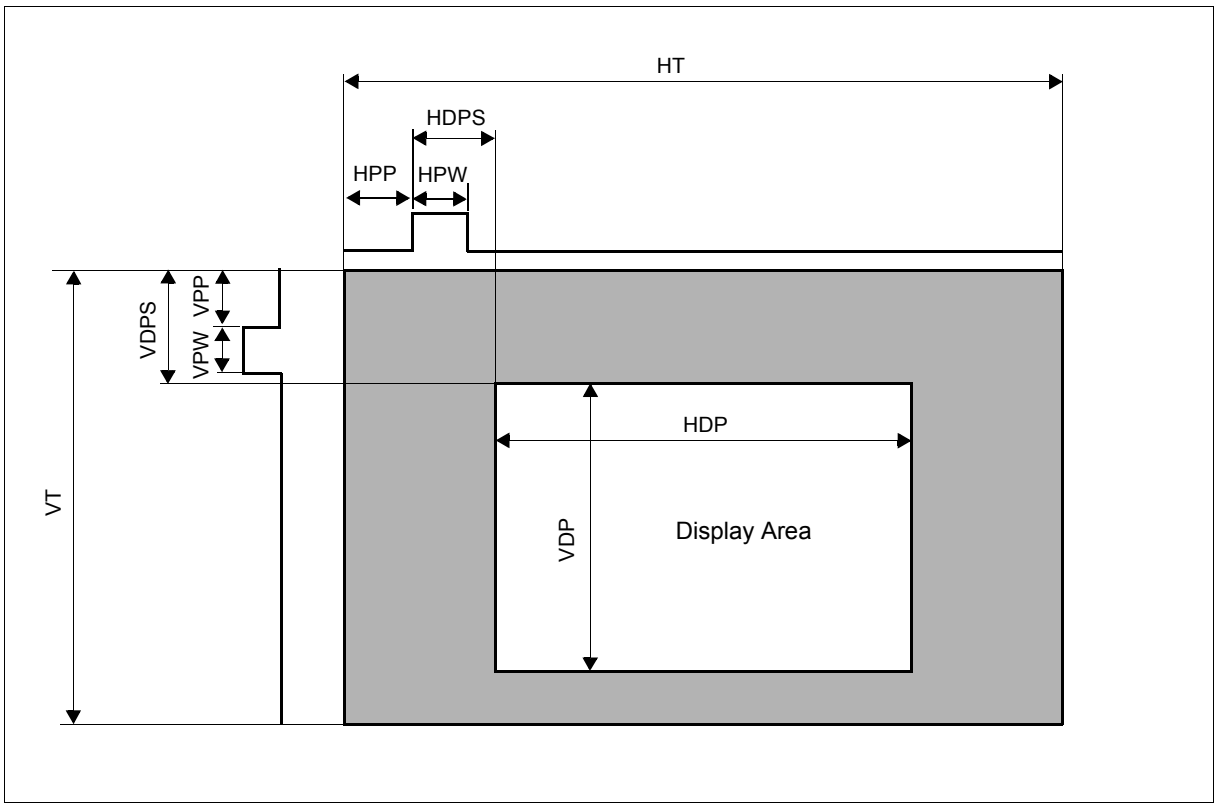


Figure 7-14: Generic TFT Panel Timing

Table 7-9: Generic TFT Panel Timing

Symbol	Description	Derived From	Units
HT	Horizontal Total (FPLINE period)	((REG[0040h] bits 6-0) + 1) x 8	PCLK
HDP	Horizontal Display Period	((REG[0042h] bits 8-0) + 1) x 2	
HDPS	Horizontal Display Period Start Position	((REG[0044h] bits 9-0) + 9	
HPW	Horizontal Pulse (FPLINE) Width	(REG[0046h] bits 6-0) + 1	
HPP	Horizontal Pulse (FPLINE) Start Position	(REG[0048h] bits 9-0) + 1	
VT	Vertical Total (FPFRAME period)	(REG[004Ah] bits 9-0) + 1	Lines
VDP	Vertical Display Period	(REG[004Ch] bits 9-0) + 1	
VDPS	Vertical Display Period Start Position	REG[004Eh] bits 9-0	
VPW	Vertical Pulse (FPFRAME) Width	(REG[0050h] bits 2-0) + 1	
VPP	Vertical Pulse (FPFRAME) Start Position	REG[0052h] bits 9-0	

1. The following formulas must be valid for all panel timings:
   HDPS + HDP < HT
   VDPS + VDP < VT

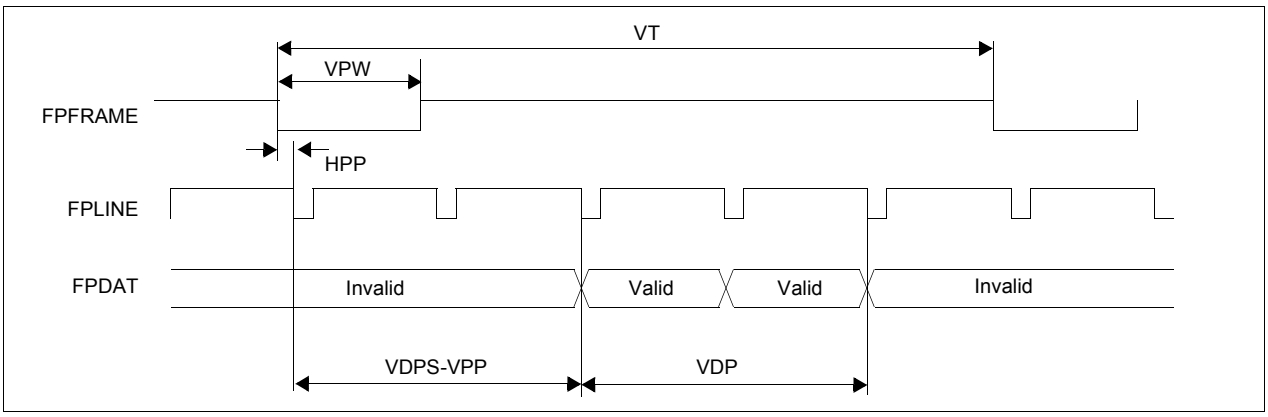


Figure 7-15: Generic TFT Vertical Timing

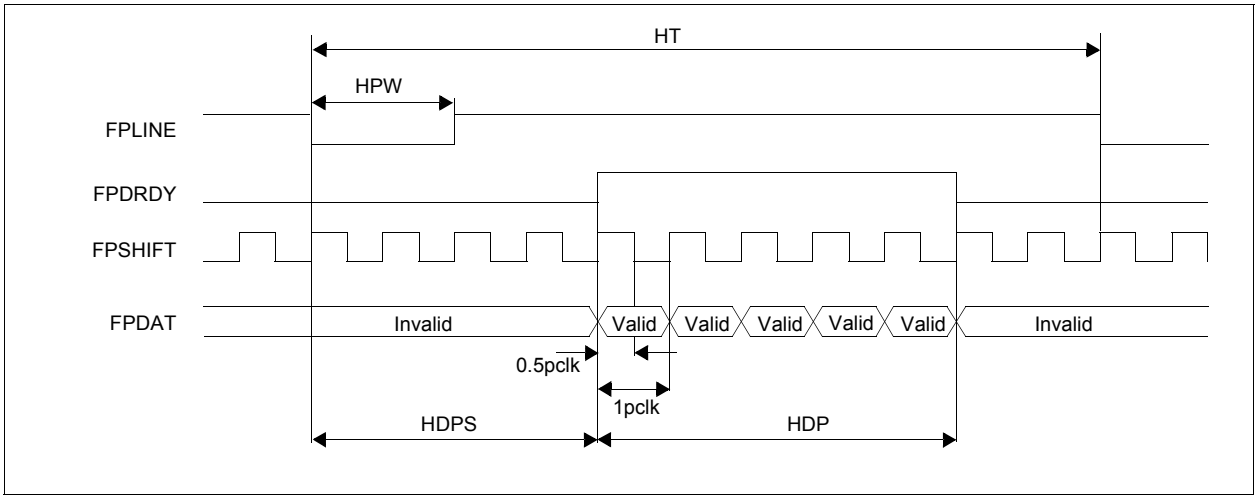


Figure 7-16: Generic TFT Horizontal Timing

8 Memory

8.1 Physical Memory

The S1D13L02 includes 1024K bytes of embedded SRAM. The SRAM consists of eight banks composed of 128K bytes. Each bank is mapped at consecutive addresses.

The memory is used for the display buffer which can contain image data for the following.

- Main1 window image data for LCD
- Main2 window image data for LCD
- PIP1 window image data for LCD
- PIP2 window image data for LCD

The following figure shows how the S1D13L02 physical memory is mapped.

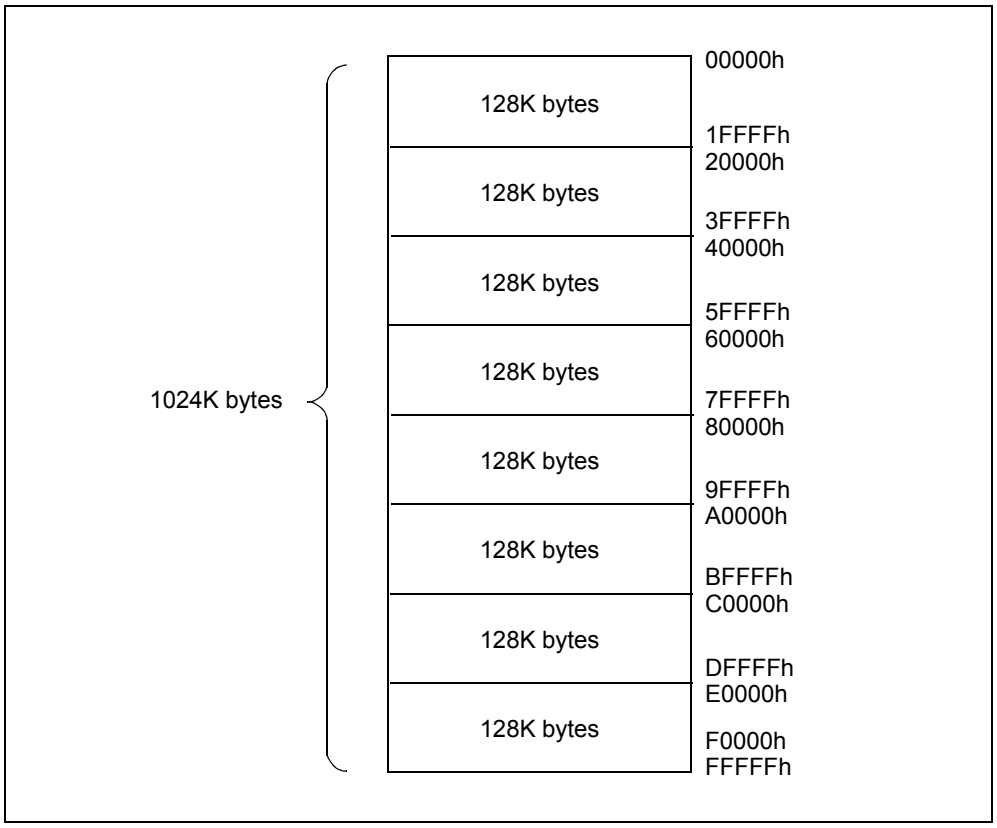


Figure 8-1: Physical Memory

8.2 Memory Map Examples

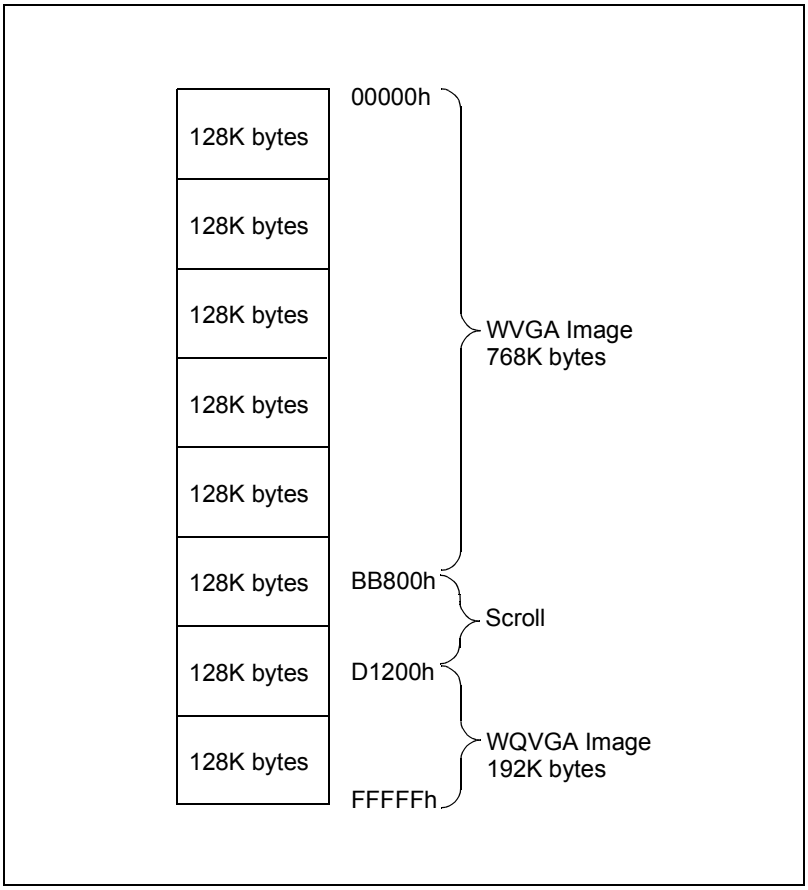


Figure 8-2: Memory Map for WVGA Display

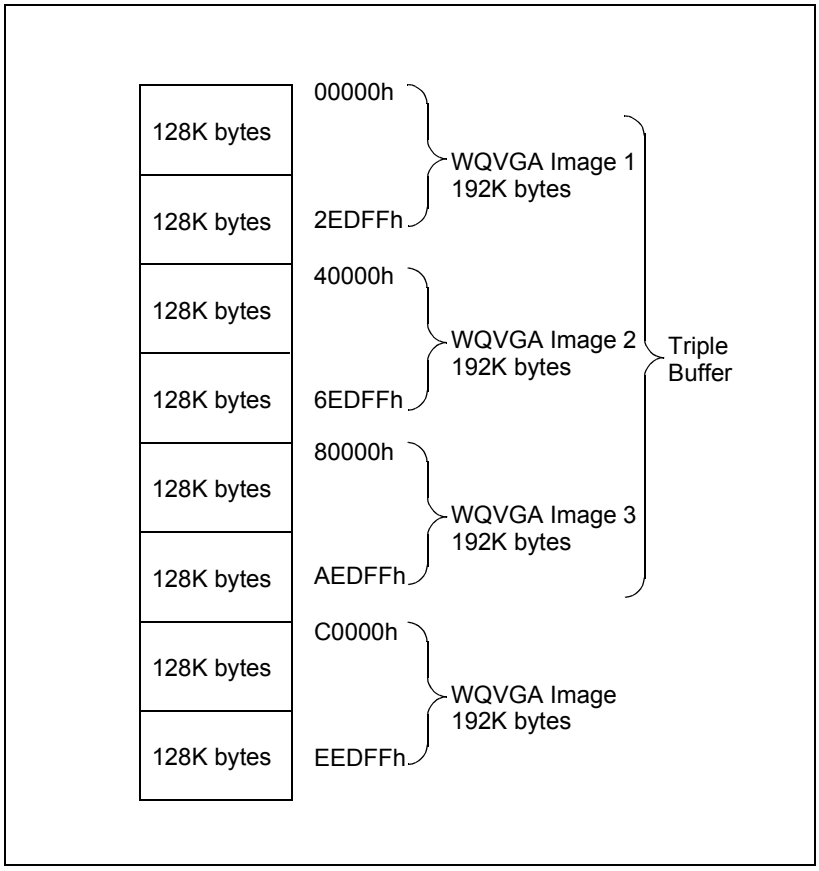


Figure 8-3: Memory Map for Triple-buffered WQVGA Display

9 Clocks

9.1 Clock Diagram

The following figure shows the clock tree of the S1D13L02. All required internal clocks are derived from the system clock (SYSCLK).

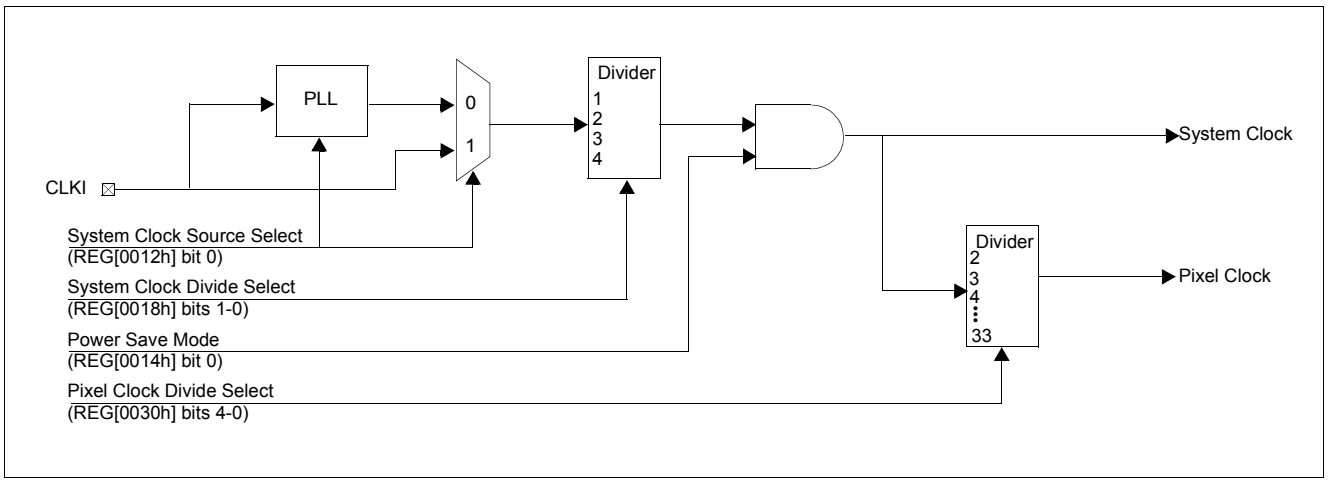


Figure 9-1: Clock Tree Diagram

9.2 Internal Clock Descriptions

9.2.1 System Clock

The system clock (SYSCLK) is used for the S1D13L02 internal main clock. The system clock source can be selected, using REG[0012h] bit 0, from either the internal PLL, or an external clock input (CLKI). The system clock source can be divided down using the System Clock Divide Select bits (REG[0018h] bits 1-0). The divided down system clock is the source clock for the Pixel Clock.

9.2.2 Pixel Clock

The pixel clock (PCLK) is used as the LCD shift clock for RGB type panels. The pixel clock source is always the system clock and can be divided down using the Pixel Clock Divide Select bits (REG[0030h] bits 4-0).

9.3 PLL

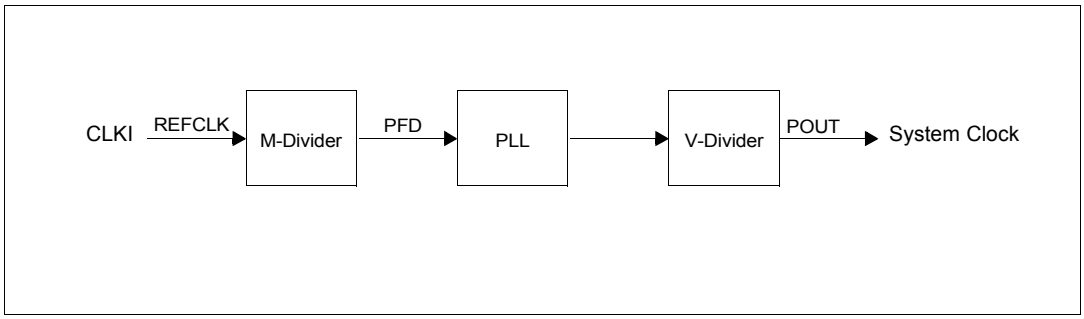


Figure 9-2: PLL Block Diagram

REFCLK input frequency	1MHz to 33MHz
PFD frequency	1MHz to 2MHz
POUT output frequency	33MHz to 58MHz
Period Jitter	± 2%
Lock in time	1ms
M-Divider divide ratio (REG[000Ch] bits 5-0)	1 to 1/33
PLL up convert ratio (REG[000Ch] bits 14-8)	17 to 33
V-Divider Divide ratio (REG[000Eh] bits 5-4)	1 or 1/2

10 Registers

This section discusses how and where to access the S1D13L02 registers. It also provides detailed information about the layout and usage of each register.

10.1 Register Mapping

The S1D13L02 registers are memory mapped. Asynchronous registers are accessible at all times. Synchronous registers are only available when power save mode is disabled, REG[0014h] bit 0 = 0b.

Table 10-1: S1D13L02 Register Mapping

Address	Type	Function
0000h to 0006h	Asynchronous	System Configuration Registers
000Ch to 0018h	Asynchronous	Clock Configuration Registers
0030h to 003Ch	Synchronous	LCD Interface Configuration Registers
0040h to 0064h	Synchronous	LCD Configuration Registers
0068h to 00FEh	Synchronous	Extended LCD Configuration Registers
0180h to 019Ah	Synchronous	Host Interface Registers
0200h to 0252h	Synchronous	Display Configuration Registers
0260h to 0292h	Synchronous	PIP1 Window Configuration Registers
02A0h to 02E2h	Synchronous	PIP2 Window Configuration Register
0300h to 031Ah	Asynchronous	GPIO Registers
0400h to 0502h	Synchronous	LUT Registers
0A00h to 0A04h	Synchronous	Interrupt Control Registers

10.2 Register Set

The S1D13L02 registers are listed in the following table.

Table 10-2: S1D13L02 Register Set

System Configuration Registers			
REG[0004h] Configuration Pin Status Register	56	REG[0006h] is Reserved	56
Clock Configuration Registers			
REG[000Ch] PLL Setting Register 0	57	REG[000Eh] PLL Setting Register 1	58
REG[0010h] PLL Setting Register 2	58	REG[0012h] PLL Setting Register 3	59
REG[0014h] Miscellaneous Configuration Register	60	REG[0016h] Software Reset Register	60
REG[0018h] System Clock Setting Register	61		
LCD Interface Configuration Registers			
REG[0030h] LCD Interface Clock Setting Register	62	REG[0032h] LCD Interface Configuration Register	63
LCD Configuration Registers			
REG[0040h] LCD Horizontal Total Register	65	REG[0042h] LCD Horizontal Display Period Register	65
REG[0044h] LCD Horizontal Display Period Start Position Register	65	REG[0046h] LCD Horizontal Pulse Register	66
REG[0048h] LCD Horizontal Pulse Start Position Register	66	REG[004Ah] LCD Vertical Total Register	66
REG[004Ch] LCD Vertical Display Period Register	66	REG[004Eh] LCD Vertical Display Period Start Position Register	67
REG[0050h] LCD Vertical Pulse Register	68	REG[0052h] LCD Vertical Pulse Start Position Register	68
REG[0068h] LCD Vsync Output Register	69		
Host Interface Registers			
REG[0180h] Host Interface Configuration Register	70	REG[0182h] Memory Start Address Register 0	72
REG[0184h] Memory Start Address Register 1	72	REG[0186h] HWC Memory Rectangular Write Address Offset Register	73
REG[0188h] HWC Memory Rectangular Write Horizontal Size Register	73	REG[018Ah] HWC Memory Rectangular Write Vertical Size Register	73
REG[018Ch] Memory Access Port Register	74	REG[018Eh] HWC Raw Status Register	74
REG[0190h] HWC Interrupt Control Register	75	REG[0192h] HWC Status Register	76
REG[0194h] Memory Rectangular Write Address Offset Register	77	REG[0196h] Memory Rectangular Write Address Width Register	77
REG[0198h] VOUT Configuration Register	78	REG[019Ah] is Reserved	
Display Configuration Registers			
REG[0200h] Display Mode Setting Register 0	80	REG[0202h] Display Mode Setting Register 1	81
REG[0204h] Transparency and Alpha Blend Control Register	84	REG[0206h] Background Color Setting Register	85
REG[0208h] Alpha Blend Ratio Setting Register	86	REG[020Ch] PIP1 Window Transparency Key Color Register	87
REG[020Eh] PIP2 Window Transparency Key Color Register	88	REG[0210h] Alpha Blend 1 Key Color Register	88
REG[0212h] Alpha Blend 2 Key Color Register	89	REG[0214h] Alpha Blend 3 Key Color Register	89
REG[0216h] Alpha Blend 4 Key Color Register	90	REG[0218h] Main1 Window X Start Position Register	90
REG[021Ah] Main1 Window Y Start Position Register	90	REG[0220h] Main2 Window X Start Position Register	91
REG[0222h] Main2 Window Y Start Position Register	91	REG[0228h] PIP1 Window X Start Position Register	91
REG[022Ah] PIP1 Window Y Start Position Register	91	REG[022Ch] PIP1 Window X End Position Register	92
REG[022Eh] PIP1 Window Y End Position Register	92	REG[0230h] PIP2 Window X Start Position Register	92
REG[0232h] PIP2 Window Y Start Position Register	93	REG[0234h] PIP2 Window X End Position Register	93
REG[0236h] PIP2 Window Y End Position Register	93	REG[0238h] Main1 Window Scroll Start Address Register 0	94
REG[023Ah] Main1 Window Scroll Start Address Register 1	94	REG[023Ch] Main1 Window Scroll End Address Register 0	95
REG[023Eh] Main1 Window Scroll End Address Register 1	95	REG[0240h] Main1 Window Display Start Address Register 0	96
REG[0242h] Main1 Window Display Start Address Register 1	96	REG[0244h] Main1 Window Line Address Offset Register	96
REG[0246h] Main1 Window Image Horizontal Size Register	97	REG[0248h] Main1 Window Image Vertical Size Register	97
REG[024Ah] Main2 Window Display Start Address Register 0	98	REG[024Ch] Main2 Window Display Start Address Register 1	98
REG[024Eh] Main2 Window Line Address Offset Register	98	REG[0250h] Main2 Window Image Horizontal Size Register	99
REG[0252h] Main2 Window Image Vertical Size Register	99		

Table 10-2: S1D13L02 Register Set

10.3 Register Restrictions

All reserved bits must be set to the default value. Writing a non-default value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect. Unless specified otherwise, all register bits are set to 0b during power-on reset.

Reserved registers must not be written.

For all register accesses, the Host must issue an index cycle except for the Memory Access Data Port (REG[018Ch]) which supports multiple data cycle burst accesses.

Some registers are only accessible when certain conditions exist. Any attempts to read/write in-accessible registers are invalid.

The following registers are asynchronous and always accessible.

- System Configuration Registers (REG[0004h])
- Clock Configuration Registers (REG[000Ch] ~ REG[0018h])
- GPIO Registers (REG[0300h] ~ REG[031Ah])

The following registers are synchronous and cannot be accessed when Power Save Mode is enabled (REG[0014h] bit 0 = 1b).

- All registers from REG[0030h] ~ REG[0A04h] except REG[0300h] ~ REG[031Ah]

For further information on performing read/write accesses to the S1D13L02 registers, see Section 14.2, “Register Access” on page 157.

Note

The register index must be set for each read cycle.

10.4 Register Descriptions

10.4.1 System Configuration Registers

REG[0004h] Configuration Pin Status Register
Default = 0000h — Read/Write

HIOVDD Interface Drive Level	PIOVDD Interface Drive Level	GPIOVDD Interface Drive Level	n/a				
15	14	13	12	11	10	9	8
n/a					CNF[2:0] Status		
7	6	5	4	3	2	1	0

bit 15 HIOVDD Interface Drive Level
This bit specifies the input/output buffer voltage level for the Host interface (HIOVDD) pins.
When this bit = 0b, HIOVDD is configured for 4.0mA/-4.0mA at 3.3V or 3.6mA/-3.6mA at 2.8V or 1.8mA/-1.8mA at 1.8V. (default)
When this bit = 1b, HIOVDD is configured for 12.0mA/-12.0mA at 3.3V or 10.8mA/-10.8mA at 2.8V or 5.4mA/-5-4mA at 1.8V.

bit 14 PIOVDD Interface Drive Level
This bit specifies the input/output buffer voltage level for the Panel interface (PIOVDD) pins.
When this bit = 0b, PIOVDD is configured for 4.0mA/-4.0mA at 3.3V or 3.6mA/-3.6mA at 2.8V or 1.8mA/-1.8mA at 1.8V. (default)
When this bit = 1b, PIOVDD is configured for 12.0mA/-12.0mA at 3.3V or 10.8mA/-10.8mA at 2.8V or 5.4mA/-5-4mA at 1.8V.

bit 13 GPIOVDD Interface Drive Level
This bit specifies the input/output buffer voltage level for the GPIO interface (GPIOVDD) pins.
When this bit = 0b, GPIOVDD is configured for 4.0mA/-4.0mA at 3.3V or 3.6mA/-3.6mA at 2.8V or 1.8mA/-1.8mA at 1.8V. (default)
When this bit = 1b, GPIOVDD is configured for 12.0mA/-12.0mA at 3.3V or 10.8mA/-10.8mA at 2.8V or 5.4mA/-5-4mA at 1.8V.

bits 2-0 CNF[2:0] Status (Read Only)
These bits indicate the status of the corresponding S1D13L02 configuration pins CNF[2:0] which are latched at the rising edge of RESET#. For functional description of each configuration pin, refer to Section 5.3, “Summary of Configuration Options” on page 22.

REG[0006h] is Reserved

This register is Reserved and should not be written.

10.4.2 Clock Configuration Registers

REG[000Ch] PLL Setting Register 0
Default = 0000h — Read/Write

n/a	L-Counter bits 6-0						
15	14	13	12	11	10	9	8
n/a	M-Divider bits 5-0						
7	6	5	4	3	2	1	0

bits 14-8 L-Counter bits [6:0]

These bits are used to configure the PLL Output (in MHz) and must be set according to the following formula.

$$\text{PLL Output} = (\text{L-Counter} + 1) \times \text{PLLCLK}$$
$$= \text{LL} \times \text{PLLCLK}$$

Where:
PLL Output is the desired PLL output frequency (in MHz)
L-Counter is the value of these bits (in decimal)
PLLCLK is the internal input clock to the PLL (in MHz)

Note
The L-Counter must be programmed such that the following formula is valid.
$10h \leq \text{L-Counter} \leq 41h$

bits 5-0 M-Divider bits [5:0]

These bits determine the divide ratio between CLKI and the actual input clock to the PLL. These bits must be set according to the frequency of CLKI to achieve an internal input clock to the PLL (PLLCLK) between 1 MHz and 2 MHz.

Table 10-3: M-Divide Ratio

REG[000Ch] bits 5-0	M-Divide Ratio
00h	1:1
01h	2:1
02h	3:1
03h	4:1
. . .	. .
20h	33:1
21h to 3Fh	Reserved

REG[000Eh] PLL Setting Register 1
Default = 0000h — Read/Write

n/a			HCP bits 4-0				
15	14	13	12	11	10	9	8
n/a		V bits 1-0		VC bits 3-0			
7	6	5	4	3	2	1	0

bits 12-8 HCP bits [4:0]
These bits specify the HCP value used for configuring the PLL. For a PLL output between 33-58MHz, these bits should be set to 0_0000b.

bits 5-4 V bits [1:0]
These bits specify the V value used for configuring the PLL. For a PLL output between 33-58MHz, these bits should be set to 00b.

bits 3-0 VC bits [3:0]
These bits specify the VC value used for configuring the PLL. For a PLL output between 33-58MHz, these bits should be set to 0010b.

REG[0010h] PLL Setting Register 2
Default = 0000h — Read/Write

HLOCK	X2	HG	OSCS	RS bits 3-0			
15	14	13	12	11	10	9	8
n/a			CP bits 4-0				
7	6	5	4	3	2	1	0

bit 15 HLOCK
This bit specifies the HLOCK value used for configuring the PLL. For a PLL output between 33-58MHz, this bit should be set to 0b.

bit 14 X2
This bit specifies the X2 value used for configuring the PLL. For a PLL output between 33-58MHz, this bit should be set to 0b.

bit 13 HG
This bit specifies the HG value used for configuring the PLL. For a PLL output between 33-58MHz, this bit should be set to 0b.

bit 12 OSCS
This bit specifies the OSCS value used for configuring the PLL. For a PLL output between 33-58MHz, this bit should be set to 0b.

bits 11-8 RS bits [3:0]
These bits specify the RS value used for configuring the PLL. For a PLL output between 33-58MHz, these bits should be set to 1000b.

bits 4-0 CP bits [4:0]
These bits specify the CP value used for configuring the PLL. For a PLL output between 33-58MHz, these bits should be set to 1_0000b.

REG[0012h] PLL Setting Register 3
Default = 0001h — Read/Write

15	14	13	12	11	10	9	8
n/a							CLKI Input Control
7	6	5	4	3	2	1	0
n/a							System Clock Source Select

Note
Before setting these bits, power save mode must be enabled (REG[0014h] bit 0 = 1b).

bit 8 CLKI Input Control

When the PLL is disabled (REG[0012h] bit 0 = 1b), this bit allows the CLKI input to be stopped for power save considerations. In this condition CLKI may be left at high impedance.
When this bit = 0b, the CLKI input is enabled when the PLL is disabled.
When this bit = 1b, the CLKI input is disabled when the PLL is disabled.

bit 0 System Clock Source Select

This bit controls the internal PLL and determines the source for the System Clock (SYSCLK). A PLL reference clock must be supplied and the PLL must be configured using the PLL Setting Registers (REG[000Ch] ~ REG[0010h]) before enabling this bit. For details on the clock structure, refer to Section 9, “Clocks” on page 50.
When this bit = 0b, the PLL is enabled and uses the CLKI input as the PLL reference clock. When this option is selected, the PLL output is the source for the system clock divider.
When this bit = 1b, the PLL is disabled (default). When this option is selected the external clock (CLKI) is the source for the system clock divider.

Note
1. A CLKI source (external CLKI or PLL reference clock) is required in order to change this bit.
2. If the PLL reference clock (CLKI input) is to be stopped, a 100us delay must be observed after disabling the PLL, REG[0012h] bit 0 = 1b.
3. There may be up to a 1ms delay before the PLL output becomes stable. The S1D13L02 must not be accessed during this time.

REG[0014h] Miscellaneous Configuration Register
Default = 04D1h — Read/Write

Reserved							
15	14	13	12	11	10	9	8
VNDP Status (RO)	Memory Power Save Status (RO)	n/a	Reserved		n/a		Power Save Mode Enable
7	6	5	4	3	2	1	0

bits 15-8 Reserved

The default value for these bits is 04h and should not be changed.

bit 7 Vertical Non-Display Period Status (Read Only)
This status bit indicates whether the panel is in a Vertical Non-Display Period.

When this bit = 0b, the LCD panel output is in a Vertical Display Period.
When this bit = 1b, the LCD panel output is in a Vertical Non-Display Period.

bit 6 Memory Power Save Status (Read Only)
This bit indicates the status of the memory controller and must be checked before enabling Power Save Mode (REG[0014h] bit 0) or disabling the PLL (REG[0012h] bit 0).
When this bit = 0b, the memory controller is powered up.
When this bit = 1b, the memory controller is idling and the system clock source can be disabled.

bits 4-3 Reserved

The default value for these bits is 10b and should not be changed.

bit 0 Power Save Mode Enable
This bit controls the state of the software initiated power save mode. When power save mode is disabled, the S1D13L02 is operating normally. When power save mode is enabled, the S1D13L02 is in a power efficient state.
When this bit = 0b, power save mode is disabled.
When this bit = 1b, power save mode is enabled (default).

Note
Before enabling power save mode, the Display Output Port must be turned off (REG[0202h] bit 10 = 0b) and the Memory Controller Idle Status bit (REG[0014h] bit 6) must return a 1b.

REG[0016h] Software Reset Register
Default = not applicable — Write Only

Software Reset bits 15-8							
15	14	13	12	11	10	9	8
Software Reset bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Software Reset bits [15:0] (Write Only)
When any value is written to these bits, all registers except REG[0000h] ~ REG[0018h] and REG[0300h] ~ REG[031Ah] are reset to their default values. A software reset using these bits does not clear the display buffer.

REG[0018h] System Clock Setting Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a						System Clock Divide Select bits 1-0	
7	6	5	4	3	2	1	0

bits 1-0 System Clock Divide Select bits [1:0]
These bits determine the divide ratio for the system clock. For details on the clock structure, refer to Section 9, “Clocks” on page 50.

Table 10-4: System Clock Divide Ratio Selection

REG[0018h] bits 1-0	System Clock Divide Ratio
00b	1:1
01b	2:1
10b	3:1
11b	4:1

Note
When the System Clock divide ratio is not 1:1 (REG[0018h] bits 1-0 ≠ 00b), odd integer Pixel Clock divide ratios are not supported (see REG[0030h] bits 4-0). For example, if a 2:1 System Clock divide ratio is selected, a Pixel Clock divide ratio of 3:1 is not supported.

10.4.3 LCD Interface Configuration Registers

REG[0030h] LCD Interface Clock Setting Register
Default = 0000h — Read/Write

n/a					Reserved		
15	14	13	12	11	10	9	8
n/a			Pixel Clock Divide Select bits 4-0				
7	6	5	4	3	2	1	0

bits 10-8 Reserved

bits 4-0 Pixel Clock Divide Select bits [4:0]
These bits specify the divide ratio for the pixel clock. The clock source for the pixel clock is the system clock. The pixel clock is the same as the shift clock. For details on the clock structure, refer to Section 9, “Clocks” on page 50.

Table 10-5: Pixel Clock Divide Ratio Selection

REG[0030h] bits 4-0	Pixel Clock Divtio	REG[0030h] bits 4-0	Pixel Clock Divide Ratio
00000b	2:1	10000b	18:1
00001b	3:1	10001b	19:1
00010b	4:1	10010b	20:1
00011b	5:1	10011b	21:1
00100b	6:1	10100b	22:1
00101b	7:1	10101b	23:1
00110b	8:1	10110b	24:1
00111b	9:1	10111b	25:1
01000b	10:1	11000b	26:1
01001b	11:1	11001b	27:1
01010b	12:1	11010b	28:1
01011b	13:1	11011b	29:1
01100b	14:1	11100b	30:1
01101b	15:1	11101b	31:1
01110b	16:1	11110b	32:1
01111b	17:1	11111b	33:1

Note
When the System Clock divide ratio is not 1:1 (REG[0018h] bits 1-0 ≠ 00b), odd integer Pixel Clock divide ratios are not supported. For example, if a 2:1 System Clock divide ratio is selected, a Pixel Clock divide ratio of 3:1 is not supported.

REG[0032h] LCD Interface Configuration Register
Default = 0000h Read/Write

Reserved						FPDRDY Polarity Select	Reserved
15	14	13	12	11	10	9	8
FPSHIFT Polarity Select	RGB Interface Panel Data Bus Width bits 2-0			n/a		Reserved	
7	6	5	4	3	2	1	0

bits 15-10 Reserved
The default value for these bits is 00_0000b and should not be changed.

bit 9 FPDRDY Polarity Select
This bit sets the polarity of the data ready signal (FPDRDY) for RGB type panels.
When this bit = 0b, the FPDRDY signal is not reversed.
When this bit = 1b, the FPDRDY signal is reversed.

bit 8 Reserved

The default value for this bits is 0b and should not be changed.

bit 7 FPSHIFT Polarity Select
This bit sets the polarity of the shift clock for RGB type panels (inverts FPSHIFT).
When this bit = 0b, all panel interface signals change at the rising edge of FPSHIFT.
When this bit = 1b, all panel interface signals change at the falling edge of FPSHIFT.

bits 6-4 RGB Interface Panel Data Bus Width bits [2:0]

These bits determine the RGB Interface Panel Data Bus size. Un-used pins are forced low. For LCD interface pin mapping, see Section 5.5, “LCD Interface Pin Mapping” on page 24 and Section 15.1, “RGB Interface Data Formats” on page 174.

Table 10-6: RGB Interface Panel Data Bus Width Selection

REG[0032h] bits 6-4	RGB Interface Panel Data Bus Width
000b	9-bit
001b	12-bit
010b	16-bit
011b	18-bit
100b	24-bit
101b ~ 111b	Reserved

bits 1-0 Reserved

The default value for these bits is 00b and should not be changed.

10.4.4 LCD Configuration Registers

REG[0040h] LCD Horizontal Total Register
Default = 0001h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a	LCD Horizontal Total bits 6-0						

bits 6-0 LCD Horizontal Total bits [6:0]

These bits specify the Horizontal Total (FPLINE period) for LCD, in 8 pixel resolution. The Horizontal Total is the sum of the Horizontal Display Period and the Horizontal Non-Display Period. These bits must not be set to 0.

REG[0040h] bits 6-0 = (Horizontal Total in pixels ÷ 8) - 1

Note

These bits must be programmed such that the following are valid.

REG[0040h] bits 6-0 > 0

HT ≥ HDP + HNDP

REG[0042h] LCD Horizontal Display Period Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							LCDHDP bit 8
7	6	5	4	3	2	1	0
LCD Horizontal Display Period bits 7-0							

bits 8-0 LCD Horizontal Display Period bits [8:0]

These bits specify the Horizontal Display Period for LCD, in 2 pixel resolution. The Horizontal Display Period must be less than the Horizontal Total to allow for sufficient Horizontal Non-Display Period.

REG[0042h] bits 8-0 = (Horizontal Display Period in pixels ÷ 2) - 1

Note

1. These bits must be programmed such that the following formula is valid.
   HT ≥ HDP + HNDP

REG[0044h] LCD Horizontal Display Period Start Position Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						LCD Horizontal Display Period bits 9-8	
7	6	5	4	3	2	1	0
LCD Horizontal Display Period bits 7-0							

bits 9-0 LCD Horizontal Display Period Start Position bits [9:0]

These bits specify the Horizontal Display Period Start Position for LCD, in pixels.

REG[0044h] bits 9-0 = Horizontal Display Period Start Position in pixels - 9

REG[0046h] LCD Horizontal Pulse Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LCD Horizontal Pulse Polarity	LCD Horizontal Pulse Width bits 6-0						

bit 7 LCD Horizontal Pulse Polarity
This bit selects the polarity of the horizontal sync signal (FPLINE).
When this bit = 0b, the horizontal sync signal (FPLINE) is active low. (default)
When this bit = 1b, the horizontal sync signal (FPLINE) is active high.

bits 6-0 LCD Horizontal Pulse Width bits [6:0]
These bits specify the pulse width of the horizontal sync signal (FPLINE) for LCD, in pixels.
REG[0046h] bits 6-0 = Horizontal Pulse Width in pixels - 1

REG[0048h] LCD Horizontal Pulse Start Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						LCD Horizontal Pulse Start Position bits 9-8	
7	6	5	4	3	2	1	0
LCD Horizontal Pulse Start Position bits 7-0							

bits 9-0 LCD Horizontal Pulse Start Position bits [9:0]
These bits specify the start position of the horizontal sync pulse (FPLINE) for LCD, in pixels.
REG[0048h] bits 9-0 = FPFRAME edge to FPLINE edge in pixels - 1

REG[004Ah] LCD Vertical Total Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						LCD Vertical Total bits 9-8	
7	6	5	4	3	2	1	0
LCD Vertical Total bits 7-0							

bits 9-0 LCD Vertical Total bits [9:0]
These bits specify the Vertical Total (FPFRAME period) for LCD in lines. The Vertical Total is the sum of the Vertical Display Period and the Vertical Non-Display Period.
REG[004Ah] bits 9-0 = Vertical Total in lines - 1

REG[004Ch] LCD Vertical Display Period Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						LCD Vertical Display Period bits 9-8	
7	6	5	4	3	2	1	0
LCD Vertical Display Period bits 7-0							

bits 9-0 LCD Vertical Display Period bits [9:0]

These bits specify the Vertical Display period for LCD, in lines. The Vertical Display Period must be less than the Vertical Total to allow for a sufficient Vertical Non-Display period.

REG[004Ch] bits 9-0 = Vertical Display Period in lines - 1

REG[004Eh] LCD Vertical Display Period Start Position Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						LCD Vertical Display Period Start Position bits 9-8	
LCD Vertical Display Period Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 LCD Vertical Display Period Start Position bits [9:0]

These bits specify the Vertical Display Period Start Position for LCD in lines.

REG[004Eh] bits 9-0 = Vertical Display Period Start Position in lines

REG[0050h] LCD Vertical Pulse Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
LCD Vertical Pulse Polarity	n/a			Reserved	LCD Vertical Pulse Width bits 2-0		
7	6	5	4	3	2	1	0

bit 7 LCD Vertical Pulse Polarity
This bit selects the polarity of the vertical sync signal (FPFRAME).
When this bit = 0b, the vertical sync signal (FPFRAME) is active low. (default)
When this bit = 1b, the vertical sync signal (FPFRAME) is active high.

bit 3 Reserved
The default value for this bit is 0b.

bits 2-0 LCD Vertical Pulse Width bits [2:0]
These bits specify the pulse width of the vertical sync signal (FPFRAME), in lines.
REG[0050h] bits 2-0 = Vertical Pulse Width in lines - 1

REG[0052h] LCD Vertical Pulse Start Position Register
Default = 0000h Read/Write

n/a						LCD Vertical Pulse Start Position bits 9-8	
15	14	13	12	11	10	9	8
LCD Vertical Pulse Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 LCD Vertical Pulse Start Position bits [9:0]
These bits specify the start position of the vertical sync pulse (FPFRAME), in lines.
REG[0052h] bits 9-0 = Vertical Pulse Start Position in lines

REG[0058h] through REG[0064h] are Reserved

These registers are Reserved and should not be written.

10.4.5 Extended LCD Configuration Registers

REG[0068h] LCD Vsync Output Register
Default = 0000h — Read/Write

LCD Vsync Width bits 15-8							
15	14	13	12	11	10	9	8
LCD Vsync Position bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 LCD Vsync Width bits [7:0]
REG[0056h] bit 15 = 1b. These bits determine the width of VSYNC for LCD, in PCLKs.
REG[0068h] bits 15-8 = LCD VSYNC Width ÷ 2

bits 7-0 LCD Vsync Position bits [7:0]
REG[0056h] bit 15 = 1b. These bits determine the position of VSYNC for LCD, in PCLKs.
REG[0068h] bits 7-0 = LCD VSYNC Position ÷ 2

REG[006Ah] is Reserved

This register is Reserved and should not be written.

REG[0070h] through REG[0074h] are Reserved

These registers are Reserved and should not be written.

REG[00FEh] is Reserved

This register is Reserved and should not be written.

10.4.6 Host Interface Registers

REG[0180h] Host Interface Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
HWC Software Reset (WO)	n/a						

7	6	5	4	3	2	1	0
Host Interface HWC Data Port Active	reserved		HWC Data Bus Swap Enable	HWC Mirror Enable	HWC Rotation Mode Select bits 1-0		HWC Module Enable

bit 15 HWC Software Reset (Write Only)

This bit initiates a software reset of the Host interface Write Controller (HWC) module.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit initiates a software reset of the HWC module.

Note
If a software reset of the HWC is performed using this bit, the HWC Module is disabled (REG[0180h] bit 0 = 0b).

bits 7 Host Interface HWC Data Port Active

This bit only have an effect when the HWC module is enabled, REG[0180h] bit 0 = 1b.

When the Host Interface HWC Data Port Active = 1b, HWC function is available.

When the Host Interface HWC Data Port Active = 0b, HWC function is not available.

bits 6-5 Reserved

These bit should be set 00b.

bit 4 HWC Data Bus Swap Enable

This bit only has an effect when the HWC module is enabled, REG[0180h] bit 0 = 1b.

This bit controls how the Host interface Write Controller (HWC) receives data from the Host.

When this bit = 0b, data from the Host goes straight into the HWC.

When this bit = 1b, data from the Host has the upper and lower bytes "swapped" before going into the HWC.

Table 10-7: HWC Data Bus Swap Selection

REG[0180h] bit 4	Data into the HWC
0b	DB[15:0]
1b	DB[7:0], DB[15:8]

bit 3 HWC Mirror Enable

This bit only has an effect when the HWC module is enabled, REG[0180h] bit 0 = 1b.

This bit determines whether a horizontal "mirror" effect is applied to Host interface memory writes by the Host interface Write Controller (HWC). For further information see Section 14.3, "Memory Access Using the HWC" on page 161.

When this bit = 0b, Host interface memory writes are not mirrored.

When this bit = 1b, Host interface memory writes are mirrored.

bits 2-1 HWC Rotation Mode Select bits [1:0]

These bits only have an effect when the HWC module is enabled, REG[0180h] bit 0 = 1b. These bits select the clockwise rotation applied to Host interface memory writes by the Host interface Write Controller (HWC). For further information, see Section 14.3, "Memory Access Using the HWC" on page 161.

Table 10-8: Rotation Mode Selection

REG[0180h] bits 2-1	Rotation Mode
00b (default)	0° (Normal)
01b	90°
10b	180°
11b	270°

bit 0 HWC Module Enable

This bit controls the Host interface Write Controller (HWC) module. The HWC allows writing a rectangular memory area and supports optional rotation (see REG[0180h] bits 2-1) and mirror (see REG[0180h] bit 3) functions. To allow the Host interface to directly access the memory, this bit must set to 0b.

When this bit = 0b, the HWC module is disabled and memory is accessed directly.

When this bit = 1b, the HWC module is enabled and used by the Host for memory writes.

Note

If a software reset of the HWC is performed using REG[0180h] bit 15, the HWC Module is disabled (REG[0180h] bit 0 = 0b).

REG[0182h] Memory Start Address Register 0
Default = 0000h — Read/Write

Memory Start Address bits 15-8							
15	14	13	12	11	10	9	8
Memory Start Address bits 7-1							Read/Write Cycle
7	6	5	4	3	2	1	0

REG[0184h] Memory Start Address Register 1
Default = 0000h — Read/Write

Direct Memory Access Mode	n/a						
15	14	13	12	11	10	9	8
n/a				Memory Start Address bits 19-16			
7	6	5	4	3	2	1	0

REG[0182h] bit 15-1
REG[0184h] bit 3-0 Memory Start Address bits [19:1]

These bits determine the memory start address for each memory access. After a completed memory access, these bits are incremented automatically.

Note

1. When the HWC is enabled (REG[0180h] bit 0 = 1b), the memory start address must be set according to the selected Mirror (REG[0180h] bit 3) and Rotation Mode (REG[0180h] bits 2-1) settings. Examples for each combination are shown in Section 14.3, “Memory Access Using the HWC” on page 161.
2. REG[0184h] must be set before REG[0182h].

REG[0182h] bit 0 Read/Write Cycle

This bit determines whether a memory read or write operation takes place.
When this bit = 0b, a write operation takes place. (default)
When this bit = 1b, a read operation takes place.

REG[0184h] bit 15 Direct Memory Access Mode

If the HWC Module is enabled (REG[0180h] bit 0 = 1b), this bit has no effect.
This bit selects the address mode for direct memory accesses.
When this bit = 0b, linear memory address mode is selected.
When this bit = 1b, rectangular memory address mode is selected (see REG[0194h] and REG[0196h]).

Note

The Memory Rectangular Write Address Offset (REG[0194h]) and Memory Rectangular Write Address Width (REG[0196h] must be configured before selecting rectangular memory address mode.

REG[0186h] HWC Memory Rectangular Write Address Offset Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a				HWC Memory Rectangular Write Address Offset bits 11-8			
7	6	5	4	3	2	1	0
HWC Memory Rectangular Write Address Offset bits 7-1							n/a

bits 11-1 HWC Memory Rectangular Write Address Offset bits [11:1]
These bits only have an effect when the HWC module is enabled, REG[0180h] bit 0 = 1b. These bits determine the memory address offset used by the Host interface Write Controller (HWC) module.

REG[0188h] HWC Memory Rectangular Write Horizontal Size Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						HWC Memory Rectangular Write Horizontal Size bits 9-8	
7	6	5	4	3	2	1	0
HWC Memory Rectangular Write Horizontal Size bits 7-1							n/a

bits 9-1 HWC Memory Rectangular Write Horizontal Size bits [9:1]
These bits only have an effect when the HWC module is enabled, REG[0180h] bit 0 = 1b. These bits determine the horizontal size used by the Host interface Write Controller (HWC) module, in pixels.

REG[0188h] bits 9-1 = HWC Memory Rectangular Write Horizontal Size in pixels - 2

REG[018Ah] HWC Memory Rectangular Write Vertical Size Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						HWC Memory Rectangular Write Vertical Size bits 9-8	
7	6	5	4	3	2	1	0
HWC Memory Rectangular Write Vertical Size bits 7-0							

bits 9-0 HWC Memory Rectangular Write Vertical Size bits [9:0]
These bits only have an effect when the HWC module is enabled, REG[0180h] bit 0 = 1b. These bits determine the vertical size used by the Host interface Write Controller (HWC) module is enabled (REG[0180h] bit 0 = 1b).

REG[018Ah] bits 9-0 = HWC Memory Rectangular Write Vertical Size in pixels - 1

Note
When the HWC is configured for 90° or 270° write mode (REG[0180h] bits 2-1 = 01b or 11b), these bits must be programmed to an even value.

REG[018Ch] Memory Access Port Register
Default = not applicable — Read/Write

Memory Access Port bits 15-8							
15	14	13	12	11	10	9	8
Memory Access Port bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Memory Access Port bits [15:0]
These bits are the memory read/write port for the Indirect Host Interface.

REG[018Eh] HWC Raw Status Register
Default = 0000h — Read Only

n/a							
15	14	13	12	11	10	9	8
n/a			Memory Access Write Error Raw Status	Memory Access Read Error Raw Status	HWC Overwrite Error Raw Status	HWC Access Timeout Raw Status	HWC Access Complete Raw Status
7	6	5	4	3	2	1	0

bit 4 Memory Access Write Error Raw Status (Read Only)
This bit indicates the raw status of the Memory Access Write Error interrupt. This bit is not masked by the Memory Access Write Error Interrupt Enable bit, REG[0190h] bit 4.
When this bit = 0b, the Memory Access Write Error interrupt has not occurred.
When this bit = 1b, the Memory Access Write Error interrupt has occurred.

To clear this bit, write a 1b to REG[0192h] bit 4.

bit 3 Memory Access Read Error Raw Status (Read Only)
This bit indicates the raw status of the Memory Access Read Error interrupt. This bit is not masked by the Memory Access Read Error Interrupt Enable bit, REG[0190h] bit 3.
When this bit = 0b, the Memory Access Read Error interrupt has not occurred.
When this bit = 1b, the Memory Access Read Error interrupt has occurred.

To clear this bit, write a 1b to REG[0192h] bit 3.

bit 2 HWC Overwrite Error Raw Status (Read Only)
This bit indicates the raw status of the HWC Overwrite Error interrupt. This bit is not masked by the HWC Overwrite Error Interrupt Enable bit, REG[0190h] bit 2.
When this bit = 0b, the HWC Overwrite Error interrupt has not occurred.
When this bit = 1b, the HWC Overwrite Error interrupt has occurred.

To clear this bit, write a 1b to REG[0192h] bit 2.

bit 1 HWC Access Timeout Raw Status (Read Only)
This bit indicates the raw status of the HWC Access Timeout interrupt. This bit is not masked by the HWC Access Timeout Interrupt Enable bit, REG[0190h] bit 1.
When this bit = 0b, the HWC Access Timeout interrupt has not occurred.
When this bit = 1b, the HWC Access Timeout interrupt has occurred.

To clear this bit, write a 1b to REG[0192h] bit 1.

bit 0 HWC Access Complete Raw Status (Read Only)
This bit indicates the raw status of the HWC Access Complete interrupt. This bit is not masked by the HWC Access Complete Interrupt Enable bit, REG[0190h] bit 0.
When this bit = 0b, the HWC Access Complete interrupt has not occurred.
When this bit = 1b, the HWC Access Complete interrupt has occurred.

To clear this bit, write a 1b to REG[0192h] bit 0.

REG[0190h] HWC Interrupt Control Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a			Memory Access Write Error Interrupt Enable	Memory Access Read Error Interrupt Enable	HWC Overwrite Error Interrupt Enable	HWC Access Timeout Interrupt Enable	HWC Access Complete Interrupt Enable
7	6	5	4	3	2	1	0

bit 4 Memory Access Write Error Interrupt Enable
This bit controls the Memory Access Write Error interrupt. The status of this interrupt is indicated by the Memory Access Write Error Status bit, REG[0192h] bit 4.
When this bit = 0b, the Memory Access Write Error interrupt is disabled.
When this bit = 1b, the Memory Access Write Error interrupt is enabled.

bit 3 Memory Access Read Error Interrupt Enable
This bit controls the Memory Access Read Error interrupt. The status of this interrupt is indicated by the Memory Access Read Error Status bit, REG[0192h] bit 3.
When this bit = 0b, the Memory Access Read Error interrupt is disabled.
When this bit = 1b, the Memory Access Read Error interrupt is enabled.

bit 2 HWC Overwrite Error Interrupt Enable
This bit controls the HWC Overwrite Error interrupt. The status of this interrupt is indicated by the HWC Overwrite Error Status bit, REG[0192h] bit 2.
When this bit = 0b, the HWC Overwrite Error interrupt is disabled.
When this bit = 1b, the HWC Overwrite Error interrupt is enabled.

bit 1 HWC Access Timeout Interrupt Enable
This bit controls the HWC Access Timeout interrupt. The status of this interrupt is indicated by the HWC Access Timeout Status bit, REG[0192h] bit 1.
When this bit = 0b, the HWC Access Timeout interrupt is disabled.
When this bit = 1b, the HWC Access Timeout interrupt is enabled.

bit 0 HWC Access Complete Interrupt Enable
This bit controls the HWC Access Complete interrupt. The status of this interrupt is indicated by the HWC Access Complete Status bit, REG[0192h] bit 0.
When this bit = 0b, the HWC Access Complete interrupt is disabled.
When this bit = 1b, the HWC Access Complete interrupt is enabled.

REG[0192h] HWC Status Register
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a			Memory Access Write Error Status	Memory Access Read Error Status	HWC Overwrite Error Status	HWC Access Timeout Status	HWC Access Complete Status
7	6	5	4	3	2	1	0

bit 4 Memory Access Write Error Status
This bit indicates the status of the Memory Access Write Error interrupt. This bit is masked by the Memory Access Write Error Interrupt Enable bit and is only available when REG[0190h] bit 4 = 1b.
When this bit = 0b, the Memory Access Write Error interrupt has not occurred.
When this bit = 1b, the Memory Access Write Error interrupt has occurred.

To clear this bit, write a 1b to this bit.

bit 3 Memory Access Read Error Status
This bit indicates the status of the Memory Access Read Error interrupt. This bit is masked by the Memory Access Read Error Interrupt Enable bit and is only available when REG[0190h] bit 4 = 1b.
When this bit = 0b, the Memory Access Read Error interrupt has not occurred.
When this bit = 1b, the Memory Access Read Error interrupt has occurred.

To clear this bit, write a 1b to this bit.

bit 2 HWC Overwrite Error Status
This bit indicates the status of the HWC Overwrite Error interrupt. This bit is masked by the HWC Overwrite Error Interrupt Enable bit and is only available when REG[0190h] bit 4 = 1b.
When this bit = 0b, the HWC Overwrite Error interrupt has not occurred.
When this bit = 1b, the HWC Overwrite Error interrupt has occurred.

To clear this bit, write a 1b to this bit.

bit 1 HWC Access Timeout Status
This bit indicates the status of the HWC Access Timeout interrupt. This bit is masked by the HWC Access Timeout Interrupt Enable bit and is only available when REG[0190h] bit 4 = 1b.
When this bit = 0b, the HWC Access Timeout interrupt has not occurred.
When this bit = 1b, the HWC Access Timeout interrupt has occurred.

To clear this bit, write a 1b to this bit.

bit 0 HWC Access Complete Status

This bit indicates the status of the HWC Access Complete interrupt. This bit is masked by the HWC Access Complete Interrupt Enable bit and is only available when REG[0190h] bit 4 = 1b.

When this bit = 0b, the HWC Access Complete interrupt has not occurred.

When this bit = 1b, the HWC Access Complete interrupt has occurred.

To clear this bit, write a 1b to this bit.

REG[0194h] Memory Rectangular Write Address Offset Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a				Memory Rectangular Write Address Offset bits 11-8			
7	6	5	4	3	2	1	0
Memory Rectangular Write Address Offset bits 7-1							n/a

bits 11-1 Memory Rectangular Write Address Offset bits [11:1]

These bits specify the memory address offset, in bytes, used for rectangular memory writes when the HWC module is disabled (REG[0180h] bit 0 = 0b and REG[0184h] bit 15 = 1b).

REG[0194h] bits 11-0 = memory rectangular write address offset in bytes - 2

REG[0196h] Memory Rectangular Write Address Width Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a				Memory Rectangular Write Address Width bits 11-8			
7	6	5	4	3	2	1	0
Memory Rectangular Write Address Width bits 7-1							n/a

bits 11-1 Memory Rectangular Write Address Width bits [11:1]

These bits specify the memory address width, in bytes, used for rectangular memory writes when the HWC module is disabled (REG[0180h] bit 0 = 0b and REG[0184h] bit 15 = 1b).

REG[0196h] bits 11-1 = memory rectangular write address width in bytes - 2

Note

The horizontal size of the source image for PIP1 Window and PIP2 Window must be an even number (REG[0196h] bit 1 = 0b).

REG[0198h] VOUT Configuration Register

Default = 0000h — Read/Write

VOUT Output Rate bits 3-0				n/a		VOUT Delay Control bits 9-8	
15	14	13	12	11	10	9	8
VOUT Delay Control bits 7-0							
7	6	5	4	3	2	1	0

bits 15-12 VOUT Output Rate bits [3:0]

These bits control the frequency of VOUT which outputs the state of the LCD VSYNC signal (on the FPFRAME LCD interface pin) to the Host interface. For further information on VOUT, refer to Section 14.5, “Host Interface VSYNC Output” on page 173.

Table 10-9: VOUT Output Rate Selection

REG[0198h] bits 15-12	VOUT Output Rate
0000b (default)	No Output
0001b	Every VSYNC is output
0010b	1 VSYNC is output for every 2 LCD-VSYNC
0011b	1 VSYNC is output for every 3 LCD-VSYNC
0100b	1 VSYNC is output for every 4 LCD-VSYNC
• • •	• • •
1111b	1 VSYNC is output for every 15 LCD-VSYNC

Note

The VOUT polarity is the same as the FPFRAME polarity (see REG[0050h] bit 7).

bits 9-0 VOUT Delay Control bits [9:0]

These bits specify the number of lines delayed from VSYNC for LCD interface.

Table 10-10: VOUT Delay Selection

REG[0198h] bits 9-0	VOUT Delay
000h (default)	No Delay
001h	1 Line
002h	2 Lines
003h	3 Lines
• • •	• • •
3FFh	1023 Lines

REG[019Ah] is Reserved

This register is Reserved and should not be written.

10.4.7 Display Configuration Registers

REG[0200h] Display Mode Setting Register 0
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
LCD Software Reset (WO)	n/a	LCD-LUT Bypass Enable	PIP2-LUT Bypass Enable	n/a		Reserved	Reserved
7	6	5	4	3	2	1	0

bit 7 LCD Software Reset (Write Only)
This bit performs a software reset of the LCD module.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit performs a software reset of the LCD module.

bit 5 LCD-LUT Bypass Enable
This bit controls whether the LCD-LUT is used for gamma control of the LCD display output.
When this bit = 0b, the LCD-LUT is used.
When this bit = 1b, the LCD-LUT is bypassed.

Note
The LCD-LUT can only be accessed when the LCD-LUT is bypassed or the display is not active (REG[0202h] bit 13 = 0b).

bit 4 PIP2-LUT Bypass Enable
This bit controls whether the PIP2-LUT is used for gamma control of the PIP2 window.
When this bit = 0b, the PIP2-LUT is used.
When this bit = 1b, the PIP2-LUT is bypassed.

bit 1 Reserved
The default value for this bit is 0b.

bit 0 Reserved
The default value for this bit is 0b.

REG[0202h] Display Mode Setting Register 1
Default = 0000h Read/Write

Reserved		LCD Display Active Status bits 2-0 (RO)	Reserved		LCD Display Output Enable	Software Video Invert	Display Blank
15	14	13	12	11	10	9	8
n/a	Layer Mode Select bits 1-0		Main Display Mode Select	n/a	PIP2 Window Display Enable	PIP1 Window Display Enable	Main Window Display Enable
7	6	5	4	3	2	1	0

bits 15-14 Reserved

bit 13 LCD Display Active Status (Read Only)
These bits indicate whether display output port is active or not.

When this bit is 0, LCD display pipe is inactive.

When this bit is 1, LCD display pipe is active.

bits 12-11 Reserved.

This bits should be set 0.

bit10 LCD Display Output Enable

Table 10-11: LCD Output Enable

REG[0202h] bits 10	LCD Output Enable
0b (default)	Display Off
1b	LCD Display On

bit 9 Software Video Invert
This bit determines whether the RGB type panel data outputs (GPIO[23:18], FPDAT[17:0]) are inverted or left unchanged (normal). This bit has an effect both when the display is active and when the display is blanked (see REG[0202h] bit 8). For a summary, see Table 10-12: “LCD Interface Data Output Selection,” on page 81.
When this bit = 0b, the panel data output is left unchanged (normal).
When this bit = 1b, the panel data output is inverted.

bit 8 Display Blank
This bit blanks the display of RGB type panels by disabling the display pipe and forcing all data outputs (GPIO[23:18], FPDAT[17:0]) low (or high).
When this bit = 0b, the display is active.
When this bit = 1b, display is blanked and all data outputs are forced low or high based on the setting of the Software Video Invert bit (REG[0202h] bit 9).

Table 10-12: LCD Interface Data Output Selection

REG[0202h] bit 8	REG[0202h] bit 9	LCD Interface Data Output
0b	0b	Normal
	1b	Inverted
1b	0b	Force low
	1b	Force high

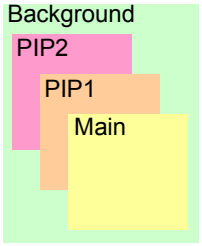
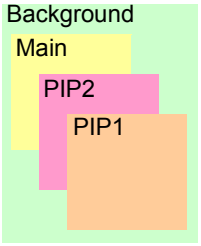
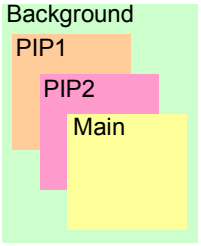
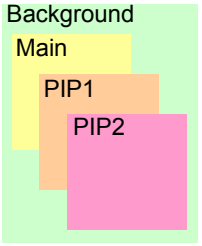
Note

For details on which pins are affected, see Table 5-9: “LCD Interface Pin Mapping,” on page 24.

bits 6-5 Layer Mode Select bits [1:0]

These bits select the order that the layers are shown on the display area. Any part of the display area that does not have a Main or PIP window covering it, is automatically filled with the Background Color (see REG[0206h]). The possible layer combinations are as follows.

Table 10-13: Layer Mode Selection

REG[0202h] bits 6-5	00b	01b	10b	11b
Window Layering				

Note

The Main Layer has an optional second window that is available when the Main Layer Display Mode Select bit is set to 1b (REG[0202h] bit 4 = 1b). However, the Main windows may not overlap and have certain restrictions that must be observed. For details, refer to Figure 13-3: “Main Layer Restrictions,” on page 141.

bit 4 Main Layer Display Mode Select

The Main Layer can consist of two windows, Main1 and Main2 (see Section 13.1, “Main Layer” on page 140). This bit selects the number of windows that are displayed on the Main Layer. When two main windows are selected, the Main windows may not overlap and have certain restrictions that must be observed. For details, refer to Figure 13-3: “Main Layer Restrictions,” on page 141.

When this bit = 0b, the Main layer includes the Main1 window only.

When this bit = 1b, the Main layer includes Main1 window and Main2 window.

bit 2 PIP2 Window Display Enable

This bit controls whether the PIP2 window is displayed.

When this bit = 0b, the PIP2 window is disabled.

When this bit = 1b, the PIP2 window is enabled.

Note

1. The PIP2-LUT can be programmed only when the PIP2 window is disabled (REG[0202h] bit 2 = 0b) or when the LCD Output Enable is set to “Display Off”(REG[0202h]bit10=0b.

bit 1	PIP1 Window Display Enable This bit controls whether the PIP1 window is displayed. When this bit = 0b, the PIP1 window is disabled. When this bit = 1b, the PIP1 window is enabled.
bit 0	Main Window Display Enable This bit controls whether the Main window is displayed. When this bit = 0b, the Main window is disabled. When this bit = 1b, the Main window is enabled.

REG[0204h] Transparency and Alpha Blend Control Register

Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a				Alpha Blend 4 Key Color Enable	Alpha Blend 3 Key Color Enable	Alpha Blend 2 Key Color Enable	Alpha Blend 1 Key Color Enable
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Alpha Blend Mode Select	n/a				PIP2 Transparency Enable	PIP1 Transparency Enable	Reserved

bit 11 Alpha Blend 4 Key Color Enable

This bit controls the Alpha Blend 4 key color. Alpha blending is only available when the Main Layer is on top of the PIP Layers, REG[0202h] bits 6-5 = 00b or 10b.

When this bit = 0b, the Alpha Blend 4 key color is disabled.

When this bit = 1b, the Alpha Blend 4 key color is enabled.

bit 10 Alpha Blend 3 Key Color Enable

This bit controls the Alpha Blend 3 key color. Alpha blending is only available when the Main Layer is on top of the PIP Layers, REG[0202h] bits 6-5 = 00b or 10b.

When this bit = 0b, the Alpha Blend 3 key color is disabled.

When this bit = 1b, the Alpha Blend 3 key color is enabled.

bit 9 Alpha Blend 2 Key Color Enable

This bit controls the Alpha Blend 2 key color. Alpha blending is only available when the Main Layer is on top of the PIP Layers, REG[0202h] bits 6-5 = 00b or 10b.

When this bit = 0b, the Alpha Blend 2 key color is disabled.

When this bit = 1b, the Alpha Blend 2 key color is enabled.

bit 8 Alpha Blend 1 Key Color Enable

This bit controls the Alpha Blend 1 key color. Alpha blending is only available when the Main Layer is on top of the PIP Layers, REG[0202h] bits 6-5 = 00b or 10b.

When this bit = 0b, the Alpha Blend 1 key color is disabled.

When this bit = 1b, the Alpha Blend 1 key color is enabled.

bit 7 Alpha Blend Mode Select

This bit selects which windows are alpha blended.

When this bit = 0b, alpha blending is performed on the Main and PIP windows.

When this bit = 1b, alpha blending is performed on the PIP1 and PIP2 windows. If the PIP1 and PIP2 windows overlap each other and are overlapped by the active Main window containing the selected alpha blend key color, the PIP1 and PIP2 windows are alpha blended using the specified alpha blend setting. However, if the PIP1 and PIP2 windows do not overlap but are overlapped by the active Main window containing the selected alpha blend color, the PIP1 or PIP2 window will “show through” the Main window alpha blend key color similar to a transparency function.

bit 2 PIP2 Transparency Enable
This bit controls the PIP2 Transparency.
When this bit = 0b, the PIP2 Transparency is disabled.
When this bit = 1b, the PIP2 Transparency is enabled.

Note
1. When the PIP2 Transparency is enabled, the vertical and horizontal scaling filters should be disabled (REG[02A0h] bit 5 = 0b and bit 1 = 0b).
2. PIP2 Transparency affects only the window layers underneath the PIP2 window and has no effect on the background color. For example, if the PIP2 window has transparency enabled, with a key color selected but nothing underneath, the background color will not show through and the key color will be visible.

bit 1 PIP1 Transparency Enable
This bit controls the PIP1 Transparency.
When this bit = 0b, the PIP1 Transparency is disabled.
When this bit = 1b, the PIP1 Transparency is enabled.

Note
1. When the PIP1 Transparency is enabled, the vertical and horizontal scaling filters should be disabled (REG[0260h] bit 5 = 0b and bit 1 = 0b).
2. PIP1 Transparency affects only the window layers underneath the PIP1 window and has no effect on the background color. For example, if the PIP1 window has transparency enabled, with a key color selected but nothing underneath, the background color will not show through and the key color will be visible.

bit 0 Reserved
The default value for this bit is 0b

REG[0206h] Background Color Setting Register
Default = 0000h Read/Write

Background Color Red bits 4-0					Background Color Green bits 5-3		
15	14	13	12	11	10	9	8
Background Color Green bits 2-0			Background Color Blue bits 4-0				
7	6	5	4	3	2	1	0

bits 15-11 Background Color Red bits [4:0]
These bits specify the 5-bit red component used to define the background color.

bits 10-5 Background Color Green bits [5:0]
These bits specify the 6-bit green component used to define the background color.

bits 4-0 Background Color Blue bits [4:0]
These bits specify the 5-bit blue component used to define the background color.

REG[0208h] Alpha Blend Ratio Setting Register
Default = 8888h — Read/Write

Alpha Blend 4 Ratio Setting bits 3-0				Alpha Blend 3 Ratio Setting bits 3-0			
15	14	13	12	11	10	9	8
Alpha Blend 2 Ratio Setting bits 3-0				Alpha Blend 1 Ratio Setting bits 3-0			
7	6	5	4	3	2	1	0

bits 15-12 Alpha Blend 4 Ratio Setting bits [3:0]

These bits only have an effect when the Alpha Blend 4 key color is enabled, REG[0204h] bit 11 = 1b. These bits select the Alpha Blend ratio for the Alpha Blend 4 key color.

Table 10-14: Alpha Blend 4 Ratio Selection

REG[0208h] bits 15-12	Alpha Blend Ratio
0000b	0%
0001b	12.5%
0010b	25%
0011b	37.5%
0100b	50%
0101b	62.5%
0110b	75%
0111b	87.5%
1000b	100%
1001b ~ 1111b	Reserved

bits 11-8 Alpha Blend 3 Ratio Setting bits [3:0]

These bits only have an effect when the Alpha Blend 3 Key Color is enabled, REG[0204h] bit 10 = 1b. These bits select the Alpha Blend ratio for the Alpha Blend 3 key color.

Table 10-15: Alpha Blend 3 Ratio Selection

REG[0208h] bits 11-8	Alpha Blend Ratio
0000b	0%
0001b	12.5%
0010b	25%
0011b	37.5%
0100b	50%
0101b	62.5%
0110b	75%
0111b	87.5%
1000b	100%
1001b ~ 1111b	Reserved

bits 7-4 Alpha Blend 2 Ratio Setting bits [3:0]

These bits only have an effect when the Alpha Blend 2 key color is enabled, REG[0204h] bit 9 = 1b. These bits select the Alpha Blend ratio for Alpha Blend 2 key color.

Table 10-16: Alpha Blend 2 Ratio Selection

REG[0208h] bits 7-4	Alpha Blend Ratio
0000b	0%
0001b	12.5%
0010b	25%
0011b	37.5%
0100b	50%
0101b	62.5%
0110b	75%
0111b	87.5%
1000b	100%
1001b ~ 1111b	Reserved

bits 3-0 Alpha Blend 1 Ratio Setting bits [3:0]

These bits only have an effect when the Alpha Blend 1 Key Color is enabled, REG[0204h] bit 8 = 1b. These bits select the Alpha Blend ratio for Alpha Blend 1 key color.

Table 10-17: Alpha Blend 1 Ratio Selection

REG[0208h] bits 3-0	Alpha Blend Ratio
0000b	0%
0001b	12.5%
0010b	25%
0011b	37.5%
0100b	50%
0101b	62.5%
0110b	75%
0111b	87.5%
1000b	100%
1001b ~ 1111b	Reserved

REG[020Ch] PIP1 Window Transparency Key Color Register

Default = 0000h Read/Write

PIP1 Window Transparency Key Color Red bits 4-0					PIP1 Window Transparency Key Color Green bits 5-3		
15	14	13	12	11	10	9	8
PIP1 Window Transparency Key Color Green bits 2-0			PIP1 Window Transparency Key Color Blue bits 4-0				
7	6	5	4	3	2	1	0

bits 15-11 PIP1 Window Transparency Key Color Red bits [4:0]

These bits only have an effect when the PIP1 transparency is enabled, REG[0204h] bit 1 = 1b. These bits specify the 5-bit red component used to define the PIP1 window transparency key color.

bits 10-5 PIP1 Window Transparency Key Color Green bits [5:0]
These bits only have an effect when the PIP1 transparency is enabled, REG[0204h] bit 1 = 1b. These bits specify the 6-bit green component used to define the PIP1 window transparency key color.

bits 4-0 PIP1 Window Transparency Key Color Blue bits [4:0]
These bits only have an effect when the PIP1 transparency is enabled, REG[0204h] bit 1 = 1b. These bits specify the 5-bit blue component used to define the PIP1 window transparency key color.

REG[020Eh] PIP2 Window Transparency Key Color Register
Default = 0000h Read/Write

PIP2 Window Transparency Key Color Red bits 4-0					PIP2 Window Transparency Key Color Green bits 5-3		
15	14	13	12	11	10	9	8
PIP2 Window Transparency Key Color Green bits 2-0			PIP2 Window Transparency Key Color Blue bits 4-0				
7	6	5	4	3	2	1	0

bits 15-11 PIP2 Window Transparency Key Color Red bits [4:0]
These bits only have an effect when the PIP2 transparency is enabled, REG[0204h] bit 2 = 1b. These bits specify the 5-bit red component used to define the PIP2 window transparency key color.

bits 10-5 PIP2 Window Transparency Key Color Green bits [5:0]
These bits only have an effect when the PIP2 transparency is enabled, REG[0204h] bit 2 = 1b. These bits specify the 6-bit green component used to define the PIP2 window transparency key color.

bits 4-0 PIP2 Window Transparency Key Color Blue bits [4:0]
These bits only have an effect when the PIP2 transparency is enabled, REG[0204h] bit 2 = 1b. These bits specify the 5-bit blue component used to define the PIP2 window transparency key color.

REG[0210h] Alpha Blend 1 Key Color Register
Default = 0000h Read/Write

Alpha Blend 1 Key Color Red bits 4-0					Alpha Blend 1 Key Color Green bits 5-3		
15	14	13	12	11	10	9	8
Alpha Blend 1 Key Color Green bits 2-0			Alpha Blend 1 Key Color Blue bits 4-0				
7	6	5	4	3	2	1	0

bits 15-11 Alpha Blend 1 Key Color Red bits [4:0]
These bits only have an effect when the Alpha Blend 1 key color is enabled, REG[0204h] bit 8 = 1b. These bits specify the 5-bit red component used to define the Alpha Blend 1 key color.

bits 10-5 Alpha Blend 1 Key Color Green bits [5:0]
These bits only have an effect when the Alpha Blend 1 key color is enabled, REG[0204h] bit 8 = 1b. These bits specify the 6-bit green component used to define the Alpha Blend 1 key color.

bits 4-0 Alpha Blend 1 Key Color Blue bits [4:0]
These bits only have an effect when the Alpha Blend 1 key color is enabled, REG[0204h] bit 8 = 1b. These bits specify the 5-bit blue component used to define the Alpha Blend 1 key color.

REG[0212h] Alpha Blend 2 Key Color Register
Default = 0000h Read/Write

Alpha Blend 2 Key Color Red bits 4-0					Alpha Blend 2 Key Color Green bits 5-3		
15	14	13	12	11	10	9	8
Alpha Blend 2 Key Color Green bits 2-0			Alpha Blend 2 Key Color Blue bits 4-0				
7	6	5	4	3	2	1	0

bits 15-11 Alpha Blend 2 Key Color Red bits [4:0]
These bits only have an effect when the Alpha Blend 2 key color is enabled, REG[0204h] bit 9 = 1b. These bits specify the 5-bit red component used to define the Alpha Blend 2 key color.

bits 10-5 Alpha Blend 2 Key Color Green bits [5:0]
These bits only have an effect when the Alpha Blend 2 key color is enabled, REG[0204h] bit 9 = 1b. These bits specify the 6-bit green component used to define the Alpha Blend 2 key color.

bits 4-0 Alpha Blend 2 Key Color Blue bits [4:0]
These bits only have an effect when the Alpha Blend 2 key color is enabled, REG[0204h] bit 9 = 1b. These bits specify the 5-bit blue component used to define the Alpha Blend 2 key color.

REG[0214h] Alpha Blend 3 Key Color Register
Default = 0000h Read/Write

Alpha Blend 3 Key Color Red bits 4-0					Alpha Blend 3 Key Color Green bits 5-3		
15	14	13	12	11	10	9	8
Alpha Blend 3 Key Color Green bits 2-0			Alpha Blend 3 Key Color Blue bits 4-0				
7	6	5	4	3	2	1	0

bits 15-11 Alpha Blend 3 Key Color Red bits [4:0]
These bits only have an effect when the Alpha Blend 3 key color is enabled, REG[0204h] bit 10 = 1b. These bits specify the 5-bit red component used to define the Alpha Blend 3 key color.

bits 10-5 Alpha Blend 3 Key Color Green bits [5:0]
These bits only have an effect when the Alpha Blend 3 key color is enabled, REG[0204h] bit 10 = 1b. These bits specify the 6-bit green component used to define the Alpha Blend 3 key color.

bits 4-0 Alpha Blend 3 Key Color Blue bits [4:0]
These bits only have an effect when the Alpha Blend 3 key color is enabled, REG[0204h] bit 10 = 1b. These bits specify the 5-bit blue component used to define the Alpha Blend 3 key color.

REG[0216h] Alpha Blend 4 Key Color Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Alpha Blend 4 Key Color Red bits 4-0					Alpha Blend 4 Key Color Green bits 5-3		
7	6	5	4	3	2	1	0
Alpha Blend 4 Key Color Green bits 2-0			Alpha Blend 4 Key Color Blue bits 4-0				

bits 15-11 Alpha Blend 4 Key Color Red bits [4:0]
These bits only have an effect when the Alpha Blend 4 key color is enabled, REG[0204h] bit 11 = 1b. These bits specify the 5-bit red component used to define the Alpha Blend 4 key color.

bits 10-5 Alpha Blend 4 Key Color Green bits [5:0]
These bits only have an effect when the Alpha Blend 4 key color is enabled, REG[0204h] bit 11 = 1b. These bits specify the 6-bit green component used to define the Alpha Blend 4 key color.

bits 4-0 Alpha Blend 4 Key Color Blue bits [4:0]
These bits only have an effect when the Alpha Blend 4 key color is enabled, REG[0204h] bit 11 = 1b. These bits specify the 5-bit blue component used to define the Alpha Blend 4 key color.

REG[0218h] Main1 Window X Start Position Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						Main1 Window X Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main1 Window X Start Position bits 7-0							

bits 9-0 Main1 Window X Start Position bits [9:0]
These bits determine the X start position of the Main1 Window in relation to the origin of the panel, in pixels. For details on configuring the Main Layer, see Section 13.1, “Main Layer” on page 140.

REG[021Ah] Main1 Window Y Start Position Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						Main1 Window Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main1 Window Y Start Position bits 7-0							

bits 9-0 Main1 Window Y Start Position bits [9:0]
These bits determine the Y start position of the Main1 Window in relation to the origin of the panel, in pixels. For details on configuring the Main Layer, see Section 13.1, “Main Layer” on page 140.

REG[0220h] Main2 Window X Start Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						Main2 Window X Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main2 Window X Start Position bits 7-0							

bits 9-0 Main2 Window X Start Position bits [9:0]
These bits determine the X start position of the Main2 Window in relation to the origin of the panel, in pixels. For details on configuring the Main Layer, see Section 13.1, “Main Layer” on page 140.

REG[0222h] Main2 Window Y Start Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						Main2 Window Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main2 Window Y Start Position bits 7-0							

bits 9-0 Main2 Window Y Start Position bits [9:0]
These bits determine the Y start position of the Main2 Window in relation to the origin of the panel, in pixels. For details on configuring the Main Layer, see Section 13.1, “Main Layer” on page 140.

REG[0228h] PIP1 Window X Start Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP1 Window X Start Position bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Window X Start Position bits 7-0							

bits 9-0 PIP1 Window X Start Position bits [9:0]
These bits determine the X start position of the PIP1 Window in relation to the origin of the panel, in pixels. For details on configuring the PIP window(s), see Section 13.2, “PIP Layers” on page 144.

REG[022Ah] PIP1 Window Y Start Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP1 Window Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Window Y Start Position bits 7-0							

bits 9-0 PIP1 Window Y Start Position bits [9:0]
These bits determine the Y start position of the PIP1 Window in relation to the origin of the panel, in pixels. For details on configuring the PIP window(s), see Section 13.2, “PIP Layers” on page 144.

REG[022Ch] PIP1 Window X End Position Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						PIP1 Window X End Position bits 9-8	
PIP1 Window X End Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP1 Window X End Position bits [9:0]
These bits determine the X end position of the PIP1 Window in relation to the origin of the panel, in pixels. For details on configuring the PIP window(s), see Section 13.2, “PIP Layers” on page 144.

Note
This register must be programmed such that the following formula is valid.
REG[022Ch] - REG[0228h] ≥ 4

REG[022Eh] PIP1 Window Y End Position Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						PIP1 Window Y End Position bits 9-8	
PIP1 Window Y End Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP1 Window Y End Position bits [9:0]
These bits determine the Y end position of the PIP1 Window in relation to the origin of the panel, in pixels. For details on configuring the PIP window(s), see Section 13.2, “PIP Layers” on page 144.

Note
This register must be programmed such that the following formula is valid.
REG[022Eh] - REG[022Ah] ≥ 4

REG[0230h] PIP2 Window X Start Position Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						PIP2 Window X Start Position bits 9-8	
PIP2 Window X Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP2 Window X Start Position bits [9:0]
These bits determine the X start position of the PIP2 Window in relation to the origin of the panel, in pixels. For details on configuring the PIP window(s), see Section 13.2, “PIP Layers” on page 144.

REG[0232h] PIP2 Window Y Start Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP2 Window Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
PIP2 Window Y Start Position bits 7-0							

bits 9-0 PIP2 Window Y Start Position bits [9:0]
These bits determine the Y start position of the PIP2 Window in relation to the origin of the panel, in pixels. For details on configuring the PIP window(s), see Section 13.2, “PIP Layers” on page 144.

REG[0234h] PIP2 Window X End Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP2 Window X End Position bits 9-8	
7	6	5	4	3	2	1	0
PIP2 Window X End Position bits 7-0							

bits 9-0 PIP2 Window X End Position bits [9:0]
These bits determine the X end position of the PIP2 Window in relation to the origin of the panel, in pixels. For details on configuring the PIP window(s), see Section 13.2, “PIP Layers” on page 144.

Note
This register must be programmed such that the following formula is valid.
REG[0234h] - REG[0230h] ≥ 4

REG[0236h] PIP2 Window Y End Position Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP2 Window Y End Position bits 9-8	
7	6	5	4	3	2	1	0
PIP2 Window Y End Position bits 7-0							

bits 9-0 PIP2 Window Y End Position bits [9:0]
These bits determine the Y end position of the PIP2 Window in relation to the origin of the panel, in pixels. For details on configuring the PIP window(s), see Section 13.2, “PIP Layers” on page 144.

Note
This register must be programmed such that the following formula is valid.
REG[0236h] - REG[0232h] ≥ 4

REG[0238h] Main1 Window Scroll Start Address Register 0

Default = 0000h — Read/Write

Main1 Window Scroll Start Address bits 15-8							
15	14	13	12	11	10	9	8
Main1 Window Scroll Start Address bits 7-1							n/a
7	6	5	4	3	2	1	0

REG[023Ah] Main1 Window Scroll Start Address Register 1

Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				Main1 Window Scroll Start Address bits 19-16			
7	6	5	4	3	2	1	0

REG[023Ah] bits 3-0

REG[0238h] bits 15-1 Main1 Window Scroll Start Address bits [19:1]

These bits specify the scroll start address for the Main1 window in the display buffer. To disable scrolling for the Main1 window, set the Main1 Window Scroll Start Address to 0h (REG[0238h] ~ REG[023Ah]) and the Main1 Window Scroll End Address to the maximum value (REG[023Ch] ~ REG[023Eh]). For further information on scrolling, see Section 13.4, “Scroll Buffer” on page 153.

Note

1. The Main1 Window Scroll Start Address must be less than the Main1 Window Scroll End Address.
   REG[0238h] ~ REG[023Ah] < REG[023Ch] ~ REG[023Eh]
2. The Main1 Window Display Start Address must be less than the Main1 Window Scroll End Address.
   REG[0240h] ~ REG[0242h] < REG[023Ch] ~ REG[023Eh]

REG[023Ch] Main1 Window Scroll End Address Register 0
Default = FFFEh — Read/Write

15	14	13	12	11	10	9	8
Main1 Window Scroll End Address bits 15-8							
7	6	5	4	3	2	1	0
Main1 Window Scroll End Address bits 7-1							n/a

REG[023Eh] Main1 Window Scroll End Address Register 1
Default = 000Fh — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a				Main1 Window Scroll End Address bits 19-16			

REG[023Eh] bits 3-0

REG[023Ch] bits 15-1 Main1 Window Scroll End Address bits [19:1]

These bits specify the scroll end address for the Main1 window in the display buffer. If the Main1 window display address is larger than this address, the Main1 window display address goes to the Main1 window scroll start address. To disable scrolling for the Main1 window, set the Main1 Window Scroll Start Address to 0h (REG[0238h] ~ REG[023Ah]) and the Main1 Window Scroll End Address to the maximum value (REG[023Ch] ~ REG[023Eh]).For further information on scrolling, see Section 13.4, “Scroll Buffer” on page 153.

Note

1. The Main1 Window Scroll Start Address must be less than the Main1 Window Scroll End Address.
   REG[0238h] ~ REG[023Ah] < REG[023Ch] ~ REG[023Eh]
2. The Main1 Window Display Start Address must be less than the Main1 Window Scroll End Address.
   REG[0240h] ~ REG[0242h] < REG[023Ch] ~ REG[023Eh]

REG[0240h] Main1 Window Display Start Address Register 0
Default = 0000h — Read/Write

Main1 Window Display Start Address bits 15-8							
15	14	13	12	11	10	9	8
Main1 Window Display Start Address bits 7-1							n/a
7	6	5	4	3	2	1	0

REG[0242h] Main1 Window Display Start Address Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				Main1 Window Display Start Address bits 19-16			
7	6	5	4	3	2	1	0

REG[0242h] bits 3-0
REG[0240h] bits 15-1 Main1 Window Display Start Address bits [19:1]
These bits specify the start address for the Main1 window image in the display buffer.

Note
The Main1 Window Display Start Address must be less than the Main1 Window Scroll End Address.
REG[0240h] ~ REG[0242h] < REG[023Ch] ~ REG[023Eh]

REG[0244h] Main1 Window Line Address Offset Register
Default = 0000h — Read/Write

n/a		Main1 Window Vertical Pixel Doubling Enable	Main1 Window Horizontal Pixel Doubling Enable	Main1 Window Line Address Offset bit 11-8			
15	14	13	12	11	10	9	8
Main1 Window Line Address Offset bit 7-1							n/a
7	6	5	4	3	2	1	0

bit 13 Main1 Window Vertical Pixel Doubling Enable
This bit controls the pixel doubling feature for the vertical dimension, or height, of the Main1 window.
When this bit = 0b, there is no hardware effect.
When this bit = 1b, pixel doubling in the vertical dimension (height) is enabled.

Note
When Main1 Window Vertical Pixel Doubling is enabled (REG[0244h] bit 13 = 1b), the bottom edge of the resulting window must not exceed the bottom edge of the panel (must be less than or equal to the panel VDP). For further information on Main1 window pixel doubling restrictions, see Section 13.1.1, “Main Layer Restrictions” on page 141 and Section 13.1.3, “Main Layer Pixel Doubling” on page 142.

bit 12 Main1 Window Horizontal Pixel Doubling Enable
This bit controls the pixel doubling feature for the horizontal dimension, or width, of the Main1 window.
When this bit = 0b, there is no hardware effect.
When this bit = 1b, pixel doubling in the horizontal dimension (width) is enabled.

Note
When Main1 Window Horizontal Pixel Doubling is enabled (REG[0244h] bit 12 = 1b), the right edge of the resulting window must not exceed the right edge of the panel (must be less than or equal to the panel HDP). For further information on Main1 window pixel doubling restrictions, see Section 13.1.1, "Main Layer Restrictions" on page 141 and Section 13.1.3, "Main Layer Pixel Doubling" on page 142.

bits 11-1 Main1 Window Line Address Offset bits [11:1]
These bits specify the offset from the beginning of one display line to the beginning of the next display line in the memory used for the Main1 window. The Line Address Offset can be calculated as follows (valid for both pixel doubling enabled and disabled).
REG[0244h] bits 11-0 = Line width in pixels x 16 ÷ 8

REG[0246h] Main1 Window Image Horizontal Size Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						Main1 Window Image Horizontal Size bits 9-8	
Main1 Window Image Horizontal Size bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 Main1 Window Image Horizontal Size bits [9:0]
These bits specify the horizontal size of the Main1 window image, in pixels.
REG[0246h] bits 9-0 = Main1 Window Image Horizontal Size in pixels - 1

REG[0248h] Main1 Window Image Vertical Size Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						Main1 Window Image Vertical Size bits 9-8	
Main1 Window Image Vertical Size bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 Main1 Window Image Vertical Size bits [9:0]
These bits specify the vertical size of the Main1 window image, in pixels.
REG[0248h] bits 9-0 = Main1 Window Image Vertical Size in pixels - 1

REG[024Ah] Main2 Window Display Start Address Register 0
Default = 0000h Read/Write

Main2 Window Display Start Address bits 15-8							
15	14	13	12	11	10	9	8
Main2 Window Display Start Address bits 7-1							n/a
7	6	5	4	3	2	1	0

REG[024Ch] Main2 Window Display Start Address Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				Main2 Window Display Start Address bits 19-16			
7	6	5	4	3	2	1	0

REG[024Ch] bits 3-0
REG[024Ah] bits 15-1 Main2 Window Display Start Address bits [19:1]
These bits specify the start address of the Main2 window image in the display buffer.

REG[024Eh] Main2 Window Line Address Offset Register
Default = 0000h Read/Write

n/a		Main2 Window Vertical Pixel Doubling Enable	Main2 Window Horizontal Pixel Doubling Enable	Main2 Window Line Address Offset bit 11-8			
15	14	13	12	11	10	9	8
Main2 Window Line Address Offset bit 7-1							n/a
7	6	5	4	3	2	1	0

bit 13 Main2 Window Vertical Pixel Doubling Enable
This bit controls the pixel doubling feature for the vertical dimension, or height, of the Main2 window.
When this bit = 0b, there is no hardware effect.
When this bit = 1b, pixel doubling in the vertical dimension (height) is enabled.

Note
When Main2 Window Vertical Pixel Doubling is enabled (REG[024Eh] bit 13 = 1b), the bottom edge of the resulting window must not exceed the bottom edge of the panel (must be less than or equal to the panel VDP). Additionally, the bottom edge of the Main1 window must not be greater than the top edge of the Main2 window. For further information on Main2 window pixel doubling restrictions, see Section 13.1.1, “Main Layer Restrictions” on page 141 and Section 13.1.3, “Main Layer Pixel Doubling” on page 142.

bit 12 Main2 Window Horizontal Pixel Doubling Enable
This bit controls the pixel doubling feature for the horizontal dimension, or width, of the Main2 window.
When this bit = 0b, there is no hardware effect.
When this bit = 1b, pixel doubling in the horizontal dimension (width) is enabled.

Note
When Main2 Window Horizontal Pixel Doubling is enabled (REG[024Eh] bit 12 = 1b), the right edge of the resulting window must not exceed the right edge of the panel (must be less than or equal to the panel HDP). For further information on Main2 window pixel doubling restrictions, see Section 13.1.1, "Main Layer Restrictions" on page 141 and Section 13.1.3, "Main Layer Pixel Doubling" on page 142.

bits 11-1 Main2 Window Line Address Offset bits [11:1]
These bits specify the offset from the beginning of one display line to the beginning of the next display line in the memory used for the main window2. The Line Address Offset can be calculated as follows (valid for both pixel doubling enabled and disabled).
REG[0244h] bits 11-0 = Line width in pixels x 16 ÷ 8

REG[0250h] Main2 Window Image Horizontal Size Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						Main2 Window Image Horizontal Size bits 9-8	
Main2 Window Image Horizontal Size bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 Main2 Window Image Horizontal Size bits [9:0]
These bits specify the horizontal size of the Main2 window image, in pixels.
REG[0250h] bits 9-0 = Main2 Window Image Horizontal Size in pixels - 1

REG[0252h] Main2 Window Image Vertical Size Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						Main2 Window Image Vertical Size bits 9-8	
Main2 Window Image Vertical Size bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 Main2 Window Image Vertical Size bits [9:0]
These bits specify the vertical size of the Main2 window image, in pixels.
REG[0252h] bits 9-0 = Main2 Window Image Vertical Size in pixels - 1

10.4.8 PIP1 Window Configuration Registers

REG[0260h] PIP1 Scaling Mode Register
Default = 0000h — Read/Write

PIP1 Edge Enhance Enable	n/a				PIP1 Edge Enhance Effect bits 2-0		
15	14	13	12	11	10	9	8
PIP1 Vertical Scaling Enable	n/a	PIP1 Vertical Filter Mode Select	n/a	PIP1 Horizontal Scaling Enable	n/a	PIP1 Horizontal Filter Mode Select	n/a
7	6	5	4	3	2	1	0

bit 15 PIP1 Edge Enhance Enable

This bit controls the edge enhancement effect for the PIP1 window.
When this bit = 0b, the edge enhancement effect for the PIP1 window is disabled.
When this bit = 1b, the edge enhancement effect for the PIP1 window is enabled.

Note
When the PIP1 Transparency is enabled (REG[0204h] bit 1 = 1b), PIP1 edge enhancement should be disabled, REG[0260h] bit 15 = 0b.

bits 10-8 PIP1 Edge Enhance Effect bits [2:0]

These bits only have an effect when PIP1 edge enhance is enabled, REG[0260h] bit 15 = 1b. These bits specify the strength of the edge enhancement effect. A value of 001b specifies the weakest edge enhancement and a value of 111b specifies the strongest edge enhancement. A value of 000b disables the edge enhancement effect.

bit 7 PIP1 Vertical Scaling Enable

This bit controls vertical scaling for the PIP1 window. For details on configuring vertical scaling, see Section 13.2.2, “Using The Scalers” on page 146.
When this bit = 0b, vertical scaling for PIP1 is disabled.
When this bit = 1b, vertical scaling for PIP1 is enabled.

bit 5 PIP1 Vertical Filter Mode Select

This bit sets the filter mode for vertical scaling of the PIP1 window. For details on configuring vertical scaling, see Section 13.2.2, “Using The Scalers” on page 146.
When this bit = 0b, the vertical scaling filter is disabled.
When this bit = 1b, the vertical scaling filter is enabled.

Table 10-18: Vertical Filter Mode

REG[0260h] bits 5	Vertical Filter Mode
0b	Line replication/decimation
1b	SINC interpolation function as an impulse response

Note
When the PIP1 Transparency is enabled (REG[0204h] bit 1 = 1b), the vertical scaling filter should be disabled, REG[0260h] bit 5 = 0b.

bit 3 PIP1 Horizontal Scaling Enable
This bit controls horizontal scaling for the PIP1 window. For details on configuring horizontal scaling, see Section 13.2.2, "Using The Scalers" on page 146.
When this bit = 0b, horizontal scaling for PIP1 is disabled.
When this bit = 1b, horizontal scaling for PIP1 is enabled.

bit 1 PIP1 Horizontal Filter Mode Select
This bit sets the filter mode for horizontal scaling of the PIP1 window.
When this bit = 0b, the horizontal scaling filter is disabled.
When this bit = 1b, the horizontal scaling filter is enabled.

Table 10-19: Horizontal Filter Mode

REG[0260h] bits 1	Horizontal Filter Mode
0b	Pixel replication/decimation
1b	SINC interpolation function as an impulse response

Note
When the PIP1 Transparency is enabled (REG[0204h] bit 1 = 1b), the horizontal scaling filter should be disabled, REG[0260h] bit 1 = 0b.

REG[0262h] PIP1 Scaler Horizontal Scale Register
Default = 0000h Read/Write

Reserved			PIP1 Horizontal Scale bits 12-8				
15	14	13	12	11	10	9	8
PIP1 Horizontal Scale bits 7-0							
7	6	5	4	3	2	1	0

bits 15-13 Reserved
The default value for these bits is 000b.

bits 12-0 PIP1 Horizontal Scale bits [12:0]
These bits determine the horizontal scaling factor for the PIP1 scaler and must be programmed based on the following formula.

REG[0262h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)

The fractional point is to the right of bit 10. If the scaling mode is ZOOM (Scaled up), REG[0262h] bits 12-10 should equal zero. If the scaling mode is SHRINK (Scaled down), REG[0262h] bits 12-10 should be non-zero.

Example: For a scaling ratio of 3.51 (Zoom case), REG[0262h] bits 12-0 should be programmed as follows.

REG[0262h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)
= 1024 x (1 ÷ 3.51)
= 291 (round down)
= 123h

Note

The scale-down rate depends on the PCLK (Dot Clock), size of the panel, and the PIP1 window size. The horizontal scale rate must observe the following formula.

Horizontal Scale Rate ≥ PCLK Divide

For example, selecting a horizontal scale rate of 1/2 and a PCLK Divide of 1/2 is valid. Selecting a horizontal scale rate of 1/3 and a PCLK Divide of 1/2 is not valid.

REG[0264h] PIP1 Scaler Vertical Scale Register
Default = 0000h — Read/Write

Reserved			PIP1 Vertical Scale bits 12-8				
15	14	13	12	11	10	9	8
PIP1 Vertical Scale bits 7-0							
7	6	5	4	3	2	1	0

bits 15-13 Reserved
The default value for these bits is 000b.

bits 12-0 PIP1 Vertical Scale bits [12:0]
These bits determine the vertical scaling factor for the PIP1 scaler and must be programmed based on the following formula.
REG[0264h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)

The fractional point is to the right of bit 10. If the scaling mode is ZOOM (Scaled up), REG[0262h] bits 12-10 should equal zero. If the scaling mode is SHRINK (Scaled down), REG[0262h] bits 12-10 should be non-zero.

Example: For a scaling ratio of 3.51 (Zoom case), REG[0262h] bits 12-0 should be programmed as follows.

REG[0262h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)
= 1024 x (1 ÷ 3.51)
= 291 (round down)
= 123h

Note

The scale-down rate depends on the PCLK (Dot Clock), size of the panel, and the PIP1 window size. Two different sets of formulas must be observed based on the relationship between the Horizontal Scale Rate and the PCLK Divide.

When the PCLK Divide is less than the Horizontal Scale Rate and the Horizontal Scale Rate is less than or equal to 1 (PCLK < Horizontal Scale Rate ≤ 1), the following formulas must be observed.

For a Vertical Scale Rate of:

1 to 1/2: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 1) + 64 < HT x (1÷PCLK Divide)
1/2 to 1/3: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 2) + 64 < HT x (1÷PCLK Divide)
1/3 to 1/4: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 3) + 64 < HT x (1÷PCLK Divide)
1/4 to 1/5: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 4) + 64 < HT x (1÷PCLK Divide)
1/5 to 1/6: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 5) + 64 < HT x (1÷PCLK Divide)
1/6 to 1/7: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 6) + 64 < HT x (1÷PCLK Divide)
1/7 to 1/8: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 7) + 64 < HT x (1÷PCLK Divide)

Where:

A = Horizontal size of the PIP1 window
B = Horizontal scale rate
HT = Horizontal total of the panel

When the PCLK Divide is equal to the Horizontal Scale Rate (PCLK = Horizontal Scale Rate), the following formulas must be observed.

For a Vertical Scale Rate of:

1 to 1/2: (A x (1÷B) x 2 + 64 < HT x (1÷PCLK Divide)
1/2 to 1/3: (A x (1÷B) x 3 + 64 < HT x (1÷PCLK Divide)
1/3 to 1/4: (A x (1÷B) x 4 + 64 < HT x (1÷PCLK Divide)
1/4 to 1/5: (A x (1÷B) x 5 + 64 < HT x (1÷PCLK Divide)
1/5 to 1/6: (A x (1÷B) x 6 + 64 < HT x (1÷PCLK Divide)
1/6 to 1/7: (A x (1÷B) x 7 + 64 < HT x (1÷PCLK Divide)
1/7 to 1/8: (A x (1÷B) x 8 + 64 < HT x (1÷PCLK Divide)

Where:

A = Horizontal size of the PIP1 window
B = Horizontal scale rate
HT = Horizontal total of the panel

Examples:

For a horizontal scale rate of 1/2 and a vertical scale rate of 1/2, with a horizontal PIP window size of 200, horizontal total of 480, and a PCLK divide of 1/2, the following calculation would be used.

200 x (1 ÷ (1/2)) x 2 + 64 < 480 x (1 ÷ (1/2))
864 < 960 (this case is valid)

For a horizontal scale rate of 1/2 and a vertical scale rate of 1/2, with a horizontal PIP

window size of 300, horizontal total of 480, and a PCLK divide of 1/2, the following calculation would be used.

300 x (1 ÷ (1/2)) x 2 + 64 < 480 x (1 ÷ (1/2))
1264 < 960 (this case is **not** valid)

For a horizontal scale rate of 1 and a vertical scale rate of 1/8, with a horizontal PIP window size of 192, horizontal total of 920, and a PCLK divide of 1/2, the following calculation would be used.

(A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 7) + 64 < HT x (1÷PCLK Divide)
(192 x 1 x 2) + (192 x 1 x 7) + 64 < 920 x 2
1792 < 1840 (this case is valid)

For a horizontal scale rate of 1 and a vertical scale rate of 1/8, with a horizontal PIP window size of 200, horizontal total of 920, and a PCLK divide of 1/2, the following calculation would be used.

(A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 7) + 64 < HT x (1÷PCLK Divide)
(200 x 1 x 2) + (200 x 1 x 7) + 64 < 920 x 2
1864 < 1840 (this case is **not** valid)

REG[0266h] PIP1 Scaler Port Address Counter Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a			PIP1 Scaler Port Address Counter bits 4-0 (RO)				
7	6	5	4	3	2	1	0
n/a			Filter Coefficient Select	n/a		Reserved	Port Address Counter Reset (WO)

bits 12-8 PIP1 Scaler Port Address Counter bits [4:0] (Read Only)

These bits indicate the address (or index) into the PIP1 Scaler Filter Coefficient table. There are two tables, one for each of the horizontal and vertical filters, which are selected using the PIP1 Scaler Filter Coefficient Select bit, REG[0266h] bit 4.

After each write to the PIP1 Scaler Filter Coefficient Table Access Port (REG[0268h] bits 7-0) is completed, this counter is automatically incremented up to a value of 1Fh. When the port address counter value reaches 1Fh, it must be manually reset to 00h. This counter is not incremented when the PIP1 Scaler Filter Coefficient Table Access Port is read.

bit 4 PIP1 Scaler Filter Coefficient Select

This bit selects which scaler filter coefficient table (Horizontal Filter or Vertical Filter) is accessed through the PIP1 Scaler Filter Coefficient Table Access Port, REG[0268h] bits 7-0.
When this bit = 0b, the PIP1 scaler horizontal filter coefficient table is selected.
When this bit = 1b, the PIP1 scaler vertical filter coefficient table is selected.

bit 1 Reserved

The default value for this bit is 0b.

bit 0 PIP1 Scaler Port Address Counter Reset (Write Only)
This bit resets the PIP1 Scaler Port Address Counter, REG[0266h] bits 12-8.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit resets the PIP1 Scaler Port Address Counter.

REG[0268h] PIP1 Scaler Coefficient Table Access Port Register
Default = 0000h — Write Only

n/a							
15	14	13	12	11	10	9	8
PIP1 Scaler Filter Coefficient Table Access Port bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 PIP1 Scaler Filter Coefficient Table Access Port bits [7:0] (Write Only)
These bits are the access port for the PIP1 scaler horizontal/vertical filter coefficient tables. The PIP1 Scaler Filter Coefficient Select bit is used to select whether the horizontal or vertical filter coefficient table is accessed (see REG[0266h] bit 4). The filter coefficients **must** be set before the scaler filter operation starts.

The Scaler horizontal filter and vertical filter coefficients should be set according to the values shown in Table 10-20: “PIP1 Filter Coefficient Examples”. The column used varies based on the scaling rates which are set individually for the horizontal filter (REG[0262h]) and the vertical filter (REG[0264h]).

Example interpolation filter coefficients are listed below.
Every coefficient has 8-bit accuracy. The msb is a sign bit, the lower 6 bits define the fractional part, and bit 6 is the integer part.

Table 10-20: PIP1 Filter Coefficient Examples

Port Address	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
Cubic-1.0	00h	FDh	FBh	F8h	F7h	F7h	FAh	00h	08h	13h	1Dh	28h	31h	39h	3Eh	40h
Cubic-0.5	00h	FFh	FEh	FCh	FCh	FCh	FEh	00h	05h	0Eh	18h	24h	2Eh	37h	3Dh	40h
B-spline	00h	00h	01h	02h	03h	05h	08h	0Bh	0Fh	14h	19h	1Eh	23h	27h	29h	2Ah
Linear	00h	00h	00h	00h	00h	00h	00h	00h	08h	10h	18h	20h	28h	30h	38h	40h
Average	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	20h

REG[026Ah] through REG[026Ch] are Reserved

These registers are Reserved and should not be written.

REG[026Eh] PIP1 Scaler Control Register
Default = 0000h — Read/Write

PIP1 Scaler Software Reset (WO)	n/a		Reserved	n/a			
15	14	13	12	11	10	9	8
Reserved	n/a						
7	6	5	4	3	2	1	0

bit 15	PIP1 Scaler Software Reset (Write Only) This bit initiates a software reset of the PIP1 scaler module. Performing a software reset of the PIP1 scaler using this bit has no effect on other LCDC functions. Writing a 0b to this bit has no hardware effect. Writing a 1b to this bit initiates a software reset of the PIP1 scaler module.
bit 12	Reserved The default value of this bit is 0b.
bit 7	Reserved This bit should be set to 0.

REG[0270h] PIP1 Window Scroll Start Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
PIP1 Window Scroll Start Address bits 15-8							
PIP1 Window Scroll Start Address bits 7-2						n/a	
7	6	5	4	3	2	1	0

REG[0272h] PIP1 Window Scroll Start Address Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
n/a				PIP1 Window Scroll Start Address bits 19-16			
7	6	5	4	3	2	1	0

REG[0272h] bits 3-0

REG[0270h] bits 15-2 PIP1 Window Scroll Start Address bits [19:2]

These bits specify the scroll start address for the PIP1 window in the display buffer. To disable scrolling for the PIP1 window, set the PIP1 Window Scroll Start Address to 0h (REG[0270h] ~ REG[0272h]) and the PIP1 Window Scroll End Address to the maximum value (REG[0274h] ~ REG[0276h]). For further information on scrolling, see Section 13.4, “Scroll Buffer” on page 153.

Note

1. The PIP1 Window Scroll Start Address must be less than the PIP1 Window Scroll End Address.
   REG[0270h] ~ REG[0272h] < REG[0274h] ~ REG[0276h]
2. The PIP1 Window Display Start Address must be less than the PIP1 Window Scroll End Address.
   REG[0278h] ~ REG[027Ah] < REG[0274h] ~ REG[0276h]

REG[0274h] PIP1 Window Scroll End Address Register 0
Default = FFFCh — Read/Write

PIP1 Window Scroll End Address bits 15-8							
15	14	13	12	11	10	9	8
PIP1 Window Scroll End Address bits 7-2						n/a	
7	6	5	4	3	2	1	0

REG[0276h] PIP1 Window Scroll End Address Register 1
Default = 000Fh — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				PIP1 Window Scroll End Address bits 19-16			
7	6	5	4	3	2	1	0

REG[0276h] bits 3-0

REG[0274h] bits 15-2 PIP1 Window Scroll End Address bits [19:2]

These bits specify the scroll end address for the PIP1 window in the display buffer. If the current PIP1 window display memory address is bigger than this address, the PIP1 Window Display address goes to the PIP1 Window Scroll Start Address. To disable scrolling for the PIP1 window, set the PIP1 Window Scroll Start Address to 0h (REG[0270h] ~ REG[0272h]) and the PIP1 Window Scroll End Address to the maximum value (REG[0274h] ~ REG[0276h]). For further information on scrolling, see Section 13.4, "Scroll Buffer" on page 153.

Note

1. The PIP1 Window Scroll Start Address must be less than the PIP1 Window Scroll End Address.
   REG[0270h] ~ REG[0272h] < REG[0274h] ~ REG[0276h]
2. The PIP1 Window Display Start Address must be less than the PIP1 Window Scroll End Address.
   REG[0278h] ~ REG[027Ah] < REG[0274h] ~ REG[0276h]

REG[0278h] PIP1 Window Display Start Address Register 0
Default = 0000h — Read/Write

PIP1 Window Display Start Address bits 15-8							
15	14	13	12	11	10	9	8
PIP1 Window Display Start Address bits 7-1							n/a
7	6	5	4	3	2	1	0

REG[027Ah] PIP1 Window Display Start Address Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				PIP1 Window Display Start Address bits 19-16			
7	6	5	4	3	2	1	0

REG[027Ah] bits 3-0
REG[0278h] bits 15-1 PIP1 Window Display Start Address bits [19:1]

These bits specify the start address of the PIP1 window image in the display buffer.

Note

1. The PIP1 Window Display Start Address must be less than the PIP1 Window Scroll End Address.
   REG[0278h] ~ REG[027Ah] < REG[0274h] ~ REG[0276h]
2. These bits must be set to a 32-bit aligned value (REG[0278h] bit 1 = 0b).

REG[027Ch] PIP1 Window Line Address Offset Register
Default = 0000h — Read/Write

n/a				PIP1 window Line Address Offset bit 11-8			
15	14	13	12	11	10	9	8
PIP1 window Line Address Offset bit 7-1							n/a
7	6	5	4	3	2	1	0

bits 11-1 PIP1 Window Line Address Offset bits [11:1]

These bits specify the offset from the beginning of one display line to the beginning of the next display line in the memory used for the PIP1 window. Calculate the Line Address Offset as follows (valid for both pixel doubling enabled and disabled).

REG[027Ch] bits 11-0 = Line width in pixels x 16 ÷ 8

Note

These bits must be set to a 32-bit aligned value (REG[027Ch] bit 1 = 0b).

REG[027Eh] PIP1 Source Image Horizontal Size Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							PIP1 Source Image Horizontal Size bit 8
7	6	5	4	3	2	1	0
PIP1 Source Image Horizontal Size bits 7-1							n/a

bits 8-1 PIP1 Source Image Horizontal Size bits [8:1]

These bits specify the horizontal size (or width) of the PIP1 source image, in pixels.

REG[027Eh] bits 8-1 = PIP1 Source Image Horizontal Size in pixels

Note

1. These bits must be set to an even number of pixels.
2. These bits must be set such that the following formula is valid.
   REG[027Eh] bits 8-1 ≥ 4

REG[0280h] PIP1 Source Image Vertical Size Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						PIP1 Source Image Vertical Size bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Source Image Vertical Size bits 7-0							

bits 9-0 PIP1 Source Image Vertical Size bits [9:0]

These bits specify the vertical size (or height) of the PIP1 source image, in pixels.

REG[0280h] bits 9-0 = PIP1 Source Image Vertical Size in pixels

Note

These bits must be set such that the following formula is valid.

REG[0280h] bits 9-0 ≥ 4

REG[0282h] Pseudo Setting Register
Default = 0020h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a		Pseudo RGB Output Color Format bits 1-0		n/a	Pseudo Color Output Mode bits 2-0		
7	6	5	4	3	2	1	0

bits 5-4 Pseudo RGB Output Color Format bits [1:0]

When a valid Pseudo Color Output Mode is selected (see REG[0282h] bits 2-0), these bits select the RGB format that is output to the LCD panel interface. It is recommended that these bits be set according to the data width of the panel (i.e. 18-bit panel uses RGB 6:6:6).

Table 10-21: Pseudo Output Color Format

REG[0282h] bits 5-4	Pseudo Output Color Format
00b	RGB 4:4:4
01b	RGB 5:6:5
10b (default)	RGB 6:6:6
11b	Reserved

bits 2-0 Pseudo Color Output Mode bits [2:0]

These bits select the method used to convert internal RGB 8:8:8 image data into RGB 4:4:4, RGB 5:6:5, or RGB 6:6:6 data for output to the LCD interface. This function is designed for panels with data widths of less than 24-bit. The output color format is selected using the Pseudo RGB Output Color Format bits, REG[0282h] bits 5-4.

The following methods are available.

Table 10-22: Pseudo Color Output Mode

REG[0282h] bits 2-0	Pseudo Mode
000b (default)	Disable (Pass-through)
001b	2x2 Matrix Dither Enable
010b	FRM Enable
011b	Reserved
100b	Error Diffusion Enable
101b ~ 111b	Reserved

REG[0290h] through REG[0292h] are Reserved

These registers are Reserved and should not be written.

10.4.9 PIP2 Window Configuration Register

REG[02A0h] PIP2 Scaling Mode Register Default = 0000h							Read/Write
PIP2 Edge Enhance Enable	n/a				PIP2 Edge Enhance Effect bits 2-0		
15	14	13	12	11	10	9	8
PIP2 Vertical Scaling Enable	n/a	PIP2 Vertical Filter Mode Select	n/a	PIP2 Horizontal Scaling Enable	n/a	PIP2 Horizontal Filter Mode Select	n/a
7	6	5	4	3	2	1	0

bit 15 PIP2 Edge Enhance Enable

This bit controls the edge enhancement effect for PIP2 window.
When this bit = 0b, the edge enhancement effect for the PIP2 window is disabled.
When this bit = 1b, the edge enhancement effect for the PIP2 window is enabled.

Note

When the PIP2 Transparency is enabled (REG[0204h] bit 2 = 1b), PIP2 edge enhancement should be disabled, REG[02A0h] bit 15 = 0b.

bits 10-8 PIP2 Edge Enhance Effect bits [2:0]

These bits only have an effect when PIP2 edge enhance is enabled, REG[02A0h] bit 15 = 1b. These bits specify the strength of the edge enhancement effect.
A value of 001b specifies the weakest edge enhancement and a value of 111b specifies the strongest edge enhancement. A value of 000b disables the edge enhancement effect.

bit 7 PIP2 Vertical Scaling Enable

This bit controls vertical scaling for the PIP2 window. For details on configuring vertical scaling, see Section 13.2.2, “Using The Scalers” on page 146.
When this bit = 0b, vertical scaling for PIP2 is disabled.
When this bit = 1b, vertical scaling for PIP2 is enabled.

bits 5 PIP2 Vertical Filter Mode Select

This bit sets the filter mode for vertical scaling of the PIP2 window. For details on configuring vertical scaling, see Section 13.2.2, “Using The Scalers” on page 146.
When this bit = 0b, the vertical scaling filter is disabled.
When this bit = 1b, the vertical scaling filter is enabled.

Table 10-23: PIP2 Vertical Filter Mode

REG[02A0h] bits 5	PIP2 Vertical Filter Mode
0b	Line replication/decimation
1b	SINC interpolation function as an impulse response

Note

When the PIP2 Transparency is enabled (REG[0204h] bit 2 = 1b), the vertical scaling filter should be disabled, REG[02A0h] bit 5 = 0b.

bit 3 PIP2 Horizontal Scaling Enable
This bit controls horizontal scaling for the PIP2 window. For details on configuring vertical scaling, see Section 13.2.2, “Using The Scalers” on page 146.
When this bit = 0b, horizontal scaling for the PIP2 is disabled.
When this bit = 1b, horizontal scaling for the PIP2 is enabled.

bit 1 PIP2 Horizontal Filter Mode Select
This bit sets the filter mode for horizontal scaling of the PIP2 window. For details on configuring vertical scaling, see Section 13.2.2, “Using The Scalers” on page 146.
When this bit = 0b, the horizontal scaling filter is disabled.
When this bit = 1b, the horizontal scaling filter is enabled.

Table 10-24: PIP2 Horizontal Filter Mode

REG[02A0h] bits 1	PIP2 Horizontal Filter Mode
0b	Pixel replication/decimation
1b	SINC interpolation function as an impulse response

Note
When the PIP2 Transparency is enabled (REG[0204h] bit 2 = 1b), the horizontal scaling filter should be disabled, REG[02A0h] bit 1 = 0b.

REG[02A2h] PIP2 Scaler Horizontal Scale Register
Default = 0000h Read/Write

Reserved			PIP2 Horizontal Scale bits 12-8				
15	14	13	12	11	10	9	8
PIP2 Horizontal Scale bits 7-0							
7	6	5	4	3	2	1	0

bits 15-13 Reserved
The default value for these bits is 000b.

bits 12-0 PIP2 Horizontal Scale bits [12:0]
These bits determine the horizontal scaling factor for the PIP2 scaler and must be programmed based on the following formula.
REG[02A2h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)

The fractional point is to the right of bit 10. If the scaling mode is ZOOM (Scaled up), REG[02A2h] bits 12-10 should equal zero. If the scaling mode is SHRINK (Scaled down), REG[02A2h] bits 12-10 should be non-zero.

Example: For a scaling ratio of 3.51 (Zoom case), REG[02A2h] bits 12-0 should be programmed as follows.

REG[02A2h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)
= 1024 x (1 ÷ 3.51)
= 291 (round down)
= 123h

Note
The scale-down rate depends on the PCLK (Dot Clock), size of the panel, and the PIP2 window size. The horizontal scale rate must observe the following formula.
Horizontal Scale Rate ≥ PCLK Divide

For example, selecting a horizontal scale rate of 1/2 and a PCLK Divide of 1/2 is valid. Selecting a horizontal scale rate of 1/3 and a PCLK Divide of 1/2 is not valid.

REG[02A4h] PIP2 Scaler Vertical Scale Register
Default = 0000h Read/Write

Reserved			PIP2 Vertical Scale bits 12-8				
15	14	13	12	11	10	9	8
PIP2 Vertical Scale bits 7-0							
7	6	5	4	3	2	1	0

bits 15-13 Reserved
The default value for these bits is 000b.

bits 12-0 PIP2 Vertical Scale bits [12:0]
These bits determine the vertical scaling factor for the PIP2 scaler and must be programmed based on the following formula.
REG[02A4h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)

The fractional point is to the right of bit 10. If the scaling mode is ZOOM (Scaled up), REG[02A2h] bits 12-10 should equal zero. If the scaling mode is SHRINK (Scaled down), REG[0262h] bits 12-10 should be non-zero.

Example: For a scaling ratio of 3.51 (Zoom case), REG[02A4h] bits 12-0 should be programmed as follows.

REG[02A4h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)
= 1024 x (1 ÷ 3.51)
= 291 (round down)
= 123h

Note

The scale-down rate depends on the PCLK (Dot Clock), size of the panel, and the PIP2 window size. Two different sets of formulas must be observed based on the relationship between the Horizontal Scale Rate and the PCLK Divide.

When the PCLK Divide is less than the Horizontal Scale Rate and the Horizontal Scale Rate is less than or equal to 1 (PCLK < Horizontal Scale Rate ≤ 1), the following formulas must be observed.

For a Vertical Scale Rate of:

1 to 1/2: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 1) + 64 < HT x (1÷PCLK Divide)
1/2 to 1/3: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 2) + 64 < HT x (1÷PCLK Divide)
1/3 to 1/4: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 3) + 64 < HT x (1÷PCLK Divide)
1/4 to 1/5: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 4) + 64 < HT x (1÷PCLK Divide)
1/5 to 1/6: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 5) + 64 < HT x (1÷PCLK Divide)
1/6 to 1/7: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 6) + 64 < HT x (1÷PCLK Divide)
1/7 to 1/8: (A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 7) + 64 < HT x (1÷PCLK Divide)

Where:
A = Horizontal size of the PIP1 window
B = Horizontal scale rate
HT = Horizontal total of the panel

When the PCLK Divide is equal to the Horizontal Scale Rate (PCLK = Horizontal Scale Rate), the following formulas must be observed.

For a Vertical Scale Rate of:

1 to 1/2: (A x (1÷B) x 2 + 64 < HT x (1÷PCLK Divide)
1/2 to 1/3: (A x (1÷B) x 3 + 64 < HT x (1÷PCLK Divide)
1/3 to 1/4: (A x (1÷B) x 4 + 64 < HT x (1÷PCLK Divide)
1/4 to 1/5: (A x (1÷B) x 5 + 64 < HT x (1÷PCLK Divide)
1/5 to 1/6: (A x (1÷B) x 6 + 64 < HT x (1÷PCLK Divide)
1/6 to 1/7: (A x (1÷B) x 7 + 64 < HT x (1÷PCLK Divide)
1/7 to 1/8: (A x (1÷B) x 8 + 64 < HT x (1÷PCLK Divide)

Where:
A = Horizontal size of the PIP1 window
B = Horizontal scale rate
HT = Horizontal total of the panel

Examples:

For a horizontal scale rate of 1/2 and a vertical scale rate of 1/2, with a horizontal PIP window size of 200, horizontal total of 480, and a PCLK divide of 1/2, the following calculation would be used.
200 x (1 ÷ (1/2)) x 2 + 64 < 480 x (1 ÷ (1/2))
864 < 960 (this case is valid)

For a horizontal scale rate of 1/2 and a vertical scale rate of 1/2, with a horizontal PIP

window size of 300, horizontal total of 480, and a PCLK divide of 1/2, the following calculation would be used.
300 x (1 ÷ (1/2)) x 2 + 64 < 480 x (1 ÷ (1/2))
1264 < 960 (this case is **not** valid)

For a horizontal scale rate of 1 and a vertical scale rate of 1/8, with a horizontal PIP window size of 192, horizontal total of 920, and a PCLK divide of 1/2, the following calculation would be used.
(A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 7) + 64 < HT x (1÷PCLK Divide)
(192 x 1 x 2) + (192 x 1 x 7) + 64 < 920 x 2
1792 < 1840 (this case is valid)

For a horizontal scale rate of 1 and a vertical scale rate of 1/8, with a horizontal PIP window size of 200, horizontal total of 920, and a PCLK divide of 1/2, the following calculation would be used.
(A x (1÷B) x (1÷PCLK Divide)) + (A x (1÷B) x 7) + 64 < HT x (1÷PCLK Divide)
(200 x 1 x 2) + (200 x 1 x 7) + 64 < 920 x 2
1864 < 1840 (this case is **not** valid)

REG[02A6h] PIP2 Scaler Port Address Counter Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a			PIP2 Scaler Port Address Counter bits 4-0 (RO)				
7	6	5	4	3	2	1	0
n/a			PIP2 Scaler Filter Coefficient Select	n/a		Reserved	PIP2 Scaler Port Address Counter Reset (WO)

bits 12-8 PIP2 Scaler Port Address Counter bits [4:0] (Read Only)

These bits indicate the address (or index) into the PIP2 Scaler Filter Coefficient table. There are two tables, one for each of the horizontal and vertical filters, which are selected using the PIP2 Scaler Filter Coefficient Select bit, REG[02A6h] bit 4.

After each write to the PIP2 Scaler Filter Coefficient Table Access Port (REG[02A8h] bits 7-0) is completed, this counter is automatically incremented up to a value of 1Fh. When the port address counter value reaches 1Fh, it must be manually reset to 00h. This counter is not incremented when the PIP2 Scaler Filter Coefficient Table Access Port is read.

bit 4 PIP2 Scaler Filter Coefficient Select

This bit selects which scaler filter coefficient table (horizontal filter or vertical filter) is accessed through the PIP2 Scaler Filter Coefficient Table Access Port, REG[02A8h] bits 7-0.
When this bit = 0b, the PIP2 scaler horizontal filter coefficient table is selected.
When this bit = 1b, the PIP2 scaler vertical filter coefficient table is selected.

bit 1 Reserved

The default value for this bit is 0b.

bit 0 PIP2 Scaler Port Address Counter Reset (Write Only)
This bit resets the PIP2 Scaler Port Address Counter, REG[02A6h] bits 12-8.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit resets the PIP2 Scaler Port Address Counter.

REG[02A8h] PIP2 Scaler Coefficient Table Access Port Register
Default = 0000h — Write Only

n/a							
15	14	13	12	11	10	9	8
PIP2 Scaler Filter Coefficient Table Access Port bits 7-0 (WO)							
7	6	5	4	3	2	1	0

bits 7-0 PIP2 Scaler Filter Coefficient Table Access Port bits [7:0] (Write Only)
These bits are the access port for the PIP2 scaler horizontal/vertical filter coefficient tables. The PIP2 Scaler Filter Coefficient Select bit is used to select whether the horizontal or vertical filter coefficient table is accessed (see REG[0266h] bit 4). The filter coefficients **must** be set before the scaler filter operation starts.

The Scaler horizontal filter and vertical filter coefficients should be set according to the values shown in Table 10-25: “PIP2 Filter Coefficient Examples”. The column used varies based on the scaling rates which are set individually for the horizontal filter (REG[02A2h]) and the vertical filter (REG[02A4h]).

Example interpolation filter coefficients are listed below.
Every coefficient has 8-bit accuracy. The MSB is a sign bit, the lower 6 bits define the fractional part, and bit 6 is the integer part.

Table 10-25: PIP2 Filter Coefficient Examples

Port Address	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
Cubic-1.0	00h	FDh	FBh	F8h	F7h	F7h	FAh	00h	08h	13h	1Dh	28h	31h	39h	3Eh	40h
Cubic-0.5	00h	FFh	FEh	FCh	FCh	FCh	FEh	00h	05h	0Eh	18h	24h	2Eh	37h	3Dh	40h
B-spline	00h	00h	01h	02h	03h	05h	08h	0Bh	0Fh	14h	19h	1Eh	23h	27h	29h	2Ah
Linear	00h	00h	00h	00h	00h	00h	00h	00h	08h	10h	18h	20h	28h	30h	38h	40h
Average	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	20h

REG[02AAh] through REG[02ACh] are Reserved

These registers are Reserved and should not be written.

REG[02AEh] PIP2 Scaler Control Register
Default = 0000h — Read/Write

PIP2 Scaler Software Reset (WO)	n/a		Reserved	n/a			
15	14	13	12	11	10	9	8
Reserved	n/a	Reserved		n/a			
7	6	5	4	3	2	1	0

bit 15 PIP2 Scaler Software Reset (Write Only)
This bit initiates a software reset of the PIP2 scaler module. Performing a software reset of the PIP2 scaler using this bit has no effect on other LCDC functions.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit initiates a software reset of the Scaler module.

bit 12 Reserved
The default value of this bit is 0b.

bit 7 Reserved

This bit should be set to 0.

bits 5-4 Reserved

These bits should be set to 00b.

REG[02B0h] PIP2 Window Scroll Start Address Register 0
Default = 0000h — Read/Write

PIP2 Window Scroll Start Address bits 15-8							
15	14	13	12	11	10	9	8
PIP2 Window Scroll Start Address bits 7-2						n/a	
7	6	5	4	3	2	1	0

REG[02B2h] PIP2 Window Scroll Start Address Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				PIP2 Window Scroll Start Address bits 19-16			
7	6	5	4	3	2	1	0

REG[02B2h] bits 3-0
REG[02B0h] bits 15-2 PIP2 Window Scroll Start Address bits [19:2]
These bits specify scroll start address for the PIP2 window in the display buffer. To disable scrolling for the PIP2 window, set the PIP2 Window Scroll Start Address to 0h (REG[02B0h] ~ REG[02B2h]) and the PIP2 Window Scroll End Address to the maximum value (REG[02B4h] ~ REG[02B6h]). For further information on scrolling, see Section 13.4, “Scroll Buffer” on page 153.

Note

1. The PIP2 Window Scroll Start Address must be less than the PIP2 Window Scroll End Address.
   REG[02B0h] ~ REG[02B2h] < REG[02B4h] ~ REG[02B6h]
2. The PIP2 Window Display Start Address must be less than the PIP2 Window Scroll End Address.
   REG[02B8h] ~ REG[02BAh] < REG[02B4h] ~ REG[02B6h]

REG[02B4h] PIP2 Window Scroll End Address Register 0
Default = FFFCh Read/Write

PIP2 Window Scroll End Address bits 15-8							
15	14	13	12	11	10	9	8
PIP2 Window Scroll End Address bits 7-2						n/a	
7	6	5	4	3	2	1	0

REG[02B6h] PIP2 Window Scroll End Address Register 1
Default = 000Fh Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				PIP2 Window Scroll End Address bits 19-16			
7	6	5	4	3	2	1	0

REG[02B6h] bits 3-0

REG[02B4h] bits 15-2 PIP2 Window Scroll End Address bits [19:2]

These bits specify scroll end address for the PIP2 window in the display buffer. If the current PIP2 window display memory address is larger than this address, the PIP2 window display address goes to the PIP2 Window Scroll Start Address. To disable scrolling for the PIP2 window, set the PIP2 Window Scroll Start Address to 0h (REG[02B0h] ~ REG[02B2h]) and the PIP2 Window Scroll End Address to the maximum value (REG[02B4h] ~ REG[02B6h]). For further information on scrolling, see Section 13.4, “Scroll Buffer” on page 153.

Note

1. The PIP2 Window Scroll Start Address must be less than the PIP2 Window Scroll End Address.
   REG[02B0h] ~ REG[02B2h] < REG[02B4h] ~ REG[02B6h]
2. The PIP2 Window Display Start Address must be less than the PIP2 Window Scroll End Address.
   REG[02B8h] ~ REG[02BAh] < REG[02B4h] ~ REG[02B6h]

REG[02B8h] PIP2 Window Display Start Address Register 0

Default = 0000h — Read/Write

PIP2 Window Display Start Address bits 15-8							
15	14	13	12	11	10	9	8
PIP2 Window Display Start Address bits 7-1							n/a
7	6	5	4	3	2	1	0

REG[02BAh] PIP2 Window Display Start Address Register 1

Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				PIP2 Window Display Start Address bits 19-16			
7	6	5	4	3	2	1	0

REG[02BAh] bits 3-0
REG[02B8h] bits 15-1 PIP2 Window Display Start Address bits [19:1]

These bits specify the start address of the PIP2 window image in the display buffer.

Note

1. The PIP2 Window Display Start Address must be less than the PIP2 Window Scroll End Address.
   REG[02B8h] ~ REG[02BAh] < REG[02B4h] ~ REG[02B6h]
2. These bits must be set to a 32-bit aligned value (REG[02B8h] bit 1 = 0b).

REG[02BCh] PIP2 Window Line Address Offset Register

Default = 0000h — Read/Write

n/a				PIP2 window Line Address Offset bit 11-8			
15	14	13	12	11	10	9	8
PIP2 window Line Address Offset bit 7-1							n/a
7	6	5	4	3	2	1	0

bits 11-1 PIP2 Window Line Address Offset bits [11:1]

These bits specify the offset from the beginning of one display line to the beginning of the next display line in the memory used for the PIP2 window. Calculate the Line Address Offset as follows (valid for both pixel doubling enabled and disabled).

REG[02BCh] bits 11-0 = Line width in pixels x 16 ÷ 8

Note

These bits must be set to a 32-bit aligned value (REG[02BCh] bit 1 = 0b).

REG[02BEh] PIP2 Source Image Horizontal Size Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							PIP2 Source Image Horizontal Size bit 8
PIP2 Source Image Horizontal Size bits 7-1							n/a
7	6	5	4	3	2	1	0

bits 8-1 PIP2 Source Image Horizontal Size bits [8:1]

These bits specify the horizontal size (or width) of the PIP2 source image, in pixels.

REG[02BEh] bits 8-1 = PIP2 Source Image Horizontal Size in pixels

Note

1. These bits must be set to an even number of pixels.
2. These bits must be set such that the following formula is valid.
   REG[02BEh] bits 8-1 ≥ 4

REG[02C0h] PIP2 Source Image Vertical Size Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP2 Source Image Vertical Size bits 9-8	
PIP2 Source Image Vertical Size bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP2 Source Image Vertical Size bits [9:0]

These bits specify the vertical size (or height) of the PIP2 source image, in pixels.

REG[02C0h] bits 9-0 = PIP2 Source Image Vertical Size in pixels

Note

These bits must be set such that the following formula is valid.

REG[02C0h] bits 9-0 ≥ 4

REG[02E0h] through REG[02E2h] are Reserved

These registers are Reserved and should not be written.

10.4.10 GPIO Registers

REG[0300h] GPIO Configuration Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
GPIO15 Configuration	GPIO14 Configuration	GPIO13 Configuration	GPIO12 Configuration	GPIO11 Configuration	GPIO10 Configuration	GPIO9 Configuration	GPIO8 Configuration
7	6	5	4	3	2	1	0
GPIO7 Configuration	GPIO6 Configuration	GPIO5 Configuration	GPIO4 Configuration	GPIO3 Configuration	GPIO2 Configuration	GPIO1 Configuration	GPIO0 Configuration

REG[0302h] GPIO Configuration Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
GPIO23 Configuration	GPIO22 Configuration	GPIO21 Configuration	GPIO20 Configuration	GPIO19 Configuration	GPIO18 Configuration	GPIO17 Configuration	GPIO16 Configuration
7	6	5	4	3	2	1	0

REG[0302h] bits 7-0
REG[0300h] bits 15-0 GPIO[23:0] Configuration
These bits configure each individual GPIO pin between an input or an output.
When this bit = 0b, the corresponding GPIO pin is configured as an input pin. (default)
When this bit = 1b, the corresponding GPIO pin is configured as an output pin.

REG[0304h] GPIO Input Enable Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
GPIO15 Input Enable	GPIO14 Input Enable	GPIO13 Input Enable	GPIO12 Input Enable	GPIO11 Input Enable	GPIO10 Input Enable	GPIO9 Input Enable	GPIO8 Input Enable
7	6	5	4	3	2	1	0
GPIO7 Input Enable	GPIO6 Input Enable	GPIO5 Input Enable	GPIO4 Input Enable	GPIO3 Input Enable	GPIO2 Input Enable	GPIO1 Input Enable	GPIO0 Input Enable

REG[0306h] GPIO Input Enable Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
GPIO23 Input Enable	GPIO22 Input Enable	GPIO21 Input Enable	GPIO20 Input Enable	GPIO19 Input Enable	GPIO18 Input Enable	GPIO17 Input Enable	GPIO16 Input Enable
7	6	5	4	3	2	1	0

REG[0306h] bits 7-0
REG[0304h] bits 15-0 GPIO[23:0] Input Enable
These bits enable the input function of each individual GPIO pin. They must be changed to a 1b after power-on/reset to enable the input function of the corresponding GPIO pin.
When this bit = 0b, the input function for the corresponding GPIO pin is disabled. (default)
When this bit = 1b, the input function for the corresponding GPIO pin is enabled.

REG[0308h] GPIO Pull-down Control Register 0
Default = FFFFh — Read/Write

GPIO15 Pull-down Control	GPIO14 Pull-down Control	GPIO13 Pull-down Control	GPIO12 Pull-down Control	GPIO11 Pull-down Control	GPIO10 Pull-down Control	GPIO9 Pull-down Control	GPIO8 Pull-down Control
15	14	13	12	11	10	9	8
GPIO7 Pull-down Control	GPIO6 Pull-down Control	GPIO5 Pull-down Control	GPIO4 Pull-down Control	GPIO3 Pull-down Control	GPIO2 Pull-down Control	GPIO1 Pull-down Control	GPIO0 Pull-down Control
7	6	5	4	3	2	1	0

REG[030Ah] GPIO Pull-down Control Register 1
Default = 00FFh — Read/Write

n/a							
15	14	13	12	11	10	9	8
GPIO23 Pull-down Control	GPIO22 Pull-down Control	GPIO21 Pull-down Control	GPIO20 Pull-down Control	GPIO19 Pull-down Control	GPIO18 Pull-down Control	GPIO17 Pull-down Control	GPIO16 Pull-down Control
7	6	5	4	3	2	1	0

REG[030Ah] bits 7-0
REG[0308h] bits 15-0 GPIO[23:0] Pull-down Control

All GPIO pins have internal pull-down resistors. These bits control the state of the pull-down resistor for each individual GPIO pin.
When the bit = 0b, the pull-down resistor for the associated GPIO pin is inactive.
When the bit = 1b, the pull-down resistor for the associated GPIO pin is active.

REG[030Ch] GPIO Status Register 0
Default = 0000h — Read/Write

GPIO15 Status	GPIO14 Status	GPIO13 Status	GPIO12 Status	GPIO11 Status	GPIO10 Status	GPIO9 Status	GPIO8 Status
15	14	13	12	11	10	9	8
GPIO7 Status	GPIO6 Status	GPIO5 Status	GPIO4 Status	GPIO3 Status	GPIO2 Status	GPIO1 Status	GPIO0 Status
7	6	5	4	3	2	1	0

REG[030Eh] GPIO Status Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
GPIO23 Status	GPIO22 Status	GPIO21 Status	GPIO20 Status	GPIO19 Status	GPIO18 Status	GPIO17 Status	GPIO16 Status
7	6	5	4	3	2	1	0

REG[030Eh] bits 7-0
REG[030Ch] bits 15-0 GPIO[23:0] Status

When GPIOx is configured as an output (see REG[0300h] ~ REG[0302h]), writing a 1b to these bits drives GPIOx high and writing a 0b to these bits drives GPIOx low.
When GPIOx is configured as an input (see REG[0300h] ~ REG[0302h]), a read from these bits returns the status of GPIOx.

REG[0310h] GPIO Positive Edge Interrupt Trigger Register 0
Default = 0000h — Read/Write

GPIO15 Positive Edge Trigger	GPIO14 Positive Edge Trigger	GPIO13 Positive Edge Trigger	GPIO12 Positive Edge Trigger	GPIO11 Positive Edge Trigger	GPIO10 Positive Edge Trigger	GPIO9 Positive Edge Trigger	GPIO8 Positive Edge Trigger
15	14	13	12	11	10	9	8
GPIO7 Positive Edge Trigger	GPIO6 Positive Edge Trigger	GPIO5 Positive Edge Trigger	GPIO4 Positive Edge Trigger	GPIO3 Positive Edge Trigger	GPIO2 Positive Edge Trigger	GPIO1 Positive Edge Trigger	GPIO0 Positive Edge Trigger
7	6	5	4	3	2	1	0

REG[0312h] GPIO Positive Edge Interrupt Trigger Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
GPIO23 Positive Edge Trigger	GPIO22 Positive Edge Trigger	GPIO21 Positive Edge Trigger	GPIO20 Positive Edge Trigger	GPIO19 Positive Edge Trigger	GPIO18 Positive Edge Trigger	GPIO17 Positive Edge Trigger	GPIO16 Positive Edge Trigger
7	6	5	4	3	2	1	0

REG[0312h] bits 7-0
REG[0310h] bits 15-0 GPIO[23:0] Positive Edge Trigger

These bits determine whether the corresponding GPIO interrupt (see REG[0318h] ~ REG[031Ah]) is triggered on the positive edge (when the GPIOx pin changes from 0 to 1).
When this bit = 0b, the corresponding GPIO interrupt is not triggered on the positive edge.
When this bit = 1b, the corresponding GPIO interrupt is triggered on the positive edge.

REG[0314h] GPIO Negative Edge Interrupt Trigger Register 0
Default = 0000h — Read/Write

GPIO15 Negative Edge Trigger	GPIO14 Negative Edge Trigger	GPIO13 Negative Edge Trigger	GPIO12 Negative Edge Trigger	GPIO11 Negative Edge Trigger	GPIO10 Negative Edge Trigger	GPIO9 Negative Edge Trigger	GPIO8 Negative Edge Trigger
15	14	13	12	11	10	9	8
GPIO7 Negative Edge Trigger	GPIO6 Negative Edge Trigger	GPIO5 Negative Edge Trigger	GPIO4 Negative Edge Trigger	GPIO3 Negative Edge Trigger	GPIO2 Negative Edge Trigger	GPIO1 Negative Edge Trigger	GPIO0 Negative Edge Trigger
7	6	5	4	3	2	1	0

REG[0316h] GPIO Negative Edge Interrupt Trigger Register 1
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
GPIO23 Negative Edge Trigger	GPIO22 Negative Edge Trigger	GPIO21 Negative Edge Trigger	GPIO20 Negative Edge Trigger	GPIO19 Negative Edge Trigger	GPIO18 Negative Edge Trigger	GPIO17 Negative Edge Trigger	GPIO16 Negative Edge Trigger
7	6	5	4	3	2	1	0

REG[0316h] bits 7-0
REG[0314h] bits 15-0 GPIO[23:0] Negative Edge Trigger

These bits determine whether the corresponding GPIO interrupt (see REG[0318h] ~ REG[031Ah]) is triggered on the negative edge (when the GPIOx pin changes from 1 to 0).
When this bit = 0b, the corresponding GPIO interrupt is not triggered on the negative edge.
When this bit = 1b, the corresponding GPIO interrupt is triggered on the negative edge.

REG[0318h] GPIO Interrupt Status Register 0

Default = 0000h — Read/Write

GPIO15 Interrupt Status	GPIO14 Interrupt Status	GPIO13 Interrupt Status	GPIO12 Interrupt Status	GPIO11 Interrupt Status	GPIO10 Interrupt Status	GPIO9 Interrupt Status	GPIO8 Interrupt Status
15	14	13	12	11	10	9	8
GPIO7 Interrupt Status	GPIO6 Interrupt Status	GPIO5 Interrupt Status	GPIO4 Interrupt Status	GPIO3 Interrupt Status	GPIO2 Interrupt Status	GPIO1 Interrupt Status	GPIO0 Interrupt Status
7	6	5	4	3	2	1	0

REG[031Ah] GPIO Interrupt Status Register 1

Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
GPIO23 Interrupt Status	GPIO22 Interrupt Status	GPIO21 Interrupt Status	GPIO20 Interrupt Status	GPIO19 Interrupt Status	GPIO18 Interrupt Status	GPIO17 Interrupt Status	GPIO16 Interrupt Status
7	6	5	4	3	2	1	0

REG[031Ah] bits 7-0

REG[0318h] bits 15-0 GPIO[23:0] Interrupt Status

These bits indicate the status of the corresponding GPIOx interrupt.
When this bit = 0b, a GPIOx interrupt has not occurred.
When this bit = 1b, a GPIOx interrupt has occurred.

To clear a GPIOx Interrupt Status bit, write a 1b then a 0b to the bit.

10.4.11 LUT Registers

REG[0400h] PIP2-LUT Address Counter Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
PIP2-LUT Address Counter bits 7-0							

bits 7-0 PIP2-LUT Address Counter bits [7:0]
These bits specify the address (or index) into the PIP2-LUT. The PIP2-LUT can be used for gamma control of the PIP2 window and consists of 256 RGB entries.

The RGB values are written into the PIP2-LUT using the PIP2-LUT Data Port (REG[0402h] bits 15-0) as shown in Table 10-26: "PIP2-LUT Data Mapping," on page 128. After each RGB data write to the PIP2-LUT Data Port is completed, the counter is automatically incremented up to a value of FFh. When the address counter value reaches FFh, the address counter is reset to 00h.

REG[0402h] PIP2-LUT Data Port Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
PIP2-LUT Data Port bits 15-8							
7	6	5	4	3	2	1	0
PIP2-LUT Data Port bits 7-0							

bits 15-0 PIP2-LUT Data Port bits [15:0]
These bits are the access port for setting the PIP2-LUT RGB data. The PIP2-LUT can only be accessed when the PIP2 window is disabled (REG[0202h] bit 2 = 0b) or the LCD Output Enable is set to "Display Off" (REG[0202h] bits 10 = 0b). The LUT data must be set as follows.

Table 10-26: PIP2-LUT Data Mapping

Cycle	PIP2-LUT Address (REG[0400h] bits 7-0)	REG[0402h] bits 15-8	REG[0402h] bits 7-0
1	00h	Green 0	Red 0
2	00h	n/a	Blue 0
3	01h	Green 1	Red 1
4	01h	n/a	Blue 1
•	•	•	•
•	•	•	•
•	•	•	•
511	FFh	Green 255	Red 255
512	FFh	n/a	Blue 255

REG[0500h] LCD-LUT Address Counter Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LCD-LUT Address Counter bits 7-0							

bits 7-0 LCD-LUT Address Counter bits [7:0]

These bits specify the address (or index) into the LCD-LUT. The LCD-LUT can be used for gamma control of the LCD display output and consists of 256 RGB entries.

The RGB values are written into the LCD-LUT using the LCD-LUT Data Port (REG[0502h] bits 15-0) as shown in Table 10-27: “LCD-LUT Data Mapping,” on page 129. After each RGB data write to the LCD-LUT Data Port is completed, the counter is automatically incremented up to a value of FFh. When the address counter value reaches FFh, the address counter is reset to 00h.

REG[0502h] LCD-LUT Data Port Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
LCD-LUT Data Port bits 15-8							
7	6	5	4	3	2	1	0
LCD-LUT Data Port bits 7-0							

bits 15-0 LCD-LUT Data Port bits [15:0]

These bits are the access port for setting the LCD-LUT RGB data. The LCD-LUT can only be accessed when the LCD-LUT is bypassed (REG[0200h] bit 5 = 1b) or the display is not active (REG[0202h] bit 13 = 0b). The LUT data must be set as follows.

Table 10-27: LCD-LUT Data Mapping

Cycle	LCD-LUT Address (REG[0500h] bits 7-0)	REG[0502h] bits 15-8	REG[0502h] bits 7-0
1	00h	Green 0	Red 0
2	00h	n/a	Blue 0
3	01h	Green 1	Red 1
4	01h	n/a	Blue 1
•	•	•	•
•	•	•	•
•	•	•	•
511	FFh	Green 255	Red 255
512	FFh	n/a	Blue 255

10.4.12 Interrupt Control Registers

REG[0A00h] Interrupt Status Register
Default = 0000h — Read Only

GPIO Interface Interrupt Status	n/a						
15	14	13	12	11	10	9	8
n/a			Host Interface Interrupt Status	n/a			Reserved
7	6	5	4	3	2	1	0

bit 15 GPIO Interface Interrupt Status (Read Only)
This bit indicates the status of the GPIO Interface interrupt. This bit is masked by the GPIO Interface Interrupt Enable bit and is only available when REG[0A02h] bit 15 = 1b.
When this bit = 0b, a GPIO Interface interrupt has not occurred.
When this bit = 1b, a GPIO Interface interrupt has occurred. To determine the exact nature of the interrupt, refer to the status bits in REG[0318h] ~ REG[031Ah] or the status of REG[0A04h] bit 15.

To clear this status bit, clear the interrupt condition in REG[0318h] ~ REG[031Ah] or REG[0A04h] bit 15, or disable the interrupt (REG[0A02h] bit 15 = 0b).

bit 4 Host Interface Interrupt Status (Read Only)
This bit indicates the status of the Host Interface interrupt. This bit is masked by the Host Interface Interrupt Enable bit and is only available when REG[0A02h] bit 4 = 1b.
When this bit = 0b, a Host Interface interrupt has not occurred.
When this bit = 1b, a Host Interface interrupt has occurred. To determine the exact nature of the interrupt, refer to the status bits in REG[0192h] or the status of REG[0A04h] bit 4.

To clear this status bit, clear the interrupt condition in REG[0192h] or REG[0A04h] bit 4, or disable the interrupt (REG[0A02h] bit 4 = 0b).

bit 0 Reserved
The default value for this bit is 0b.

REG[0A02h] Interrupt Control Register 0
Default = 0000h — Read/Write

GPIO Interface Interrupt Enable	n/a						
15	14	13	12	11	10	9	8
n/a			Host Interface Interrupt Enable	n/a			Reserved
7	6	5	4	3	2	1	0

bit 15 GPIO Interface Interrupt Enable
This bit controls the GPIO Interface interrupt. The status of the GPIO Interface interrupt is indicated by the GPIO Interface Interrupt Status bit, REG[0A00h] bit 15.
When this bit = 0b, the GPIO Interface interrupt is disabled.
When this bit = 1b, the GPIO Interface interrupt is enabled.

bit 4 Host Interface Interrupt Enable
This bit controls the Host Interface interrupt. The status of the Host Interface interrupt is indicated by the Host Interface Interrupt Status bit, REG[0A00h] bit 4.
When this bit = 0b, the Host Interface interrupt is disabled.
When this bit = 1b, the Host Interface interrupt is enabled.

bit 0 Reserved
The default value for this bit is 0b.

REG[0A04h] Interrupt Control Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
GPIO Interface Manual Interrupt	n/a						

7	6	5	4	3	2	1	0
n/a			Host Interface Manual Interrupt	n/a			Reserved

bit 15 GPIO Interface Manual Interrupt
This bit allows manual control of the GPIO Interface interrupt. Changes to this bit are reflected in the GPIO Interface Interrupt Status bit, REG[0A00h] bit 15.
When this bit = 0b, the GPIO Interface interrupt is cleared.
When this bit = 1b, the GPIO Interface interrupt is asserted.

bit 4 Host Interface Manual Interrupt
This bit allows manual control of the Host Interface interrupt. Changes to this bit are reflected in the Host Interface Interrupt Status bit, REG[0A00h] bit 4.
When this bit = 0b, the Host Interface interrupt is cleared.
When this bit = 1b, the Host Interface interrupt is asserted.

bit 0 Reserved
The default value for this bit is 0b.

11 Power Save Modes

11.1 Power-On/Power-Off Sequence

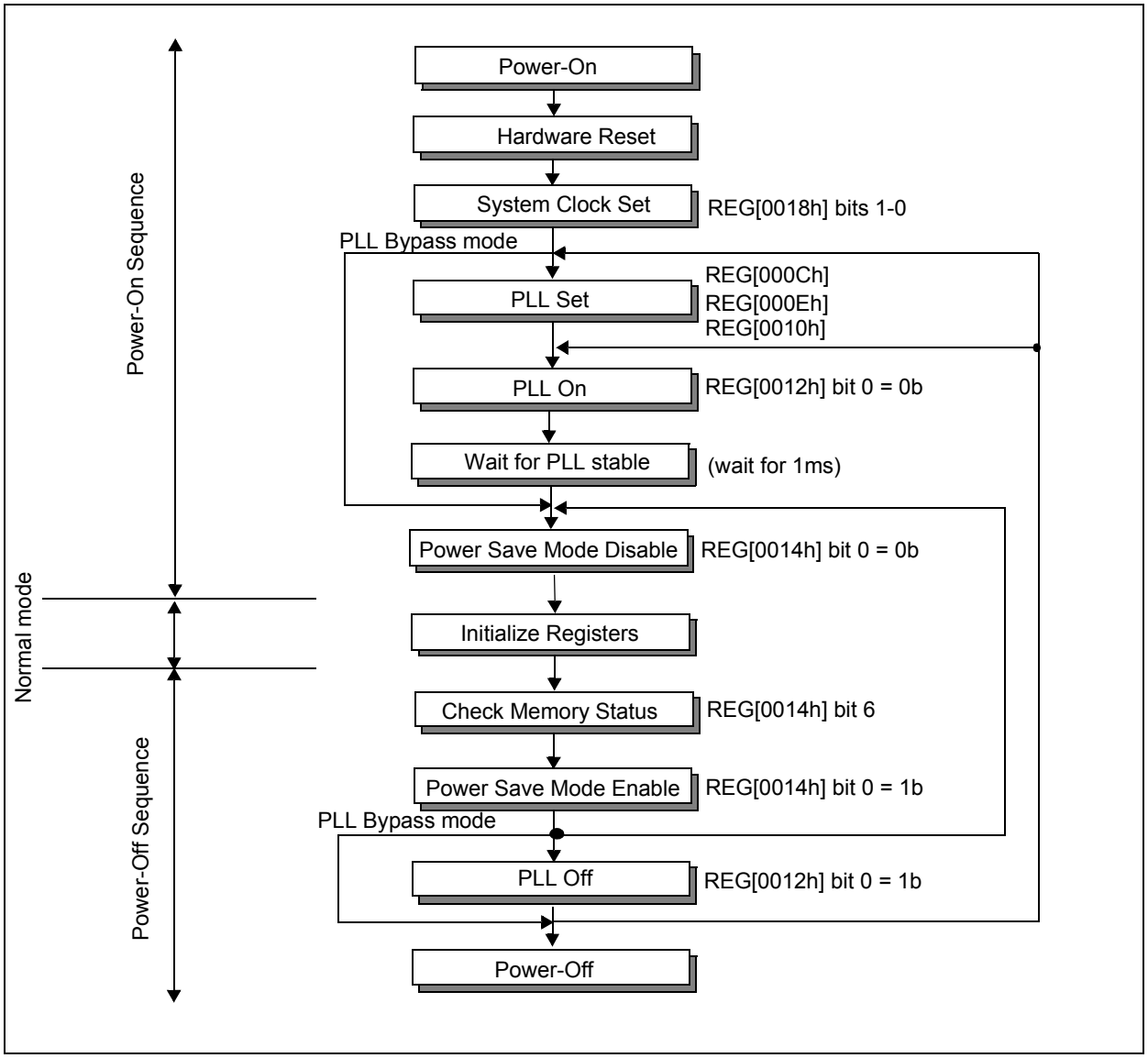


Figure 11-1: Power-On/Power-Off Sequence

11.2 Operational Modes

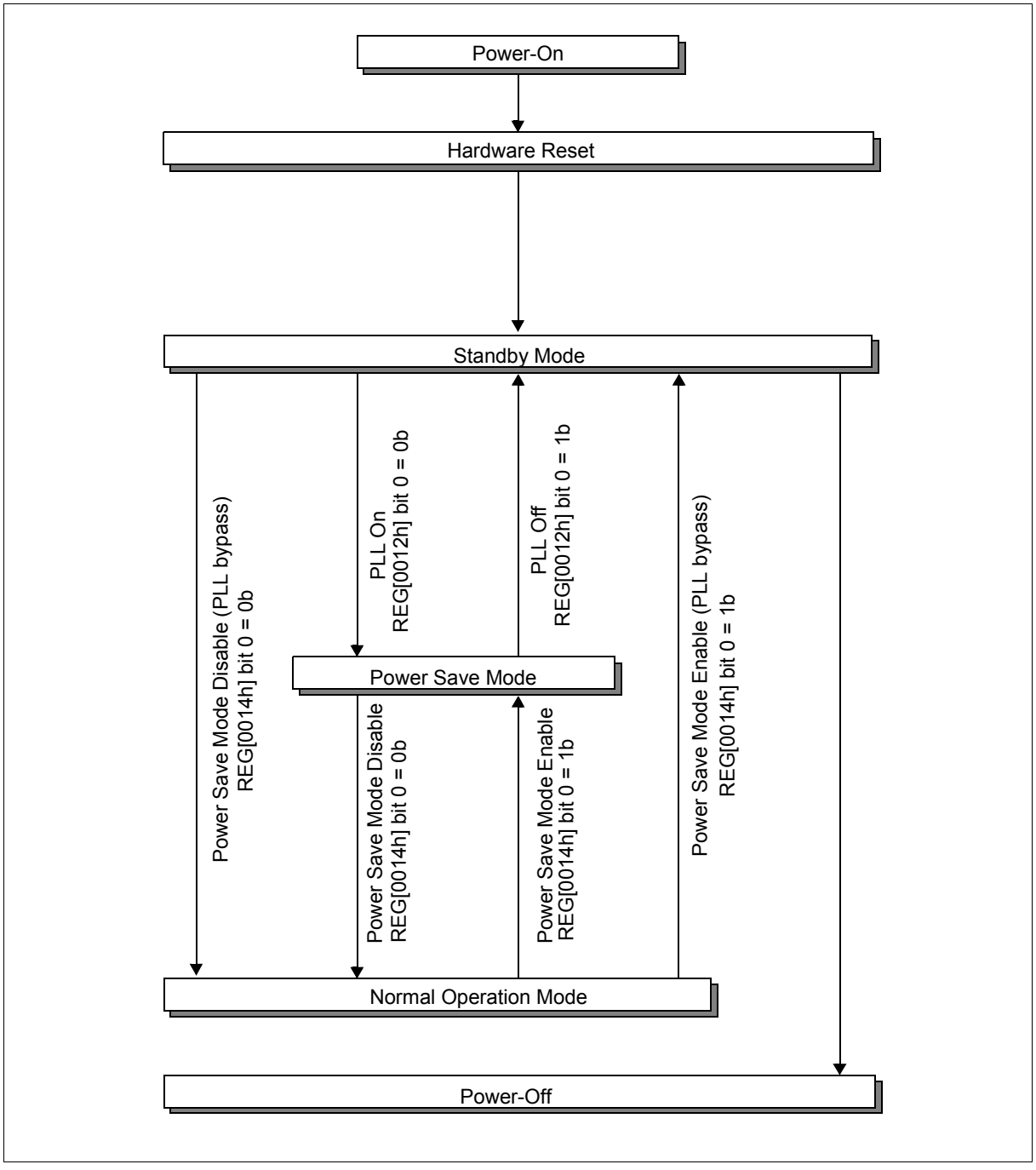


Figure 11-2: Power Modes

11.2.1 Power-On

When powering-on the S1D13L02, the following sequence must be used.

1. COREVDD, PLLVDD On
2. HIOVDD, PIOVDD, GPIOVDD On

11.2.2 Reset

After power-on, an active low hardware reset pulse, which is two external clock cycles (CLKI) in length, must be input to the S1D13L02 RESET# pin. All registers, including the Clock Configuration registers (REG[000Eh] ~ REG[0018h]) are reset by a hardware reset. After releasing the RESET# signal, the Clock Configuration registers are immediately accessible.

A software reset is enabled by writing to REG[0016h]. All registers, except for the asynchronous registers (REG[0004h] ~ REG[0018h], REG[0300h] ~ REG[031Ah]) are reset. After a software reset, the registers cannot be accessed for four external clock cycles (CLKI).

11.2.3 Standby Mode

Standby Mode offers the lowest power consumption because all internal clock supplies are stopped and the PLL is disabled. This mode must be entered before turning off the power supplies or setting the PLL registers.

In standby mode, the asynchronous registers (REG[0004h] ~ REG[0018h], REG[0300h] ~ REG[031Ah]) can be accessed.

11.2.4 Power Save Mode

Power Save Mode stops all internal clock supplies. This mode must be entered before setting the System Clock Setting register (REG[0018h]). Also, there may be up to a 1ms delay before the PLL output becomes stable after it is enabled. The S1D13L02 should be in Power Save Mode during this time.

In power save mode, the asynchronous register (REG[0004h] ~ REG[0018h], REG[0300h] ~ REG[031Ah]) can be accessed.

11.2.5 Normal Mode

All functions are available in Normal Mode. However, clocks to modules that are not in use are dynamically stopped. Before enabling Power Save Mode (REG[0014] bit 0 = 1b) from Normal Mode, confirm that the memory controller is idle (REG[0014h] bit 6 = 1b).

11.2.6 Power-Off

When powering-off the S1D13L02, the following sequence must be used.

1. HIOVDD, PIOVDD, GPIOVDD Off
2. COREVDD, PLLVDD Off

12 Data Formats

12.1 Host Interface Input Formats

The S1D13L02 can receive image data from the Host directly or through the HWC (Host interface Write Controller). The HWC provides configurable functions such as rectangular write, rotational write, mirror write.

When the HWC is enabled (REG[0180h] bit 0 = 1b), data can be sent as RGB 5:6:5. The following sections describe each possible data format.

12.1.1 RGB 5:6:5 format

When the HWC is enabled (REG[0180h] bit 0 = 1b) and RGB 5:6:5 is selected (REG[0180h] bit 7 = 1b), the HWC is configured to receive image data from the Host using the following format.

The following table specifies pixel data in the following manner. For example, $R_{(0,0)}{}^{4}$ defines the most significant bit of R data for the pixel at X,Y position 0,0. All pixel positions correspond to the row and column positions shown below.

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)

Table 12-1: RGB 5:6:5 Data Format

	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	$R_{(0,0)}{}^{4}$	$R_{(0,0)}{}^{3}$	$R_{(0,0)}{}^{2}$	$R_{(0,0)}{}^{1}$	$R_{(0,0)}{}^{0}$	$G_{(0,0)}{}^{5}$	$G_{(0,0)}{}^{4}$	$G_{(0,0)}{}^{3}$	$G_{(0,0)}{}^{2}$	$G_{(0,0)}{}^{1}$	$G_{(0,0)}{}^{0}$	$B_{(0,0)}{}^{4}$	$B_{(0,0)}{}^{3}$	$B_{(0,0)}{}^{2}$	$B_{(0,0)}{}^{1}$	$B_{(0,0)}{}^{0}$
2	$R_{(1,0)}{}^{4}$	$R_{(1,0)}{}^{3}$	$R_{(1,0)}{}^{2}$	$R_{(1,0)}{}^{1}$	$R_{(1,0)}{}^{0}$	$G_{(1,0)}{}^{5}$	$G_{(1,0)}{}^{4}$	$G_{(1,0)}{}^{3}$	$G_{(1,0)}{}^{2}$	$G_{(1,0)}{}^{1}$	$G_{(1,0)}{}^{0}$	$B_{(1,0)}{}^{4}$	$B_{(1,0)}{}^{3}$	$B_{(1,0)}{}^{2}$	$B_{(1,0)}{}^{1}$	$B_{(1,0)}{}^{0}$
3	$R_{(2,0)}{}^{4}$	$R_{(2,0)}{}^{3}$	$R_{(2,0)}{}^{2}$	$R_{(2,0)}{}^{1}$	$R_{(2,0)}{}^{0}$	$G_{(2,0)}{}^{5}$	$G_{(2,0)}{}^{4}$	$G_{(2,0)}{}^{3}$	$G_{(2,0)}{}^{2}$	$G_{(2,0)}{}^{1}$	$G_{(2,0)}{}^{0}$	$B_{(2,0)}{}^{4}$	$B_{(2,0)}{}^{3}$	$B_{(2,0)}{}^{2}$	$B_{(2,0)}{}^{1}$	$B_{(2,0)}{}^{0}$
4	$R_{(3,0)}{}^{4}$	$R_{(3,0)}{}^{3}$	$R_{(3,0)}{}^{2}$	$R_{(3,0)}{}^{1}$	$R_{(3,0)}{}^{0}$	$G_{(3,0)}{}^{5}$	$G_{(3,0)}{}^{4}$	$G_{(3,0)}{}^{3}$	$G_{(3,0)}{}^{2}$	$G_{(3,0)}{}^{1}$	$G_{(3,0)}{}^{0}$	$B_{(3,0)}{}^{4}$	$B_{(3,0)}{}^{3}$	$B_{(3,0)}{}^{2}$	$B_{(3,0)}{}^{1}$	$B_{(3,0)}{}^{0}$
	$R_{(0,1)}{}^{4}$	$R_{(0,1)}{}^{3}$	$R_{(0,1)}{}^{2}$	$R_{(0,1)}{}^{1}$	$R_{(0,1)}{}^{0}$	$G_{(0,1)}{}^{5}$	$G_{(0,1)}{}^{4}$	$G_{(0,1)}{}^{3}$	$G_{(0,1)}{}^{2}$	$G_{(0,1)}{}^{1}$	$G_{(0,1)}{}^{0}$	$B_{(0,1)}{}^{4}$	$B_{(0,1)}{}^{3}$	$B_{(0,1)}{}^{2}$	$B_{(0,1)}{}^{1}$	$B_{(0,1)}{}^{0}$
	$R_{(1,1)}{}^{4}$	$R_{(1,1)}{}^{3}$	$R_{(1,1)}{}^{2}$	$R_{(1,1)}{}^{1}$	$R_{(1,1)}{}^{0}$	$G_{(1,1)}{}^{5}$	$G_{(1,1)}{}^{4}$	$G_{(1,1)}{}^{3}$	$G_{(1,1)}{}^{2}$	$G_{(1,1)}{}^{1}$	$G_{(1,1)}{}^{0}$	$B_{(1,1)}{}^{4}$	$B_{(1,1)}{}^{3}$	$B_{(1,1)}{}^{2}$	$B_{(1,1)}{}^{1}$	$B_{(1,1)}{}^{0}$
	$R_{(2,1)}{}^{4}$	$R_{(2,1)}{}^{3}$	$R_{(2,1)}{}^{2}$	$R_{(2,1)}{}^{1}$	$R_{(2,1)}{}^{0}$	$G_{(2,1)}{}^{5}$	$G_{(2,1)}{}^{4}$	$G_{(2,1)}{}^{3}$	$G_{(2,1)}{}^{2}$	$G_{(2,1)}{}^{1}$	$G_{(2,1)}{}^{0}$	$B_{(2,1)}{}^{4}$	$B_{(2,1)}{}^{3}$	$B_{(2,1)}{}^{2}$	$B_{(2,1)}{}^{1}$	$B_{(2,1)}{}^{0}$
	$R_{(3,1)}{}^{4}$	$R_{(3,1)}{}^{3}$	$R_{(3,1)}{}^{2}$	$R_{(3,1)}{}^{1}$	$R_{(3,1)}{}^{0}$	$G_{(3,1)}{}^{5}$	$G_{(3,1)}{}^{4}$	$G_{(3,1)}{}^{3}$	$G_{(3,1)}{}^{2}$	$G_{(3,1)}{}^{1}$	$G_{(3,1)}{}^{0}$	$B_{(3,1)}{}^{4}$	$B_{(3,1)}{}^{3}$	$B_{(3,1)}{}^{2}$	$B_{(3,1)}{}^{1}$	$B_{(3,1)}{}^{0}$

12.2 Frame Buffer Data Format

Image data is stored in the frame buffer using the following formats according to the selected input format from the Host. The input format is selected using the Host Interface HWC Data Port Active bit, REG[0180h] bit 7. Set the writing starting address so that it is stored as follows when it rotates, the mirror reverses, and input the image from the host interface.

RGB 5:6:5 input data is stored as shown below. For example, R_0^4 defines the most significant bit of R data for pixel 0.

Table 12-2: RGB Format Data Stored in the Frame Buffer

Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000h	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
0002h	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
0004h	R_2^4	R_2^3	R_2^2	R_2^1	R_2^0	G_2^5	G_2^4	G_2^3	G_2^2	G_2^1	G_2^0	B_2^4	B_2^3	B_2^2	B_2^1	B_2^0
0006h	R_3^4	R_3^3	R_3^2	R_3^1	R_3^0	G_3^5	G_3^4	G_3^3	G_3^2	G_3^1	G_3^0	B_3^4	B_3^3	B_3^2	B_3^1	B_3^0

13 Display Functions

The S1D13L02 supports up to three layers which support Transparency and Alpha Blending functions.

- Main Layer
- PIP1 Layer
- PIP2 Layer

The Main Layer can consist of up to two non-overlapping windows. The image data is always stored as RGB 5:6:5 and the output image can be doubled in size using the Pixel Doubling feature.

The PIP1 Layer image data is stored as RGB 5:6:5. It includes a bi-cubic scaler that can resize the image data from 8x ~ 1/8x and an edge enhancement function.

The PIP2 Layer image data is stored as RGB 5:6:5. It also includes a bi-cubic scaler that can resize the image data from 8x ~ 1/8x. In addition, it can perform Panorama scaling (vertical variable rate scaling). The PIP2 includes an edge enhancement function and a LUT which can be used for independent gamma control of the PIP2 window.

Any portion of the display not covered by one of the layers is set to the configurable Background Color (see REG[0206h]).

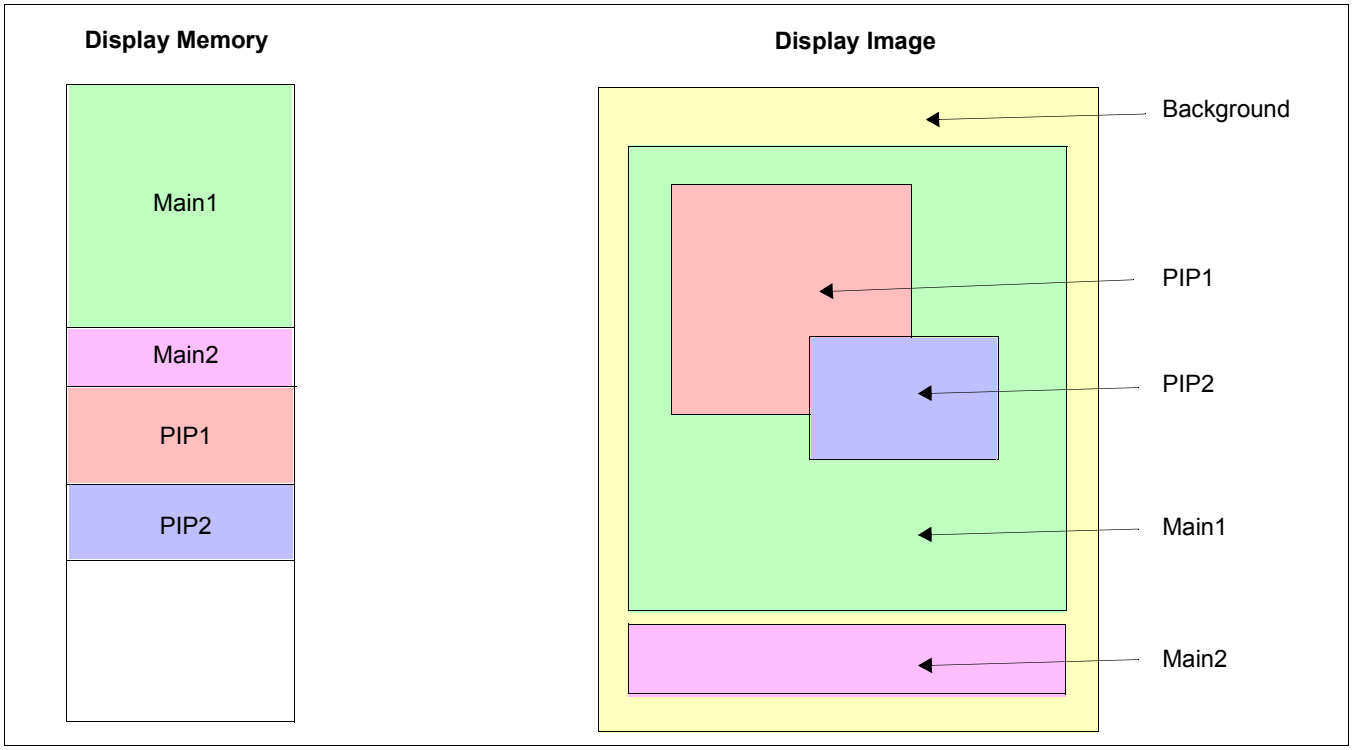


Figure 13-1: Available Display Layers

13.1 Main Layer

The Main Layer can consist of up to 2 windows (Main1 and Main2). The windows cannot overlap and must observe the restrictions shown in Section 13.1.1, “Main Layer Restrictions” on page 141. Each window is independently configured using an x,y coordinate to determine the location of the window relative to the top left corner of the panel (0,0), and height and width registers to specify the size of each window.

The size of the entire display image is determined by the HDP (Horizontal Display Period) and VDP (Vertical Display Period) settings. Any portion of the display not covered is set to the background color.

The main window(s) image data is stored in display memory as RGB 5:6:5 format starting at the specified display start address. The following figure shows the registers used to configure the x,y start positions and sizes of the Main windows.

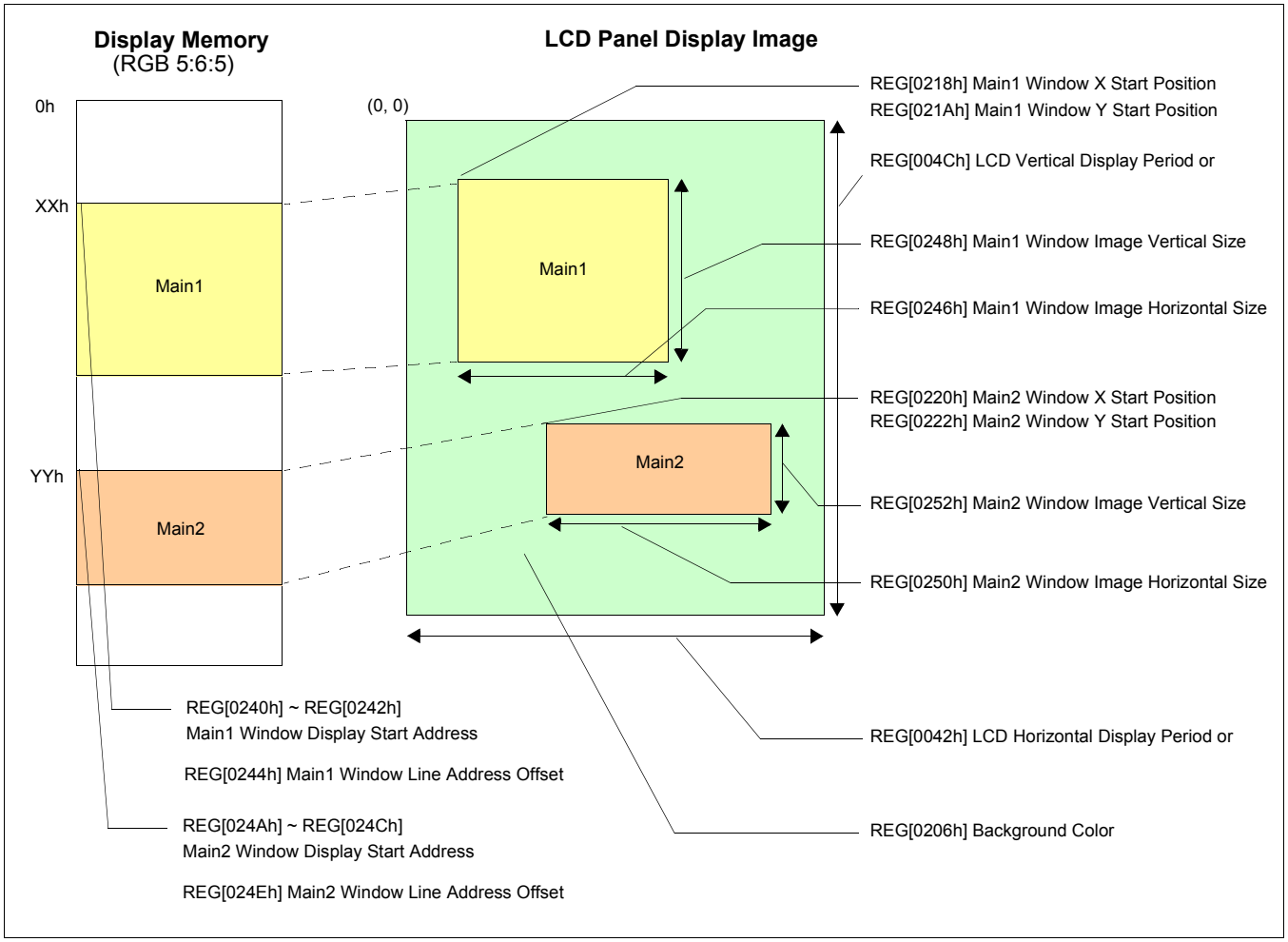


Figure 13-2: Configuring the Main Windows

13.1.1 Main Layer Restrictions

The following restrictions must be considered when configuring the Main Layer windows.

- The right edge of the main window (Main1 or Main2) must not exceed the width of the display panel as defined by HDP, in pixels.
- The bottom edge of the main window (Main1 or Main2) must not exceed the height of the display panel as defined by VDP, in lines.
- The bottom edge of the Main1 window must not exceed the top edge of the Main2 window, in lines.

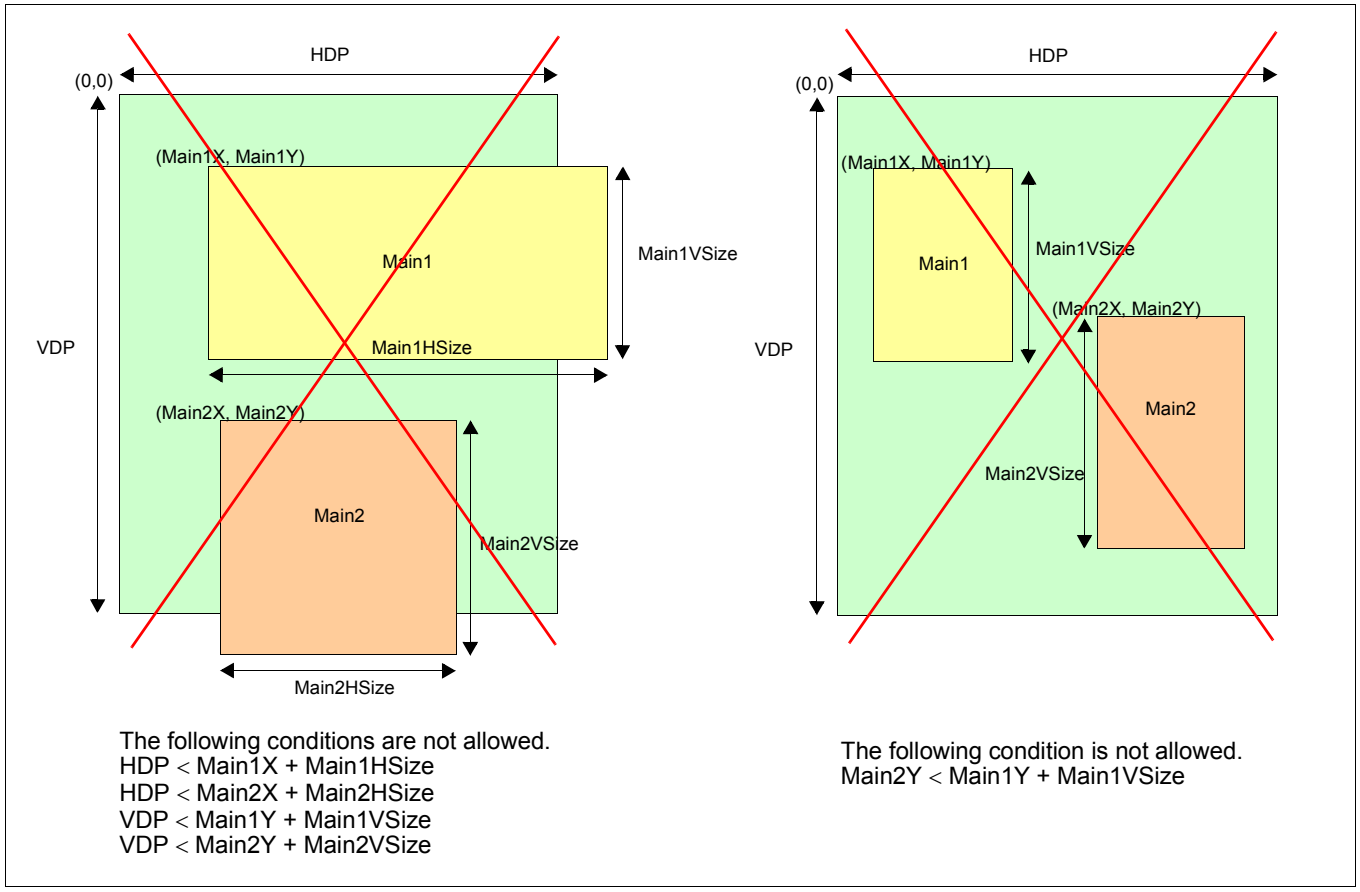


Figure 13-3: Main Layer Restrictions

13.1.2 Main Layer Input Format

The image data must be input to the S1D13L02 as RGB 5:6:5 format. It is stored in this format and converted to RGB 8:8:8 format before being output to the panel in the following manner.

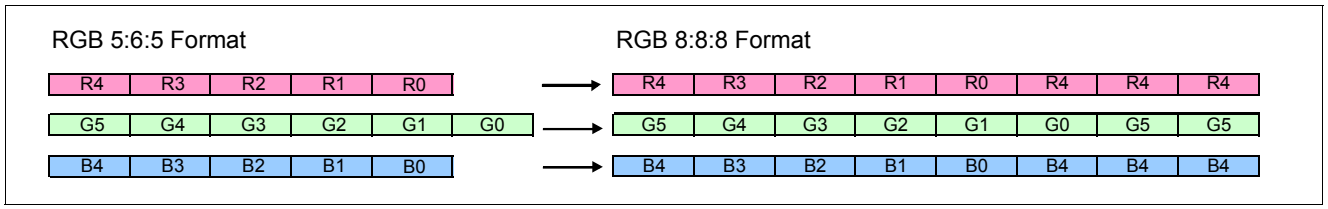


Figure 13-4: RGB 5:6:5 to RGB 8:8:8 Conversion

13.1.3 Main Layer Pixel Doubling

The image data for both main windows can be expanded using Pixel Doubling allowing easy migration to larger panel sizes using existing image data. The following figure shows an example where pixel doubling is enabled for the Main1 Window.

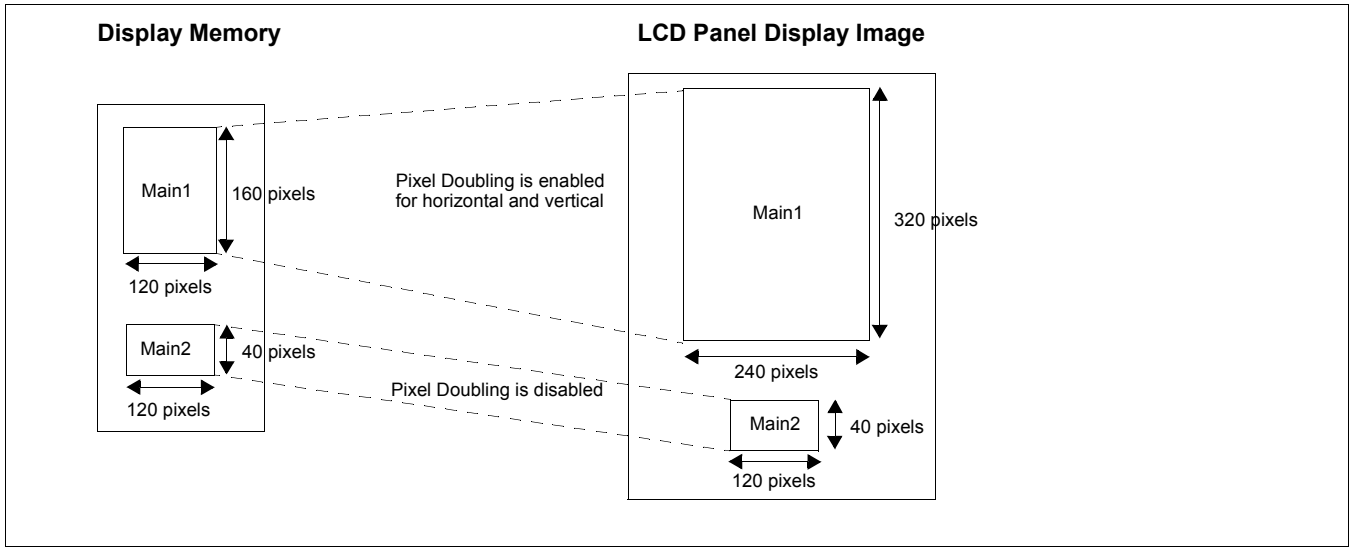


Figure 13-5: Main Layer Pixel Doubling Example

Note

The Main Layer restrictions contained in Section 13.1.1, “Main Layer Restrictions” on page 141 apply to the “Pixel Doubled” dimensions. For example, enabling horizontal pixel doubling cannot cause the right edge of the Main1 window to exceed the HDP.

Pixel Doubling can be independently controlled in both the horizontal and vertical directions for each Main window using the following registers. For further information on each bit, refer to the bit descriptions in Section 10.4.7, “Display Configuration Registers” on page 80

Table 13-1: Main Layer Pixel Doubling Registers

Main Window	Horizontal Enable	Vertical Enable
Main 1	REG[0244h] bit 12	REG[0244h] bit 13
Main 2	REG[024Eh] bit 12	REG[024Eh] bit 13

13.2 PIP Layers

The S1D13L02 supports two PIP Layers (PIP1 and PIP2). Each layer consists of a window which can overlap the other PIP window and the Main windows. The PIP windows must observe the restrictions shown in Section 13.2.1, "PIP Window Restrictions" on page 145. Each PIP window is independently configured by defining the start and end x,y coordinates of the window relative to the top left corner of the panel (0,0).

The size of the entire display image is determined by the HDP (Horizontal Display Period) and VDP (Vertical Display Period) settings. Any portion of the display not covered by a PIP layer or the Main layer (see Section 13.1, "Main Layer" on page 140), is set to the background color.

The image data for the PIP windows is stored in display memory as RGB 5:6:5 format starting at the specified display start address. The following shows the registers used to configure the PIP windows.

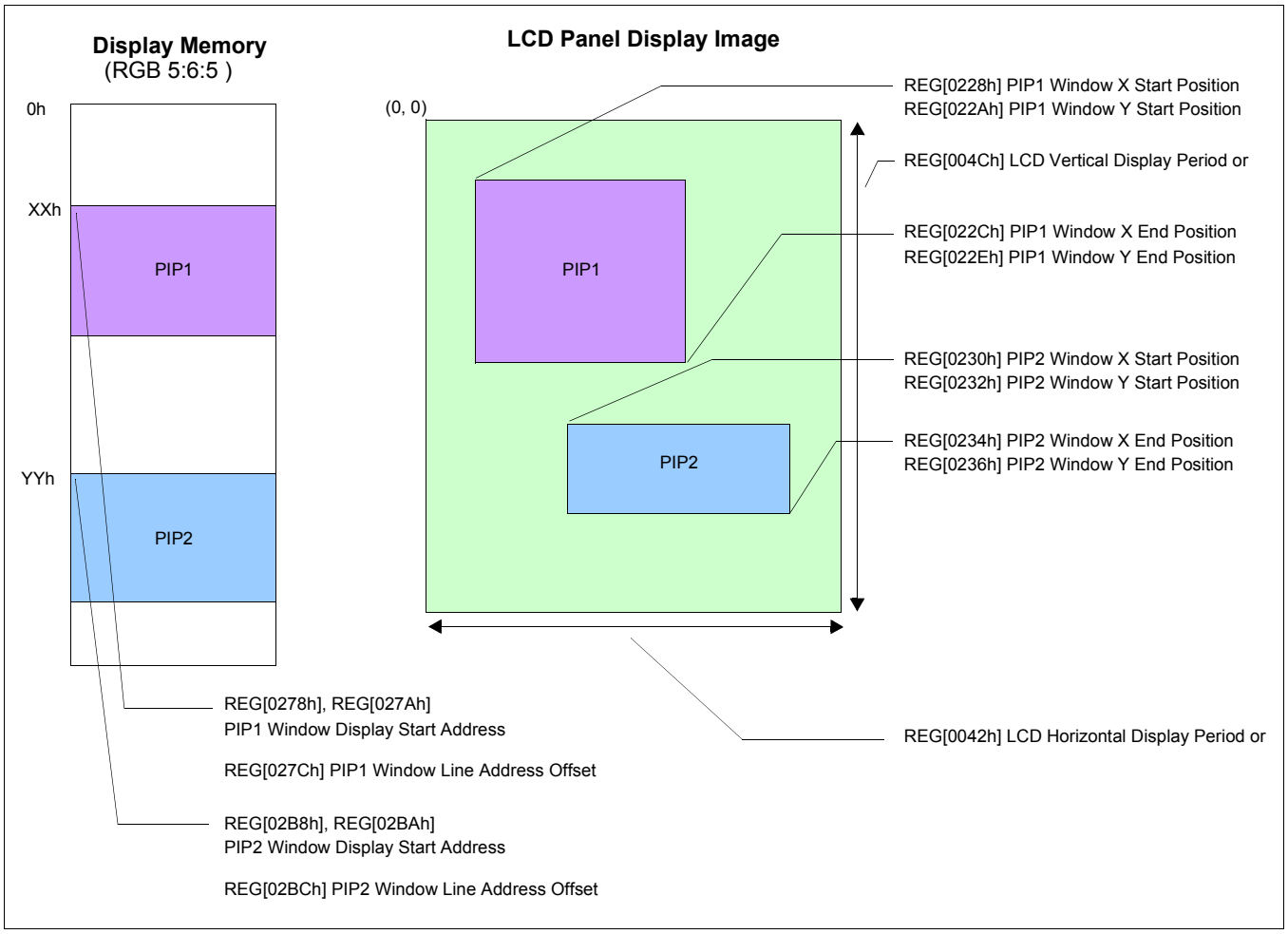


Figure 13-6: PIP Window Setting

13.2.1 PIP Window Restrictions

The following restrictions must be considered when configuring the PIP windows.

- The right edge of the PIP window (PIP1 or PIP2) must not exceed the total width of the display panel as defined by HDP, in pixels.
- The bottom edge of the PIP window (PIP1 or PIP2) must not exceed the total height of the display panel as defined by VDP, in lines.

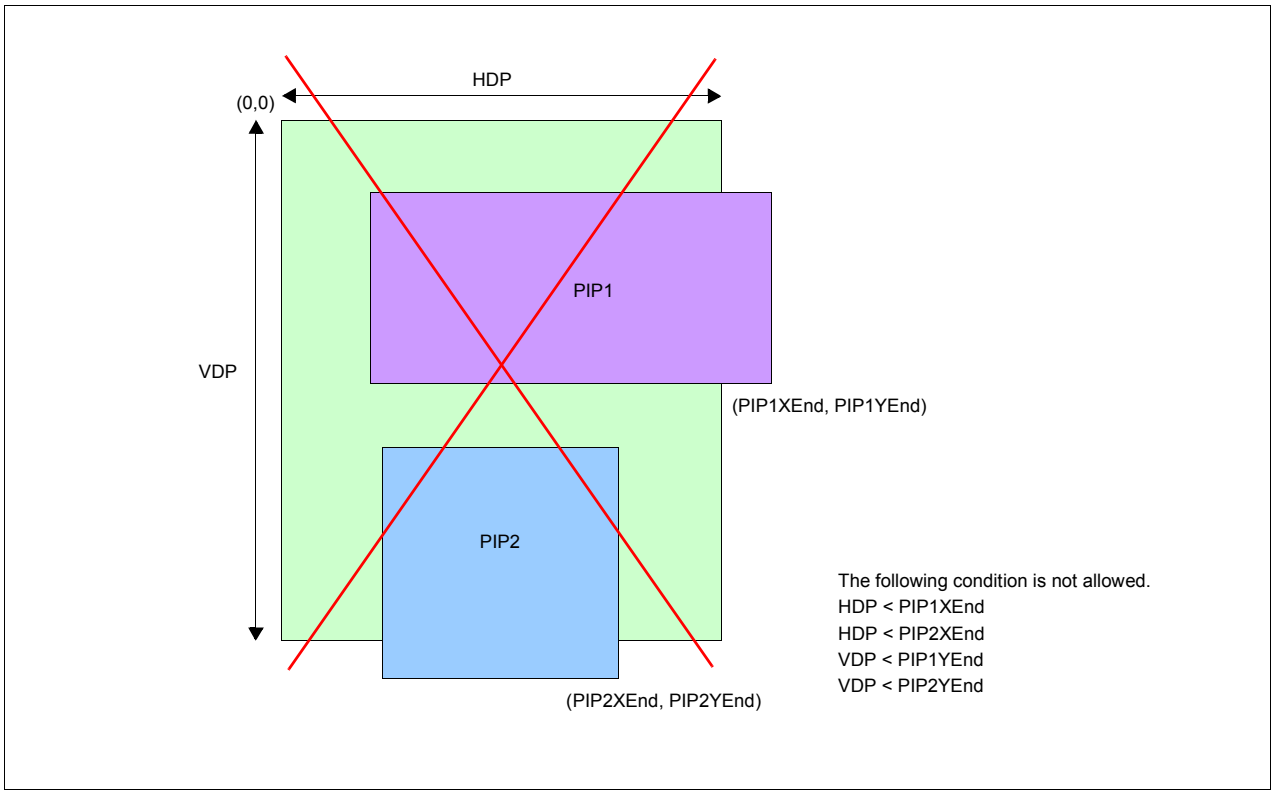


Figure 13-7: PIP Window Restrictions

13.2.2 Using The Scalers

Both PIP Layers include a bi-cubic scaler which can be used to expand the PIP window source image data up to 8x or reduce it down to 1/8x. Both scalers include configurable horizontal and vertical filters which reduce artifacting caused by large scaling (see REG[0260h] and REG[0268h] for PIP1, REG[02A0h] and REG[02A8h] for PIP2). The following restrictions must be observed when configuring the both the PIP1 and PIP2 Scalers.

- The minimum source image size is 4x4 pixels.
- The maximum source image size is 510x1022 pixels.
- The maximum scale-down rate is 1/8 (for details on this restriction refer to REG[0262h] ~ REG[0264h] and REG[02A2h] ~ REG[02A4h] in Section 10.4, "Register Descriptions" on page 56).

When using the scaler, three sizes are important: the Source Image size, the Resulting Image size, and the PIP window size. The horizontal and vertical scaling is applied to the source image to produce the resulting image which is displayed in the PIP window. Depending on the relationship between the resulting size and the PIP window size, there are three possible cases.

- Case 1 - The resulting image is smaller than the defined PIP window in either the horizontal or vertical direction. In this case, the PIP image is positioned at coordinate 0,0 of the PIP window and the area of the PIP window not filled with image data remains black. This case takes place when either of the following formulas are true.

  PIP Image Horizontal Size < (PIP Window X End Position - PIP Window X Start Position)
  PIP Image Vertical Size < (PIP Window Y End Position - PIP Window Y Start Position)

- Case 2 - The resulting image is the same size as the defined PIP window. In this case, the PIP image is positioned at coordinate 0,0 of the PIP window and fills the entire area of the PIP window. This case takes place when both of the following formulas are true.

  PIP Image Horizontal Size = (PIP Window X End Position - PIP Window X Start Position)
  PIP Image Vertical Size = (PIP Window Y End Position - PIP Window Y Start Position)

- Case 3 - The resulting image is larger than the defined PIP window. In this case, the PIP image is positioned at coordinate 0,0 of the PIP window, but it is trimmed to the size of the PIP window. Any image data outside of the PIP window is not displayed. This case takes place when either of the following formulas are true.

  PIP Image Horizontal Size > (PIP Window X End Position - PIP Window X Start Position)
  PIP Image Vertical Size > (PIP Window Y End Position - PIP Window Y Start Position)

The following figure shows examples for each case.

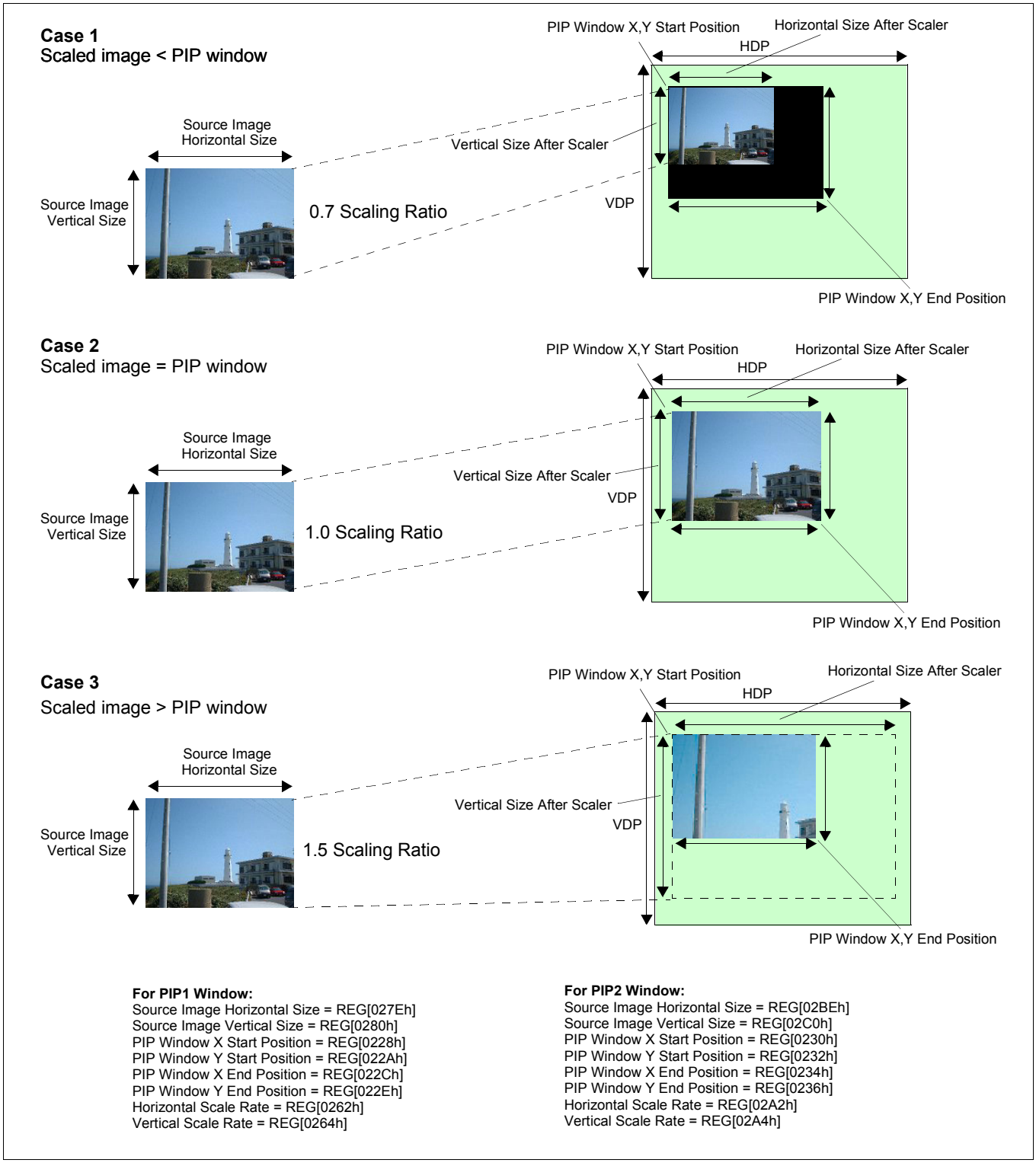


Figure 13-8: Displaying Scaled Images in a PIP Window

To scale the source image display in the PIP window use the following procedure.

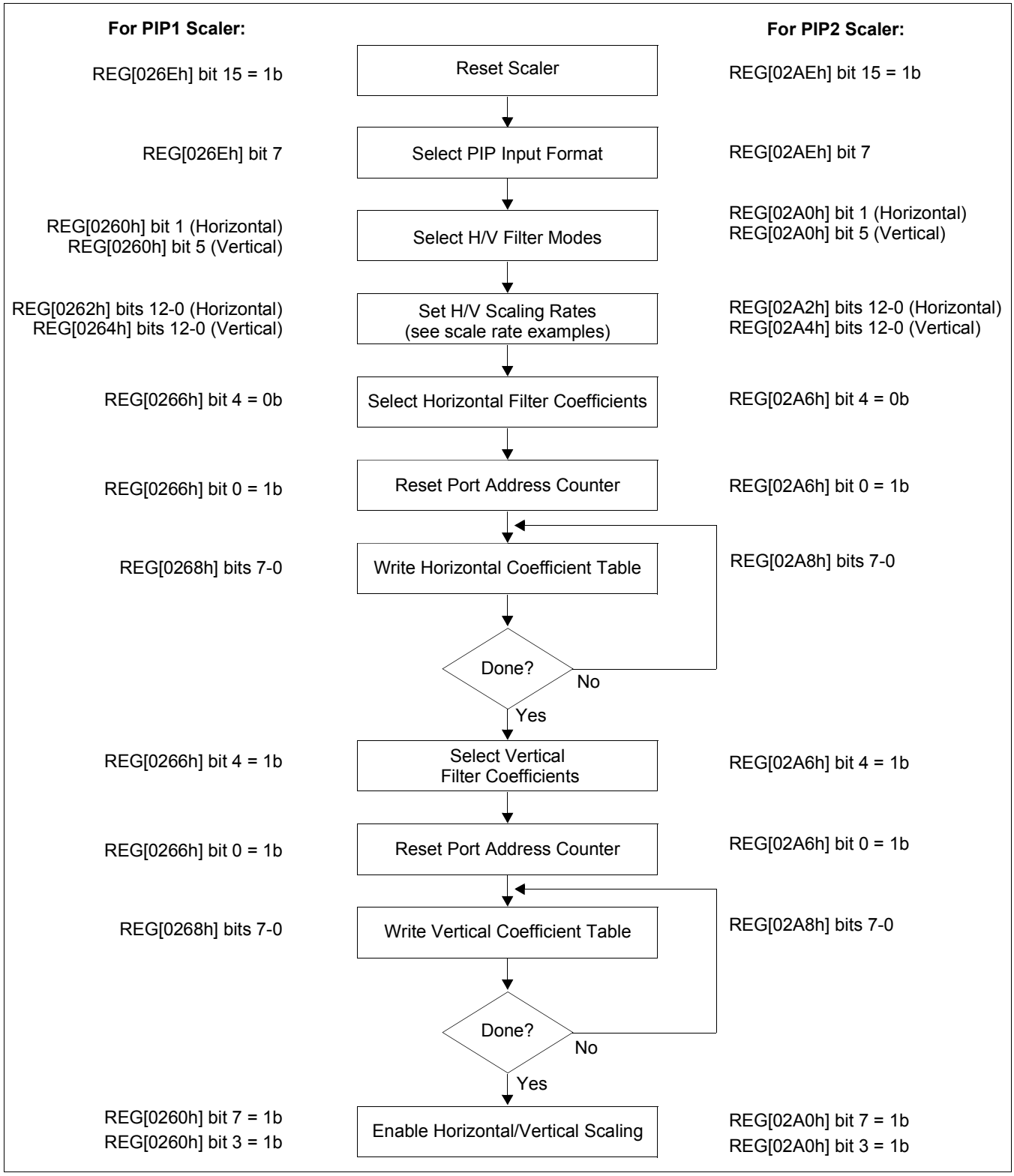


Figure 13-9: Scaler Programming Procedure

The PIP1 and PIP2 scalers support independent scaling rates for both the horizontal and vertical directions. The following calculations provides examples for scale-down and scale-up operations.

Horizontal Scale Rate

To scale-down the source image using a scaling ratio of 0.7, program the Horizontal Scale Rate register (REG[0262h] for PIP1, REG[02A2h] for PIP2) as follows.

Horizontal Scale Rate = 1024 x (1 ÷ 0.7)
= 1462
= 5B6h

To scale-up the source image using a scaling ratio of 1.5, program the Horizontal Scale Rate register (REG[0262h] for PIP1, REG[02A2h] for PIP2) as follows.

Horizontal Scale Rate = 1024 x (1 ÷ 1.5)
= 682
= 2AAh

Vertical Scale Rate

To scale-down the source image using a scaling ratio of 0.7, program the Vertical Scale Rate register (REG[0264h] for PIP1, REG[02A4h] for PIP2) as follows.

Vertical Scale Rate = 1024 x (1 ÷ 0.7)
= 1462
= 5B6h

To scale-up the source image using a scaling ratio of 1.5, program the Horizontal Scale Rate register (REG[0264h] for PIP1, REG[02A4h] for PIP2) as follows.

Vertical Scale Rate = 1024 x (1 ÷ 1.5)
= 682
= 2AAh

13.2.3 Data Conversion to RGB

After scaling takes place, all PIP window image data is converted to RGB 8:8:8.

If the input format is RGB 5:6:5, it is converted using the following method.

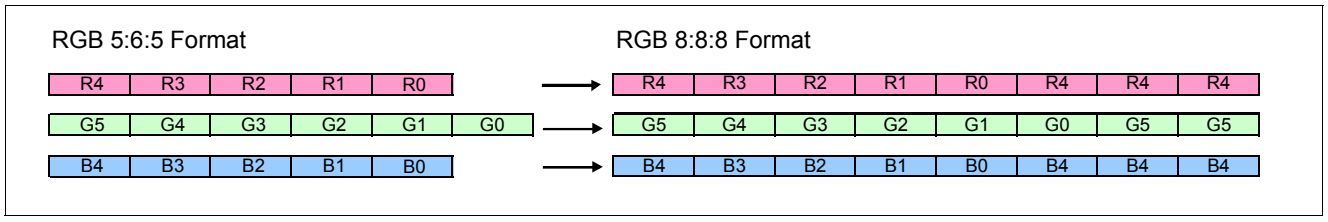


Figure 13-10: RGB 5:6:5 to RGB 8:8:8 Conversion

13.3 Alpha Blending

When the Main layer is on top of the PIP layers (REG[0202h] bits 6-5 = 00b or 10b), the S1D13L02 can perform Alpha Blending on the pixel data of the selected windows. Four independently enabled key colors are available, each supporting a blend ratio from 0% to 100% in increments of 12.5%.

The Alpha Blend Mode Select bit (REG[0204h] bit 7) determines which windows are alpha blended. When alpha blending between the Main window and the PIP windows is selected (REG[0204h] bit 7 = 0b), the pixel data from the PIP window that is overlapped by the Main window key color is alpha blended with the pixel data from the main window at the selected alpha blend ratio. If the PIP Transparency for the "top" PIP window is enabled and the key color is matched, the main window pixel data is alpha blended with the "bottom" PIP window instead of the top PIP window. For further information on PIP Transparency, see Section 13.3.2, "PIP Transparency" on page 152.

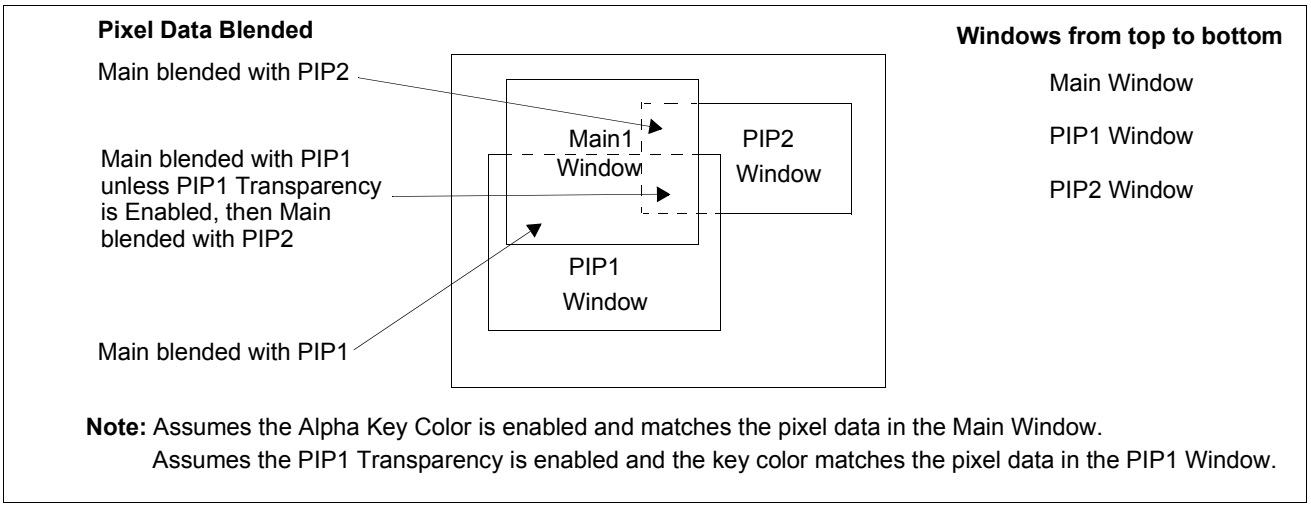


Figure 13-11: Main Window and PIP Windows Alpha Blending Example

When alpha blending between the PIP windows is selected (REG[0204h] bit 7 = 1b), the pixel data from the PIP windows that are overlapped by the Main window key color are alpha blended at the selected alpha blend ratio. If the PIP windows do not overlap, the PIP1 or PIP2 pixel data will "show through" the Main window key color similar to a transparency effect.

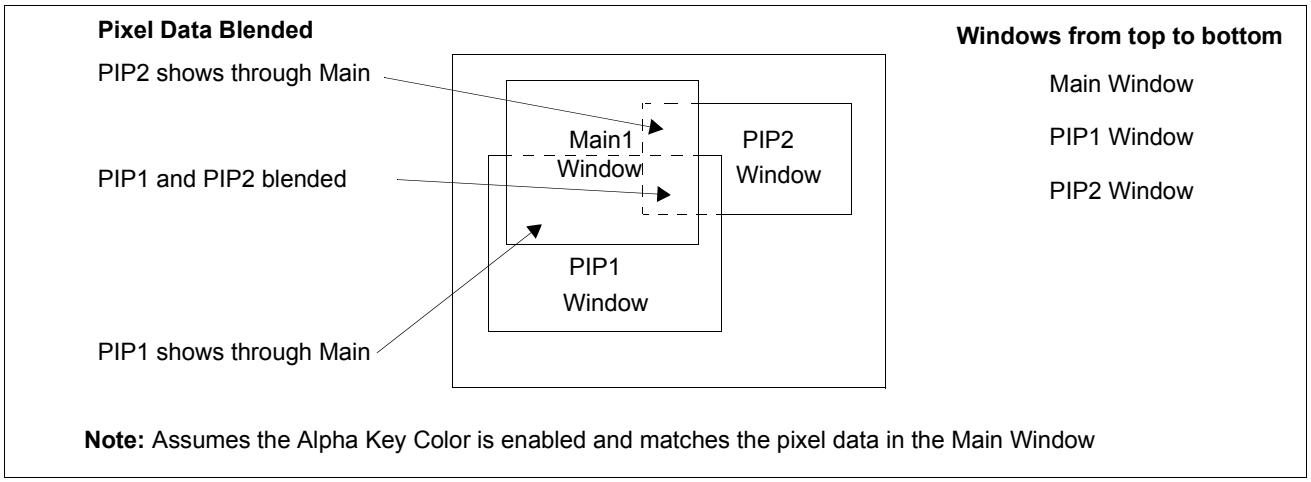


Figure 13-12: Main Window and PIP Windows Alpha Blending Example

For alpha blending and transparency examples for the Main, PIP1, and PIP2 windows, refer to Section 16, "Use Cases" on page 176.

13.3.1 Registers

The following registers are used to control and configure each Alpha Blend Key Color.

Table 13-2: Alpha Blend Register Summary

Alpha Blend	Enable	Blend Ratio	Key Color
1	REG[0204h] bit 8	REG[0208h] bits 3-0	REG[0210h] bits 15-0
2	REG[0204h] bit 9	REG[0208h] bits 7-4	REG[0212h] bits 15-0
3	REG[0204h] bit 10	REG[0208h] bits 11-8	REG[0214h] bits 15-0
4	REG[0204h] bit 11	REG[0208h] bits 15-12	REG[0216h] bits 15-0

13.3.2 PIP Transparency

Both PIP windows have a transparency function. When the PIP window transparency is enabled, the PIP window becomes transparent where the pixel data matches the key color. This feature can be used to allow pixel data to "show through" an overlapping PIP window, or allow Main window pixel data to "show through" when the PIP windows are on top of the Main window.

The following registers are used to control and configure PIP Window Transparency.

Table 13-3: PIP Window Transparency Register Summary

PIP Window	Enable	Key Color
PIP1 Window	REG[0204h] bit 1	REG[020Ch] bits 15-0
PIP2 Window	REG[0204h] bit 2	REG[020Eh] bits 15-0

When alpha blending is enabled, the PIP transparency may be used to allow pixel data to be blended with a PIP window that is on the "bottom".

For alpha blending and transparency examples for the Main, PIP1, and PIP2 windows, refer to Section 16, "Use Cases" on page 176.

13.4 Scroll Buffer

The S1D13L02 supports a scroll buffer function for the Main1 window, PIP1 window, and PIP2 window. The Main2 window does not support the scroll buffer function.

The scroll buffer function allows image data to be stored non-contiguously. When the scroll buffer is used, image data for the display is read starting from the Display Start Address. When the Scroll End Address is reached, data continues to be read from the Scroll Start Address as shown in the following diagram.

Note
The scroll buffer function cannot be used to write image data from the Host to memory.

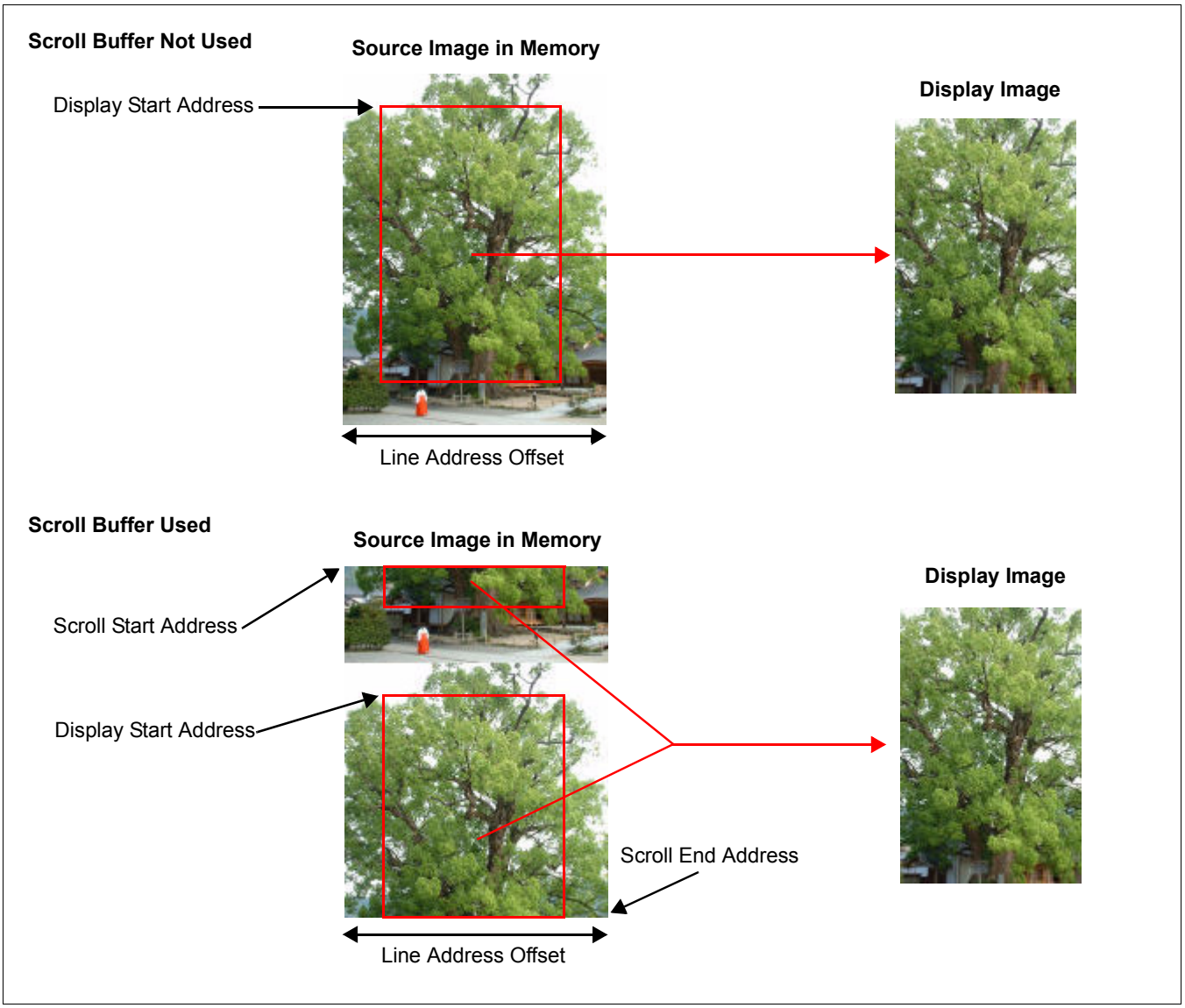


Figure 13-13: Scroll Buffer Examples

13.4.1 Registers

The scroll buffer function uses the following registers to define the Display Start Address, Scroll Start Address, and Scroll End Address for each window.

Table 13-4: Scroll Buffer Registers

Window	Scroll Start Address	Scroll End Address	Display Start Address
Main1 Window	REG[0238h] ~ REG[023Ah]	REG[023Ch] ~ REG[023Eh]	REG[0240h] ~ REG[0242h]
PIP1 Window	REG[0270h] ~ REG[0272h]	REG[0274h] ~ REG[0276h]	REG[0278h] ~ REG[027Ah]
PIP2 Window	REG[02B0h] ~ REG[02B2h]	REG[02B4h] ~ REG[02B6h]	REG[02B8h] ~ REG[02BAh]

Note
To disable scrolling for the selected window, set the Scroll Start Address to 0h and the Scroll End Address to the maximum value.

13.4.2 Restrictions

When configuring the scroll buffer for each window, the following restrictions must be observed.

- The Scroll Start Address must specify the address of the first line of an image in the display memory.
- The Scroll End Address must specify the address of the last line of an image in the display memory.
- The Scroll Start Address for each window must be less than the Scroll End Address.
  Main1 Window: REG[0238h] ~ REG[023Ah] < REG[023Ch] ~ REG[023Eh]
  PIP1 Window: REG[0270h] ~ REG[0272h] < REG[0274h] ~ REG[0276h]
  PIP2 Window: REG[02B0h] ~ REG[02B2h] < REG[02B4h] ~ REG[02B6h]

14 Host Interface

The S1D13L02 has a 16-bit indirect Host interface which allows high speed register writes (1 write cycle = 3 internal system clocks). It also includes a Host interface Write Controller (HWC) which supports clockwise rotation and mirror functions while writing to a rectangular area of the frame buffer. Alternately, image data can be written to the frame buffer without using the HWC, if rotation and mirroring are not required.

14.1 Indirect Interface Overview

The Host controls the S1D13L02 through the indirect interface which provides access to the S1D13L02 internal register set using the Index and Data register ports. The Status register port provides the status of the HWC (Host interface Write Controller) and the memory controller. All internal register ports are accessed using address lines AB[3:1] as shown in Figure 14-1: Indirect Interface Overview. For a detailed description of the register ports, see Section 14.1.1, “Indirect Addressing Register Ports” on page 156).

AB[3:1] also provide optional access to selected GPIO registers. Note that although the S1D13L02 includes GPIO[23:0], only GPIO[15:0] are controllable/readable using this method. The complete GPIO registers (REG[0300h] ~ REG[031Ah]) are accessible by accessing the internal register set through the Index and Data register ports. For a detailed description of the GPIO registers, see Section 10.4.10, “GPIO Registers” on page 124.

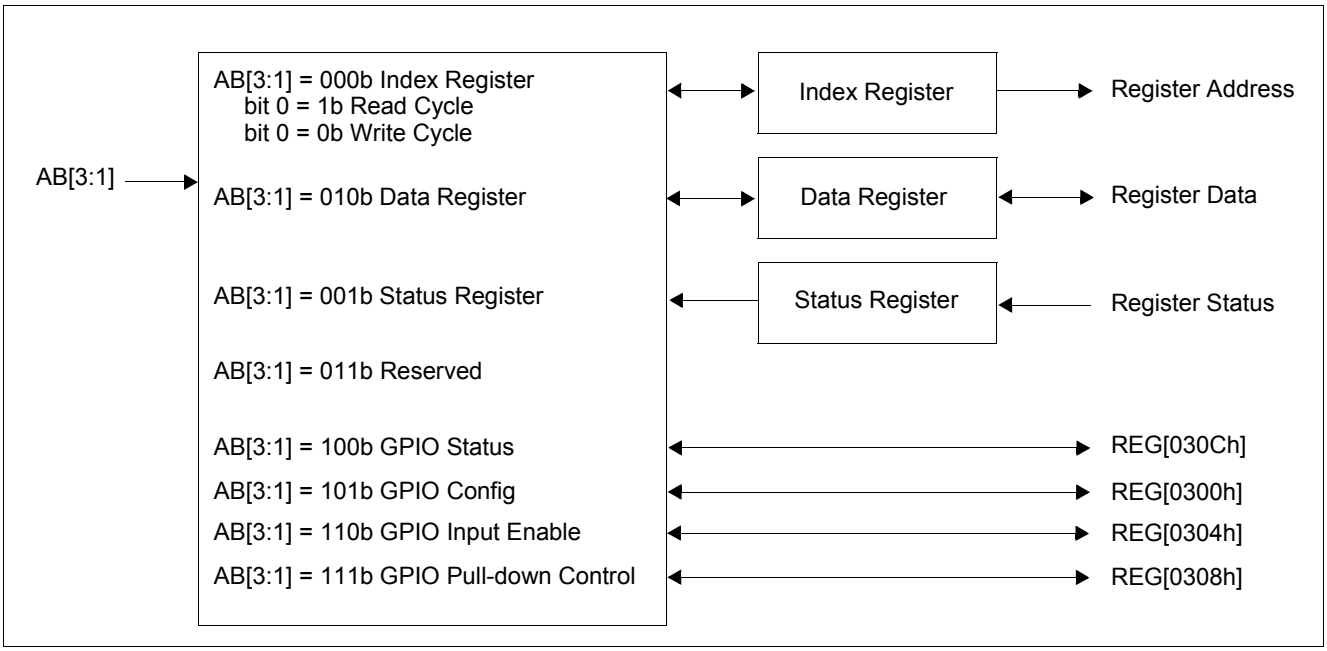


Figure 14-1: Indirect Interface Overview

14.1.1 Indirect Addressing Register Ports

AB[3:1] = 000b Indirect Interface Index Register
Default = 0000h — Read/Write

Register Address bits 15-1															R/W Select
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 15-1 Register Address bits [15:1]
These bits set the register address for the indirect interface.

bit 0 R/W Select
This bit selects whether a read or a write is performed.
When this bit = 0b, a write is performed.
When this bit = 1b, a read is performed.

AB[3:1] = 010b Indirect Interface Data Register
Default = 0000h — Read/Write

Register Data bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 15-0 Register Data bits [15:0]
These bits are the data port for the indirect interface.

AB[3:1] = 001b Indirect Interface Status Register
Default = 0000h — Read Only

n/a							HWC Status (RO)	n/a							Memory Status (RO)
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bit 8 HWC Status (Read Only)
This bit indicates the status of the Host interface Write Controller (HWC) block.
When this bit = 0b, the HWC is ready (not busy).
When this bit = 1b, the HWC is busy.

bit 0 Memory Status (Read Only)
This bit indicates the status of the Memory Controller. The status of this bit must be checked before accessing the memory, however confirmation for continuous memory accesses is not necessary.
When this bit = 0b, the memory controller is ready (not busy).
When this bit = 1b, the memory controller is busy.

14.2 Register Access

The indirect addressing register ports (see Section 14.1.1, “Indirect Addressing Register Ports” on page 156) are used to access the S1D13L02 internal register set as shown in the following procedures. For a list of the internal register set, see Section 10.2, “Register Set” on page 53.

When the Host interface access cycle is greater than or equal to 6 internal system clocks (SYSCLK), the following procedure should be used to access the internal registers.

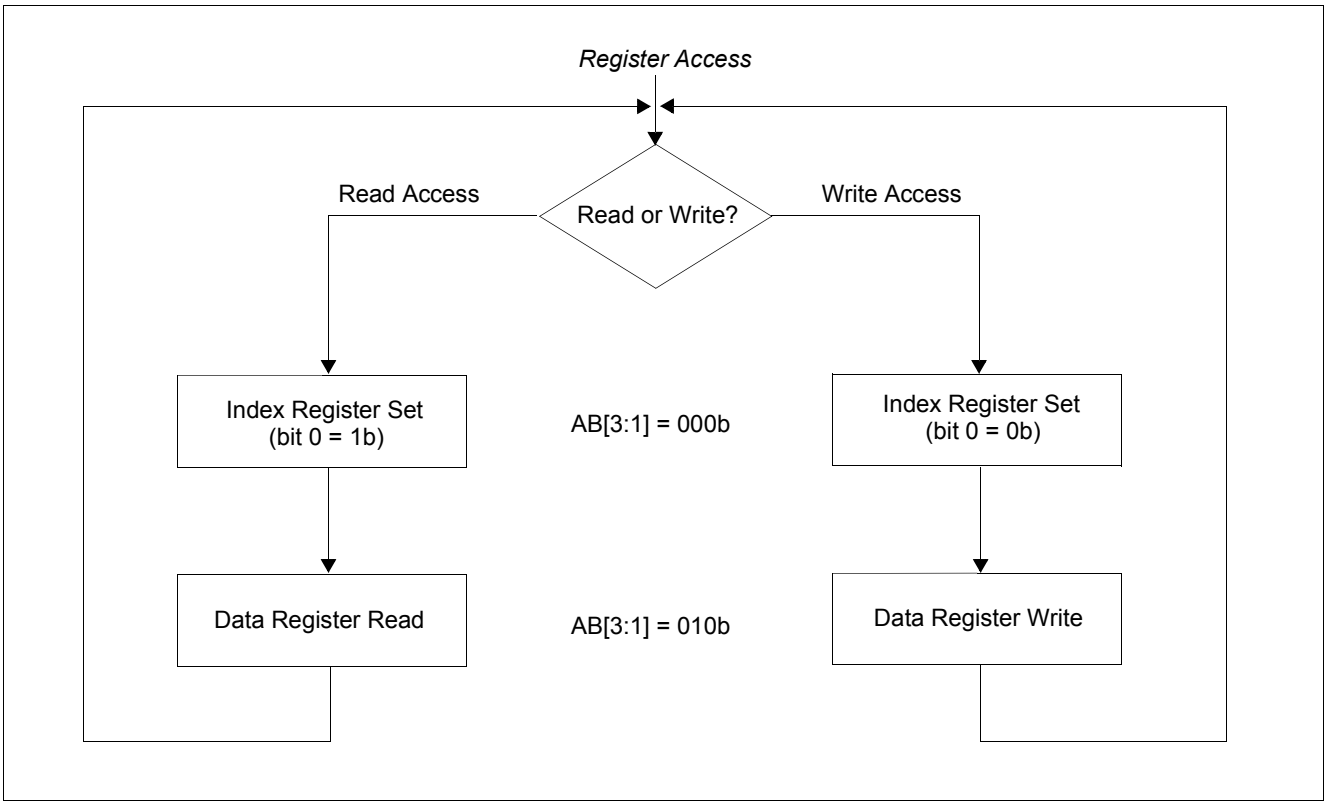


Figure 14-2: Register Access Procedure for Access Cycles ≥ 6 SYSCLK

Note
The register index must be set for each read cycle.

When the Host interface access cycle is from 3 to 5 internal system clocks (SYSCLK), the following procedure should be used to access the internal registers.

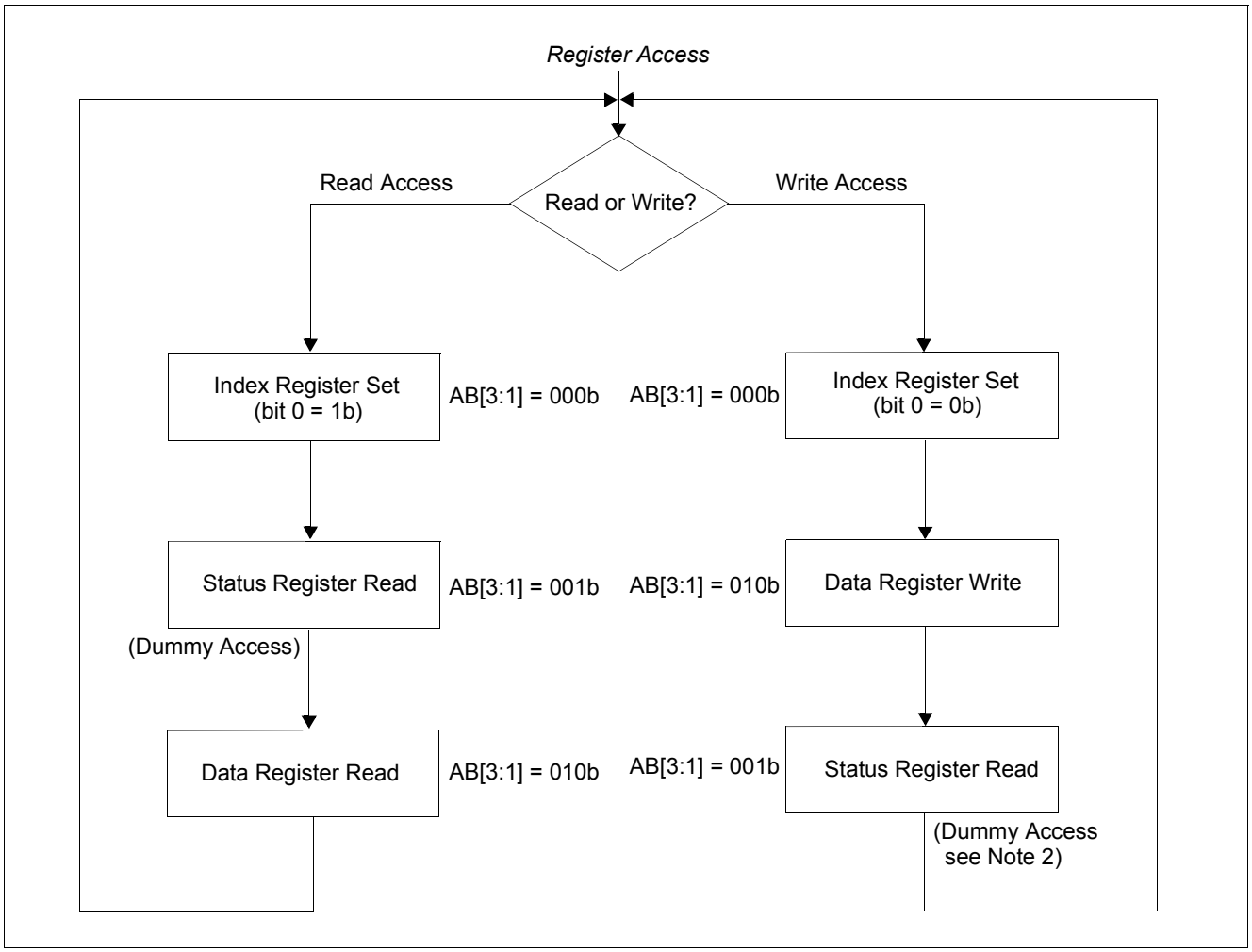


Figure 14-3: Register Access Procedure for Host Access Cycles from 3-5 SYSCLK

Note

1. The register index must be set for each read cycle.
2. The status read on the Write Access path is a dummy access and is not required if the next "Index Register Set" takes place 3 or more SYSCLKs after the previous "Data Register Write".

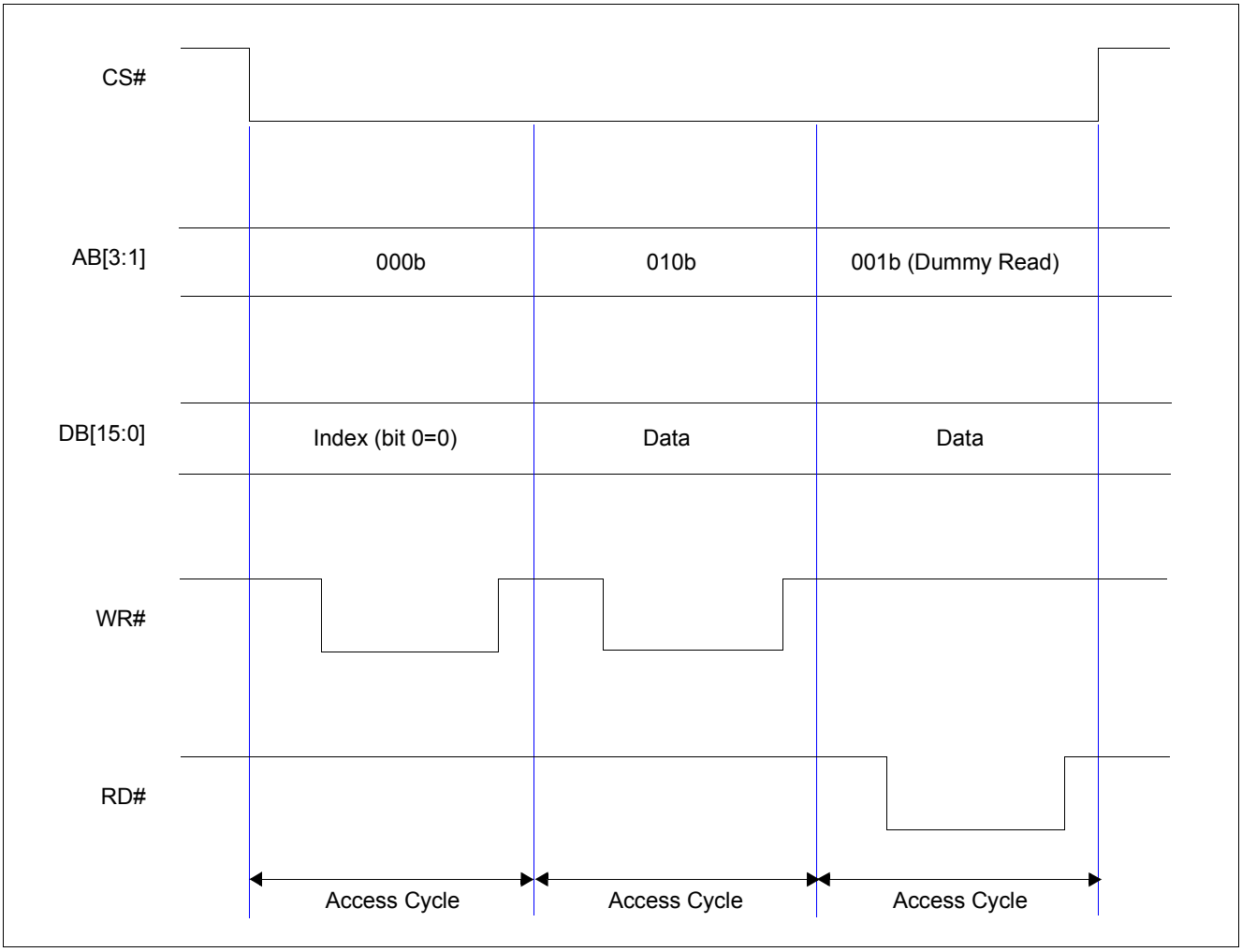


Figure 14-4: Register Write Access Timing (Access Cycle = 3~5 Internal System Clocks)

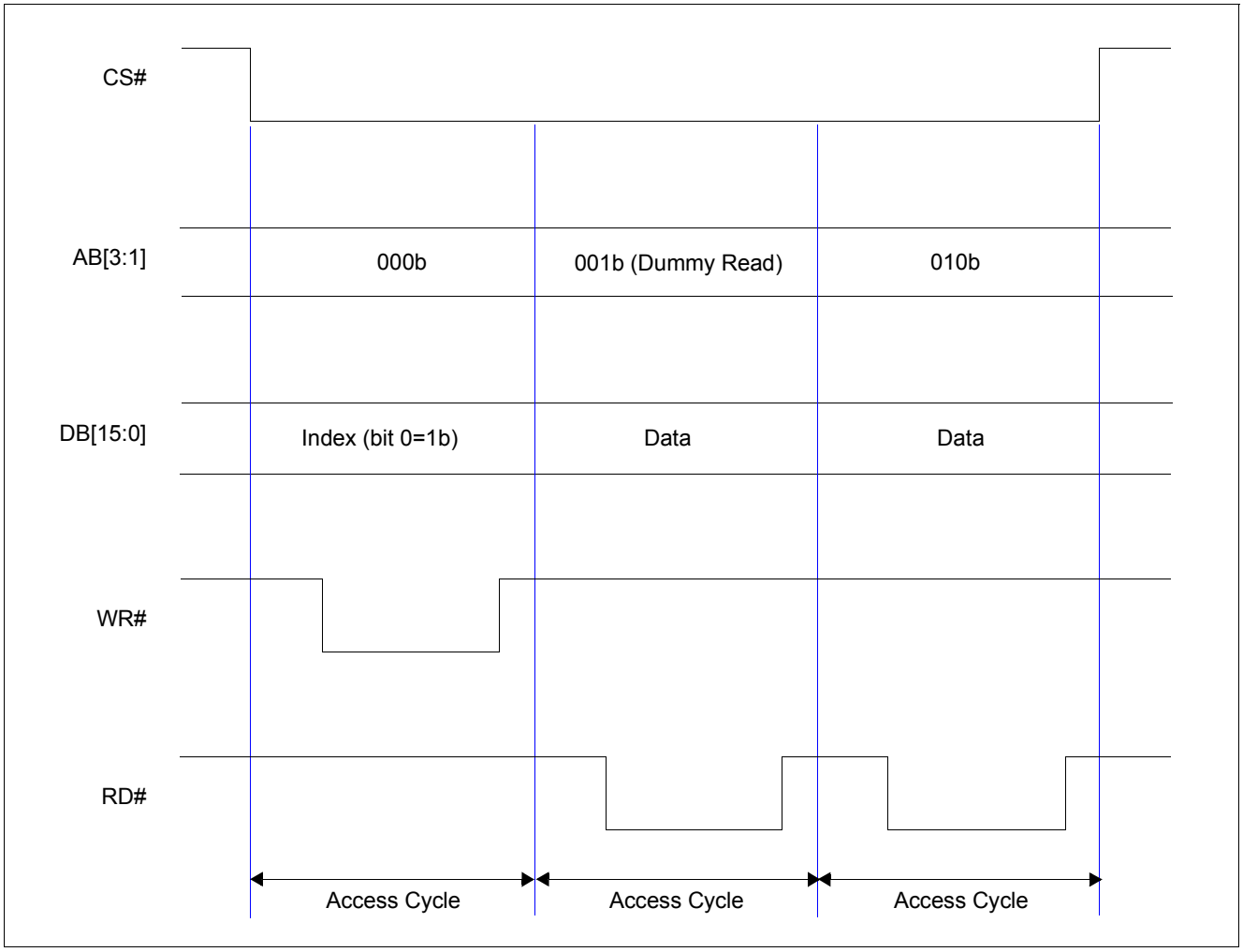


Figure 14-5: Register Read Access Timing (Access Cycle = 3~5 Internal System Clocks)

14.3 Memory Access Using the HWC

The HWC (Host interface Write Controller) can be used to write image data from the Host to a rectangular area of the frame buffer (REG[0180h] bit 0 = 1b). The HWC can be independently configured for the following write modes.

- Rotation: 0°, 90°, 180°, or 270° clockwise rotation of the image data
- Mirror: horizontal mirror effect

When using the HWC, the following bit fields must be configured before writing to the frame buffer using the Memory Access Port, REG[018Ch].

REG[0180h] bit 7	Host Interface HWC Data Port Activet
REG[0180h] bit 3	HWC Mirror Enable
REG[0180h] bits 2-1	HWC Rotation Mode Select
REG[0180h] bit 0	HWC Module Enable
REG[0184h] bits 3-0	Memory Start Address 1
REG[0182h] bits 15-1	Memory Start Address 0
REG[0186h] bits 11-1	HWC Memory Rectangular Write Address Offset
REG[0188h] bits 9-1	HWC Memory Rectangular Write Horizontal Size
REG[018Ah] bits 9-0	HWC Memory Rectangular Write Vertical Size

The input image data is written to the frame buffer according to the setting of the HWC Mirror Enable bit (REG[0180h] bit 3) and the HWC Rotation Mode Select bits (REG[0180h] bits 2-1). For each combination of rotation and mirror, the write direction of the input data changes and the start address must be re-programmed. The vertical size and horizontal size remain the same for all combinations.

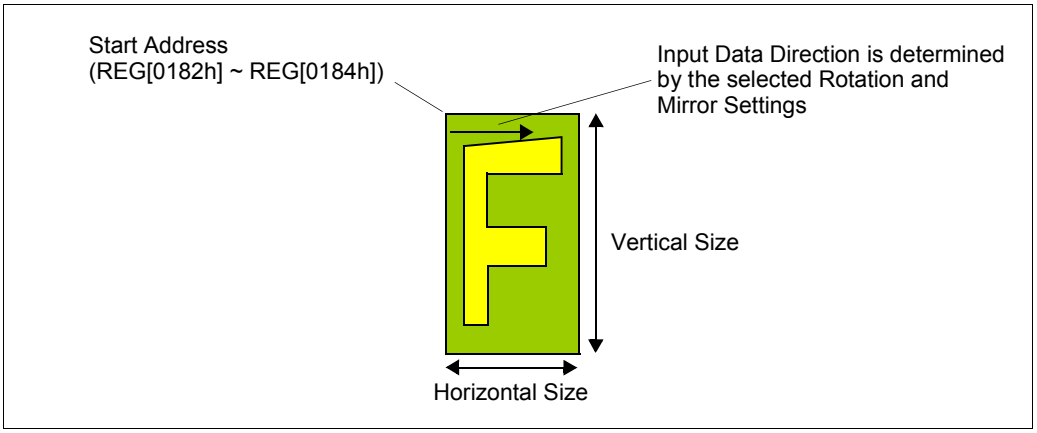


Figure 14-6: Input Image Example

The following sections provide examples for each combination of Rotation and Mirror settings.

14.3.1 Writing for Rotation=0° and Mirror Disabled

When REG[0180h] bits 2-1 = 00b and REG[0180h] bit 3 = 0b, bit 1 of the Memory Start Address must be set to 0b (REG[0182h] bit 1 = 0b).

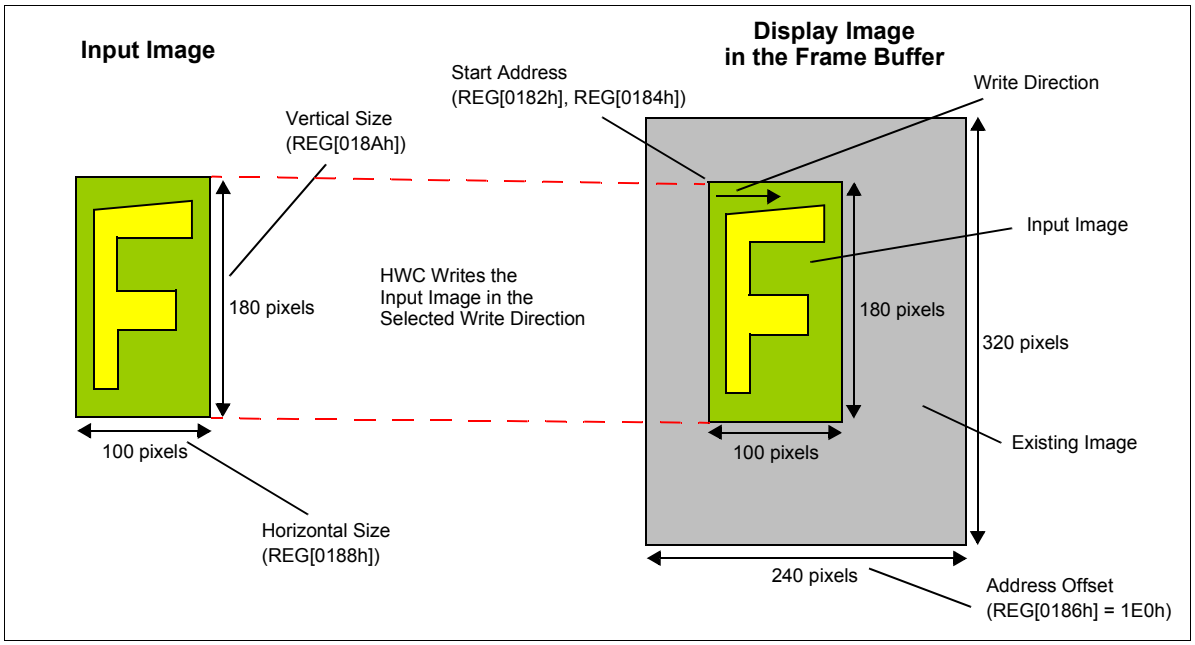


Figure 14-7: Writing for Rotation=0° and Mirror Disabled Example

For the above example, the Start Address is calculated using the following formula.

REG[0182h] ~ REG[0184h]
= memory start address
= 1000h

14.3.2 Writing for Rotation=90° and Mirror Disabled

When REG[0180h] bits 2-1 = 01b and REG[0180h] bit 3 = 0b, bit 1 of the Memory Start Address must be set to 1b (REG[0182h] bit 1 = 1b).

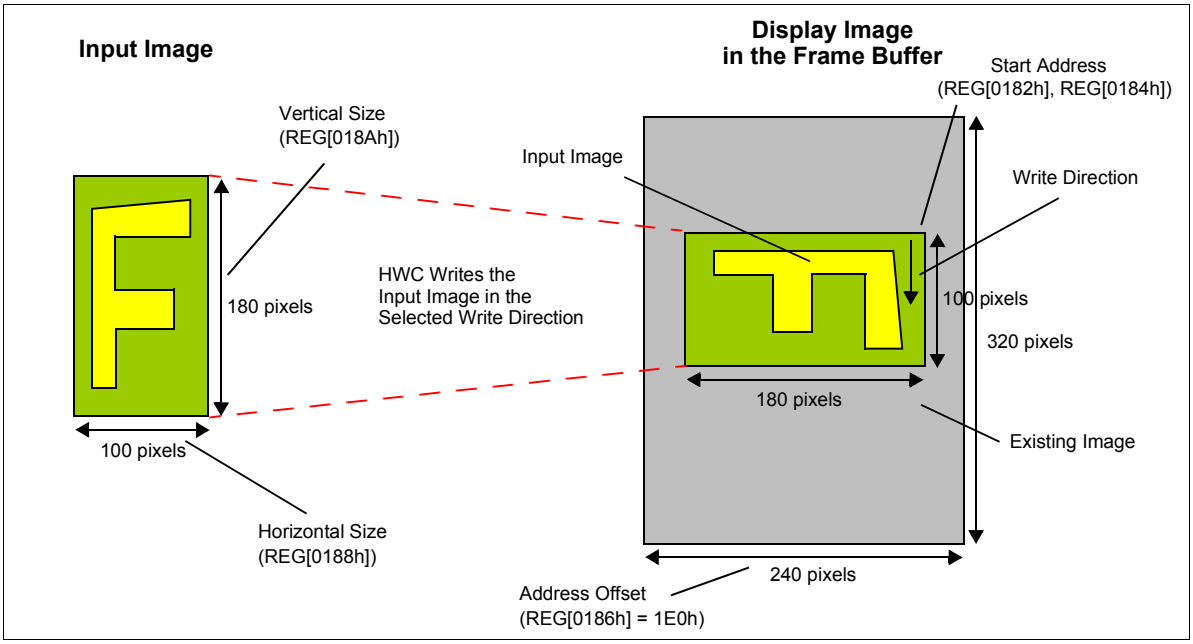


Figure 14-8: Writing for Rotation=90° and Mirror Disabled Example

For the above example, the Start Address is calculated using the following formula.

REG[0182h] ~ REG[0184h]
= memory start address + (input image vertical size x 2) - 2
= 1000h + (180 pixels x 2) - 2h
= 1000h + 168h - 2h
= 1166h

14.3.3 Writing for Rotation=180° and Mirror Disabled

When REG[0180h] bits 2-1 = 10b and REG[0180h] bit 3 = 0b, bit 1 of the Memory Start Address must be set to 1b (REG[0182h] bit 1 = 1b).

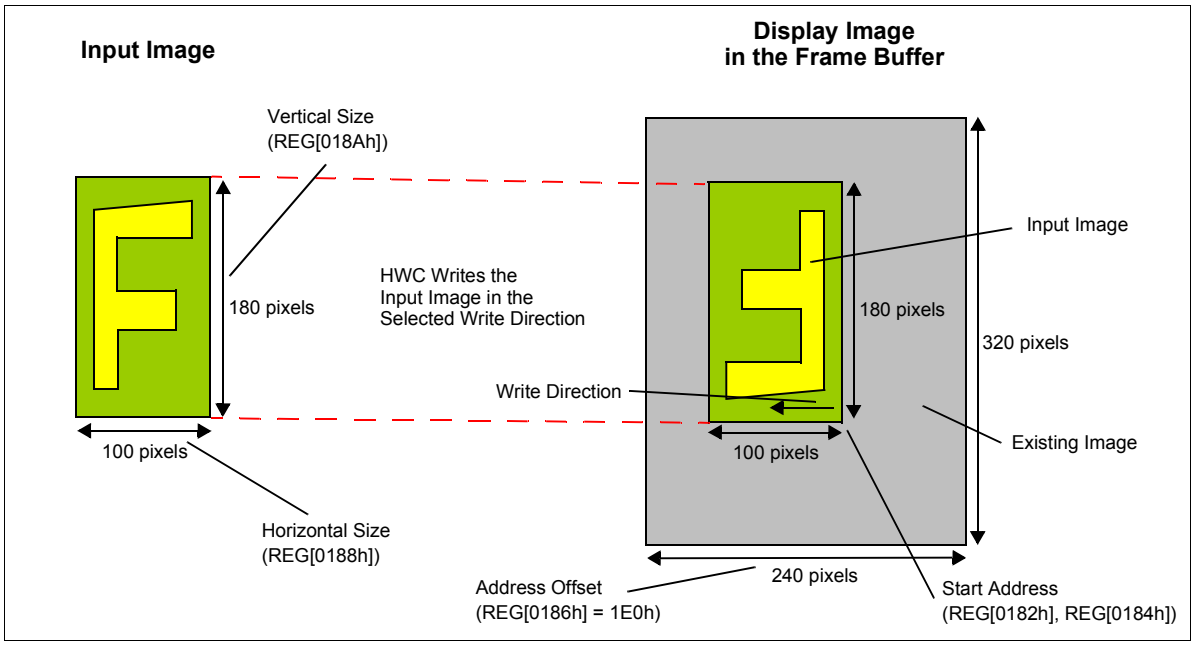


Figure 14-9: Writing for Rotation=180° and Mirror Disabled Example

For the above example, the Start Address is calculated using the following formula.

REG[0182h] ~ REG[0184h]
= (memory start address + input image data size) - 2
= (1000h + (180 x 100 x 2)) - 2h
= (1000h + 8CA0h) - 2h
= 9CA0h - 2h
= 9C9Eh

14.3.4 Writing for Rotation=270° and Mirror Disabled

When REG[0180h] bits 2-1 = 11b and REG[0180h] bit 3 = 0b, bit 1 of the Memory Start Address must be set to 0b (REG[0182h] bit 1 = 0b).

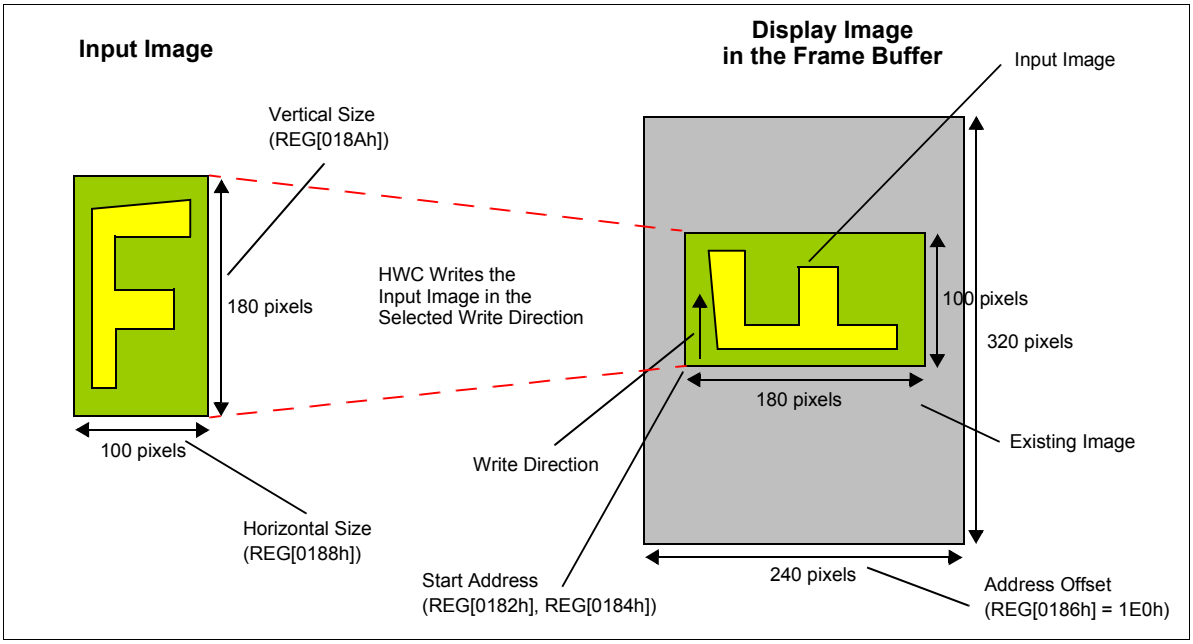


Figure 14-10: Writing for Rotation=270° and Mirror Disabled Example

For the above example, the Start Address is calculated using the following formula.

REG[0182h] ~ REG[0184h]
= (memory start address + input image data size) - (input image vertical size x 2)
= (1000h + (180 x 100 x 2)) - (180 pixels x 2)
= (1000h + 8CA0h) - 168h
= 9CA0h - B4h
= 9B38h

14.3.5 Writing for Rotation=0° and Mirror Enabled

When REG[0180h] bits 2-1 = 00b and REG[0180h] bit 3 = 1b, bit 1 of the Memory Start Address must be set to 1b (REG[0182h] bit 1 = 1b).

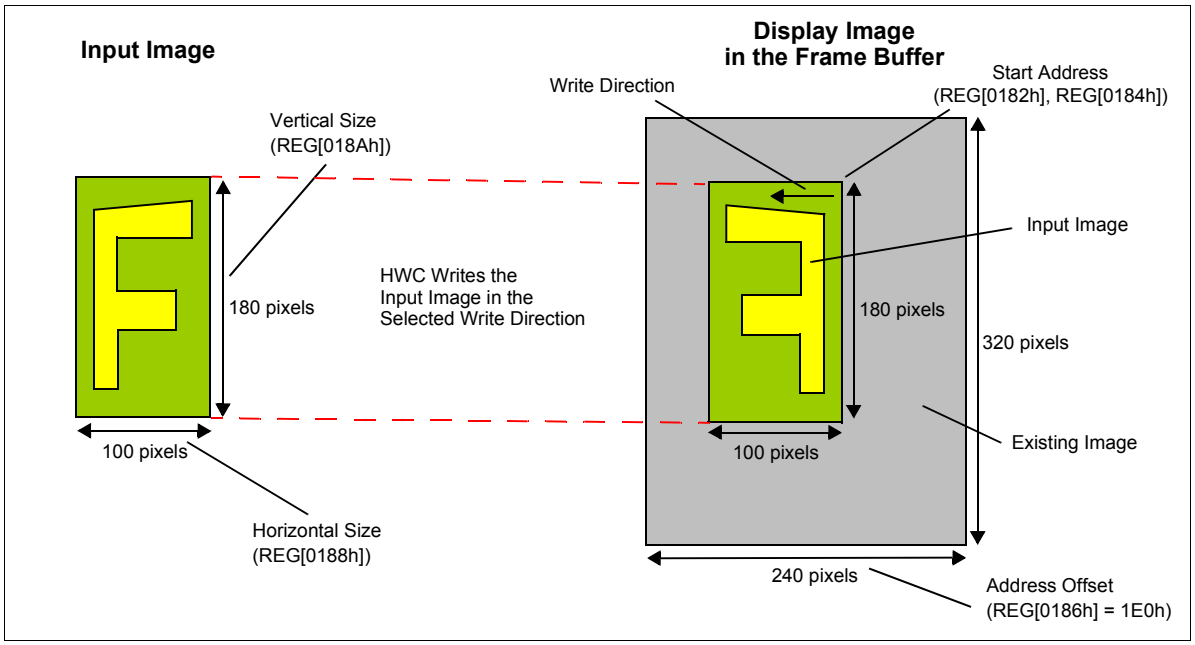


Figure 14-11: Writing for Rotation=0° and Mirror Enabled Example

For the above example, the Start Address is calculated using the following formula.

REG[0182h] ~ REG[0184h]
= memory start address + (input image horizontal size x 2) - 2
= 1000h + (100 pixels x 2) - 2h
= 1000h + C8h - 2h
= 10C6h

14.3.6 Writing for Rotation=90° and Mirror Enable

When REG[0180h] bits 2-1 = 01b and REG[0180h] bit 3 = 0b, bit 1 of the Memory Start Address must be set to 0b (REG[0182h] bit 1 = 0b).

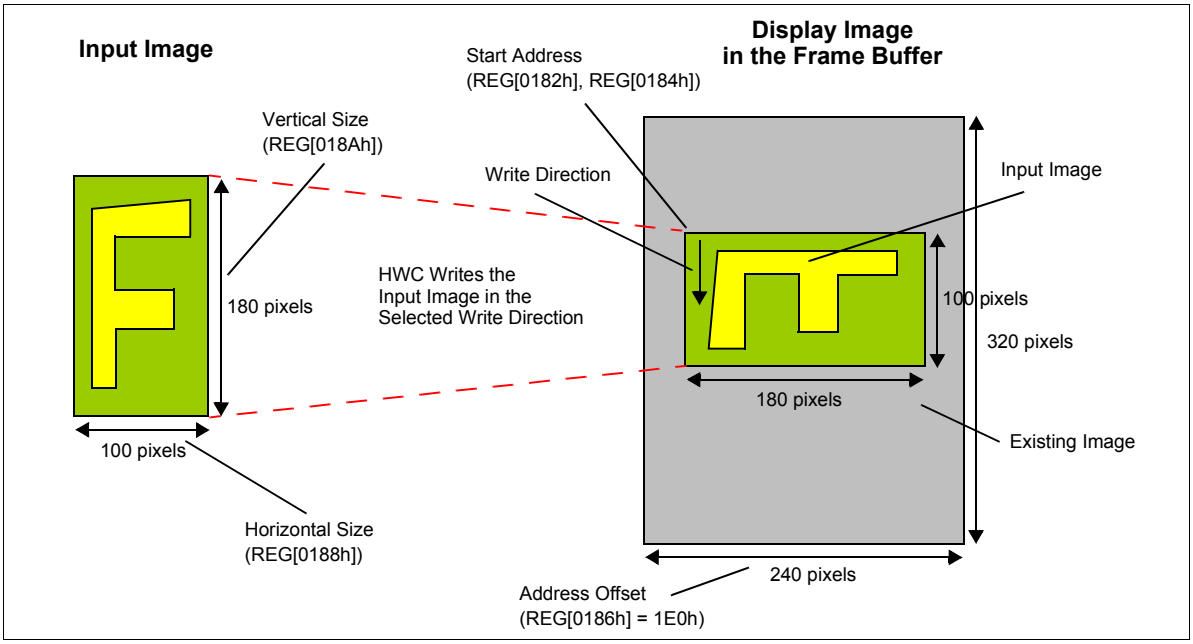


Figure 14-12: Writing for Rotation=90° and Mirror Enabled Example

For the above example, the Start Address is calculated using the following formula.

REG[0182h] ~ REG[0184h]
= memory start address
= 1000h

14.3.7 Writing for Rotation=180° and Mirror Enabled

When REG[0180h] bits 2-1 = 10b and REG[0180h] bit 3 = 0b, bit 1 of the Memory Start Address must be set to 0b (REG[0182h] bit 1 = 0b).

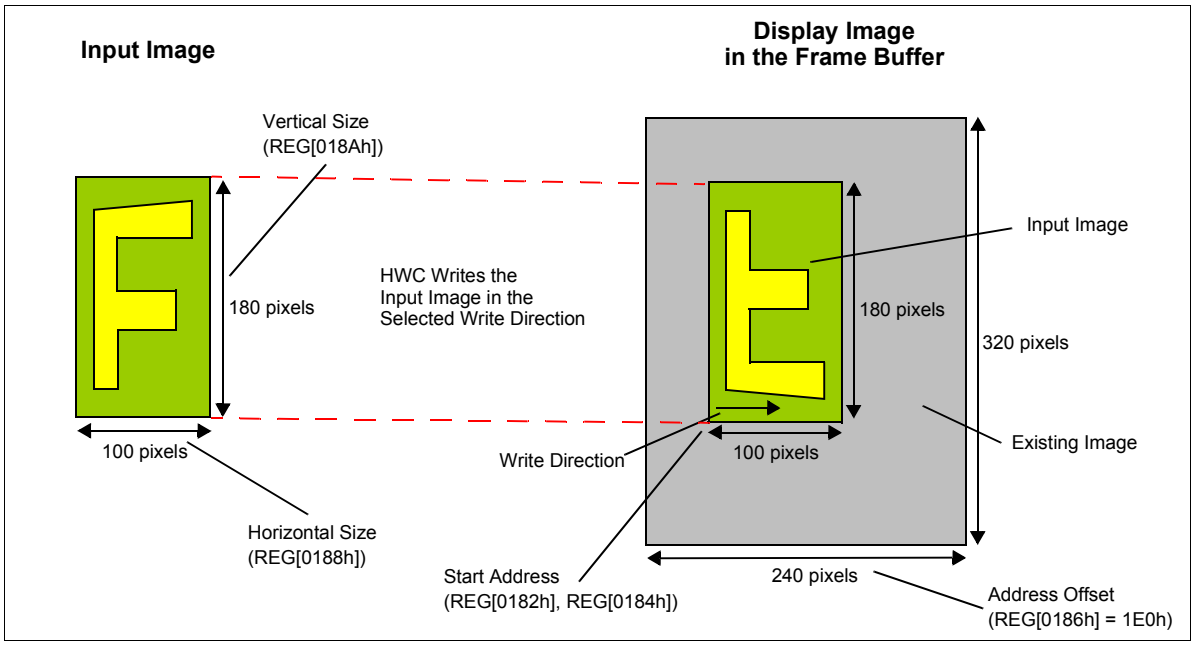


Figure 14-13: Writing for Rotation=180° and Mirror Enabled Example

For the above example, the Start Address is calculated using the following formula.

REG[0182h] ~ REG[0184h]
= (memory start address + input image data size) - (input image horizontal size x 2)
= (1000h + (180 x 100 x 2)) - (100 pixels x 2)
= 1000h + 8CA0h - C8h
= 9CA0h - C8h
= 9BD8h

14.3.8 Writing for Rotation=270° and Mirror Enabled

When REG[0180h] bits 2-1 = 11b and REG[0180h] bit 3 = 0b, bit 1 of the Memory Start Address must be set to 1b (REG[0182h] bit 1 = 1b).

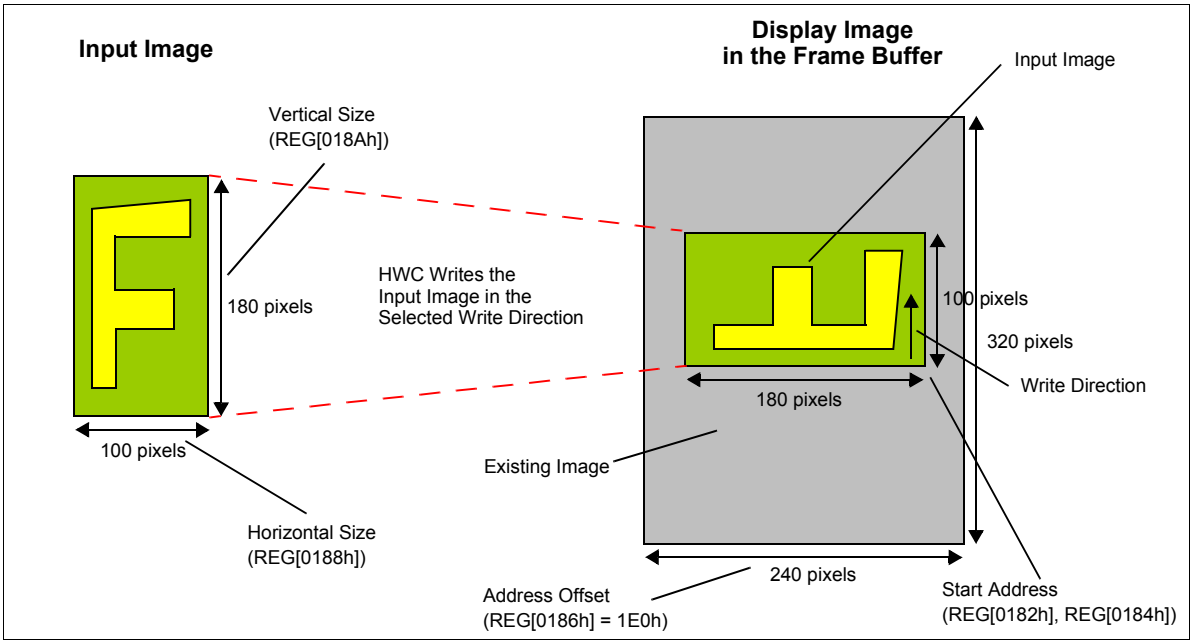


Figure 14-14: Writing for Rotation=270° and Mirror Enabled Example

For the above example, the Start Address is calculated using the following formula.

REG[0182h] ~ REG[0184h]
= (memory start address + input image data size) - 2
= (1000h + (180 x 100 x 2)) - 2h
= 1000h + 8CA0h - 2h
= 9CA0h - 2h
= 9C9Eh

14.3.9 HWC Memory Write Procedure

All memory accesses through the HWC use the Memory Access Port (REG[018Ch]). The following procedure allows data to be continuously written without resetting the Index. This procedure is used for all access using the HWC, regardless of the number of CLKs required for each Host interface access.

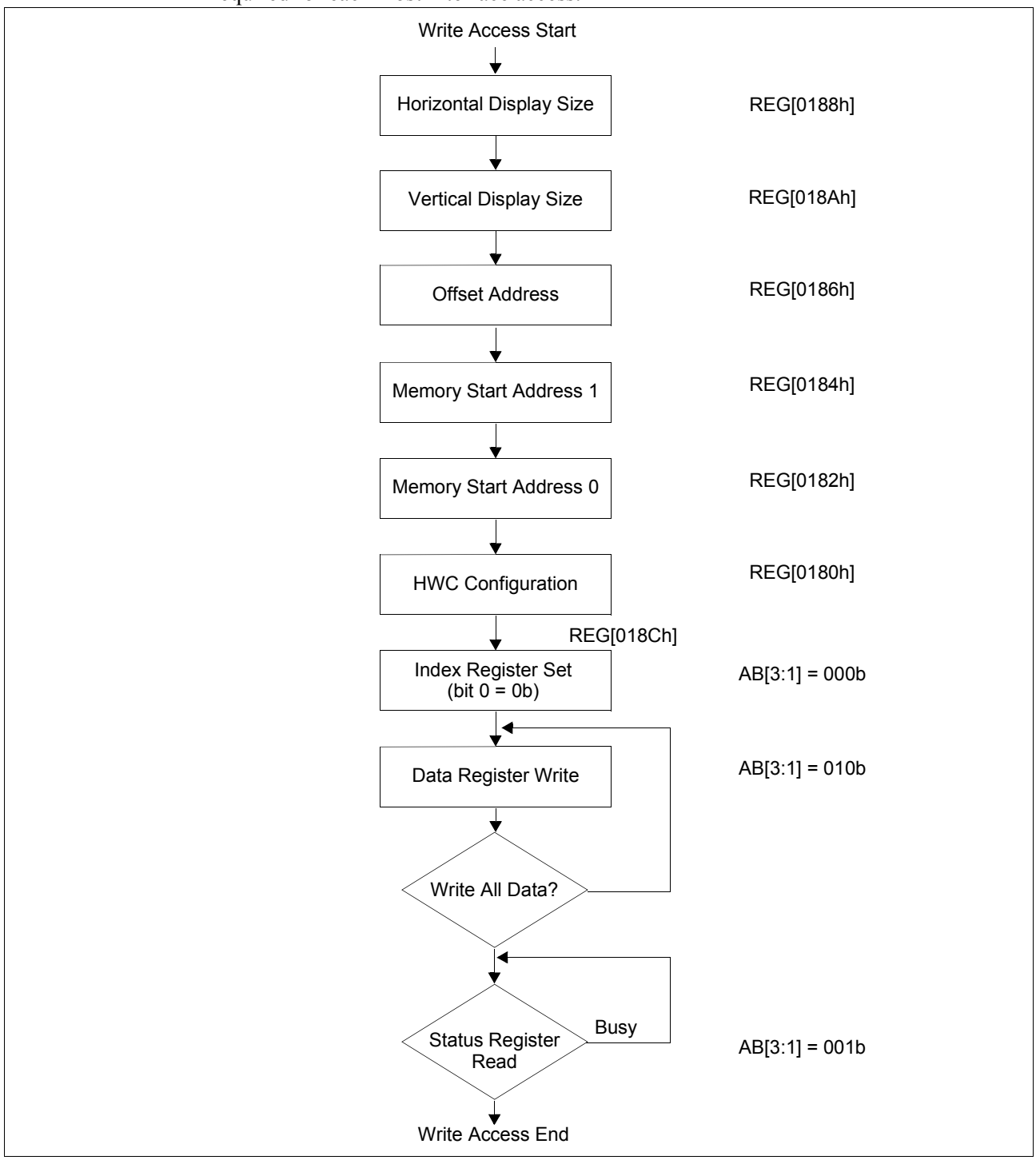


Figure 14-15: HWC Write Access Procedure (REG[0180h] bit 0 = 1b)

14.4 Direct Memory Access

The Host can directly access the S1D13L02 frame buffer memory without using the HWC. Direct memory access (REG[0180h] bit 0 = 0b) allows the frame buffer to be accessed using linear address mode or rectangular address mode (see REG[0184h] bit 15). However, when direct memory access is selected, the rotation and mirror functions are not available because they are part of the HWC.

14.4.1 Linear Address Mode

The S1D13L02 frame buffer can be directly accessed using the following procedure when linear access mode is selected, REG[0184h] bit 15 = 0b.

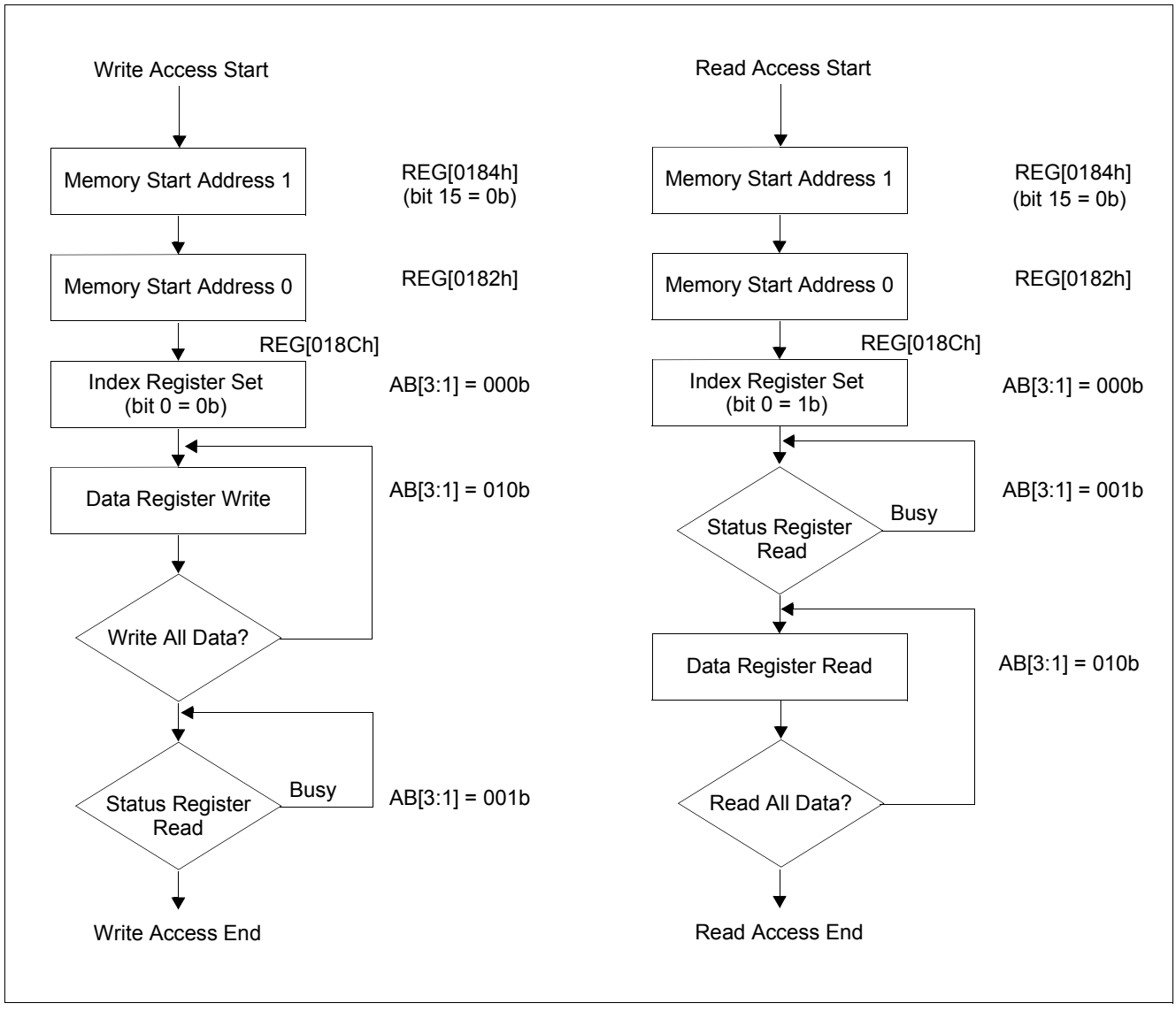


Figure 14-16: Direct Memory Access (REG[0180h] bit 0 = 0b, REG[0184h] bit 15 = 0b)

14.4.2 Rectangular Address Mode

The S1D13L02 frame buffer can be directly accessed using the following procedure when rectangular access mode is selected, REG[0184h] bit 15 = 1b.

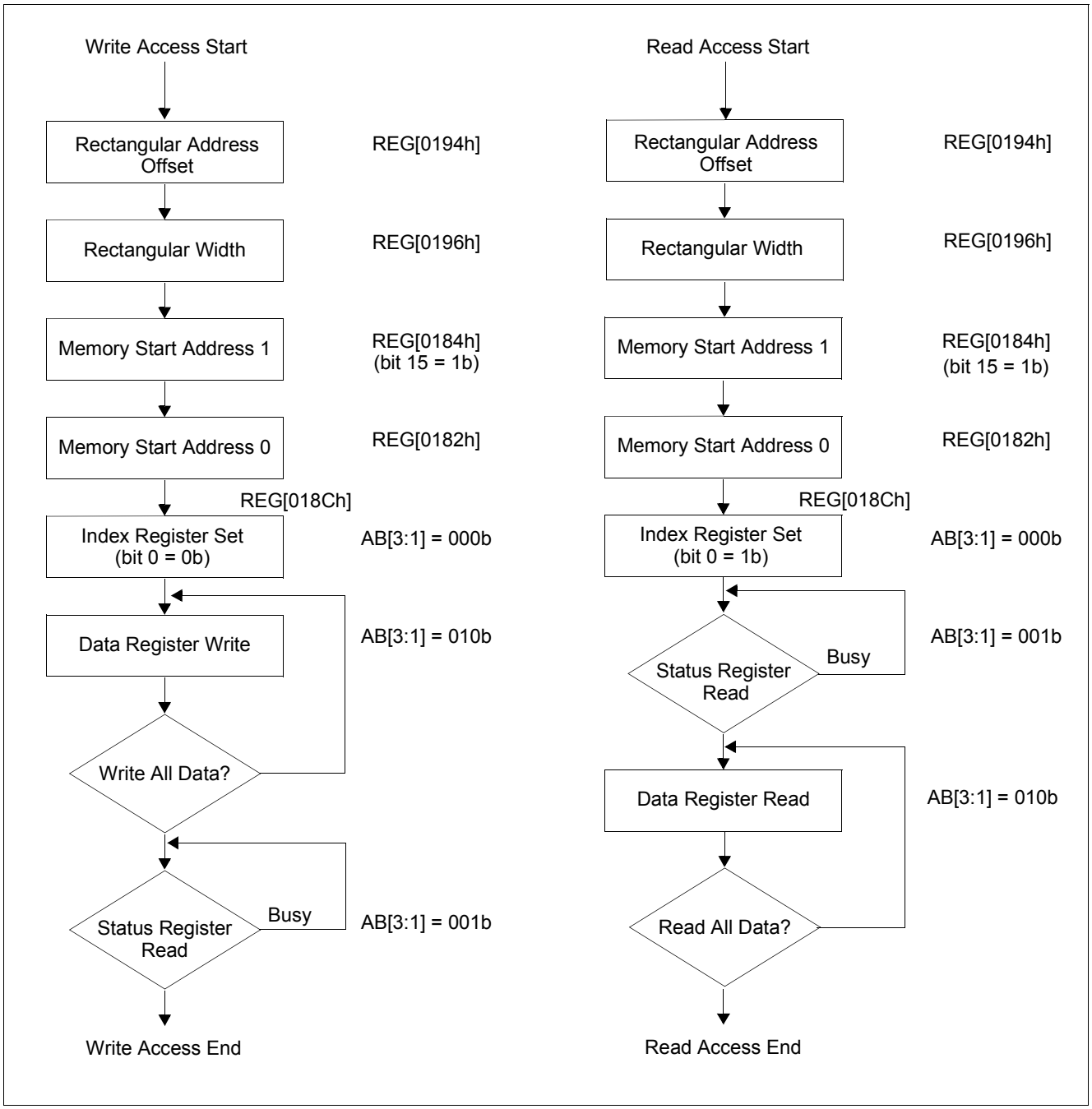


Figure 14-17: Direct Rectangular Memory Access (REG[0180h] bit 0 = 0b, REG[0184h] bit 15 = 1b)

14.5 Host Interface VSYNC Output

The state of the LCD VSYNC signal (on the FPFRAME LCD interface pin) is output to the Host interface on the VOUT pin.

The frequency of VOUT output can be varied using the VOUT Output Rate bits (REG[0198h] bits 15-12) to range from one VOUT output for each LCD VSYNC to one VOUT for every 15 LCD VSYNCs. VOUT output can also be delayed for up to 1023 lines after the LCD VSYNC takes place by configuring the VOUT Delay Control bits (REG[0198h] bits 9-0).

15 LCD Interface

The S1D13L02 can be connected to RGB interface LCD panel.

RGB 8:8:8 image data is passed from Window Control, which controls windowing functions such as transparency and alpha blending, to the LCD Interface. The LCD-LUT allows the LCD output to be gamma corrected, if required. The Dither (or Pseudo Output Color) block provides several methods to optimize the internal RGB 8:8:8 format data for output to panels of various data widths.

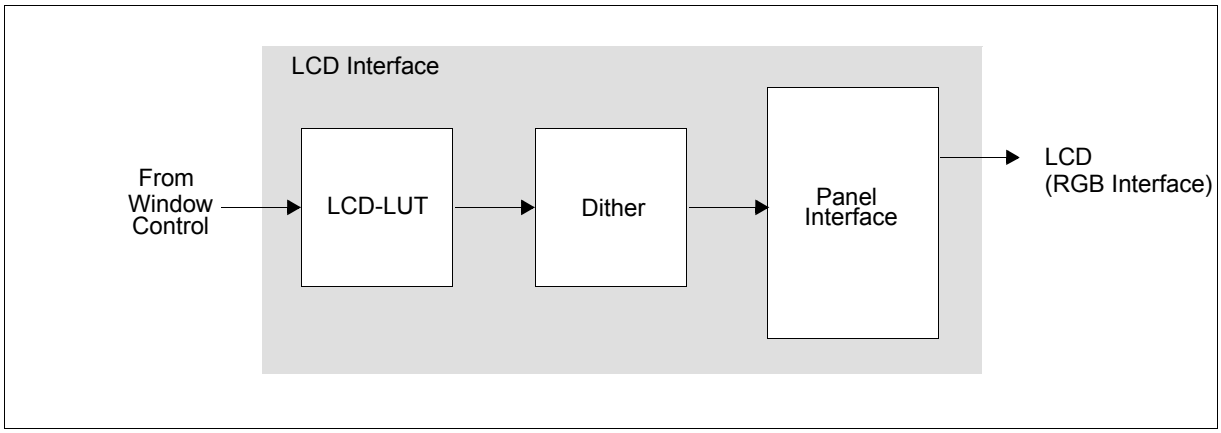


Figure 15-1: LCD Interface Overview

15.1 RGB Interface Data Formats

The RGB Interface data format for the panel is determined by the data bus width, which is set using the RGB Interface Panel Data Bus Width bits (REG[0032h] bits 6-4). The following data formats are supported.

When REG[0032h] bits 6-4 = 000b, the data width is 9-bit
When REG[0032h] bits 6-4 = 001b, the data width is 12-bit
When REG[0032h] bits 6-4 = 010b, the data width is 16-bit
When REG[0032h] bits 6-4 = 011b, the data width is 18-bit
When REG[0032h] bits 6-4 = 100b, the data width is 24-bit

Table 15-1: 9/12/16/18/24-bit RGB Interface Data Formats

Pin	9-bit	12-bit	16-bit	18-bit	24-bit
FPDAT0	R^7	R^7	R^7	R^7	R^7
FPDAT1	R^6	R^6	R^6	R^6	R^6
FPDAT2	R^5	R^5	R^5	R^5	R^5
FPDAT3	G^7	G^7	G^7	G^7	G^7
FPDAT4	G^6	G^6	G^6	G^6	G^6
FPDAT5	G^5	G^5	G^5	G^5	G^5
FPDAT6	B^7	B^7	B^7	B^7	B^7

Table 15-1: 9/12/16/18/24-bit RGB Interface Data Formats

Pin	9-bit	12-bit	16-bit	18-bit	24-bit
FPDAT7	B^6	B^6	B^6	B^6	B^6
FPDAT8	B^5	B^5	B^5	B^5	B^5
FPDAT9	Low	R^4	R^4	R^4	R^4
FPDAT10	Low	Low	R^3	R^3	R^3
FPDAT11	Low	Low	Low	R^2	R^2
FPDAT12	Low	G^4	G^4	G^4	G^4
FPDAT13	Low	Low	G^3	G^3	G^3
FPDAT14	Low	Low	G^2	G^2	G^2
FPDAT15	Low	B^4	B^4	B^4	B^4
FPDAT16	Low	Low	B^3	B^3	B^3
FPDAT17	Low	Low	Low	B^2	B^2
FPDAT18	Low	Low	Low	Low	R^1
FPDAT19	Low	Low	Low	Low	R^0
FPDAT20	Low	Low	Low	Low	G^1
FPDAT21	Low	Low	Low	Low	G^0
FPDAT22	Low	Low	Low	Low	B^1
FPDAT23	Low	Low	Low	Low	B^0

16 Use Cases

16.1 Display using Main and PIP1 Window

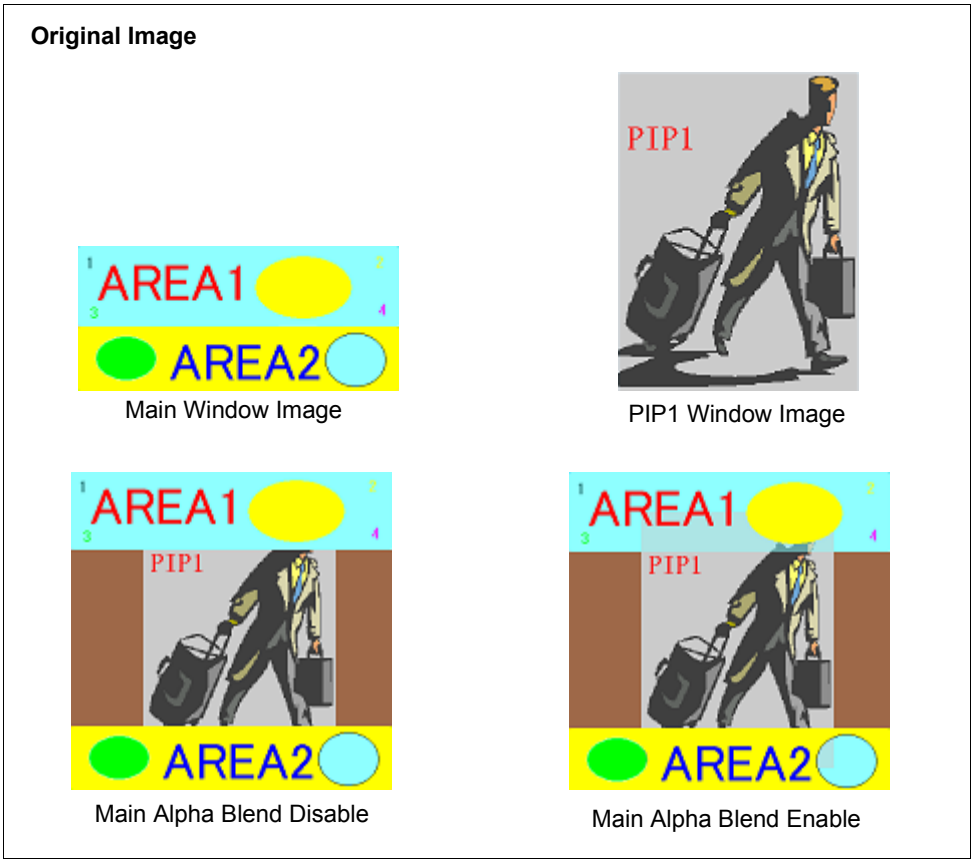


Figure 16-1: Main Window (Top) and PIP1 Window (Bottom) Display Example

Table 16-1: Main Window (Top) and PIP1 Window (Bottom) Display Example Settings

REG[0202h] bit 0	Main Window Display Enable	1: on
REG[0202h] bit 1	PIP1 Window Display Enable	1: on
REG[0202h] bit 2	PIP2 Window Display Enable	0: off
REG[0202h] bit 4	Main Display Mode Select	1: Main1 and Main2
REG[0202h] bit 5	Main Layer Mode Select	0: Main on PIP
REG[0202h] bit 6	PIP Layer Mode Select	-
REG[0204h] bit 1	PIP1 Transparency Enable	0: off
REG[0204h] bit 2	PIP2 Transparency Enable	0: off
REG[0204h] bit 7	Alpha Blend Mode Select	0: Main and PIP
REG[0204h] bit 8	Alpha Blend Key Color1 Enable	0 or 1
REG[0204h] bit 9	Alpha Blend Key Color2 Enable	0: off
REG[0204h] bit 10	Alpha Blend Key Color3 Enable	0: off
REG[0204h] bit 11	Alpha Blend Key Color4 Enable	0: off
REG[0206h] bit 15-0	Back Ground Color	
REG[0208h] bit 3-0	Alpha Blend1 Ratio	4h: 50%
REG[0208h] bit 7-4	Alpha Blend2 Ratio	-
REG[0208h] bit 11-8	Alpha Blend3 Ratio	-
REG[0208h] bit 15-12	Alpha Blend4 Ratio	-
REG[020Ch] bit 15-0	PIP1 Transparency Key Color	-
REG[020Eh] bit 15-0	PIP2 Transparency Key Color	-
REG[0210h] bit 15-0	Alpha Blend1 Key Color	
REG[0212h] bit 15-0	Alpha Blend2 Key Color	-
REG[0214h] bit 15-0	Alpha Blend3 Key Color	-
REG[0216h] bit 15-0	Alpha Blend4 Key Color	-

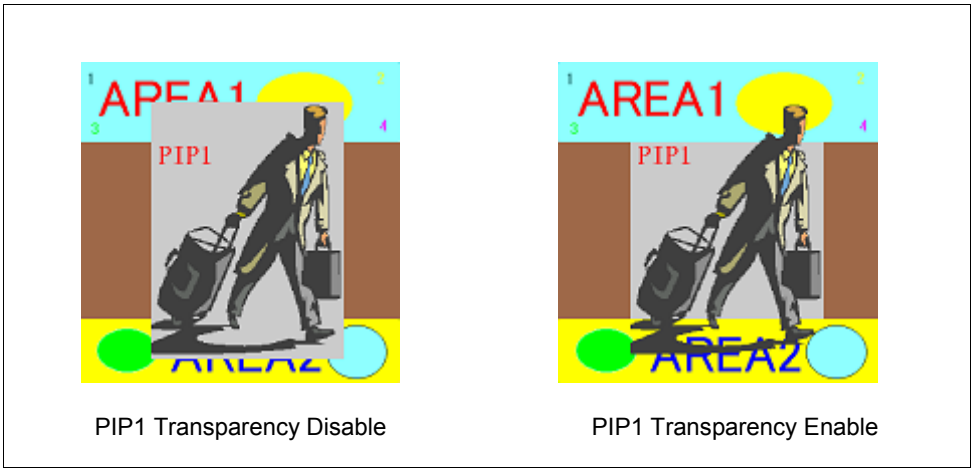


Figure 16-2: PIP1 Window (Top) and Main Window (Bottom) Display Example

Table 16-2: PIP1 Window (Top) and Main Window (Bottom) Display Example Settings

REG[0202h] bit 0	Main Window Display Enable	1: on
REG[0202h] bit 1	PIP1 Window Display Enable	1: on
REG[0202h] bit 2	PIP2 Window Display Enable	0: off
REG[0202h] bit 4	Main Display Mode Select	1: Main1 and Main2
REG[0202h] bit 5	Main Layer Mode Select	1: PIP on Main
REG[0202h] bit 6	PIP Layer Mode Select	-
REG[0204h] bit 1	PIP1 Transparency Enable	0 or 1
REG[0204h] bit 2	PIP2 Transparency Enable	0: off
REG[0204h] bit 7	Alpha Blend Mode Select	-
REG[0204h] bit 8	Alpha Blend Key Color1 Enable	0: off
REG[0204h] bit 9	Alpha Blend Key Color2 Enable	0: off
REG[0204h] bit 10	Alpha Blend Key Color3 Enable	0: off
REG[0204h] bit 11	Alpha Blend Key Color4 Enable	0: off
REG[0206h] bit 15-0	Back Ground Color	
REG[0208h] bit 3-0	Alpha Blend1 Ratio	-
REG[0208h] bit 7-4	Alpha Blend2 Ratio	-
REG[0208h] bit 11-8	Alpha Blend3 Ratio	-
REG[0208h] bit 15-12	Alpha Blend4 Ratio	-
REG[020Ch] bit 15-0	PIP1 Transparency Key Color	
REG[020Eh] bit 15-0	PIP2 Transparency Key Color	-
REG[0210h] bit 15-0	Alpha Blend1 Key Color	-
REG[0212h] bit 15-0	Alpha Blend2 Key Color	-
REG[0214h] bit 15-0	Alpha Blend3 Key Color	-
REG[0216h] bit 15-0	Alpha Blend4 Key Color	-

16.2 Display using Main and PIP2 Window

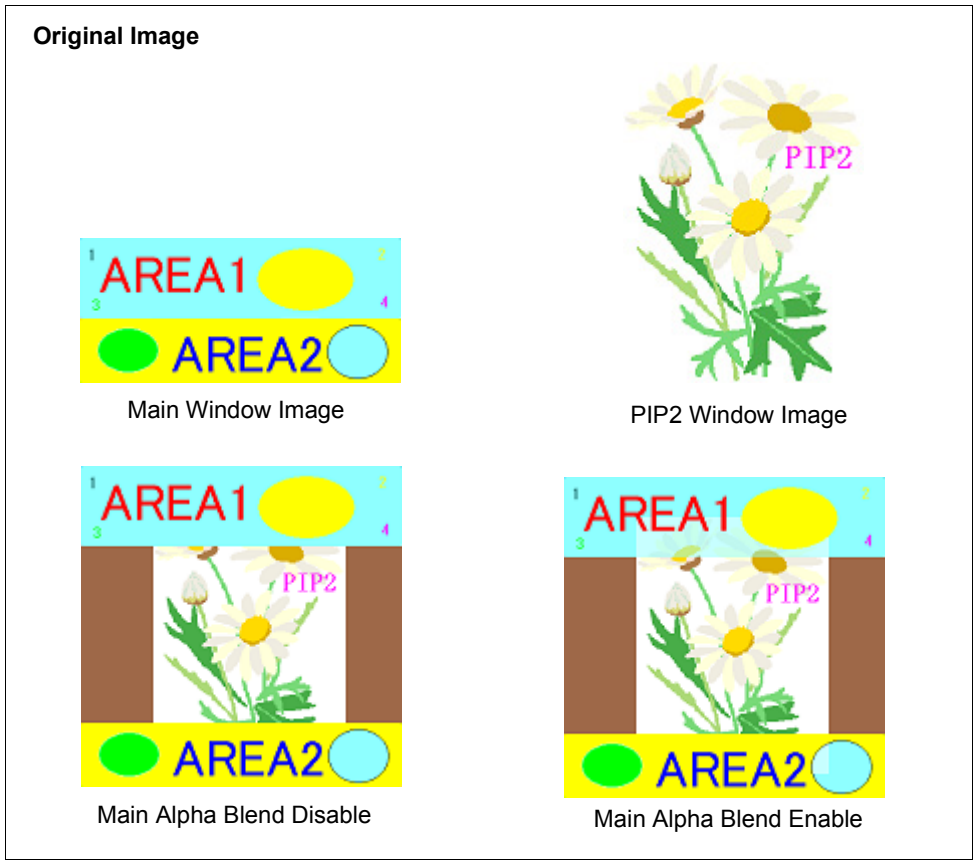


Figure 16-3: Main Window (Top) and PIP2 Window (Bottom) Display Example

Table 16-3: Main Window (Top) and PIP2 Window (Bottom) Display Example Settings

REG[0202h] bit 0	Main Window Display Enable	1: on
REG[0202h] bit 1	PIP1 Window Display Enable	0: off
REG[0202h] bit 2	PIP2 Window Display Enable	1: on
REG[0202h] bit 4	Main Display Mode Select	1: Main1 and Main2
REG[0202h] bit 5	Main Layer Mode Select	0: Main on PIP
REG[0202h] bit 6	PIP Layer Mode Select	-
REG[0204h] bit 1	PIP1 Transparency Enable	0: off
REG[0204h] bit 2	PIP2 Transparency Enable	0: off
REG[0204h] bit 7	Alpha Blend Mode Select	0: Main and PIP
REG[0204h] bit 8	Alpha Blend Key Color1 Enable	0 or 1
REG[0204h] bit 9	Alpha Blend Key Color2 Enable	0: off
REG[0204h] bit 10	Alpha Blend Key Color3 Enable	0: off
REG[0204h] bit 11	Alpha Blend Key Color4 Enable	0: off
REG[0206h] bit 15-0	Back Ground Color	
REG[0208h] bit 3-0	Alpha Blend1 Ratio	4h: 50%
REG[0208h] bit 7-4	Alpha Blend2 Ratio	-
REG[0208h] bit 11-8	Alpha Blend3 Ratio	-
REG[0208h] bit 15-12	Alpha Blend4 Ratio	-
REG[020Ch] bit 15-0	PIP1 Transparency Key Color	-
REG[020Eh] bit 15-0	PIP2 Transparency Key Color	-
REG[0210h] bit 15-0	Alpha Blend1 Key Color	
REG[0212h] bit 15-0	Alpha Blend2 Key Color	-
REG[0214h] bit 15-0	Alpha Blend3 Key Color	-
REG[0216h] bit 15-0	Alpha Blend4 Key Color	-

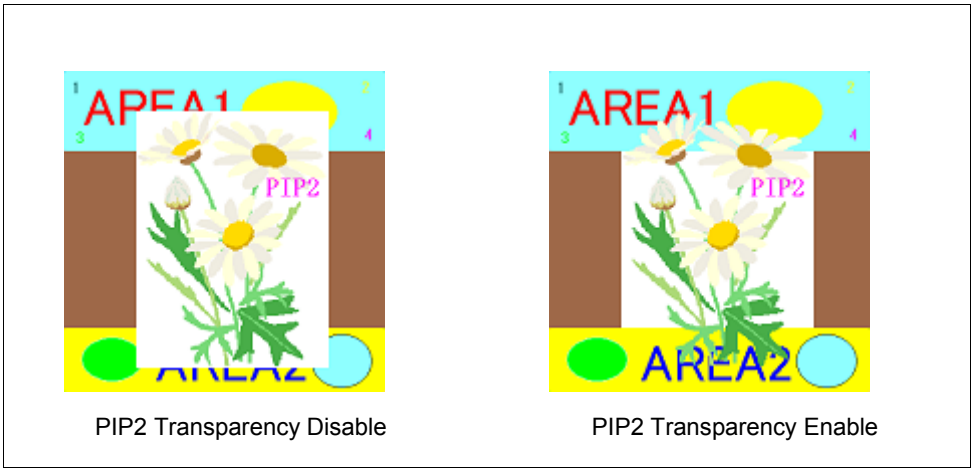


Figure 16-4: PIP2 Window (Top) and Main Window (Bottom) Display Example

Table 16-4: PIP2 Window (Top) and Main Window (Bottom) Display Example Settings

REG[0202h] bit 0	Main Window Display Enable	1: on
REG[0202h] bit 1	PIP1 Window Display Enable	0: off
REG[0202h] bit 2	PIP2 Window Display Enable	1: on
REG[0202h] bit 4	Main Display Mode Select	1: Main1 and Main2
REG[0202h] bit 5	Main Layer Mode Select	1: PIP on Main
REG[0202h] bit 6	PIP Layer Mode Select	-
REG[0204h] bit 1	PIP1 Transparency Enable	0: off
REG[0204h] bit 2	PIP2 Transparency Enable	0 or 1
REG[0204h] bit 7	Alpha Blend Mode Select	-
REG[0204h] bit 8	Alpha Blend Key Color1 Enable	0: off
REG[0204h] bit 9	Alpha Blend Key Color2 Enable	0: off
REG[0204h] bit 10	Alpha Blend Key Color3 Enable	0: off
REG[0204h] bit 11	Alpha Blend Key Color4 Enable	0: off
REG[0206h] bit 15-0	Back Ground Color	
REG[0208h] bit 3-0	Alpha Blend1 Ratio	-
REG[0208h] bit 7-4	Alpha Blend2 Ratio	-
REG[0208h] bit 11-8	Alpha Blend3 Ratio	-
REG[0208h] bit 15-12	Alpha Blend4 Ratio	-
REG[020Ch] bit 15-0	PIP1 Transparency Key Color	-
REG[020Eh] bit 15-0	PIP2 Transparency Key Color	
REG[0210h] bit 15-0	Alpha Blend1 Key Color	-
REG[0212h] bit 15-0	Alpha Blend2 Key Color	-
REG[0214h] bit 15-0	Alpha Blend3 Key Color	-
REG[0216h] bit 15-0	Alpha Blend4 Key Color	-

16.3 Display using Main, PIP1 and PIP2 Window

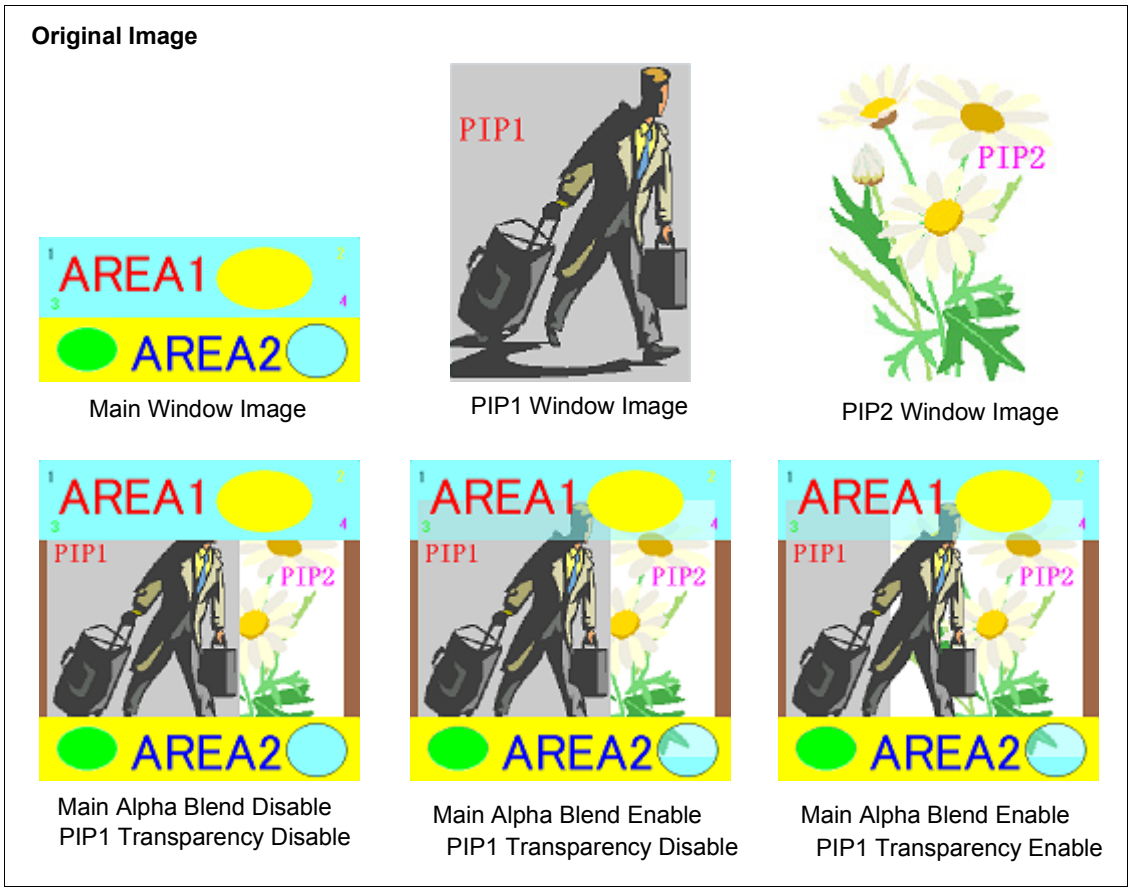


Figure 16-5: Main Window (Top), PIP1 (Middle), PIP2 (Bottom) Display Example

Table 16-5: Main Window (Top), PIP1 (Middle), PIP2 (Bottom) Display Example Settings

REG[0202h] bit 0	Main Window Display Enable	1: on
REG[0202h] bit 1	PIP1 Window Display Enable	1: on
REG[0202h] bit 2	PIP2 Window Display Enable	1: on
REG[0202h] bit 4	Main Display Mode Select	1: Main1 and Main2
REG[0202h] bit 5	Main Layer Mode Select	0: Main on PIP
REG[0202h] bit 6	PIP Layer Mode Select	0: PIP1 on PIP2
REG[0204h] bit 1	PIP1 Transparency Enable	0 or 1
REG[0204h] bit 2	PIP2 Transparency Enable	0: off
REG[0204h] bit 7	Alpha Blend Mode Select	0: Main and PIP
REG[0204h] bit 8	Alpha Blend Key Color1 Enable	0 or 1
REG[0204h] bit 9	Alpha Blend Key Color2 Enable	0: off
REG[0204h] bit 10	Alpha Blend Key Color3 Enable	0: off
REG[0204h] bit 11	Alpha Blend Key Color4 Enable	0: off
REG[0206h] bit 15-0	Back Ground Color	
REG[0208h] bit 3-0	Alpha Blend1 Ratio	4h: 50%
REG[0208h] bit 7-4	Alpha Blend2 Ratio	-
REG[0208h] bit 11-8	Alpha Blend3 Ratio	-
REG[0208h] bit 15-12	Alpha Blend4 Ratio	-
REG[020Ch] bit 15-0	PIP1 Transparency Key Color	
REG[020Eh] bit 15-0	PIP2 Transparency Key Color	-
REG[0210h] bit 15-0	Alpha Blend1 Key Color	
REG[0212h] bit 15-0	Alpha Blend2 Key Color	-
REG[0214h] bit 15-0	Alpha Blend3 Key Color	-
REG[0216h] bit 15-0	Alpha Blend4 Key Color	-

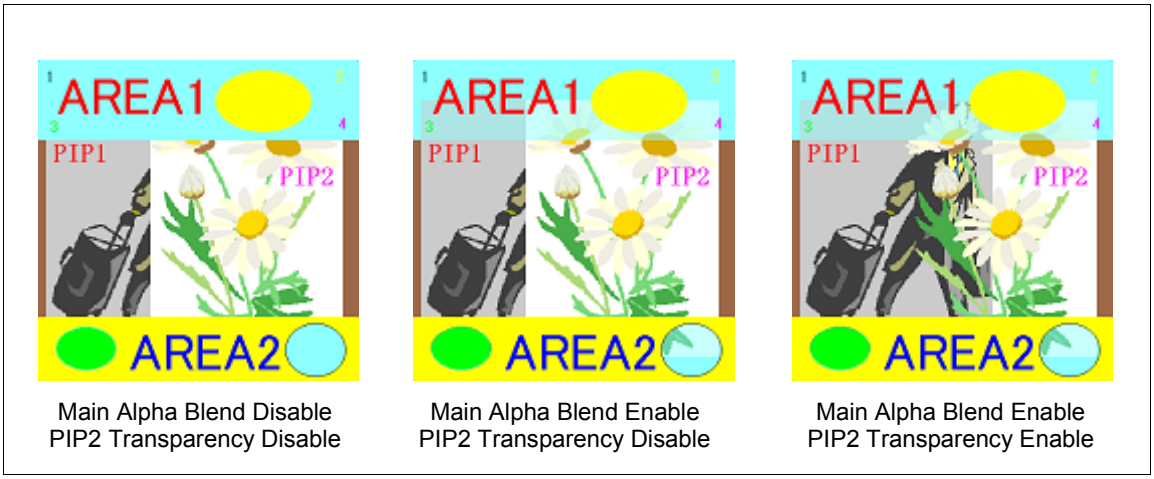


Figure 16-6: Main Window (Top), PIP2 (Middle), and PIP1 (Bottom) Display Example

Table 16-6: Main Window (Top), PIP2 (Middle), and PIP1 (Bottom) Display Example Settings

REG[0202h] bit 0	Main Window Display Enable	1: on
REG[0202h] bit 1	PIP1 Window Display Enable	1: on
REG[0202h] bit 2	PIP2 Window Display Enable	1: on
REG[0202h] bit 4	Main Display Mode Select	1: Main1 and Main2
REG[0202h] bit 5	Main Layer Mode Select	0: Main on PIP
REG[0202h] bit 6	PIP Layer Mode Select	1: PIP2 on PIP1
REG[0204h] bit 1	PIP1 Transparency Enable	0: off
REG[0204h] bit 2	PIP2 Transparency Enable	0 or 1
REG[0204h] bit 7	Alpha Blend Mode Select	0: Main and PIP
REG[0204h] bit 8	Alpha Blend Key Color1 Enable	0 or 1
REG[0204h] bit 9	Alpha Blend Key Color2 Enable	0: off
REG[0204h] bit 10	Alpha Blend Key Color3 Enable	0: off
REG[0204h] bit 11	Alpha Blend Key Color4 Enable	0: off
REG[0206h] bit 15-0	Back Ground Color	
REG[0208h] bit 3-0	Alpha Blend1 Ratio	4h: 50%
REG[0208h] bit 7-4	Alpha Blend2 Ratio	-
REG[0208h] bit 11-8	Alpha Blend3 Ratio	-
REG[0208h] bit 15-12	Alpha Blend4 Ratio	-
REG[020Ch] bit 15-0	PIP1 Transparency Key Color	-
REG[020Eh] bit 15-0	PIP2 Transparency Key Color	
REG[0210h] bit 15-0	Alpha Blend1 Key Color	
REG[0212h] bit 15-0	Alpha Blend2 Key Color	-
REG[0214h] bit 15-0	Alpha Blend3 Key Color	-
REG[0216h] bit 15-0	Alpha Blend4 Key Color	-

PIP1 Transparency Disable
PIP2 Transparency Disable

PIP1 Transparency Enable
PIP2 Transparency Disable

PIP1 Transparency Enable
PIP2 Transparency Enable

Figure 16-7: PIP1 (Top), PIP2 (Middle), and Main (Bottom) Display Example

Table 16-7: PIP1 (Top), PIP2 (Middle), and Main (Bottom) Display Example Settings

REG[0202h] bit 0	Main Window Display Enable	1: on
REG[0202h] bit 1	PIP1 Window Display Enable	1: on
REG[0202h] bit 2	PIP2 Window Display Enable	1: on
REG[0202h] bit 4	Main Display Mode Select	1: Main1 and Main2
REG[0202h] bit 5	Main Layer Mode Select	1: PIP on Main
REG[0202h] bit 6	PIP Layer Mode Select	0: PIP1 on PIP2
REG[0204h] bit 1	PIP1 Transparency Enable	0 or 1
REG[0204h] bit 2	PIP2 Transparency Enable	0 or 1
REG[0204h] bit 7	Alpha Blend Mode Select	-
REG[0204h] bit 8	Alpha Blend Key Color1 Enable	0: off
REG[0204h] bit 9	Alpha Blend Key Color2 Enable	0: off
REG[0204h] bit 10	Alpha Blend Key Color3 Enable	0: off
REG[0204h] bit 11	Alpha Blend Key Color4 Enable	0: off
REG[0206h] bit 15-0	Back Ground Color	
REG[0208h] bit 3-0	Alpha Blend1 Ratio	-
REG[0208h] bit 7-4	Alpha Blend2 Ratio	-
REG[0208h] bit 11-8	Alpha Blend3 Ratio	-
REG[0208h] bit 15-12	Alpha Blend4 Ratio	-
REG[020Ch] bit 15-0	PIP1 Transparency Key Color	
REG[020Eh] bit 15-0	PIP2 Transparency Key Color	
REG[0210h] bit 15-0	Alpha Blend1 Key Color	-
REG[0212h] bit 15-0	Alpha Blend2 Key Color	-
REG[0214h] bit 15-0	Alpha Blend3 Key Color	-
REG[0216h] bit 15-0	Alpha Blend4 Key Color	-

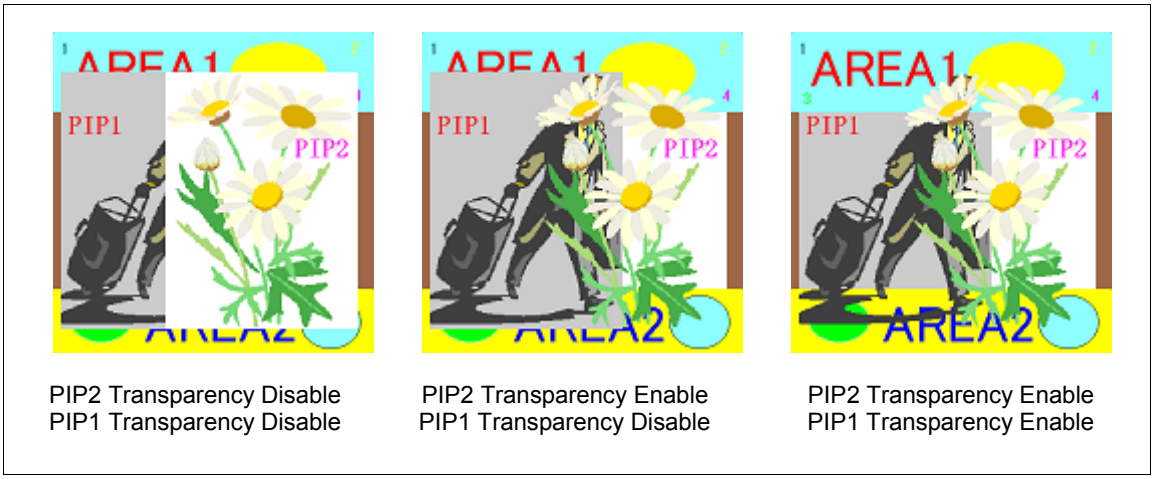


Figure 16-8: PIP2 (Top), PIP1 (Middle), and Main (Bottom) Display Example

Table 16-8: PIP1 (Top), PIP2 (Middle), and Main (Bottom) Display Example Settings

REG[0202h] bit 0	Main Window Display Enable	1: on
REG[0202h] bit 1	PIP1 Window Display Enable	1: on
REG[0202h] bit 2	PIP2 Window Display Enable	1: on
REG[0202h] bit 4	Main Display Mode Select	1: Main1 and Main2
REG[0202h] bit 5	Main Layer Mode Select	1: PIP on Main
REG[0202h] bit 6	PIP Layer Mode Select	1: PIP2 on PIP1
REG[0204h] bit 1	PIP1 Transparency Enable	0 or 1
REG[0204h] bit 2	PIP2 Transparency Enable	0 or 1
REG[0204h] bit 7	Alpha Blend Mode Select	-
REG[0204h] bit 8	Alpha Blend Key Color1 Enable	0: off
REG[0204h] bit 9	Alpha Blend Key Color2 Enable	0: off
REG[0204h] bit 10	Alpha Blend Key Color3 Enable	0: off
REG[0204h] bit 11	Alpha Blend Key Color4 Enable	0: off
REG[0206h] bit 15-0	Back Ground Color	
REG[0208h] bit 3-0	Alpha Blend1 Ratio	-
REG[0208h] bit 7-4	Alpha Blend2 Ratio	-
REG[0208h] bit 11-8	Alpha Blend3 Ratio	-
REG[0208h] bit 15-12	Alpha Blend4 Ratio	-
REG[020Ch] bit 15-0	PIP1 Transparency Key Color	
REG[020Eh] bit 15-0	PIP2 Transparency Key Color	
REG[0210h] bit 15-0	Alpha Blend1 Key Color	-
REG[0212h] bit 15-0	Alpha Blend2 Key Color	-
REG[0214h] bit 15-0	Alpha Blend3 Key Color	-
REG[0216h] bit 15-0	Alpha Blend4 Key Color	-

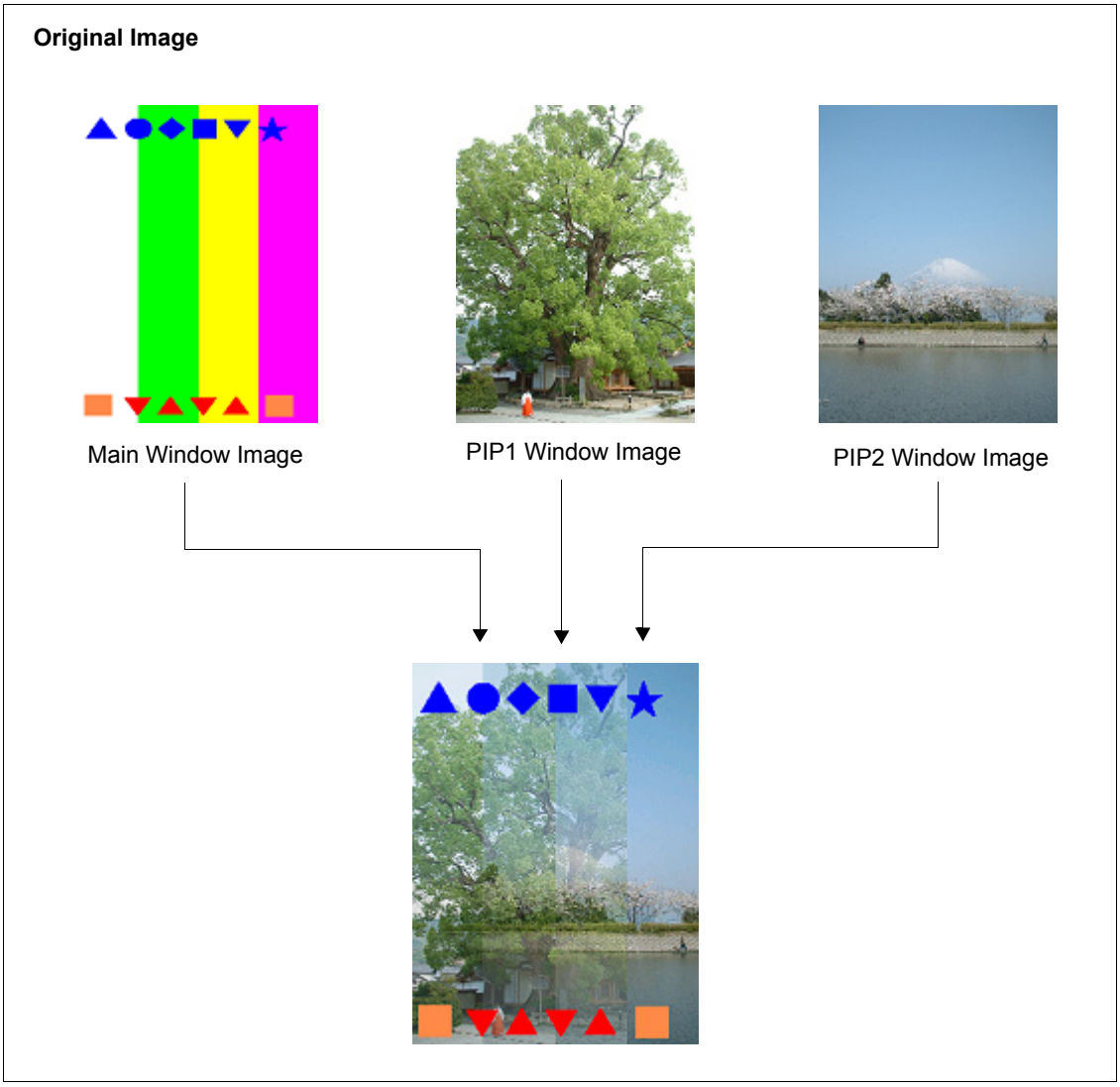
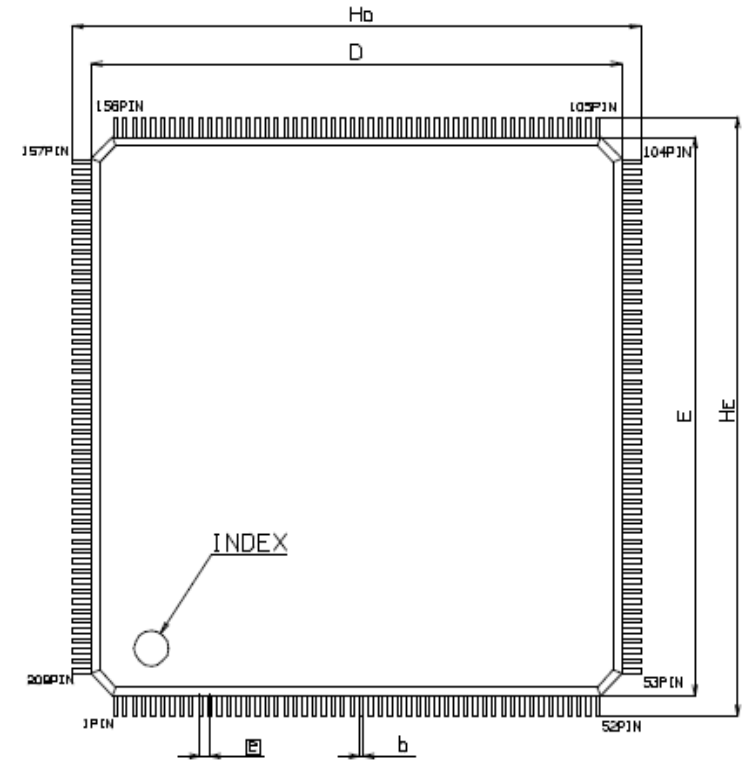


Figure 16-9: Main Window (Top), PIP1 (Middle), PIP2 (Bottom) Display Example 2

Table 16-9: Main Window (Top), PIP1 (Middle), PIP2 (Bottom) Display Example 2 Settings

REG[0202h] bit 0	Main Window Display Enable	1: on
REG[0202h] bit 1	PIP1 Window Display Enable	1: on
REG[0202h] bit 2	PIP2 Window Display Enable	1: on
REG[0202h] bit 4	Main Display Mode Select	0: Main1
REG[0202h] bit 5	Main Layer Mode Select	0: Main on PIP
REG[0202h] bit 6	PIP Layer Mode Select	0: PIP1 on PIP2
REG[0204h] bit 1	PIP1 Transparency Enable	0: off
REG[0204h] bit 2	PIP2 Transparency Enable	0: off
REG[0204h] bit 7	Alpha Blend Mode Select	1: PIP1 and PIP2
REG[0204h] bit 8	Alpha Blend Key Color1 Enable	1
REG[0204h] bit 9	Alpha Blend Key Color2 Enable	1
REG[0204h] bit 10	Alpha Blend Key Color3 Enable	1
REG[0204h] bit 11	Alpha Blend Key Color4 Enable	1
REG[0206h] bit 15-0	Back Ground Color	-
REG[0208h] bit 3-0	Alpha Blend1 Ratio	2h: 25%
REG[0208h] bit 7-4	Alpha Blend2 Ratio	4h: 50%
REG[0208h] bit 11-8	Alpha Blend3 Ratio	6h: 75%
REG[0208h] bit 15-12	Alpha Blend4 Ratio	8h: 100%
REG[020Ch] bit 15-0	PIP1 Transparency Key Color	-
REG[020Eh] bit 15-0	PIP2 Transparency Key Color	-
REG[0210h] bit 15-0	Alpha Blend1 Key Color	
REG[0212h] bit 15-0	Alpha Blend2 Key Color	
REG[0214h] bit 15-0	Alpha Blend3 Key Color	
REG[0216h] bit 15-0	Alpha Blend4 Key Color	

17 Mechanical Data



Symbol	Dimension in Millimeters		
	Min	Nom	Max
E	-	28	-
D	-	28	-
Amax	-	-	1.7
A1	-	0.1	-
A2	-	1.4	-
e	-	0.5	-
b	0.17	-	0.27
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.75
L1	-	1	-
HE	-	30	-
HD	-	30	-
y	-	-	0.08

1 = 1mm

Figure 17-1: S1D13L02 QFP22 208-Pin Package

18 Change Record

XB0A-A-001-01 Revision 1.1 - Issued: March 12, 2018

- updated Sales and Technical Support Section
- updated some formatting

XB0A-A-001-01 Revision 1.0 - Issued: February 13, 2014

- initial release

19 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html