EPSON
EXCEED YOUR VISION

S1D13U11 Display Controller

Hardware Functional Specification

Document Number: X96A-A-001-01.7

SEIKO EPSON CORPORATION

Rev. 1.7

NOTICE

Table of Contents

Chapter 1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13U11 External SDRAM LCD Controller. Included in this document are timing diagrams. AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at vdc.epson.com.

We appreciate your comments on our documentation. Please contact us via email at vdc-documentation@ea.epson.com.

1.2 Overview Description

The S1D13U11 is a low power color LCD Controller with support for up to 128M-bit external SDRAM memory. The S1D13U11 supports a USB2.0 High-speed device port interface while providing high performance bandwidth into the external display memory allowing for fast screen updates. The S1D13U11 also provides support for multiple display buffers, Picture-in-Picture, Alpha-Blend, and display rotation/mirror.

Additionally the S1D13U11 supports one I2C and two SPI serial interfaces. These can be connected to an external touch screen controller and serial flash memory. The S1D13U11 is an excellent solution to connect between the host CPU and LCD panel via the USB port.

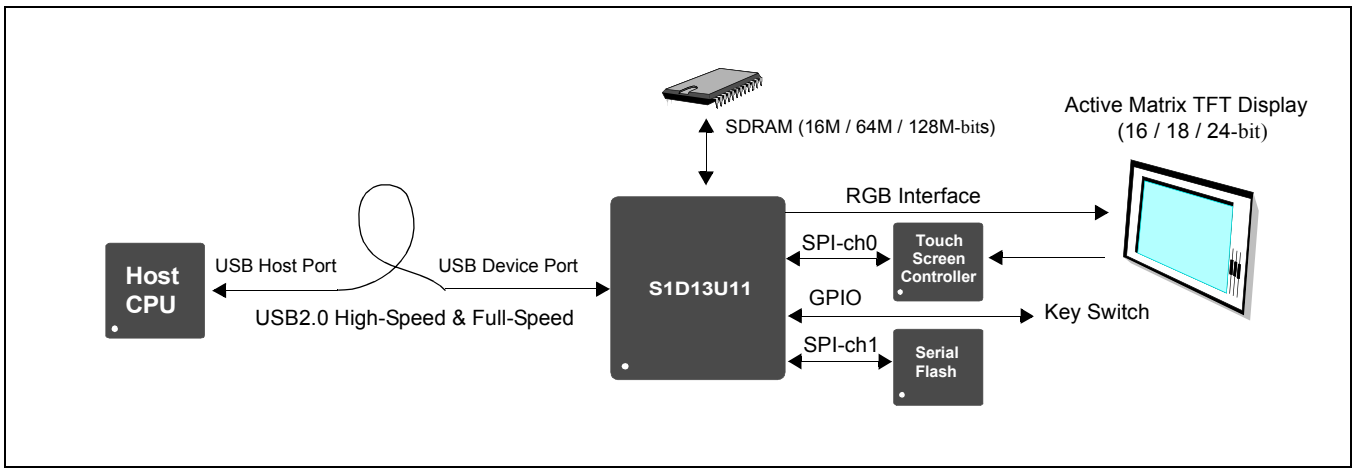


Figure 1-1: System Overview

Chapter 2 Features

2.1 Frame Buffer

- Single External 16M-bit, 64M-bit or 128M-bit SDRAM memory support (16-bit bus interface)
- Maximum 96MHz SDRAM clock

2.2 Host CPU Interface

- USB2.0 device port (1-port)
  - HS mode (480Mbps) and FS mode (12Mbps) transfer support
  - Embedded FS/HS termination (no need for external components)
  - VBUS 5V direct interface (requires protection components)
- Endpoint
  - Endpoint 0: For system control (Control transfer)
  - Endpoint 1: For command write (Bulk OUT transfer)
  - Endpoint 2: For status read (Bulk IN transfer)
  - Endpoint 3: For event read (Interrupt IN transfer)
  - Endpoint 4: For display data write (Bulk OUT transfer)
- USB protocol control
  - Embedded protocol sequencer and 96K-byte work SRAM
  - Device class: Vendor class
  - Need the download configuration data into work SRAM from USB port or external serial flash

2.3 Input Data Formats

- RGB 8:8:8 (3-byte/pixel or 4-byte/pixel)
- RGB 5:6:5 (2-byte/pixel)

2.4 Display Mode

- 24bpp (RGB 8:8:8) or 16bpp (RGB 5:6:5) color depths selectable

2.5 Display Support

- Active matrix 16/18/24-bit TFT interface
- Maximum 800 x 600 display support (QVGA/WQVGA/HVGA/VGA/WVGA/SVGA)

2.6 Display Features

- Display Window
  The display window is defined by the size of the LCD display. Complete or partial updates to the display window are done through the Write Window. The write window size and start position are specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical). All window coordinates are referenced to top left corner of the display window (even when rotation or mirror are enabled no host side translation is required).
  All display updates can have independent mirror, rotation, and transparency settings.
- Picture-in-Picture (PIP) display
  Up to two PIP windows are supported. When enabled the PIP windows are displayed over the Main window. The PIP windows sizes and start positions are specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical). Image scrolling can be performed by changing the start address of a PIP window. The PIP windows do not support a transparent overlay function.
- Alpha-Blend
  Alpha-blending allows two images to be blended to create a new image which can then be displayed using a PIP window. The Alpha-blend image size is specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical). The processing speed of Alpha-blend function varies depending on the image size. Optionally, a single input image can be processed.
- Copy / Fill
  A new window can be copied by Alpha-Blending the image of a window. A new window can be filled by Alpha-Blending a programmed color.
- Mirror / Rotation
  Mirror and 180° counter-clockwise hardware rotation functions are available for image data writes. All windows can have independent rotation and mirror settings. No additional programming is necessary when enabling these modes.
- Double buffer display
  Double buffering is available to prevent image tearing during streaming input.
- Multi Buffer
  Multi buffering allows the active display window to be switched between a maximum of 16 buffers. The number of buffers depends on the external SDRAM size and the desired size of the write buffers. Multi buffering allows a simple animation display to be performed by switching the buffers.
- Pixel doubling display
  Display Doubling is available for the main window.
- Virtual display
  Virtual display is available to show the display data which is larger than LCD panel size. The display data can be easily scrolled to the left/right/top/bottom directions.
- Wake-up display
  Wake-up display is available to show quickly the display data which is stored into SDRAM without host CPU support. This function is used when returning from the sleep.
- Start-up display
  Start-up display is available to show quickly the display data which is stored into serial flash without host CPU support. This function is used when starting from the reset.

- Display enhancement
  Display enhancement is available to show display data which is enhanced by the Gamma correction, Brightness correction and Contrast correction.

2.7 SPI Interface

- SPI master interface (SPI-ch0: SS0#)
  - For the external touch screen controller
  - Sequential command support
- SPI master interface (SPI-ch1-1: SS1#)
  - For the expand I/O device
  - Sequential command support
- SPI master interface (SPI-ch1-2: SS2#)
  - For the external serial flash
  - 1M-bit serial flash support for the following devices:
    Sanyo LE25FU106B
    Numonyx M25PE10
    Numonyx M25PE10A

2.8 I2C Interface

- I2C master interface
  - For the expand I/O device
  - Supported I2CCLK frequencies are 117.19kHz and 468.75kHz only

2.9 GPIO Interface

- 16-bit general purpose input / output ports (GPIOA [7:0]/GPIOB[7:0])
- Programmable on/off pull-up resistor

2.10 Key-scan Interface

- 8 x 8, 8 x 4 or 8 x 2 key matrix support (share the GPIO ports)
- Programmable scan period

2.11 Buzzer Interface

- Buzzer pulse output for beep sound
- Programmable buzzer frequency and on period

2.12 PWM Interface

- PWM pulse output for LED backlight control
- Programmable high and low pulse width

2.13 Event Notification

- Event notification for host CPU via USB endpoint 3
  - INT0 input interrupt (SPI interface interrupt)
  - INT1 input interrupt (Wake-up key input)
  - GPIO input interrupt (Edge or level detection)
  - Key-scan data changing
  - SPI sequential command data receive
  - LCD interface interrupt (Alpha-Blend complete)

2.14 Clock Source

- 12MHz or 24MHz crystal oscillator (frequency is selected by CNF0 pin)
- Internal programmable PLL (maximum 96MHz)
- SDRAM clock (66MHz ~ 96MHz)
  - Spread spectrum clock available (maximum 78MHz)
- LCD pixel clock (maximum 48MHz)
  - 1/2, 1/3, 1/4, 1/6 or 1/8 the clock frequency can be selected for the SDRAM clock
  - Spread spectrum clock available
- General purpose clock output (FOUT)
  - 1/1, 1/2 or 1/4 the clock frequency for crystal oscillator

2.15 Miscellaneous

Reset

- Hardware reset
- USB bus reset
- Software command reset

Power Save

- Sleep (Crystal: stop, USB port: stop, LCD interface: stop)
  - Entry factor: USB suspend or VBUS low input
  - Exit factor: USB resume, USB bus reset, INT0/INT1 input or VBUS high input
- USB remote wake-up support

Package

- QFP20-144 pin

Chapter 3 System Diagrams

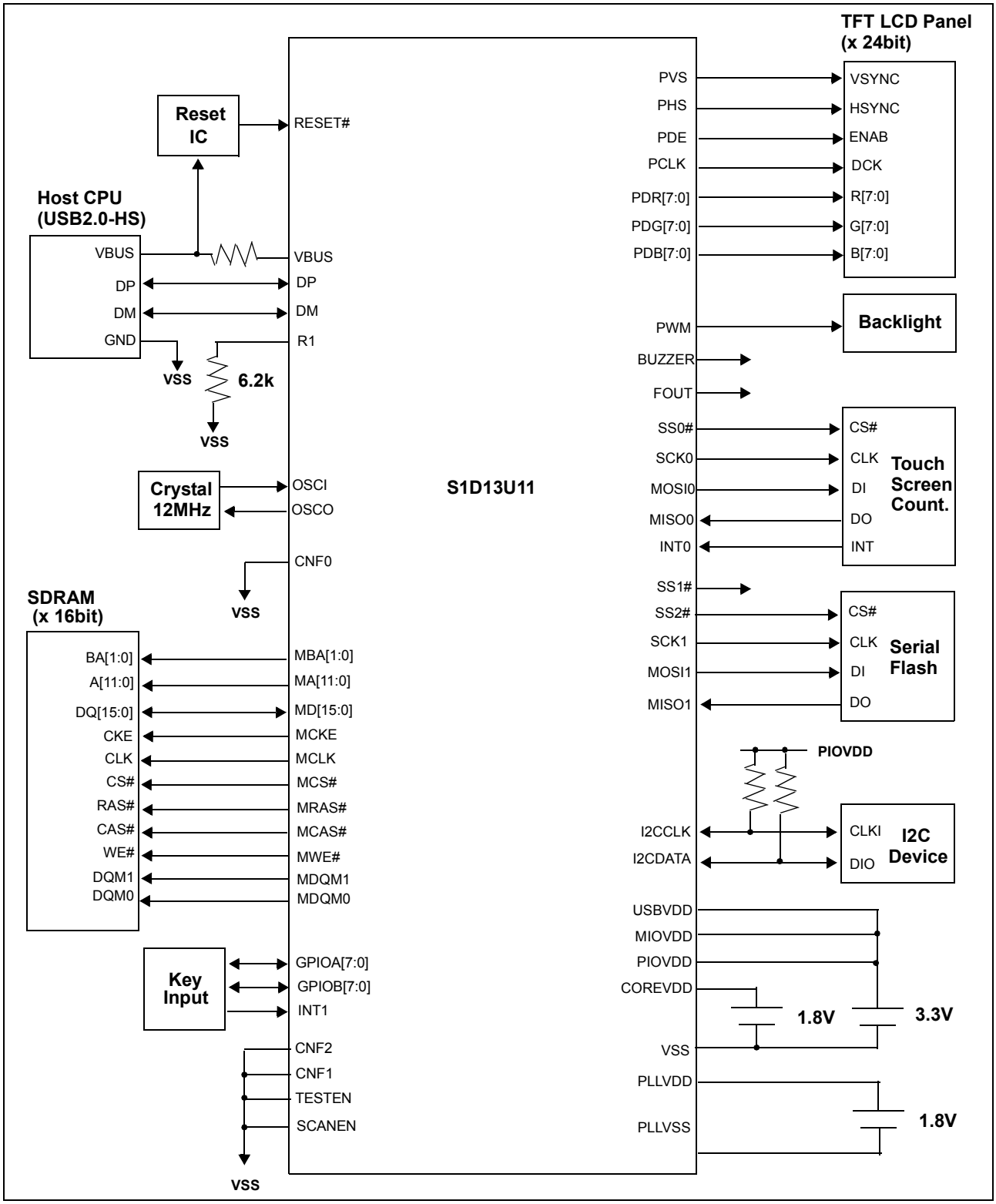


Figure 3-1: System Diagram Example

Chapter 4 Block Diagram

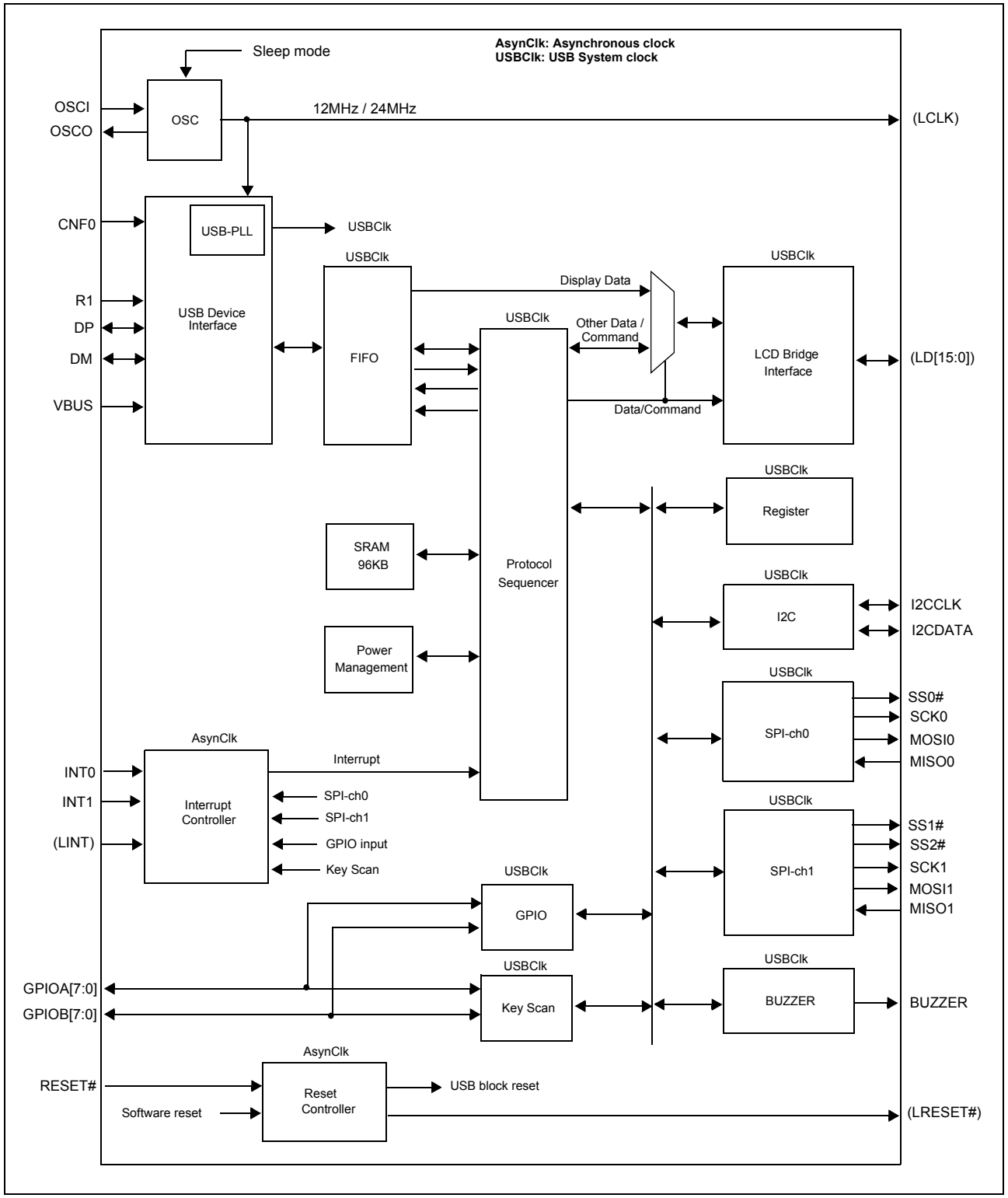


Figure 4-1: Block Diagram 1 of 2 (USB Interface Block)

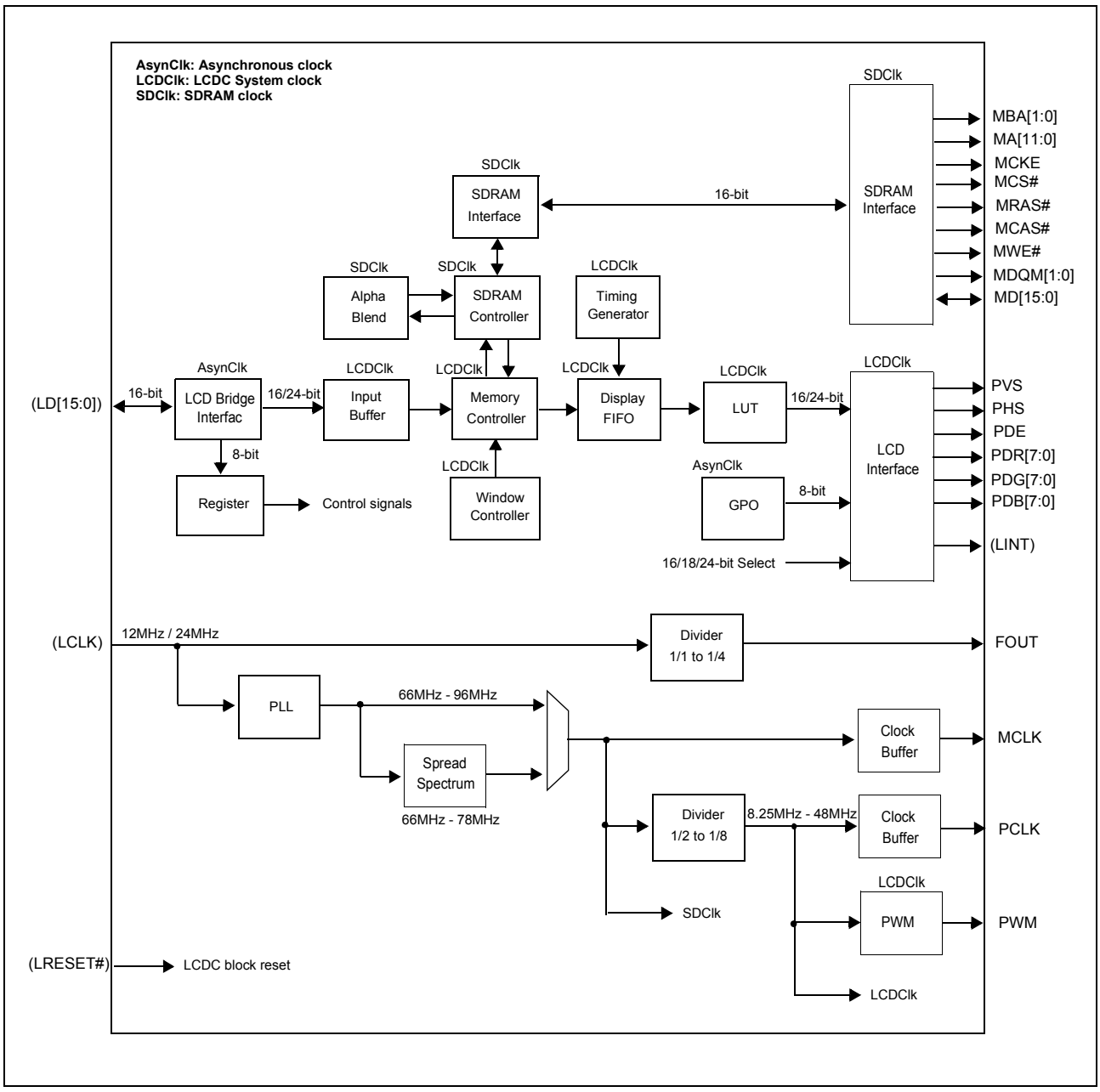


Figure 4-2: Block Diagram 2 of 2 (LCD Interface Block)

Chapter 5 Pinout Diagram

5.1 Pin-Out

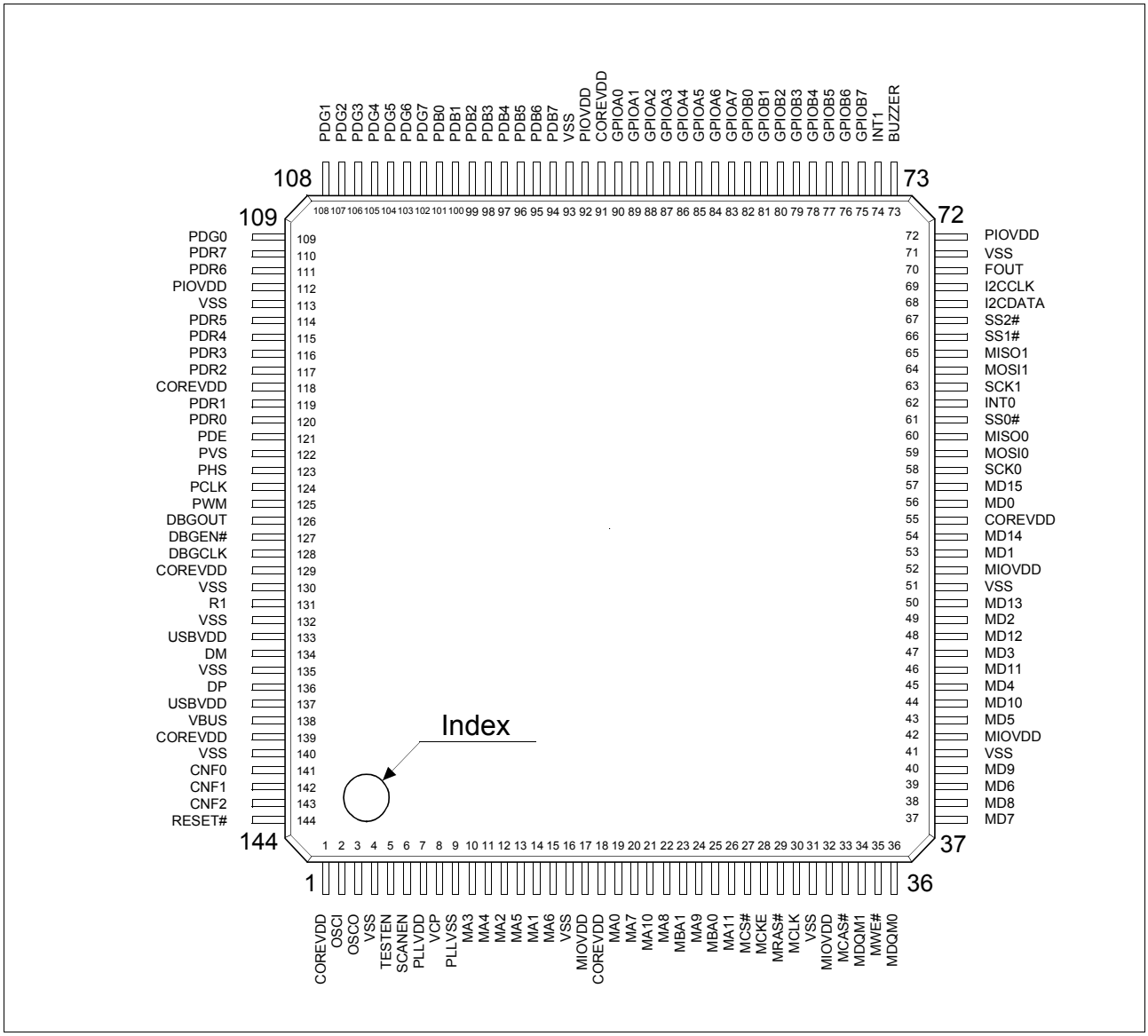


Figure 5-1: S1D13U11 Pinout (Top View)

5.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# / Power Save Status

H	=	High level output
L	=	Low level output
Z	=	High Impedance
X	=	Don't care
1	=	Pull-up resistor on
0	=	Pull-down resistor on

Table 5-1: Cell Descriptions

Item	Description
HI	H System LVCMOS Input Buffer
HID	H System LVCMOS Input Buffer with pull-down resistor
HIDC	H System LVCMOS Input Buffer with pull-down control resistor
HSI	H System LVCMOS Schmitt Input Buffer
HSID	H System LVCMOS Schmitt Input Buffer with pull-down resistor
HTID	H System LVCMOS Tolerant Input Buffer with pull-down resistor
HO1	H System LVCMOS Output Buffer Type 1 (+/- 2mA)
HO1T	H System LVCMOS Output Buffer Type 1 (+/- 2mA) with tri-state
HO2	H System LVCMOS Output Buffer Type 2 (+/- 3mA)
HO2S	H System LVCMOS Output Buffer Type 2S (+/- 3mA or +/- 4mA)
HO3	H System LVCMOS Output Buffer Type 3(+/- 5mA)
HSB1	H System LVCMOS Bidirectional Buffer Type 1 (+/- 2mA)
HSB1U	H System LVCMOS Bidirectional Buffer Type 1 (+/- 2mA) with pull-up resistor
HSB1UC	H System LVCMOS Bidirectional Buffer Type 1 (+/- 2mA) with pull-up control resistor
HSB1D	H System LVCMOS Bidirectional Buffer Type 1 (+/- 2mA) with pull-down resistor
HSB1DC	H System LVCMOS Bidirectional Buffer Type 1 (+/- 2mA) with pull-down control resistor
HB2	H System LVCMOS Bidirectional Buffer Type 2 (+/- 3mA)
HB2D	H System LVCMOS Bidirectional Buffer Type 2(+/- 3mA) with pull-down resistor
HBA	H System Analog Input / Output
LBA	L System Analog Input / Output

Note

1. H System is PIOVDD, MIOVDD and USBVDD
2. L System is COREVDD and PLLVDD

5.2.1 Host CPU Interface

Table 5-2: Host CPU Interface Pin Descriptions

Pin Name	Type	PIN #	Cell	IO Voltage	RESET #State	Power Save Status	Description
DP	IO	136	HBA	USB	Z	Z	This bidirectional pin is the USB data line +.
DM	IO	134	HBA	USB	Z	Z	This bidirectional pin is the USB data line -.
VBUS	I	138	HTID	USB	0	0	This input pin is the USB device detection. 5V level can be input.
R1	I	131	HBA	USB	—	—	This input pin is the reference current input for USB. A 6.2kΩ +/- 1% resistor should be connected between this pin and VSS.
OSCI	I	2	LBA	CORE	—	—	This input pin is the crystal oscillator input.
OSCO	O	3	LBA	CORE	—	—	This output pin is the crystal oscillator output.
CNF0	I	141	HSI	USB	Z	Z	This input pin is the configuration input of crystal oscillator.
CNF[2:1]	I	143, 142	HSI	USB	Z	Z	These two pins are reserved.
RESET#	I	144	HSI	USB	Z	Z	This input pin is the Reset input. Active low input to set all internal registers to the default state and to force all signals to their inactive states. This input uses a Schmitt input and delay line for noise reduction.

5.2.2 LCD Interface

Table 5-3: LCD Interface Pin Descriptions

Pin Name	Type	PIN #	Cell	IO Voltage	RESET #State	Power Save Status	Description
PDR[7:3]	O	110, 111, 114, 115, 116	HO2S	PIO	L	L	These output pins are R[7:3] of the panel data output.
PDR[2] / GPO[6]	O	117	HO2S	PIO	L	L / Keep	This output pin has multiple functions. • R[2] of the panel data output in 18/24-bit mode. • GPO[6] output in 16-bit mode. See Table 5-8: “LCD Interface Pin Mapping,” on page 30
PDR[1:0] / GPO[1:0]	O	119, 120	HO2S	PIO	L	L / Keep	These output pins have multiple functions. • R[1:0] of the panel data output in 24-bit mode. • GPO[1:0] output in 16/18-bit mode. See Table 5-8: “LCD Interface Pin Mapping,” on page 30
PDG[7:2]	O	102, 103, 104, 105, 106, 107	HO2S	PIO	L	L	These output pins are G[7:2] of the panel data output.

Table 5-3: LCD Interface Pin Descriptions (Continued)

Pin Name	Type	PIN #	Cell	IO Voltage	RESET #State	Power Save Status	Description
PDG[1:0] / GPO[3:2]	O	108, 109	HO2S	PIO	L	L / Keep	These output pins have multiple functions. • G[1:0] of the panel data output in 24-bit mode. • GPO[3:2] output in 16/18-bit mode. See Table 5-8: "LCD Interface Pin Mapping," on page 30
PDB[7:3]	O	94, 95, 96, 97, 98	HO2S	PIO	L	L	These output pins are B[7:3] of the panel data output.
PDB[2] / GPO[7]	O	99	HO2S	PIO	L	L / Keep	This output pin has multiple functions. • B[2] of the panel data output at 18/24-bit mode. • GPO[7] output at 16-bit mode. See Table 5-8: "LCD Interface Pin Mapping," on page 30
PDB[1:0] / GPO[5:4]	O	100, 101	HO2S	PIO	L	L / Keep	These output pins have multiple functions. • B[1:0] of the panel data output at 24-bit mode. • GPO[5:4] output at 16/18-bit mode. See Table 5-8: "LCD Interface Pin Mapping," on page 30
PVS	O	122	HO2S	PIO	L	L	This output pin is the vertical sync pulse output.
PHS	O	123	HO2S	PIO	L	L	This output pin is the horizontal sync pulse output.
PCLK	O	124	HO2S	PIO	L	L	This output pin is the pixel clock output.
PDE	O	121	HO2S	PIO	L	L	This output pin is the pixel data enable output.
PWM	O	125	HO1	PIO	L	keep	This output pin is the PWM output for the LCD backlight control.

5.2.3 SDRAM Interface

Table 5-4: SDRAM Interface Pin Descriptions

Pin Name	Type	PIN #	Cell	IO Voltage	RESET #State	Power Save Status	Description
MD[15:0]	I/O	57, 54, 50, 48, 46, 44, 40, 38, 37, 39, 43, 45, 47, 49, 53, 56	HB2D	MIO	0	Keep	These pins are the data bus for the SDRAM. These pins have internal pull-down resistors.
MBA[1:0]	O	23, 25	HO2	MIO	L	Keep	These pins are the bank address output for the SDRAM.
MA[11:0]	O	26, 21, 24, 22, 20, 15, 13, 11, 10, 12, 14, 19	HO2	MIO	L	Keep	These pins are the address output for the SDRAM.
MCS#	O	27	HO2	MIO	H	Keep	This pin is the chip select for the SDRAM.
MRAS#	O	29	HO2	MIO	H	Keep	This pin is the row address strobe output of the SDRAM.
MCAS#	O	33	HO2	MIO	H	Keep	This pin is the column address strobe output of the SDRAM.
MWE#	O	35	HO2	MIO	H	Keep	This pin is the write enable output of the SDRAM.
MDQM1	O	34	HO2	MIO	L	Keep	This pin is the DQMH output of the SDRAM.
MDQM0	O	36	HO2	MIO	L	Keep	This pin is the DQML output of the SDRAM.
MCLK	O	30	HO3	MIO	X	Keep	This pin is the clock output of the SDRAM.
MCKE	O	28	HO2	MIO	H	Keep	This pin is the CKE output of the SDRAM.

5.2.4 I/O Interface

Table 5-5: I/O Interface Pin Descriptions

Pin Name	Type	PIN #	Cell	IO Voltage	RESET# State	Power Save Status	Description
GPIOA[7:0]	IO	83, 84, 85, 86, 87, 88, 89, 90	HSB1UC	PIO	1 *note	Keep	These bidirectional pins have multiple functions. • General purpose input / output ports in GPIO mode. • Key-scan input in key-scan mode.
GPIOB[7:4]	IO	75, 76, 77, 78	HSB1UC	PIO	1 *note	Keep	These bidirectional pins have multiple functions. • General purpose input / output ports in GPIO mode. • Key-scan output in 8x8 key-scan mode.
GPIOB[3:2]	IO	79, 80	HSB1UC	PIO	1 *note	Keep	These bidirectional pins have multiple functions. • General purpose input / output ports in GPIO mode. • Key-scan output in 8x8/8x4 key-scan mode.
GPIOB[1:0]	IO	81, 82	HSB1UC	PIO	1 *note	Keep	These bidirectional pins have multiple functions. • General purpose input / output ports in GPIO mode. • Key-scan output in key-scan mode.
I2CCLK	IO	69	HSB1	PIO	Z	Z	This pin is the I2C clock input. This pin requires an external pull-up resistor.
I2CDATA	IO	68	HSB1	PIO	Z	Z	This pin is the I2C data input/output. This pin requires an external pull-up resistor.
SS0#	IO	61	HSB1U	PIO	1	H	This pin is the slave select output of SPI-ch0.
SCK0	IO	58	HSB1D	PIO	0	L	This pin is the serial clock output of SPI-ch0.
MOSI0	O	59	HO1	PIO	L	L	This pin is the serial data output of SPI-ch0.
MISO0	I	60	HID	PIO	0	0	This pin is the serial data input of SPI-ch0.
SS1#	O	66	HO1	PIO	L	H	This pin is the slave select output of SPI-ch1-1.
SS2#	O	67	HO1	PIO	L	H	This pin is the slave select output of SPI-ch1-2.
SCK1	O	63	HO1	PIO	L	L	This pin is the serial clock output of SPI-ch1.
MOSI1	O	64	HO1	PIO	L	L	This pin is the serial data output of SPI-ch1.
MISO1	I	65	HID	PIO	0	0	This pin is the serial data input of SPI-ch1.
INT0	I	62	HSI	PIO	Z	Z	This pin is the interrupt input of SPI interface.
INT1	I	74	HSI	PIO	Z	Z	This pin is the interrupt input of Wake-up key.
BUZZER	O	73	HO1	PIO	L	L	This pin is the buzzer output.
FOUT	O	70	HO1	PIO	L	L	This pin is the clock output.

Note

After a hardware reset of S1D13U11, GPIO pins are set as inputs with pull-up resistors enabled. However, about 4ms after RESET# signal goes high, the pull-up resistors will be disabled by the embedded protocol sequencer, resulting in GPIO pins being in Hi-Z state. There is no influence on operation or reliability of the S1D13U11 itself. If GPIO is used as a general purpose I/O pin and in case it controls external device, it goes to Hi-Z for a certain period. It is completely avoidable by using external pull-up resistor to GPIO pins.

5.2.5 Miscellaneous

Table 5-6: Miscellaneous Pin Descriptions

Pin Name	Type	PIN #	Cell	IO Voltage	RESET# State	Power Save Status	Description
VCP	IO	8	LBA	PLL	—	—	This pin is for production test only and should be left unconnected for normal operation.
TESTEN	I	5	HSID	USB	0	0	Test Enable input used for production test only. This pin must be connected directly to GND for normal operation.
SCANEN	I	6	HSID	USB	0	0	Scan Enable input used for production test only. This pin must be connected directly to GND for normal operation.
DBGOUT	O	126	HO1	PIO	L	L	This pin is for production test only and should be left unconnected for normal operation.
DBGEN#	IO	127	HSB1U	PIO	1	1	This pin is for production test only and should be left unconnected for normal operation.
DBGCLK	O	128	HO1	PIO	H	H	This pin is for production test only and should be left unconnected for normal operation.

5.2.6 Power

Table 5-7: Power Pin Descriptions

Pin Name	Type	Pin #	Cell	Descriptions
COREVDD	P	1, 18, 55, 91, 118, 129, 139	P	Core power supply, all pins must be connected.
PLLVDD	P	7	P	PLL power supply
USBVDD	P	133, 137	P	USB power supply, all pins must be connected.
PIOVDD	P	72, 92, 112	P	Peripheral I/O power supply, all pins must be connected.
MIOVDD	P	17, 32, 42, 52	P	Memory I/O power supply, all pins must be connected.
VSS	P	4, 16, 31, 41, 51, 71, 93, 113, 130, 132, 135, 140	P	GND, all pins must be connected.
PLLVSS	P	9	P	PLL GND

5.3 Pin Structure

5.3.1 Input Pin

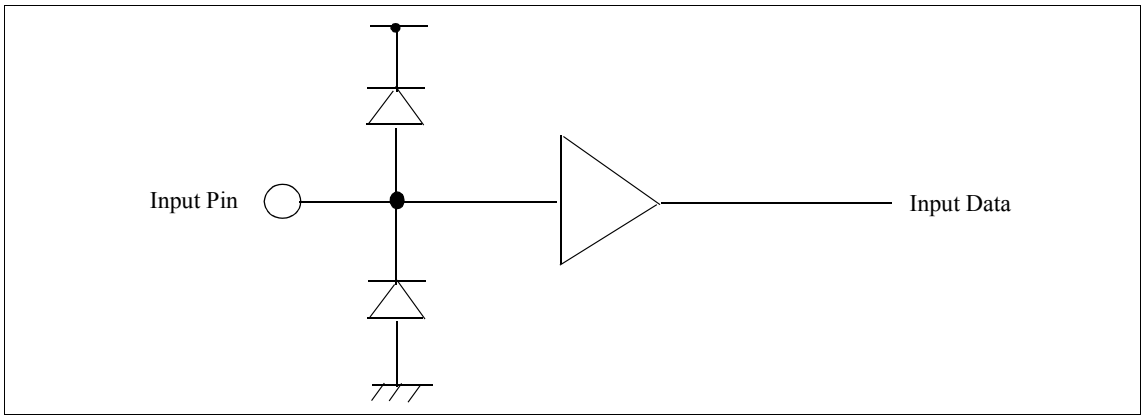


Figure 5-2: Input Pin (HI, HSI) Structure

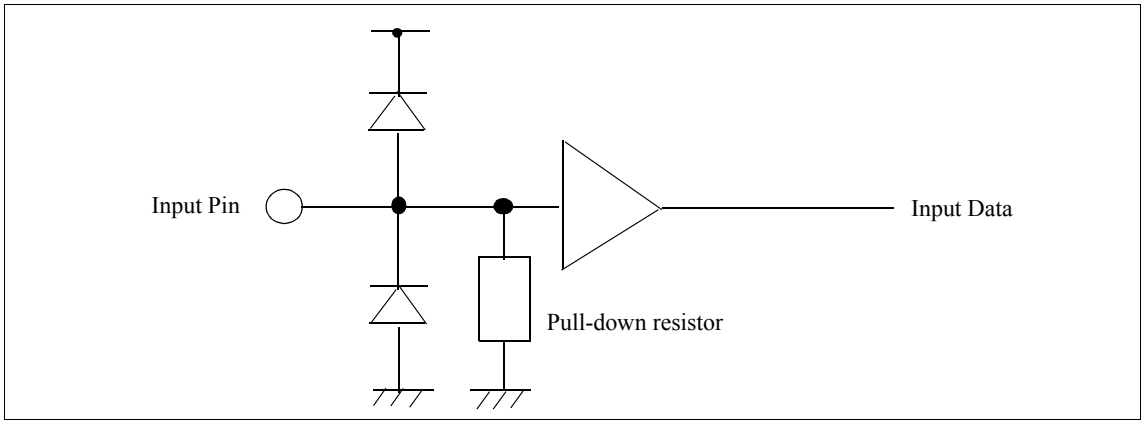


Figure 5-3: Input Pin (HID, HSID) Structure

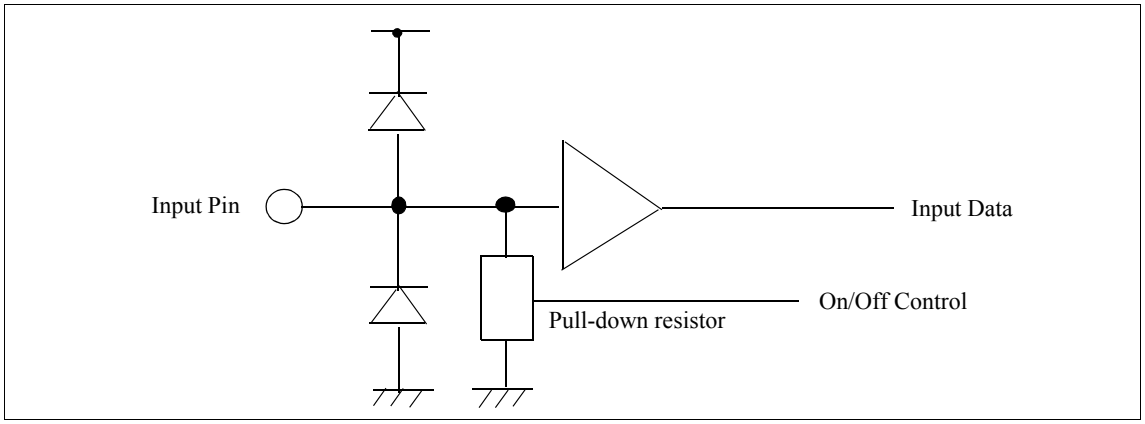


Figure 5-4: Input Pin (HIDC, HSIDC) Structure

5.3.2 Output Pin

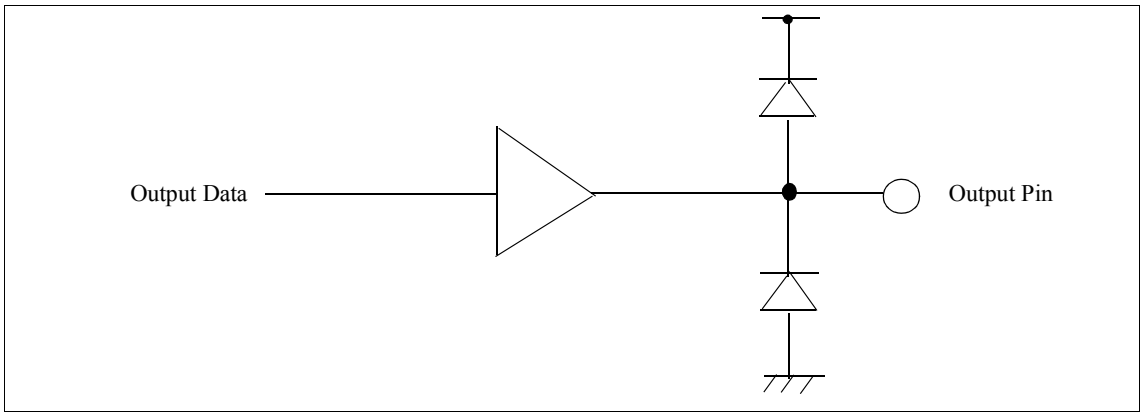


Figure 5-5: Output Pin (HO1, HO2, HO3) Structure

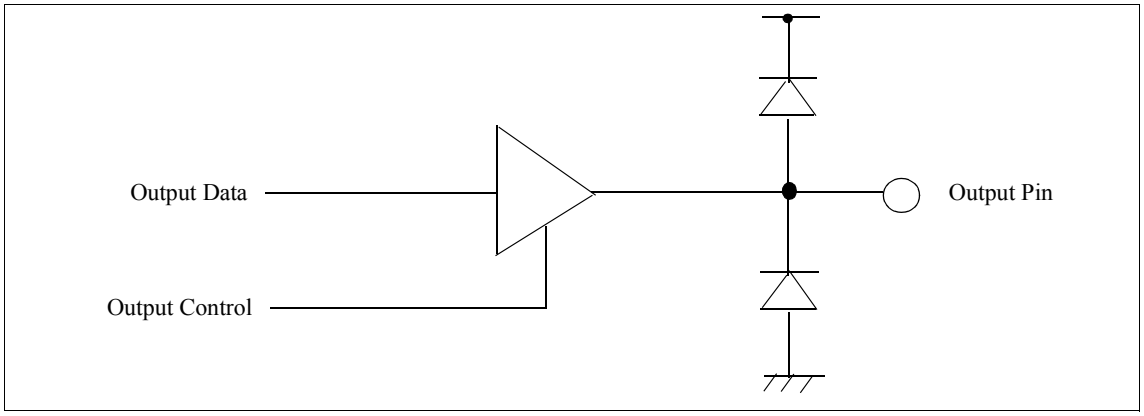


Figure 5-6: Output Pin (HO1T) Structure

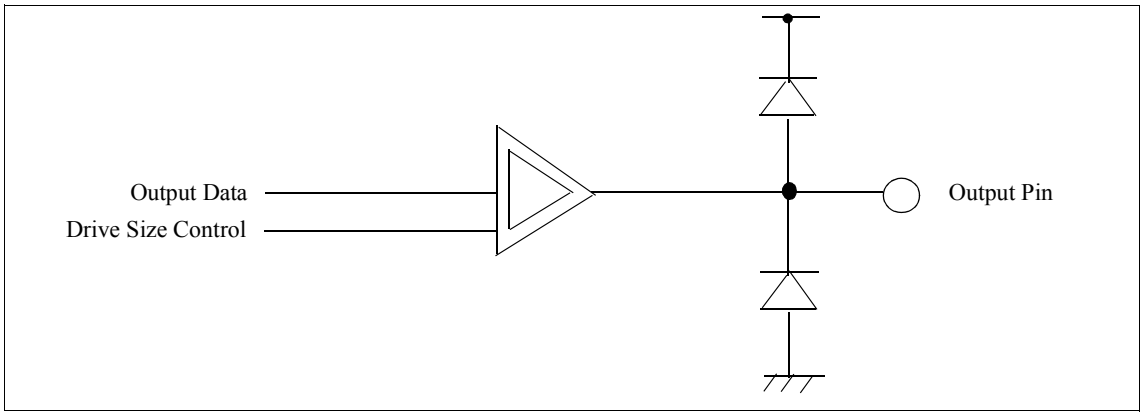


Figure 5-7: Output Pin (HO2S) Structure

5.3.3 Bi-directional Pin

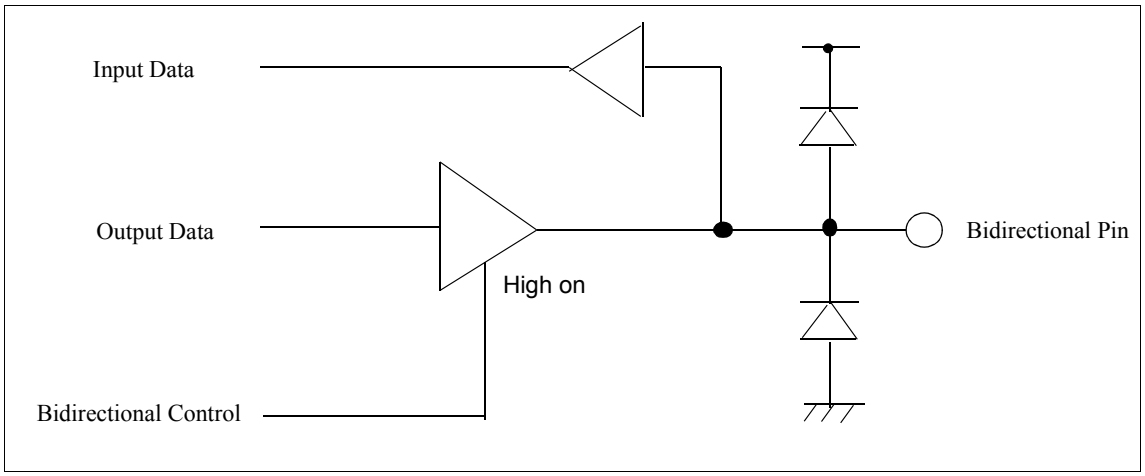


Figure 5-8: Bi-directional (HB2, HSB1) Structure

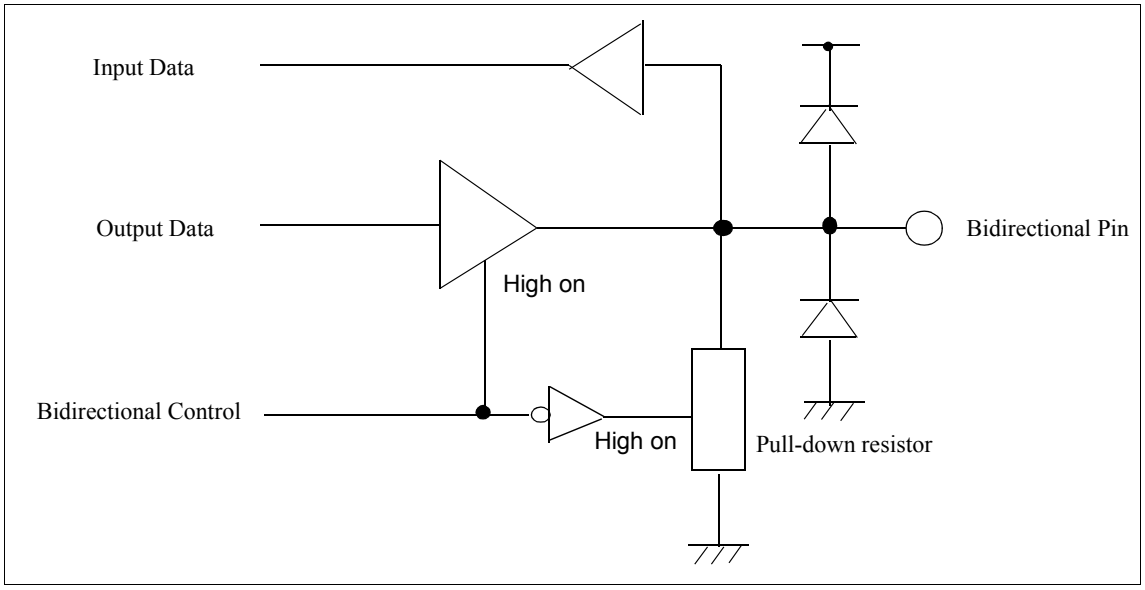


Figure 5-9: Bi-directional (HB2D, HSB1D) Structure

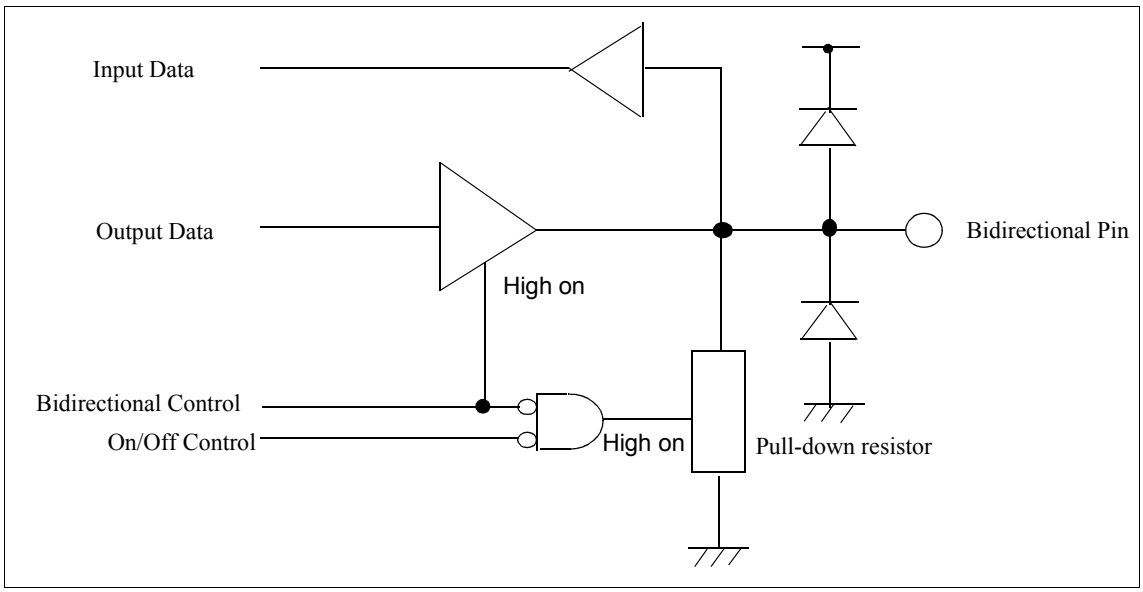


Figure 5-10: Bi-directional (HSB1DC) Structure

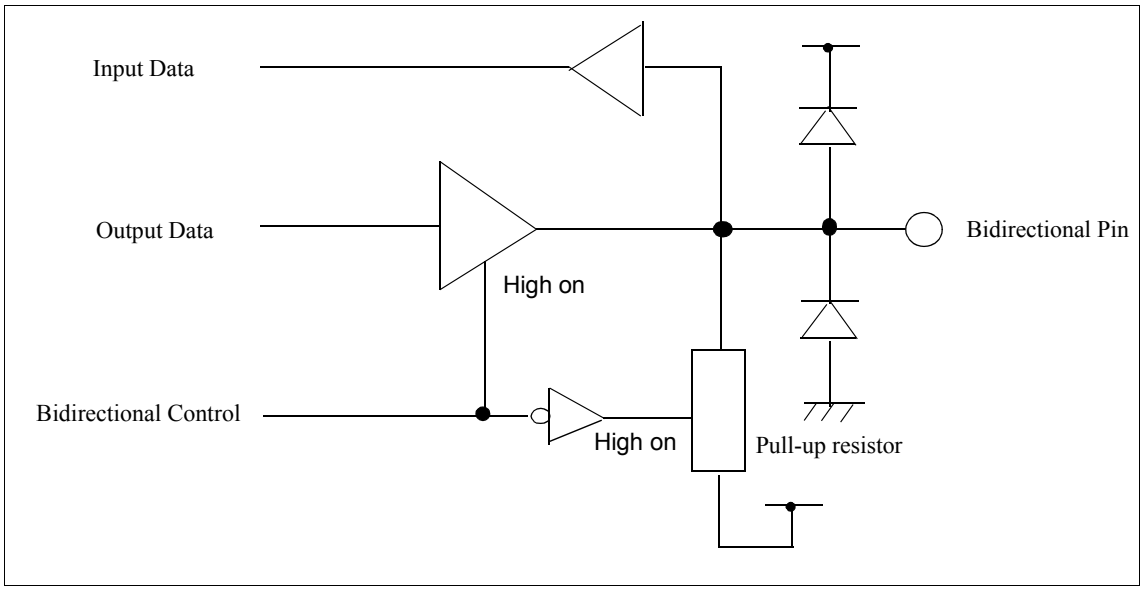


Figure 5-11: Bi-directional (HSB1U) Structure

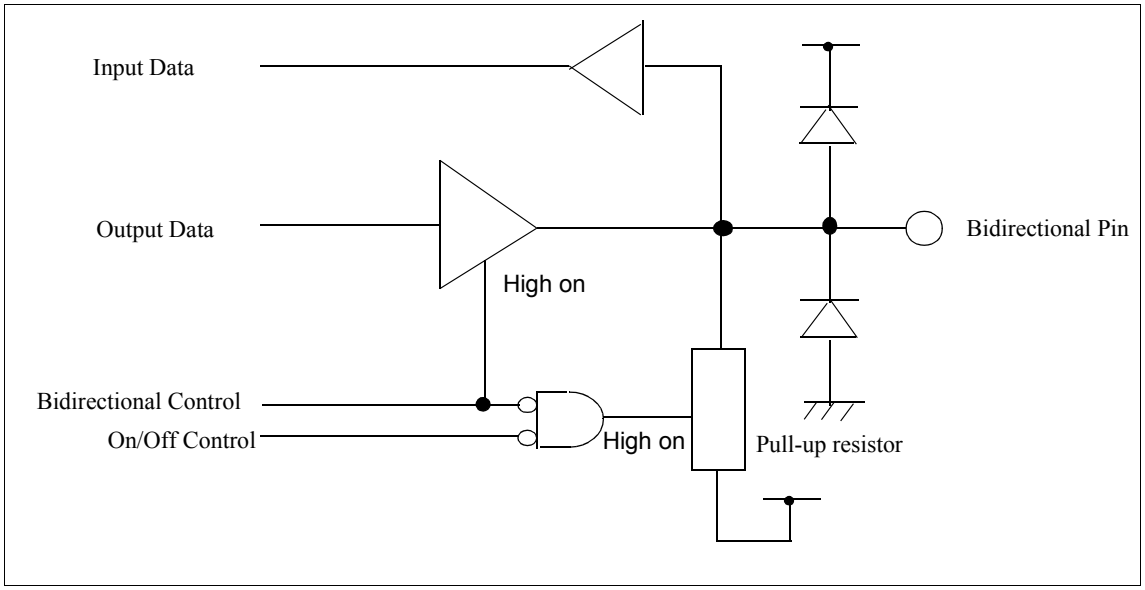


Figure 5-12: Bi-directional (HSB1UC) Structure

5.4 Configuration Options

These pins are used for power-up configuration and must be connected directly to USBVDD or VSS. The state of CNF[2:0] must not be changed during normal operation.

Pins	Power-on State	
	1 (connected to USBVDD)	0 (connected to VSS)
CNF0	24MHz crystal oscillator	12MHz crystal oscillator
CNF1	Reserved. Must be set to 0	
CNF2	Reserved. Must be set to 0	

5.5 LCD Interface Pin Mapping

Table 5-8: LCD Interface Pin Mapping

Pin Name	TFT Interface		
Color depth	16bpp	18bpp	24bpp
PVS	PVS		
PHS	PHS		
PCLK	PCLK		
PDE	PDE		
PDR0	GPO0		R0
PDR1	GPO1		R1
PDR2	GPO6	R2	
PDR3	R3		
PDR4	R4		
PDR5	R5		
PDR6	R6		
PDR7	R7		
PDG0	GPO2		G0
PDG1	GPO3		G1
PDG2	G2		
PDG3	G3		
PDG4	G4		
PDG5	G5		
PDG6	G6		
PDG7	G7		
PDB0	GPO4		B0
PDB1	GPO5		B1
PDB2	GPO7	B2	
PDB3	B3		
PDB4	B4		
PDB5	B5		
PDB6	B6		
PDB7	B7		

Chapter 6 D.C. Characteristics

6.1 Absolute Maximum Rating

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
CORE V_{DD}	Core Supply Voltage	VSS - 0.3 ~ 2.5	V
PLL V_{DD}	PLL Supply Voltage	VSS - 0.3 ~ 2.5	V
USB V_{DD}	USB Supply Voltage	COREVDD ~ 4.0	V
PIO V_{DD}	Peripheral IO Supply Voltage	COREVDD ~ 4.0	V
MIO V_{DD}	Memory IO Supply Voltage	COREVDD ~ 4.0	V
V_{IN1}	Input Signal Voltage	VSS - 0.3 ~ IOVDD + 0.5	V
V_{IN2}	Input Signal Voltage (DP, DM)	VSS - 0.3 ~ USBVDD + 0.5	V
V_{IN3}	Input Signal Voltage (VBUS)	VSS - 0.3 ~ 6.0	V
V_{IN4}	Input Signal Voltage (OSCI)	VSS - 0.3 ~ COREVDD + 0.5	V
V_{OUT1}	Output Signal Voltage	VSS - 0.3 ~ IOVDD + 0.5	V
V_{OUT2}	Output Signal Voltage (DP, DM)	VSS - 0.3 ~ USBVDD + 0.5	V
I_{OUT}	Output Signal Current	±10	mA
T_{STG}	Storage Temperature	-65 to +150	°C

6.2 Recommended Operating Conditions

Table 6-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
CORE V_{DD}	Core Supply Voltage	VSS = 0 V	1.65	1.80	1.95	V
PLL V_{DD}	PLL Supply Voltage	VSS = 0 V	1.65	1.80	1.95	V
USB V_{DD}	USB Supply Voltage	VSS = 0 V	3.00	3.30	3.60	V
PIO V_{DD}	Peripheral IO Supply Voltage	VSS = 0 V	3.00	3.30	3.60	V
MIO V_{DD}	Memory IO Supply Voltage	VSS = 0 V	3.00	3.30	3.60	V
V_{IN1}	Input Voltage	—	VSS	—	IOVDD	V
V_{IN2}	Input Voltage (DP, DM)	—	VSS	—	USBVDD	V
V_{IN3}	Input Voltage (VBUS)	—	VSS	—	5.50	V
T_{OPR}	Operating Temperature	—	-40	+25	+85	°C

6.3 Electrical Characteristics

The following conditions are for VSS = 0V, TOPR = -40 to +85°C.

Table 6-3: Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
V_{OH1}	High Level Output Voltage (1)	IOV_{DD} = min I_{OH1} = -2mA, TYPE1 pin	IOVDD - 0.40	—	IOVDD	V
V_{OH2}	High Level Output Voltage (2)	IOV_{DD} = min I_{OH2} = -3mA, TYPE2 pin	IOVDD - 0.40	—	IOVDD	V
V_{OH3}	High Level Output Voltage (3)	IOV_{DD} = min I_{OH2} = -4mA, TYPE2S pin	IOVDD - 0.40	—	IOVDD	V
V_{OH4}	High Level Output Voltage (4)	IOV_{DD} = min I_{OH2} = -5mA, TYPE3 pin	IOVDD - 0.40	—	IOVDD	V
V_{OH5}	High Level Output Voltage (5)	$USBV_{DD}$ = min USB-FS, DP, DM	2.8	—	—	V
V_{OH6}	High Level Output Voltage (6)	$USBV_{DD}$ = min USB-HS, DP, DM	360	—	—	mV
V_{OL1}	Low Level Output Voltage (1)	IOVDD = min I_{OL1} = 2mA, TYPE1 pin	VSS	—	0.40	V
V_{OL2}	Low Level Output Voltage (2)	IOVD = min I_{OL2} = 3mA, TYPE2 pin	VSS	—	0.40	V
V_{OL3}	Low Level Output Voltage (3)	IOVD = min I_{OL2} = 4mA, TYPE2S pin	VSS	—	0.40	V
V_{OL4}	Low Level Output Voltage (4)	IOVD = min I_{OL2} = 5mA, TYPE3 pin	VSS	—	0.40	V
V_{OL5}	Low Level Output Voltage (5)	IOVD = min USB-FS, DP, DM	—	—	0.30	V
V_{OL6}	Low Level Output Voltage (6)	IOVD = min USB-HS, DP, DM	—	—	10	mV
V_{IH}	High Level Input Voltage	CMOS Input	2.20	—	—	V
V_{IL}	Low Level Output Voltage	CMOS Input	—	—	0.80	V
V_{T+1}	Positive Trigger Voltage (1)	CMOS Schmitt	1.40	—	2.70	V
V_{T+2}	Positive Trigger Voltage (2)	USB-FS, DP, DM	1.10	—	1.80	V
V_{T+3}	Positive Trigger Voltage (3)	VBUS	1.86	—	2.85	V
V_{T-1}	Negative Trigger Voltage (1)	CMOS Schmitt	0.60	—	1.80	V
V_{T-2}	Negative Trigger Voltage (2)	USB-FS, DP, DM	1.00	—	1.50	V
V_{T-3}	Negative Trigger Voltage (3)	VBUS	1.48	—	2.23	V
V_{H1}	Hysteresis Voltage (1)	CMOS Schmitt	0.30	—	—	V
V_{H2}	Hysteresis Voltage (2)	USB-FS, DP, DM	0.10	—	—	V
V_{H3}	Hysteresis Voltage (3)	VBUS	0.31	—	—	V
V_{DS}	Deferential Input Voltage	V_I = 0.8V to 2.5V USB-FS, DP, DM	—	—	0.20	V
R_{PU}	Pull-Up Resistance	V_I = VSS	50	100	240	kΩ

Table 6-3: Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{PD1}	Pull-Down Resistance (1)	V_I = VDD	50	100	240	kΩ
R_{PD2}	Pull-Down Resistance (2)	V_I = 5V, VBUS	110	125	150	kΩ
C_{IO1}	Pin Capacitance (1)	f = 1MHz, VDD = 0V DP, DM	—	—	11	pF
C_{IO2}	Pin Capacitance (2)	f = 1MHz, VDD = 0V Other pins	—	—	8	pF

6.4 Power Consumption

Table 6-4: Power Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{CORE+PLL}$	Active Current (note 1)	COREVDD / PLLVDD Current	—	50	80	mA
I_{USB}		USBVDD Current	—	7	—	mA
I_{IO}		IOVDD Current	—	25	—	mA
$I_{CORE+PLL}$	Sleep Current (note 2)	COREVDD / PLLVDD Current	—	10	1000	uA
I_{USB}		USBVDD Current	—	5	20	uA
I_{IO}		IOVDD Current	—	5	80	uA

1. Typ (typical) is measured values using typical display settings of 800x480, 16bpp, MCLK = 96MHz, PCLK = 32MHz, USB data transfer and the Typ conditions listed in Table 6-2: “Recommended Operating Conditions,” on page 31.
   Max (maximum) is the estimated values using worst case display settings of 800x600, 24bpp, MCLK = 96MHz, PCLK = 48MHz, USB data transfer and on the Max conditions listed in Table 6-2: “Recommended Operating Conditions,” on page 31.
2. The values listed for this parameter do not include the pull-up/pull-down current of each input pin, or the pull-up current of the DP pin (approximately 200uA).

Chapter 7 A.C. Characteristics

Conditions: USBVDD = IOVDD = 3.3V ± 0.3V, COREVDD = PLLVDD = 1.8V ± 0.15V, T_A = -40°C ~ 85°C
T_{rise} and T_{fall} for all inputs except Schmitt must be ≤50ns (10% ~ 90%)
T_{rise} and T_{fall} for all Schmitt must be$_l$ ≤5ms (10% ~ 90%)
C_L = 15pF (SDRAM Interface)
C_L = 30pF (LCD Interface)
C_L = 30pF (Other Interface)

7.1 Clock Timing

7.1.1 Crystal Oscillator Clock

Table 7-1: Crystal Oscillator Clock (OSCI/OSCO)

Symbol	Parameter	Min	Typ	Max	Units
f_{OSC12}	Input clock frequency (12MHz)	11.9988	12	12.0012	MHz
t_{OSC24}	Input clock frequency (24MHz)	23.9976	24	24.0024	MHz
t_{OSta}	Oscillator start time (note 1)	—	—	20	ms

1. Oscillator start time is dependant upon external components. The value given is for reference only.

7.1.2 USB Clock

Both the crystal oscillator start time and USB-PLL stable time are necessary for the USB clock to become stable. The wait time is controlled by hardware automatically, software control is unnecessary while waiting for the USB clock to become stable.

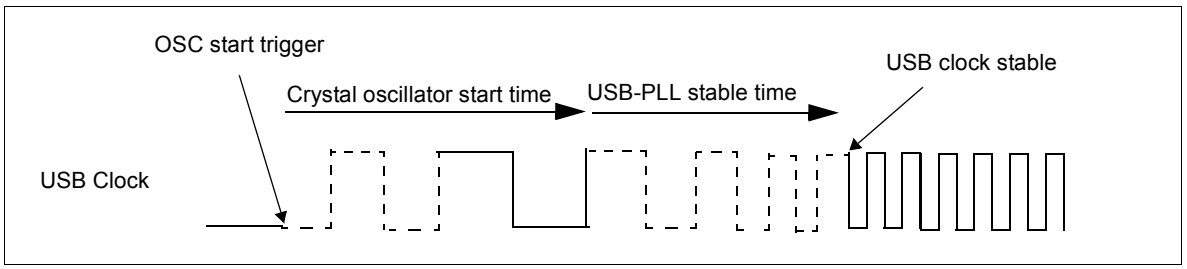


Figure 7-1: USB Clock Stable Time

Table 7-2: USB Clock Requirements

Symbol	Parameter	Min	Typ	Max	Units
f_{UCLKO}	USB clock frequency	—	60	—	MHz
t_{UPSta}	USB-PLL clock stable time	—	—	250	us

7.1.3 PLL Clock

The PLL circuit is an analog circuit that is very sensitive to noise on the power supply. If the supplied power is noisy, it may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. See Section 16.2, “Guidelines for PLL Power Layout” on page 168 for further details.

The waiting time for the PLL clock to become stable must be controlled by software.

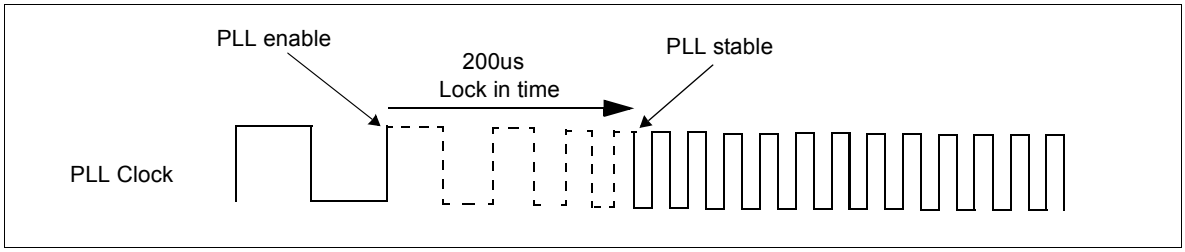


Figure 7-2: PLL Stable Time

Table 7-3: PLL Clock Requirements

Symbol	Parameter	Min	Typ	Max	Units
f_{PLLO}	PLL output clock frequency	66	—	96	MHz
$f_{PLLDuty}$	PLL output clock duty	40	—	60	%
t_{PJref}	PLL output clock period jitter	-400	—	400	ps
t_{PSta}	PLL output stable time	—	—	200	us

7.1.4 Clock Output

Table 7-4: Clock Output

Symbol	Parameter	Min	Typ	Max	Units
f_{SDCLK}	SDRAM clock (note)	66	—	96	MHz
t_{SDuty}	SDRAM clock duty	40	50	60	%
f_{LCLK}	LCD clock (note)	8.25	—	48	MHz
t_{LDuty}	LCD clock duty	45	50	55	%
f_{FCLK12}	FOUT clock 12MHz (note)	3	—	12	MHz
f_{FCLK24}	FOUT clock 24MHz (note)	6	—	24	MHz
t_{FDuty}	FOUT clock duty	45	50	55	%

Note
These values do not include the PLL jitter value and OSC input difference.

7.1.5 Spread Spectrum (SS) Clock

As Spread Spectrum modulation clock EMI decreases, the spread Spectrum modulation can be increased.

Table 7-5: Spread Spectrum Clock

Symbol	Parameter	Min	Max	Units
f_{SSCLK}	Input SS clock (note)	—	78	MHz
t_{SSW}	SS clock diffusion width (REG[10h] bits 6-4 = 000b)	-0.210	0.210	ns
	SS clock diffusion width (REG[10h] bits 6-4 = 001b)	-0.333	0.333	ns
	SS clock diffusion width (REG[10h] bits 6-4 = 010b)	-0.462	0.462	ns
	SS clock diffusion width (REG[10h] bits 6-4 = 011b)	-0.586	0.586	ns
	SS clock diffusion width (REG[10h] bits 6-4 = 100b)	-0.715	0.715	ns
	SS clock diffusion width (REG[10h] bits 6-4 = 101b)	-0.842	0.842	ns
	SS clock diffusion width (REG[10h] bits 6-4 = 110b)	-0.971	0.971	ns
	SS clock diffusion width (REG[10h] bits 6-4 = 111b)	-1.096	1.096	ns

Note
The input frequency of the SS must be up to 78MHz. SS can not be used between 84MHz to 96MHz.

7.2 Reset Timing

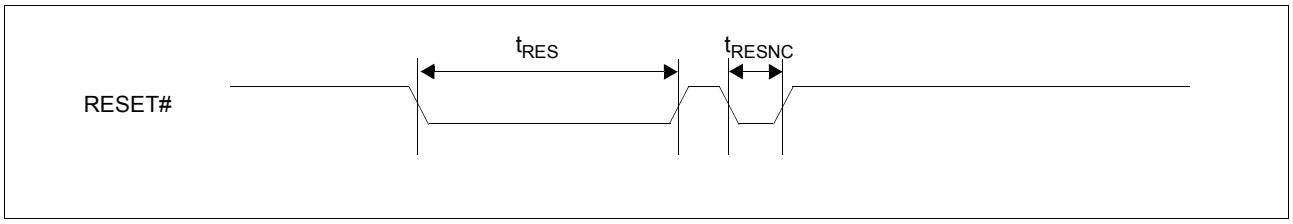


Figure 7-3: Reset Timing

Table 7-6: Reset Timing

Symbol	Parameter	Min	Max	Units
t_{RES}	Active reset pulse width	1	—	us
t_{RESNC}	Noise cancel pulse width	—	10	ns

7.3 Power Sequence Timing

7.3.1 Power-on Sequence Timing

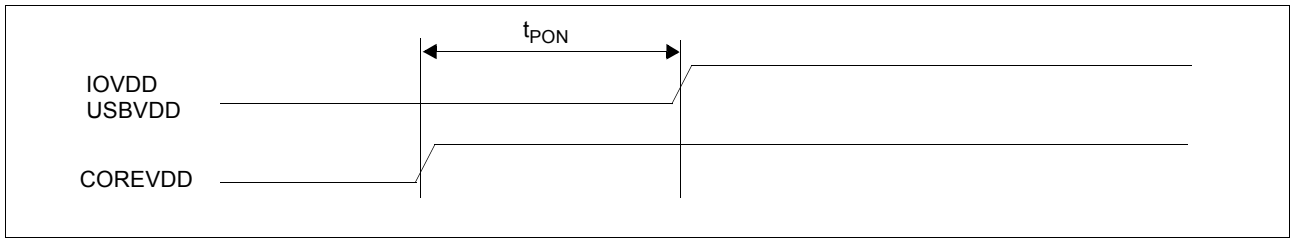


Figure 7-4: Power-on Sequence Timing

Table 7-7: Power-on Sequence Timing

Symbol	Parameter	Min	Max	Units
t_{PON}	Power-on difference time	0	—	ms

7.3.2 Power-off Sequence Timing

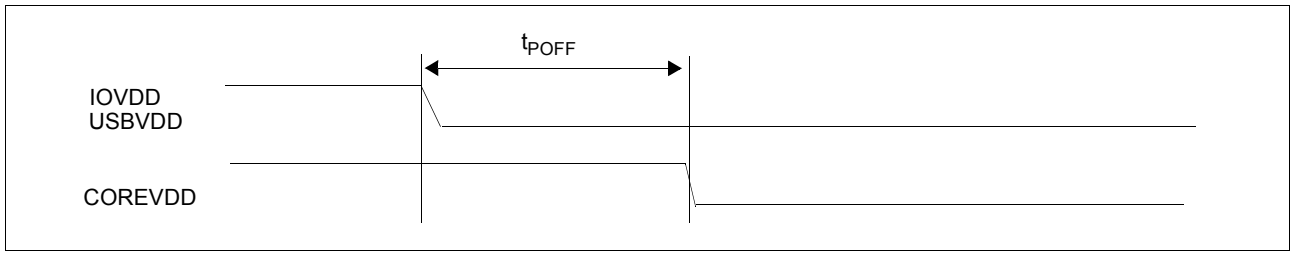


Figure 7-5: Power-off Sequence Timing

Table 7-8: Power-off Sequence Timing

Symbol	Parameter	Min	Max	Units
t_{POFF}	Power-off difference time	0	—	ms

7.4 Host CPU Interface Timing

The USB timings conform to the USB2.0 standard specification, Universal Serial Bus Specification Revision 2.0 Released April 27, 2000.

7.5 SDRAM Interface Timing

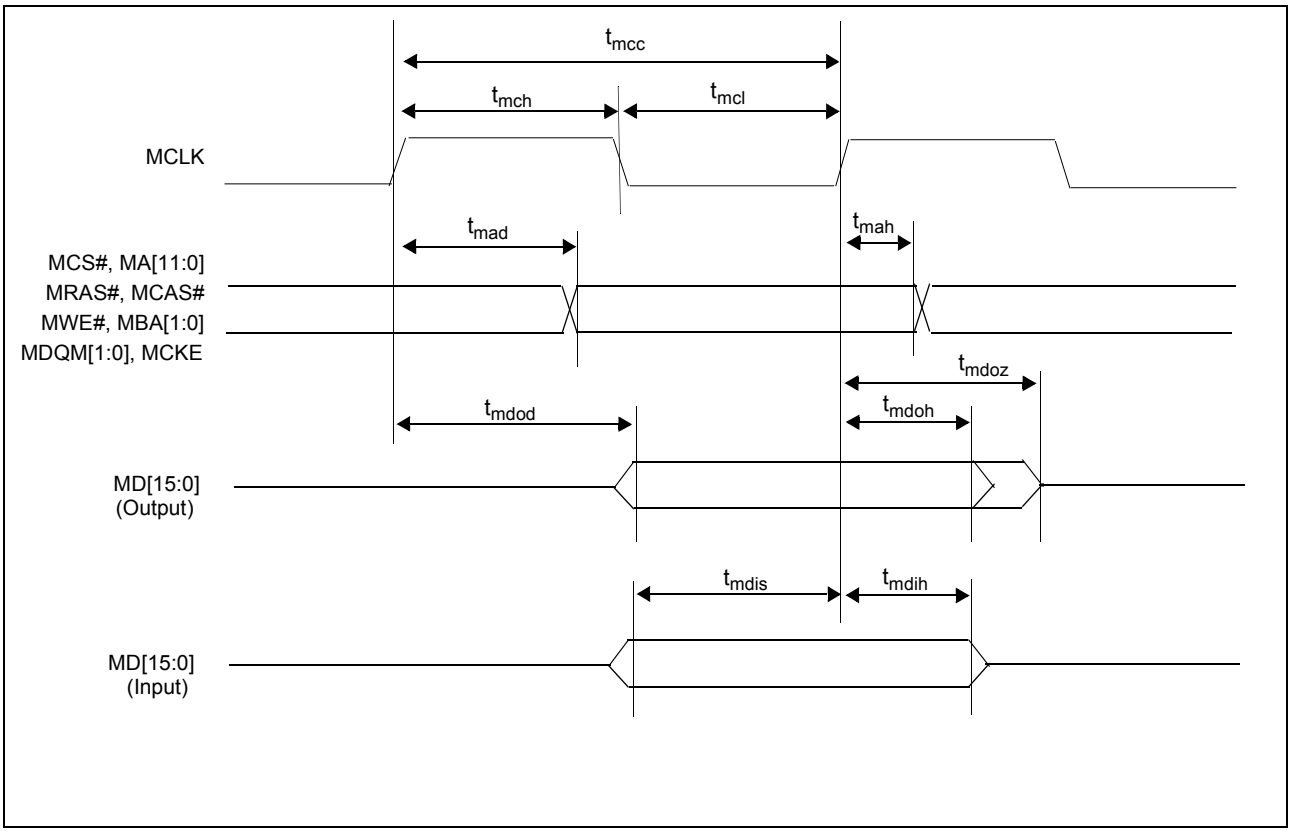


Figure 7-6: SDRAM Interface Timing

Table 7-9: SDRAM Interface Timing

Symbol	Parameter	MIN	MAX	Units
t_{mcc}	MCLK cycle period	10	—	ns
t_{mcl}	MCLK Low pulse width	3	—	ns
t_{mch}	MCLK High pulse width	3	—	ns
t_{mad}	SDRAM control signals delay time	—	7	ns
t_{mah}	SDRAM control signals hold time	1	—	ns
t_{mdod}	SDRAM data signal delay time	—	7	ns
t_{mdoh}	SDRAM data signal hold time	1	—	ns
t_{mdoz}	SDRAM data output signal Hi-Z time	—	9	ns
t_{mdis}	SDRAM data input signal setup time	3	—	ns
t_{mdih}	SDRAM data input hold time	2	—	ns

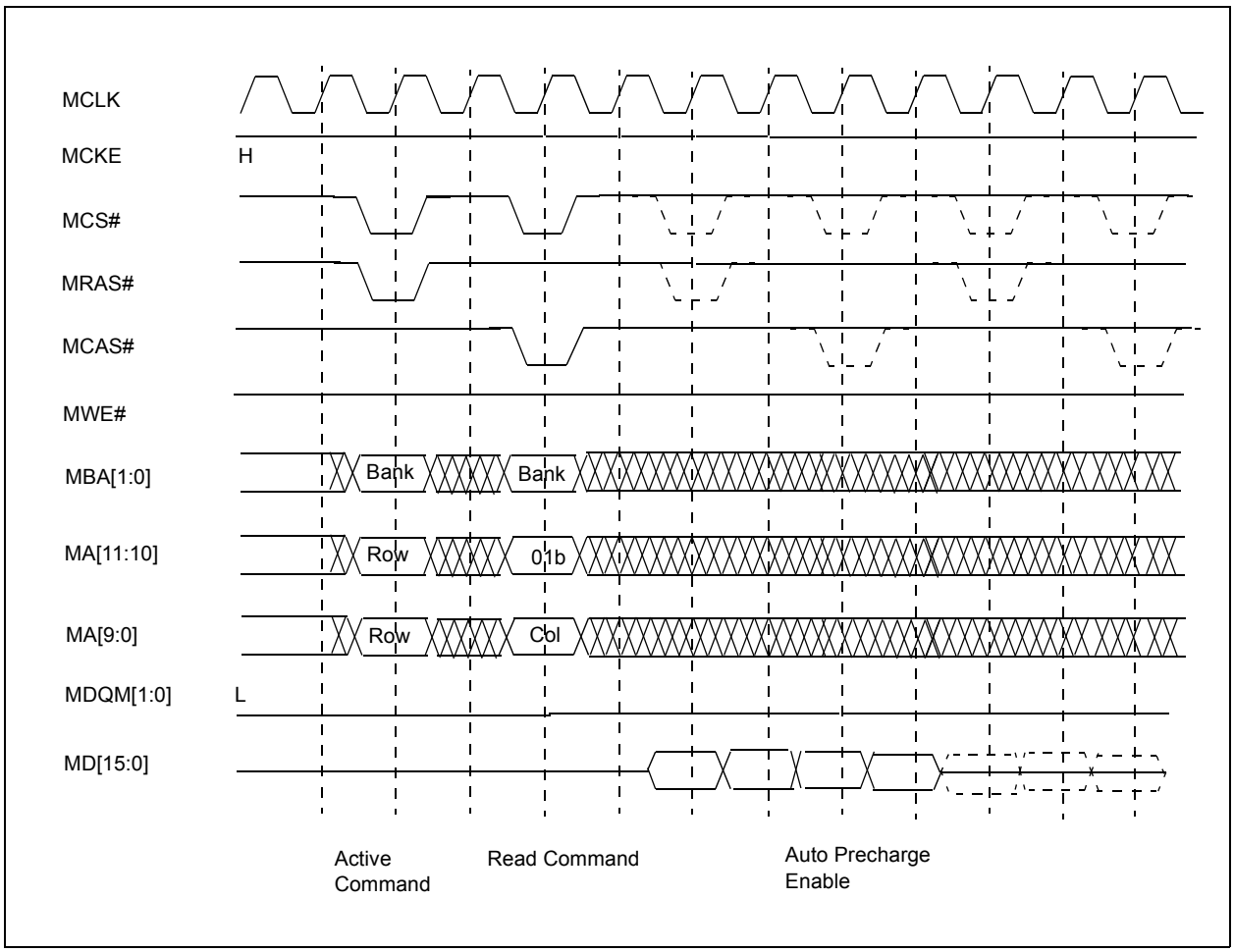


Figure 7-7: SDRAM Read Timing

Note
Burst length = 4 and CAS latency = 2 are fixed.

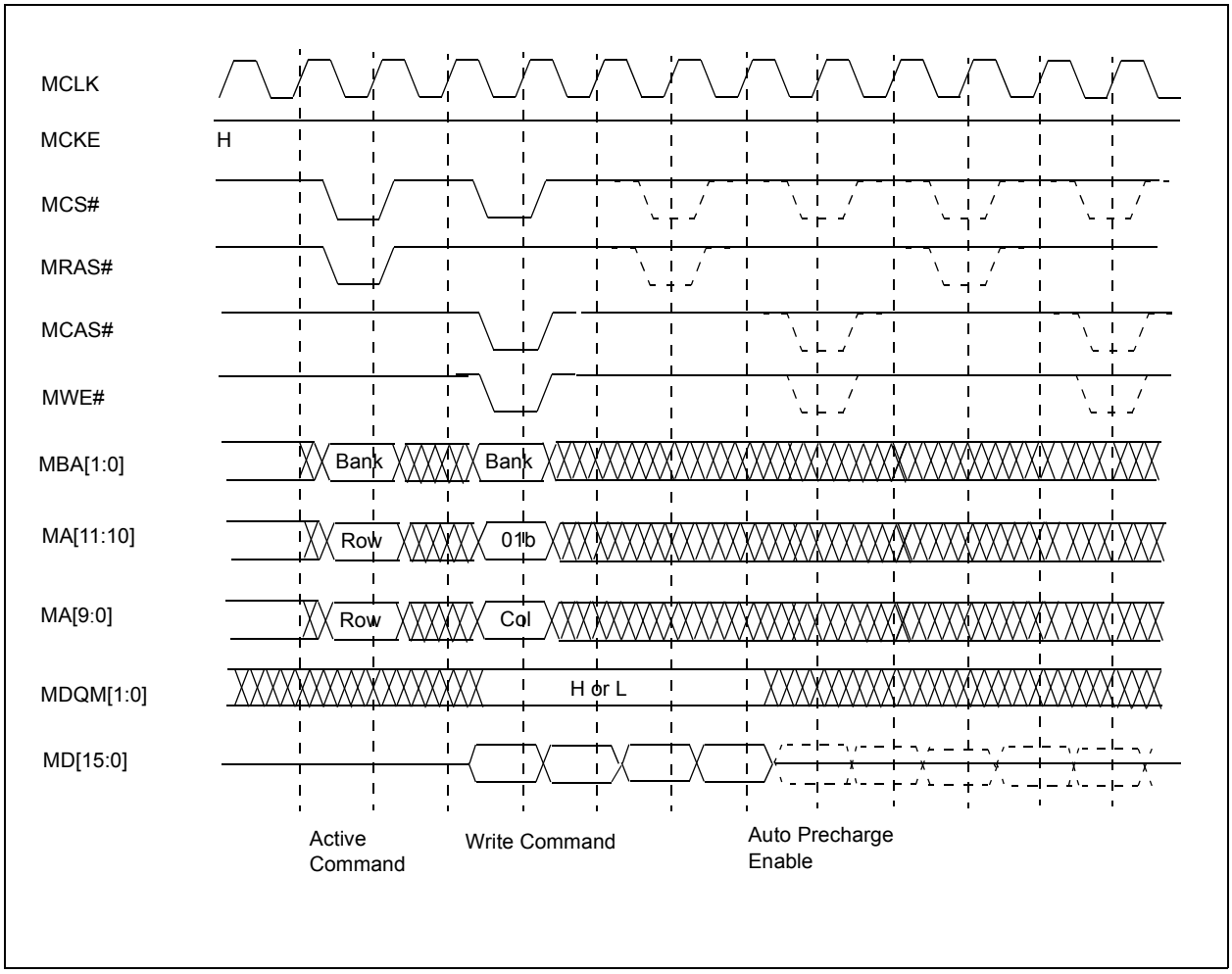


Figure 7-8: SDRAM Write Timing

Note
Burst Length = 4 is fixed.

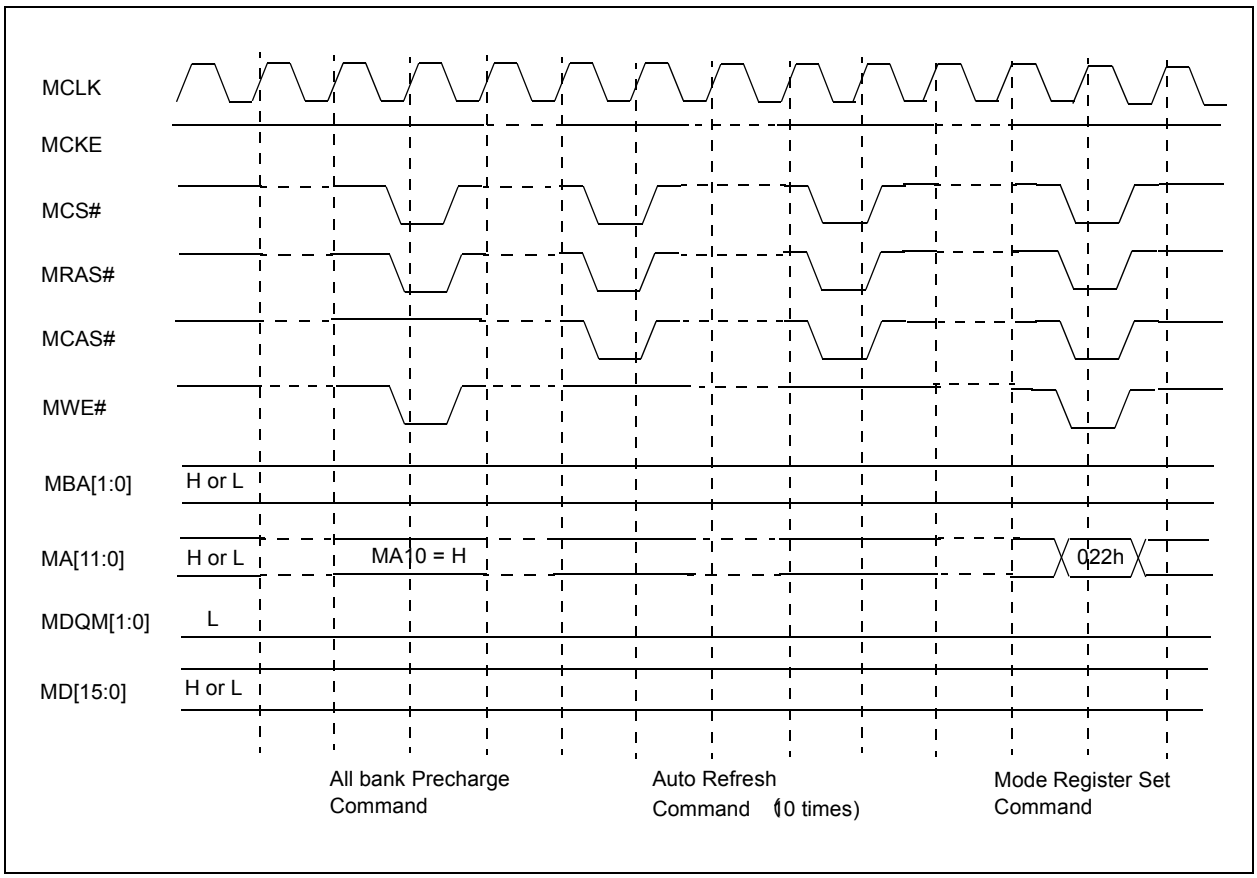


Figure 7-9: SDRAM Initialization Timing

Note
The initialization sequence is started by setting the SDRAM Initialization bit (REG[84h] bit 1 = 1). After power-on/reset, the initialization sequence can only be ran once. The initialization sequence requires 30,000 MCLK cycles.

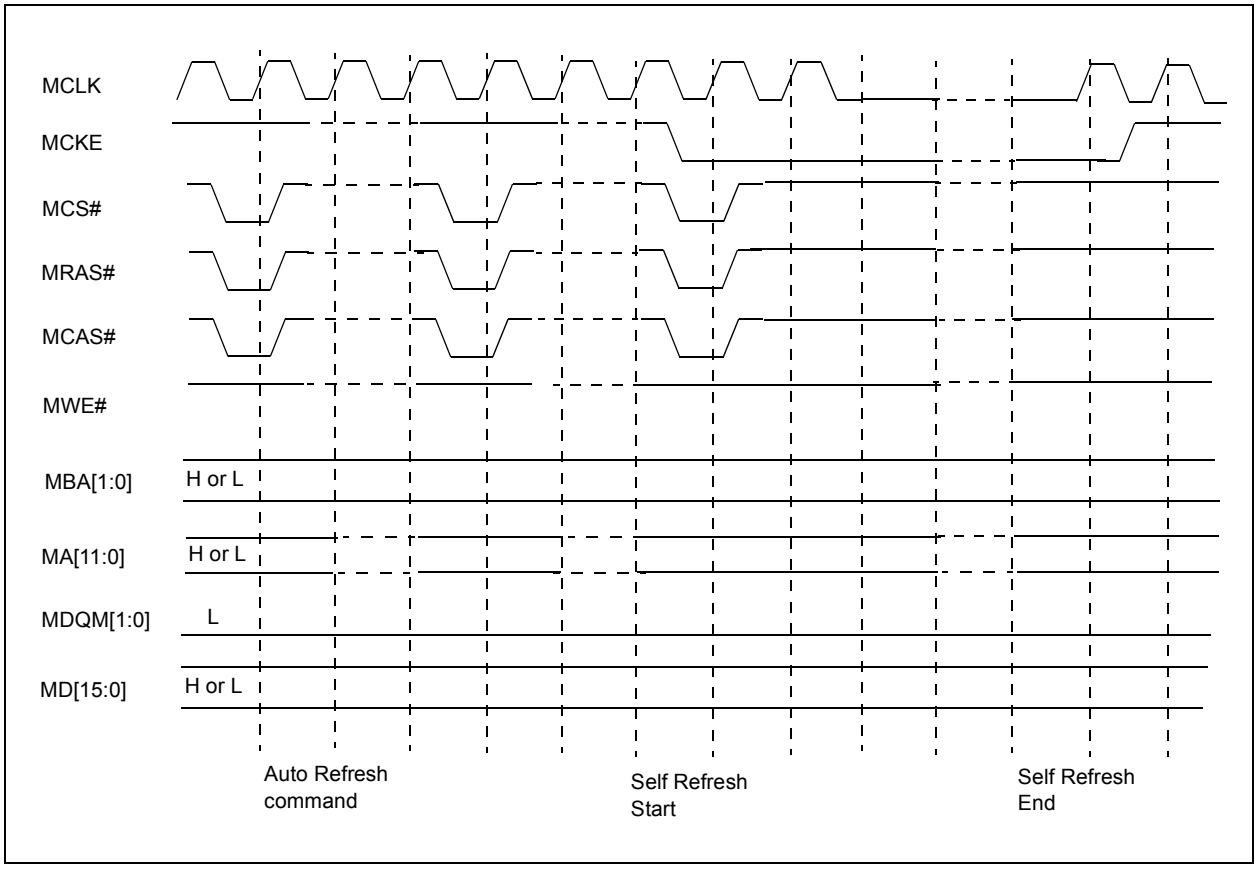


Figure 7-10: Auto Refresh / Self Refresh Timing

Note
Auto refresh time = (REG[8Eh], REG[8Ch] counter value) / f_{SDCLK}

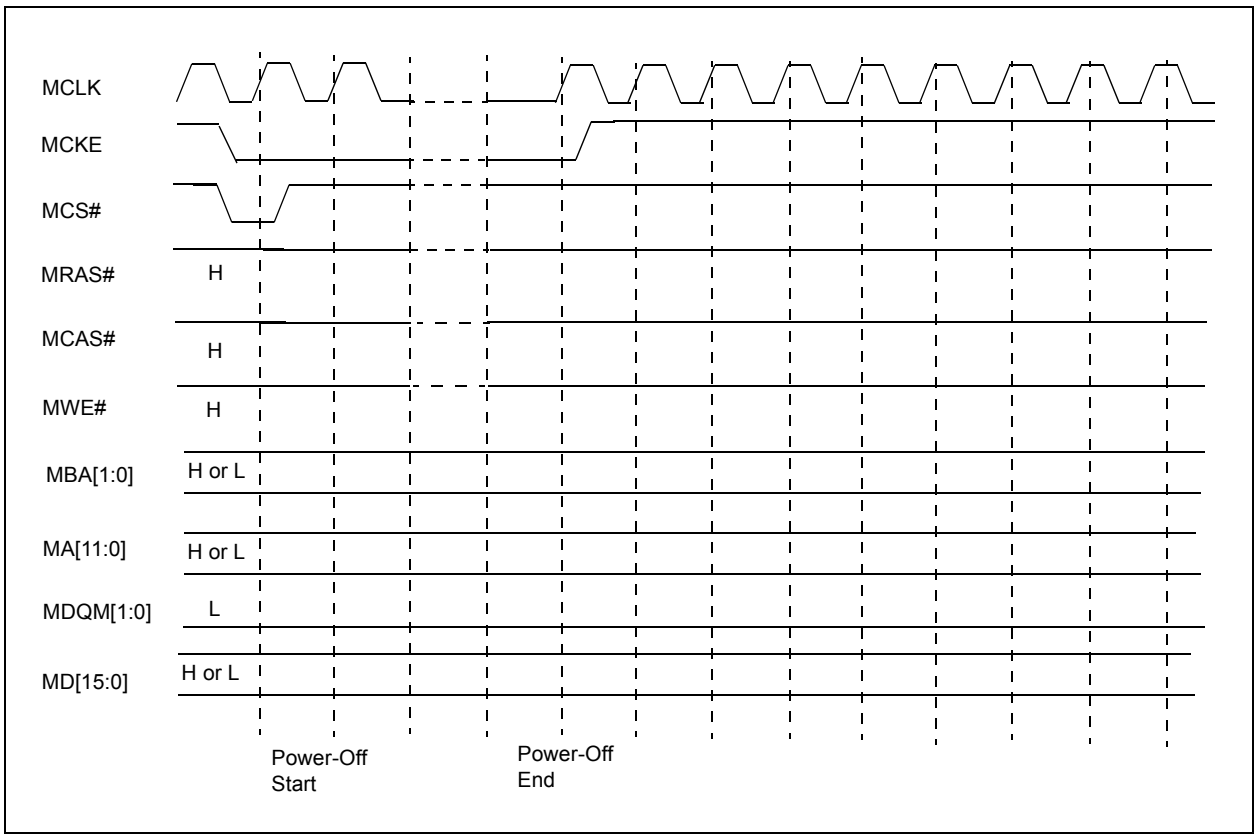


Figure 7-11: Power-Off Timing

Note
When the power-off mode is started, the control signals are forced to high level output so the SDRAM power is never shut down.

7.6 Serial Interface Timing

7.6.1 SPI Clock / Data Timing

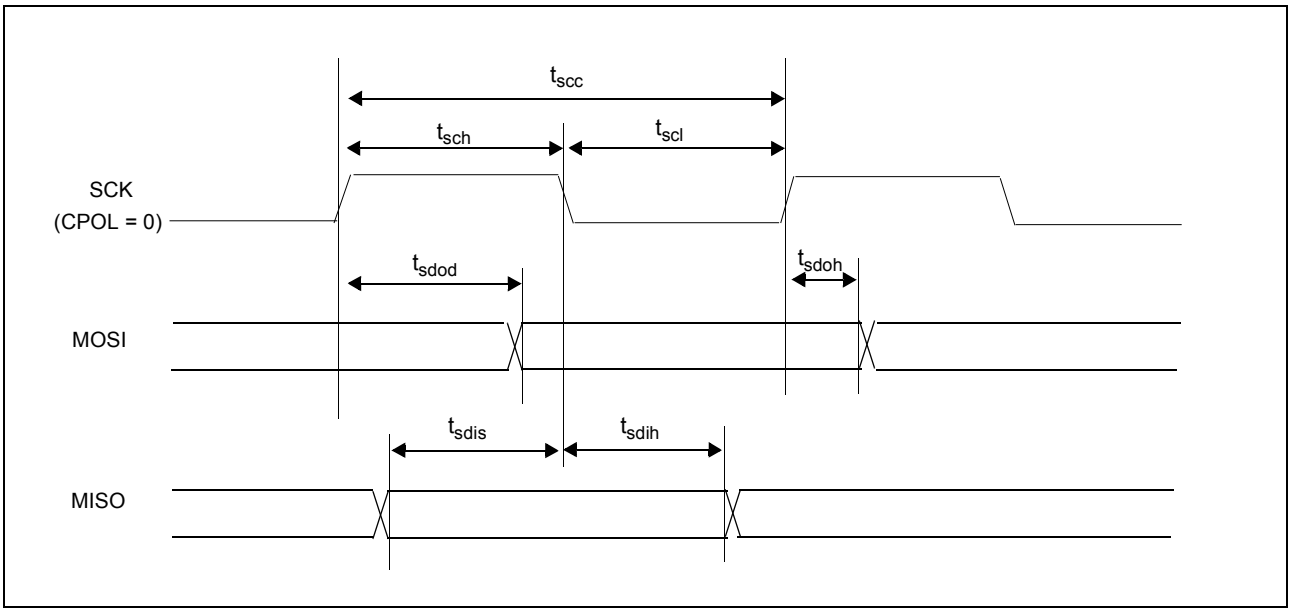


Figure 7-12: SPI Clock / Data Timing

Table 7-10: SPI Clock / Data Timing

Symbol	Parameter	Min	Max	Units
t_{scc}	SCK cycle period	66	—	ns
t_{scl}	SCK Low pulse width	t_{scc} x 0.45	—	ns
t_{sch}	SCL High pulse width	t_{scc} x 0.45	—	ns
t_{sdod}	MOSI data output delay time	—	20	ns
t_{sdoh}	MOSI data output hold time	0	—	ns
t_{sdis}	MISO data input setup time	20	—	ns
t_{sdih}	MISO data input hold time	10	—	ns

7.6.2 SPI Slave Select Timing

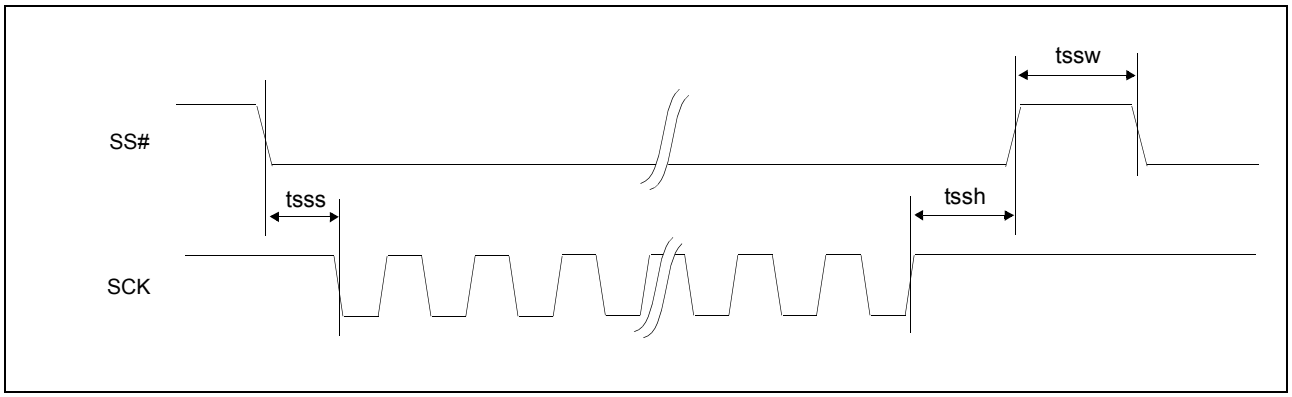


Figure 7-13: SPI Slave Select Timing

Table 7-11: SPI Slave Select Timing

Symbol	Parameter	Min	Max	Units
t_{sss}	SS# setup time	400	—	ns
t_{sshl}	SS# hold time	1000	—	ns
t_{ssw}	SS# High pulse width	1000	—	ns

7.6.3 I2C Interface Timing

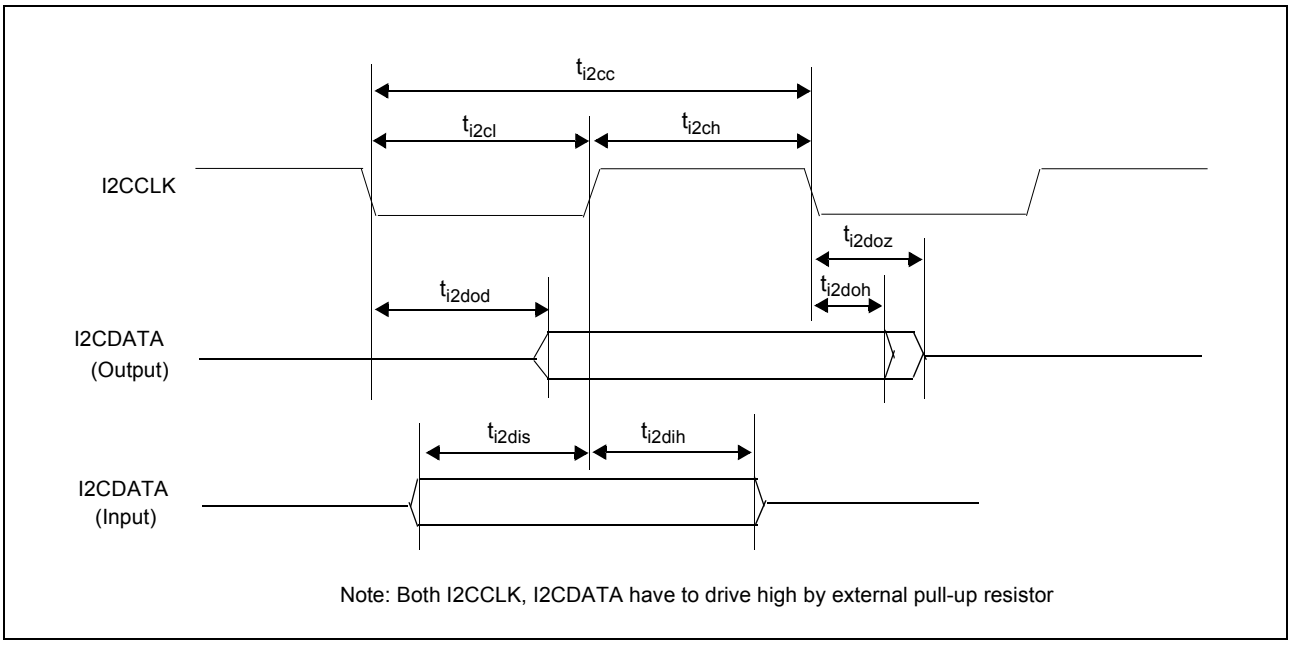


Figure 7-14: I2C Interface Timing

Table 7-12: I2C Interface Timing

Symbol	Parameter	MIN	MAX	Units
t_{i2cc}	I2CCLK cycle period	2130	—	ns
t_{i2cl}	I2CCLK Low pulse width	t_{i2cc} x 0.45	—	ns
t_{i2ch}	I2CCLK High pulse width	t_{i2cc} x 0.45	—	ns
t_{i2dod}	I2CDATA data output delay time	—	20	ns
t_{i2doh}	I2CDATA data output hold time	0	—	ns
t_{i2doz}	I2CDATA data output Hi-Z time	—	20	ns
t_{i2dis}	I2CDATA data input setup time	20	—	ns
t_{i2dih}	I2CDATA data input hold time	10	—	ns

7.7 LCD Interface Timing

The timing parameters required to drive a flat panel display are shown below. Timing details for each supported panel type are provided in the remainder of this section.

Note
All timing measurements are taken to/from the 1/2*IOVDD level in the following display interface timing diagrams.

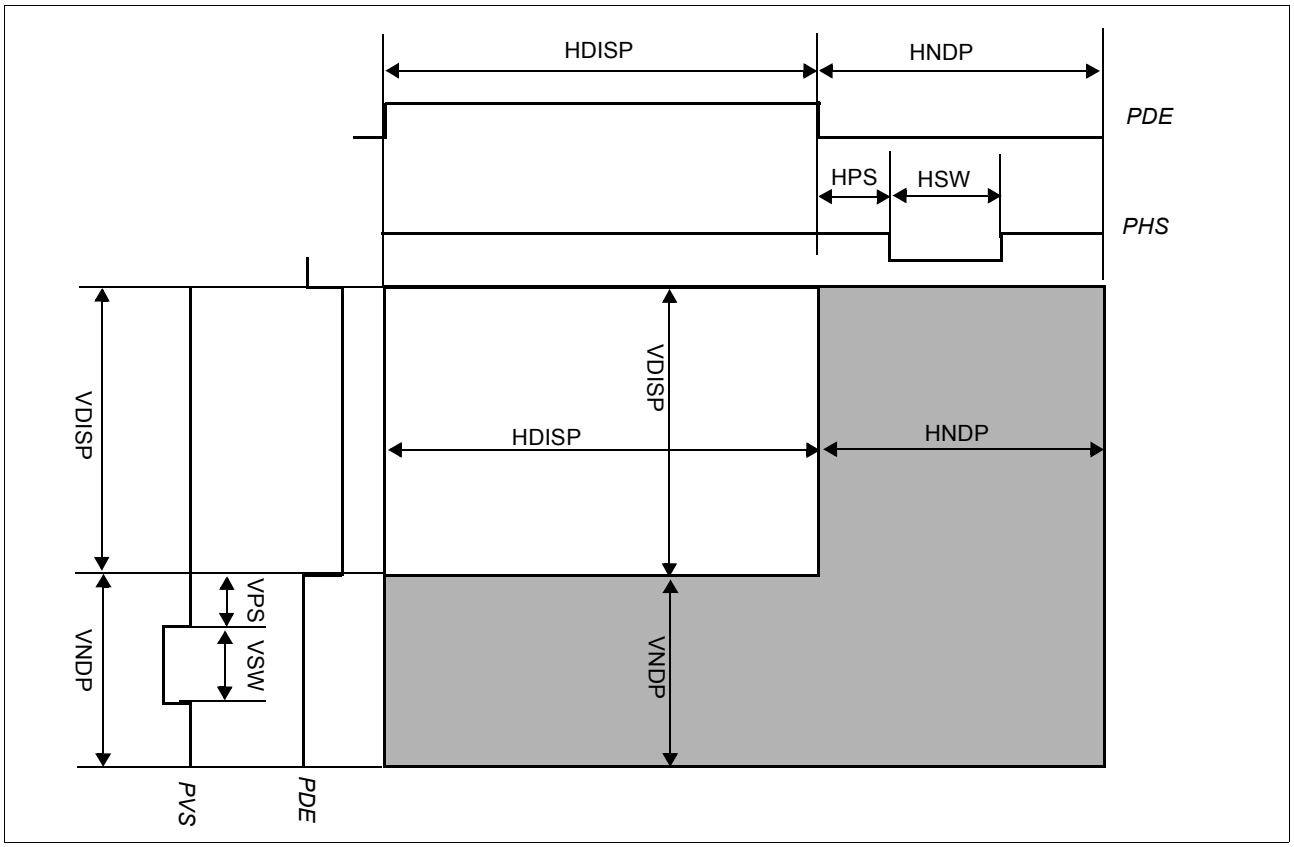


Figure 7-15: Panel Timing Parameters

Table 7-13: Panel Timing Parameters

Symbol	Description	Register	Min	Max	Units
HDISP	Horizontal Display Width	((REG[16h] bits 6-0) + 1) x 8	32	960	Ts (Note)
HNDP	Horizontal Non-Display Period	((REG[18h] bits 7-0) + 1) x 2	4	512	
HPS	PHS Pulse Start Position	(REG[22h] bits 6-0)	0	127	
HSW	PHS Pulse Width	(REG[20h] bits 6-0) + 1	1	128	
VDISP	Vertical Display Height	(REG[1Ch] bits 1-0, REG[1Ah] bits 7-0) + 1	32	960	Line
VNDP	Vertical Non-Display Period	((REG[1Eh bits 7-0) + 1) x 2	4	512	
VPS	PVS Pulse Start Position	(REG[26h] bits 7-0)	0	255	
VSW	PVS Pulse Width	(REG[24h] bits 5-0) + 1	1	64	

Note
Ts = 1/PCLK

7.7.1 LCD Panel Power-on Sequence

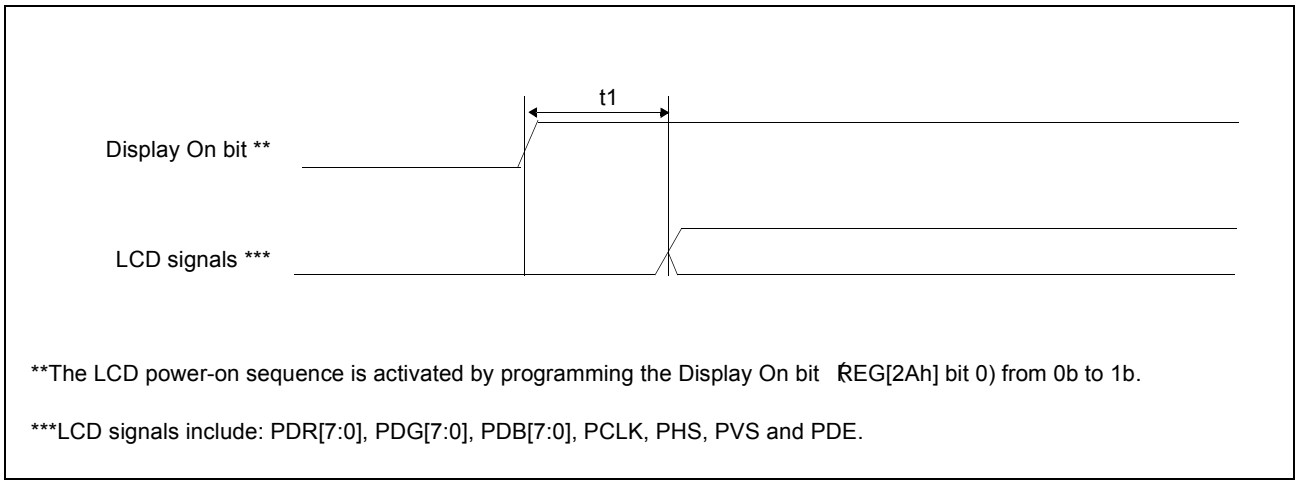


Figure 7-16: LCD Panel Power-on Sequence Timing

Table 7-14: LCD Panel Power-on Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	Display on to LCD signals active	0	10	Ts

7.7.2 LCD Panel Power-off Sequence

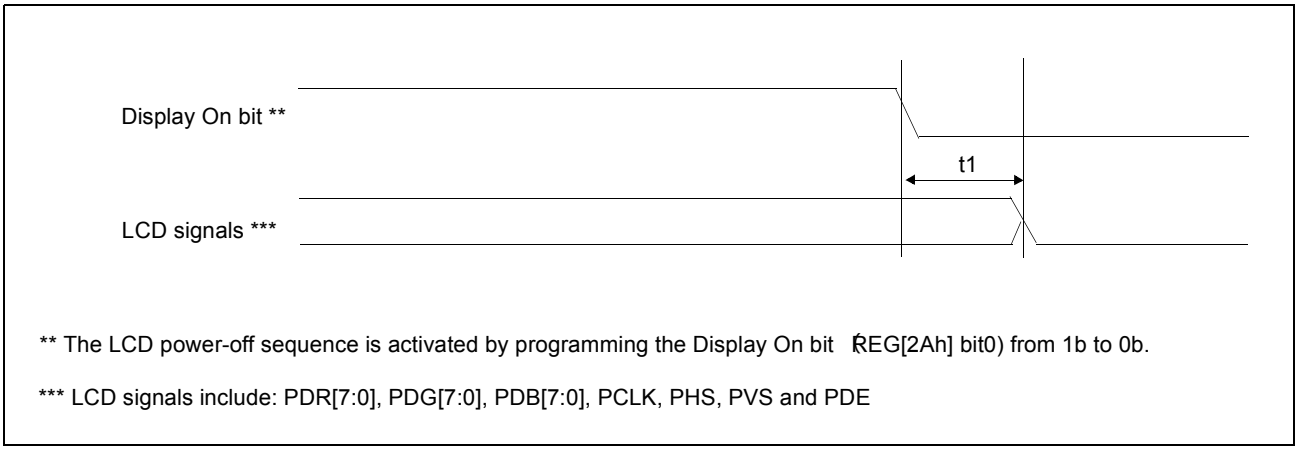


Figure 7-17: LCD Panel Power-off Sequence Timing

Table 7-15: LCD Panel Power-off Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	Display off to LCD signals inactive	0	10	Ts

7.7.3 LCD Panel Timing

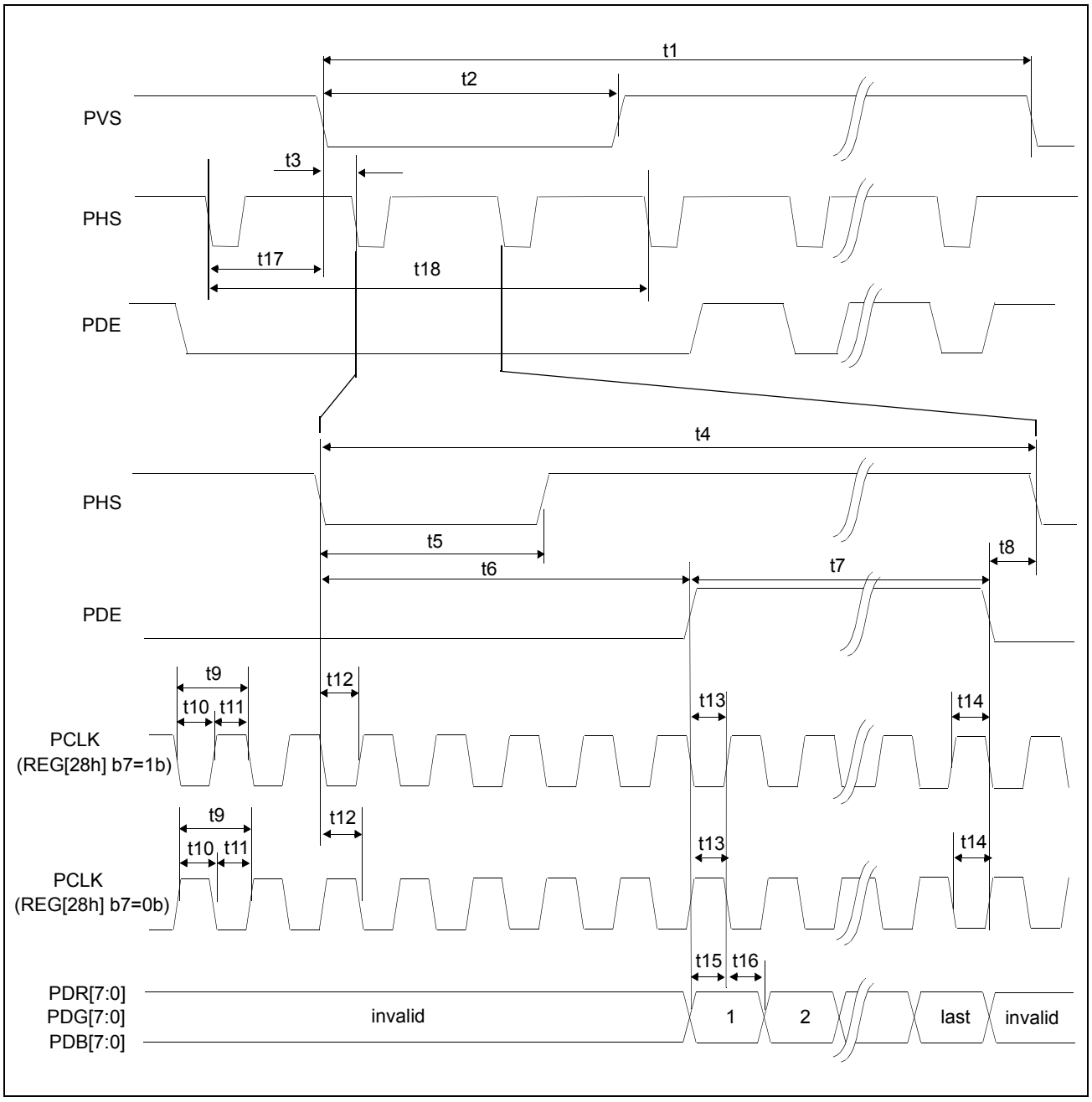


Figure 7-18: LCD Panel Timing

Note
PHS, PVS and PCLK have Polarity Select bits REG[20h] bit 7, REG[24] bit 7 and REG[28] bit 7 respectively.

Table 7-16: LCD Panel Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	PVS cycle time	—	VDISP + VNDP	—	Lines
t2	PVS pulse width Low	—	VSW	—	Lines
t3	PVS falling edge to PHS rising edge phase difference	—	HPS	—	Ts
t4	PHS cycle time	—	HDISP + HNDP	—	Ts
t5	PHS pulse width Low	—	HSW	—	Ts
t6	PHS falling edge to PDE active	—	HNDP - HPS	—	Ts
t7	PDE pulse width	—	HDISP	—	Ts
t8	PDE falling edge to PHS falling edge	—	HPS	—	Ts
t9	PCLK period	1	—	—	Ts
t10	PCLK pulse width Low	0.5	—	—	Ts
t11	PCLK pulse width High	0.5	—	—	Ts
t12	PHS setup to PCLK falling edge	0.5	—	—	Ts
t13	PDE to PCLK rising edge setup time	0.5	—	—	Ts
t14	PCLK rising edge to PDE hold time	0.5	—	—	Ts
t15	Data setup to PCLK rising edge	0.5	—	—	Ts
t16	PCLK rising edge to data hold time	0.5	—	—	Ts
t17	PDE stop setup to PVS start	—	VPS	—	Ts
t18	Vertical non-display period	—	VNDP	—	Ts

Ts = Pixel clock period

7.7.4 LCD Interface Timing

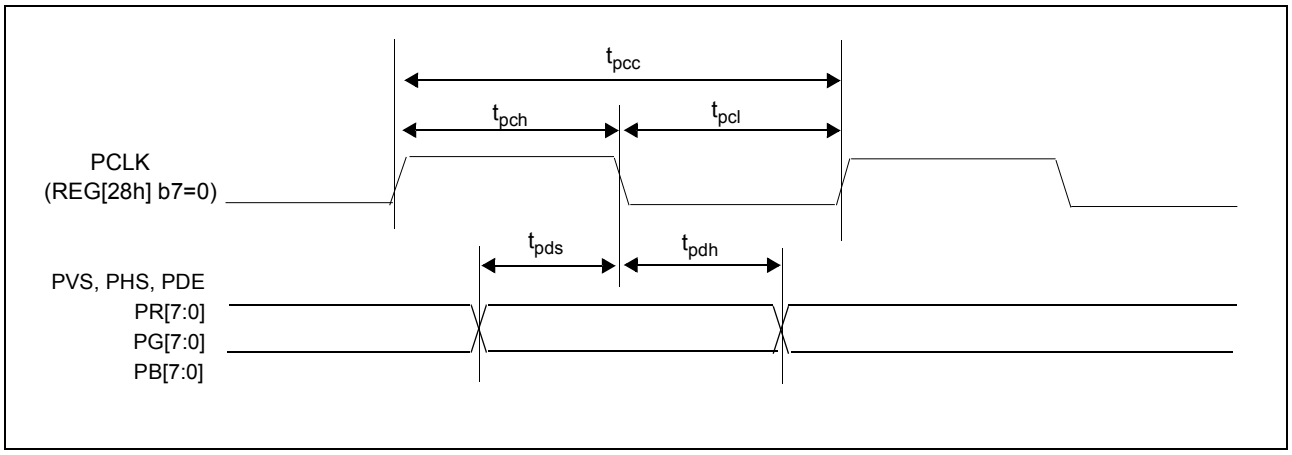


Figure 7-19: LCD Interface Timing

Table 7-17: LCD Interface Timing

Symbol	Parameter	MIN	MAX	Units
t_{pcc}	PCLK cycle time	20	—	ns
t_{pcl}	PCLK pulse width Low	t_{pcc} * 0.4	—	ns
t_{pch}	PCLK pulse width High	t_{pcc} * 0.4	—	ns
t_{pds}	LCD signals output setup time	t_{pch} - 3	—	ns
t_{pdh}	LCD signals output hold time	t_{pcl} - 3	—	ns

Chapter 8 Clocks

8.1 Clock Descriptions

The clock source for the S1D13U11 is the crystal oscillator. The USB clock (USBCLK) is generated by the USB-PLL, the SDRAM clock (SDCLK) is generated by a PLL or directly from the oscillator, and the LCD clock (LCDCLK) is divided from SDCLK, which then becomes the pixel clock (PCLK).

The Spread Spectrum modulation (SS) can be added to SDCLK or LCDCLK (however, the frequency range is limited to 78MHz.).

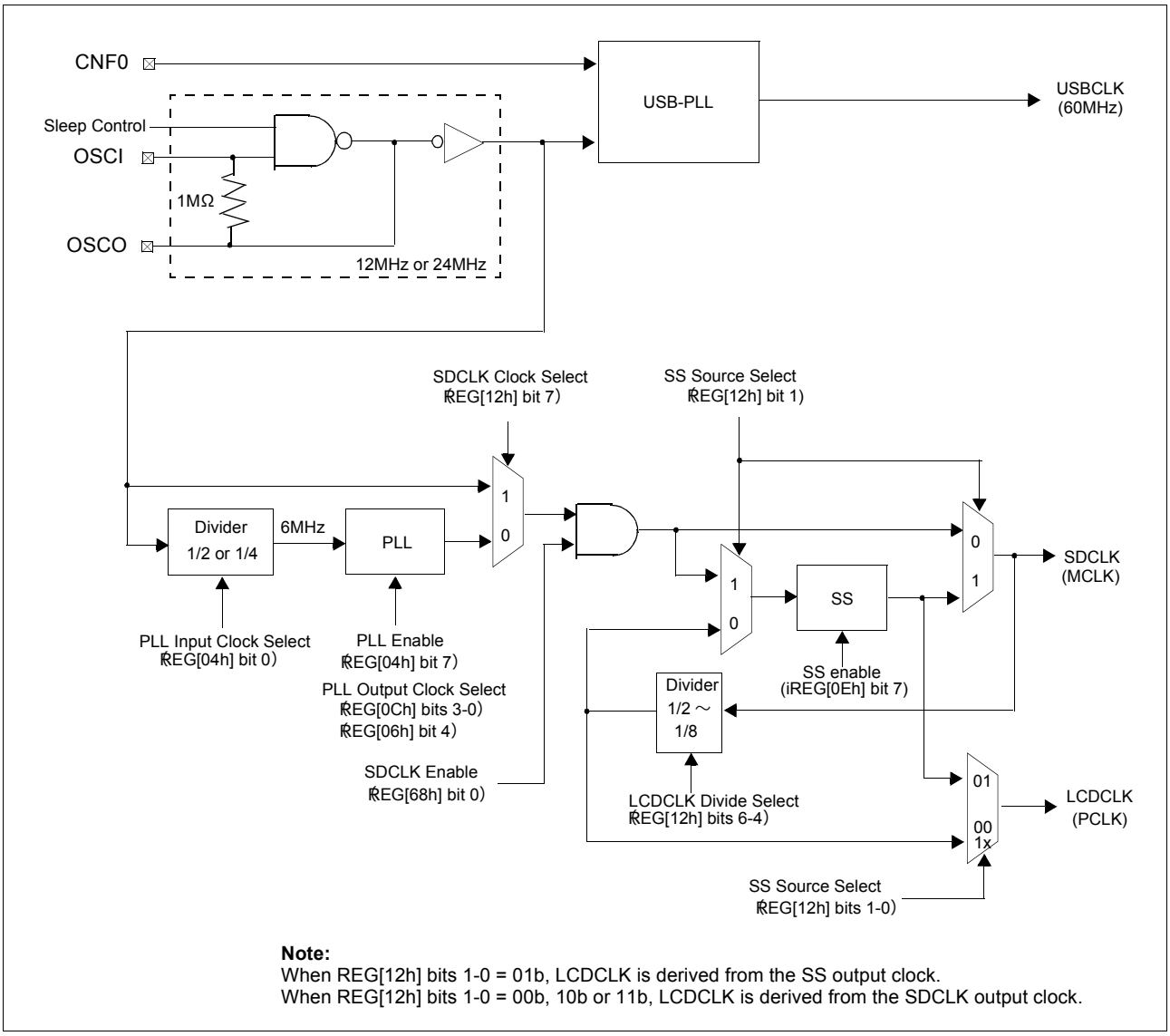


Figure 8-1: Clock Block Diagram

Chapter 9 Reset

9.1 Hardware Reset

All internal system blocks may be hardware reset by bringing the RESET# input pin low.

9.2 Software Reset

All internal system blocks may be software reset from host CPU command input. This function is the same as the hardware reset. For further information on this command, see the S1D13U11 Software Technical Manual, X96A-A-002-xx.

9.3 USB Bus Reset

The USB bus reset is triggered from host CPU input. After a USB bus reset, most internal system blocks, except the USB device port, are kept at the previous status. For further information on this function, see S1D13U11 Software Technical Manual, X96A-A-002-xx.

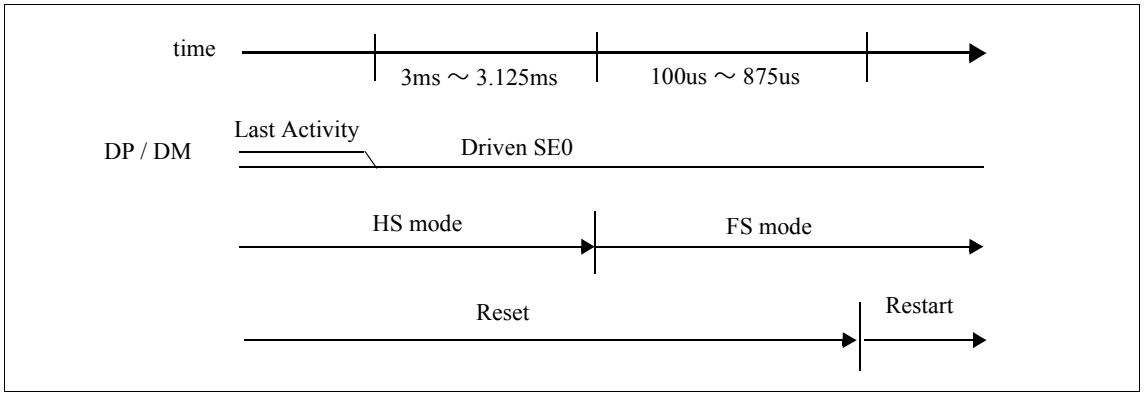


Figure 9-1: USB Bus Reset (HS mode)

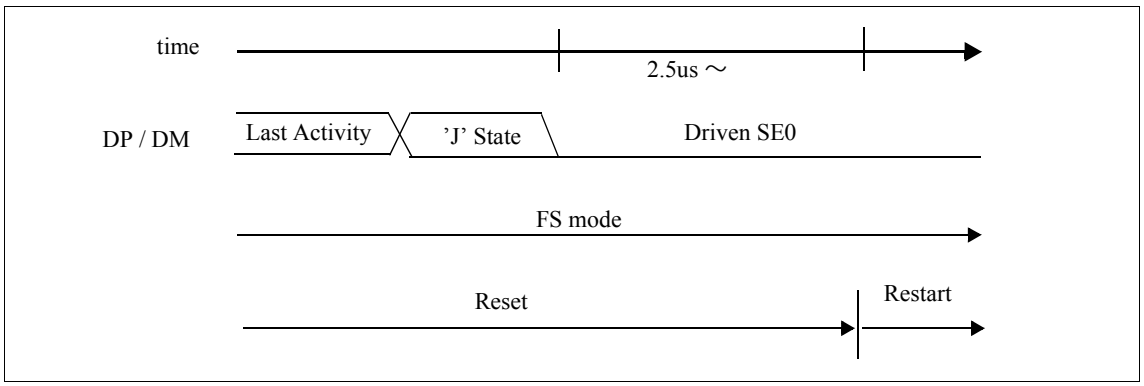


Figure 9-2: USB Bus Reset (FS mode)

Chapter 10 Host CPU Interface

10.1 USB Device Port

The S1D13U11 supports the USB2.0 (Universal Serial Bus Specification Revision 2.0) device port.

10.1.1 Speed Mode

The S1D13U11 supports High-speed mode (HS: 480Mbps) and Full-speed mode (FS: 12Mbps) USB. The speed mode is determined automatically by the speed negotiation in the USB bus reset. For example, when the S1D13U11 connects to the USB HS host, the speed negotiator will select the HS mode automatically.

10.1.2 Transfer Type

The S1D13U11 supports Control transfer, Bulk IN transfer, Bulk OUT transfer and Interrupt IN transfer. Other transfer modes are not supported.

10.1.3 Descriptor

The device class of the S1D13U11 is vender class. For further information on the descriptor, see the S1D13U11 Software Technical Manual, X96A-A-002-xx.

10.1.4 Protocol Sequencer

The S1D13U11 includes the protocol sequencer for simpler host CPU control. The host CPU must use the protocol commands to control the S1D13U11. For further information on the protocol, see the S1D13U11 Software Technical Manual, X96A-A-002-xx.

10.1.5 Configuration Data

Configuration data is necessary to run the protocol sequencer. This data has to be downloaded from the USB port or SPI interface (serial flash) into the embedded SRAM (96KB). For further information on the method of download, see the S1D13U11 Software Technical Manual, X96A-A-002-xx.

10.1.6 External Components

The S1D13U11 includes the terminal resistor for both HS mode and FS mode. Impedance matching is not necessary, so the external components are also not necessary. The DP/DM lines can connect directly between the S1D13U11 and the USB connector (or USB host device). External components for ESD protection and the EMI suppression should be added, if necessary. The VBUS pin supports 5V input, but some USB hosts may drive the voltage higher with serges, so additional protection circuits are recommended.

10.2 Endpoint

The S1D13U11 has the endpoint 0 and four specified endpoints. For further information on the endpoint, see the S1D13U11 Software Technical Manual, X96A-A-002-xx.

10.2.1 Endpoint 0

Endpoint 0 is used as the control transfer. HS mode: 64-byte, FS mode: 64-byte. The S1D13U11 uses the control transfer as the standard request and vender request.

10.2.2 Endpoint 1

Endpoint 1 is used as the command transfer (Bulk OUT transfer). HS mode: 512-byte, FS mode: 64-byte. The S1D13U11 receives the command block (command + additional data) from the host CPU.

10.2.3 Endpoint 2

Endpoint 2 is used as the status transfer (Bulk IN transfer). HS mode: 512-byte, FS mode: 64-byte. The S1D13U11 sends the status block (status + additional data) to the host CPU for returning the command response.

10.2.4 Endpoint 3

Endpoint 3 is used as the event notification (Interrupt IN transfer). HS mode: 64-byte, FS mode: 64-byte. The S1D13U11 sends the event block (event + additional data) to the host CPU.

10.2.5 Endpoint 4

Endpoint 4 is used as the display data transfer (Bulk OUT transfer). HS mode: 512-byte, FS mode: 64-byte. The S1D13U11 receives the display data from the host CPU.

10.3 Protocol

The S1D13U11 communicates the command, status, event and display data to/from host CPU. The sequence and method are determined by the protocol.

10.3.1 Command

The S1D13U11 receives the following commands from host CPU.

Table 10-1: Command Descriptions

Command	Description
Configuration	Control the download of the configuration data
LCD register write	Control the register write for LCD interface
LCD register read	Control the register read for LCD interface
LCD display data write	Control the display data write for LCD interface
LCD wake-up	Control the wake-up for LCD interface
I2C	Control the I2C interface
SPI	Control the SPI interface
SPI sequential	Control the SPI sequential interface
GPIO	Control the GPIO interface
Key-scan	Control the key-scan interface
Buzzer	Control the buzzer interface
Event	Control the event notification

10.3.2 Status

The S1D13U11 sends the following status to the host CPU.

Table 10-2: Status Description

Status	Description
Command Success	Indicate the command success
Command Error	Indicate the command error
Invalid Parameter	Indicate the invalid parameter
Protocol Error	Indicate the protocol error

10.3.3 Event Notification

The S1D13U11 sends the following event notifications to the host CPU.

Table 10-3: Event Notification Description

Event Notice	Description
LCD interface	Show the LCD interface interrupt
INT0 input	Show the SPI interface interrupt
SPI sequential	Show the receive the SPI sequential data
GPIO input	Show the GPIO interrupt
INT1 input	Show the wake-up key input
Key-scan	Show the key-scan data changing

10.4 Display Input Data Format

The data format of the display input is selected as 16bpp mode (16-bit/pixel), 24bpp mode 1 (24-bit/pixel) or 24bpp mode 2 (32-bit/pixel). The three formats can be mixed in a system, but the data format of the SDRAM must be selected as either 16bpp or 24bpp.

10.4.1 Endian Type 1 (REG[14h] bit 6 = 0b)

Table 10-4: 16bpp mode (REG[14h] bits 2-1 = 1Xb)

Order	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	G_0^4	G_0^3	G_0^2	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3
2	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	G_0^7	G_0^6	G_0^5
3	G_1^4	G_1^3	G_1^2	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3
4	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	G_1^7	G_1^6	G_1^5
5	G_2^4	G_2^3	G_2^2	B_2^7	B_2^6	B_2^5	B_2^4	B_2^3
6	R_2^7	R_2^6	R_2^5	R_2^4	R_2^3	G_2^7	G_2^6	G_2^5

Table 10-5: 24bpp mode 1 (REG[14h] bits 2-1 = 00b)

Order	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0
2	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0
3	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0
4	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
5	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
6	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0

Table 10-6: 24bpp mode 2 (REG[14h] bits 2-1 = 01b)

Order	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0
2	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
3	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
4	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0
5	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0
6	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
7	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
8	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0

10.4.2 Endian Type 2 (REG[14h] bit 6 = 1b)

Table 10-7: 16bpp mode (REG[14h] bit 2-1 = 1Xb)

Order	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	G_0^4	G_0^3	G_0^2	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3
2	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	G_0^7	G_0^6	G_0^5
3	G_1^4	G_1^3	G_1^2	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3
4	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	G_1^7	G_1^6	G_1^5
5	G_2^4	G_2^3	G_2^2	R_2^7	R_2^6	R_2^5	R_2^4	R_2^3
6	B_2^7	B_2^6	B_2^5	B_2^4	B_2^3	G_2^7	G_2^6	G_2^5

Table 10-8: 24bpp mode 1 (REG[14h] bits 2-1 = 00b)

Order	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0
2	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0
3	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
4	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0
5	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0
6	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0

Table 10-9: 24bpp mode 2 (REG[14h] bits 2-1 = 01b)

Order	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
2	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0
3	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0
4	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
5	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
6	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0
7	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0
8	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0

Chapter 11 LCD Interface

11.1 Overview

The S1D13U11 includes the color LCD interface with the external SDRAM frame buffer. The maximum panel size supported is 800x600 @ 24bpp TFT.

11.1.1 Display Support

The S1D13U11 supports the following TFT panel sizes. The maximum frequency of the pixel clock (PCLK) is 48MHz.

Table 11-1: LCD Panel Support

Panel Size	Data width
QVGA	320 x 240 @ 16bit / 18bit / 24bit
WQVGA	400 x 240 @ 16bit / 18bit / 24bit
HVGA	640 x 240 @ 16bit / 18bit / 24bit
VGA	640 x 480 @ 16bit / 18bit / 24bit
WVGA	800 x 480 @ 16bit / 18bit / 24bit
SVGA	800 x 600 @ 16bit / 18bit / 24bit

11.1.2 Display Function

The S1D13U11 supports the following display functions. The start-up display requires external flash memory.

Table 11-2: Display Function

Display Function	Description
24bpp / 16bpp display	24bpp / 16bpp color depth in the frame buffer
Write window	X/Y window data write for the frame buffer
Transparent write	Write data mask for the frame buffer
Picture-in-Picture display	PIP1 window and PIP2 window display
Overlay display	Overlay PIP window display on main window
Alpha-blend (normal mode)	Alpha-blend from 2 window
Alpha-blend (copy mode)	Copy from a window
Alpha-blend (fill mode)	Color fill from programmable color
Rotation display	180-degree rotation display
Mirror display	Right/left mirror display
Double buffer display	Hardware switching display in double buffer
Multi buffer display	Software switching display in 16 buffer
Doubling display	Pixel doubling display for main window
Virtual display	4 direction smooth scroll
Wake-up display	Wake-up display from sleep without host CPU support
Start-up display	Start-up display from reset without host CPU support
Color enhancement	Gamma / Brightness / Contrast correction for LCD output data

11.1.3 Display Data Path

The display data is stored into the external SDRAM (frame buffer), then output to the LCD panel at the required refresh rate.

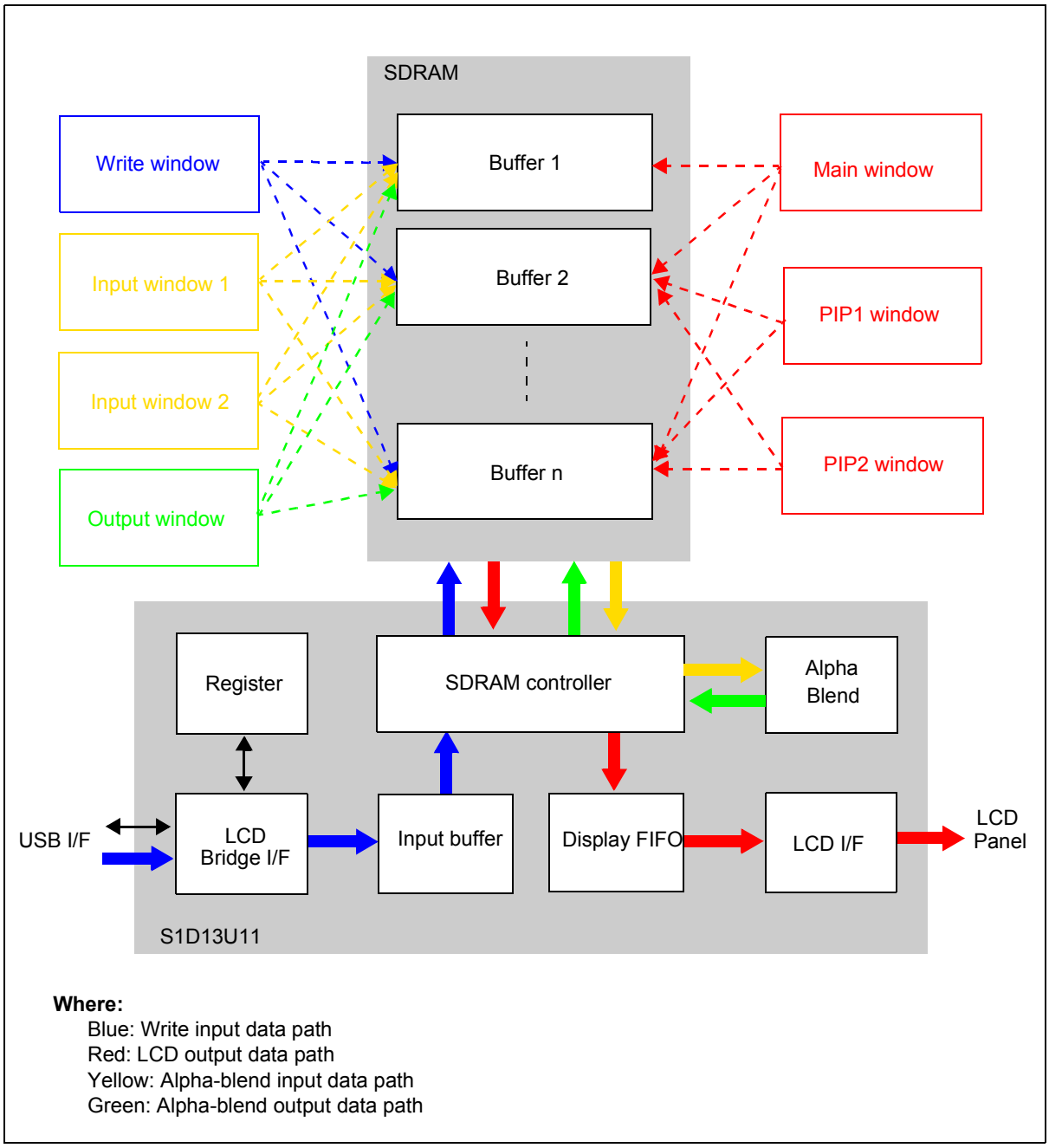


Figure 11-1: Display Data Path

11.2 LCD Bridge Interface

The LCD bridge interface is the interface block between USB interface and LCD interface. The LCD bridge interface is accessed is as follows.

11.2.1 Register Write Procedure

1. Perform the LCD register write command.

11.2.2 Register Read Procedure

1. Perform the LCD register read command.
2. Perform a data read to get the register value.

11.2.3 SDRAM (New Window) Write Procedure

1. Perform the LCD register write command to set the panel dimension registers (REG[5Ah] ~ REG[64h]).
2. Perform the LCD display data write command to start the display data write into SDRAM.
3. Perform burst data writes to fill the window.
4. Perform the LCD display data write command to complete the display data write into SDRAM.

11.2.4 SDRAM (Update Window) Write Procedure

1. Perform the LCD register write command to start the display data write into SDRAM.
2. Perform burst data writes to fill the window.
3. Perform the LCD display data write command to complete the display data write into SDRAM.

11.2.5 SDRAM Read Procedure

1. Perform the LCD register write command to set the SDRAM register (REG[E6h] bit 0 = 1).
2. Perform the LCD register write command to set the SDRAM registers (REG[E8h] ~ REG[ECh]).
3. Perform the LCD register read command to get the SDRAM dummy data port (REG[EEh]). (Dummy data is not used)
4. 500ns wait.
5. Perform the LCD register read command to get four SDRAM data at the Memory Data Port (REG[66h).
6. Return to No.3 if repeat.

11.2.6 Look-up Table Write Procedure

1. Perform the LCD register write command to set the LUT access mode (REG[B8h]). The Gamma correction enable bit is still be disabled (REG[B8h] bit 0 = 0).
2. Perform the LCD register write command to set the LUT table index register (REG[BAh]).
3. Perform the LCD register write command to point the LUT table Port (REG[BCh]).
4. Perform burst data writes to fill the LUT table.

11.2.7 Look-up Table Read Procedure

1. Perform the LCD register write command to set the LUT access mode (REG[B8h]). The Gamma correction enable bit is still be disabled (REG[B8h] bit 0 = 0).
2. Perform the LCD register write command to set the LUT table index register (REG[BAh]).
3. Perform the LCD register read command to point the LUT table Port (REG[BCh]).
4. Perform burst data read from the LUT table.

11.3 Write Window

All image data from the host is input to the LCD Controller through the Write Window. The Write Window is specified by writing the image data to a position specified by X/Y parameters. The image data can be written for a partial display update by specifying two parameters of X/Y for complete (full) display in the frame buffer.

When transparency color is enabled, the transparency color data is not written to the frame buffer.

11.3.1 Write Buffer Setting

Up to 16 write buffers may be used, depending on the buffer memory size (set in REG[90h]). The available memory is automatically divided so that all buffers are equal in size. The write buffer is selected by the register (REG[52h] bits 7-4). The mapping of the write buffers is shown in Figure 11-2: "Write Buffer Mapping".

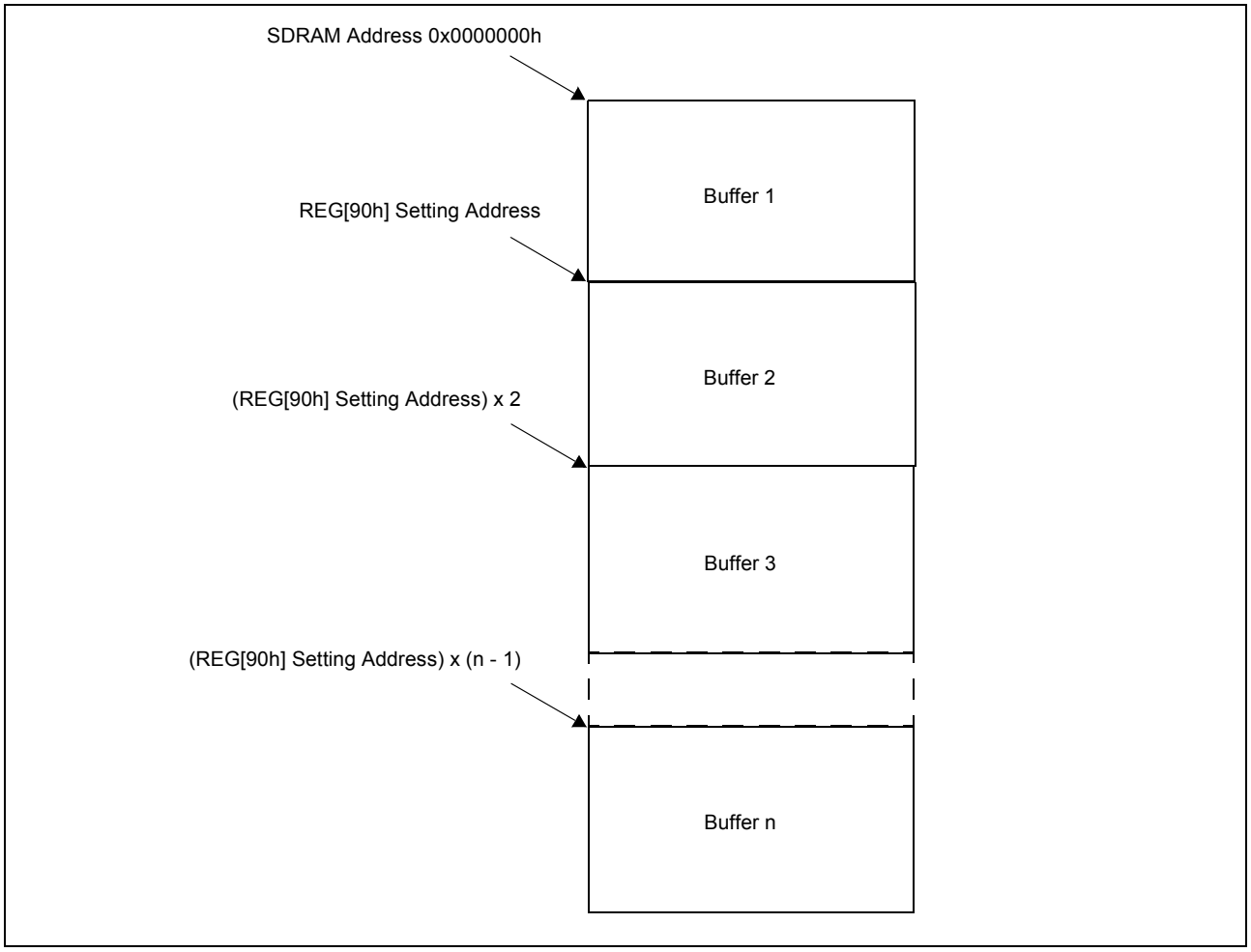


Figure 11-2: Write Buffer Mapping

11.3.2 Write Window Setting

Image data is stored in the display buffer using the write window. The write window can be configured for either a "full screen" or "partial" update according to the setting of the Write Window X/Y Start/End position registers. All position parameters are relative to the origin of the display. Horizontal position (X) must be set in eight pixel resolution. Vertical position (Y) is set in one line resolution.

The destination write buffer and other write options, such as Transparency, Mirror, and Rotation, can be selected using REG[52h]. All writes to a write buffer are "destructive" writes.

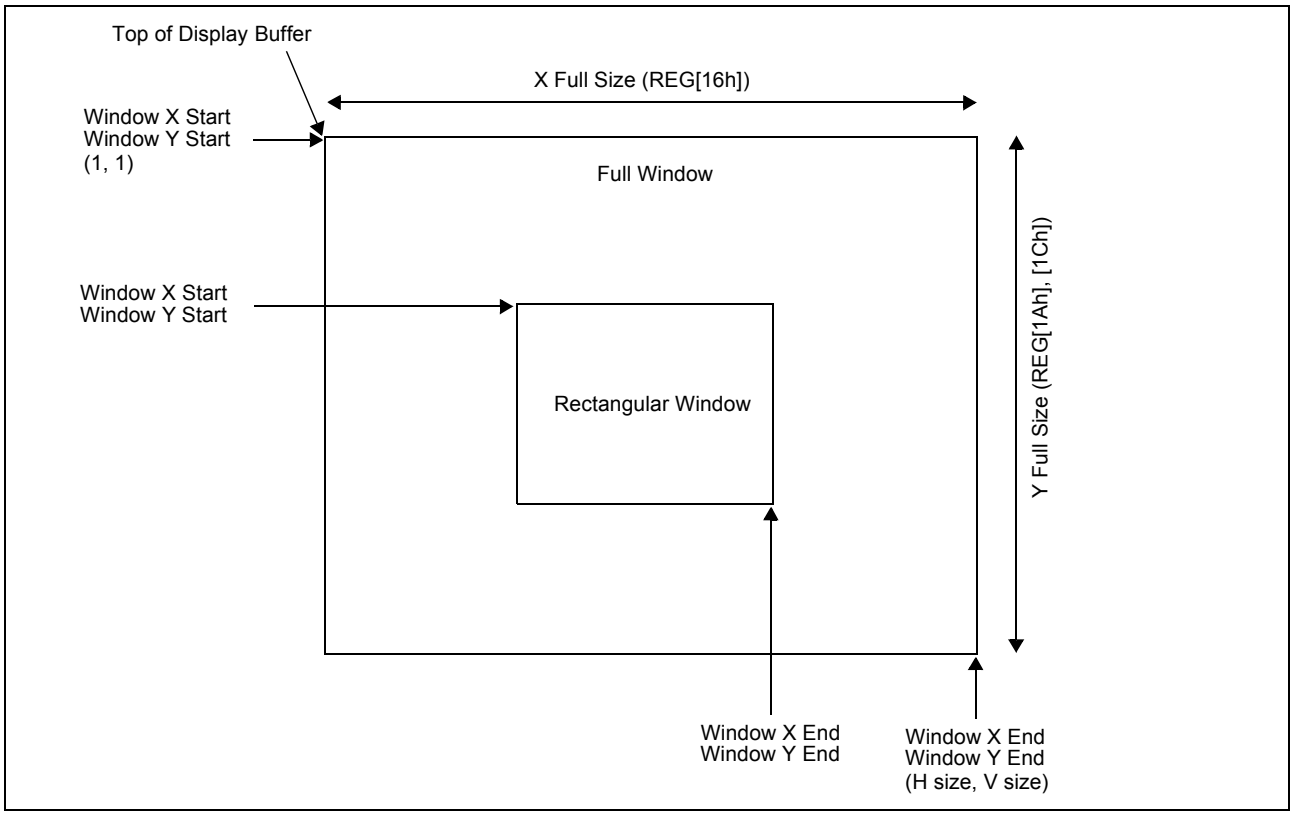


Figure 11-3: Write Window Setting

The following example shows a rectangular write window being written to a write buffer with a previously input "full screen" image.

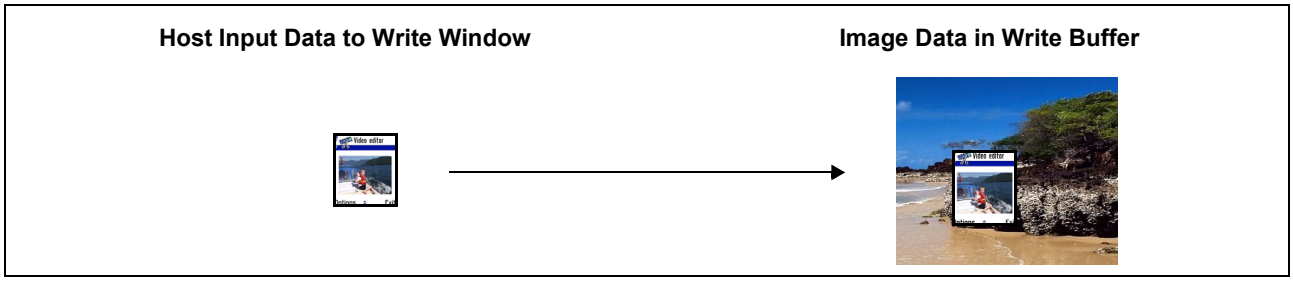


Figure 11-4: Write Window Example

11.3.3 Transparency Color

When image data is written to a write buffer, a transparency key color can be specified using REG[54h] ~ REG[58h]. When the Transparency function is enabled (REG[52h] bit 3 = 1b), pixels of the specified key color are not written to the write buffer. This function can be used to overwrite text and icons in display data.This function can not be used with rotation and mirror function, the REG[52h] bits 3-0 never be set to the value 9h, Ah and Bh.

The following example shows an example where the transparency function is enabled for the Write Window. In this case the key color is black so the black pixels are not written to the write buffer.

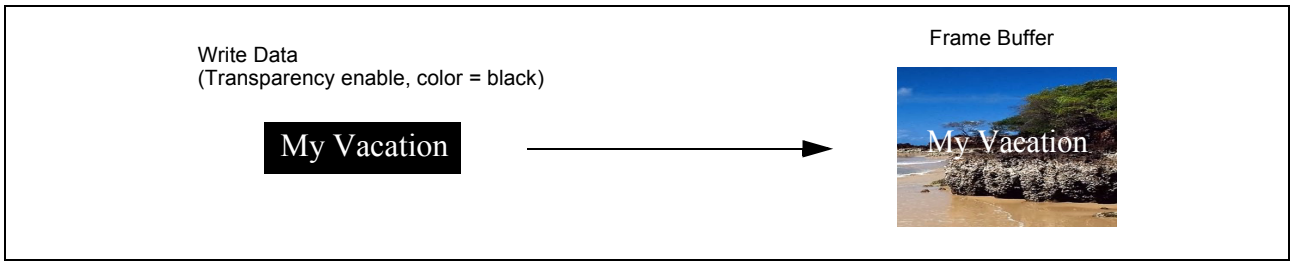


Figure 11-5: Transparency Color Example

11.4 Display Window

The S1D13U11 display window is defined by the size of the LCD display (see REG[16h] and REG[1Ah] ~ REG[1Ch]). All updates to the display window are done through a write window which allows rectangular writes to the selected write buffer (see REG[52h] bits 7-4). The write window is configured based on X/Y Start/End positions (REG[5Ah] ~ REG[64h]) relative to the origin of the display window. Once the write window is configured, all image data is written to the display buffer using the Memory Data Port registers, REG[66h] ~ REG[67h].

The write window X/Y Start/End positions are specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical). All window coordinates are referenced to top left corner of the display window (even when rotation or mirror are enabled no host side translation is required).

The display window source can be selected from any of the available write buffers (REG[2Ah] bits 7-4). All display updates can have independent mirror, rotation, and transparency settings.

11.4.1 Main Window Setting

One of the maximum 16 display buffers is used for the Main Window. The Main Window is selected by register REG[2Ah] bits 7-4, Main Window Display Buffer Select. The mapping of the display buffer is shown in Figure 11-6: “Display Buffer Map”

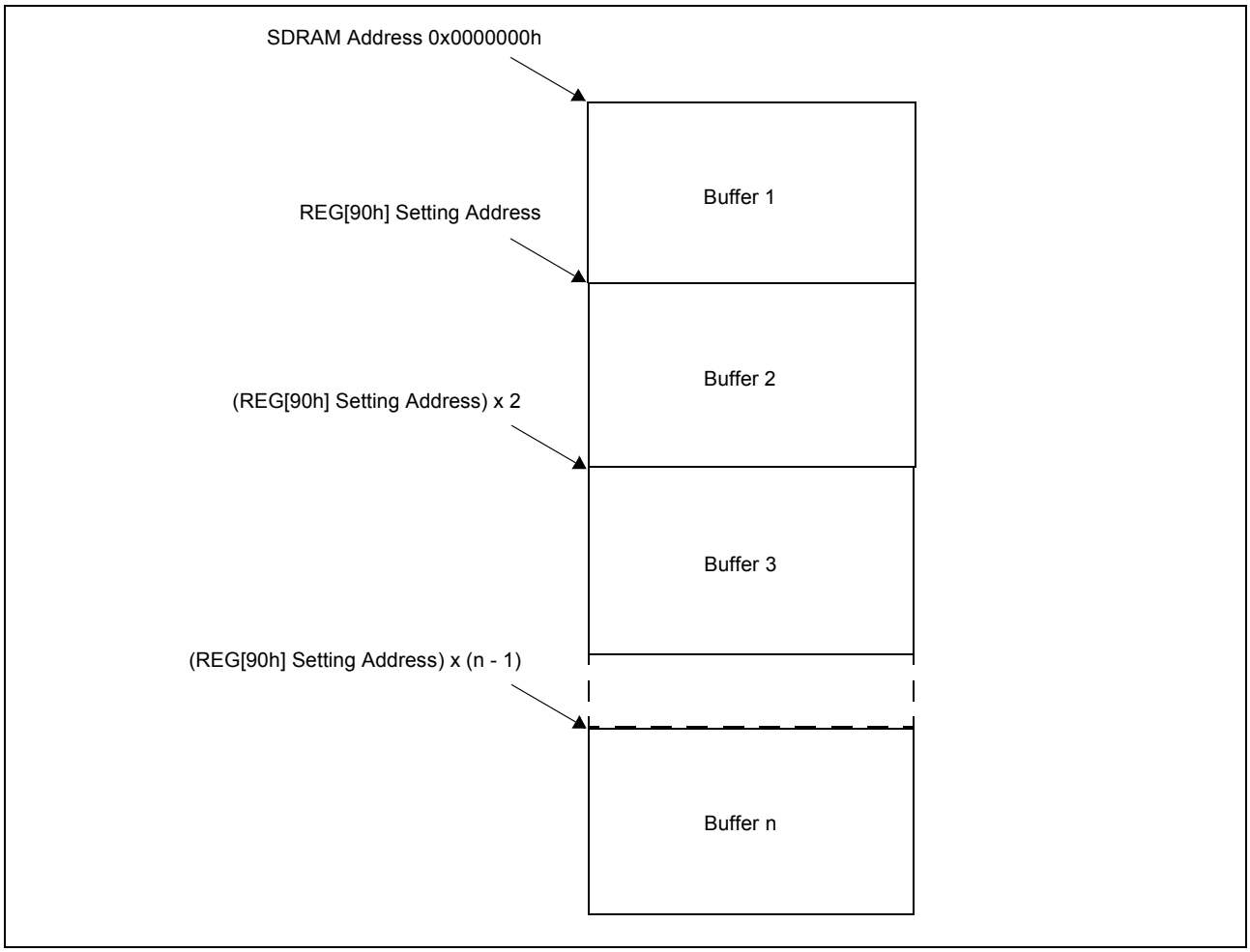


Figure 11-6: Display Buffer Map

11.4.2 Picture-in-Picture (PIP) Display

The S1D13U11 can display up to two PIP (Picture-in-Picture) windows that overlap the main display window. The PIP windows do not support transparent overlays, but provide windows that can be enabled/disabled without overwriting the display window image data.

The image data for the PIP windows must be input using the write window in the same manner as for the Display Window (see Section 11.4, “Display Window” on page 68). Typically, the PIP window image data is written to unused write buffers and the PIP1/PIP2 Display Start Address registers (REG[2Ch] ~ REG[30h] or REG[3Eh] ~ REG[42h]) are set to the beginning of selected write buffer. The PIP window position and size are configured using X/Y Start/End positions relative to the origin of the display.

If the PIP1 and PIP2 windows are overlapped, the PIP1 window appears “on top” of the PIP2 window.

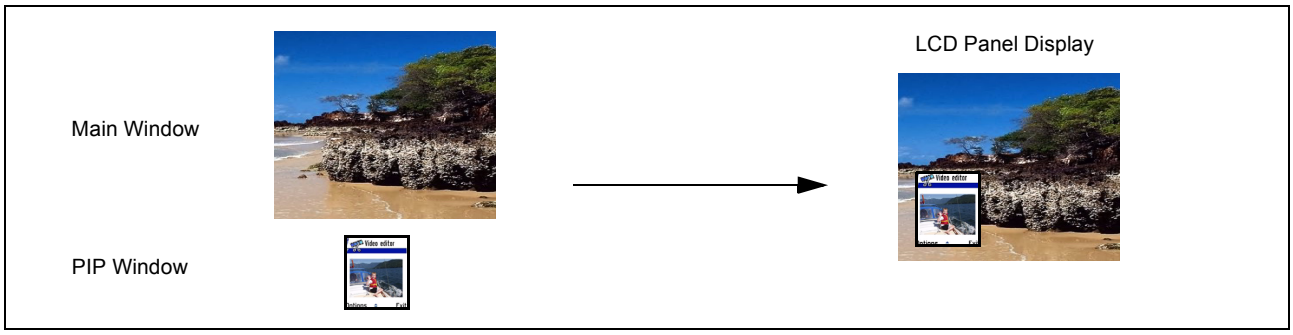


Figure 11-7: Picture-in-Picture Display

11.4.3 Picture-in-Picture Window Setting

A PIP window size and position is specified using X/Y Start/End position registers. Each PIP window has it's own set of registers (PIP1: REG[32h] ~ REG[3Ch], PIP2: REG[44h] ~ REG[4Eh]). The PIP Window X/Y Start/End positions are specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical).

Note
The PIP window must be positioned such that it remains within the dimensions of the LCD display.

The PIP window display start address is set to the beginning of the PIP window image data in the appropriate write buffer. The display start address can also be used to scroll PIP window image or provide basic animation. For more information on using the display start address in this manner, see Section 11.4.2, "Picture-in-Picture (PIP) Display" on page 70.

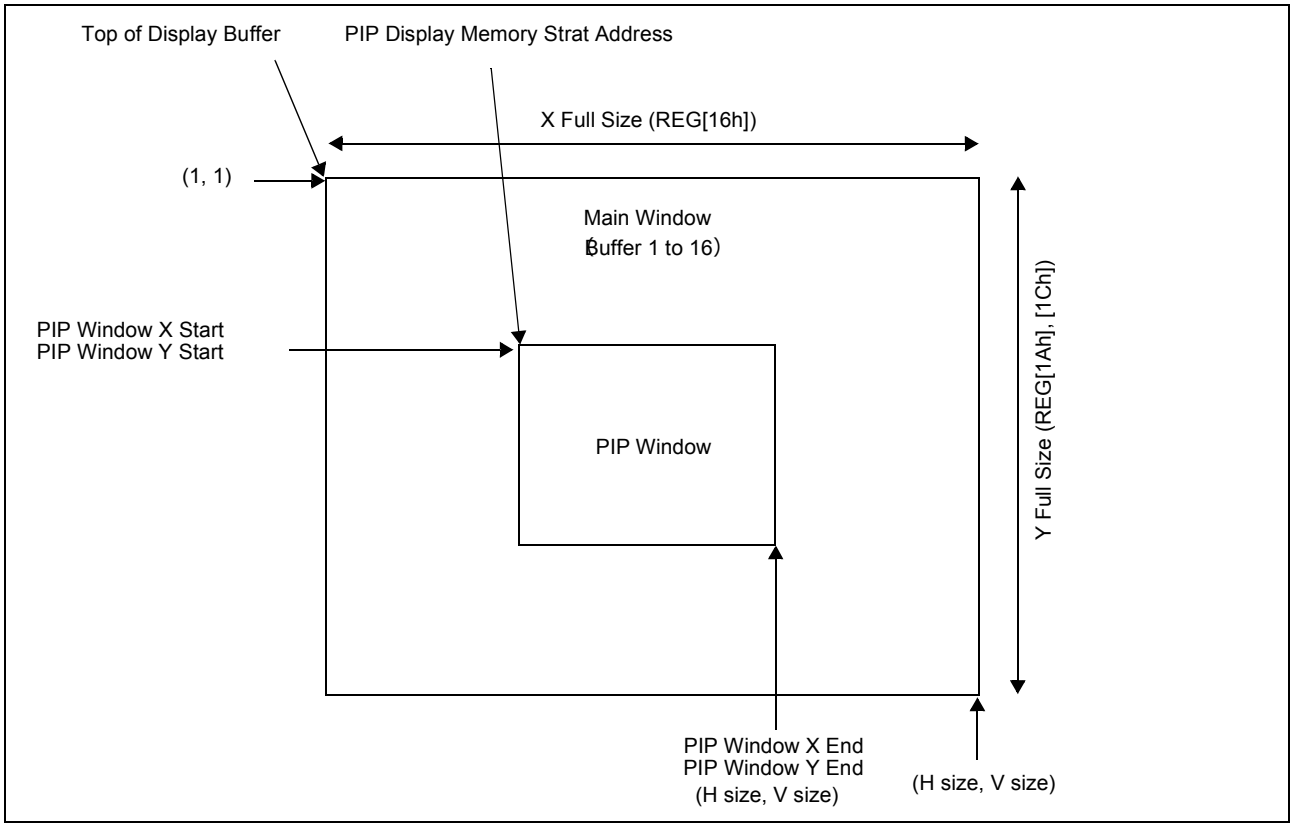


Figure 11-8: Picture-in-Picture Window Setting

11.4.4 Picture-in-Picture Window Start Start Address

The PIP window display start addresses can changed to allow scrolling within an image larger than the PIP window or basic animation by changing the start address between a series of images. This method does not alter the image data in the write buffer, but simply changes the image data that is displayed within the PIP window.

For further information on calculating memory addresses, see Section 11.13.10, “Memory Address” on page 89.

The following example shows a display window with a single PIP window. The write buffer containing the PIP window image data includes 4 separate images at DSA1, DSA2, DSA3, and DSA4. The PIP window images are “animated” by changing the PIP window display start address.

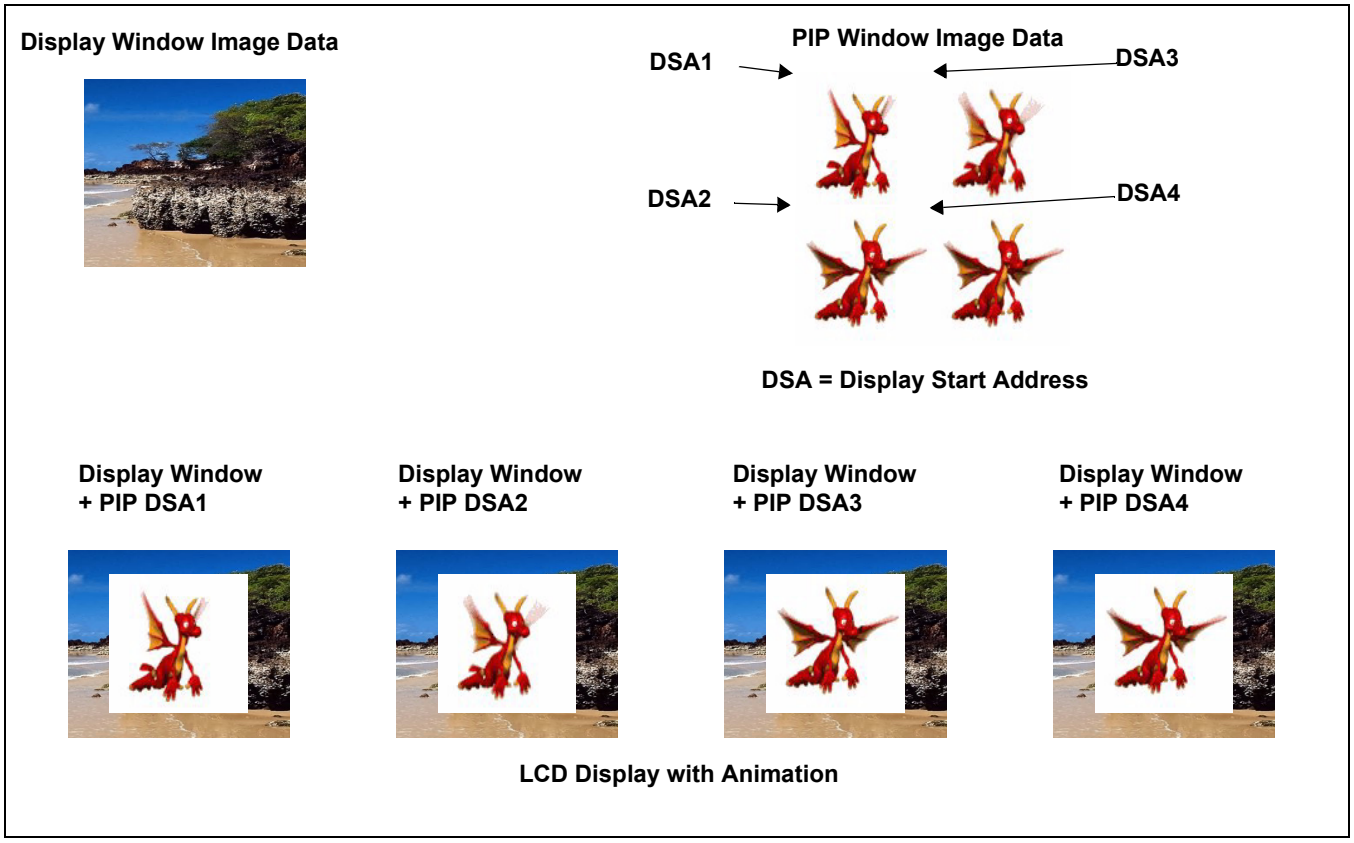


Figure 11-9: Animation Display Example

11.4.5 Overlay Display

The overlay display is a function for the main window to be overlayed with two PIP windows. The transparency color is set for PIP window. When pixels of the PIP window are matched with the transparent color, the main window data is shown instead of the PIP window data. If the overlay function is not operating correctly due to color depth (16bpp/24bpp) and clock ratio (SDCLK:LCDCLK), see "REG[12h] Clock Source Select Register" on page 100.

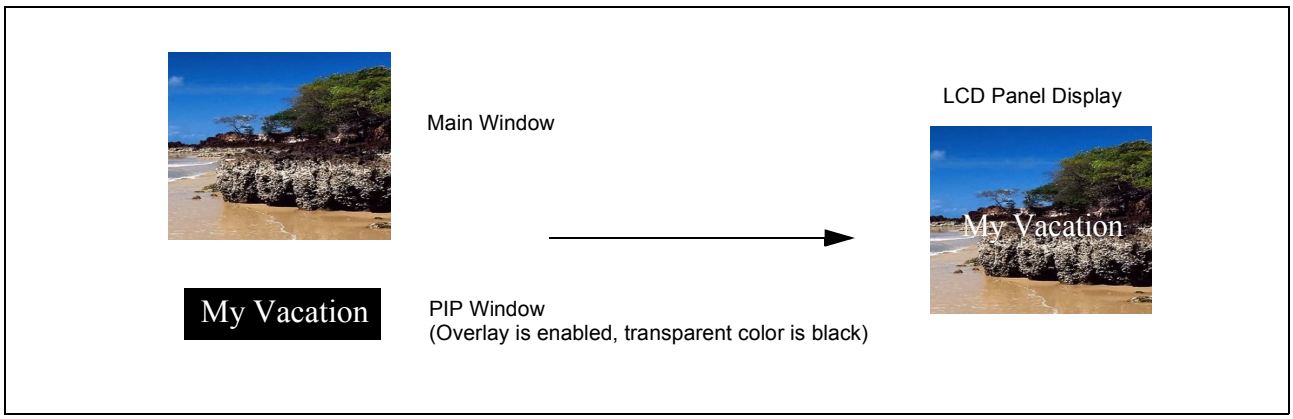


Figure 11-10: Overlay Display Example

11.5 Virtual Display

The virtual display is a method of displaying image data which is larger than the LCD panel size. The PIP window can be scrolled by changing the memory start address for the top/bottom/left/right directions. When the virtual image is written to the frame buffer, REG[52h] bit 2 must be set to 1b.

The horizontal size of the virtual image should be set by registers REG[E2h] and [E4h], the maximum size is 8192 pixels.

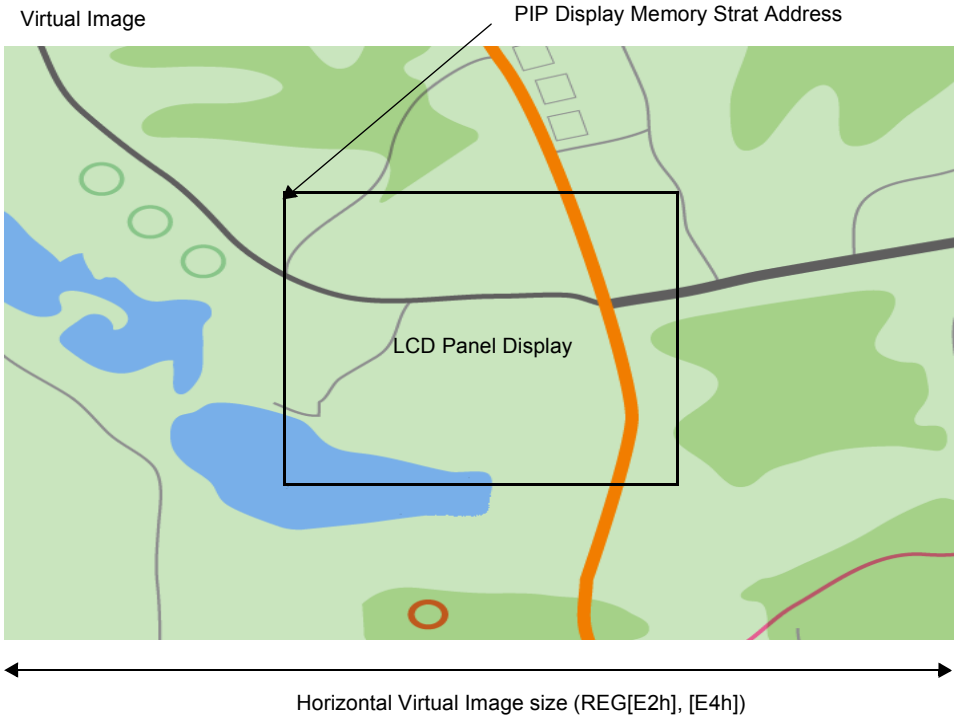


Figure 11-11: Virtual Display Example

11.6 Display Rotation and Mirror

Most computer displays are refreshed in landscape orientation - from left to right and top to bottom. Computer images are stored in the same manner.

Rotation is designed to rotate the displayed image by 180° in a counter-clockwise direction. The rotation is done in hardware and is transparent to the user. It is accomplished by rotating the image data during display writes (see REG[52h] bit 0). By processing the rotation in hardware, there is a performance advantage over software rotation of the displayed image.

Mirror is designed "mirror" the displayed image from right to left. Mirror is done in the hardware and is transparent to the user. The mirror function is done during display writes (see REG[52h] bit 1). Mirroring the image in hardware, also offers a performance advantage over software mirroring of the same image.

11.6.1 180° Rotation

The following figure shows the relationship between the image sent by the Host and the image as displayed on the LCD panel when 180° rotation is enabled (REG[52h] bit 0 = 1b). The application image is written to the S1D13U11 as A-B-C-D. However, it is stored in the write buffer as D-C-B-A and the LCD display is refreshed as D-C-B-A.

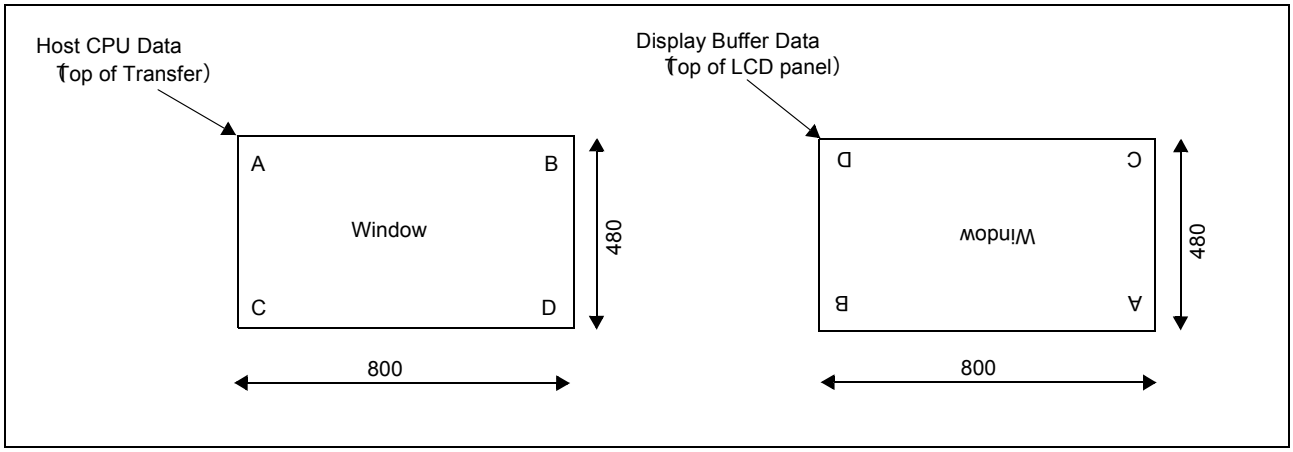


Figure 11-12: 180° Rotation Example

11.6.2 Mirror

The following figure shows the relationship between the image sent by the Host and the image as displayed on the LCD panel when Mirror is enabled (REG[52h] bit 1 = 1b). The application image is written to the S1D13U11 as A-B-C-D. However, it is stored in the write buffer as B-A-D-C and the LCD display is refreshed as B-A-D-C.

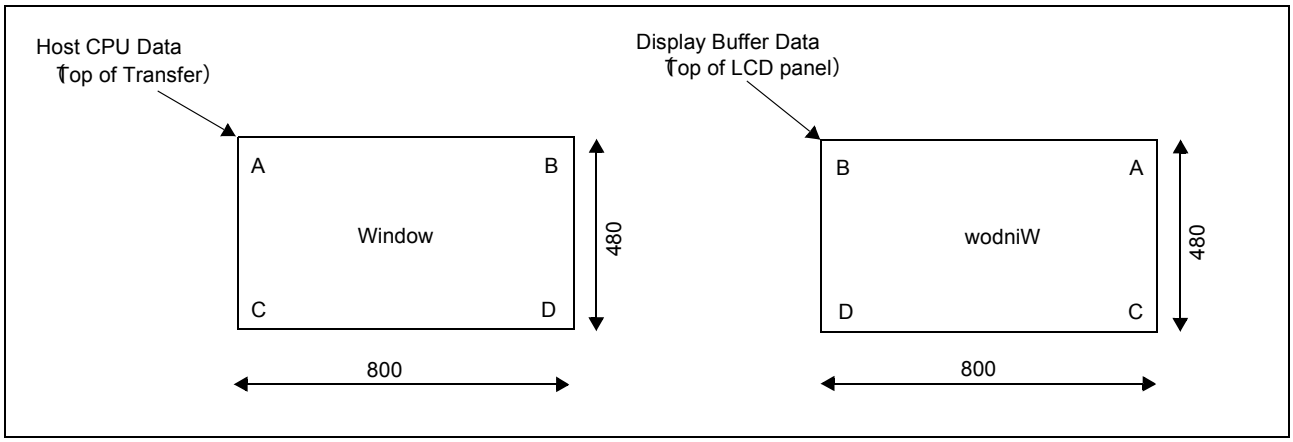


Figure 11-13: Mirror Example

11.6.3 180° Rotation and Mirror

The following figure shows the relationship between the image sent by the Host and the image as displayed on the LCD panel when both Mirror and Rotation are enabled (REG[52h] bits 1-0 = 11b). In this case, the image is rotated by the rotation function after the mirror function takes place. The application image is written to the S1D13U11 as A-B-C-D. However, it is stored in the write buffer as C-D-A-B and the LCD display is refreshed as C-D-A-B.

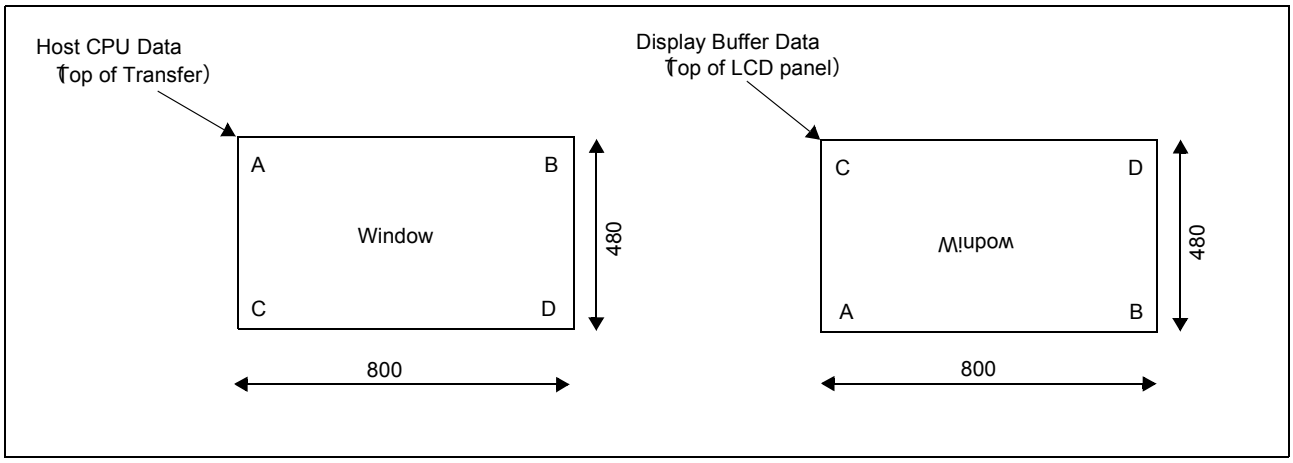


Figure 11-14: 180° Rotation and Mirror Example

11.7 Double Buffer Display

The S1D13U11 provides a display output mode which provides double buffering to prevent image tearing for streaming input. When this mode is selected (REG[2Ah] bits 3-1 = 001b), the display buffer is managed automatically. Image data is written to the write window as if a single buffer is being used. When the streaming image data is being input, the first frame is written to Buffer 1 and second frame is written to Buffer 2. Buffer 1 and 2 are fixed.

The buffer read/write pointers can only switch once per frame, at the beginning of the vertical non-display period. The pointers only switch if an animation frame has completed being updated within the last output frame period, and no new animation frame is currently being written. Because of this, each time the user finishes writing a frame of animation data, they should wait until the next vertical non-display period before writing the next frame. This can be accomplished by polling the Vertical Display Period Status (REG[6Ah] bit 7). Alternatively, if the user can guarantee that the maximum input animation data frame rate is 1/2 the LCD frame rate and that the burst length for writing a animation frame is less than one LCD frame period, then no checking for the vertical non-display period is required. However, if attention is not paid to allowing the pointers to switch, frames may be dropped.

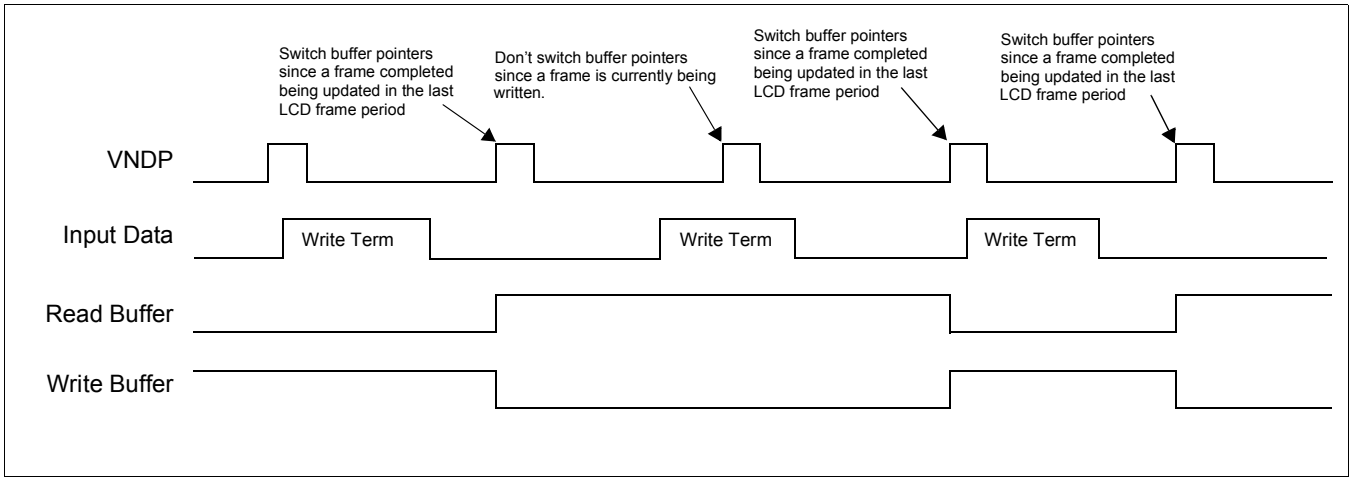


Figure 11-15: Double Buffer Switching

11.8 Display Doubling

The display doubling (also known as pixel doubling) is displayed with double the number of pixels in the frame buffer data for both the horizontal and vertical directions. The main window is only used for the display doubling.

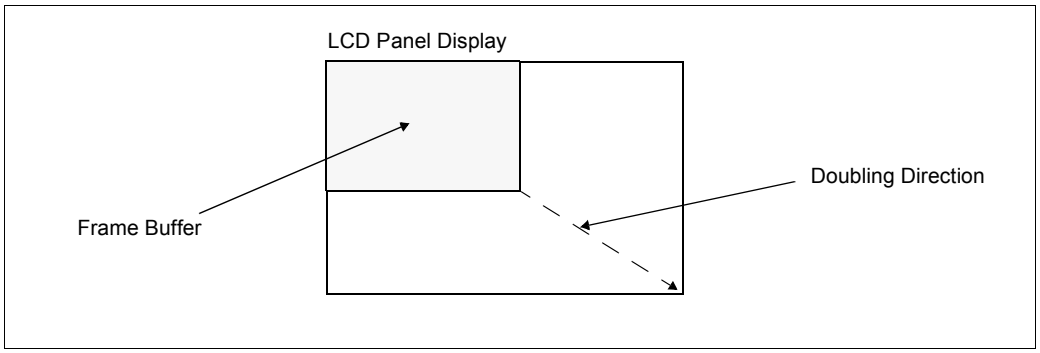


Figure 11-16: Doubling Display

11.9 Alpha-Blend

Alpha-Blend is used in computer graphics to create the effect of transparency. This technique is useful for graphics that feature glass or liquid objects and is done by combining a translucent foreground with a background color to create a blend. It can also be used for animation, where one image gradually fades into another image.

Alpha-Blend is synthesized two images of the display buffer according to the alpha value, written to Display Buffer again, and returned. Time will be required by the time the composite image is completed to access the display buffer by using the interval of the display cycle. Therefore, it can inform host CPU of the end of Alpha-Blend with an interrupt signal.

11.9.1 Alpha-Blend (Normal Mode)

In Alpha-Blend Normal Mode, the output window image is generated by blending the images from input windows 1 and 2. Either of the two input windows may over write the blended image by setting the desired input window to be the output window. All three windows should be the same size.

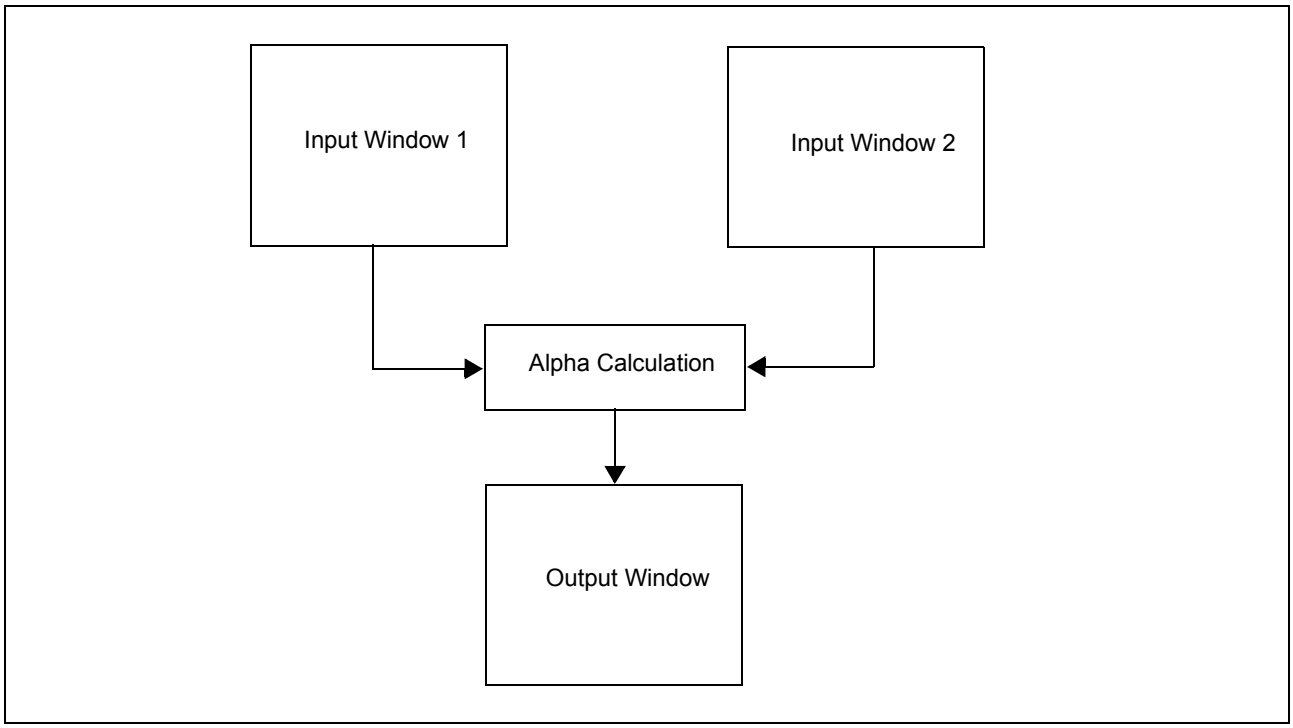


Figure 11-17: Alpha-Blend Data flow (Normal mode)

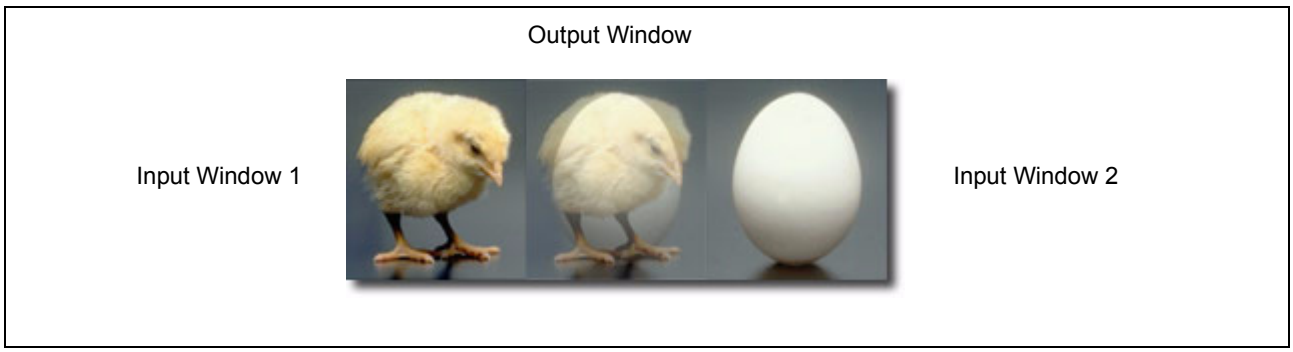


Figure 11-18: Alpha-Blend Example

11.9.2 Alpha-Blend (Copy mode)

Alpha-Blend can make the output image from the input image 1. It is possible to make it to the output image by copying input image 1 as it is if the alpha value is 32/32. The size of two images should be made the same.

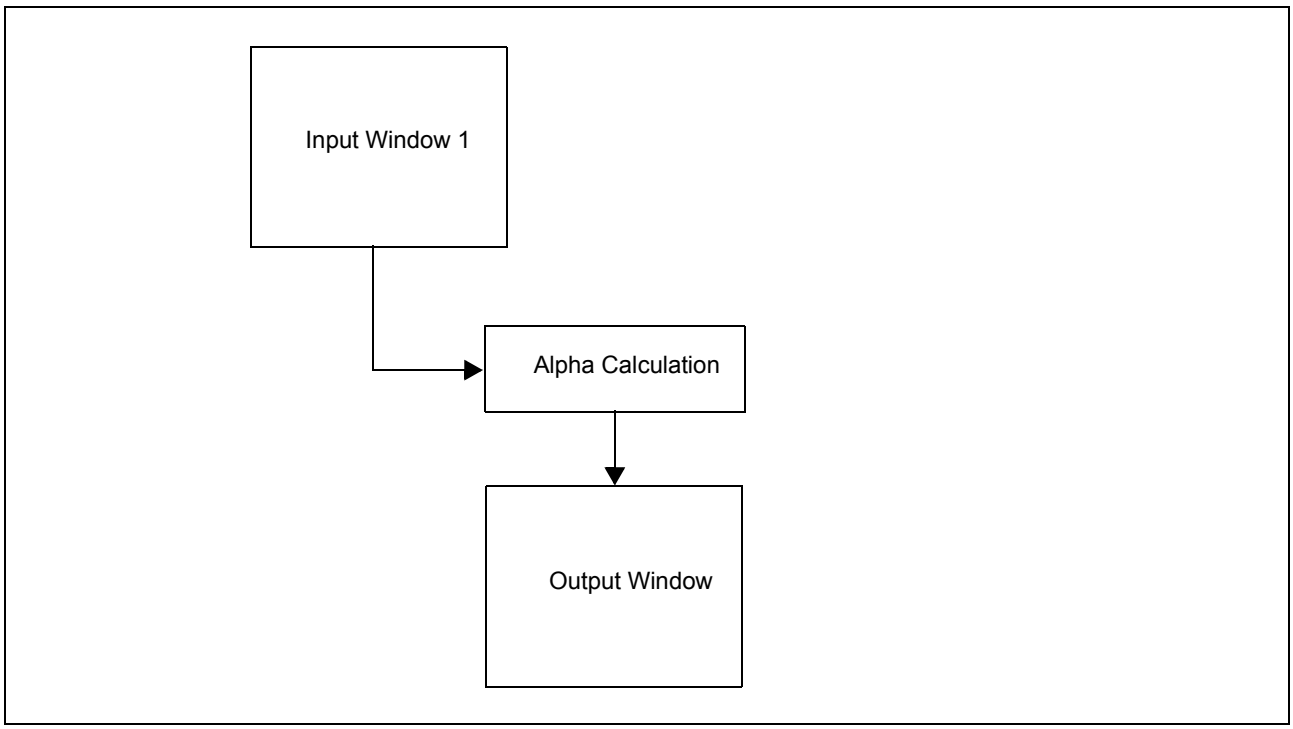


Figure 11-19: Alpha-Blend Data Flow (Copy mode)

11.9.3 Alpha-Blend (Fill mode)

Alpha-Blend can make the output image from the input color. It is possible to make it to the output image by filling programmable color as it is if the alpha value is 32/32.

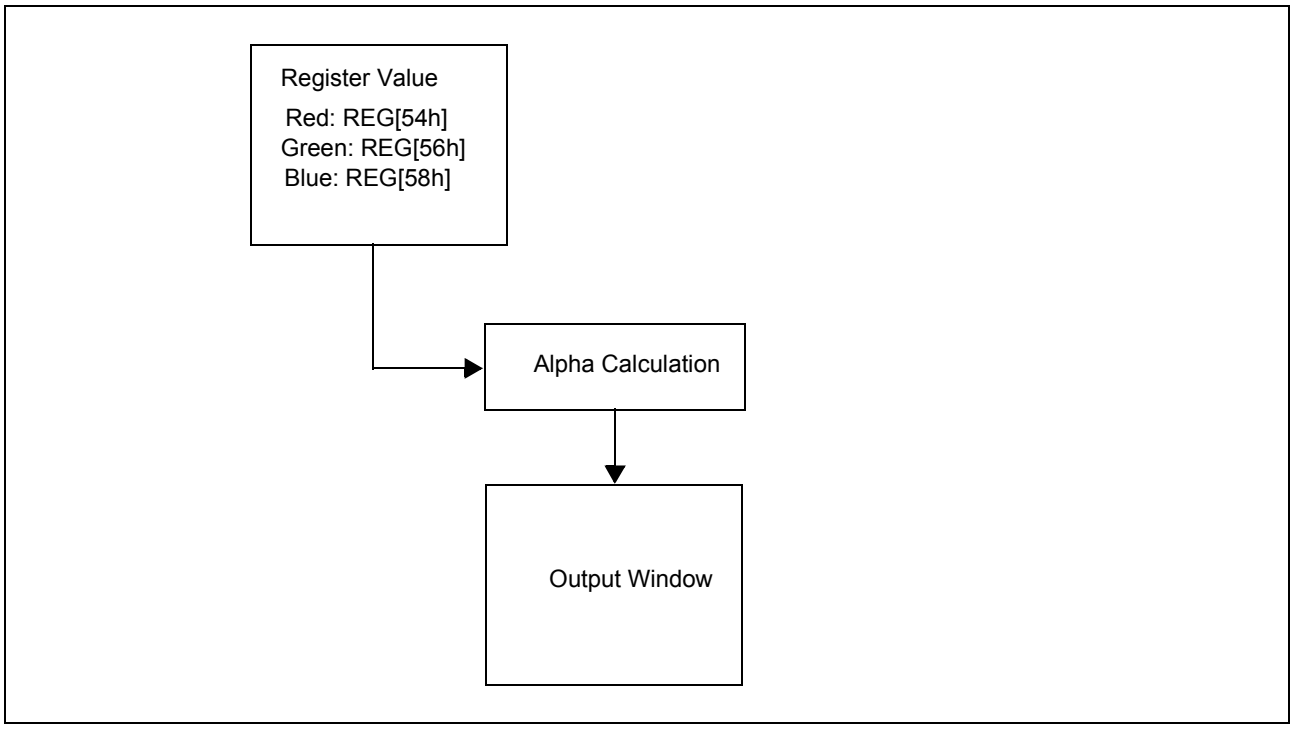


Figure 11-20: Alpha-Blend Data Flow (Fill mode)

11.9.4 Alpha-Blend Window Setting

The image size of Alpha-Blend can be set by X/Y parameters. It is necessary to set the horizontal image size by a multiple of eight. Moreover, the position of beginning the memory of the Blending window can be set by every eight pixels/one line in the SDRAM.

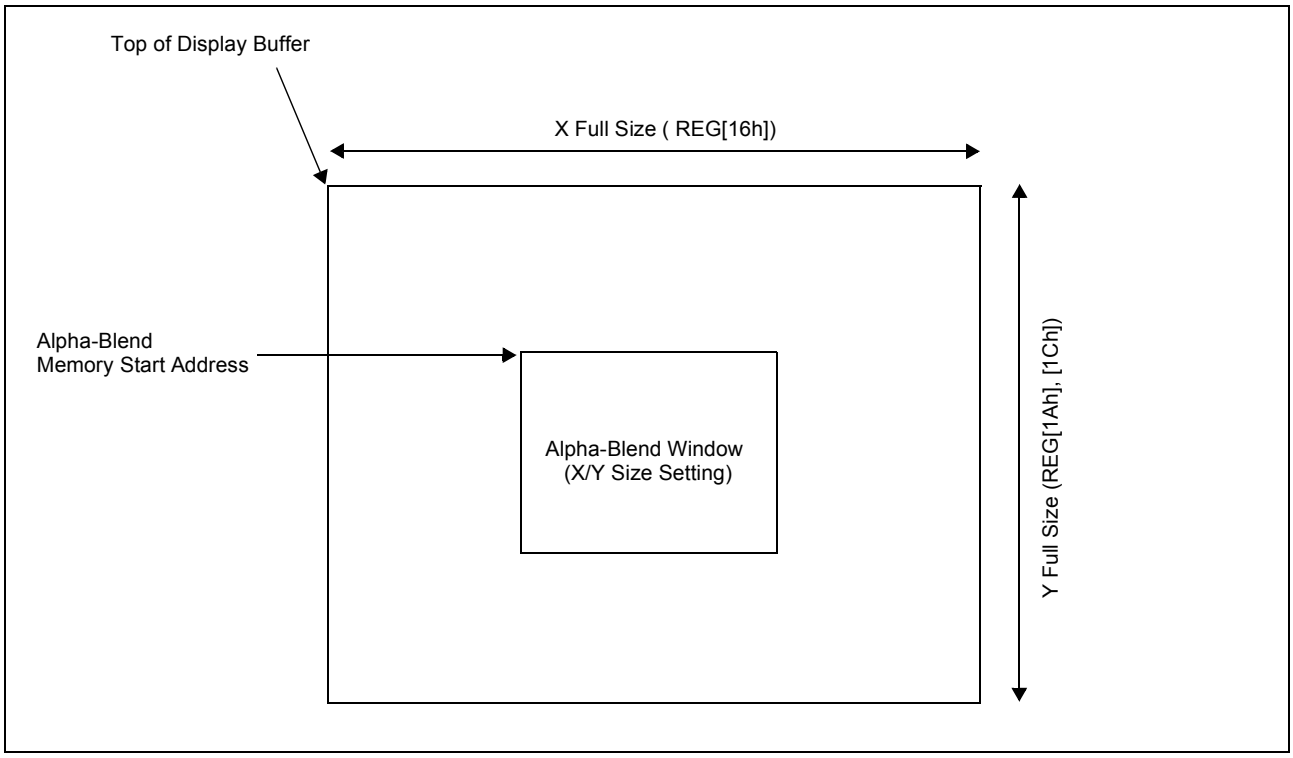


Figure 11-21: Alpha-Blend Window Setting

11.9.5 Alpha-Blend Start Setting

Alpha-blend has two modes, manual mode and auto mode. In manual mode, the operation start and the alpha value changes must be set by software every time.

In auto mode, when the Alpha-blend processing ends, the alpha value is automatically incremented (or decremented) and the next operation will start synchronizing with vertical display period. When the area of the Alpha-blend output window is set the same area with the PIP window, the display image of the alpha-blend is automatically changed. When the image size is too large, image tearing can occur because the alpha-blend has not finished within a frame. This function can be used for a small size images which the alpha blend can finish within a VNDP.

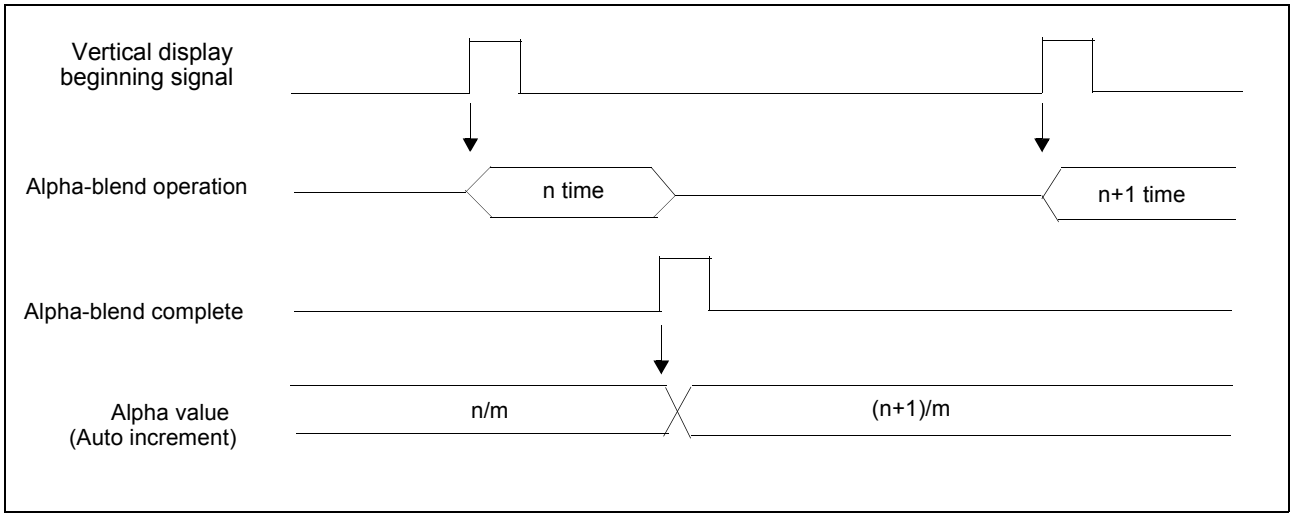


Figure 11-22: Alpha-Blend Start Setting

11.9.6 Alpha-Blend Process Time

The Alpha-Blend processing time changes depending on the SDCLK frequency because the Alpha-Blend utilizes unused SDRAM memory.

11.10 Gamma Correction Look-up Table

Gamma correction is used to correct for the nonlinear relationship between luminance and brightness in an image. The S1D13U11 applies the gamma correction from the look-up table to the data from the display FIFO. The look-up table data cannot be changed when Gamma correction is enabled (REG[B8h] bit 0 = 1b).

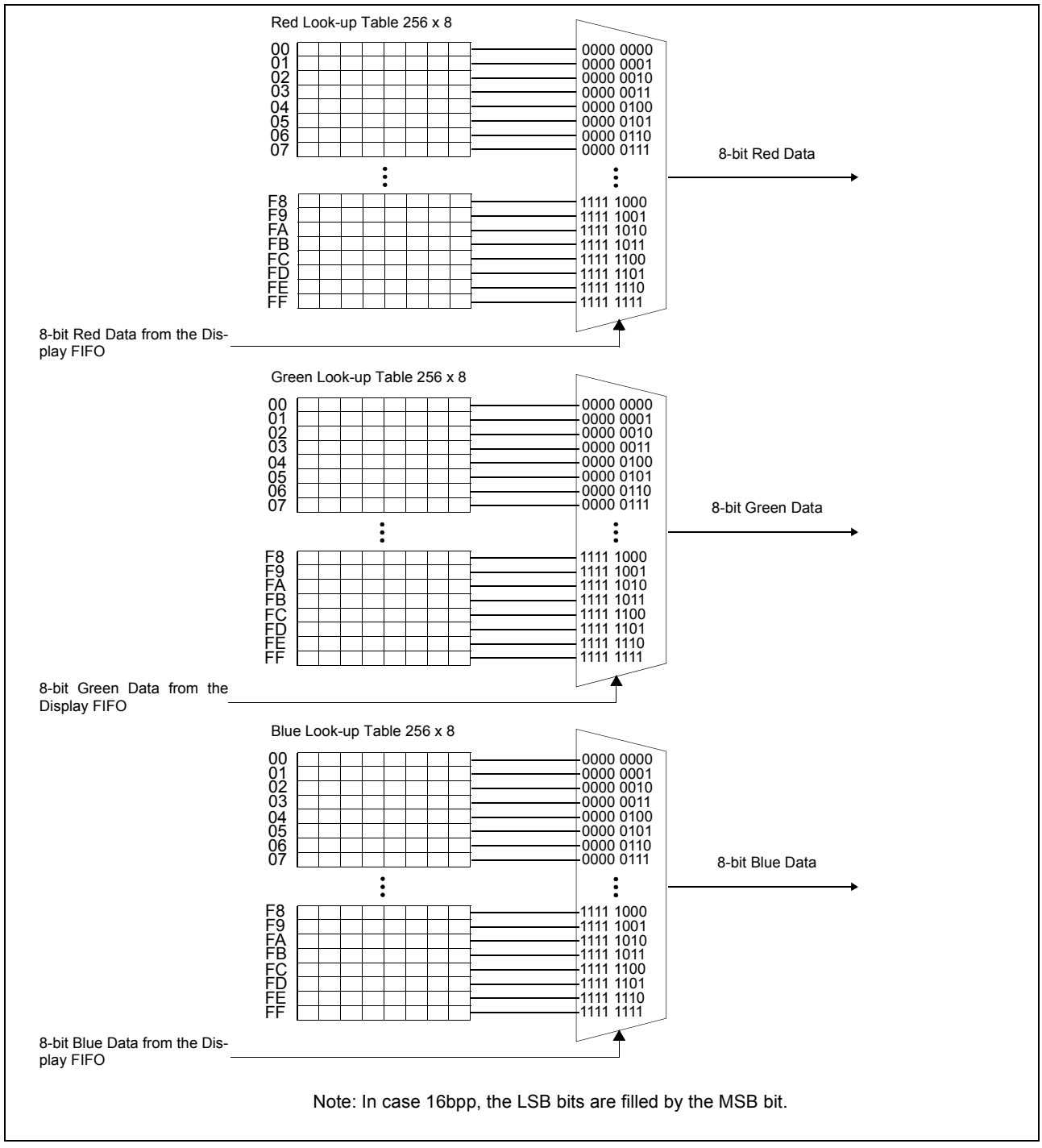


Figure 11-23: Gamma Correction

11.11 Brightness Correction

The S1D13U11 applies brightness correction to the data from the display FIFO. The register setting can be changed asynchronously, with the changes becoming effective in the next vertical display period.

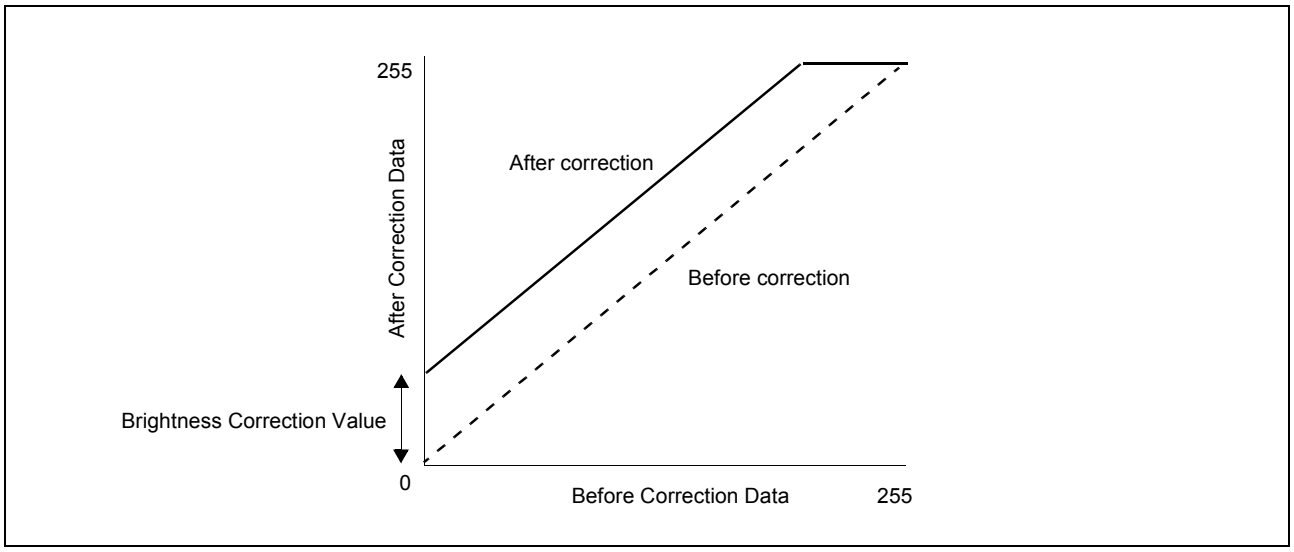


Figure 11-24: Brightness Correction

11.12 Contrast Correction

The S1D13U11 applies contrast correction to the data from the display FIFO. The register setting can be changed asynchronously, new data becomes effective synchronizing with the next vertical display period.

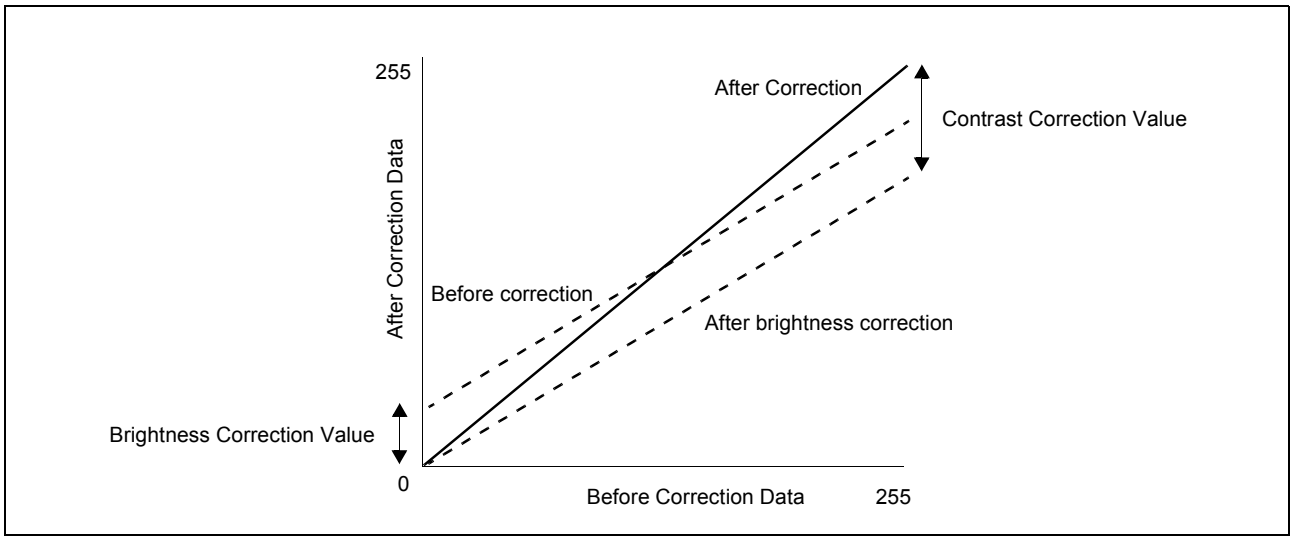


Figure 11-25: Contrast Correction

11.13 SDRAM Interface

The SDRAM interface accesses external 16/64/128 Mbit single data rate SDRAM effectively by using bank interleave. The initialization sequence and the auto refresh cycle are executed within hardware.

11.13.1 SDRAM Initialization

SDRAM must be initialized after resetting hardware. After hardware is reset, an initialization command can be executed only once. The command is ignored after initialization.

The initialization sequence is as follows.

1. Set the size setting register (REG[82h] bits 1-0) according to the memory size of SDRAM used.
2. Set the Auto Refresh Enable bit (REG[84h] bit 7) to 1b and the SDRAM Initialization bit (REG[84h] bit 1) to 1b.

Steps 3 through 6 are automatically executed in hardware.

3. SDRAM initialization start.
4. Precharge all commands are issued.
5. The auto refresh command is issued ten times.
6. The MRS command is issued. (The setting of the MRS register is unnecessary.)
7. Poll the initialization status bit (REG[86h] bit 1) with software until the bit = 1b (initialization end) or wait the processing time of steps 3 through 6 (30,000 clocks of SDCLK).
8. SDRAM can now be used.

11.13.2 SDRAM Connection

When a 16M bit SDRAM is used, the MBA0 pin is connected to the bank signal of the SDRAM.

When the MBA0 and MA11 pins are not used, they must be left unconnected.

Table 11-3: SDRAM Connection

Pin Name	16M bit	64/128M bit
MBA1	not use	MBA1
MBA0	MA11 (Bank select)	MBA0
MA11	not use	MA11

11.13.3 MRS Command

The setting of the mode register of SDRAM command (MRS) is automatically executed by hardware in the initialization sequence. S1D13U11 is set as follows.

Table 11-4: MRS Setting

MRS	Setting Value
Burst Length	4
Lap Type	Sequential
CAS Latency	2
Option	All “0”

11.13.4 Read / Write Command

Read/Write of SDRAM is accessed respectively by the bank interleave every four bursts. Auto precharge is always enabled (MA10 = Low), and the CAS latency is fixed to two.

11.13.5 Auto Refresh Command

Auto refreshing of SDRAM is automatically executed by hardware by an internal refreshing counter. Set the value of the refresh cycle counter according to the clock frequency of SDRAM used. When the clock frequency is 66MHz or higher, it is not necessary to change the register from the default value.

11.13.6 Self Refresh Command

The SDRAM self-refresh is enabled/disabled with the SDRAM Self Refresh Enable bit (REG[84h] bit 3) by software. This command must be set when SDRAM controller is idle status (REG[86h] bit 6 = 1b).

11.13.7 Power Down Command

The SDRAM power save can be enabled/disabled by the SDRAM Power Save Enable bit (REG[84h] bit 2) by software. This command must be set when SDRAM controller is idle status (REG[86h] bit 6 = 1b).

11.13.8 Controller Status

The status of the SDRAM controller is indicated by bit REG[86h] bit 6. If the SDRAM controller is move to the idle status (REG[86h] bit 6 = 1b), it is necessary to stop the access to SDRAM with disabling LCD display (REG[2Ah] bit 0 = 0b) and Alpha-Blend (REG[9Eh] bit 7 = 0b). Please put the SDRAM controller into power save state before disabling SDCLK for power saving (REG[68h] bit 0 = 0b).

11.13.9 Memory Data

The input image is stored in memory as 24bpp or 16bpp.

The data format stored in SDRAM is as follows.

Table 11-5: 24bpp Display (RGB 8:8:8 Input Data)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0000h	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
0002h	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0
0004h	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0
0006h	G_2^7	G_2^6	G_2^5	G_2^4	G_2^3	G_2^2	G_2^1	G_2^0	B_2^7	B_2^6	B_2^5	B_2^4	B_2^3	B_2^2	B_2^1	B_2^0

Table 11-6: 24bpp Display (RGB 5:6:5 Input Data)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0000h	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^7	G_0^6	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^7	B_0^6	B_0^5
0002h	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^7	B_1^6	B_1^5	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^7	R_0^6	R_0^5
0004h	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^7	R_1^6	R_1^5	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^7	G_1^6
0006h	G_2^7	G_2^6	G_2^5	G_2^4	G_2^3	G_2^2	G_2^7	G_2^6	B_2^7	B_2^6	B_2^5	B_2^4	B_2^3	B_2^7	B_2^6	B_2^5

Table 11-7: 16bpp Display (RGB 8:8:8 / RGB 5:6:5 Input Data)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0000h	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3
0002h	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3
0004h	R_2^7	R_2^6	R_2^5	R_2^4	R_2^3	G_2^7	G_2^6	G_2^5	G_2^4	G_2^3	G_2^2	B_2^7	B_2^6	B_2^5	B_2^4	B_2^3
0006h	R_3^7	R_3^6	R_3^5	R_3^4	R_3^3	G_3^7	G_3^6	G_3^5	G_3^4	G_3^3	G_3^2	B_3^7	B_3^6	B_3^5	B_3^4	B_3^3

11.13.10 Memory Address

If the memory address of an image in SDRAM must be entered into the registers to use the display or the Alpha-Blend function, the following method should be used to calculate the memory address.

Image data is arranged in SDRAM using three bytes for each pixel (see <cross-reference to section 13.4>). To determine the address of an image, the top left corner of the image must be calculated based on the X/Y start coordinates of the image data using the following formula. The memory address must be specified as a byte address.

Image address = buffer n + (Ystart x HDW x 3 bytes) + (Xstart x 3 bytes)

Where:

- Buffer n is the memory start address of the write buffer containing the image data. The address is calculated based on the SDRAM Write Buffer Memory Size in REG[90h]
- Ystart is the Y coordinate of the start of the image data relative to the start of write buffer n
- HDW is the horizontal display width as defined by REG[16h]
- Xstart is the X coordinate of the start of the image data relative to the start of write buffer n

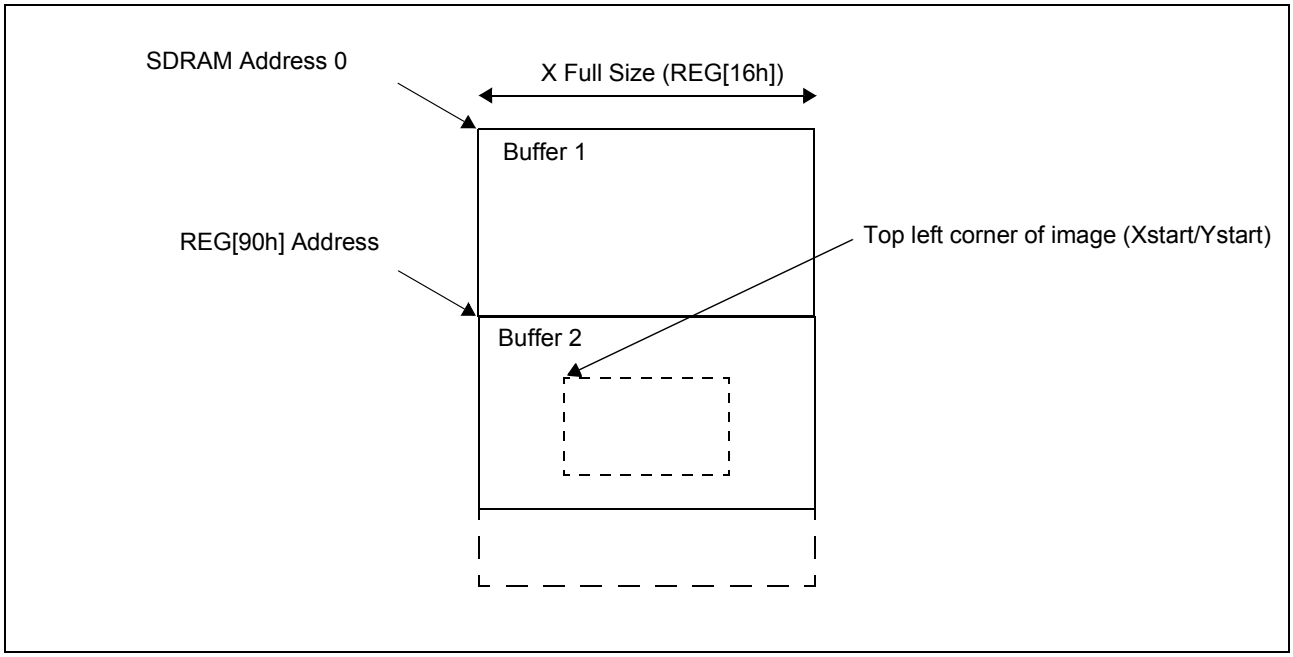


Figure 11-26: Image Address in Memory

11.13.11 SDRAM System Performance

The SDRAM memory is used by the LCD interface (LCD panel refreshing), the USB interface (image writing) and Alpha-Blend. The priority level for memory access is SDRAM refresh, the LCD interface, the USB interface, and Alpha-blend.

The usable data rate of SDRAM is show in the following tables. The SDRAM refresh and the access penalty are considered as 10%.

Table 11-8: SDRAM Usable Data Rate

SDRAM Clock	Usable Data rate
96MHz	192M bytes/sec * 90%
90MHz	180M byes/sec * 90%
84MHz	168M bytes/sec * 90%
78MHz	156M bytes/sec * 90%
72MHz	144M bytes/sec * 90%
66MHz	132M bytes/sec * 90%

The consumption data rate of SDRAM is show in the following tables.

Table 11-9: SDRAM Consumption Data Rate

Priority Order	Circuit	Operation Condition	Peak Rate
1	SDRAM Refresh	Auto refresh cycle	-
2	LCD Interface	16bpp, no overlay display	f_{LCLK} * 2 bytes/sec
		16bpp, overlay display	f_{LCLK} * 4 bytes/sec
		24bpp, no overlay display	f_{LCLK} * 3 bytes/sec
		24bpp, overlay display	f_{LCLK} * 6 bytes/sec
		no display period	0
3	USB Interface	Access	60M bytes/sec
		No access	0
4	Alpha-blend	-	f_{SDCLK} * 2 bytes/sec

When the consumption data rate nears the usable data rate, the following phenomenons will occur. When the overlay display is enabled, the clock ratio of SDCLK vs. PCLK must be considered for the target system.

Table 11-10: Phenomenon

Circuit	Phenomenon
USB Interface	Data write operation is waiting for NAK response.
Alpha-blend	It takes time to execute Alpha-blend.

11.14 PWM Output

PWM output can be used for the backlight control of the LCD panel. The high and low pulse width are set to the system clock (LCDCLK) with a 32 bit counter. REG 70h bit 7 is used to update the PWM registers once they have been set.

To stop PWM output, disable the PWM (REG[70h] bit 2 = 0b) after ensuring the logic level of the output by setting REG[70h] bits 1-0.

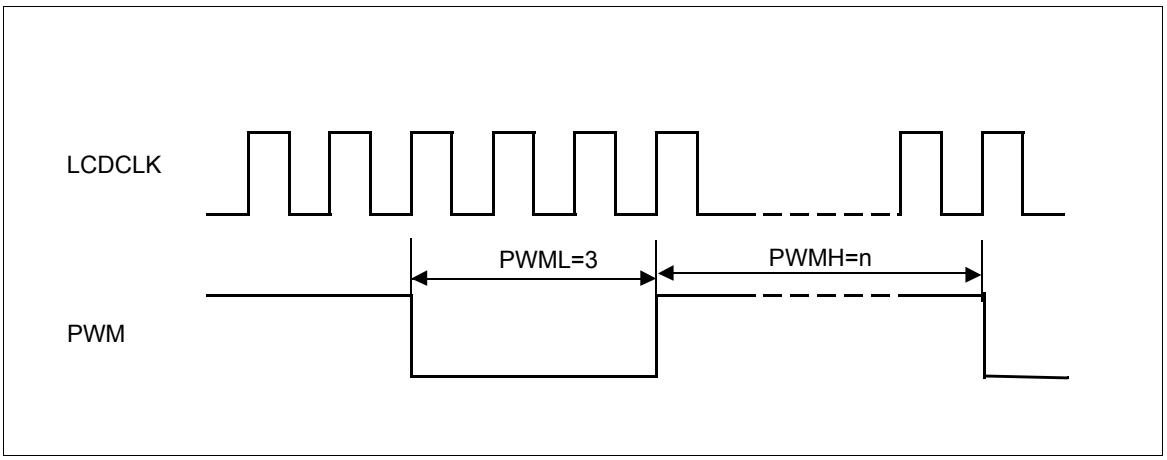


Figure 11-27: PWM Timing Example

11.15 LCD Interface Interrupt

The following Figure shows the block diagram of the LCD interface interrupt.

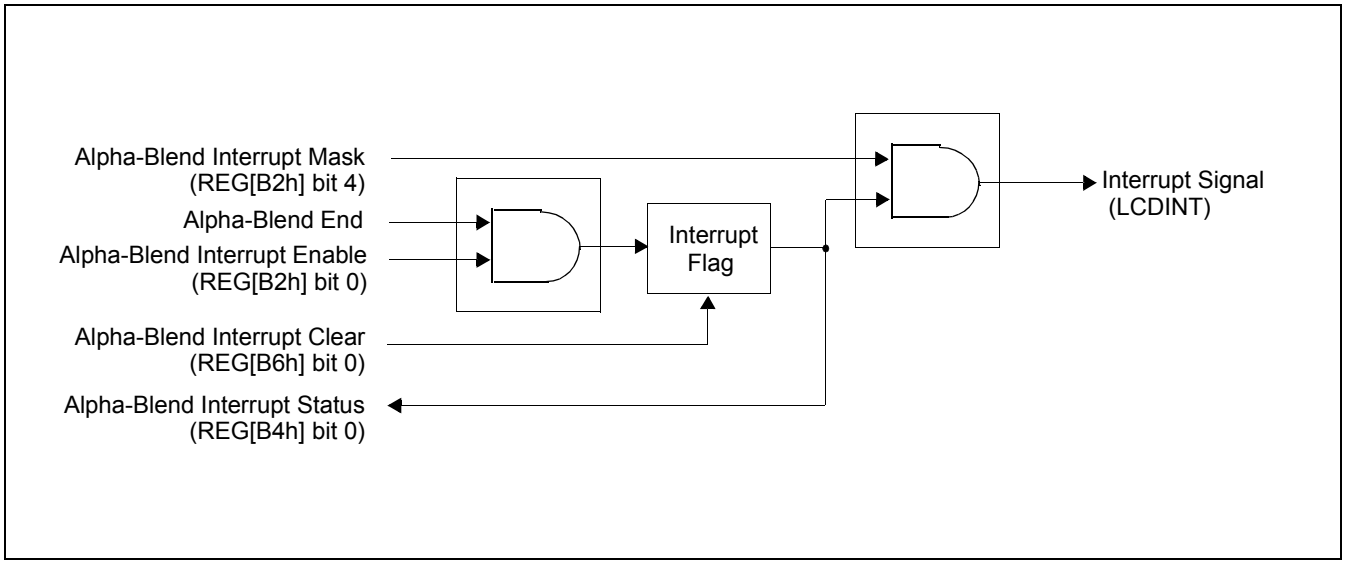


Figure 11-28: LCD Interface Interrupt Block Diagram

11.16 Color Bar Display Test

The color bar display test does not use the SDRAM memory and is selected when REG[2Ah] bits 3-1 = 111b

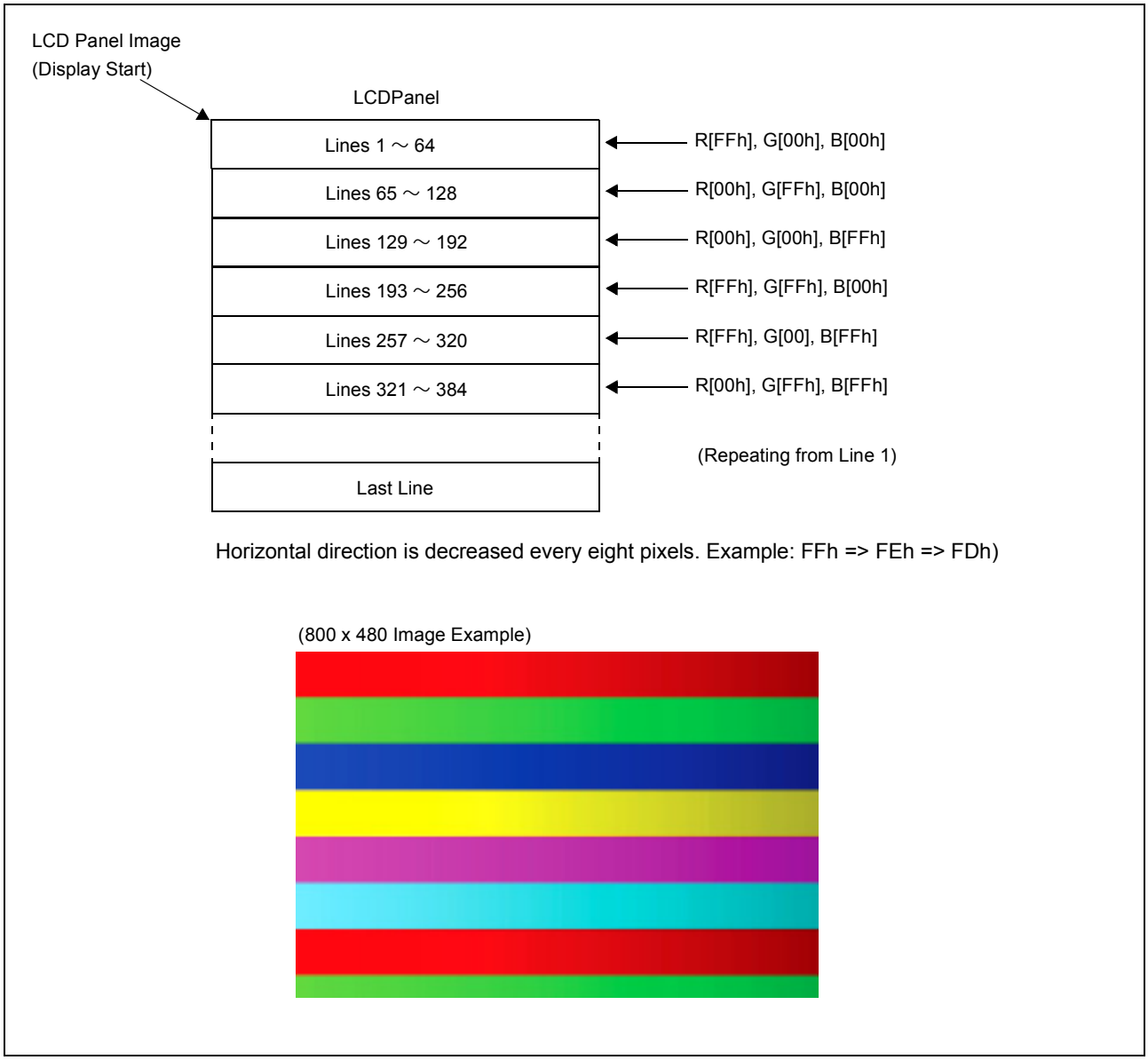


Figure 11-29: Color Bar Display Test

11.17 LCD Interface Registers

The LCD interface registers are listed in the following table.

All reserved bits must be set to the default value. Writing a non-default value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect. Unless specified otherwise, all register bits are set to 0b during power-on reset.

Table 11-11: LCD Interface Register Set

Register	Pg	Register	Pg
Read-Only Configuration Registers			
REG[00h] Product Code Register	96	REG[02h] Configuration Readback Register	96
Clock Configuration Registers			
REG[04h] PLL D-Divider Register	97	REG[06h] PLL Setting Register 0	97
REG[08h] through REG[0Ah] are Reserved	97		
REG[0Ch] PLL Setting Register 1	98	REG[0Eh] SS Control Register 0	99
REG[10h] SS Control Register 1	99	REG[12h] Clock Source Select Register	100
Panel Configuration Registers			
REG[14h] LCD Panel Type Register	102	REG[16h] Horizontal Display Width Register (HDISP)	103
REG[18h] Horizontal Non-Display Period Register (HNDP)	103	REG[1Ah] Vertical Display Height Register 0 (VDISP)	103
REG[1Ch] Vertical Display Height Register 1 (VDISP)	103	REG[1Eh] Vertical Non-Display Period Register (VNDP)	104
REG[20h] PHS Pulse Width Register (HSW)	104	REG[22h] PHS Pulse Start Position Register (HPS)	104
REG[24h] PVS Pulse Width Register (VSW)	105	REG[26h] PVS Pulse Start Position Register (VPS)	105
REG[28h] PCLK Polarity Register	105		
Display Mode Register			
REG[2Ah] Display Mode Register	106	REG[2Ch] PIP1 Display Start Address Register 0	108
REG[2Eh] PIP1 Display Start Address Register 1	108	REG[30h] PIP1 Display Start Address Register 2	108
REG[32h] PIP1 Window X Start Position Register	108	REG[34h] PIP1 Window Y Start Position Register 0	109
REG[36h] PIP1 Window Y Start Position Register 1	109	REG[38h] PIP1 Window X End Position Register	109
REG[3Ah] PIP1 Window Y End Position Register 0	110	REG[3Ch] PIP1 Window Y End Position Register 1	110
REG[3Eh] PIP2 Display Start Address Register 0	110	REG[40h] PIP2 Display Start Address Register 1	110
REG[42h] PIP2 Display Start Address Register 2	110	REG[44h] PIP2 Window X Start Position Register	111
REG[46h] PIP2 Window Y Start Position Register 0	111	REG[48h] PIP2 Window Y Start Position Register 1	111
REG[4Ah] PIP2 Window X End Position Register	112	REG[4Ch] PIP2 Window Y End Position Register 0	112
REG[4Eh] PIP2 Window Y End Position Register 1	112	REG[50h] Display Control Register	113
Input Mode Registers			
REG[52h] Input Mode Register	114	REG[54h] Transparency Key Color Red Register	115
REG[56h] Transparency Key Color Green Register	115	REG[58h] Transparency Key Color Blue Register	116
REG[5Ah] Write Window X Start Position Register	116	REG[5Ch] Write Window Y Start Position Register 0	116
REG[5Eh] Write Window Y Start Position Register 1	116	REG[60h] Write Window X End Position Register	117
REG[62h] Write Window Y End Position Register 0	117	REG[64h] Write Window Y End Position Register 1	117
Memory Access			
REG[66h] Memory Data Port Register 0	118	REG[67h] Memory Data Port Register 1	118
Miscellaneous Registers			
REG[68h] Power Save Register	119	REG[6Ah] Non-Display Period Control / Status Register	120
General Purpose Output Pins Registers			
REG[6Ch] is Reserved	121	REG[6Eh] General Purpose Output Register	121

Table 11-11: LCD Interface Register Set (Continued)

Register	Pg	Register	Pg
PWM Registers			
REG[70h] PWM Control Register	122	REG[72h] PWM High Duty Cycle Register 0	123
REG[74h] PWM High Duty Cycle Register 1	123	REG[76h] PWM High Duty Cycle Register 2	123
REG[78h] PWM High Duty Cycle Register 3	123	REG[7Ah] PWM Low Duty Cycle Register 0	124
REG[7Ch] PWM Low Duty Register 1	124	REG[7Eh] PWM Low Duty Register 2	124
REG[80h] PWM Low Duty Register 3	124		
SDRAM Control Registers			
REG[82h] SDRAM Control Register 0	125	REG[84h] SDRAM Status Register 0	125
REG[86h] SDRAM Status Register 1	126	REG[88h] SDRAM MRS Value Register 0	127
REG[8Ah] SDRAM MRS Value Register 1	127	REG[8Ch] SDRAM Refresh Counter Register 0	127
REG[8Eh] SDRAM Refresh Counter Register 1	127	REG[90h] SDRAM Write Buffer Memory Size Register 0	128
REG[92h] SDRAM Debug Register	128		
Alpha-Blend Registers			
REG[94h] Alpha-Blend Control Register	130	REG[96h] is Reserved	130
REG[98h] Alpha-Blend Horizontal Size Register	131	REG[9Ah] Alpha-Blend Vertical Size Register 0	131
REG[9Ch] Alpha-Blend Vertical Size Register 1	131	REG[9Eh] Alpha-Blend Value Register	132
REG[A0h] Alpha-Blend Input Image 1 Start Address Register 0	133	REG[A2h] Alpha-Blend Input Image 1 Start Address Register 1	133
REG[A4h] Alpha-Blend Input Image 1 Start Address Register 2	133	REG[A6h] Alpha-Blend Input Image 2 Start Address Register 0	134
REG[A8h] Alpha-Blend Input Image 2 Start Address Register 1	134	REG[AAh] Alpha-Blend Input Image 2 Start Address Register 2	134
REG[ACh] Alpha-Blend Output Image Start Address Register 0	134	REG[AEh] Alpha-Blend Output Image Start Address Register 1	134
REG[B0h] Alpha-Blend Output Image Start Address Register 2	134		
Interrupt Registers			
REG[B2h] Interrupt Control Register	135	REG[B4h] Interrupt Status Register	135
REG[B6h] Interrupt Clear Register	135		
Display Enhancement Registers			
REG[B8h] Display Enhancement Control Register	136	REG[BAh] Gamma Correction Table Index Register	137
REG[BCh] Gamma Correction Table Data Register	137	REG[BEh] Brightness Correction Red Register 0	137
REG[C0h] Brightness Correction Red Register 1	137	REG[C2h] Brightness Correction Green Register 0	138
REG[C4h] Brightness Correction Green Register 1	138	REG[C6h] Brightness Correction Blue Register 0	138
REG[C8h] Brightness Correction Blue Register 1	138	REG[CAh] Contrast Correction Red Register	139
REG[CCh] Contrast Correction Green Register	139	REG[CEh] Contrast Correction Blue Register	139
Display Extend Registers			
REG[E0h] Extend Display Control Register	140	REG[E2h] Virtual Display Horizontal Width Register 0	140
REG[E4h] Virtual Display Horizontal Width Register 1	140	REG[E6h] SDRAM Read Register	141
REG[E8h] SDRAM Read Start Address Register 0	141	REG[EAh] SDRAM Read Start Address Register 1	141
REG[ECh] SDRAM Read Start Address Register 2	141	REG[EEh] SDRAM Dummy Read Port Register	141

11.17.1 Read-Only Configuration Registers

REG[00h] Product Code Register
Default = BCh — Read Only

Product Code bits 5-0						Revision Code bits 1-0	
7	6	5	4	3	2	1	0

bits 7-2 Product Code bits [5:0] (Read Only)
These read-only bits indicate the product code. The product code for the S1D13U11 is 101111b.

bits 1-0 Revision Code bits [1:0] (Read Only)
These read-only bits indicates the revision code. The revision code is 00b.

REG[02h] Configuration Readback Register
Default = xxh — Read Only

n/a					CNF2 Status	CNF1 Status	CNF0 Status
7	6	5	4	3	2	1	0

bits 2-0 CNF[2:0] Status (Read Only)
These read-only status bits return the status of the configuration pins CNF[2:0]. For details on CNF[2:0] functionality, see Section 5.4, “Configuration Options” on page 30.

11.17.2 Clock Configuration Registers

REG[04h] PLL D-Divider Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PLL Enable	n/a						PLL Input Clock Select

bit 7 PLL Enable
This bit enables the PLL output.
When this bit = 0, the PLL is disabled.
When this bit = 1, the PLL is enabled.

Note
All other PLL registers must be set before enabling SS or PLL. SDCLK must be disabled (REG[68h] bit 0 = 0b) before changing the value of this bit. Do not change this bit while operating.

bit 0 PLL Input Clock Select
This bit determines the input clock to the PLL. This bit must be set before enabling PLL.
When this bit = 0, the OSC frequency is 12MHz.
When this bit = 1, the OSC frequency is 24MHz.

REG[06h] PLL Setting Register 0
Default = 3Ah — Read/Write

7	6	5	4	3	2	1	0
Reserved			VC bit	Reserved			

bits 7-5 Reserved
The default value for these bits are 001b.

bit 4 VC bit
This bit sets the range of the PLL frequency.

Table 11-12: VC Selection

REG[06h] Bit 4	PLL Frequency
0b	66 ~ 78MHz
1b	84 ~ 96MHz

bits 3-0 Reserved
The default value for these bits are 1010b.

REG[08h] through REG[0Ah] are Reserved

These registers are Reserved and should not be written.
The default value for these registers are 01h and 00h respectively.

REG[0Ch] PLL Setting Register 1
Default = 0Fh — Read/Write

n/a				PLL Output Clock Select bits 3-0			
7	6	5	4	3	2	1	0

bits 3-0 PLL Output Clock Select bits [3:0]
These bits are used to configure the PLL output clock frequency.

Table 11-13: PLL Output Clock Selection

REG[0Ch] Bit 3-0	PLL Frequency
1010b	66MHz
1011b	72MHz
1100b	78MHz
1101b	84MHz
1110b	90MHz
1111b	96MHz (default)
Other	don't use

REG[0Eh] SS Control Register 0
Default = 00h Read/Write

Spread Spectrum Enable	n/a						
7	6	5	4	3	2	1	0

bit 7 Spread Spectrum Enable
This bit controls Spread Spectrum (SS) modulation.
When this bit = 0b, SS modulation is disabled.
When this bit = 1b, SS modulation is enabled.

Note
Program the SS setting registers before enabling SS or PLL. The enabling of this bit is synchronized with PLL enable bit (REG[04h] bit 7). The frequency for which SS can not be used in 84 ~ 96MHz.

REG[10h] SS Control Register 1
Default = 55h Read/Write

Reserved	W-Counter bits 2-0			Reserved			
7	6	5	4	3	2	1	0

bit 7 Reserved
The default value for this bit is 0b.

bits 6-4 W-Counter bits [2:0]
These bits set the width of the SS output frequency change.

Table 11-14: W-Counter Selection

REG[10h] bits 6-4	Width of Frequency Change (TYP)
000b	+/- 0.10ns
001b	+/- 0.17ns
010b	+/- 0.23ns
011b	+/- 0.30ns
100b	+/- 0.35ns
101b	+/- 0.42ns (default)
110b	+/- 0.48ns
111b	+/- 0.54ns

bits 3-0 Reserved
The default value for these bits is 0101b.

REG[12h] Clock Source Select Register
Default = 00h — Read/Write

SDCLK Source Select	LCDCLK Divide Select bits 2-0			FOUT Clock Divide Select bits 1-0		SS Clock Select bits 1-0	
7	6	5	4	3	2	1	0

bit 7 SDCLK Source Select

This bit selects the source of the external SDRAM clock (SDCLK) for the S1D13U11. For details on the clock structure see Chapter 8, "Clocks" on page 53.
When this bit = 0b, the SDCLK source is the OSC clock input.
When this bit = 1b, the SDCLK source is the internal PLL.

Note
The PLL output will become stable after 200us.

bits 6-4 LCDCLK Divide Select bits [2:0]

These bits specify the ratio of the dividing frequency for the LCD clock (LCDCLK).

Table 11-15: LCDCLK Divide Selection

REG[12h] bits 6-4	LCDCLK Divide (SDRAM Data Type is 24bpp, Overlay is disabled)	LCDCLK Divide (SDRAM Data Type is 16bpp, Overlay is disabled)	LCDCLK Divide (SDRAM Data Type is 24bpp, Overlay is enabled)	LCDCLK Divide (SDRAM Data Type is 16bpp, Overlay is enabled)
000b	1/3 divide (default)	1/3 divide (default)	reserved	1/3 divide (default)
001b	1/2 divide	1/2 divide	reserved	reserved
010b	1/4 divide	1/4 divide	1/4 divide	1/4 divide
011b	1/6 divide	reserved	1/6 divide	reserved
100b	1/8 divide	reserved	1/8 divide	reserved
101b ~ 111b	reserved	reserved	reserved	reserved

Note
SDCLK must be disabled (REG[68h] bit 0 = 0b) before changing the value of these bits. Please do not change these bits while operating.

bits 3-2 FOUT Clock Divide Select bits [1:0]

These bits specify the ration of dividing frequency of FOUT clock.

Table 11-16: FOUT Clock Divide Selection

REG[12h] bits 3-2	FOUT Clock Divide
00b	no output (default)
01b	1/1 divide
10b	1/2 divide
11b	1/4 divide

bits 1-0 SS Clock Select bits [1:0]
These bits select the using of the SS clock.

Table 11-17: SS Clock Using Selection

REG[12h] bits 1-0	SS Clock Using
00b	SS is not used (default)
01b	LCDCLK
1xb	SDCLK

Note
SDCLK must be disabled (REG[68h] bit 0 = 0b) before changing the value of these bits. Please do not change while operating.

Note
The frequency for which SS can not be used is 84MHz ~ 96MHz.

11.17.3 Panel Configuration Registers

REG[14h] LCD Panel Type Register
Default = 00h — Read/Write

LCD Pin Driver Size	LCD Input Data Endian	SDRAM Data Type	LCD Output Data Width bit 1	n/a	Input Image Format bits 1-0		LCD Output Data Width bit 0
7	6	5	4	3	2	1	0

bit 7 LCD Pin Driver Size
This bit specifies the driver size for the LCD interface.
When this bit = 0b, the LCD interface pins are TYPE2 driver size.
When this bit = 1b, the LCD interface pins are TYPE2S driver size.

bit 6 LCD Input Data Endian
This bit specifies the input data endian for the USB interface.
When this bit = 0b, the input data is the Endian Type 1.
When this bit = 1b, the input data is the Endian Type 2.

bit 5 SDRAM Data Type
This bit specifies the data type for the SDRAM.
When this bit = 0b, the data is stored into the SRAM as 24bpp.
When this bit = 1b, the data is stored into the SDRAM as 16bpp.

Note
There are some limitations when this bit is set for 16bpp, please refer to Table 11-15: "LCDCLK Divide Selection," on page 100 for further information

bits 2-1 Input Image Format bits [1:0]
These bits select the input image format.

Table 11-18: Input Image Format Setting

REG[14h] bits 2-1	Input Data Format
00b	24bpp (RGB 8:8:8) mode 1
01b	24bpp (RGB 8:8:8) mode 2
1xb	16bpp (RGB 5:6:5)

Note
Input image data is always stored in memory as RGB 8:8:8 (REG[14h] bit 5 = 0b) or RGB 5:6:5 (REG[14h] bit 5 = 1b). For details see Section 11.13.9, "Memory Data" on page 88.

bits 4, 0 LCD Output Data Width bits [1:0]
These bits specify the data width for the LCD interface.

Table 11-19: Output Data Width Setting

REG[14h] bits 4, 0	Output Data Width
00b	24bit
01b	18bit
1xb	16bit

REG[16h] Horizontal Display Width Register (HDISP)
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a	Horizontal Display Width bits 6-0						

bits 6-0 Horizontal Display Width bits [6:0]
These bits specify the Horizontal Display Width (HDISP) for the LCD panel, in 8 pixel resolution (bytes).

HDISP in number of pixels = ((REG[16h] bits 6-0) + 1)× 8

Note
The minimum Horizontal Display Width is 32 pixels and the maximum is 960 pixels.

REG[18h] Horizontal Non-Display Period Register (HNDP)
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Horizontal Non-Display Period bits 7-0							

bits 7-0 Horizontal Non-Display Period bits [7:0]
These bits specify the Horizontal Non-Display Period (HNDP) for the LCD panel, in pixels.

HNDP in pixels = ((REG[18h] bits 7-0) + 1) x 2

Note
The minimum Horizontal Non-Display Period is 4 pixels and the maximum is 512 pixels.

HPS + HSW <= HNDP

REG[1Ah] Vertical Display Height Register 0 (VDISP)
Default = 01h — Read/Write

7	6	5	4	3	2	1	0
Vertical Display Height bits 7-0							

REG[1Ch] Vertical Display Height Register 1 (VDISP)
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						Vertical Display Height bits 9-8	

REG[1Ch] bits 1-0
REG[1Ah] bits 7-0 Vertical Display Height bits [9:0]
These bits specify the Vertical Display Height (VDISP) for the LCD panel, in lines.

VDISP in lines = (REG[1Ch] bits 1-0, REG[1Ah] bits 7-0) +1

Note
The minimum Vertical Display Height is 32 lines and the maximum is 960 lines.

REG[1Eh] Vertical Non-Display Period Register (VNDP)
Default = 01h — Read/Write

Vertical Non-Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Vertical Non-Display Period bits [7:0]
These bits specify the Vertical Non-Display Period (VNDP) for the LCD panel, in lines.
VNDP in lines = ((REG[1Eh] bits 7-0) + 1) x 2

Note
The minimum Vertical Non-Display Period is 4 lines and the maximum is 512 lines.

REG[20h] PHS Pulse Width Register (HSW)
Default = 00h — Read/Write

PHS Pulse Polarity	PHS Pulse Width bits 6-0						
7	6	5	4	3	2	1	0

bit 7 PHS Pulse Polarity
This bit selects the polarity of the horizontal sync signal. This bit is set according to the horizontal sync signal of the panel.
When this bit = 0b, the horizontal sync signal is active low.
When this bit = 1b, the horizontal sync signal is active high.

bits 6-0 PHS Pulse Width bits [6:0]
These bits specify the width of the horizontal sync signal for the LCD panel (HSW), in pixels. The horizontal sync signal is typically PHS, depending on the panel type.
HSW in pixels = (REG[20h] bits 6-0) + 1

REG[22h] PHS Pulse Start Position Register (HPS)
Default = 00h — Read/Write

n/a	PHS Pulse Start Position bits 6-0						
7	6	5	4	3	2	1	0

bits 6-0 PHS Pulse Start Position bits [6:0]
These bits specify the start position of the horizontal sync signal with respect to the start of Horizontal Non-Display period, in pixels.
HPS in pixels = (REG[22h] bits 6-0)

REG[24h] PVS Pulse Width Register (VSW)
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PVS Pulse Polarity	n/a	PVS Pulse Width bits 5-0					

bit 7 PVS Pulse Polarity
This bit selects the polarity of the vertical sync signal. This bit is set according to the vertical sync signal of the panel.
When this bit = 0b, the vertical sync signal is active low.
When this bit = 1b, the vertical sync signal is active high.

bits 5-0 PVS Pulse Width bits [5:0]
These bits specify the width of vertical sync signal (VSW) for the LCD panel, in lines. The vertical sync signal is typically PVS, depending on the panel type.
VSW in lines = (REG[24h] bits 5-0) + 1

REG[26h] PVS Pulse Start Position Register (VPS)
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PVS Pulse Start Position bits 7-0							

bits 7-0 PVS Pulse Start Position bits [7:0]
These bits specify the start position of the vertical sync signal with respect to the start of Vertical Non-Display period (VPS), in lines.
VPS in lines = REG[26h] bits 7-0

REG[28h] PCLK Polarity Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PCLK Polarity	n/a						

bit 7 PCLK Polarity
This bit selects the polarity of PCLK.
When this bit = 0b, data is output on the rising edge of PCLK.
When this bit = 1b, data is output on the falling edge of PCLK.

11.17.4 Display Mode Register

REG[2Ah] Display Mode Register Default = 00h							Read/Write
Main Window Display Buffer Select bits 3-0				Display Data Output Select bits 1-0			Display Interface Enable
7	6	5	4	3	2	1	0

All changes, except to bit 0, entered into this register are not loaded into internal registers until REG[50h] bit 7 has been written with a 1b. Bit 0 is not synchronized with REG[50h] bit 7.

bits 7-4 Main Window Display Buffer Select bits [3:0]
When the double buffer display is not selected, these bits select the display buffer of the main window.
When the double buffer display is selected (REG[2Ah] bits 3-1 = 001b), these bit are ignored. (Buffer 1 and 2 are fixed)

Table 11-20: Main Window Display Buffer Selection

REG[2Ah] bits 7-4	Main Window Display Buffer
0000b	Buffer 1
0001b	Buffer 2
0010b	Buffer 3
0011b	Buffer 4
0100b	Buffer 5
0101b	Buffer 6
0110b	Buffer 7
0111b	Buffer 8
1000b	Buffer 9
1001b	Buffer 10
1010b	Buffer 11
1011b	Buffer 12
1100b	Buffer 13
1101b	Buffer 14
1110b	Buffer 15
1111b	Buffer 16

bits 3-1 Display Data Output Select bits [2:0]
These bits are selected the display data. These bits can be update on LCD running.

Table 11-21: Display Data Output Selection

REG[2Ah] bits 3-1	Display Data Output
000b	Single buffer display (default)
001b	Double buffer display
010b	PIP1 window display
011b	PIP2 window display
100b	PIP1 and PIP2 window display
101b	Display blanked (all lows output)
110b	Display blanked (all highs output)
111b	Test color bar display

bit 0 Display Interface Enable
Changes to this bit are not synchronized with REG[50h] bit 7 and occur immediately.
When this bit = 0b, the LCD display interface is disabled.
When this bit = 1b, the LCD display interface is enabled. The SDCLK should be enabled (REG[68h] bit 0 = 1b) before the LCD display interface is enabled.

REG[2Ch] PIP1 Display Start Address Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP1 Display Start Address bits 7-3					n/a		

REG[2Eh] PIP1 Display Start Address Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP1 Display Start Address bits 15-8							

REG[30h] PIP1 Display Start Address Register 2
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP1 Display Start Address bits 23-16							

REG[30h] bits 7-0
REG[2Eh] bits 7-0
REG[2Ch] bits 7-3 PIP1 Display Start Address bits [23:3]

These bits specify the start address of the PIP1 window image in the display buffer. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP1 Display Start Address [23:3] = (REG[30h] bits 7-0, REG[2Eh] bits 7-0, REG[2Ch] bits 7-3)

REG[32h] PIP1 Window X Start Position Register
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP1 Window X Start Position bits 9-3							n/a

bits 7-1 PIP1 Window X Start Position bits [9:3]

These bits determine the X start position of the PIP1 Window in relation to the origin of the panel, in 8 pixel resolution (bytes). The value entered into this register is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP1 Window X Start Position = (REG[32h] bits 7-0) x 4 + 1

Note

1. The value of this register is incremented by 8 pixels (1, 9, 17, 25, ..., horizontal size - 7).
2. The PIP1 window must be positioned such that it remains within the dimensions of the LCD display.

REG[34h] PIP1 Window Y Start Position Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PIP1 Window Y Start Position bits 9-2							

REG[36h] PIP1 Window Y Start Position Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						PIP1 Window Y Start Position bits 1-0	

REG[34h] bits 7-0
REG[36h] bits 1-0 PIP1 Window Y Start Position bits [9:0]

These bits determine the Y start position of the PIP1 Window in relation to the origin of the panel, in lines. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP1 Window Y Start Position = (REG [34h] bits 7-0, REG [36h] bits 1-0) + 1

Note

The PIP1 window must be positioned such that it remains within the dimensions of the LCD display.

REG[38h] PIP1 Window X End Position Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PIP1 Window X End Position bits 9-3							n/a

bits 7-1 PIP1 Window X End Position bits [9:3]

These bits determine the X end position of the PIP1 Window in relation to the origin of the panel, in 8 pixel resolution (bytes). The value entered into this register is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP1 Window X End Position = (REG[38h] bits 7-0) x 4 + 8

Note

1. The value of this register is incremented by 8 pixels (8, 16, 24, 32, ..., horizontal size)
2. The PIP1 window must be positioned such that it remains within the dimensions of the LCD display.

REG[3Ah] PIP1 Window Y End Position Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP1 Display Window Y End Position bits 9-2							

REG[3Ch] PIP1 Window Y End Position Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a						PIP1 Display Window Y End Position bits 1-0	

REG[3Ah] bits 7-0
REG[3Ch] bits 1-0 PIP1 Window Y End Position bits [9:0]
These bits determine the Y end position of the PIP1 Window in relation to the origin of the panel, in pixels. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP1 Window Y End Position = (REG[3Ah] bits 7-0, REG[3Ch] bits 1-0) + 1

Note
The PIP1 window must be positioned such that it remains within the dimensions of the LCD display.

REG[3Eh] PIP2 Display Start Address Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP2 Display Start Address bits 7-3					n/a		

REG[40h] PIP2 Display Start Address Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP2 Display Start Address bits 15-8							

REG[42h] PIP2 Display Start Address Register 2
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP2 Display Start Address bits 23-16							

REG[42h] bits 7-0
REG[40h] bits 7-0
REG[3Eh] bits 7-3 PIP2 Display Start Address bits [23:3]
These bits specify the start address of the PIP2 window image in the display buffer. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP2 Display Start Address [23:3] = (REG[42h] bits 7-0, REG[40h] bits 7-0, REG[3Eh] bits 7-3)

REG[44h] PIP2 Window X Start Position Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PIP2 Display Window X Start Position bits 9-3							n/a

bits 7-1 PIP2 Window X Start Position bits [9:3]

These bits determine the X start position of the PIP2 Window in relation to the origin of the panel, in 8 pixel resolution (bytes). The value entered into this register is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP2 Window X Start Position = (REG[44h] bits 7-0) x 4 + 1

Note

1. The value of this register is incremented by 8 pixels (1, 9, 17, 25, ..., horizontal size - 7)
2. The PIP2 window must be positioned such that it remains within the dimensions of the LCD display.

REG[46h] PIP2 Window Y Start Position Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PIP2 Window Y Start Position bits 9-2							

REG[48h] PIP2 Window Y Start Position Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						PIP2 Window Y Start Position bits 1-0	

REG[46h] bits 7-0
REG[48h] bits 1-0 PIP2 Window Y Start Position bits [9:0]

These bits determine the Y start position of the PIP2 Window in relation to the origin of the panel, in pixels. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP2 Window Y Start Position = (REG [46h] bits 7-0, REG [48h] bits 1-0) + 1

Note

The PIP2 window must be positioned such that it remains within the dimensions of the LCD display.

REG[4Ah] PIP2 Window X End Position Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PIP2 Window X End Position bits 9-3							n/a

bits 7-1 PIP2 Window X End Position bits [9:3]

These bits determine the X end position of the PIP2 Window in relation to the origin of the panel, in 8 pixel resolution (bytes). The value entered into this register is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP2 Window X End Position = (REG [4Ah] bits 7-0) x 4 + 8

Note

1. The value of this register is incremented by 8 pixels (8, 16, 24, 32, ..., horizontal size)
2. The PIP2 window must be positioned such that it remains within the dimensions of the LCD display.

REG[4Ch] PIP2 Window Y End Position Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PIP2 Window Y End Position bits 9-2							

REG[4Eh] PIP2 Window Y End Position Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						PIP2 Window Y End Position bits 1-0	

REG[4Ch] bits 7-0
REG[4Eh] bits 1-0 PIP2 Window Y End Position bits [9:0]

These bits determine the Y end position of the PIP2 Window in relation to the origin of the panel, in pixels. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP2 Window Y End Position = (REG[4Ch] bits 7-0, REG[4Eh] bits 1-0) + 1

Note

The PIP2 window must be positioned such that it remains within the dimensions of the LCD display.

REG[50h] Display Control Register

Default = 00h — Write Only

7	6	5	4	3	2	1	0
Display Setting Register Update (WO)	n/a						

bit 7 Display Setting Register Update (Write Only)
When the display registers (REG[2Ah] ~ REG[4Eh]) are changed, except REG[2Ah] bit 0, this bit must be written 1b to update the internal register values. Writing 0b to this bit has no effect.

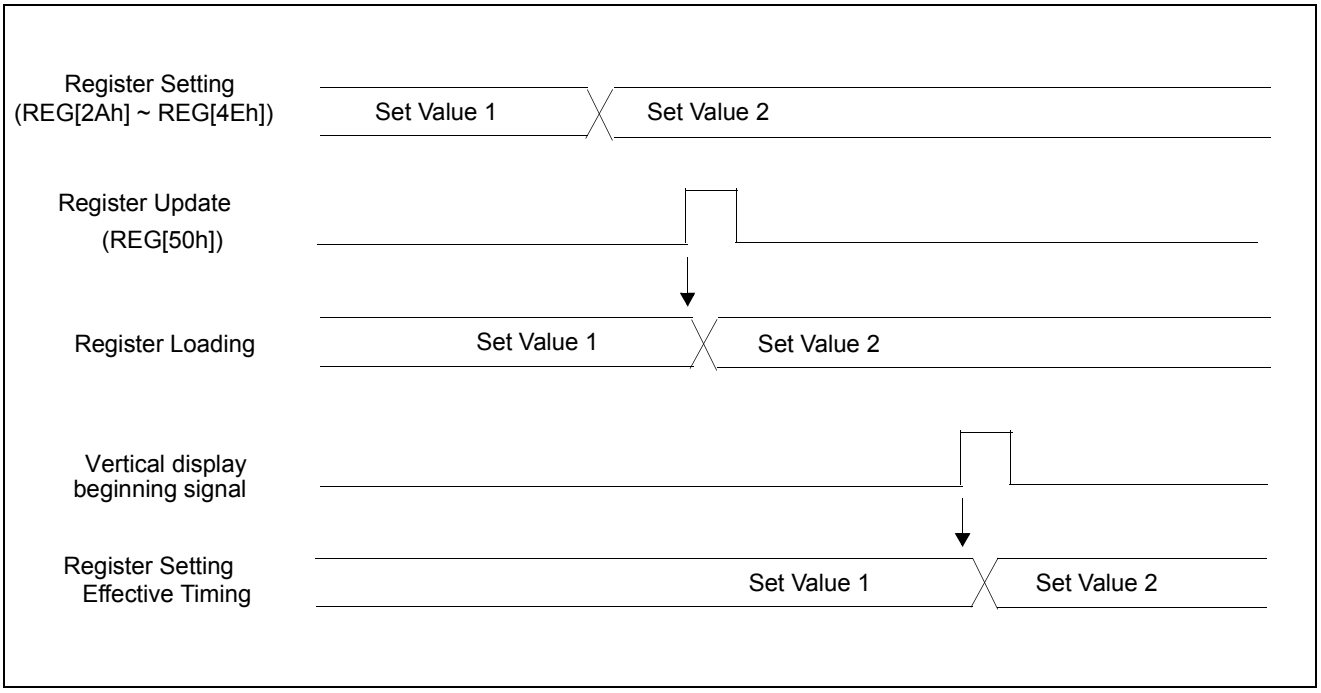


Figure 11-30: Display Setting Register Update Timing

11.17.5 Input Mode Registers

REG[52h] Input Mode Register Default = 00h							Read/Write
Write Buffer Select bits 3-0				Transparency Enable	Window Setting	Mirror Display Enable	Rotation Enable
7	6	5	4	3	2	1	0

bits 7-4 Write Buffer Select bits [3:0]

When double buffer display is not selected (REG[2Ah] bits 3-1 ≠ 001b), these bits select which write buffer will be written to by writes to the Memory Data Port registers (REG[66h] ~ REG[67h]). Up to 16 buffers are available based on the amount of memory and the Write Buffer Memory Size (see REG[90h]).

When the double buffer display is selected (REG[2Ah] bits 3-1 = 001b), these bits are ignored and Buffer 1 and 2 are fixed.

Table 11-22: Write Buffer Selection

REG[52h] bits 7-4	Write Buffer Selected
0000b	Buffer 1
0001b	Buffer 2
0010b	Buffer 3
0011b	Buffer 4
0100b	Buffer 5
0101b	Buffer 6
0110b	Buffer 7
0111b	Buffer 8
1000b	Buffer 9
1001b	Buffer 10
1010b	Buffer 11
1011b	Buffer 12
1100b	Buffer 13
1101b	Buffer 14
1110b	Buffer 15
1111b	Buffer 16

Note

These bits do not select the image data that is displayed. The display output (Main and PIP windows) is selected using the register settings in the Display Mode register (REG[2Ah])

bit 3 Transparency Enable

This bit controls whether the transparency function is enabled for writes to the write buffers. When transparency is enabled, image data that matches the transparency key color as defined by REG[54h] ~ REG[58h] will not be written to memory and the existing image data will remain. For further information on the transparency function, see Section 11.3.3, “Transparency Color” on page 68

When this bit = 0b, the Transparency is disabled.

When this bit = 1b, the Transparency is enabled.

bit 2 Window Setting
This bit controls the window setting.
When this bit = 0b, the window size is controlled by the registers (REG[5Ah] ~ [64h]).
When this bit = 1b, the window size is not controlled by the register. This bit is used the data write for the virtual display.

bit 1 Mirror Display Enable
This bit controls whether the mirror display function is enabled for writes to the write buffers. When mirror display is enabled, the image data is "mirrored" in memory. For further information on the mirror display function, see Section 11.6.2, "Mirror" on page 76.
When this bit = 0b, the mirror display function is disabled.
When this bit = 1b, the mirror display function is enabled.

bit 0 Rotation Enable
This bit controls whether the rotation function is enabled for writes to the write buffers. When rotation is enabled, the image data is rotated by 180° (counter-clockwise) in memory. For further information on the rotation function, see Section 11.6.1, "180° Rotation" on page 75.
When this bit = 0b, the rotation function is disabled.
When this bit = 1b, the rotation function is enabled.

REG[54h] Transparency Key Color Red Register
Default = 00h Read/Write

Window Transparency Key Color Red bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Window Transparency Key Color Red bits [7:0]
These bits only have an effect when the transparency is enabled, REG[52h] bit 3 = 1b. These bits specify the 8-bit red component used to define the window transparency key color.

Bits 2-0 are not used for RGB 5:6:5.

REG[56h] Transparency Key Color Green Register
Default = 00h Read/Write

Window Transparency Key Color Green bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Window Transparency Key Color Green bits [7:0]
These bits only have an effect when the transparency is enabled, REG[52h] bit 3 = 1b. These bits specify the 8-bit green component used to define the window transparency key color

Bits 1-0 are not used for RGB 5:6:5.

REG[58h] Transparency Key Color Blue Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Window Transparency Key Color Blue bits 7-0							

bits 7-0 Window Transparency Key Color Blue bits [7:0]
These bits only have an effect when the transparency is enabled, REG[52h] bit 3 = 1b. These bits specify the 8-bit blue component used to define the window transparency key color

Bits 2-0 are not used for RGB 5:6:5.

REG[5Ah] Write Window X Start Position Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Write Window X Start Position bits 9-3							n/a

bits 7-1 Write Window X Start Position bits [9:3]
These bits determine the X start position of the main window in relation to the top left corner of the displayed image, in 8 pixel resolution (bytes). Even in a rotated orientation (see REG[52h] bits 1-0), the top left corner is still relative to the displayed image.

Write Window X Start Position = (REG[5Ah] bits 7-0) x 4 +1

Note
The value of this register is incremented by 8 pixels (1, 9, 17, 25, ..., horizontal size - 7)

REG[5Ch] Write Window Y Start Position Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Write Window Y Start Position bits 9-2							

REG[5Eh] Write Window Y Start Position Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						Write Window Y Start Position bits 1-0	

REG[5Ch] bits 7-0
REG[5Eh] bits 1-0 Write Window Y Start Position bits [9:0]
These bits determine the Y start position of the window in relation to the top left corner of the displayed image, in pixels. Even in a rotated orientation (see REG[52] bit 0), the top left corner is still relative to the displayed image.

Write Window Y Start Position = (REG[5Ch] bits 7-0, REG[5Eh] bits 1-0) + 1

REG[60h] Write Window X End Position Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Write Window X End Position bits 9-3							n/a

bits 7-1 Write Window X End Position bits [9:3]
These bits determine the X end position of the window in relation to the top left corner of the displayed image, in 8 pixel resolution (bytes). Even in a rotated orientation (see REG[52h] bits 1-0), the top left corner is still relative to the displayed image.

Write Window X End Position = (REG[60h] bits 7-0) x 4 + 8

Note
The value of this register is incremented by 8 pixels (8, 16, 24, 32, ..., horizontal size)

REG[62h] Write Window Y End Position Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Write Window Y End Position bits 9-2							

REG[64h] Write Window Y End Position Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						Write Window Y End Position bits 1-0	

REG[62h] bits 7-0
REG[64h] bits 1-0 Write Window Y End Position bits [9:0]
These bits determine the Y end position of the window in relation to the top left corner of the displayed image, in pixels. Even in a rotated orientation (see REG[52h] bits 1-0), the top left corner is still relative to the displayed image.

Write Window Y End Position = (REG[62h] bits 7-0, REG[64h] bits 1-0) + 1

11.17.6 Memory Access

REG[66h] Memory Data Port Register 0							
Default = not applicable							Read/Write
Memory Data Port bits 7-0							
7	6	5	4	3	2	1	0

REG[67h] Memory Data Port Register 1							
Default = not applicable							Read/Write
Memory Data Port bits 15-8							
7	6	5	4	3	2	1	0

REG[66h] bits 7-0 Memory Data Port bits [7:0]
These bits specify the lsb of the data word.

REG[67h] bits 7-0 Memory Data Port bits [15:8]
These bits specify the msb of the data word.

Note

1. When the SDCLK is disabled (REG[68h] bit 0 = 0b), accesses to this register are invalid.
2. Burst data writes are supported through these registers. Register auto-increment is automatically disabled once reaching this address. All writes to this register will auto-increment the internal memory address only.

11.17.7 Miscellaneous Registers

REG[68h] Power Save Register
Default = 00h — Read/Write

Timing Controller Reset	PWM Controller Reset	Memory Controller Reset	SDRAM Controller Reset	Alpha-Blend Reset	Reserved		SDCLK Enable
7	6	5	4	3	2	1	0

bit 7 Timing Controller Reset
This bit controls the internal timing controller block reset.
When this bit = 0b, the timing controller block is operating normally.
When this bit = 1b, the timing controller block is reset.

bit 6 PWM Controller Reset
This bit controls the internal PWM controller block Reset.
When this bit = 0b, the PWM controller block is operating normally.
When this bit = 1b, the PWM controller block is reset.

bit 5 Memory Controller Reset
This bit controls the internal memory controller block reset.
When this bit = 0b, the memory controller block is operating normally.
When this bit = 1b, the memory controller block is reset.

bit 4 SDRAM Controller Reset
This bit controls the internal SDRAM controller block reset. After reset, the SDRAM must be initialized.
When this bit = 0b, the SDRAM controller block is operating normally.
When this bit = 1b, the SDRAM controller block is reset.

bit 3 Alpha-Blend Controller Reset
This bit controls the internal alpha-blend controller block reset.
When this bit = 0b, the alpha-blend controller block is operating normally.
When this bit = 1b, the alpha-blend controller block is reset.

bits 2-1 Reserved
The default value of these bits is 00b.

bit 0 SDCLK Enable
This bit controls the SDCLK.
When this bit = 0b, SDCLK is disabled and the LCD interface is placed in power save mode.
When this bit = 1b, SDCLK is operating normally and the LCD interface returns from power save mode.

Note
Disable SDCLK before changing PLL settings, changing SS settings, changing LCD-CLK settings, enabling PLL, enabling SS, and software reset.

REG[6Ah] Non-Display Period Control / Status Register

Default = 03h — Read/Write

7	6	5	4	3	2	1	0
Vertical Non-Display Period Status (RO)	Horizontal Non-Display Period Status (RO)	VDP OR'd with HDP Status (RO)	n/a			Reserved	

bit 7 Vertical Non-Display Period Status (Read Only)
This bit indicates whether the LCD panel output is in a vertical non-display period (VNDP). VNDP is defined as the time between the last pixel on the last line of one frame to the first pixel on the first line of the next frame.
When this bit = 0b, the LCD panel output is in a Vertical Display Period.
When this bit = 1b, the LCD panel output is in a Vertical Non-Display Period.

bit 6 Horizontal Non-Display Period Status (Read Only)
This bit indicates whether the LCD panel output is in a horizontal non-display period (HNDP). HNDP is defined as the time between the last pixel in line n to the first pixel in line n+1.
When this bit = 0b, the LCD panel output is in a Horizontal Non-Display Period.
When this bit = 1b, the LCD panel output is in a Horizontal Display Period.

bit 5 VDP OR'd with HDP Status (Read Only)
This bit indicates whether the LCD panel is in a display period or a non-display period.
When this bit = 0b, the LCD panel is in either a Horizontal or Vertical Non-Display period.
When this bit = 1b, the LCD panel is in a Display period.

bits 1-0 Reserved
The default value of these bits is 11b.

11.17.8 General Purpose Output Pins Registers

REG[6Ch] is Reserved

This register is Reserved and should not be written.

REG[6Eh] General Purpose Output Register Default = 00h							Read/Write
GPO7 Status 7	GPO6 Status 6	GPO5 Status 5	GPO4 Status 4	GPO3 Status 3	GPO2 Status 2	GPO1 Status 1	GPO0 Status 0

bits 7-0 GPO[7:0] Status
Writing a 0b to this bit drives GPOx low.
Writing a 1b to this bit drives GPOx high.

11.17.9 PWM Registers

REG[70h] PWM Control Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PWM Register Update (WO)	n/a				PWM Enable	PWM Output Select bits 1-0	

bit 7 PWM Register Update (Write Only)
When any PWM register (REG[72h] ~ REG[80h]) is changed, this bit must be written 1b to update the internal register values. Writing 0b to this bit has no effect.

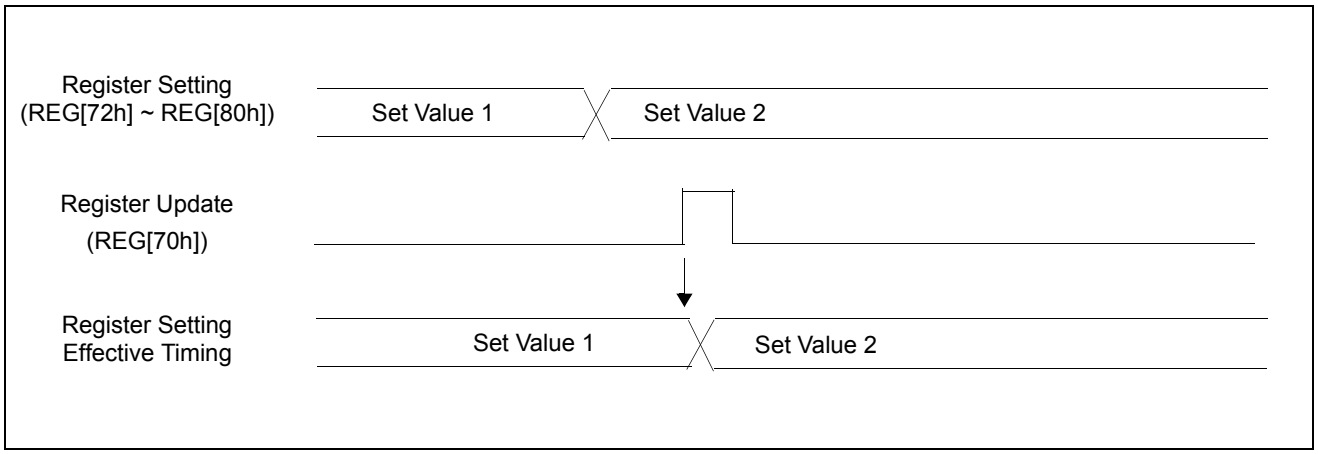


Figure 11-31: PWM Register Update Timing Sequence

bit 2 PWM Enable
This bit Pulse Width Modulation (PWM).
When this bit = 0b, PWM is disabled. When PWM is disabled, the PWM output is stopped at the current level and the may be High or Low. Use bits 1-0 of this register to set the desired output level before disabling PWM.
When this bit = 1b, PWM is enabled.

bits 1-0 PWM Output Select bits [1:0]

Table 11-23: PWM Output Select*ion*

REG[70h] bits 1-0	PWM Output Selected
00b	Low Output (Default)
01b	High Output
1xb	PWM Output

REG[72h] PWM High Duty Cycle Register 0
Default = 00h — Read/Write

PWM High Duty Cycle bits 7-0							
7	6	5	4	3	2	1	0

REG[74h] PWM High Duty Cycle Register 1
Default = 00h — Read/Write

PWM High Duty Cycle bits 15-8							
7	6	5	4	3	2	1	0

REG[76h] PWM High Duty Cycle Register 2
Default = 00h — Read/Write

PWM High Duty Cycle bits 23-16							
7	6	5	4	3	2	1	0

REG[78h] PWM High Duty Cycle Register 3
Default = 00h — Read/Write

PWM High Duty Cycle bits 31-24							
7	6	5	4	3	2	1	0

REG[72h] bits 7-0
REG[74h] bits 7-0
REG[76h] bits 7-0
REG[78h] bits 7-0 PWM High Duty Cycle bits [31:0]

These bits are the value for the PWM High duty cycle. The value entered into these registers is not loaded into internal registers until REG[70h] bit 7 has been written with a 1b.

REG[7Ah] PWM Low Duty Cycle Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PWM Low Duty Cycle bits 7-0							

REG[7Ch] PWM Low Duty Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PWM Low Duty Cycle bits 15-8							

REG[7Eh] PWM Low Duty Register 2
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PWM Low Duty Cycle bits 23-16							

REG[80h] PWM Low Duty Register 3
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PWM Low Duty Cycle bits 31-24							

REG[7Ah] bits 7-0
REG[7Ch] bits 7-0
REG[7Eh] bits 7-0
REG[80h] bits 7-0 PWM Low Duty Cycle bits [31:0]

These bits are the value for the PWM Low duty cycle. The value entered into these registers is not loaded into internal registers until REG[70h] bit 7 has been written with a 1b.

11.17.10 SDRAM Control Registers

REG[82h] SDRAM Control Register 0							
Default = 02h							Read/Write
Reserved						SDRAM Memory Size Select bits 1-0	
7	6	5	4	3	2	1	0

bits 7-2 Reserved
The default value of these bits is 00_0000b

bits 1-0 SDRAM Memory Size Select bits [1:0]

Table 11-24: SDRAM Memory Size Selection

REG[82h] bits 1-0	SDRAM Memory Size Selected
0xb	16M Bits
10b	64M Bits (Default)
11b	128M Bits

REG[84h] SDRAM Status Register 0							
Default = not applicable							Write Only
SDRAM Auto Refresh Enable (WO)	Reserved			SDRAM Self Refresh Enable (WO)	SDRAM Power Save Enable (WO)	SDRAM Initialization (WO)	Reserved
7	6	5	4	3	2	1	0

bit 7 SDRAM Auto Refresh Enable (Write Only)
This bit controls SDRAM Auto Refresh. This bit should be set at the same time as the SDRAM Initialization bit (bit 1 of this register).
When this bit is written 0b, SDRAM Auto Refresh is disabled.
When this bit is written 1b, SDRAM Auto Refresh is enabled.

bits 6-4 Reserved
The default value of these bits is 000b.

bit 3 Self Refresh Enable (Write Only)
This bit controls SDRAM Self Refresh
When this bit is written 0b, SDRAM Self Refresh is disabled.
When this bit is written 1b, SDRAM Self Refresh is enabled.

bit 2 SDRAM Power Save Enable (Write Only)
This bit controls SDRAM Power Save
When this bit is written 0b, SDRAM Power Save is disabled.
When this bit is written 1b, SDRAM Power Save is enabled.

bit 1 SDRAM Initialization (Write Only)
After power-on or reset, this bit is used to initialize the SDRAM.
When this bit is written 0b, the status bit is reset.
When this bit is written 1b, the SDRAM is initialized. This bit may only be written once after power-on/reset.

bit 0 Reserved
The default value of this bit is 0b.

REG[86h] SDRAM Status Register 1
Default = 00h Read Only

SDRAM Auto Refresh Status (RO)	SDRAM Controller Status (RO)	Reserved		SDRAM Self Refresh Status (RO)	SDRAM Power Save Status (RO)	SDRAM Initialization Status (RO)	Reserved
7	6	5	4	3	2	1	0

bit 7 SDRAM Auto Refresh Status
This bit reflects the status of REG[84h] bit 7, SDRAM Auto Refresh Enable.
When this bit = 0b, SDRAM Auto Refresh is disabled.
When this bit = 1b, SDRAM Auto Refresh is enabled.

bit 6 SDRAM Controller Status
This bit shows the status of the SDRAM Controller.
When this bit = 0b, the SDRAM Controller is busy or otherwise in use.
When this bit = 1b, the SDRAM Controller is idle.

bits 5-4 Reserved
The default value of theses bits is 00b.

bit 3 SDRAM Self Refresh Status
This bit reflects the status of REG[84h] bit 3, SDRAM Self Refresh Enable.
When this bit = 0b, SDRAM Self Refresh is disabled.
When this bit = 1b, SDRAM Self Refresh is enabled.

bit 2 SDRAM Power Save Status
This bit reflects the status of REG[84h] bit 2, SDRAM Power Save Enable.
When this bit = 0b, SDRAM Power Save is disabled.
When this bit = 1b, SDRAM Power Save is enabled.

bit 1 SDRAM Initialization Status
This bit reflects the status of the SDRAM Initialization sequence (REG[84h] bit 3 = 1b).
When this bit = 0b, the SDRAM Initialization is in progress.
When this bit = 1b, the SDRAM Initialization has finished.

bits 0 Reserved
The default value of this bit is 0b.

REG[88h] SDRAM MRS Value Register 0
Default = 22h — Read/Write

SDRAM MRS Value bits 7-0							
7	6	5	4	3	2	1	0

REG[8Ah] SDRAM MRS Value Register 1
Default = 00h — Read/Write

n/a				SDRAM MRS Value bits 11-8			
7	6	5	4	3	2	1	0

REG[8Ah] bits 3-0
REG[88h] bits 7-0 SDRAM MRS Value bits [11:0]
These bits are the MRS setting values for the SDRAM.
These bits must not be changed from the default value of 022h.

REG[8Ch] SDRAM Refresh Counter Register 0
Default = FFh — Read/Write

SDRAM Refresh Counter bits 7-0							
7	6	5	4	3	2	1	0

REG[8Eh] SDRAM Refresh Counter Register 1
Default = 03h — Read/Write

n/a				SDRAM Refresh Counter bits 11-8			
7	6	5	4	3	2	1	0

REG[8Eh] bits 3-0
REG[8Ch] bits 7-0 SDRAM Refresh Counter bits [11:0]
These bits are used to set the value of the refresh counter. The refresh counter issues the auto refresh command at the interval set by these registers. SDCLK is the input clock of the counter. The value of these registers must satisfy the following expression.

Refresh Counter = $(1/f_{SDCLK})$ x (value of these registers in decimal)
The resulting value must be less than the SDRAM refresh time.

For example, using the default value of 03FFh (1023), when SDRAM of 4096 refresh cycles /64ms is used with a 96MHz SDCLK,
set-up time of the counter = (1/96MHz) x 1023 = 10.65us
SDRAM refresh time = 64ms/4096 = 15.63us.
10.65us < 15.63us, so the value of 03FFh is good.

Using the same memory as above, but with a 66MHz SDCLK,
(1/66MHz) x 1023 = 15.50us
SDRAM refresh time = 64ms/4096 = 15.63us
15.50us < 15.63us, so the value of 03FFh is good.

REG[90h] SDRAM Write Buffer Memory Size Register 0
Default = 00h — Read/Write

SDRAM Write Buffer Memory Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 SDRAM Write Buffer Memory Size bits [7:0]
These bits determine the buffer memory size of each 16-buffers at the 16K byte units. Buffer 1 becomes the start address 0h fixing of SDRAM, the start address of buffer 2 is appointed at these bits. The buffer 3-16 is set at similar offset value. In case of initial value 00h, the start address of all buffers becomes the start addresses 0h of SDRAM.

The start address of buffer 2: A [23: 22] = 0
The start address of buffer 2: A [21: 14] = (REG [90h] bits 7-0)
The start address of buffer 2: A [13: 0] = 0

Table 11-25: SDRAM Write Buffer Memory Size Selection

LCD Panel Size	Buffer Size	REG[90h] Value
HVGA	512K byte	20h
VGA	1M byte	40h
WVGA	1.25M byte	50h
SVGA	1.5M byte	60h

REG[92h] SDRAM Debug Register
Default = 00h — Read Only

SDRAM Controller Debug Status (RO)							
7	6	5	4	3	2	1	0

bit 4 Memory Controller Read Buffer Empty (Read Only)
When this bit = 0b, the Read Buffer is not empty.
When this bit = 1b, the Read Buffer is empty.
This bit is cleared by resetting the Memory Controller.

bit 3 Memory Controller Write Buffer Overflow (Read Only)
When this bit = 0b, the Write Buffer is not full.
When this bit = 1b, the Write Buffer is full.
This bit is cleared by resetting the Memory Controller.

bits 2-0 SDRAM Controller Status (Read Only)
These three bits indicate the status of the SDRAM controller state machine as shown in the following table.

Table 11-26: SDRAM Controller Status

REG[92h] bits 2-0	Status
000	Reset
001	Initial
010	Idle
011	Read/Write
100	Auto Refreshing
101	MRS&PALL
110	Self Refresh
111	Power Save

11.17.11 Alpha-Blend Registers

REG[94h] Alpha-Blend Control Register Default = 00h							Write Only
Alpha-Blend Start Mode	Auto-mode Direction	Auto-mode Alpha Resolution bits 1-0		n/a		Alpha-Blend Start Trigger	Alpha-Blend Start (WO)
7	6	5	4	3	2	1	0

bit 7 Alpha-Blend Start Mode
This bit determines the start mode of the Alpha-blend.
When this bit is written 0b, the manual-mode is selected.
When this bit is written 1b, the auto-mode is selected.

bit 6 Auto-mode Direction
This bit determines the direction of the auto-mode. When the manual-mode is selected, this bit is ignored.
When this bit is written 0b, the direction is increment from 0 to 1.
When this bit is written 1b, the direction is decrement from 1 to 0.

bits 5-4 Auto-mode Alpha Resolution bits [1:0]
These bits determine the alpha resolution of the auto-mode. When the manual-mode is selected, these bits are ignored.

Table 11-27: Auto-mode Alpha Resolution

REG[94h] bits 5-4	Alpha Resolution
00b	1/256 (default)
01b	1/128
10b	1/64
11b	1/32

bit 1 Alpha-Blend Start Trigger
This bit determines the start trigger of the Alpha-blend.
When this bit is written 0b, the start trigger is the register set (bit 0 = 1) immediately.
When this bit is written 1b, the start trigger is the vertical non-display period after the register set (bit 0 = 1).

bit 0 Alpha-Blend Start (Write Only)
When this bit is written 0b, there is no effect.
When this bit is written 1b then 0b, Alpha-Blend is started.

REG[96h] is Reserved

This register is Reserved and should not be written.

REG[98h] Alpha-Blend Horizontal Size Register
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a	Alpha-Blend Horizontal Image Size bits 6-0						

bits 6-0 Alpha-Blend Horizontal Image Size bits [6:0]
These bits set the Alpha-Blend Horizontal Image Size in 8 pixel resolution (bytes).

Alpha-Blend Horizontal Image Size = ((REG[98h] bits 6-0) + 1) x 8

REG[9Ah] Alpha-Blend Vertical Size Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
Alpha-Blend Vertical Image Size bits 7-0							

REG[9Ch] Alpha-Blend Vertical Size Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a						Alpha-Blend Vertical Image Size bits 9-8	

REG[9Ch] bits 1-0
REG[9Ah] bits 7-0 Alpha-Blend Vertical Image Size bits [9:0]
These bits set the Alpha-Blend Horizontal Image Size.

Alpha-Blend Vertical Image Size = (REG[9Ch] bits 1-0, REG[9Ah] bits 7-0) + 1

REG[9Eh] Alpha-Blend Value Register
Default = 00h — Read/Write

Alpha-Blend Input Mode Select bits 1-0		Alpha-Blend Value Select bits 5-0					
7	6	5	4	3	2	1	0

bits 7-6 Alpha-Blend Input Mode Select bits [1:0]
These bits select the Alpha-Blend input mode.

Table 11-28: Alpha-Blend Input Mode Selection

REG[9Eh] bits 7-6	Alpha-Blend Input Image
00b	Disabled (Default)
01b	Fill mode
10b	Normal mode
11b	Copy mode

bits 5-0 Alpha-Blend Value Select bits [5:0]
These bits set the value of Alpha-Blend.

Normal mode:
Output image = (input image 1 x alpha setting value) * (input image 2 + x (1 - alpha setting value)

Copy mode:
Output image = (input image 1 x alpha setting value)

Fill mode:
Output image = (register setting color x alpha setting value)

Table 11-29: Alpha-Blend Value Selection

REG[9Eh] bits 5-0	Alpha Value
00h	0
01h	1/32
02h	2/32
03h	3/32
• • •	• • •
1Fh	31/32
2xh	1

REG[A0h] Alpha-Blend Input Image 1 Start Address Register 0
Default = 00h Read/Write

Alpha-Blend Input Image 1 Start Address bits 7-3					n/a		
7	6	5	4	3	2	1	0

REG[A2h] Alpha-Blend Input Image 1 Start Address Register 1
Default = 00h Read/Write

Alpha-Blend Input Image 1 Start Address bits 15-8							
7	6	5	4	3	2	1	0

REG[A4h] Alpha-Blend Input Image 1 Start Address Register 2
Default = 00h Read/Write

Alpha-Blend Input Image 1 Start Address bits 23-16							
7	6	5	4	3	2	1	0

REG[A4h] bits 7-0
REG[A2h] bits 7-0
REG[A0h] bits 7-3 Alpha-Blend Input Image 1 Start Address bits 7-[23:3]
These bits specify the memory start address of Alpha-Blend Input Image 1 in byte addresses.

Alpha-Blend Input Image 1 Start Address [23:3] = (REG[A4h] bits 7-0), (REG[A2h] bits 7-0), (REG[A0h] bits 7-3)

REG[A6h] Alpha-Blend Input Image 2 Start Address Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Alpha-Blend Input Image 2 Start Address bits 7-3					n/a		

REG[A8h] Alpha-Blend Input Image 2 Start Address Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Alpha-Blend Input Image 2 Start Address bits 15-8							

REG[AAh] Alpha-Blend Input Image 2 Start Address Register 2
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Alpha-Blend Input Image 2 Start Address bits 23-16							

REG[AAh] bits 7-0
REG[A8h] bits 7-0
REG[A6h] bits 7-3 Alpha-Blend Input Image 2 Start Address bits[23:3]
These bits specify the memory start address of Alpha-Blend Input Image 2 in byte addresses.

Alpha-Blend Input Image 2 Start Address [23:3] = (REG[AAh] bits 7-0), (REG[A8h] bits 7-0), (REG[A6h] bits 7-3)

REG[ACh] Alpha-Blend Output Image Start Address Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Alpha-Blend Output Image Start Address bits 7-3					n/a		

REG[AEh] Alpha-Blend Output Image Start Address Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Alpha-Blend Output Image Start Address bits 15-8							

REG[B0h] Alpha-Blend Output Image Start Address Register 2
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Alpha-Blend Output Image Start Address bits 23-16							

REG[B0h] bits 7-0
REG[AEh] bits 7-0
REG[ACh] bits 7-3 Alpha-Blend Output Image Start Address bits [23:3]
These bits specify the memory start address of Alpha-Blend Output Image in byte addresses.

Alpha-Blend Input Image 2 Start Address[23:3] = (REG[B0h] bits 7-0), (REG[AEh] bits 7-0), (REG[ACh] bits 7-3)

11.17.12 Interrupt Registers

REG[B2h] Interrupt Control Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a			Alpha-Blend Interrupt Mask Disable	n/a			Alpha-Blend Interrupt Enable

bit 4 Alpha-Blend Interrupt Mask Disable
This bit disables the Alpha-Blend Interrupt Mask.
When this bit = 0b, the interrupt mask is enabled.
When this bit = 1b, the interrupt mask is disabled.

bit 0 Alpha-Blend Interrupt Enable
This bit enables the Alpha-Blend Interrupt.
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

REG[B4h] Interrupt Status Register
Default = 00h — Read Only

7	6	5	4	3	2	1	0
n/a							Alpha-Blend Interrupt Status (RO)

bit 0 Alpha-Blend Interrupt Status (Read Only)
This bit indicates the status of the Alpha-Blend interrupt.
When this bit = 0b, an interrupt has not been generated.
When this bit = 1b, an interrupt has been generated.

REG[B6h] Interrupt Clear Register
Default = 00h — Write Only

7	6	5	4	3	2	1	0
n/a							Alpha-Blend Interrupt Clear (WO)

bit 0 Alpha-Blend Interrupt Clear (Write Only)
This bit clears the interrupt status bit.
When this bit is written 0b, there is no effect.
When this bit is written 1b then 0b, the Alpha-Blend interrupt status bit (REG[B4h] bit 0) is cleared.

11.17.13 Display Enhancement Registers

REG[B8h] Display Enhancement Control Register Default = 00h							Read/Write
LUT Access Mode bits 1-0		n/a			Brightness Correction Enable	Contrast Correction Enable	Gamma Correction Enable
7	6	5	4	3	2	1	0

bits 7-6 LUT Access Mode bits [1:0]
This bit determines the access method for the Look-up table. The Gamma correction bit must be disabled to be access the Look-up table.

Table 11-30: LUT Access Mode Selection

REG[B8h] bits 7-6	LUT Access Mode
00b	Writing will be done to each Red, Green and Blue table at the same time. Reading will be done from Red table.
01b	Writing and Reading will be done to Red table.
10b	Writing and Reading will be done to Green table.
11b	Writing and Reading will be done to Blue table.

bit 2 Brightness Correction Enable
This bit enables the Brightness correction.
When this bit = 0b, the Brightness correction is disabled.
When this bit = 1b, the Brightness correction is enabled.

bit 1 Contrast Correction Enable
This bit enables the Contrast correction.
When this bit = 0b, the Contrast correction is disabled.
When this bit = 1b, the Contrast correction is enabled.

bit 0 Gamma Correction Enable
This bit enables the Gamma correction.
When this bit = 0b, the Gamma correction is disabled.
When this bit = 1b, the Gamma correction is enabled.

REG[BAh] Gamma Correction Table Index Register

Default = 00h — Read/Write

Gamma Correction Table Index bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Gamma Correction Table Index bits [7:0]
These bits specify the index of the gamma correction look-up table which subsequent read/write start at.

REG[BCh] Gamma Correction Table Data Register

Default = 00h — Read/Write

Gamma Correction Table Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Gamma Correction Table Data bits [7:0]
When writing to gamma correction table data register, the index to the internal table will be automatically incremented. For continuos update to the table, the gamma correction table data register needs only to be written once. The index will be incremented by 1 for every write to the gamma correction table register.

REG[BEh] Brightness Correction Red Register 0

Default = 00h — Read/Write

Brightness Correction Red bits 7-0							
7	6	5	4	3	2	1	0

REG[C0h] Brightness Correction Red Register 1

Default = 00h — Read/Write

n/a							Brightness Correction Red bit 8
7	6	5	4	3	2	1	0

REG[C0h] bit 0

REG[BEh] bits 7-0 Brightness Correction Red bits [8:0]
These bits specify the red value of the brightness correction. The register value will be updated with next vertical period.

REG[C2h] Brightness Correction Green Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Brightness Correction Green bits 7-0							

REG[C4h] Brightness Correction Green Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a							Brightness Correction Green bit 8

REG[C4h] bit 0

REG[C2h] bits 7-0 Brightness Correction Green bits [8:0]
These bits specify the green value of the brightness correction. The register value will be updated with next vertical period.

REG[C6h] Brightness Correction Blue Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Brightness Correction Blue bits 7-0							

REG[C8h] Brightness Correction Blue Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a							Brightness Correction Blue bit 8

REG[C8h] bit 0

REG[C6h] bits 7-0 Brightness Correction Blue bits [8:0]
These bits specify the blue value of the brightness correction. The register value will be updated with next vertical period.

REG[CAh] Contrast Correction Red Register

Default = 00h — Read/Write

Contrast Correction Red bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Contrast Correction Red bits [7:0]

These bits specify the red value of the contrast correction. The register value will be updated with next vertical period.

REG[CCh] Contrast Correction Green Register

Default = 00h — Read/Write

Contrast Correction Green bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Contrast Correction Green bits [7:0]

These bits specify the green value of the contrast correction. The register value will be updated with next vertical period.

REG[CEh] Contrast Correction Blue Register

Default = 00h — Read/Write

Contrast Correction Blue bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Contrast Correction Blue bits [7:0]

These bits specify the blue value of the contrast correction. The register value will be updated with next vertical period.

11.17.14 Display Extend Registers

REG[E0h] Extend Display Control Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a			Overlay Display Enable	n/a			Doubling Display Enable

bit 4 Overlay Display Enable
This bit enables the overlay display.
When this bit = 0b, the overlay display is disabled.
When this bit = 1b, the overlay display is enabled.

Note
There are some limitations when this bit is enabled, please refer to Table 11-15: "LCD-CLK Divide Selection," on page 100 for further information

bit 0 Doubling Display Enable
This bit enables the doubling display.
When this bit = 0b, the doubling display is disabled.
When this bit = 1b, the doubling display is enabled.

REG[E2h] Virtual Display Horizontal Width Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Virtual Display Enable	n/a					Virtual Display Horizontal Size bits 9-8	

REG[E4h] Virtual Display Horizontal Width Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Virtual Display Horizontal Size bits 7-0							

REG[E2h] bit 7 Virtual Display Enable
This bit enables the virtual display.
When this bit = 0b, the virtual display is disabled.
When this bit = 1b, the virtual display is enabled.

REG[E2h] bits 1-0

REG[E4h] bits 7-0 Virtual Display Horizontal Size bits [9:0]
These bits specify the horizontal size of the virtual display, in 8 pixel resolution (bytes).
Horizontal Size of pixels = (REG[E2h] bits 1-0, REG[E4h] bits 7-0) × 8

Note
The minimum Horizontal Display Width is 32 pixels and the maximum is 8192 pixels.

REG[E6h] SDRAM Read Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Reserved		n/a					SDRAM Read Enable

bits 7-6 Reserved
The default value for these bits is 00b.

bit 0 SDRAM Read Enable
This bit enables the SDRAM read. When this bit is enabled, the Alpha-blend function can not be used.
When this bit = 0b, the SDRAM read is disabled.
When this bit = 1b, the SDRAM read is enabled.

REG[E8h] SDRAM Read Start Address Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
SDRAM Read Start Address bits 7-3					n/a		

REG[EAh] SDRAM Read Start Address Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
SDRAM Read Start Address bits 15-8							

REG[ECh] SDRAM Read Start Address Register 2
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
SDRAM Read Start Address bits 23-16							

REG[ECh] bits 7-0
REG[EAh] bits 7-0
REG[E8h] bits 7-3 SDRAM Read Start Address bits [23:3]
These bits specify the start address of the SDRAM read in the display buffer.

SDRAM Read Start Address A [23:3] = (REG[ECh] bits 7-0, REG[EAh] bits 7-0, REG[E8h] bits 7-3)

REG[EEh] SDRAM Dummy Read Port Register
Default = 00h — Read Only

7	6	5	4	3	2	1	0
SDRAM Dummy Read Port bits 7-0							

bits 7-0 SDRAM Dummy Read Port bits [7:0] (Read Only)
These bits are the dummy read port for the SDRAM read function. These data are not used.

Chapter 12 I/O Interface

12.1 SPI Interface

The SPI interface is a synchronous serial interface that works only as master mode. The transmission buffer and the receive buffer can be built into besides the shift register, and the data transfer be done efficiently.

The SPI interface controls the operation mode, the data transmission and the data receive by using the SPI command. For further information on the SPI command, see S1D13U11 Software Technical Manual.

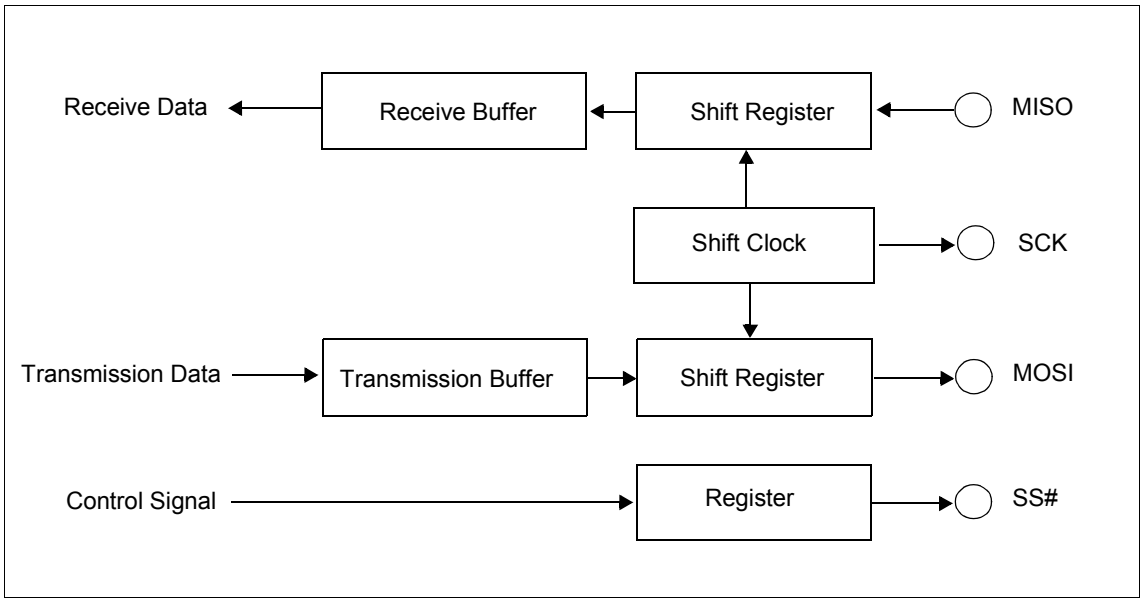


Figure 12-1: SPI Interface Block Diagram

12.1.1 SPI Clock

The frequency, polarity (CPOL) and phase (CPHA) of the SPI clock are set according to the SPI command.

Table 12-1: SPI Clock Frequency

Divide Ratio	SPI Clock Frequency	Divide Ratio	SPI Clock Frequency
1/2	15.00MHz	1/256	117kHz
1/4	7.50MHz	1/512	58.6kHz
1/8	3.75MHz	1/1024	29.3kHz
1/16	1.88MHz	1/2048	14.6kHz
1/32	938kHz	1/4096	7.32kHz
1/64	469kHz	1/8192	3.66kHz
1/128	234kHz	1/16384	1.83kHz

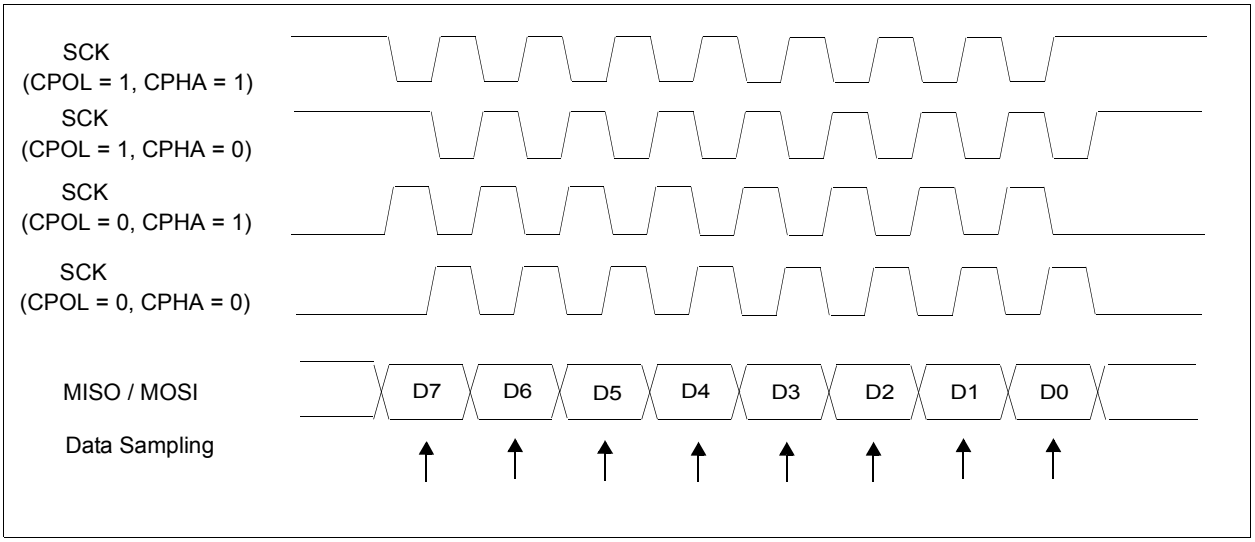


Figure 12-2: SPI Clock Timing

12.1.2 SPI Slave Select

There are three SPI slave select pins. The SS0# pin becomes SPI interface of channel 0 (Ch0). The SS1# and SS2# pins become SPI interfaces of channel 1(Ch1). (SS2 # pin is used exclusively for the serial flash memory.)

The polarity of the SPI slave select (low active or high active) and the pulse width (1-byte assert or continuous assert) are set according to the SPI command.

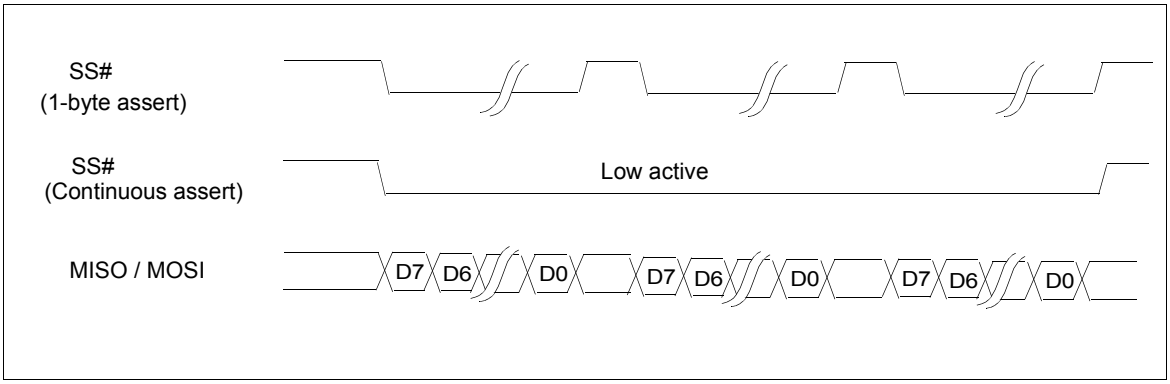


Figure 12-3: SPI Slave Select

12.1.3 SPI Sequential Command

The SPI sequential command executes several SPI commands registered beforehand synchronizing with the trigger input (constant interval or INT0 interrupt). And the event notification is generated at the same time as ending. It is possible to use it for the coordinate data from the touch screen controller etc. For further information on the SPI sequential command, see S1D13U11 Software Technical Manual.

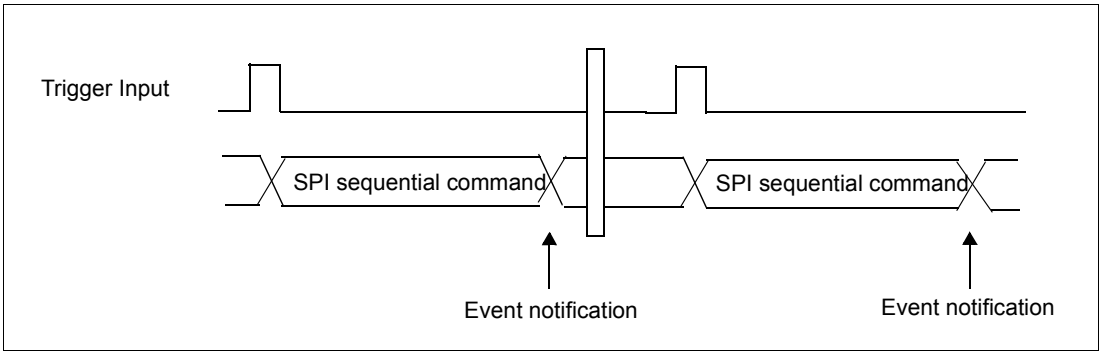


Figure 12-4: SPI Sequential Command

12.1.4 I2C Interface

The I2C interface is a synchronous serial interface that works only as single master mode and it supports 7-bit slave address output. The supported frequencies of I2CCLK are 117.19kHz and 468.75kHz.

The I2C Interface controls the operation mode, the data transmission and the data reception by using the I2C command. For further information on the I2C command, see S1D13U11 Software Technical Manual.

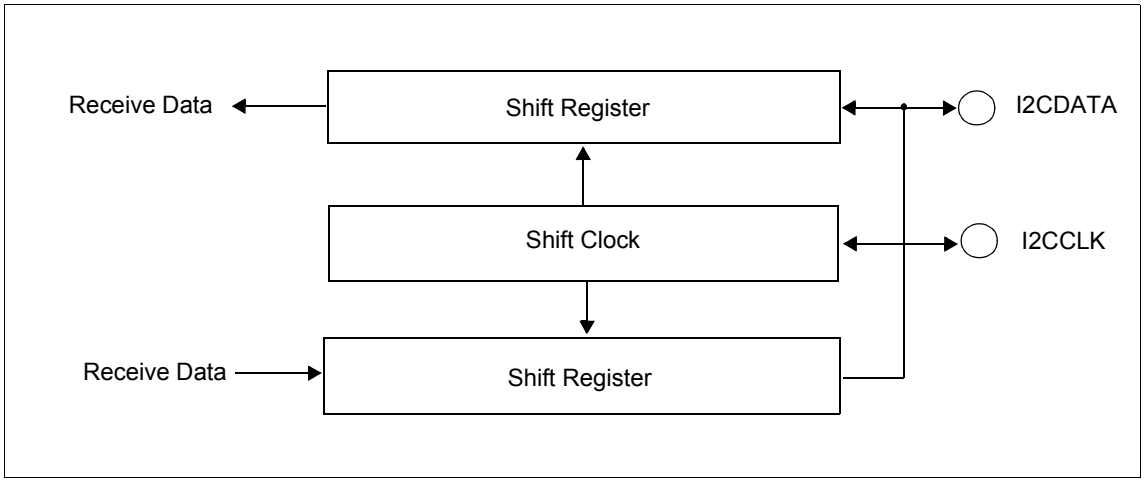


Figure 12-5: I2C Interface Block Diagram

12.1.5 I2C Clock

The frequency of the I2C clock is set according to the I2C command. The I2C hardware does not support the clock stretch function, which is initiated by the I2C slave device and holds the I2CCLK low.

Table 12-2: I2C Clock Frequency

Mode	I2C Clock Frequency
bTransferRate=01h	117.19kHz
bTransferRate=02h	468.75kHz

12.1.6 I2C Slave Address

The I2C slave address (slave side device address and forwarding direction) is output, when the data sending and receiving begins. The I2C slave address is set according to the I2C command.

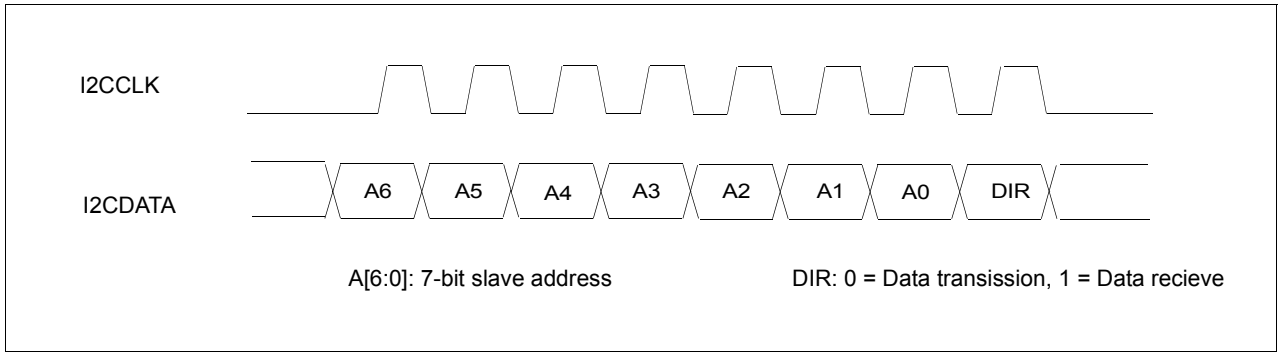


Figure 12-6: I2C Slave Address

12.1.7 Start Condition

The start condition is output, when the data sending and receiving begins. The start condition makes I2CDATA from the high level to the low level with I2CCLK kept high level.

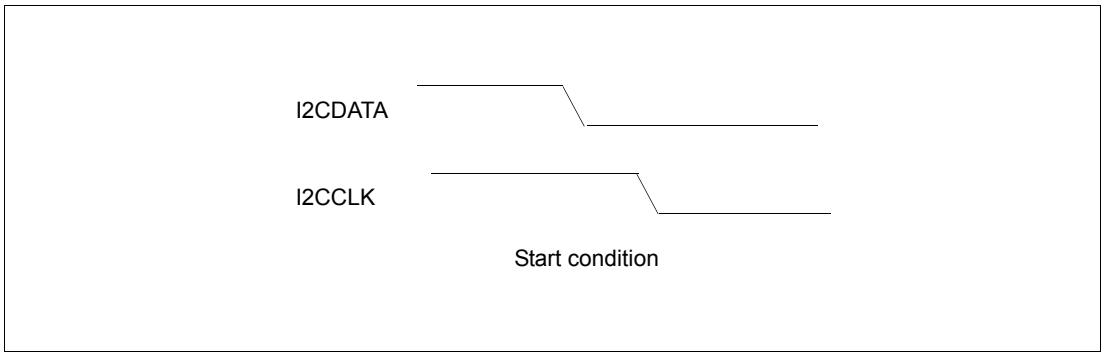


Figure 12-7: Start Condition

12.1.8 Stop Condition

The stop condition is output, when the data sending and receiving is ended. The stop condition makes I2CDATA high level from the low level with I2CCLK kept high level.

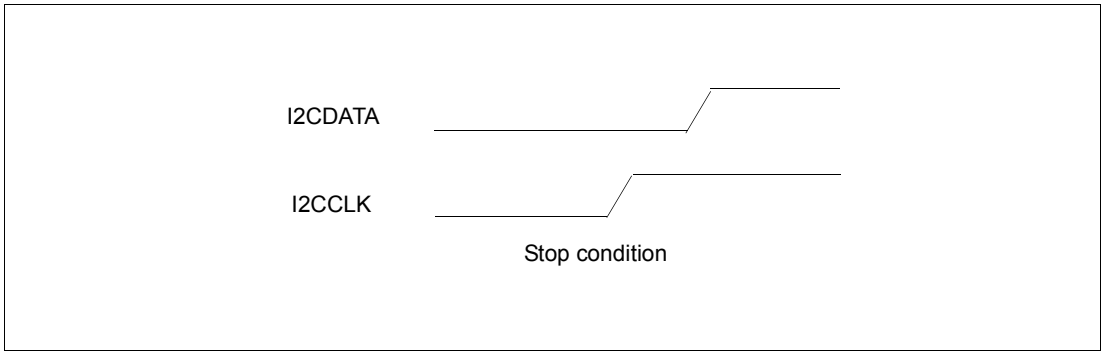


Figure 12-8: Stop Condition

12.1.9 Repeated Start Condition

The I2C hardware does not support the repeated start condition function.
The repeated start condition is output, when the sending and receiving of data begins again after the sending and receiving of data ends. The repeated start condition makes I2CDATA from the high level to the low level with I2CCLK kept high level.

12.1.10 ACK/NAK Receive

The data of the 9th clock when the I2C data is transmitted becomes ACK/NAK response receive from the slave device. The ACK (low level) is detected when the slave device can correctly receive data. The NAK (high level) is detected with the pull-up resistor when data cannot be correctly received.

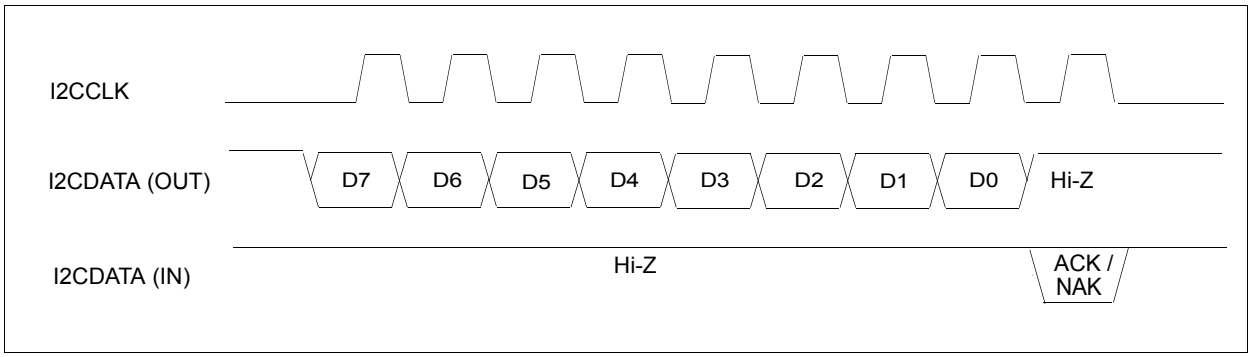


Figure 12-9: ACK/NAK Receive

12.1.11 ACK/NAK Transmission

The data of the 9th clock when the I2C data is received becomes ACK/NAK response transmission to the slave device.

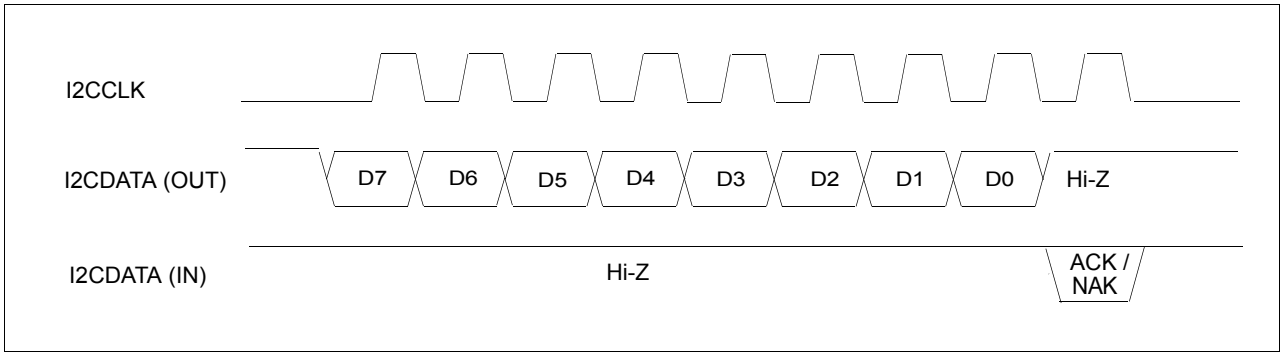


Figure 12-10: ACK/NAK Transmission

12.1.12 GPIO Interface

The GPIO interface becomes a general-purpose I/O port in 16 bits. The I/O switch and the pull-up resistor can be controlled as bit unit.

The GPIO interface controls the operation mode, the input data read and the output data write by using the GPIO command. For further information on the GPIO command, see S1D13U11 Software Technical Manual.

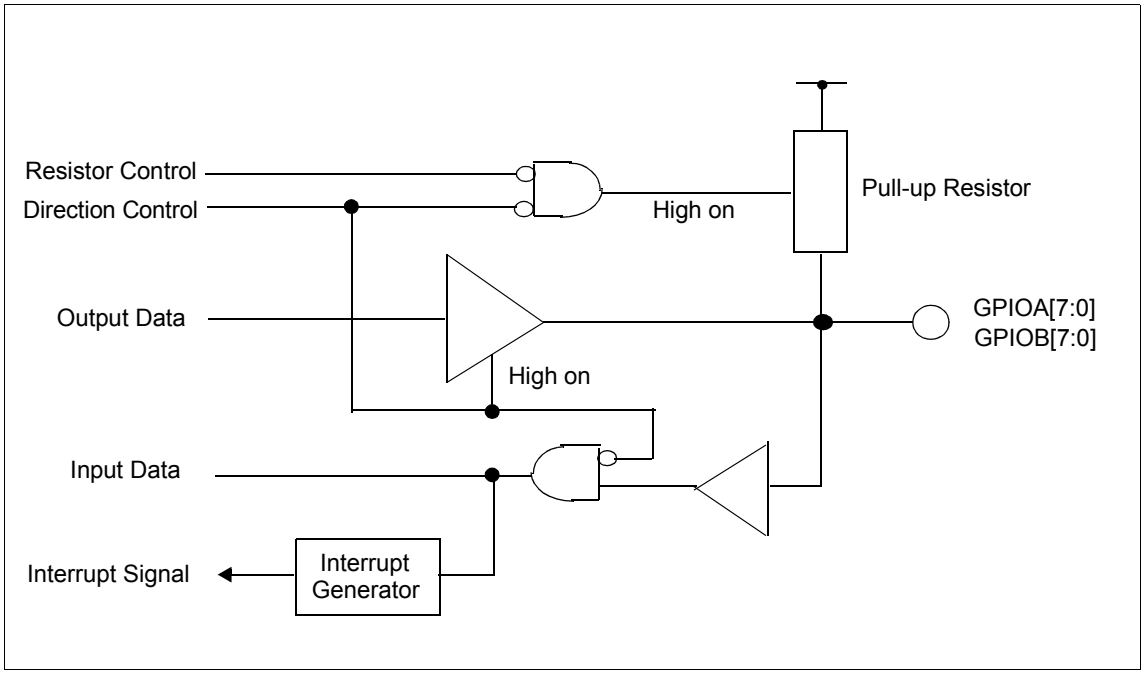


Figure 12-11: GPIO Interface Block Diagram

12.1.13 GPIO Pin Configuration

The pin configuration of the GPIO interface is set according to the GPIO command.

Table 12-3: GPIO Pin Configuration

Pin Name	GPIO Interface		Key-scan Interface			
	Pin Direction	Pull-up Resistor	8x8 Matrix	8x4 Matrix	8x2 Matrix	Pull-up Resistor
GPIOA0	Input or Output	On or Off	Key-scan Input	Key-scan Input	Key-scan Input	On or Off
GPIOA1	Input or Output	On or Off				On or Off
GPIOA2	Input or Output	On or Off				On or Off
GPIOA3	Input or Output	On or Off				On or Off
GPIOA4	Input or Output	On or Off				On or Off
GPIOA5	Input or Output	On or Off				On or Off
GPIOA6	Input or Output	On or Off				On or Off
GPIOA7	Input or Output	On or Off				On or Off
GPIOB0	Input or Output	On or Off	Key-scan Output	Key-scan Output	Key-scan Output	-
GPIOB1	Input or Output	On or Off				-
GPIOB2	Input or Output	On or Off			Input or Output	On or Off
GPIOB3	Input or Output	On or Off			Input or Output	On or Off
GPIOB4	Input or Output	On or Off		Input or Output	Input or Output	On or Off
GPIOB5	Input or Output	On or Off		Input or Output	Input or Output	On or Off
GPIOB6	Input or Output	On or Off		Input or Output	Input or Output	On or Off
GPIOB7	Input or Output	On or Off		Input or Output	Input or Output	On or Off

12.1.14 GPIO Interrupt

The interrupt setting of the GPIO interface is set according to the GPIO command. The GPIO interrupt cannot be used when Key-scan is used or in sleep mode..

Table 12-4: GPIO Interrupt

Input Interrupt	Polarity
Edge Detection	Rising Edge
	Falling Edge
Level Detection	High Level
	Low Level

12.1.15 Key-scan Interface

The key-scan interface scans reads the switch data automatically by hardware scanning the key matrix switch. It is possible to select it from three kinds of key matrices of 8x8, 8x4 or 8x2. The rest pins can be used as the GPIO interface in the key matrices of 8x4 or 8x2.

The key-scan interface controls the operation setting and the switch data read by using the Key-scan command. For further information on the Key-scan command, see S1D13U11 Software Technical Manual.

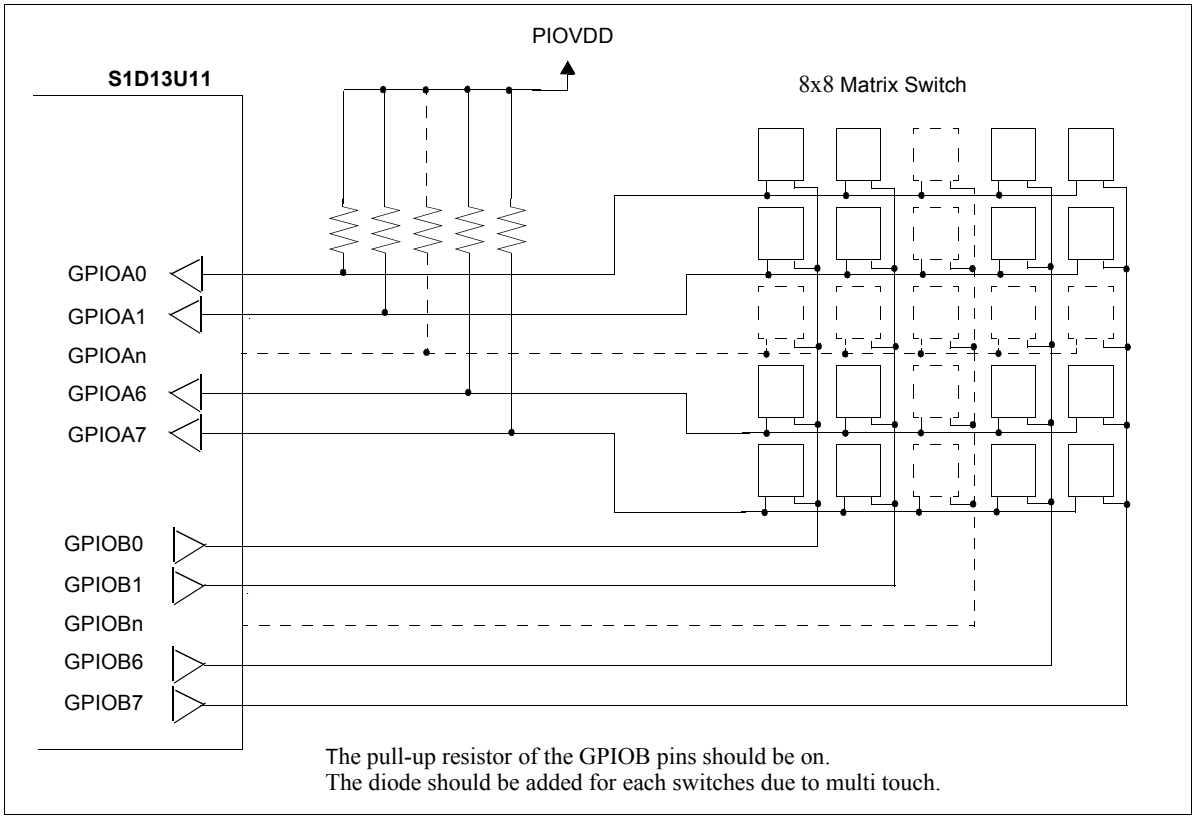


Figure 12-12: Key-scan Interface Block Diagram

12.1.16 High Drive Mode

In the high drive mode, the high level is output after one clock Hi-Z level. The expected pull-up resistor must add to recognize the high level for the scan clock.

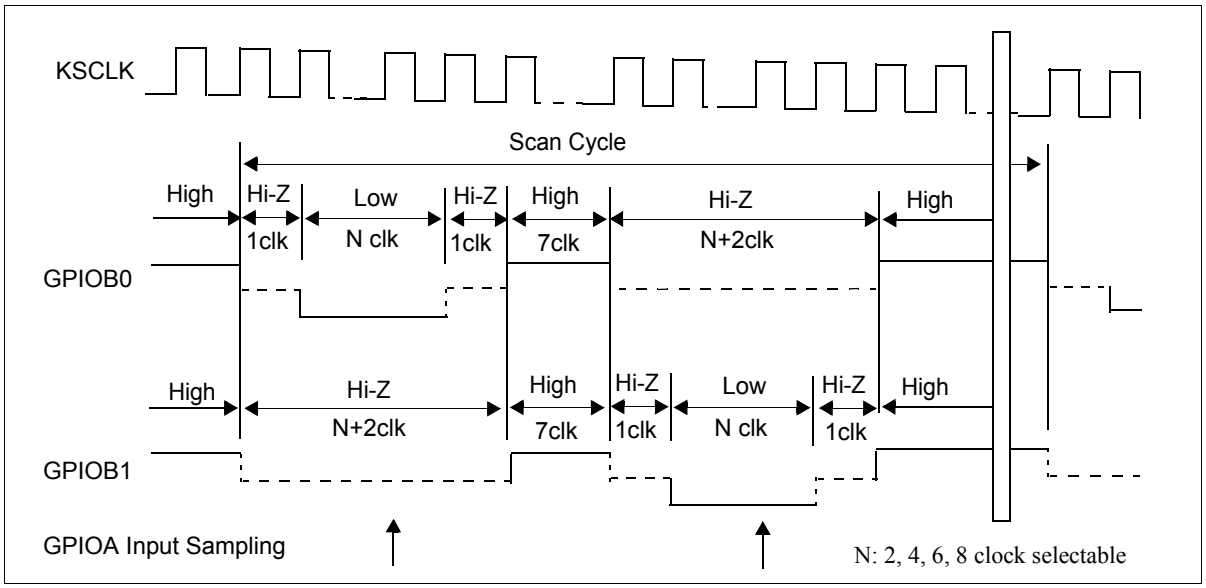


Figure 12-13: Key-scan Timing (High drive mode)

12.1.17 Hi-Z Drive Mode

In the Hi-Z drive mode, the Hi-Z is output after low level is output. The expected pull-up resistor must add to recognize the high level for the scan clock.

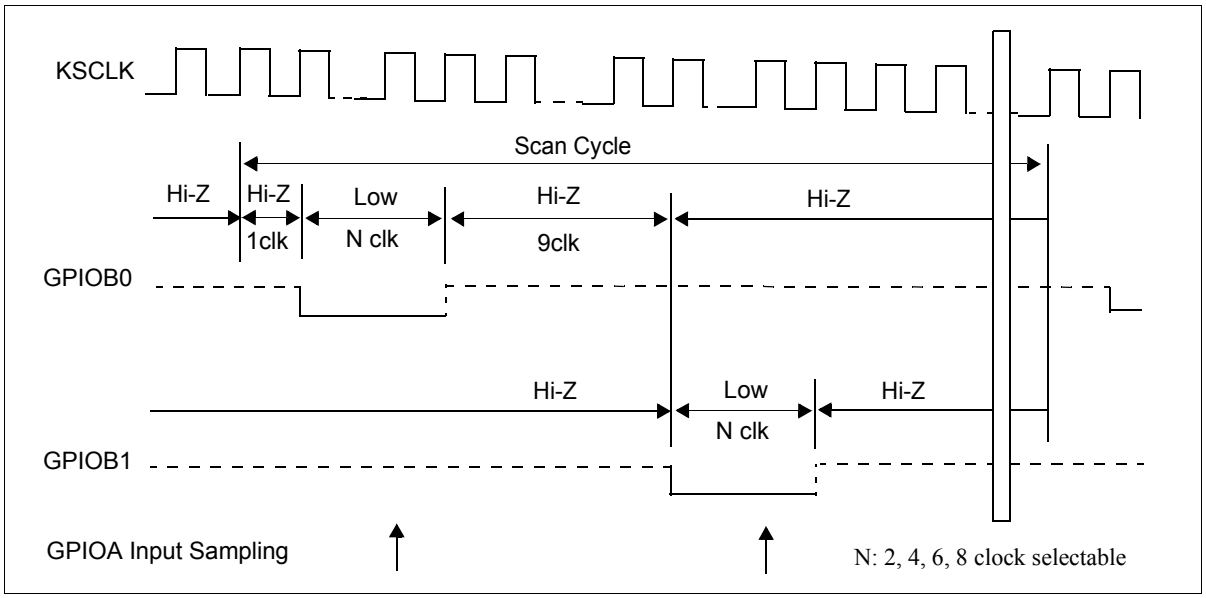


Figure 12-14: Key-scan Timing (Hi-Z drive mode)

12.1.18 Scan Clock

The scan clock frequency (KSCLK) and the scan cycle are set according to the Key-scan command.

Table 12-5: Scan Clock Frequency

Scan Clock Frequency
12MHz
6MHz
3MHz
1.5MHz

Table 12-6: Scan Cycle

Scan Cycle
1.365ms
2.731ms
5.461ms
10.92ms

12.1.19 Key-scan Event

The key-scan interface generates the event notification when the scan data is changed.

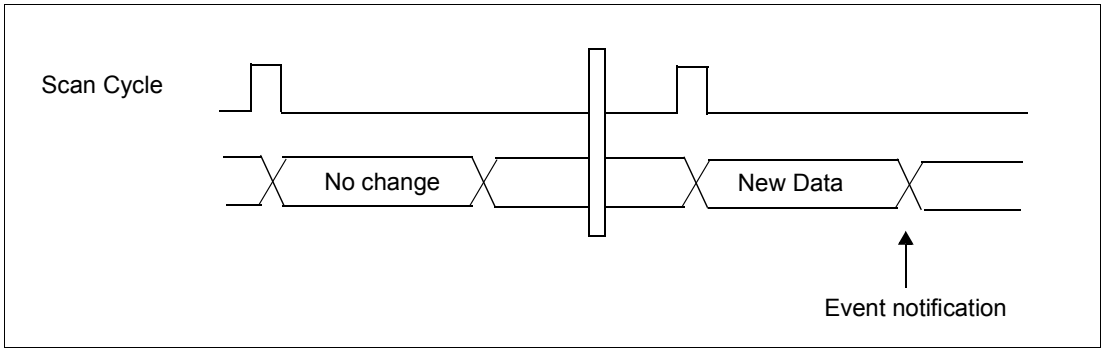


Figure 12-15: Key-scan Event

12.1.20 Buzzer Interface

The buzzer interface can be used for the beep sound that ring synchronizing with the touch screen. The on term of the buzzer can be controlled with hardware.

The buzzer interface controls operation mode and buzzer on term by using the Buzzer command. For further information on the Buzzer command, see S1D13U11 Software Technical Manual.

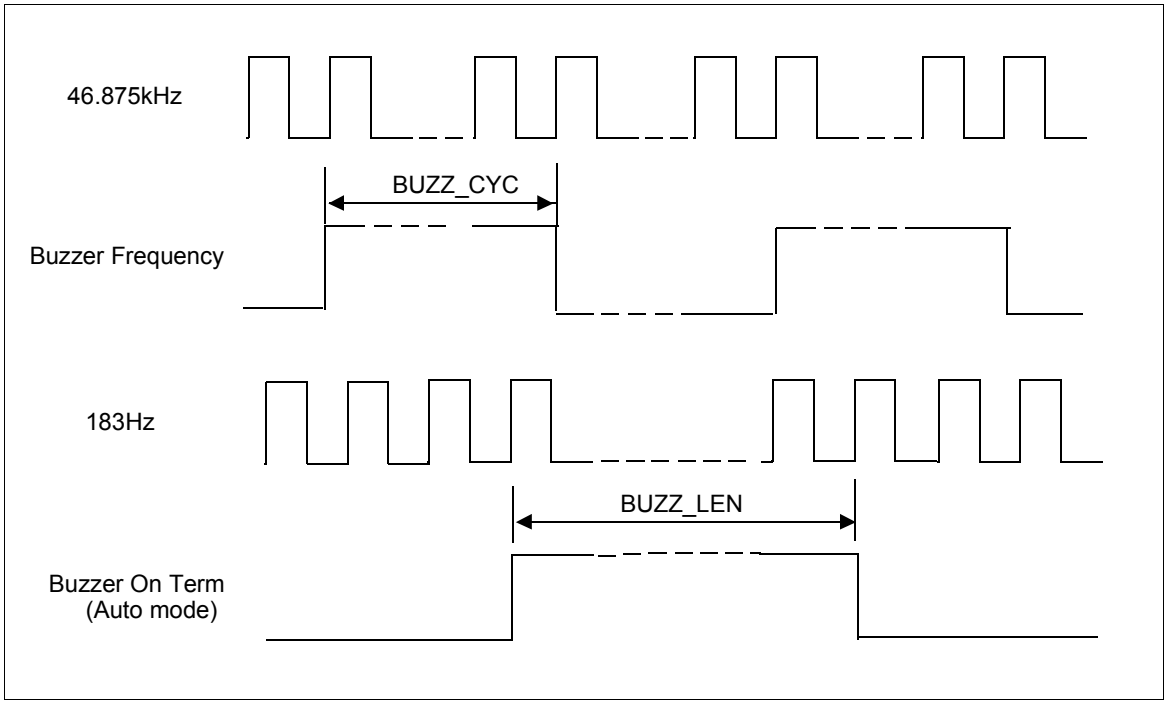


Figure 12-16: Buzzer Timing

12.1.21 Buzzer Clock

The frequency (BUZZ_CYC) of the buzzer and buzzer on term (BUZZ_LEN) are set according to the Buzzer command.

Table 12-7: Buzzer Frequency

BUZZ_CYC
46.88kHz
23.43kHz
...
183Hz

Table 12-8: Buzzer On Term

BUZZ_LEN
100ms
200ms
...
1500ms

12.1.22 Buzzer Auto Mode

The buzzer automatically is turned off after the buzzer is turned on for a set on term.

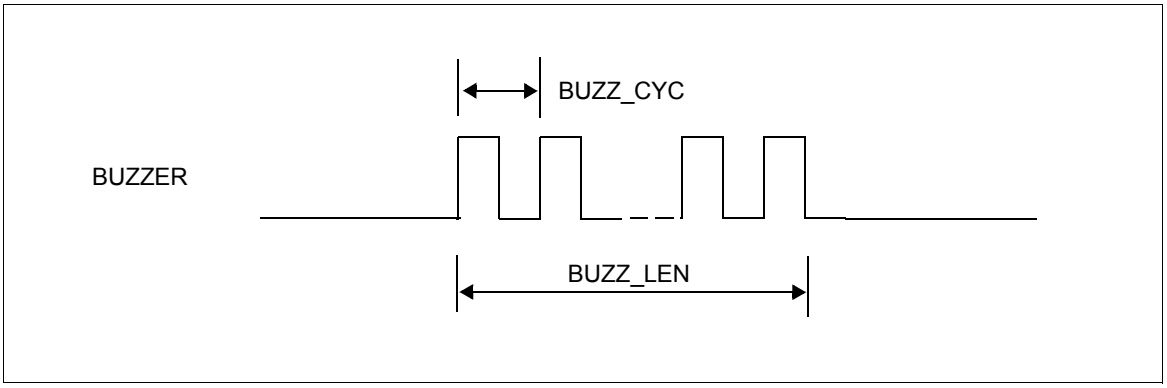


Figure 12-17: Buzzer Auto Mode

Chapter 13 Event Notification

13.1 Event Notification Function

Event Notification is the function used to inform host CPU of interrupts via end point 3 of the USB. The host CPU receives the event factor and the attached data (event block) by interrupt IN transfer. Only one event factor is included in a event notification. The event will be notified by the time series when there are two or more factors. A maximum of 10 events can be stored. A new event will not be stored when the event factor to exceed it is generated.

Each event factor can be enabled or disabled. For further information on the event notification, see the S1D13U11 Software Technical Manual.

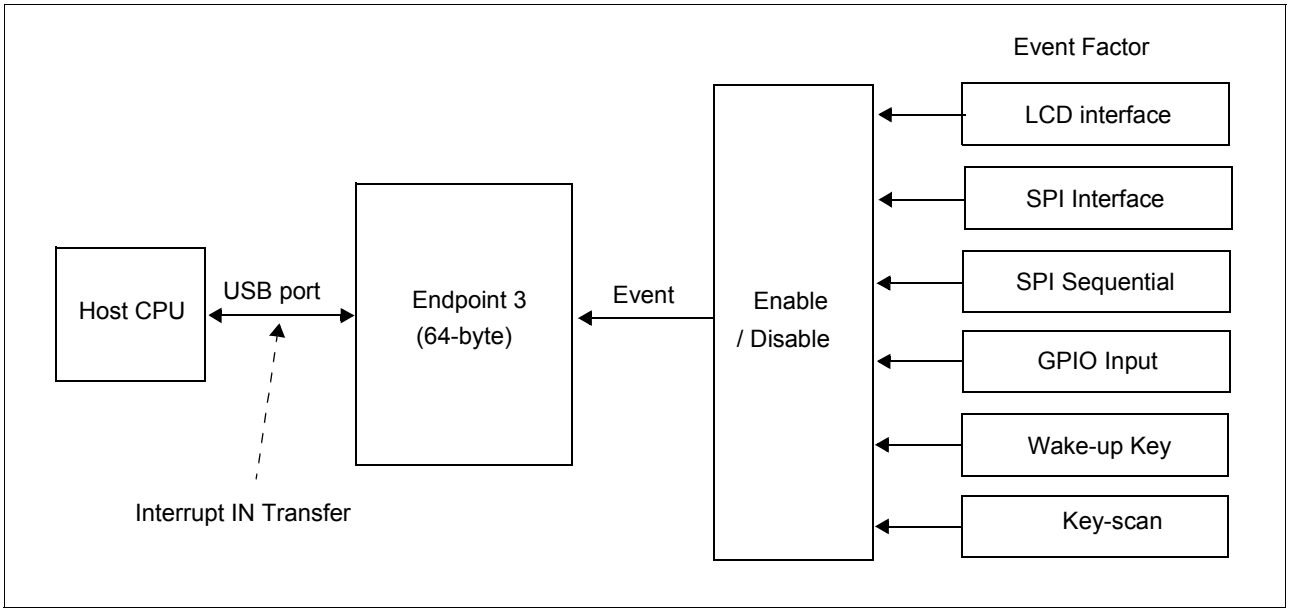


Figure 13-1: Event Notification Function

13.1.1 LCD Interface Event

The LCD interface event notifies the host CPU of an LCD interface interrupt (Alpha-blend completion).

13.1.2 SPI Interface Event

The SPI interface event notifies the host CPU of an input interrupt on the INT0 pin (interrupt of the device connected with SPI interface channel 0). Only SPI sequential event is generated when synchronizing with SPI sequential command and this interrupt.

13.1.3 SPI Sequential Event

The SPI sequential event notifies the host CPU when data is received from SPI interface. The read data from the device connected with the SPI interface is contained as an event block.

13.1.4 GPIO Input Event

The GPIO input event notifies the host CPU that the GPIO input interrupt has occurred. The GPIO input status and interrupt pin name are contained as an event block.

13.1.5 Wake-up Key Event

The wake-up key event notifies the host CPU when an INT1 pin interrupt occurs (wake-up key input generation).

13.1.6 Key-scan Event

The key-scan event notifies the host CPU when there is a change in the key-scan data.

13.2 Sleep Event Notification

Only the input of the INT0 pin (SPI interface interrupt) and the INT1 pin (wake-up key) is accepted while in sleep mode. The return sequence starts from sleep when the interrupt level matches the setting value. This event is notified to the host CPU after it returns.

Chapter 14 Power Save

14.1 Power Management

There are three power states (reset, active and sleep) in the S1D13U11. All clocks, including crystal oscillation, stop in sleep mode. The return from sleep mode has the factor of the USB resume, USB bus reset, the INT0/INT1 input, and the VBUS change (low to high). The transition to sleep mode has the factor of the USB suspend and the VBUS change (high to low).

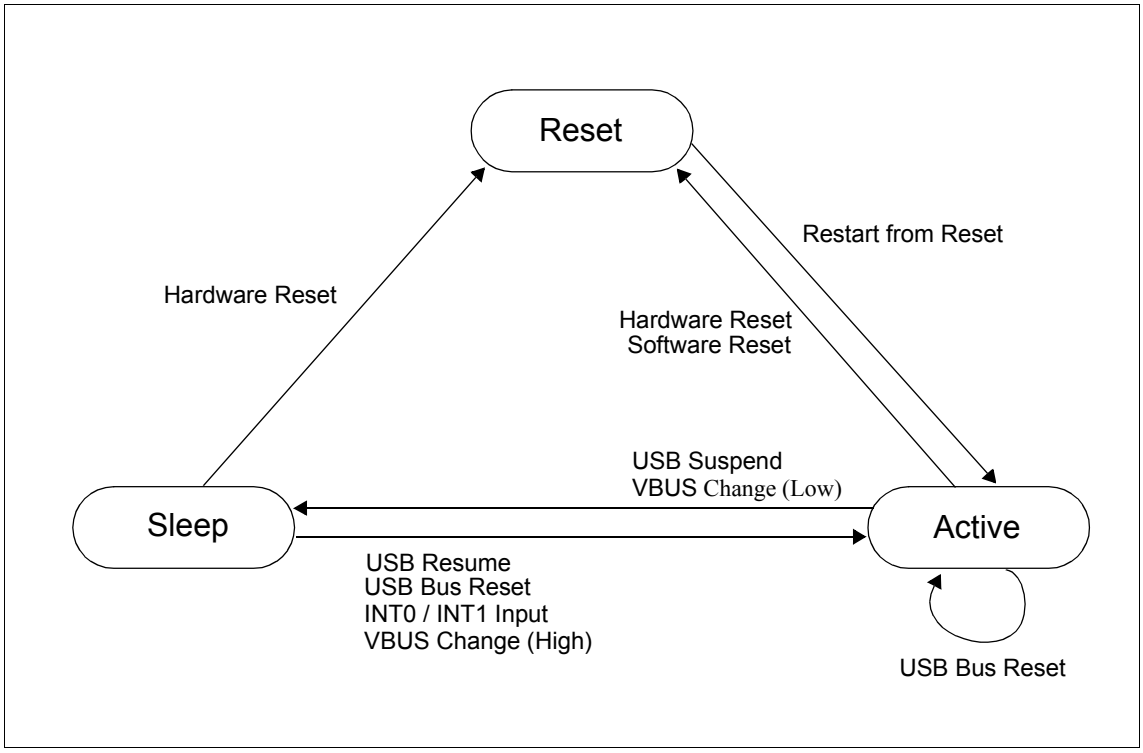


Figure 14-1: Power State Description

The power status of sleep and active are as follows.

Table 14-1: Power Status

Power Status	Crystal Oscillator	USB Device Port	LCD Interface	SDRAM
Sleep	Stop	Stop	Stop	Stop (note)
Active	Run	Run	Run	Run

Note
SDRAM can select self-refresh or power down.

14.2 USB Suspend

USB suspend uses a different transition method depending on whether HS mode or FS mode is used. The use of USB resume is prohibited within 5ms of a transition to FS mode.

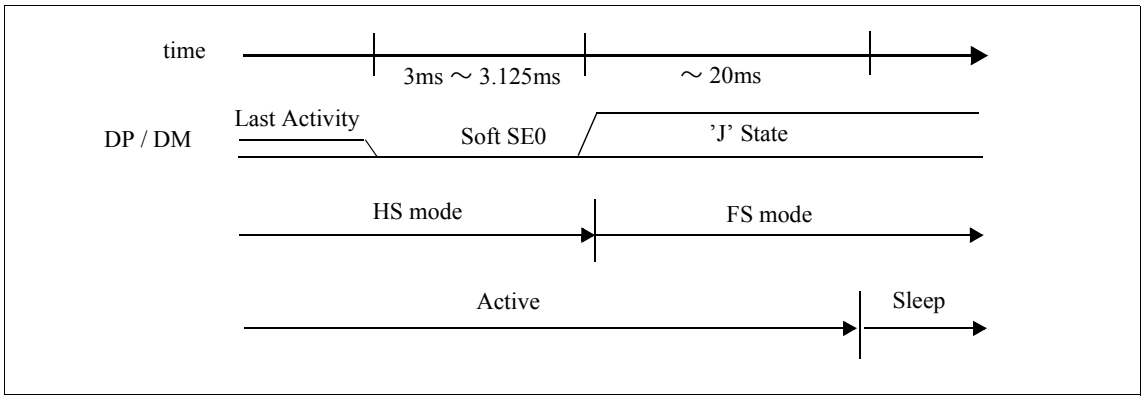


Figure 14-2: USB Suspend (HS mode)

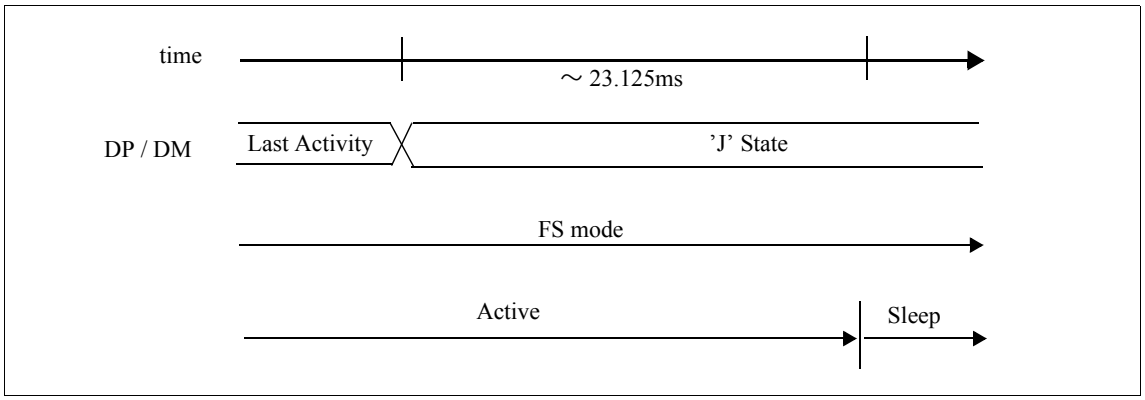


Figure 14-3: USB Suspend (FS mode)

14.3 USB Resume

The USB resume signaling is shown in the following diagram.

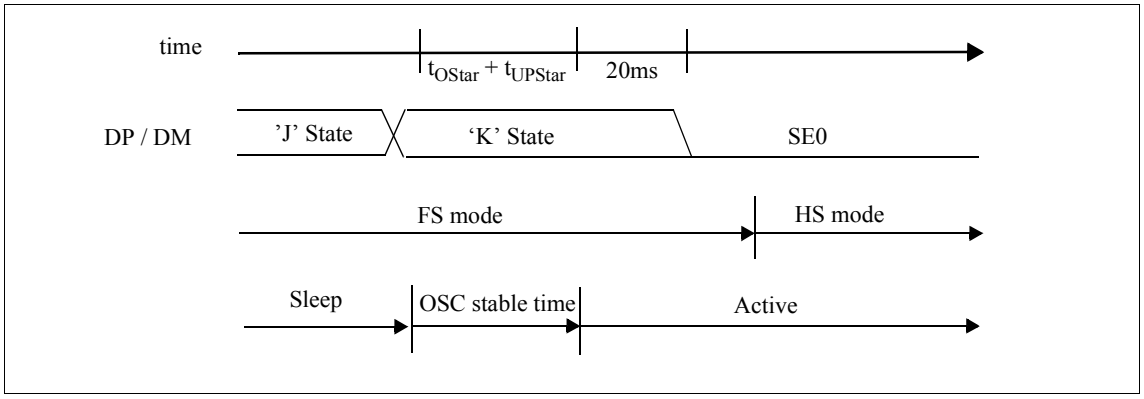


Figure 14-4: USB Resume

14.4 USB Remote Wake-up

The USB remote wake-up issues the resume command to the USB host and returns from the sleep simultaneously.

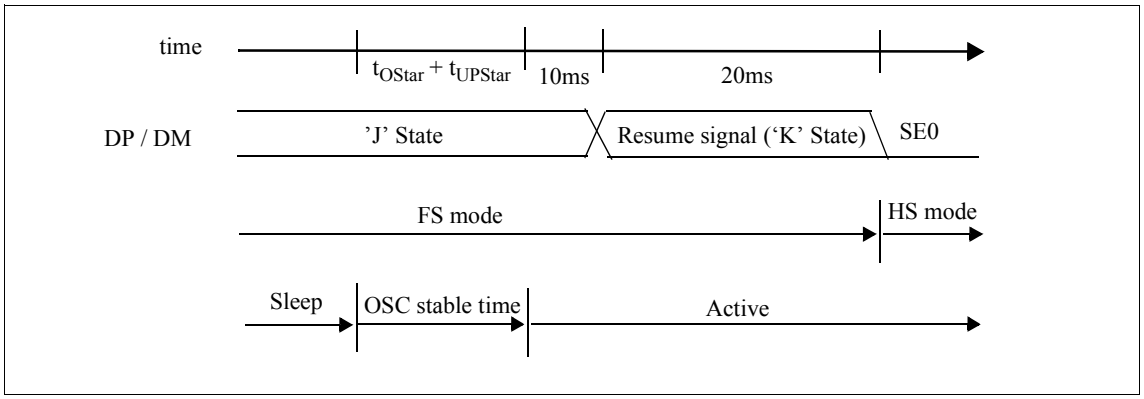


Figure 14-5: USB Remote Wake-up

Chapter 15 Use Case Examples (LCD Interface)

15.1 Sleep

The LCD interface can be active without host CPU control when the following sequences are set to the LCD wake-up command. For further information on the LCD wake-up command, see the S1D13U11 Software Technical Manual.

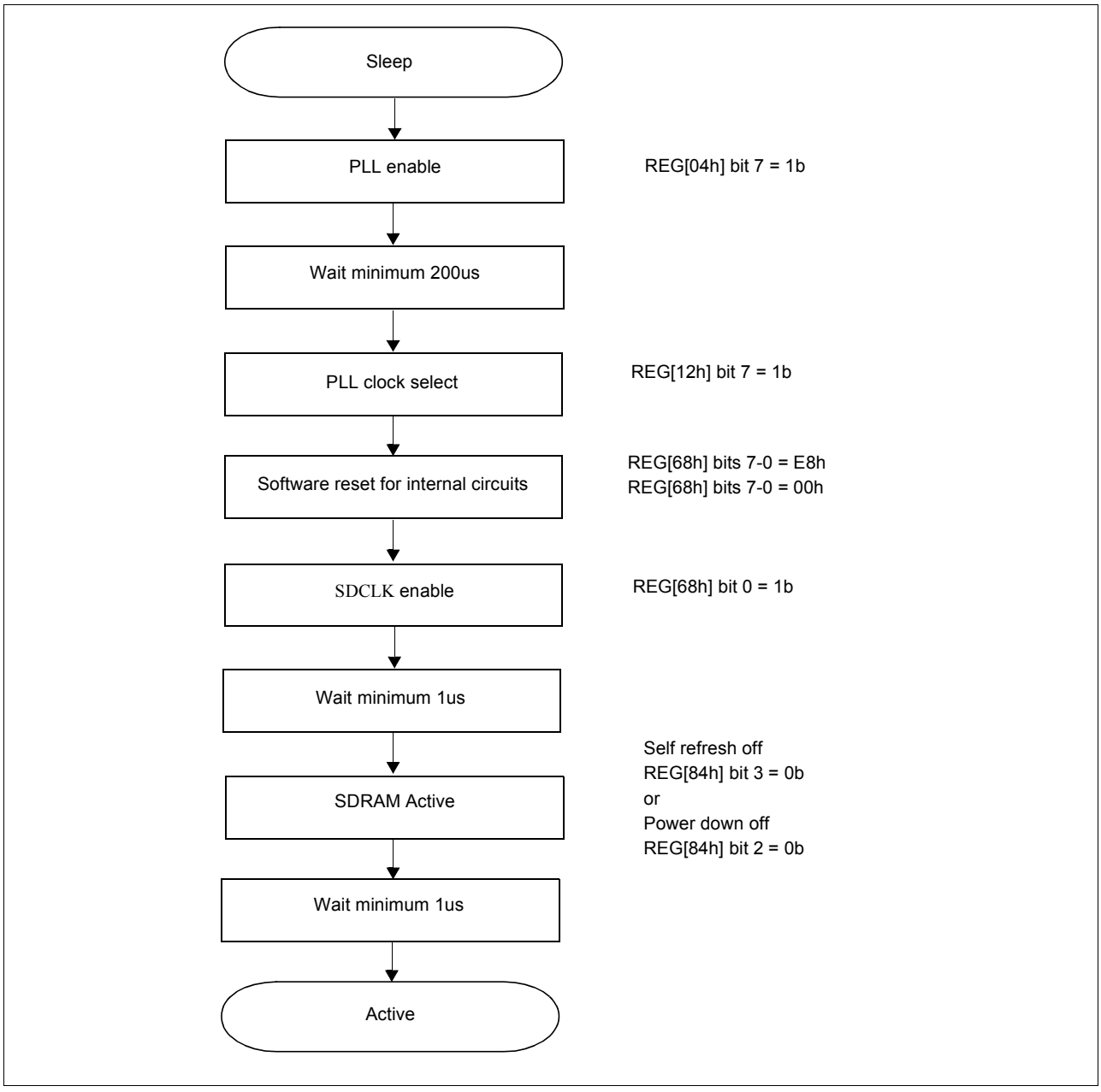


Figure 15-1: Return from Sleep Flow

The LCD interface can be placed in sleep mode without host CPU control when the following sequences are set to the LCD wake-up command. For further information on the LCD wake-up command, see the S1D13U11 Software Technical Manual.

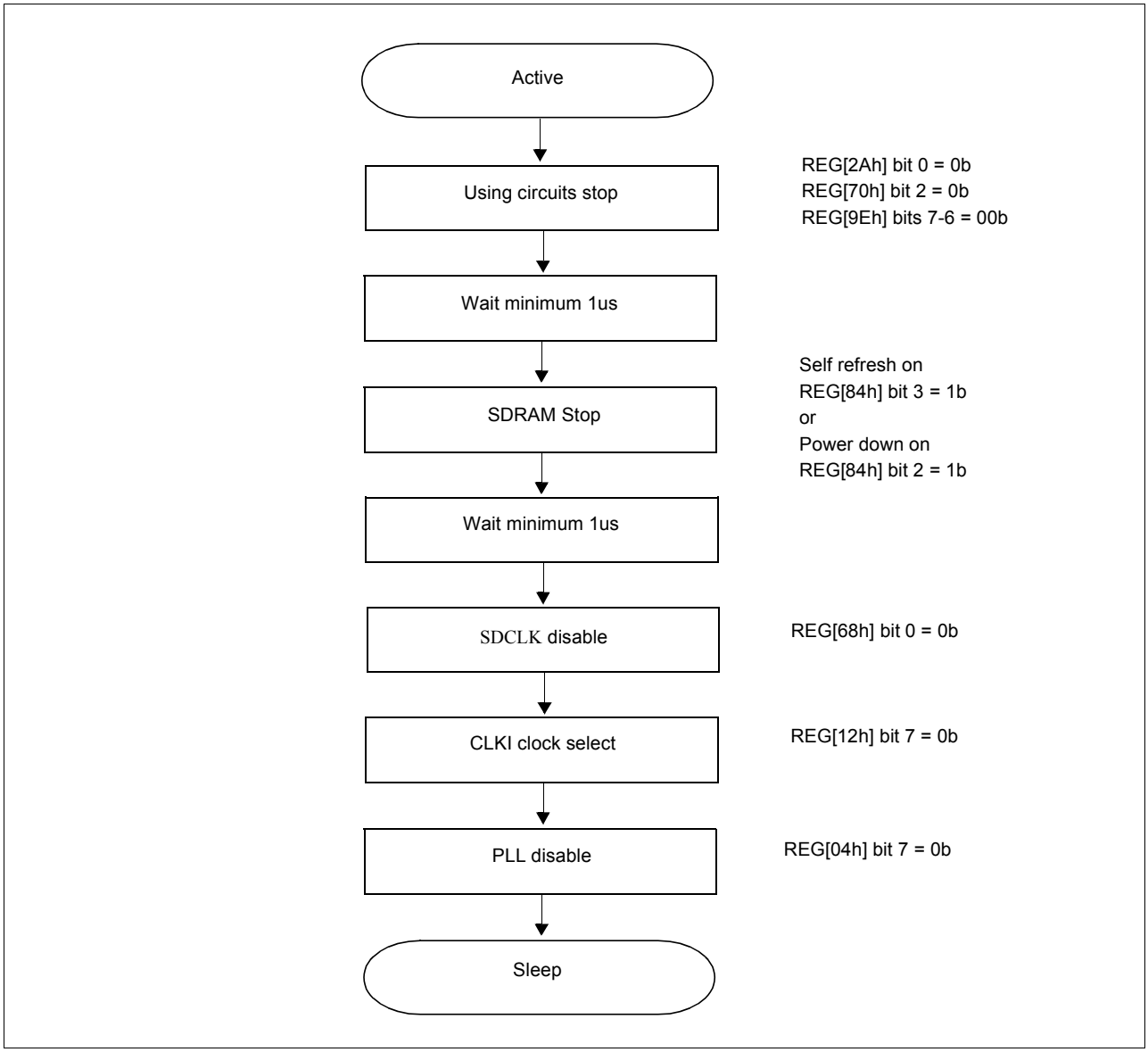


Figure 15-2: Entering Sleep Mode

15.2 Initialization Sequence

The following steps are required to initialize the S1D13U11.

Example conditions:

- CLKI: 24MHz
- PCLK: 32MHz
- SDRAM clock: 96MHz
- LCD panel: 800x480 (24bpp)
- SDRAM: 64 Mbit
- SS: is enabled.

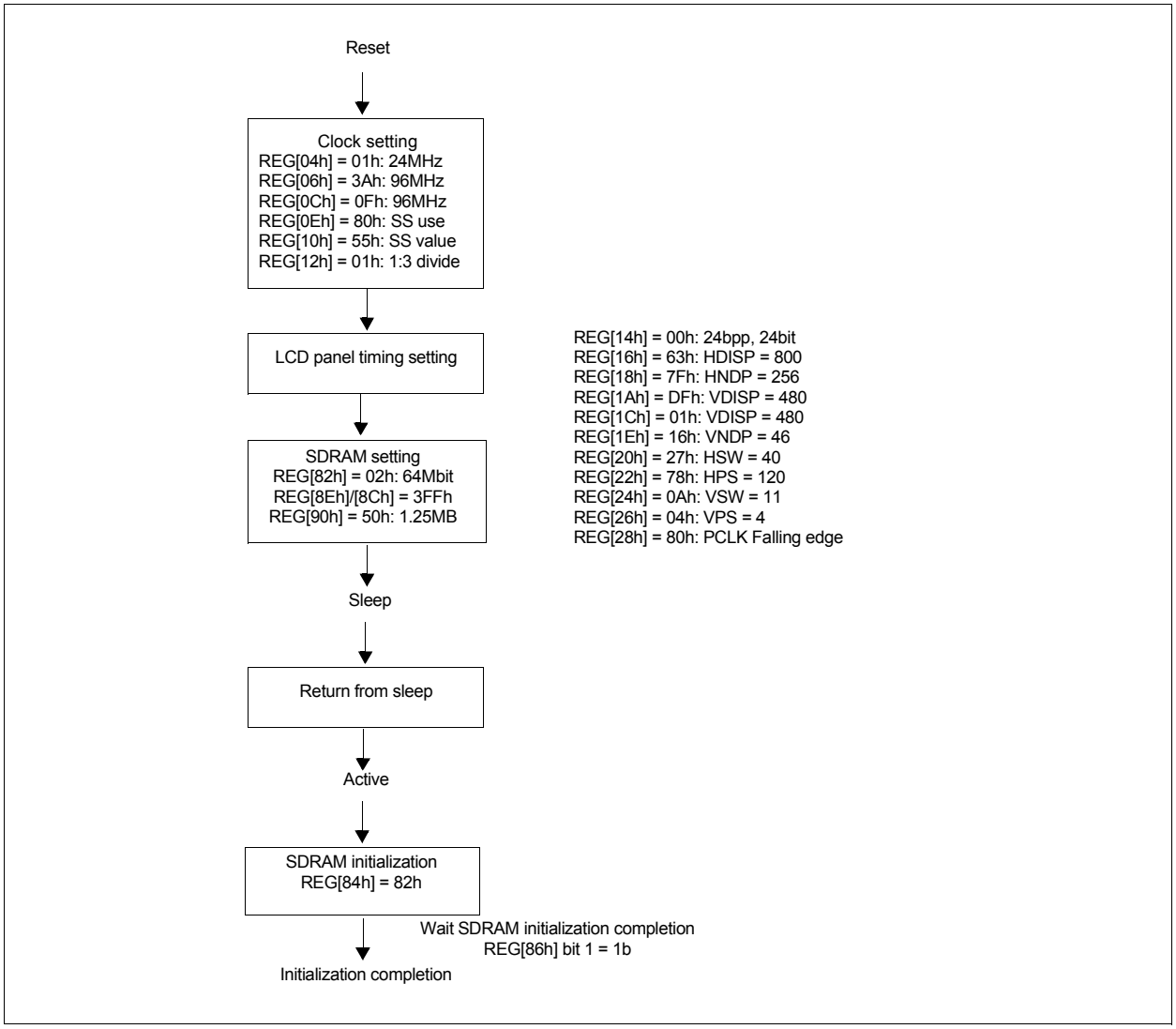


Figure 15-3: Initialization Sequence Example

15.3 LCD Display Sequence

The following steps are needed to display an image with the S1D13U11.

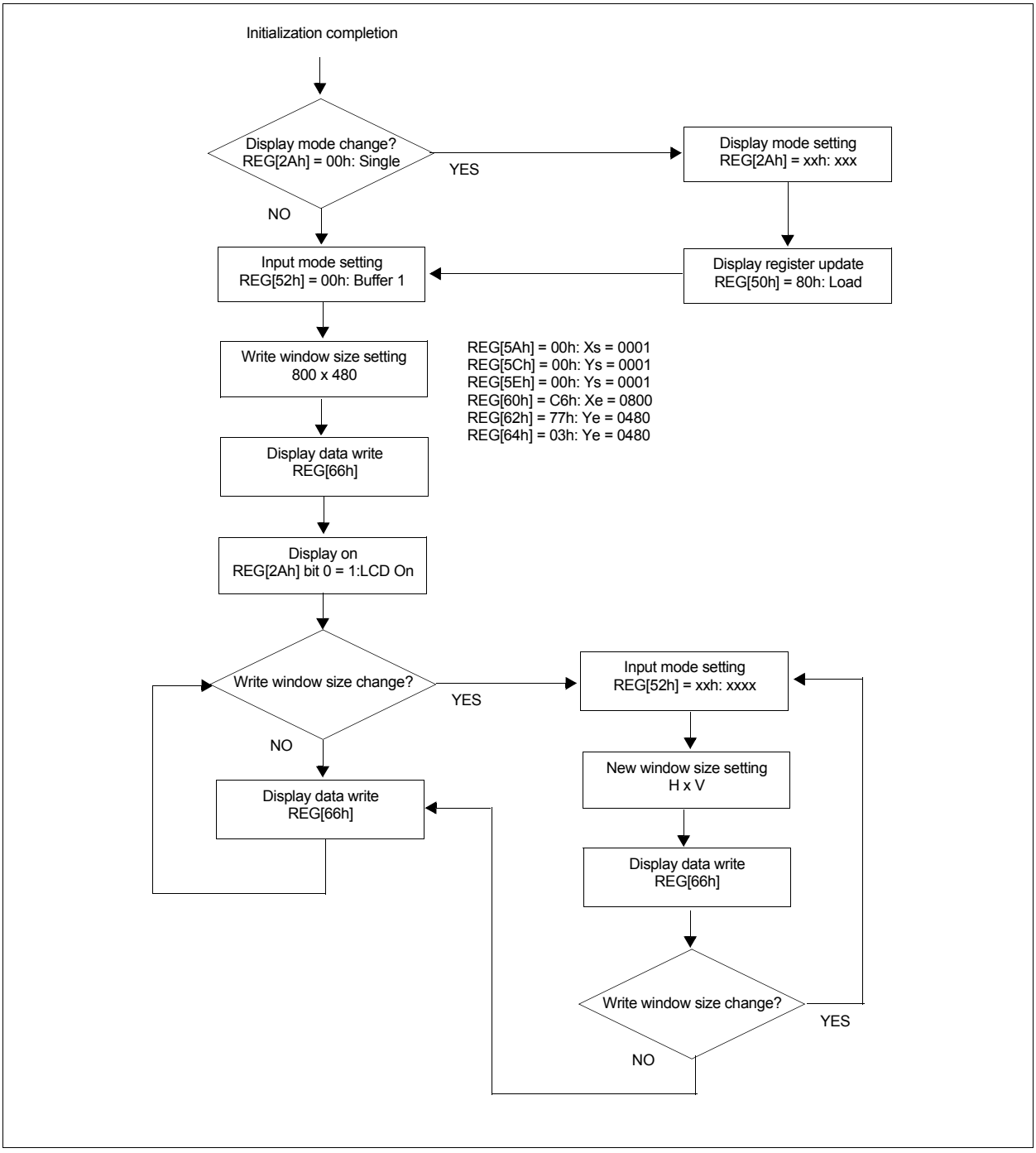


Figure 15-4: LCD Display Sequence Example

15.4 Wake-up Display Sequence

Wake-up display can be performed without host CPU control when the following sequences are set to the LCD wake-up command. For further information on the wake-up display, see the S1D13U11 Software Technical Manual.

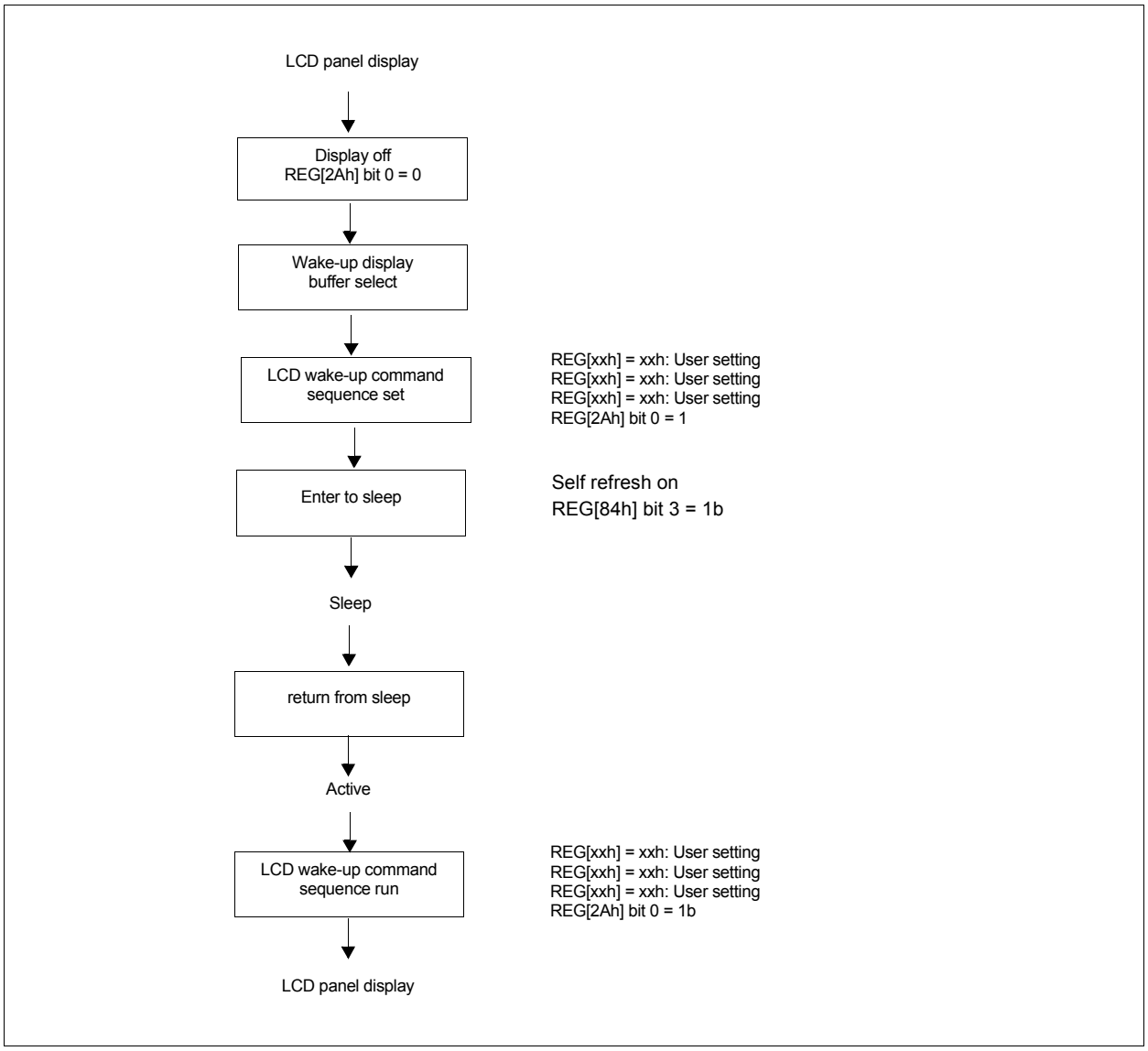


Figure 15-5: Wake-up Display Sequence Example

15.5 Start-up Display Sequence

The start-up display can be performed without host CPU control when the following sequences are stored into the external serial flash memory. For further information on the start-up display, see the S1D13U11 Software Technical Manual.

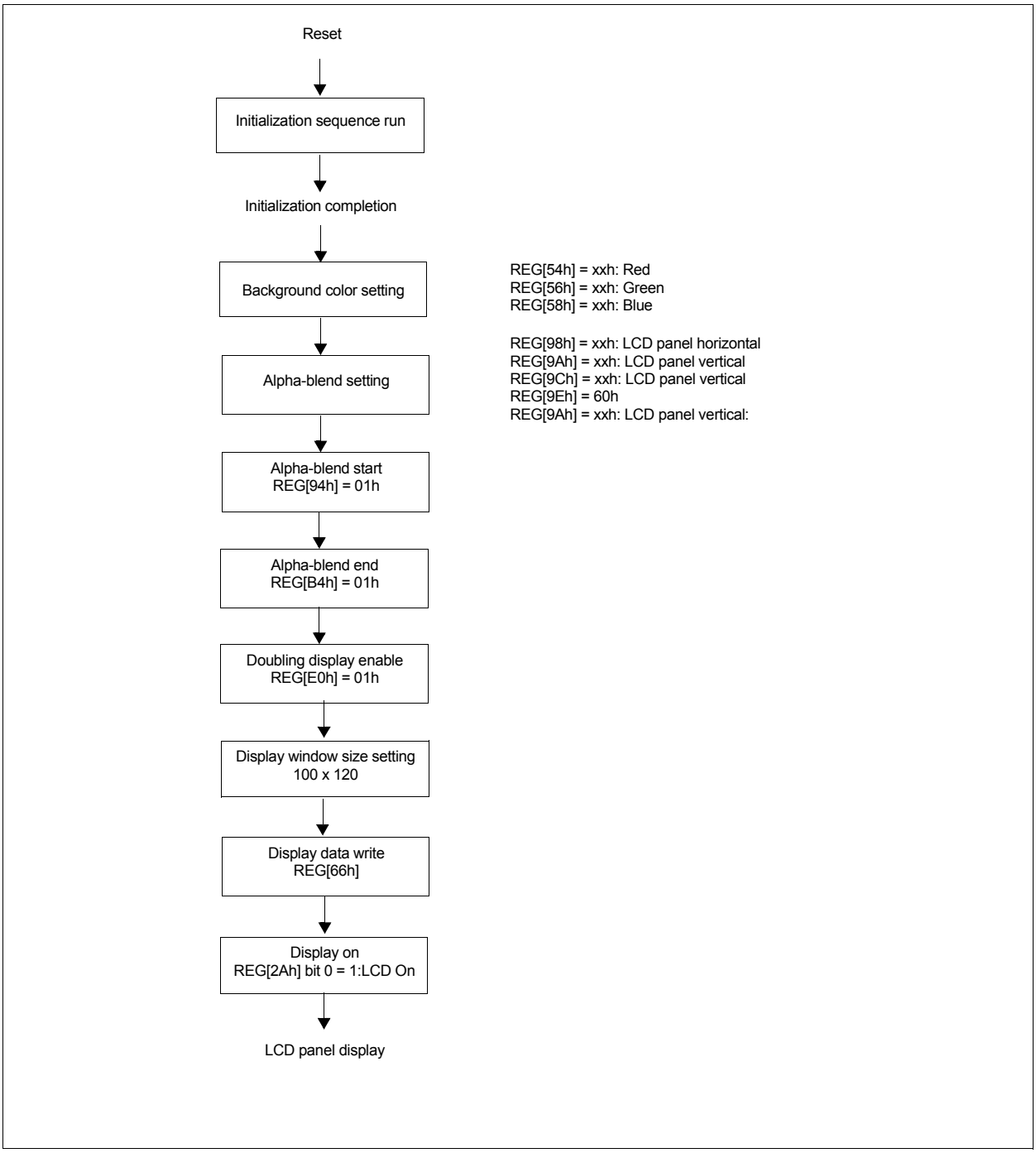


Figure 15-6: Start-up Display Sequence Example

Chapter 16 External Components

16.1 OSC

For the external components of the crystal oscillator, consult the crystal manufacturer.

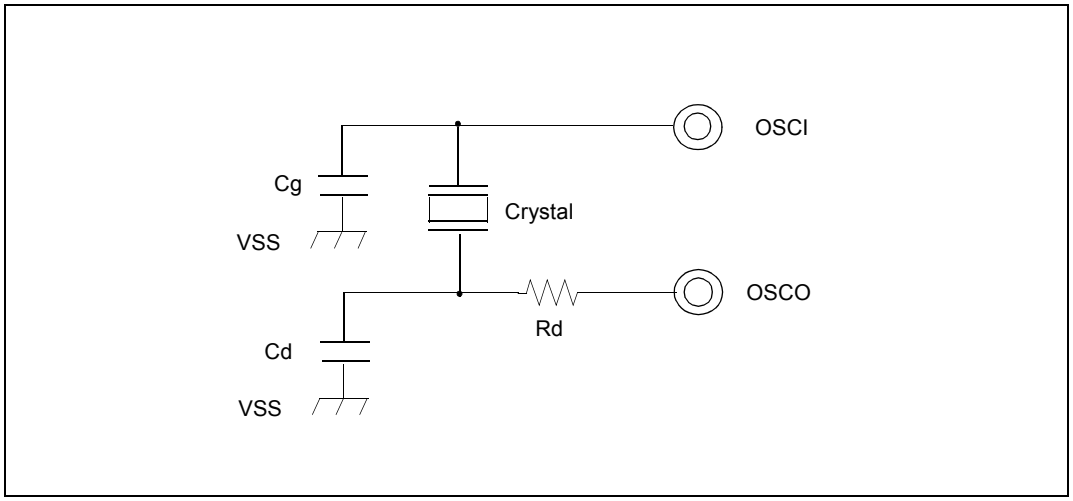


Figure 16-1: Crystal Oscillator External Component

16.2 Guidelines for PLL Power Layout

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible.

The following are guidelines which, if followed, will result in cleaner power to the PLL, resulting in a cleaner and more stable clock. Even a partial implementation of these guidelines will give results.

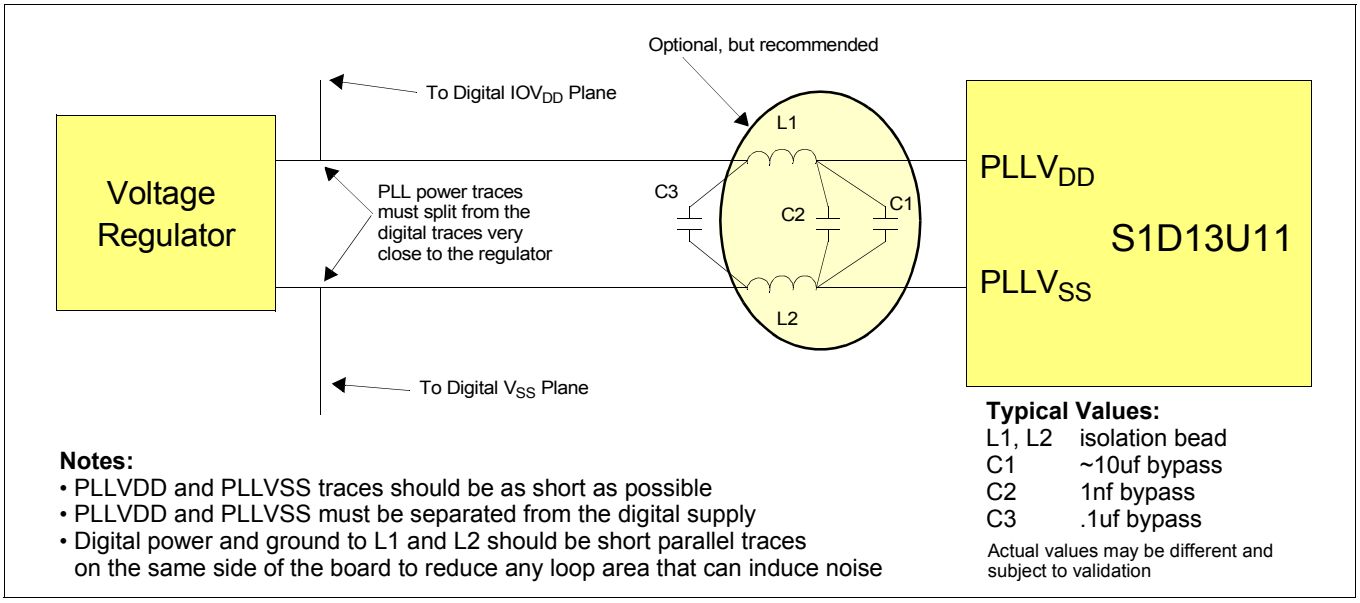


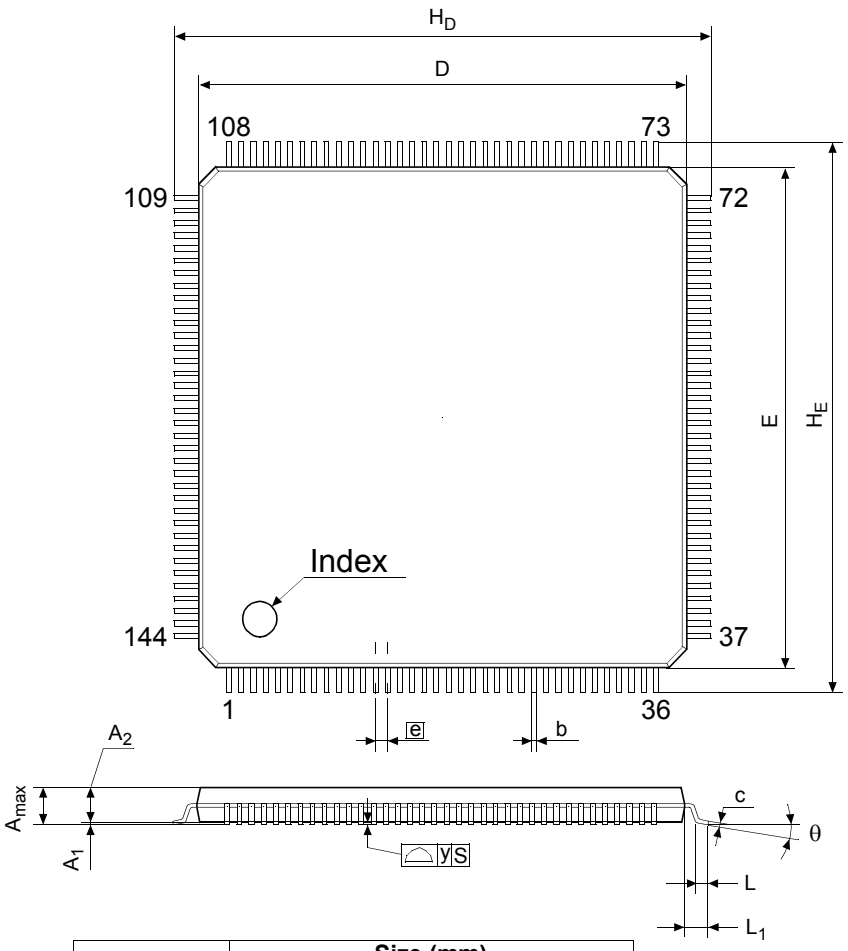
Figure 16-2: PLL Power Layout

- Place the ferrite beads (L1 and L2) parallel to each other with minimal clearance between them. Both bypass caps (C2 and C3) should be as close as possible to the inductors. The traces from C3 to the power planes should be short parallel traces on the same side of the board with just the normal small clearance between them. Any significant loop area here will induce noise. If there is a voltage regulator on the board, try to run these power traces directly to the regulator instead of dropping to the power planes (still follow above rules about parallel traces).
- The analog ground point where bypass cap (C2) connects to the ground isolation inductor (L2) becomes the analog ground central point for a ground star topology. None of the components connect directly to the analog ground pin of the MGE ($PLLV_{SS}$) except for a single short trace from C2 to the $PLLV_{SS}$ pin. The ground side of the large bypass capacitor (C1) should also have a direct connection to the star point.
- The same star topology rules used for analog ground apply to the analog power connection where L2 connects to C2.
- All of the trace lengths should be as short as possible.

- If possible, have all the PLL traces on the same outside layer of the board. The only exception is C1, which can be put on the other side of the board if necessary. C1 does not have to be as close to the analog ground and power star points as the other components.
- If possible, include a partial plane under the PLL area only (area under PLL components and traces). The solid analog plane should be grounded to the C2 (bypass) pad. This plane won't help if it is too large. It is strictly an electrostatic shield against coupling from other layers' signals in the same board area. If such an analog plane is not possible, try to have the layer below the PLL components be a digital power plane instead of a signal layer.
- If possible, keep other board signals from running right next to PLL pin vias on any layer.
- Wherever possible use thick traces, especially with the analog ground and power star connections to either side of C2. Try to make them as wide as the component pads – thin traces are more inductive.

It is likely that manufacturing rules will prohibit routing the ground and power star connections as suggested. For instance, four wide traces converging on a single pad could have reflow problems during assembly because of the thermal effect of all the copper traces around the capacitor pad. One solution might be to have only a single trace connecting to the pad and then have all the other traces connecting to this wide trace a minimum distance away from the pad. Another solution might be to have the traces connect to the pad, but with thermal relief around the pad to break up the copper connection. Ultimately the board must also be manufacturable, so best effort is acceptable.

Chapter 17 Mechanical



Symbol	Size (mm)		
	Min	Typ	Max
E	-	20	-
D	-	20	-
H_E	-	22	-
H_D	-	22	-
A_{max}	-	-	1.7
A_1	-	0.1	-
A_2	-	1.4	-
e	-	0.5	-
b	0.17	-	0.27
c	0.09	-	0.2
q	0°	-	10°
L	0.3	-	0.75
L_1	-	1	-
y	-	-	0.08

Unit = mm

Figure 17-1: QFP20 144 Package

Chapter 18 Change Record

X96A-A-001-01 Revision 1.7 - Issued: March 15, 2018

- updated Sales and Technical Support Section
- updated some formatting

X96A-A-001-01 Revision 1.6 - Issued: August 19, 2015

- chapter 2.8 I2C Interface - Changed description from “Standard mode (100kbps) and Fast mode (400kbps) support” to “Supported I2CCLK frequencies are 117.19kHz and 468.75kHz only”.
- Table 7-12:I2C Interface Timing - Changed ti2cc specification (MIN.) from 2500ns to 2130ns.
- chapter 12.1.4 I2C Interface - Changed description from “The I2C interface is a synchronous serial interface that works only as single master mode. Standard mode (100kbps), fast mode (400kbps) and 7-bit slave address mode are supported.” to “The I2C interface is a synchronous serial interface that works only as single master mode and it supports 7-bit slave address output. The supported frequencies of I2CCLK are 117.19kHz and 468.75kHz.”.
- chapter 12.1.5 I2C Clock, Table 12-2:I2C Clock Frequency- Changed I2C Clock Frequency description: Standard 93.75kHz -> bTransferRate=01h 117.19kHz, Fast 375kHz -> bTransferRate=02h 468.75kHz

X96A-A-001-01 Revision 1.5 - Issued: September 16, 2013

- chapter 5.2.4 I/O interface - add note for RESET# state of GPIOA and GPIOB

X96A-A-001-01 Revision 1.4 - Issued: May 17, 2013

- chapter 11.3.3 Transparency - add “This function can not be used with rotation and mirror function, the REG[52h] bits 3-0 never be set to the value 9h, Ah and Bh.”

X96A-A-001-01 Revision 1.3 - Issued: January 30, 2013

- chapter 6.1 Absolute Maximum Rating - add T_{STG} to table 6-1, *Absolute Maximum Ratings*
- chapter 12.1.5 I2C Clock - add “The I2C hardware does not support the clock stretch function...” to the first paragraph
- chapter 12.1.9 Repeated Start Condition - add “The I2C hardware does not support the repeated start condition function” to the first paragraph and remove figure 12-9, *Repeated Start Condition*

X96A-A-001-01 Revision 1.2 - Issued: February 23, 2011

- chapter 12.1.14 GPIO Interrupt - remove “Both Edge” from table 12-4, *GPIO Interrupt*

X96A-A-001-01 Revision 1.1 - Issued: January 25, 2011

- chapter 2.7 SPI Interface - add supported devices for 1 M-bit serial flash

X96A-A-001-01 Revision 1.0 - Issued: January 12, 2010

- initial release of the S1D13U11 specification

Chapter 19 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html