EPSON

Speech LSI

S1V3F351 / S1V3F352
Technical Manual

SEIKO EPSON CORPORATION

Rev. 1.00

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Preface

This is a technical manual for designers and programmers who develop a product using the S1V3F351 / S1V3F352. This document describes the functions of the IC, embedded circuit operations, and their control methods.

Notational conventions and symbols in this manual

Control bit read/write values

This manual describes control bit values in a hexadecimal notation except for one-bit values (and except when decimal or binary notation is required in terms of explanation). The values are described as shown below according to the control bit width.

1 bit	= 0 or 1
2 to 4 bits	= 0x0 to 0xF
5 to 8 bits	= 0x00 to 0xFF
9 to 12 bits	= 0x000 to 0xFFF
13 to 16 bits	= 0x0000 to 0xFFFF
Decimal	= 0 to 9999...
Binary	= 0b0000... to 0b1111...

Message names

There is a REQ message that has two or more functions, and an IND message that acquires various status information and data. In this manual, they are described as follows:

Examples:

ISC_FLASH_PROGRAM_REQ: Write Flash message	(Write Flash Memory Data)
ISC_FLASH_PROGRAM_REQ: Sector Erase message	(Erase Flash Memory Sector)
ISC_STATUS_IND: Error / Warning Status message	(Acquire Error Information)
ISC_FLASH_PROGRAM_STATUS_IND: Read Flash message	(Acquire Flash Memory Data)

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1. Overview

The S1V3F351 / S1V3F352 is an LSI, which is most suitable for integrating to voice guidance products.

- High-compression, high-quality audio decoding algorithm
- Two-channel sound mixing play
- Playback speed conversion
- Playback pitch conversion (S1V3F351 only)
- Embedded flash memory for storing Sound ROM data
- External QSPI flash memory interface for extending Sound ROM
- Embedded DA converter
- Embedded oscillator
- Two control modes
  Host Interface mode: The functions of this IC are controlled with commands sent from a host device.
  Standalone mode: This IC operates alone by controlling pin inputs without a host connected.

This IC enables voice / audio playback from a buzzer by Epson Original Algorithm, as well as voice / audio playback from a speaker. Use of "ESPER2," which is a dedicated PC tool for this IC, allows easy generation of high-quality voice data from texts without studio recording. All the functions can be controlled via the serial host interface, this makes it possible to implement voice / audio playback functions to an existing system with a host MCU. Standalone mode, which controls voice / audio playback using pin inputs without using the host interface, can also be selected. The S1V3F351 / S1V3F352 enables shortening of time-to-market for products with voice guidance functions.

1.1 Features

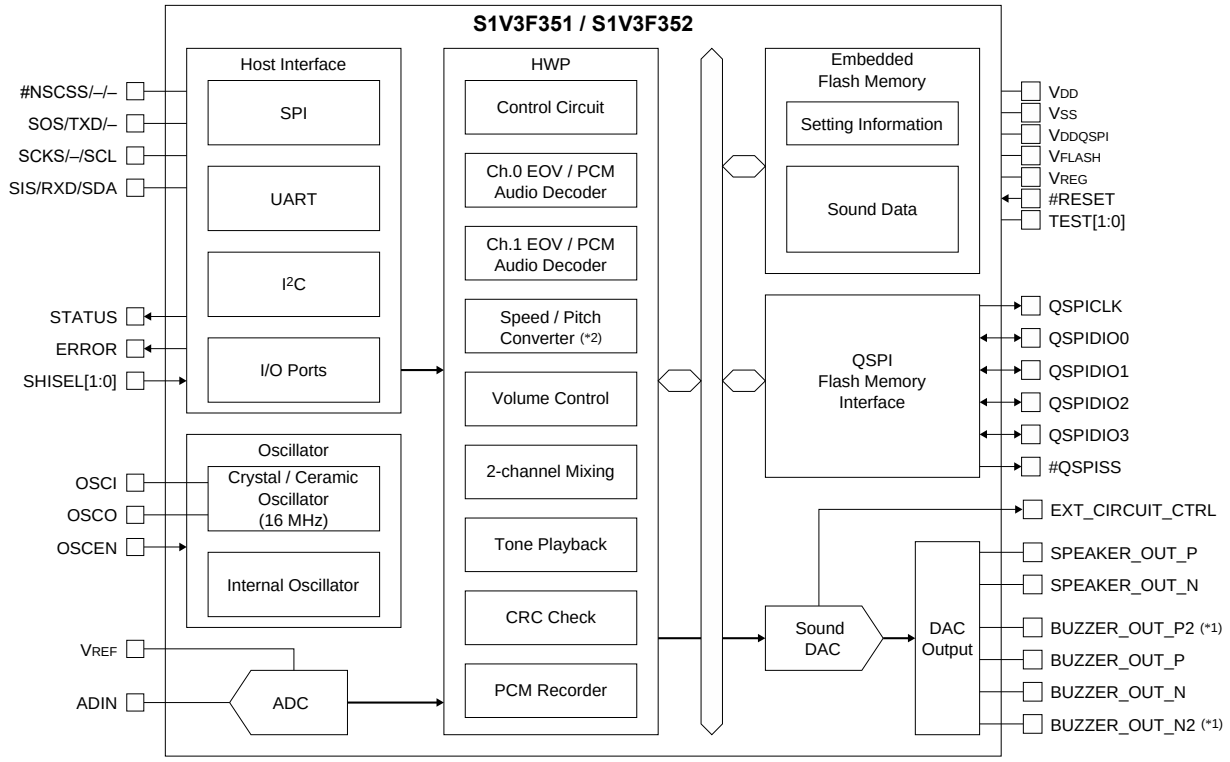
Table 1.1 Features

Model	S1V3F351	S1V3F352
SOUND PLAYBACK		
Sound Formats		
EPSON original high-compression / high-quality audio format (EOV)	16 / 24 kbps, 15625 Hz	16 / 24 / 32 / 40 kbps, 15625 Hz
Uncompressed audio format (PCM)	16 bits	
Sound Processing Functions		
Sound mixing	2-channel mixing playback (e.g., Ch.0: Voice, Ch.1: BGM)	
Playback speed conversion function	75% to 125% (5% steps), supported only in Ch.0	
Playback pitch conversion function	75% to 125% (5% steps), supported only in Ch.0	–
Tone generation function	Patterned tone output with a combination of a maximum of four tone frequencies	
Sound data protection	Available	
Repeat playback	1 to 254 times or endless	
Volume setting	0 dB to -63 dB (0.5 dB steps) or silence	
Sound recording function	Usable when an external QSPI flash memory is connected	
Sound ROM Data		
Maximum phrase count for sequence playback	64 phrases per 1 sentence	
Programmable delay time between phrases	Ch.0: 0 (gapless) to 2000 ms (25 ms steps) Ch.1: 25 ms to 2000 ms (25 ms steps)	
Multiple Sound ROMs	Supported only in Host Interface mode	
Sound Control Commands		
Main commands	Start / Stop / Mute	

1. Overview

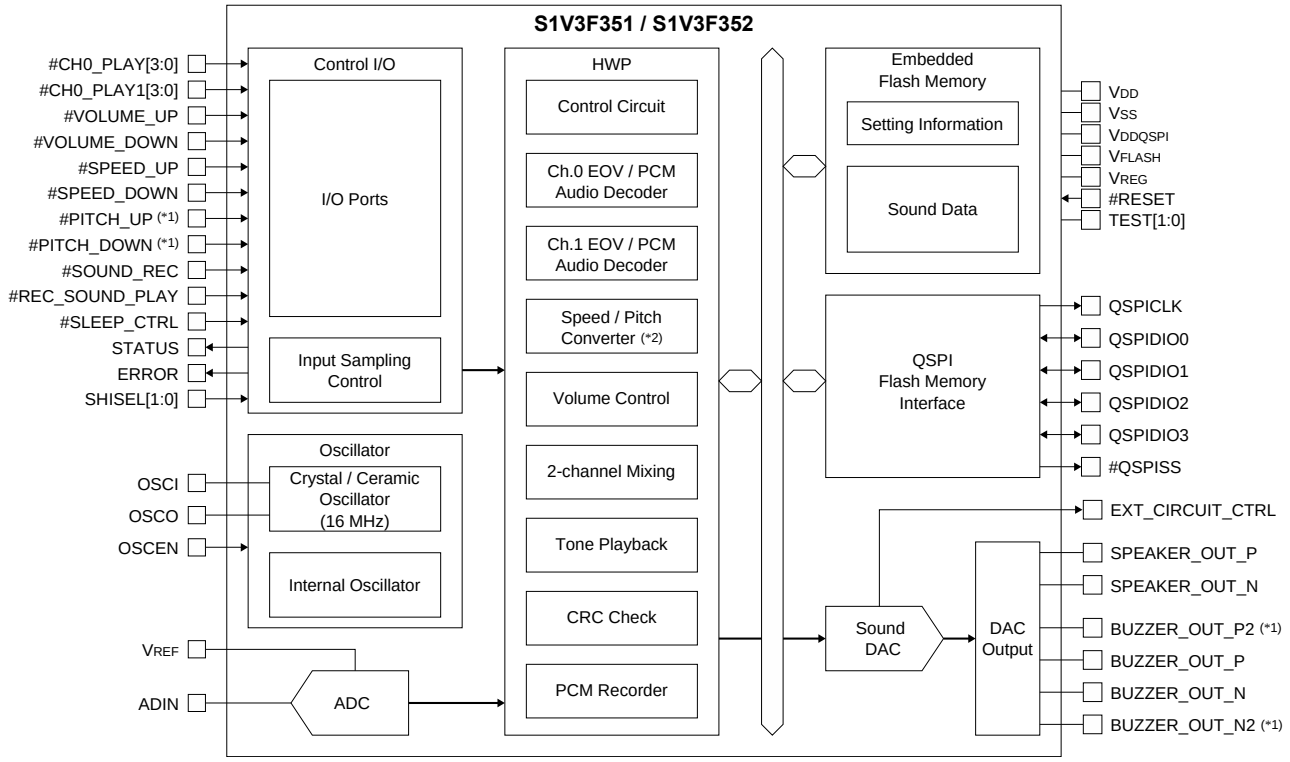
Model	S1V3F351	S1V3F352
HOST INTERFACE		
Synchronous serial interface (SPI)	One channel of these interfaces can be used.	
UART		
I^2C		
STANDALONE MODE		
Standalone playback	Maximum 30 sentences can be played using the #CHn_PLAY[3:0] pins x 2 channels without using the host interface.	
EMBEDDED FLASH MEMORY		
Capacity	64K bytes (About 30 seconds of data at EOV 16 kbps can be stored.)	160K bytes (About 80 seconds of data at EOV 16 kbps can be stored.)
Erase / program count	1000 times (Min.)	
EXTERNAL SERIAL FLASH MEMORY INTERFACE		
Quad synchronous serial interface (QSPI)	1 channel A QSPI flash memory that supports XIP (eXecute-In-Place) mode can be connected.	
SOUND OUTPUT		
Speaker output	1 channel	
Electromagnetic / piezo buzzer output	1 channel	
STANDBY MODE		
Supported standby mode	Sleep and Deep Sleep mode	
POWER SUPPLY VOLTAGE		
V_{DD} operating voltage	1.8 V to 5.5 V	
V_{DD} operating voltage for Flash programming	2.2 V to 5.5 V	2.4 V to 5.5 V
QSPI-Flash interface power supply voltage (V_{DDQSPI})	3.0 V to 3.6 V	
OPERATING TEMPERATURE		
Operating temperature range	-40°C to 85°C	
CURRENT CONSUMPTION (Typ. value)		
During idle	4.6 mA (internal oscillation)	5.8 mA (internal oscillation)
During playing	7.4 mA (internal oscillation)	7.2 mA (internal oscillation)
During standby	0.34 µA (Deep Sleep mode)	0.46 µA (Deep Sleep mode)
SHIPPING FORM		
Package	TQFP12-48PIN (P-TQFP048-0707-0.50, 7 x 7 mm, t = 1.2 mm, 0.5 mm pitch)	

1.2 Block Diagram



*1 These pins are available only for S1V3F351.
*2 Pitch Converter is available only for S1V3F351.

Figure 1.1 Block Diagram (Host Interface Mode)



*1 These pins are available only for S1V3F351.
*2 Pitch Converter is available only for S1V3F351.

Figure 1.2 Block Diagram (Standalone Mode)

1.3 Pin Assignment Diagram

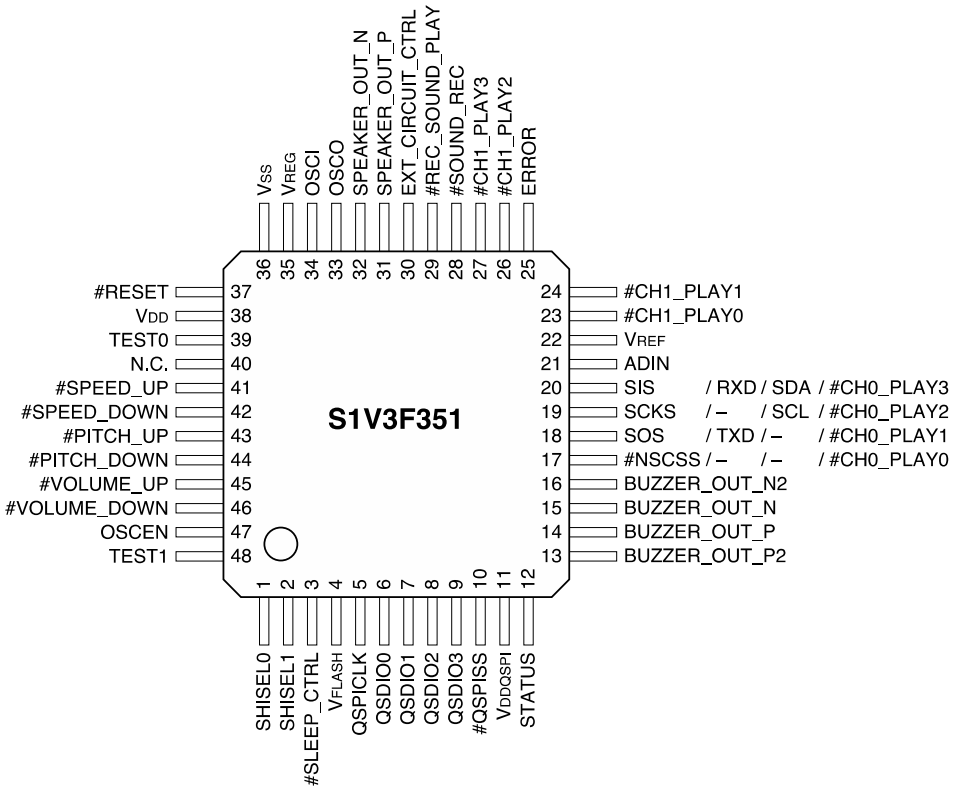


Figure 1.3 S1V3F351 (P-TQFP048-0707-0.50)

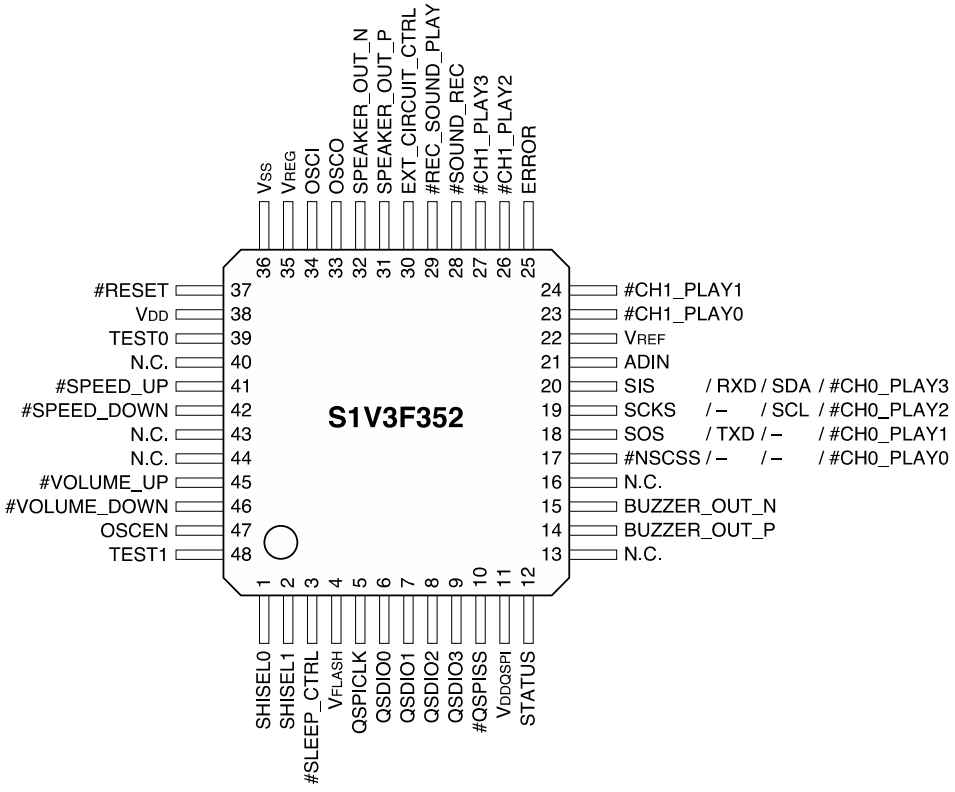


Figure 1.4 S1V3F352 (P-TQFP048-0707-0.50)

1.4 Pin Description

Symbols in pin tables

I/O: P = Power supply
A = Analog signal
I = Input

I (Pull-up) = Input with pulled up
I (Pull-down) = Input with pulled down
O = Output
I/O = Input/output
Hi-Z = High impedance state

Table 1.2 Pin Description

Pin name	Pin No.	I/O		Function
		During reset	Initial status	
V_{DD}	38	P	P	Power supply (+)
V_{SS}	36	P	P	GND
V_{DDQSPI}	11	P	P	[QSPI-Flash connected] QSPI interface power supply (3.0 V to 3.6 V) [QSPI-Flash unconnected] Power supply (V_{DD})
V_{FLASH}	4	A	A	Flash programming voltage regulator output
V_{REG}	35	A	A	V_{D1} regulator output
TEST1	48	I (Pull-down)	I (Pull-down)	Test mode enable input. Connect to V_{SS}.
TEST0	39	Hi-Z	Hi-Z	Connect to V_{SS}.
#RESET	37	I (Pull-up)	I (Pull-up)	Reset input
N.C.	40	Hi-Z	Hi-Z	Open
SHISEL0	1	Hi-Z	I	Serial host interface selection SHISEL[1:0] = LL: SPI SHISEL[1:0] = LH: UART SHISEL[1:0] = HL: I^2C SHISEL[1:0] = HH: Standalone
SHISEL1	2	Hi-Z	I	
SIS /	20	Hi-Z	I	[SPI] SIS (Serial data input)
RXD /			I	[UART] RXD (Serial data input)
SDA /			I	[I^2C] SDA (Serial data input/output)
#CH0_PLAY3			I (Pull-up)	[Standalone] CH0_PLAY3 (Ch.0 sentence select / play)
SCKS /	19	Hi-Z	I	[SPI] SCKS (Serial clock input)
– /			Hi-Z	[UART] N.C.
SCL /			I	[I^2C] SCL (Serial clock input)
#CH0_PLAY2			I (Pull-up)	[Standalone] CH0_PLAY2 (Ch.0 sentence select / play)
SOS /	18	Hi-Z	O	[SPI] SOS (Serial data output)
TXD /			O	[UART] TXD (Serial data output)
– /			Hi-Z	[I^2C] N.C.
#CH0_PLAY1			I (Pull-up)	[Standalone] CH0_PLAY1 (Ch.0 sentence select / play)
#NSCSS /	17	Hi-Z	I	[SPI] #NSCSS (Slave-select input)
– /			Hi-Z	[UART] N.C.
– /			Hi-Z	[I^2C] N.C.
#CH0_PLAY0			I (Pull-up)	[Standalone] CH0_PLAY0 (Ch.0 sentence select / play)
#CH1_PLAY3	27	Hi-Z	I (Pull-up)	[Standalone] CH1_PLAY3 (Ch.1 sentence select / play)
			Hi-Z	[SPI / UART / I^2C] N.C.
#CH1_PLAY2	26	Hi-Z	I (Pull-up)	[Standalone] CH1_PLAY2 (Ch.1 sentence select / play)
			Hi-Z	[SPI / UART / I^2C] N.C.
#CH1_PLAY1	24	Hi-Z	I (Pull-up)	[Standalone] CH1_PLAY1 (Ch.1 sentence select / play)
			Hi-Z	[SPI / UART / I^2C] N.C.
#CH1_PLAY0	23	Hi-Z	I (Pull-up)	[Standalone] CH1_PLAY0 (Ch.1 sentence select / play)
			Hi-Z	[SPI / UART / I^2C] N.C.
ERROR	25	Hi-Z	O	Error output H: An error has occurred. L: Normal
#SPEED_UP	41	Hi-Z	I (Pull-up)	[Standalone] Playback speed up
			Hi-Z	[SPI / UART / I^2C] N.C.
#SPEED_DOWN	42	Hi-Z	I (Pull-up)	[Standalone] Playback speed down
			Hi-Z	[SPI / UART / I^2C] N.C.

Pin name	Pin No.	I/O		Function
		During reset	Initial status	
#PITCH_UP	43	Hi-Z	I (Pull-up)	[Standalone (S1V3F351)] Playback pitch up
			Hi-Z	[Standalone (S1V3F352)] N.C.
			Hi-Z	[SPI / UART / I^{2}C] N.C.
#PITCH_DOWN	44	Hi-Z	I (Pull-up)	[Standalone (S1V3F351)] Playback pitch down
			Hi-Z	[Standalone (S1V3F352)] N.C.
			Hi-Z	[SPI / UART / I^{2}C] N.C.
#VOLUME_UP	45	Hi-Z	I (Pull-up)	[Standalone] Volume up
			Hi-Z	[SPI / UART / I^{2}C] N.C.
#VOLUME_DOWN	46	Hi-Z	I (Pull-up)	[Standalone] Volume down
			Hi-Z	[SPI / UART / I^{2}C] N.C.
#SOUND_REC	28	Hi-Z	I (Pull-up)	[Standalone] Recording (Recorded at Low level)
			Hi-Z	[SPI / UART / I^{2}C] N.C.
#REC_SOUND_PLAY	29	Hi-Z	I (Pull-up)	[Standalone] Recorded sound playback
			Hi-Z	[SPI / UART / I^{2}C] N.C.
#QSPISS	10	Hi-Z	O *1	Quad synchronous serial interface slave-select output
			Hi-Z	No external QSPI flash memory connected
QSPICLK	5	Hi-Z	O *1	Quad synchronous serial interface clock output
			Hi-Z	No external QSPI flash memory connected
QSDIO0	6	Hi-Z	Hi-Z *1	Quad synchronous serial interface data input/output
			Hi-Z	No external QSPI flash memory connected
QSDIO1	7	Hi-Z	Hi-Z *1	Quad synchronous serial interface data input/output
			Hi-Z	No external QSPI flash memory connected
QSDIO2	8	Hi-Z	Hi-Z *1	Quad synchronous serial interface data input/output
			Hi-Z	No external QSPI flash memory connected
QSDIO3	9	Hi-Z	Hi-Z *1	Quad synchronous serial interface data input/output
			Hi-Z	No external QSPI flash memory connected
SPEAKER_OUT_N	32	O	O	[Speaker output] Speaker negative output
			Hi-Z	[2-pin buzzer output] N.C.
			Hi-Z	[4-pin buzzer output] N.C.
SPEAKER_OUT_P	31	O	O	[Speaker output] Speaker positive output
			Hi-Z	[2-pin buzzer output] N.C.
			Hi-Z	[4-pin buzzer output] N.C.
BUZZER_OUT_N2	16	Hi-Z	Hi-Z	[Speaker output] N.C.
			Hi-Z	[2-pin buzzer output] N.C.
			O	[4-pin buzzer output] Buzzer negative output 2 (S1V3F351 only)
BUZZER_OUT_N	15	Hi-Z	Hi-Z	[Speaker output] N.C.
			O	[2-pin buzzer output] Buzzer negative output 1
			O	[4-pin buzzer output] Buzzer negative output 1
BUZZER_OUT_P	14	Hi-Z	Hi-Z	[Speaker output] N.C.
			O	[2-pin buzzer output] Buzzer positive output 1
			O	[4-pin buzzer output] Buzzer positive output 1
BUZZER_OUT_P2	13	Hi-Z	Hi-Z	[Speaker output] N.C.
			Hi-Z	[2-pin buzzer output] N.C.
			O	[4-pin buzzer output] Buzzer positive output 2 (S1V3F351 only)
EXT_CIRCUIT_CTRL	30	Hi-Z	Hi-Z / O	External speaker / buzzer amplifier control output In Host Interface mode, this pin is switched to output mode from a Hi-Z state when the ISC_SOUND_OUTPUT_CONFIG_REQ message is received. In Standalone mode, this pin is switched to output mode from a Hi-Z state according to the parameter information.
STATUS	12	Hi-Z	O	Status output H: During sound playing, sound recording, tone outputting, flash memory operating, memory checking, self-checking, or initializing L: Other than above
V_{REF}	22	Hi-Z	Hi-Z	[No recording] N.C.
			A	[Recording] Reference voltage for sound input
ADIN	21	Hi-Z	Hi-Z	[No recording] N.C.
			A	[Recording] Sound input
OSCEN	47	Hi-Z	I	Oscillator selection H: Crystal / ceramic oscillator (OSCI / OSCO) Connect a resonator to OSCI / OSCO. L: Embedded oscillator

Pin name	Pin No.	I/O		Function
		During reset	Initial status	
OSCI	34	Hi-Z	Hi-Z / A	Oscillator input (Leave open when the embedded oscillator is used.) Enabled when OSCEN = H; Hi-Z when OSCEN = L
OSCO	33	Hi-Z	Hi-Z / A	Oscillator output (Leave open when the embedded oscillator is used.) Enabled when OSCEN = H; Hi-Z when OSCEN = L
#SLEEP_CTRL	3	Hi-Z	I (Pull-up)	[Standalone] Sleep control H: During Normal Operating mode H → L → H: Set to Sleep mode
			Hi-Z	[SPI / UART / I^2C] N.C.

*1: After reset state is canceled, this IC checks if an external flash memory is connected. The pin goes into Hi-Z state if no flash memory is connected.

2. Power Supply

2.1 Overview

This IC operates by supplying a voltage within the specified range to the V_{DD} pin with the V_{SS} pin set as a GND level. When using an external flash memory, its operating voltage must be supplied to the V_{DDQSPI} pin. When an external flash memory is not connected, the V_{DDQSPI} pin should be connected to V_{DD}.

This IC is equipped with a power supply system to operate the internal circuits in stable and low power conditions.
The V_{D1} regulator generates the V_{D1} voltage for driving the internal circuits, this makes it possible to keep current consumption constant independent of the V_{DD} voltage level.
The voltage booster generates the embedded flash memory programming voltage.

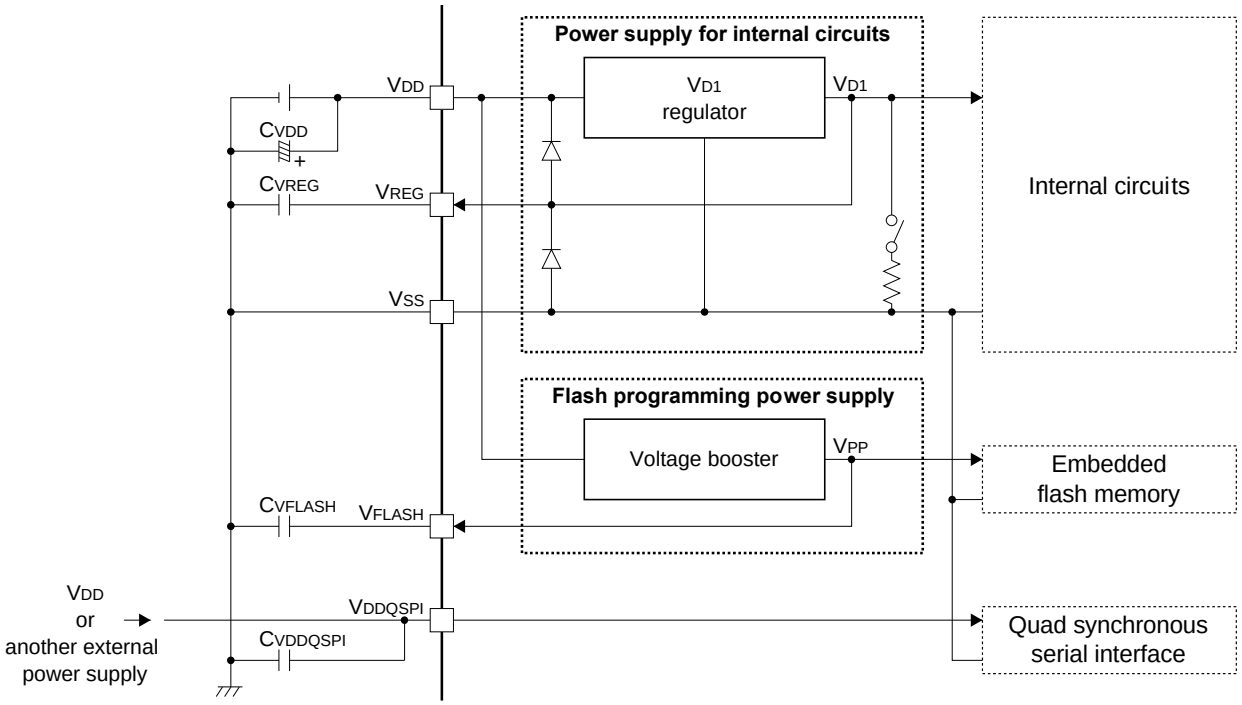


Figure 2.1 Power System Configuration

2.2 Power Supply Pins

Table 2.1 lists the power supply pins.

Table 2.1 List of Power Supply Pins

Pin No.	Pin name	I/O	Function
38	V_{DD}	P	Power supply (+)
36	V_{SS}	P	GND
11	V_{DDQSPI}	P	QSPI flash memory interface power supply
4	V_{FLASH}	A	Flash programming voltage regulator output
35	V_{REG}	A	Internal operating voltage (V_{D1}) regulator output

For the V_{DD} / V_{DDQSPI} operating voltage ranges and recommended external parts, refer to "*10.2 Recommended Operating Conditions*."

If an external QSPI flash memory is not used, the V_{DDQSPI} pin should be connected to V_{DD}.

3. Reset

3.1 Overview

This IC has a power-on reset function that initializes the internal circuits after turning power On, and the #RESET pin to reset this IC from outside.

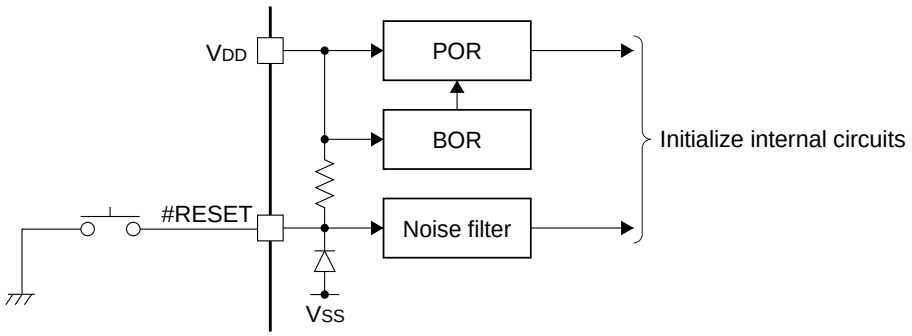


Figure 3.1 Reset System Configuration

3.2 Reset Pin

Table 3.1 shows the reset input pin.

Table 3.1 Reset Input Pin

Pin No.	Pin name	I/O	Function
37	#RESET	I (Pull-up)	Reset input

The #RESET pin is connected to the noise filter that removes pulses not conforming to the requirements. An internal pull-up resistor is connected to the #RESET pin, so the pin can be left open. For the #RESET pin characteristics, refer to "*10.5 Reset Characteristics*."

3.3 Reset Sources

The following shows the reset sources that initializes this IC:

3.3.1 Hardware Reset

#RESET Pin

Inputting a Low-level pulse longer than the specified width to the #RESET pin resets this IC.

POR and BOR

POR (Power-On Reset) detects the rise of V_{DD} after power is turned On to place this IC into Reset state until V_{DD} reaches the specified voltage level. BOR (Brown-Out Reset) detects the V_{DD} voltage level and places this IC into Reset state if the V_{DD} voltage drops below the specified level. These functions ensure that the system will be reset properly when the power is turned On and the supply voltage is out of the operating voltage range. Figure 3.2 shows an example of the POR and BOR internal reset operation according to variations in V_{DD}.

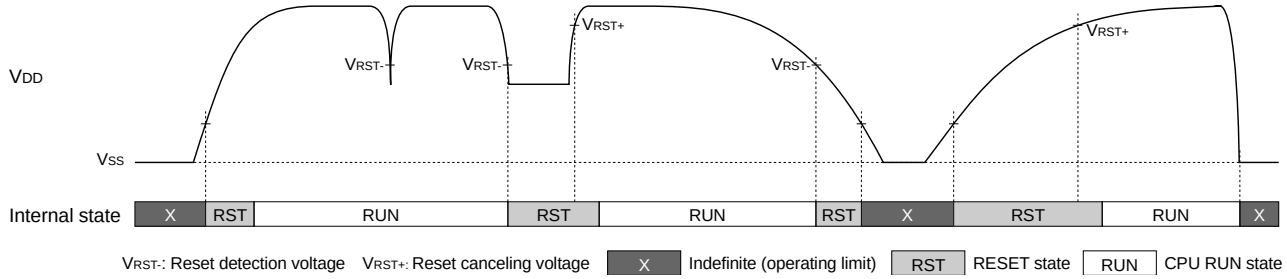


Figure 3.2 Example of Internal Reset by POR and BOR

For the POR and BOR electrical specifications, refer to "*10.5 Reset Characteristics*."

A hardware reset initializes all the sound processing configurations and internal circuits.

3.3.2 Issuing Reset Command from Host

In Host Interface mode (described later), the host can initialize a part of or all functions of this IC by sending a reset command. The reset command is used by selecting either Non-fatal error clear or Forced reset.

When the reset command is executed with the Non-fatal error clear selected, it clears the Non-fatal error of ERROR0 or ERROR1 that has occurred.

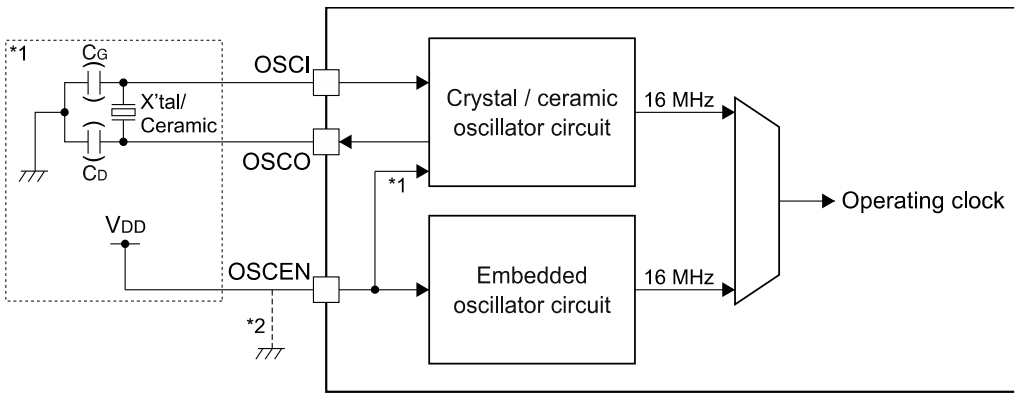
When the reset command is executed with Forced reset selected, this IC restarts the same as the hardware reset, therefore, all the sound processing configurations and internal circuits are initialized.

4. Oscillator Circuit and Standby Mode

4.1 Overview

This IC has an embedded oscillator (16 MHz, Typ.) to generate the clocks necessary for sound playback, communication with the host and external flash memory, and other internal operations.

Also this IC has a standby function that stops clocks to reduce power consumption.



*1: When crystal / ceramic oscillation is selected (OSCEN = H)
*2: When internal oscillation is selected (OSCEN = L)

Figure 4.1 Oscillator Circuit and Clock Controller

4.2 List of Input / Output Pins

Table 4.1 lists the oscillator circuit pins.

Table 4.1 List of Oscillator Pins

Pin No.	Pin name	I/O	Initial status	Function
47	OSCEN	I	I	Oscillator selection H: Crystal / ceramic oscillator (Connect a resonator to OSCI / OSCO.) L: Embedded oscillator
34	OSCI	A	Hi-Z	Oscillator input (Leave open when the internal oscillator is used.)
33	OSCO	A	Hi-Z	Oscillator output (Leave open when the internal oscillator is used.)

4.3 Selecting Oscillator Circuit

This IC is equipped with a crystal / ceramic oscillator circuit that generates a high-precision clock and an embedded oscillator circuit that does not need any external parts.

When using the crystal / ceramic oscillator circuit, connect the OSCEN pin to V_{DD} and connect a 16 MHz crystal or ceramic resonator between the OSCI and OSCO pins (see Figure 4.1). For the recommended external component values, refer to "*10.2 Recommended Operating Conditions*."

When using the embedded oscillator circuit, connect the OSCEN pin to V_{SS}.The OSCI and OSCO pins should be left open.

4.4 Standby Mode (Sleep / Deep Sleep)

This IC provides two standby modes for low power operation, Sleep mode and Deep Sleep mode.

4.4.1 Sleep Mode

Sleep mode stops all clock supplies to the sound play and other functions to reduce power consumption. The system clock continues operating as is, this makes it possible to return to Normal mode quickly when Sleep mode is cancelled.

Sleep mode is supported only in Host Interface mode, and it can be entered or returned by a command sent from the host.

Standalone mode cannot enter Sleep mode.

4.4.2 Deep Sleep Mode

Deep Sleep mode stops all clocks including the system clock to reduce power consumption, therefore, it has the effect of reducing power consumption superior to Sleep mode.

In Host Interface mode, Deep Sleep mode can be entered or returned by a command sent from the host.

In Standalone mode, it can be entered by controlling the #SLEEP_CTRL pin or counting with an internal timer and returned by any control pin input.

5. Memory

5.1 Overview

This IC has a re-writable embedded flash memory for storing Sound ROM data.
Also external flash memory can be added as necessary. It is used to store recording sound data as well as storing sound data for playback.

This IC is equipped with a programming power supply for the embedded flash memory, this makes it possible to write sound data to the embedded flash memory by sending a message from the host.
It is possible to write sound data to the external flash memory as well.

5.2 Embedded Flash Memory

The S1V3F351 includes a 64K-byte flash memory; the S1V3F352 includes a 160K-byte flash memory.

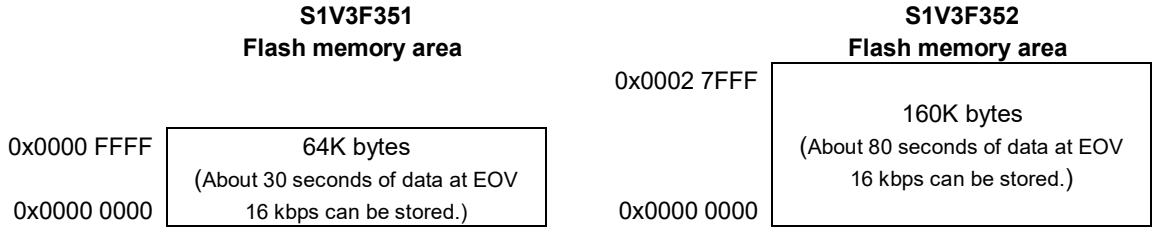


Figure 5.1 Embedded Flash Memory

5.3 External QSPI Flash Memory

This IC is equipped with a quad synchronous serial interface. Therefore, it allows accessing of large-capacity sound data by connecting an external QSPI flash memory.

It is necessary to use a QSPI flash memory with XIP (eXecute-In-Place) mode as the external flash memory.

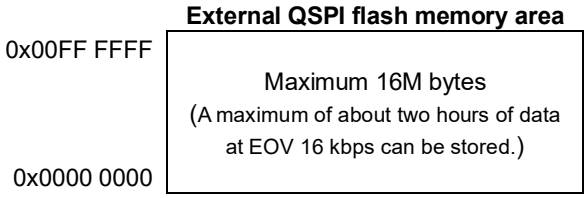


Figure 5.2 External QSPI Flash Memory

5.3.1 Quad Synchronous Serial Interface Pins

List of Input/Output Pins

Table 5.1 lists the quad synchronous serial interface pins.

Table 5.1 List of Quad Synchronous Serial Interface Pins

Pin No.	Pin name	I/O	Function
10	#QSPISS	O	Quad synchronous serial interface slave-select signal output
5	QSPICLK	O	Quad synchronous serial interface clock output
6	QSDIO0	Hi-Z	Quad synchronous serial interface data input / output
7	QSDIO1	Hi-Z	
8	QSDIO2	Hi-Z	
9	QSDIO3	Hi-Z	

When an external QSPI flash memory is not used, these pins should be all left open.

External Connections

This IC operates as a QSPI master device, and it can control one external QSPI slave device. Figure 5.3 shows an example of a connection with an external QSPI flash memory.

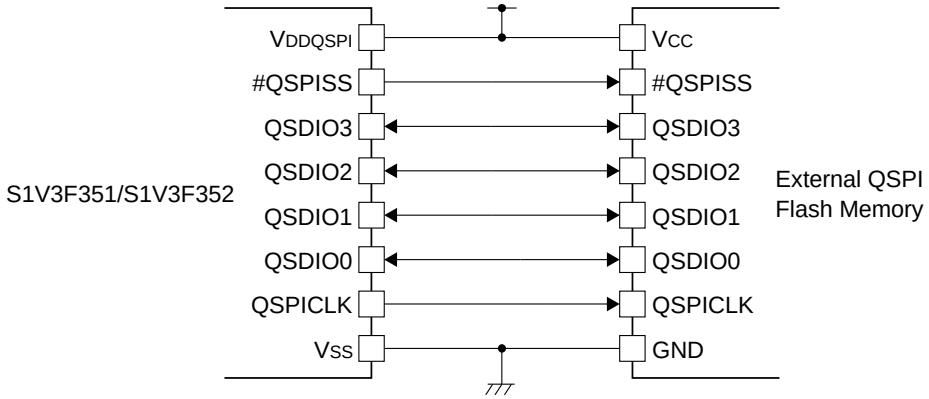


Figure 5.3 Connection with External QSPI Flash Memory

5.4 Switching Between Embedded and External Flash Memories

In Host Interface mode, both the embedded and external flash memories can store sound data for playback, and they are switchable by sending a command from the host.

In Standalone mode, if an external flash memory that contains Sound ROM data is connected, it is used as the Sound ROM. The embedded flash memory is used only when an external flash memory is not connected or when the external flash memory connected has no Sound ROM data. Standalone mode does not enable switching between the embedded and external flash memories for sound playback.

The external flash memory is also used to store recording sound data when this IC is used for recording. The embedded flash memory cannot store recording sound data.

6. Control Mode

This IC provides two control modes, Host Interface mode and Standalone mode.

6.1.1 Host Interface Mode

In Host Interface mode, the host controls the functions of this IC, such as sound play, by sending commands (messages) to this IC via the SPI, I^2C, or UART interface.

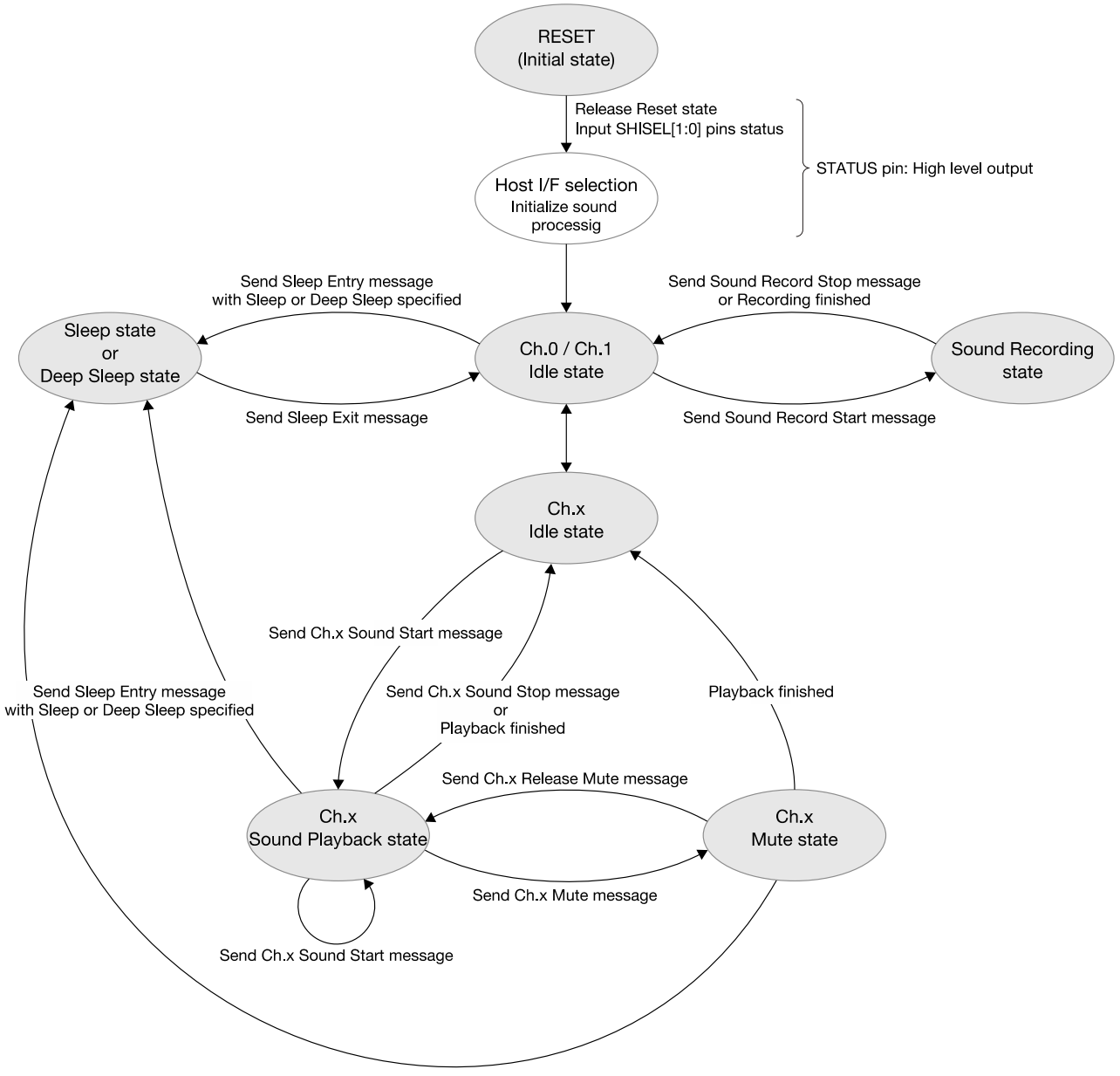


Figure 6.1 Internal Operating State Transition Diagram in Host Interface Mode

6.1.2 Standalone Mode

In Standalone mode, this IC operates independently without a host. The functions of this IC, such as sound play, are controlled by manipulating the key, buttons, or other components connected to the control input pins. Configuration values required for each function are saved in the dedicated 256-byte area in this IC.

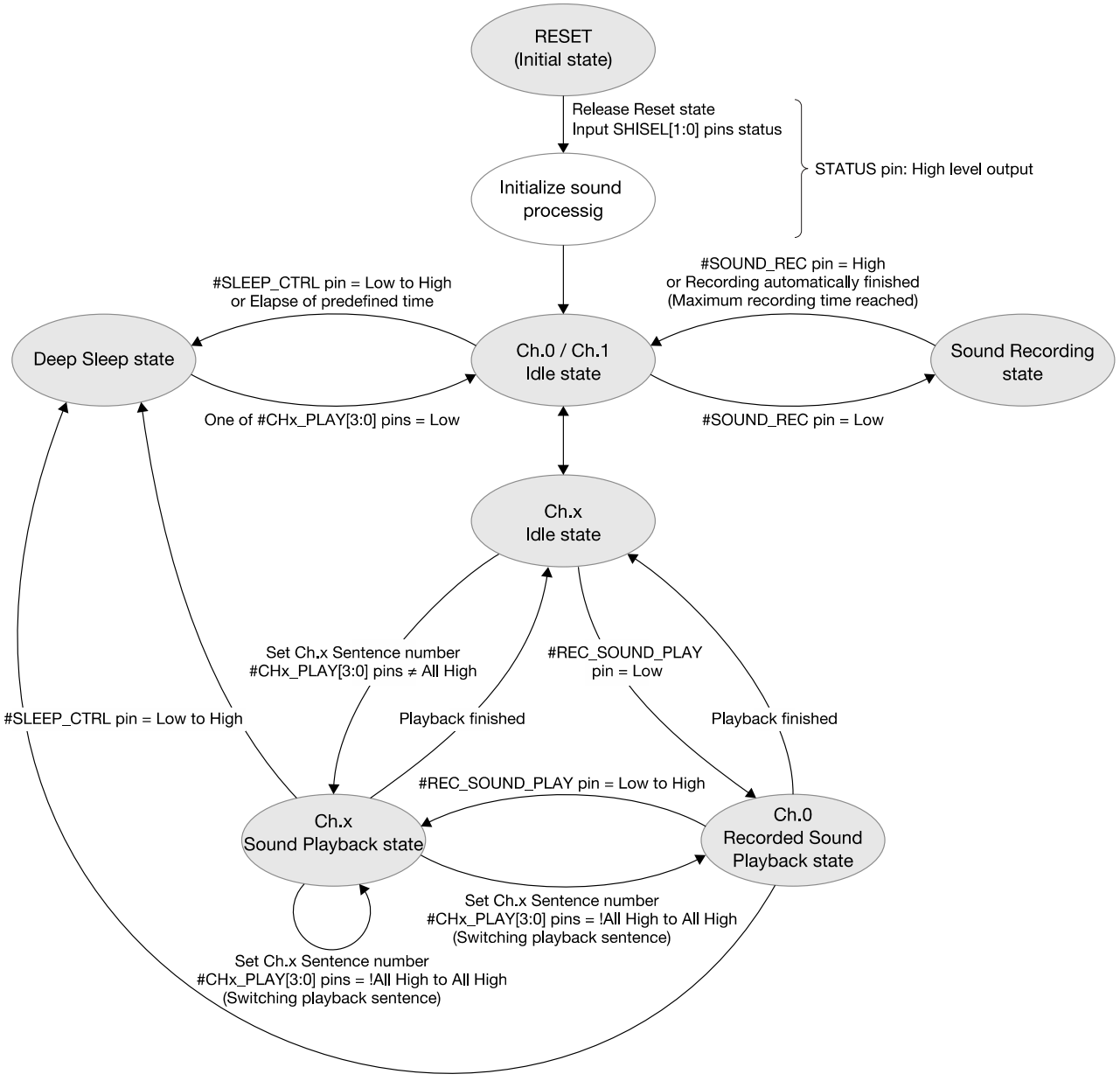


Figure 6.2 Internal Operating State Transition Diagram in Standalone Mode

6.2 Control Mode Pins and Mode Switching

Table 6.1 and Table 6.2 show the control mode pins to select a control mode and the host interface selections.

Table 6.1 Control Mode Select Pins

Pin No.	Pin name	I/O	Function
1	SHISEL0	I	Control mode / serial interface selection
2	SHISEL1	I	

Table 6.2 Control Mode / Serial Interface Selection

SHISEL1	SHISEL0	Control mode	Host interface
L	L	Host Interface mode	SPI interface
L	H		UART interface
H	L		I^2C interface
H	H	Standalone mode	–

When controlling this IC from the host, select Host Interface mode and the serial interface type to be used using these pins.
When operating this IC independently without connecting to a host, place this IC into Standalone mode.

In Host Interface mode, Pins 17 to 20 are configured as the input / output pins for the selected serial interface and the following pins for Standalone mode go into Hi-Z state.

Pin No. 3, 23, 24, 26, 27 to 29, 41 to 46

6.3 Input / Output Pins for Each Mode

6.3.1 SPI Interface Pins

List of Input / Output Pins

When SPI is selected as the host interface using the SHISEL[1:0] pins, Pins 17 to 20 are configured as the SPI pins as listed in Table 6.3.

Table 6.3 List of SPI Pins

Pin No.	Pin name	I/O	Function
17	#NSCSS	I	Slave-select input
18	SOS	O	Serial data output
19	SCKS	I	Serial clock input
20	SIS	I	Serial data input

External Connections

Figure 6.3 shows a connection diagram between this IC and the host.

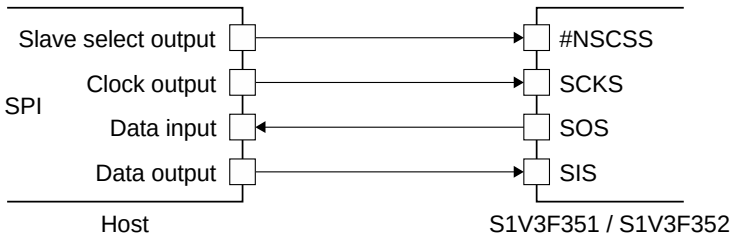


Figure 6.3 SPI Connection Diagram

6.3.2 I²C Interface Pins

List of Input / Output Pins

When I²C is selected as the host interface using the SHISEL[1:0] pins, Pins 19 and 20 are configured as the I²C pins as listed in Table 6.4.

Table 6.4 List of I²C Pins

Pin No.	Pin name	I/O	Function
17	N.C.	Hi-Z	N.C.
18	N.C.	Hi-Z	N.C.
19	SCL	I/O	Serial clock input
20	SDA	I/O	Serial data input / output

External Connections

Figure 6.4 shows a connection diagram between this IC and the host.

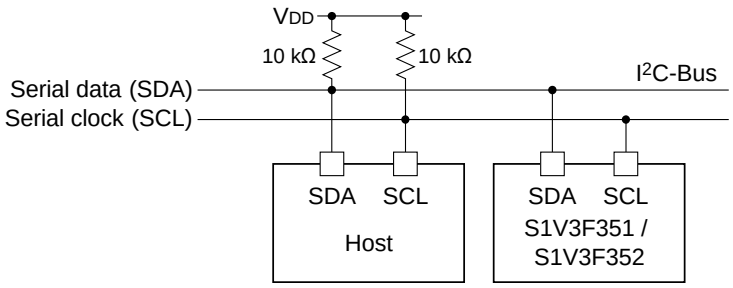


Figure 6.4 I²C Connection Diagram

6.3.3 UART Interface Pins

List of Input / Output Pins

When UART is selected as the host interface using the SHISEL[1:0] pins, Pins 18 and 20 are configured as the UART pins as listed in Table 6.5.

Table 6.5 List of UART Pins

Pin No.	Pin name	I/O	Function
17	N.C.	Hi-Z	N.C.
18	TXD	O	Serial data output
19	N.C.	Hi-Z	N.C.
20	RXD	I	Serial data input

External Connections

Figure 6.5 shows a connection diagram between this IC and the host.

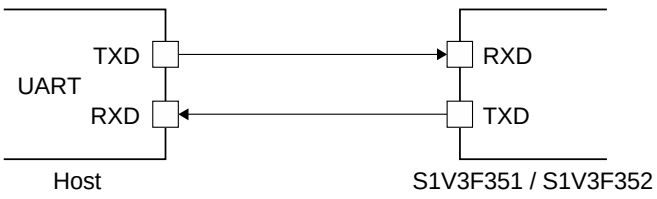


Figure 6.5 UART Connection Diagram

6.3.4 Standalone Mode Control Input Pins

When Standalone mode is selected using the SHISEL[1:0] pins, the pins listed in Table 6.6 are configured as the Standalone mode control input pins.

Table 6.6 List of Standalone Mode Control Input Pins

Pin No.	Pin name	I/O	Function
20	#CH0_PLAY3	I (Pull-up)	CH0_PLAY[3:0] Ch.0 sentence selection / sound playback start
19	#CH0_PLAY2	I (Pull-up)	
18	#CH0_PLAY1	I (Pull-up)	
17	#CH0_PLAY0	I (Pull-up)	
27	#CH1_PLAY3	I (Pull-up)	CH1_PLAY[3:0] Ch.1 sentence selection / sound playback start
26	#CH1_PLAY2	I (Pull-up)	
24	#CH1_PLAY1	I (Pull-up)	
23	#CH1_PLAY0	I (Pull-up)	
41	#SPEED_UP	I (Pull-up)	Playback speed up
42	#SPEED_DOWN	I (Pull-up)	Playback speed down
43	#PITCH_UP	I (Pull-up)	Playback pitch up (Available only in S1V3F351. N.C. in S1V3F352)
44	#PITCH_DOWN	I (Pull-up)	Playback pitch down (Available only in S1V3F351. N.C. in S1V3F352)
45	#VOLUME_UP	I (Pull-up)	Volume up
46	#VOLUME_DOWN	I (Pull-up)	Volume down
28	#SOUND_REC	I (Pull-up)	Recording
29	#REC_SOUND_PLAY	I (Pull-up)	Recorded sound playback
3	#SLEEP_CTRL	I (Pull-up)	Sleep control H: During Normal Operating mode H → L → H: Set to Sleep mode

7. Functions

This IC provides a sound play function, a sound recording function, and other functions. These functions are controlled by messages sent from the host in Host Interface mode, or inputs to the control input pins in Standalone mode. This chapter outlines the main functions.

For how to control them, refer to the relevant section in "*8 Host Interface Mode*" and "*9 Standalone Mode*."

7.1 Sound Play Function

7.1.1 Overview

This IC converts the sound data stored in the flash memory into PWM signals and outputs them to an external audio amplifier or an external differential circuit. The main features are listed below.

- Reproduces sound data in EPSON high quality and high compression algorithm format (EOV: EPSON Original Sound Format).
  - Sampling Frequency: 7.813 kHz / 15.625 kHz
  - Bitrate: 16 / 24 kbps (S1V3F351), 16 / 24 / 32 / 40 kbps (S1V3F352)
- Reproduces sound data in PCM format (recorded by the sound recording function of this IC).
  - Sampling Frequency: 15.625 kHz
- Single channel playback and 2-channel mixing playback (e.g., Ch.0 = Voice and Ch.1 = BGM are mixed and played)
  - * Sound and tone cannot be output simultaneously. If an attempt is made to start a sound playback while a tone is being output, the sound playback starts after terminating the tone output.
- Volume adjustment *1
  - Volume is adjustable within the range of 0 dB to -63 dB (in 0.5 dB steps).
- Mute *2
  - Sound output can be silenced during playback.
- Playback speed conversion (Ch.0 only) *1
  - When using only the playback speed conversion
    Playback speed is configurable from 75% (slow) to 125% (fast) in 5% steps based on the standard speed of 100%.
  - When using with the playback pitch conversion
    Playback speed is configurable from 85% (slow) to 115% (fast) in 5% steps based on the standard speed of 100%.
- Playback pitch conversion (S1V3F351 CH.0 only) *1
  - When using only the playback pitch conversion
    Playback pitch is configurable from 75% (low) to 125% (high) in 5% steps based on the standard pitch of 100%.
  - When using with the playback speed conversion
    Playback pitch is configurable from 90% (low) to 110% (high) in 5% steps based on the standard pitch of 100%.
- Smoothing process to suppress generation of noise at suspending and resuming playback output (refer to *Section 7.1.3*) *2
- Programmable delay time between phrases
  - Ch.0: 0 (gapless) to 2000 ms (25 ms steps)
  - Ch.1: 25 ms to 2000 ms (25 ms steps)

*1 Standalone mode restricts a part of the function.
*2 Supported only in Host Interface mode

7.1.2 Sound Output Pins

This IC outputs the sound signals for driving a speaker or buzzer by D/A converting sound data. The speaker output pins and the buzzer output pins are provided separately, and either one can be selected as the sound output target. The buzzer output is configurable to 2-pin output or 4-pin output*.

* The 4-pin output configuration is available only in the S1V3F351.

List of Output Pins

Table 7.1 lists the speaker / buzzer output pins.

Table 7.1 List of Speaker / Buzzer Output Pins

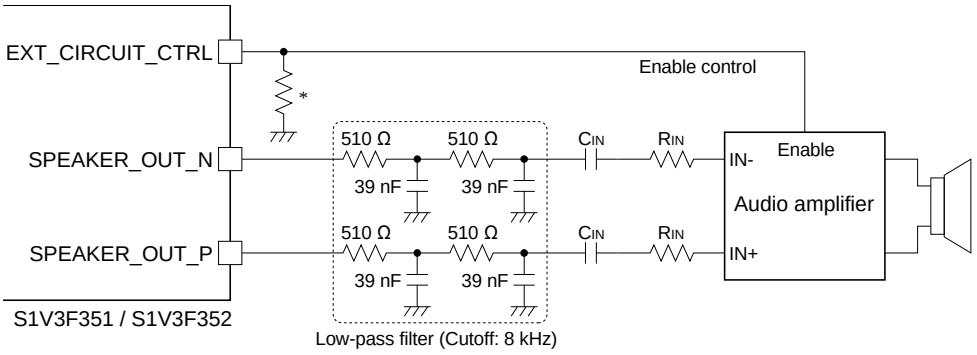
Pin No.	Pin name	I/O	Function
32	SPEAKER_OUT_N	O	Speaker negative output
31	SPEAKER_OUT_P	O	Speaker positive output
16	BUZZER_OUT_N2	Hi-Z	Buzzer negative output 2 (Available only in S1V3F351. N.C. in S1V3F352)
15	BUZZER_OUT_N	Hi-Z	Buzzer negative output 1
14	BUZZER_OUT_P	Hi-Z	Buzzer positive output 1
13	BUZZER_OUT_P2	Hi-Z	Buzzer positive output 2 (Available only in S1V3F351. N.C. in S1V3F352)
30	EXT_CIRCUIT_CTRL	O	External speaker / buzzer amplifier control output

Connection with Speaker

Use the SPEAKER_OUT_P and SPEAKER_ OUT_N outputs to drive a speaker in Differential mode (recommended); use the SPEAKER_OUT_P pin output to drive a speaker in Single mode. A low-pass filter (cutoff 8 kHz) and an audio amplifier are required as the external components besides a speaker. When turning the external audio amplifier On and Off from this IC, use the EXT_CIRCUIT_CTRL output. In Host Interface mode, the EXT_CIRCUIT_CTRL output can be controlled by sending a message from the host. In Standalone mode, the EXT_CIRCUIT_CTRL output timings should be configured as parameter information.

Figure 7.1 and Figure 7.2 show external circuit examples to input the speaker output signals of this IC to an external audio amplifier. The circuit configuration and component values should be modified according to the specifications of the audio amplifier to be used.

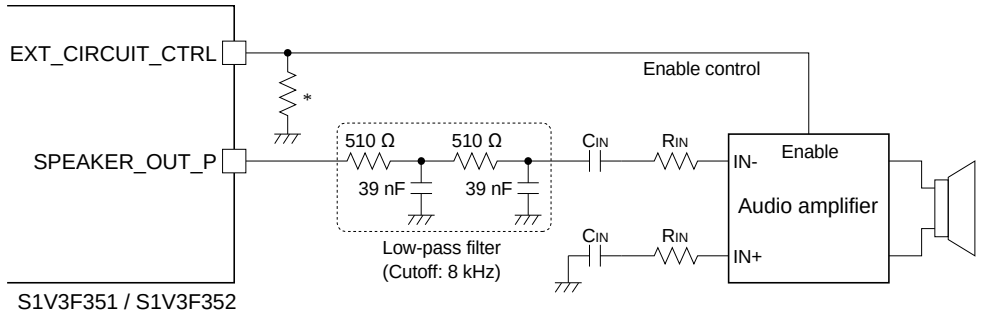
Differential Mode (Selected output destination: 0x00)



* Use a pull-down resistor if the audio amplifier enters sleep state by a Low level input to the enable pin. (Confirm the specification as it depends on the amplifier.)

Figure 7.1 Speaker Connection Example in Differential Mode

Single Mode (Selected output destination: 0x00)



* Use a pull-down resistor if the audio amplifier enters sleep state by a Low level input to the enable pin. (Confirm the specification as it depends on the amplifier.)

Figure 7.2 Speaker Connection Example in Single Mode

Connection with Buzzer

Use the BUZZER_OUT_P and BUZZER_OUT_N pin outputs to drive a 2-pin buzzer. The S1V3F351 supports 4-pin drive as well. In this case, use the BUZZER_OUT_P, BUZZER_OUT_P2, BUZZER_OUT_N, and BUZZER_OUT_N2 pin outputs. An external differential circuit is required as the external component besides an electromagnetic buzzer or a piezoelectric buzzer. When turning the external power supply for the differential circuit On and Off from this IC, use the EXT_CIRCUIT_CTRL output. In Host Interface mode, the EXT_CIRCUIT_CTRL output can be controlled by sending a message from the host. In Standalone mode, the EXT_CIRCUIT_CTRL output timings should be configured as parameter information.

Figure 7.3 and Figure 7.4 show examples of connections between the buzzer output signals of this IC and an external differential circuit composed of discrete parts. For more information on the differential circuit configuration, refer to the "Sound Input/Output Application Note."

2-pin Output Mode (Selected output destination: 0x01, 0x03, 0x05, 0x07 in S1C3F351 / 0x01, 0x07 in S1V3F352)

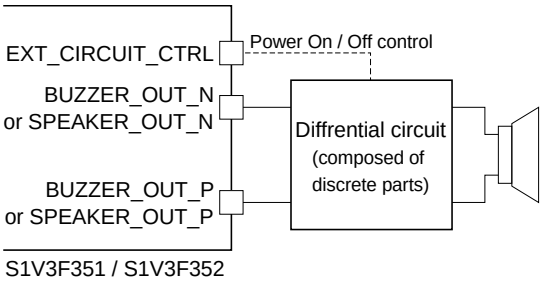


Figure 7.3 Connection Example with External Discrete Differential Circuit (2-pin Output Mode)

4-pin Output Mode (Selected output destination: 0x02, 0x04, 0x06 in S1V3F351)

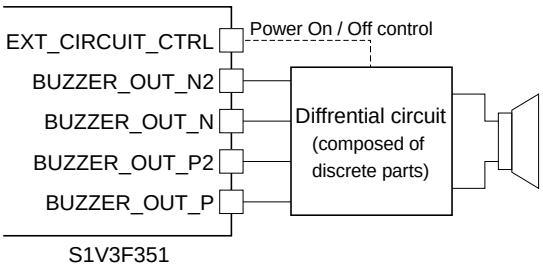


Figure 7.4 Connection Example with External Discrete Differential Circuit (4-pin Output Mode)

7.1.3 Sound Output Smoothing Process

The Host Interface mode provides the Sound Stop and Mute commands to control sound output during playback. There are two Sound Stop commands provided, the Sound Stop Immediately command that stops sound output immediately and the Sound Stop after Current Phrase command that stops sound output after the phrase being currently played ends. Likewise, two Mute commands are provided, the Mute Immediately command that mutes sound output immediately and the Mute after Current Phrase command that mutes sound output after the phrase being currently played ends. Figure 7.5 shows examples of sound output stop positions by these commands.

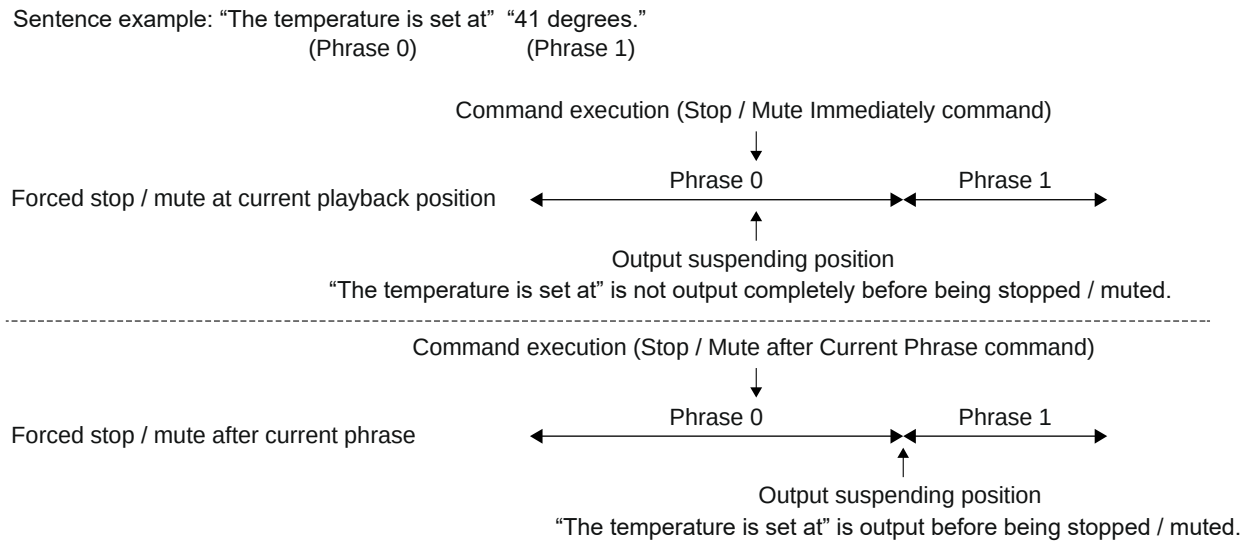


Figure 7.5 Sound Output Stop Position

When the Sound Stop Immediately command, Mute Immediately command, or Release Mute command is executed while a sound is being output, the sound output level may change rapidly. To suppress noise that may occur at this time, this IC performs a smoothing process to the rise and fall of the sound output signal.

When a sound output is suspended immediately by the Sound Stop Immediately or Mute Immediately command, the output is faded out by the smoothing process.

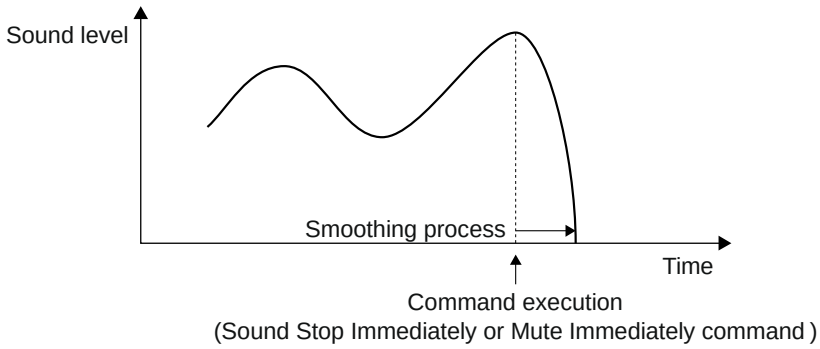


Figure 7.6 Smoothing Process when Sound Output is Suspended

When a muted state is released by the Release Mute command, the output is faded in by the smoothing process.

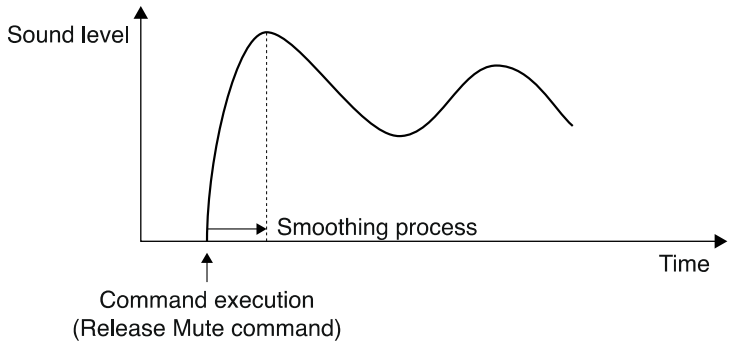


Figure 7.7 Smoothing Process when Muted State is Released

7.2 Sound Recording Function

7.2.1 Overview

This IC is equipped with a sound recording function that records the sound input from the external microphone using the internal 12-bit AD converter and stores the recorded data to the external flash memory.

The recording sound format is as follows:

- PCM (uncompressed format)
- Sampling frequency: 15.625 kHz
- Quantization bit number: 16 bits
- Maximum recording data size: 16M bytes (64K-byte steps)

7.2.2 Sound Recording Requirements

When using the sound recording function, a microphone, a gain amplifier, and an external flash memory must be connected to this IC.

7.2.3 Sound Input Pins

List of Input Pins

Table 7.2 lists the pins used for sound input.

Table 7.2 List of Pins Used for Sound Input

Pin No.	Pin name	I/O	Function
22	V_{REF}	Hi-Z	Reference voltage for sound input
21	ADIN	Hi-Z	Sound input

Connection with External Microphone

Figure 7.8 shows an external microphone connection example.

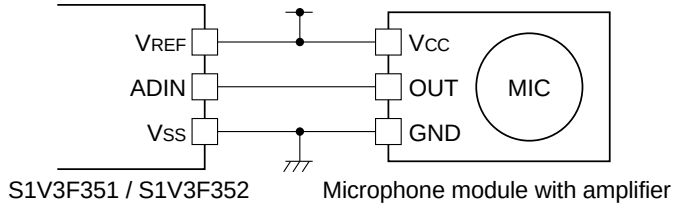


Figure 7.8 External Microphone Connection Example

7.3 Tone Output

The tone output function outputs square wave(s) with a frequency specified as a tone signal. A patterned tone generated with up to four frequencies can be output as well as a single frequency tone output.

* Tone and sound cannot be output simultaneously. If an attempt is made to start a tone output while a sound is being played, the tone output starts after terminating the sound playback.

7.3.1 Single Tone Output

This function generates a tone signal with a single frequency (31 Hz to 16 kHz) and outputs the generated tone.

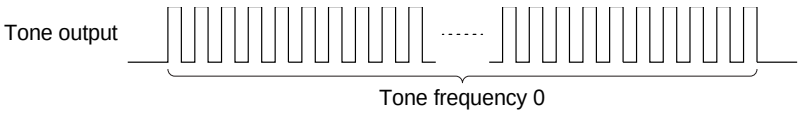


Figure 7.9 Single Tone Output

7.3.2 Patterned Tone Output

A patterned tone can be generated and output by specifying up to four frequencies within the range from 31 Hz to 16 kHz and their output durations.

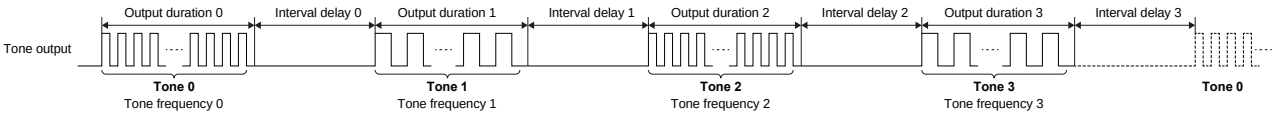


Figure 7.10 Patterned Tone Output

7.4 Operating Status Monitor Output

7.4.1 Overview

This IC has an operating status output function that informs the operating status and the error occurrence status.

7.4.2 Operating Status Output Pins

Table 7.3 lists the operating status output pins.

Table 7.3 Operating Status Output Pins

Pin No.	Pin name	Initial status	Function
25	ERROR	O	Error output H: An error has occurred. L: Normal
12	STATUS	O	Status output H: During sound playing, sound recording, tone outputting, flash memory operating, memory checking, self-checking, or initializing L: Other than above

The ERROR pin informs to an external device that an error has occurred in this IC. The ERROR pin is set to Low in normal status and set to High when an error occurs.

The STATUS pin informs to an external device of the operating status of this IC. It is set to High in the cases shown below.

- While a sound is being played
- While a sound is being recorded
- While a tone is being output
- While data is being written to or read from the flash memory
- While the memory is being checked
- While the self-check is being executed
- While this IC is being initialized

7.5 Self-Check Function

This IC is equipped with a self-check function that checks for abnormalities in the internal circuits. The STATUS pin goes High while the self-check is being executed. The ERROR pin goes High when an abnormality has been detected in the self-check.
There are differences in the execution procedure and check items between the control modes.

Host Interface Mode

The self-check can be executed by sending the ISC_SELF_CHECK_REQ message from the host immediately after canceling a reset.
The following lists the self-check items in this control mode:

- Abnormality detection in the internal circuits
- Read / write check of the internal RAM area

Standalone Mode

The self-check can be executed by canceling a reset by holding the four pins, #CH1_PLAY0, #CH1_PLAY1, #CH1_PLAY2, and #CH1_PLAY3, at a Low level.
The following lists the self-check items in this control mode:

- Abnormality detection in the internal circuits
- Read / write check of the internal RAM area
- CRC check of the Sound ROM data stored in the embedded or external flash memory

  * The CRC value used in this check must be previously set as parameter information to be stored in the embedded flash memory.

8. Host Interface Mode

This chapter describes the operations and control procedure in Host Interface mode.

8.1 Message Protocol

This IC placed into Host Interface mode acts as a companion device, and is controlled by the host via the selected serial interface.

The host device can configure and control this IC using the ISC (Inter-System Communication) messages. The ISC message is used to transfer sound data as well.

There are two types of messages defined as shown below.

8.1.1 REQuest

REQuest (hereinafter referred as REQ message) is a type of message for the host to send commands to this IC. The REQ messages are used to configure and control this IC, and to transfer sound data. When a REQ message is received, this IC returns a receive status byte to notify whether the message has been successfully received or not to the host. The host cannot send the succeeding message until the receive status byte is received.

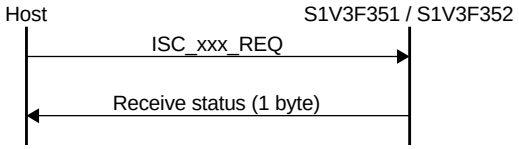


Figure 8.1 REQ Message Flow

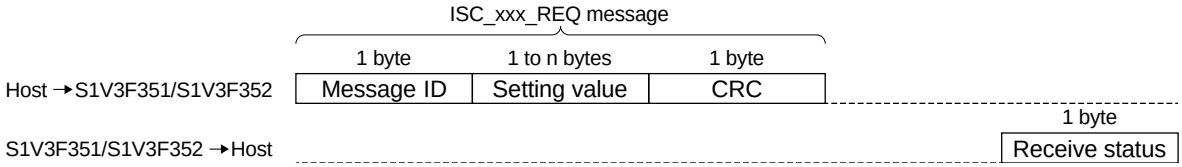


Figure 8.2 REQ Massage Configuration

Table 8.1 Receive Status Byte

Receive status byte	Receive status field	Description
0x0F	0b0000_1111	Reception success / Processing completed
0x10	0b***1_0000	Invalid message ID
0x20	0b**1*_0000	CRC error
0x40	0b*1**_0000	Buffer overflow
0x80	0b1***_0000	Other error

8.1.2 INDication

INDication (hereinafter referred as IND message) is a type of message for the host to request that this IC will return statuses and data. For example, the host can obtain the operating status of this IC (e.g., playback, sleep), the values set by the host, and error information (*1). When an IND message is received, this IC returns the requested information following a receive status byte (Table 8.1).

*1: When an error has occurred, the ERROR pin goes High. The host can recognize that an error has occurred by monitoring this signal.

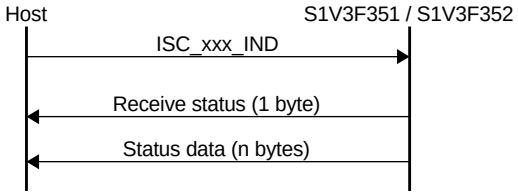


Figure 8.3 IND Message Flow

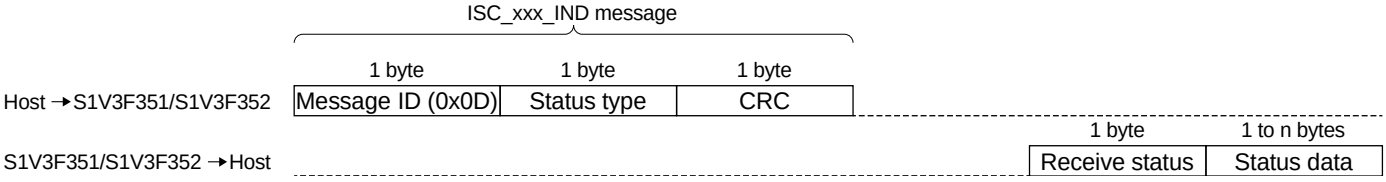


Figure 8.4 IND Massage Configuration

8.1.3 CRC

The host can add a one-byte CRC to messages. The CRC check by this IC can be enabled or disabled by sending the ISC_CRC_CONFIG_REQ message. When enabled, this IC calculates CRC beginning from the first message byte to the byte just before the CRC byte and compares it with the received CRC. If an error results from the check, this IC informs the host that a CRC error has occurred using the receive status byte. When the CRC check is disabled, this IC does not perform CRC check. The contents of the CRC byte field in messages are ignored (note, however, that the host must send a dummy byte as the CRC byte).

The following shows the CRC calculation condition used in the message protocol:

- Method: CRC-8 AUTOSAR
- Generator polynomial: 0x2F $x^8 + x^6 + x^5 + x^4 + x^2 + 1$
- Initial value: 0xFF

8.2 Transmitting / Receiving Messages

8.2.1 SPI Interface

This IC includes a clock synchronous serial interface (SPI) that has the features below and can be used to communicate with the host in Host Interface mode.

- Slave device (Clock must be supplied from the master device (host).)
- Data length: 8 bits/word
- Data format: MSB first
- Clock polarity: High at inactive state
- Clock phase: Data bit is sampled at the SCKS rising edge and shifted out at the falling edge while #NSCSS = Low.
- Communication method: Full-duplex communication
- Maximum SCKS frequency: 400 kHz at normal operation
  4 MHz at high-speed operation (high-speed clock period for flash memory read / write)

See Table 6.3 and Figure 6.3 for the SPI interface pin configuration and the connection with the host, respectively.

The SPI interface in this IC can be used even if the #NSCSS pin is fixed at Low.

SPI Transmission / Reception

Data Format

Figure 8.5 shows the clock and data input / output timing. The data length of this SPI interface is fixed at 8 bits and data are transferred with MSB first.

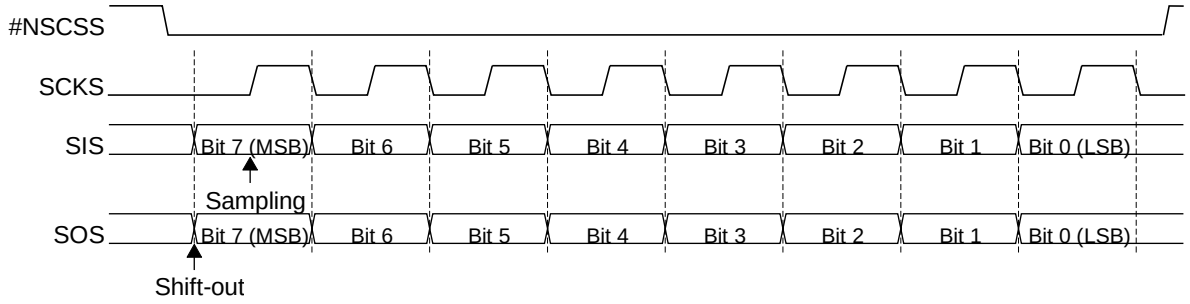


Figure 8.5 SPI Data Format

Data Transfer between Host and This IC

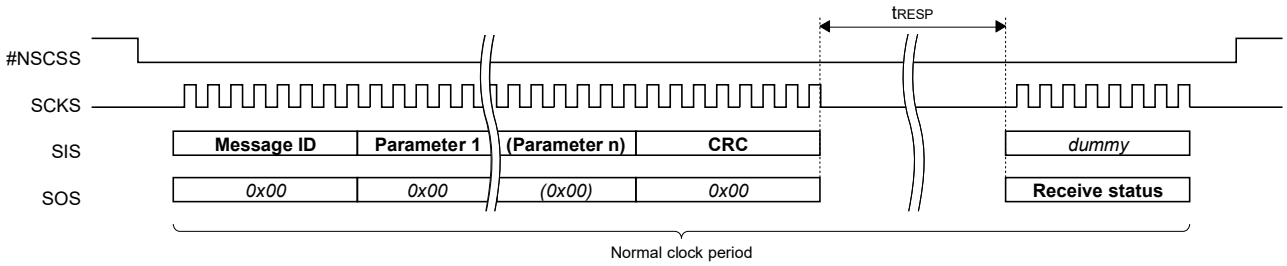
The SPI interface receives and transmits data simultaneously in sync with the clock output from the host.

1. The host (SPI master) changes the #NSCSS signal from High to Low and starts transmitting and receiving data with this IC.
2. The host outputs the clock to the SCKS pin of this IC.
3. The host outputs a transmit data bit to the SIS pin at the falling edge of the #NSCSS signal or the clock. At the same time, a data bit is output from the SOS pin of this IC.
4. The host and this IC fetch the data bit at the rising edge of the clock.
5. Steps 3 and 4 are repeated eight times until transfer for one byte is completed.
6. When the data transfer for the necessary number of bytes has been completed, the host sets the #NSCSS signal to High to terminate the data transmission / reception.

REQ Message Transmission / Reception

Ordinary REQ Message Transmission / Reception

Figure 8.6 shows a timing chart of an ordinary REQ message transmission / reception.



Use the normal-speed clock for the communication except when the flash memory data is transmitted / received.

Figure 8.6 REQ Message Transmission / Reception (SPI)

1. The host initiates a communication with this IC by setting the #NSCSS pin to Low.
   This IC starts a transmit / receive operation.
2. The host transmits a REQ message to this IC.
   This IC receives each REQ message byte and calculates CRC. When this IC receives the CRC byte in the message, it compares the calculated CRC with the received CRC (when the CRC check is enabled).

   During this message reception period, this IC outputs dummy bytes (0x00) as the transmit data.
3. The host transmits a dummy byte after the lapse of t_{RESP} (receive status response wait time) from the REQ message transmission, for this IC to send the receive status (REQ message reception completed).
   If the host outputs the dummy byte before the lapse of t_{RESP}, this IC returns a dummy byte (0x00) to the host until the receive status can be transmitted.
   Therefore, the host can determine that the received byte is the receive status when it is not 0x00.

   When this IC receives the REQ message successfully, it returns 0x0F to the host as the receive status. Otherwise, it indicates a reception failure (see Table 8.1).
4. The host sets the #NSCSS pin to High to terminate the communication.

Note: The host cannot transmit a subsequent message until the receive status from this IC is received. Furthermore, the host must take a wait time (refer to "*10.11 Command Receive Timing*") before a subsequent message can be transmitted, as this IC executes the received message command function after returning the receive status.

Transmission / Reception of REQ Message to Request Process Taking Time

Figure 8.7 and Figure 8.8 show transmission / reception timing charts when this IC executes the internal processing that requires a certain time (it sets the STATUS pin to High) after a REQ message has been received.

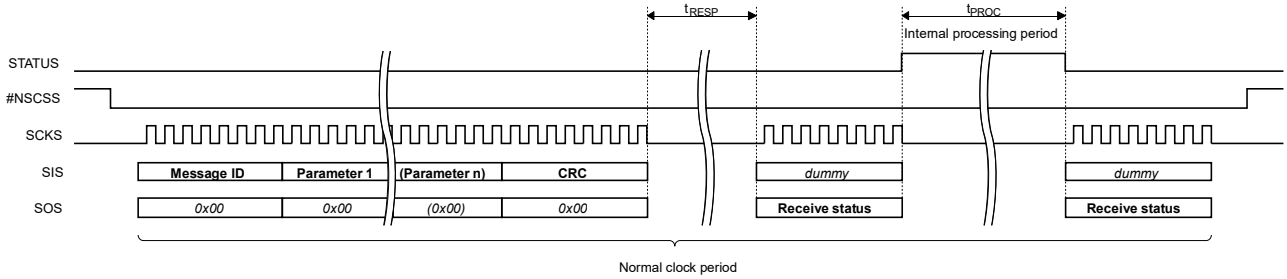


Figure 8.7 Transmission / Reception of REQ Message to Request Process Taking Time (SPI)

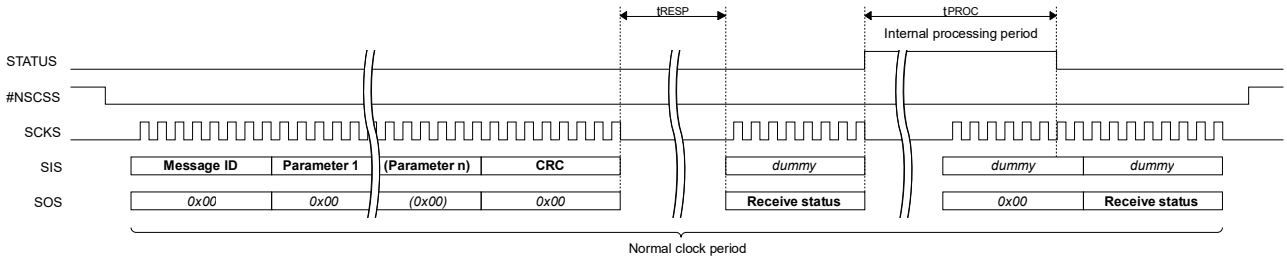


Figure 8.8 Transmission / Reception of REQ Message to Request Process Taking Time (SPI) (when the clock is input during internal processing)

The applicable REQ messages and the processes executed in the t_{PROC} period are listed in the table below.

Table 8.2 REQ Message to Request Process Taking Time

REQ message		Internal process in t_{PROC} period
ISC_FLASH_PROGRAM _REQ: Read Flash	(Flash Memory Data Read)	Read data from the flash memory
ISC_FLASH_PROGRAM_REQ: Chip Erase	(Flash Memory Chip Erase)	Erase entire flash memory
ISC_FLASH_PROGRAM_REQ: Sector Erase	(Flash Memory Sector Erase)	Erase a flash memory sector
ISC_FLASH_PROGRAM_REQ: CRC Check	(Flash Memory Check)	Check the memory in CRC
ISC_FLASH_PROGRAM_REQ: Erase Settings Area	(Embedded Flash Memory Setting Information Area Erase)	Erase setting information area
ISC_FLASH_PROGRAM_REQ: Read Settings Area	(Embedded Flash Memory Setting Information Read)	Read setting information
ISC_KEYCODE_CONFIG_REQ	(Keycode Configuration)	Write keycode
ISC_SELF_CHECK_REQ	(Self-check)	Execute self-check

1. The operations from the REQ message reception to the receive status (REQ message reception completed) transmission are the same as those for the ordinary REQ message transmission / reception mentioned above.
2. After the receive status has been received, the host stops the clock output and waits until the internal process of this IC is completed (t_{PROC} period). While this IC is executing the internal process, the STATUS pin outputs a High level. The host can determine that the process has completed by monitoring this signal.
3. After the fall of the STATUS signal is detected, the host outputs the clock and a dummy byte to fetch the receive status (process completion notice) being transmitted from this IC.

   If the host outputs the clock before the lapse of t_{PROC}, this IC returns a dummy byte (0x00) to the host until the receive status can be transmitted (Figure 8.8).
4. The host sets the #NSCSS pin to High to terminate the communication.

Transmission / Reception of REQ Message for Writing Data to Flash Memory

Figure 8.9 shows a transmission / reception timing chart for the REQ message (ISC_FLASH_PROGRAM _REQ: Write Flash, Write Settings Area) that requests a data writing to the flash memory. The host can switch the synchronous clock to a high-speed clock during write data transmission to perform high-speed data transfer.

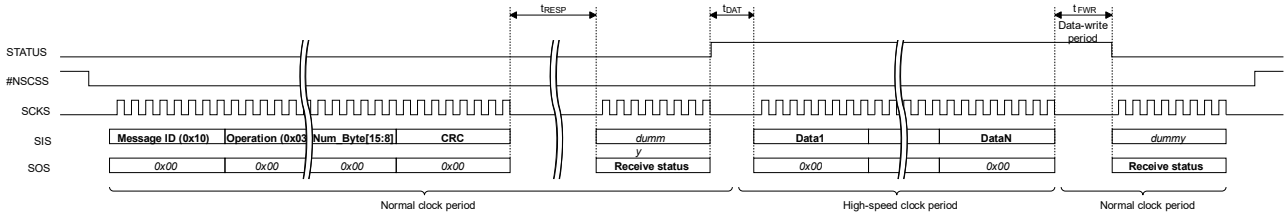


Figure 8.9 Flash Memory Data Write Message Transmission / Reception (SPI)

1. The operations from the ISC_FLASH_PROGRAM_REQ: Write Flash (Write Settings Area) message reception to the receive status (REQ message reception completed) transmission are the same as those for the ordinary REQ message transmission / reception mentioned above.
2. The host switches the SPI clock to a high-speed clock during the t_{DAT} period and transmits write data to this IC.
3. After the write data has been transmitted, the host stops the clock output and waits until the data writing of this IC is completed. While this IC is writing data to the flash memory, the STATUS pin outputs a High level. The host can determine that the writing has completed by monitoring this signal. The host must return the clock to normal speed in this period.
4. After the fall of the STATUS signal is detected, the host outputs the clock and a dummy byte to fetch the receive status (data writing completion notice) being transmitted from this IC.

   If the host outputs the clock before the lapse of t_{FWR}, this IC returns a dummy byte (0x00) to the host until the receive status can be transmitted.
5. The host sets the #NSCSS pin to High to terminate the communication.

Transmission / Reception of REQ Message for Sound Recording

Figure 8.10 and Figure 8.11 show transmission / reception timing charts for the REQ message (ISC_SOUND_ RECORD_START_REQ) that start a sound recording.

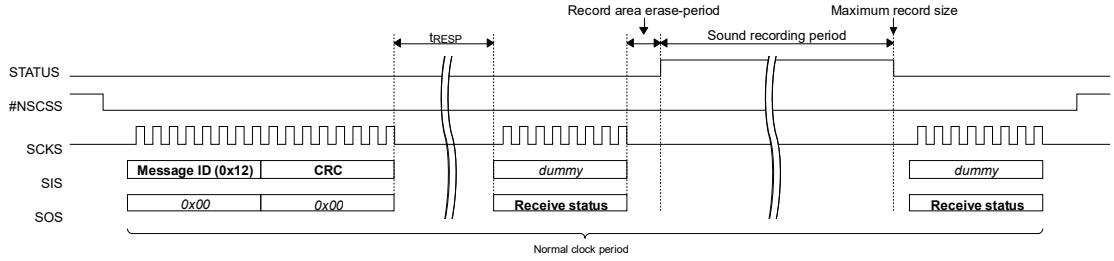


Figure 8.10 ISC_SOUND_RECORD_START_REQ Message Transmission / Reception (SPI) (when recorded up to the maximum recording time)

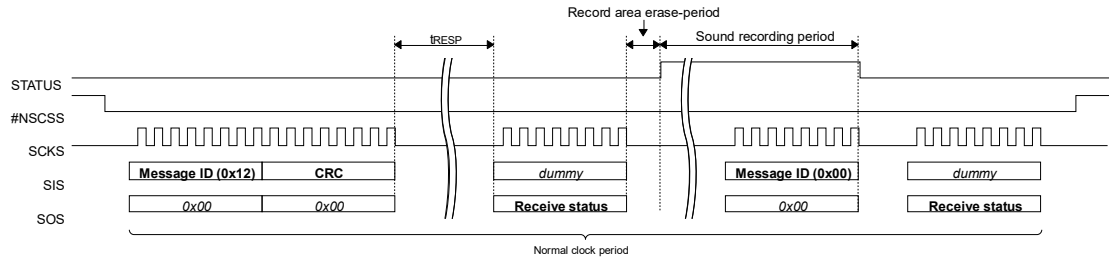


Figure 8.11 ISC_SOUND_RECORD_START_REQ Message Transmission / Reception (SPI) (when the host outputs the clock before reaching the maximum recording time)

1. The operations from the ISC_SOUND_RECORD_START_REQ message reception to the receive status (REQ message reception completed) transmission are the same as those for the ordinary REQ message transmission / reception mentioned above.
2. After the receive status has been received, the host stops the clock output and waits until the sound recording is completed.

   First, this IC erases the recording data area in the external flash memory. And then, this IC sets the STATUS pin to High and starts a sound recording. The STATUS pin remains High until the sound recording is completed. The host can determine that the sound recording has completed by monitoring this signal.

   If the host transmits the ISC_SOUND_RECORD_STOP_REQ message before the lapse of the maximum recording time, this IC stops recording. After that it returns a dummy byte (0x00) to the host until the receive status can be transmitted.
3. After the fall of the STATUS signal is detected, the host outputs the clock and a dummy byte to fetch the receive status (recording completion notice) being transmitted from this IC.
4. The host sets the #NSCSS pin to High to terminate the communication.

IND Message Transmission / Reception

Ordinary IND Message Transmission / Reception

Figure 8.12 shows a timing chart of an IND message transmission / reception.

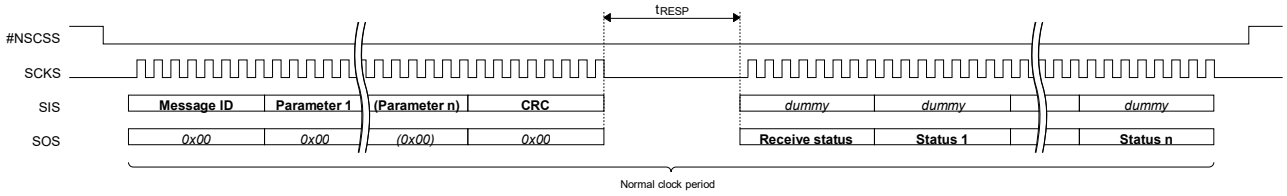


Figure 8.12 IND Message Transmission / Reception (SPI)

1. The host initiates a communication with this IC by setting the #NSCSS pin to Low.
   This IC starts a transmit / receive operation.
2. The host transmits an IND message to this IC.
   This IC receives each IND message byte and calculates CRC. When this IC receives the CRC byte in the message, it compares the calculated CRC with the received CRC (when the CRC check is enabled).

   During this message reception period, this IC outputs dummy bytes (0x00) as the transmit data.
3. The host transmits a dummy byte after the lapse of t_{RESP} (receive status response wait time) from the IND message transmission, for this IC to send the receive status (IND message reception completed).
   If the host outputs the dummy byte before the lapse of t_{RESP}, this IC returns a dummy byte (0x00) to the host until the receive status can be transmitted.
   Therefore, the host can determine that the received byte is the receive status when it is not 0x00.

   When this IC receives the IND message successfully, it returns 0x0F to the host as the receive status. Otherwise, it indicates a reception failure (see Table 8.1).
4. After the receive status (no error) has been received, the host outputs the clock according to the byte length of the status to be obtained to the SCKS pin. During this period, the host outputs dummy bytes as the transmit data.
   This IC returns the read status to the host.
5. The host sets the #NSCSS pin to High to terminate the communication.

Transmission / Reception of IND Message to Transfer Flash Memory Read Data to Host

Figure 8.13 shows a transmission / reception timing chart for the IND message (ISC_FLASH_PROGRAM_ STATUS_IND: Read Flash) that transfers the data read from the flash memory using the ISC_FLASH_ PROGRAM _REQ: Read Flash message. The host can switch the synchronous clock to a high-speed clock during the read data reception to perform high-speed data transfer.

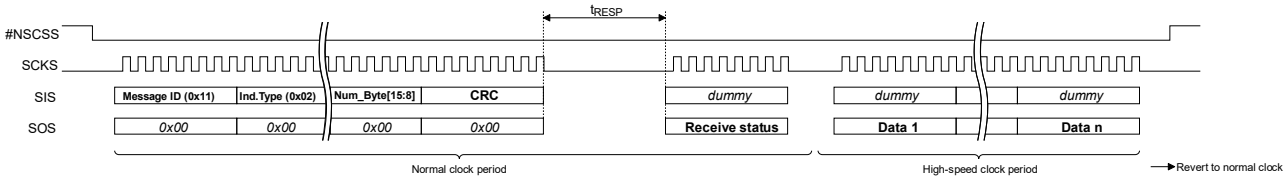


Figure 8.13 Transmission / Reception of IND Message to Obtain Flash Memory Read Data (SPI)

1. The operations from the ISC_FLASH_PROGRAM_STATUS_IND: Read Flash message reception to the receive status (IND message reception completed) transmission are the same as those for the ordinary IND message transmission / reception mentioned above.
2. The host switches the SPI clock to a high-speed clock.
3. The host resumes the clock output and receives data at high speed.
4. After all data have been received, the host returns the clock to normal speed.
5. The host sets the #NSCSS pin to High to terminate the communication.

8.2.2 I²C Interface

This IC includes an I²C interface that has the features below and can be used to communicate with the host in Host Interface mode.

- Slave device (Clock must be supplied from the I²C bus.)
- Data length: 8 bits/word
- Data format: MSB first
- Clock polarity: High at inactive state
- Clock phase: Data bit is sampled at the SCL rising edge and shifted out at the falling edge.
- Clock stretching: Supported
- Maximum SCL frequency: 300 kHz

See Table 6.4 and Figure 6.4 for the I²C interface pin configuration and the connection with the host, respectively.

I²C Transmission / Reception

Slave Address

The figure below shows the 7-bit slave address defined in this IC. The host transmits this slave address at the beginning of a communication to specify that this IC is the slave device of the communication target.

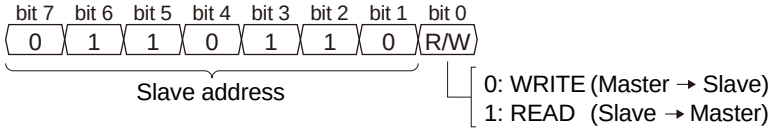


Figure 8.14 I²C Slave Address

Data Write from Host to This IC

Figure 8.15 shows a data write operation to this IC.

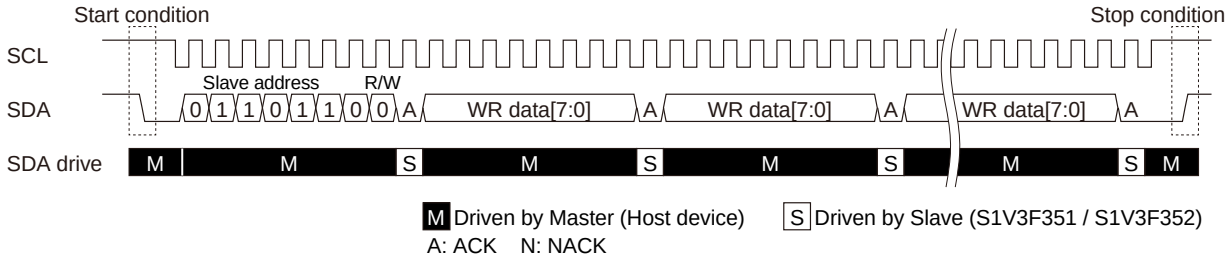


Figure 8.15 Data Write from Host (I^2C)

1. The host initiates a communication with this IC by generating a Start condition (SDA transition from High to Low when SCL = High).
2. The host starts supplying the clock to the SCL line and outputs the slave address with Write mode specified (bit 0 = 0) on the I^2C bus.
3. When a valid slave address (0x6C) is detected, this IC returns an ACK (SDA = Low) to the host and starts a receive operation.
4. After an ACK has been received, the host outputs an 8-bit write data on the SDA line.
5. When an 8-bit data is received, this IC returns an ACK. If this IC is not ready to receive subsequent data at this time, this IC fixes the SCL line at Low (clock stretching state) until it becomes a ready-to-receive status. The host must suspend the next 8-bit data transmission until the clock stretching state is canceled.
6. Steps 4 and 5 are repeated as many times as necessary.
7. The host terminates the communication with this IC by generating a Stop condition (SDA transition from Low to High when SCL = High).

Data Read from this IC by Host

Figure 8.16 shows a data read operation from this IC by the host.

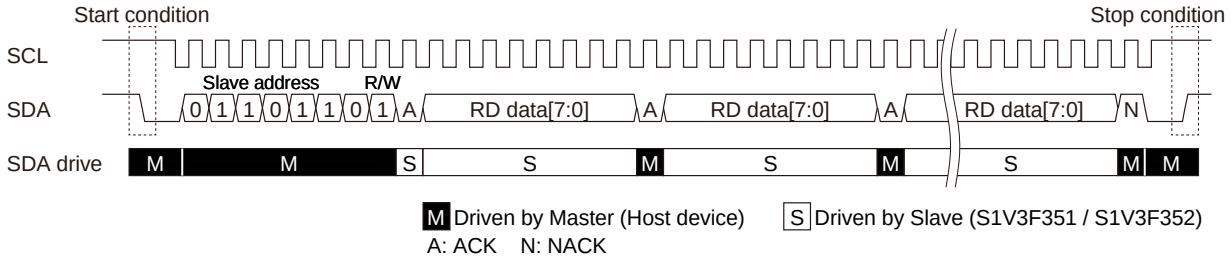


Figure 8.16 Data Read by Host (I^2C)

1. The host initiates a communication with this IC by generating a Start condition (SDA transition from High to Low when SCL = High).
2. The host starts supplying the clock to the SCL line and outputs the slave address with Read mode specified (bit 0 = 1) on the I^2C bus.
3. When a valid slave address (0x6D) is detected, this IC returns an ACK (SDA = Low) to the host and starts a transmit operation.
4. This IC outputs an 8-bit transmit data on the SDA line.
   If this IC is not ready to transmit data at this time, this IC fixes the SCL line at Low (clock stretching state) until it becomes a ready-to-transmit status.
5. When an 8-bit data has been received, the host returns an ACK to this IC.

6. Steps 4 and 5 are repeated as many times as necessary.
   When the last data has been received, the host returns a NACK to this IC at Step 5.
7. The host terminates the communication with this IC by generating a Stop condition (SDA transition from Low to High when SCL = High).

REQ Message Transmission / Reception

Ordinary REQ Message Transmission / Reception

Figure 8.17 shows a timing chart of an ordinary REQ message transmission / reception.

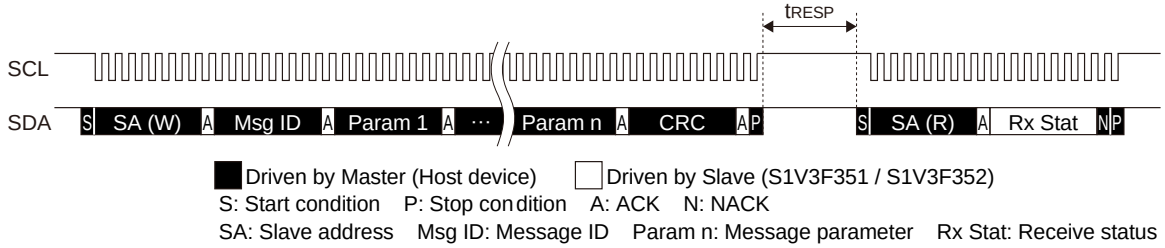


Figure 8.17 REQ Message Transmission / Reception (I^2C)

1. The host generates a Start condition and outputs the slave address to start a data write sequence.
   This IC starts a receive operation.
2. The host outputs a REQ message on the I^2C bus.
   This IC receives each REQ message byte and calculates CRC. When this IC receives the CRC byte in the message, it compares the calculated CRC with the received CRC (when the CRC check is enabled).
3. After the REQ message has been transmitted, the host generates a Stop condition to terminate the data write sequence.
4. The host waits for the lapse of t_{RESP} (receive status response wait time).
5. The host generates a Start condition and outputs the slave address to start a data read sequence.
6. This IC returns the receive status (REQ message reception completed) to the host. The receive status is 0x0F when the REQ message is successfully received. Otherwise, it indicates a reception failure.
7. When the receive status byte has been received, the host returns a NACK, and then generates a Stop condition to terminate the data read sequence.

Transmission / Reception of REQ Message to Request Process Taking Time

Figure 8.18 shows a transmission / reception timing chart when this IC executes the internal processing (flash memory data read / erase, memory check) that requires a certain time (it sets the STATUS pin to High) after a REQ message has been received.

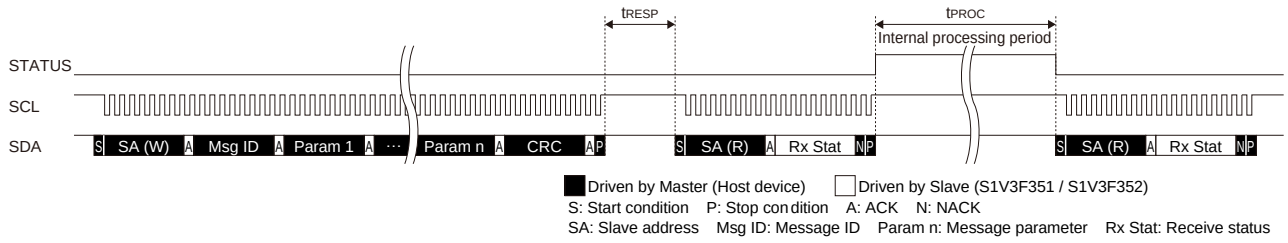


Figure 8.18 Transmission / Reception of REQ Message to Request Process Taking Time (I^2C)

See Table 8.2 for the applicable REQ messages and the processes executed in the t_{PROC} period.

1. The operations from the REQ message reception to the receive status (REQ message reception completed) transmission are the same as those for the ordinary REQ message transmission / reception mentioned above.
2. After the receive status has been received, the host stops the clock output and waits until the internal process of this IC is completed (t_{PROC} period). While this IC is executing the internal process, the STATUS pin outputs a High level. The host can determine that the process has completed by monitoring this signal.
3. After the fall of the STATUS signal is detected, the host starts a data read sequence to fetch the receive status (process completion notice) being transmitted from this IC.
4. The host terminates the data read sequence.

Transmission / Reception of REQ Message for Writing Data to Flash Memory

Figure 8.19 shows a transmission / reception timing chart for the REQ message (ISC_FLASH_PROGRAM _REQ: Write Flash, Write Settings Area) that requests a data writing to the flash memory.

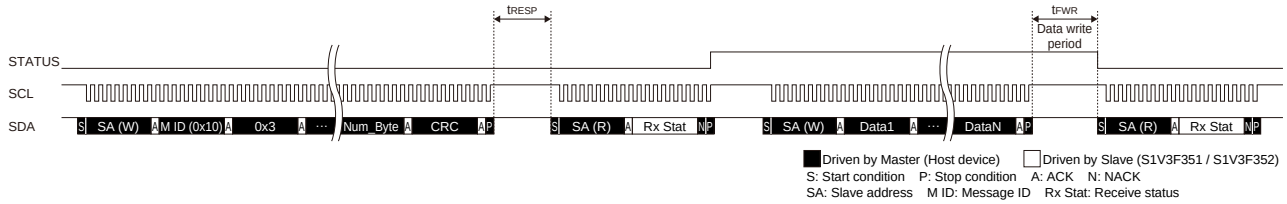


Figure 8.19 Flash Memory Data Write Message Transmission / Reception (I^2C)

1. The operations from the ISC_FLASH_PROGRAM_REQ: Write Flash (Write Settings Area) message reception to the receive status (REQ message reception completed) transmission are the same as those for the ordinary REQ message transmission / reception mentioned above.
2. After the receive status has been received, the host starts a data write sequence and transmits write data to this IC.
3. After the write data has been transmitted, the host stops the clock output and waits until the data writing of this IC is completed. While this IC is writing data to the flash memory, the STATUS pin outputs a High level. The host can determine that the writing has completed by monitoring this signal.
4. After the fall of the STATUS signal is detected, the host starts a data read sequence to fetch the receive status (data writing completion notice) being transmitted from this IC.
5. The host terminates the data read sequence.

Transmission / Reception of REQ Message for Sound Recording

Figure 8.20 and Figure 8.21 show transmission / reception timing charts for the REQ message (ISC_SOUND_ RECORD_START_REQ) that start a sound recording.

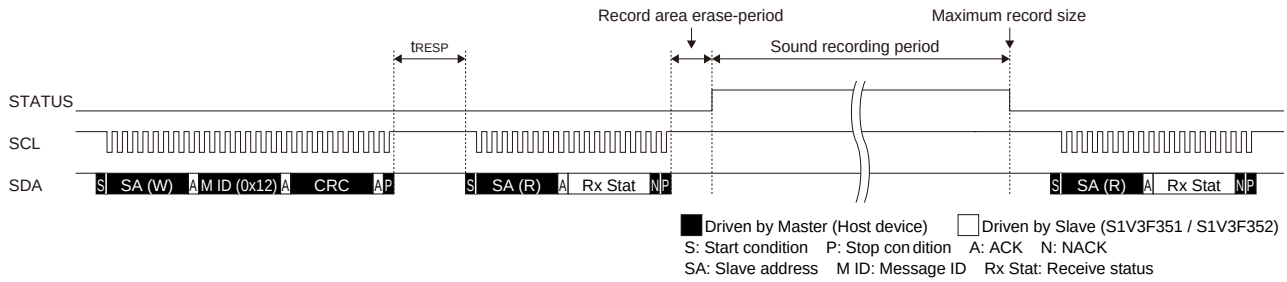


Figure 8.20 ISC_SOUND_RECORD_START_REQ Message Transmission / Reception (I^2C) (when recorded up to the maximum recording time)

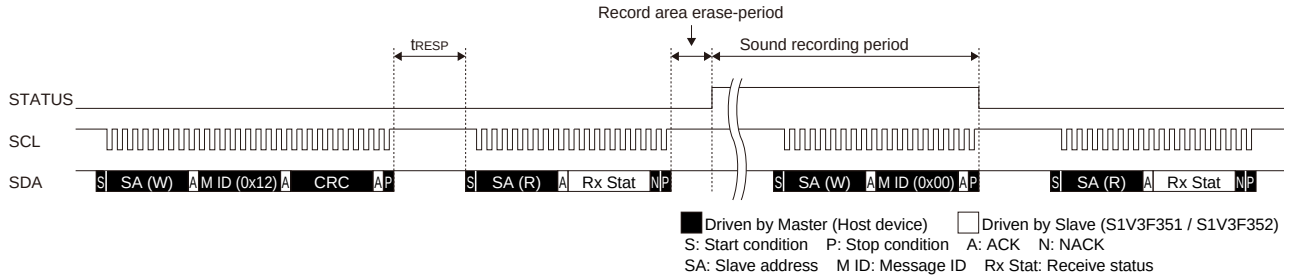


Figure 8.21 ISC_SOUND_RECORD_START_REQ Message Transmission / Reception (I^2C) (when the host outputs the clock before reaching the maximum recording time)

1. The operations from the ISC_SOUND_RECORD_START_REQ message reception to the receive status (REQ message reception completed) transmission are the same as those for the ordinary REQ message transmission / reception mentioned above.
2. After the receive status has been received, the host stops the clock output and waits until the sound recording is completed.

   First, this IC erases the recording data area in the external flash memory. And then, this IC sets the STATUS pin to High and starts a sound recording. The STATUS pin remains High until the sound recording is completed. The host can determine that the sound recording has completed by monitoring this signal.

   If the host transmits the ISC_SOUND_RECORD_STOP_REQ message before the lapse of the maximum recording time, this IC stops recording.
3. After the fall of the STATUS signal is detected, the host starts a data read sequence to fetch the receive status (recording completion notice) being transmitted from this IC.
4. The host terminates the data read sequence.

IND Message Transmission / Reception

Figure 8.22 shows a timing chart of an IND message transmission / reception.

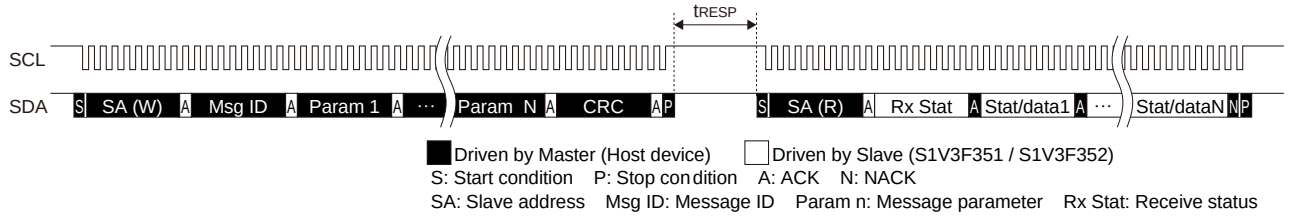


Figure 8.22 IND Message Transmission / Reception (I^2C)

1. The host generates a Start condition and outputs the slave address to start a data write sequence.
   This IC starts a receive operation.
2. The host outputs an IND message on the I^2C bus.
   This IC receives each IND message byte and calculates CRC. When this IC receives the CRC byte in the message, it compares the calculated CRC with the received CRC (when the CRC check is enabled).
3. After the IND message has been transmitted, the host generates a Stop condition to terminate the data write sequence.
4. The host stops the clock output and waits for the lapse of t_{RESP} (receive status response wait time).
5. The host generates a Start condition and outputs the slave address to start data read sequence.
6. This IC transmits the receive status (IND message reception completed). The receive status is 0x0F when the IND message is successfully received. Otherwise, it indicates a reception failure.
7. This IC returns the read status data or flash memory data to the host following the receive status byte.
8. When the last status / data byte has been received, the host returns a NACK, and then generates a Stop condition to terminate the data read sequence.

8.2.3 UART Interface

This IC includes a UART interface that has the features below and can be used to communicate with the host in Host Interface mode.

- Data length: 8 bits/word
- Parity: Even parity, Odd parity, or no parity is selectable.
- Start bit: Fixed at 1 bit.
- Stop bit: 1 bit or 2 bits is selectable.
- Data format: LSB first
- Data line polarity: High at inactive state
- Baud rate: S1V3F351) 9600 bps to 230400 bps, selectable from 6 types.
  S1V3F352) 9600 bps to 115200 or 230400 bps, selectable from 5 or 6 types.
  (The maximum baud rate of the S1V3F352 depends on the operating temperature.
  Refer to *Section 10.8*.)

See Table 6.5 and Figure 6.5 for the UART interface pin configuration and the connection with the host, respectively.

UART Transmission / Reception

Data Format

Figure 8.23 shows the UART data formats (one format can be selected).

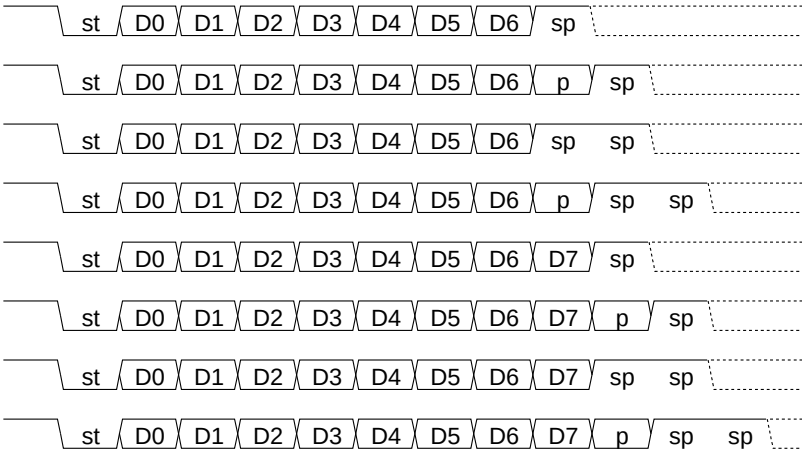


Figure 8.23 UART Data Format

Start Bit

When the transmitter device generates a start bit (sets the transmit line to a Low level), the receiver device starts sampling of the data bits following the start bit. This Low-level period corresponds to 1-bit length of the set baud rate. In this IC, the start bit is fixed as 1 bit.

Data Bits

In this USRT, the serial data length is fixed at 8 bits and data are transferred with LSB first.

Parity Bit

This IC supports parity bit addition and check function.
The parity function is configured with UART_Config[10:9] in the ISC_UART_CONFIG_REQ message.

Table 8.3 Configuration of Parity Function

UART_Config[10:9]	Parity function
0b11	Odd parity
0b01	Even parity
0b10	No parity (default)
0b00	

Stop Bit

The stop bit is placed after the data bit 7 or parity bit and is used to indicate the end of data.
It can be configured to 1 bit or 2 bits using UART_Config[8] of the ISC_UART_CONFIG_REQ message.

Table 8.4 Configuration of Stop Bit

UART_Config[8]	Stop bit
1	2 bits
0	1 bit (default)

Baud Rate

The baud rate can be configured using UART_Config[7:0] of the ISC_UART_CONFIG_REQ message.

Table 8.5 Configuration of Baud Rate

UART_Config[7:0]	Baud rate
Other	Setting prohibited
0x05	230400 bps *
0x04	115200 bps
0x03	57600 bps
0x02	38400 bps
0x01	19200 bps
0x00	9600 bps (default)

* Depending on the operating temperature range, the S1V3F352 cannot select this baud rate (refer to "*10.8 UART Interface Characteristics*").

Data Transfer between Host and This IC

1. The data transmitter device outputs the data signal of each data byte from the TXD pin as shown in Figure 8.23 using its own internal clock.
2. The receiver device starts data sampling when a start bit is input to the RXD pin, and then it fetches the following 8-bit data, parity bit (when the parity check is enabled), and stop bit.
3. When the parity check is enabled, the receiver device calculates parity from the received 8-bit data and compares the result with the received parity bit. If a mismatch occurs, it is handled as a parity error.
   When the stop bit is sampled as 0, it is handled as a framing error (out of sync).

REQ Message Transmission / Reception

Ordinary REQ Message Transmission / Reception

Figure 8.24 shows a timing chart of an ordinary REQ message transmission / reception.

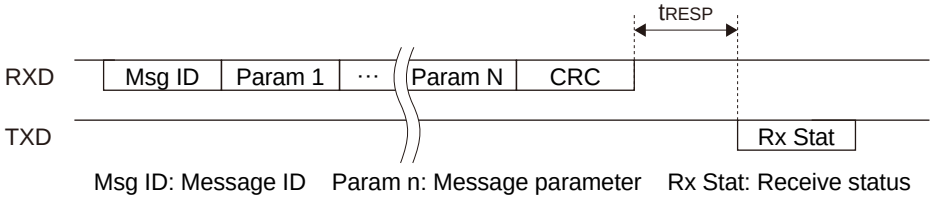


Figure 8.24 REQ Message Transmission / Reception (UART)

1. The host transmits a REQ message to the RXD pin of this IC.
   This IC receives each REQ message byte and calculates CRC. When this IC receives the CRC byte in the message, it compares the calculated CRC with the received CRC (when the CRC check is enabled).

   When a parity error or a flaming error occurs, this IC outputs a High level from the ERROR pin.
2. After the lapse of t_{RESP} (receive status response wait time), this IC transmits the receive status (REQ message reception completed) to the host from the TXD pin. The receive status is 0x0F when the REQ message is successfully received. Otherwise, it indicates a reception failure.

Transmission / Reception of REQ Message to Request Process Taking Time

Figure 8.25 shows a transmission / reception timing chart when this IC executes the internal processing (flash memory data read / erase, memory check) that requires a certain time (it sets the STATUS pin to High) after a REQ message has been received.

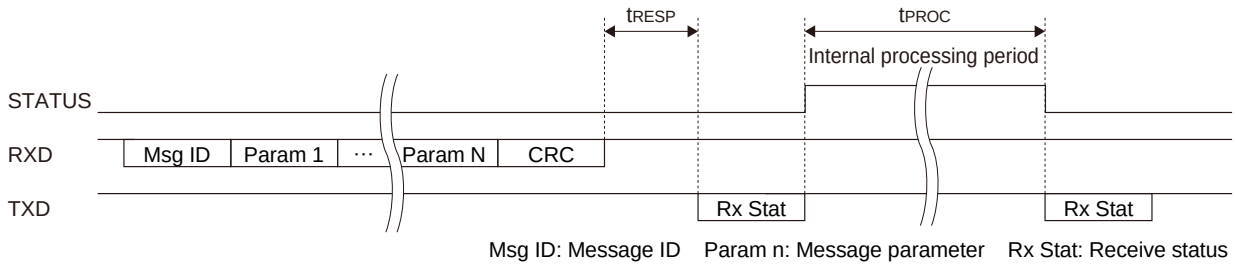


Figure 8.25 Transmission / Reception of REQ Message to Request Process Taking Time (UART)

See Table 8.2 for the applicable REQ messages and the processes executed in the t_{PROC} period.

1. The operations from the REQ message reception to the receive status (REQ message reception completed) transmission are the same as those for the ordinary REQ message transmission / reception mentioned above.
2. After the receive status has been received, the host waits until the internal process of this IC is completed (t_{PROC} period). While this IC is executing the internal process, the STATUS pin outputs a High level. The host can determine that the process has completed by monitoring this signal.
3. After the internal process has completed, this IC sets the STATUS signal to Low and transmits a receive status (process completion notice) to the host.
4. The host fetches the receive status being transmitted from this IC and terminates the REQ message transmission / reception.

Transmission / Reception of REQ Message for Writing Data to Flash Memory

Figure 8.26 shows a transmission / reception timing chart for the REQ message (ISC_FLASH_PROGRAM _REQ: Write Flash) that requests a data writing to the flash memory.

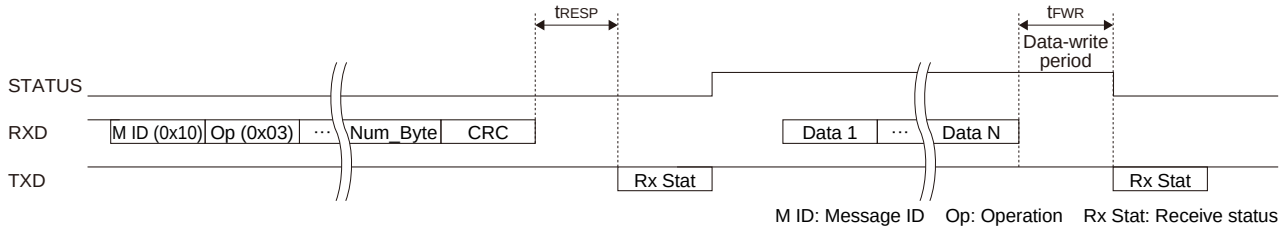


Figure 8.26 Flash Memory Data Write Message Transmission / Reception (UART)

1. The operations from the ISC_FLASH_PROGRAM_REQ: Write Flash (Write Settings Area) message reception to the receive status (REQ message reception completed) transmission are the same as those for the ordinary REQ message transmission / reception mentioned above.
2. After the receive status has been received, the host transmits write data to this IC.
3. After the write data has been transmitted, the host waits until the data writing of this IC is completed. While this IC is writing data to the flash memory, the STATUS pin outputs a High level. The host can determine that the writing has completed by monitoring this signal.
4. After the data writing has completed, this IC sets the STATUS signal to Low and transmits a receive status (data writing completion notice) to the host.
5. The host fetches the receive status being transmitted from this IC and terminates the REQ message transmission / reception.

Transmission / Reception of REQ Message for Sound Recording

Figure 8.27 and Figure 8.28 show transmission / reception timing charts for the REQ message (ISC_SOUND_ RECORD_START_REQ) that starts a sound recording.

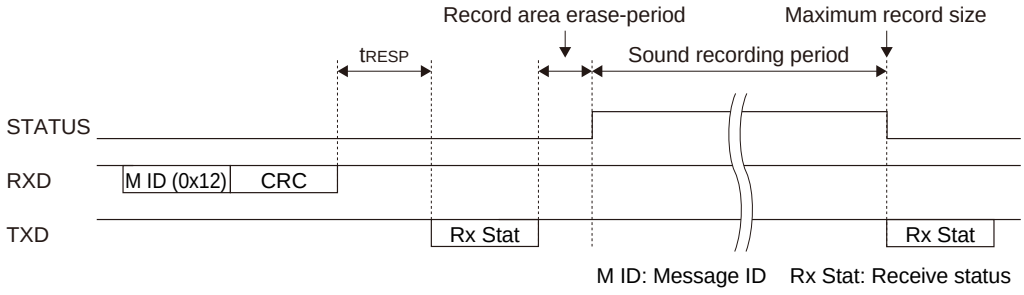


Figure 8.27 ISC_SOUND_RECORD_START_REQ Message Transmission / Reception (UART)
(when recorded up to the maximum recording time)

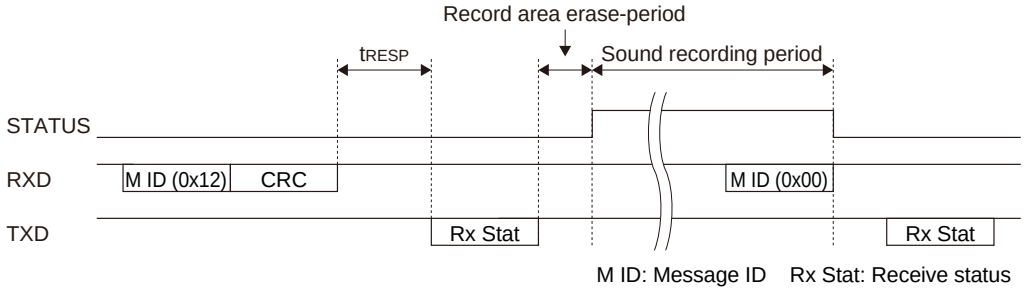


Figure 8.28 ISC_SOUND_RECORD_START_REQ Message Transmission / Reception (UART)
(when the host outputs the clock before reaching the maximum recording time)

1. The operations from the ISC_SOUND_RECORD_START_REQ message reception to the receive status (REQ message reception completed) transmission are the same as those for the ordinary REQ message transmission / reception mentioned above.
2. After the receive status has been received, the host waits until the sound recording is completed.

   First, this IC erases the recording data area in the external flash memory. And then, this IC sets the STATUS pin to High and starts a sound recording. The STATUS pin remains High until the sound recording is completed. The host can determine that the sound recording has completed by monitoring this signal.

   If the host transmits the ISC_SOUND_RECORD_STOP_REQ message before the lapse of the maximum recording time, this IC stops recording.
3. After the recording has completed, this IC sets the STATUS signal to Low and transmits a receive status (recording completion notice) to the host.
4. The host fetches the receive status being transmitted from this IC and terminates the REQ message transmission / reception.

IND Message Transmission / Reception

Figure 8.29 shows a timing chart of an IND message transmission / reception.

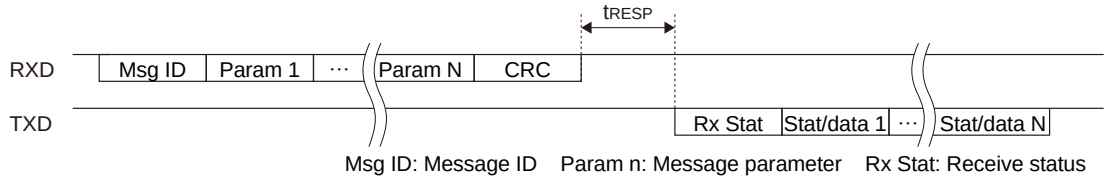


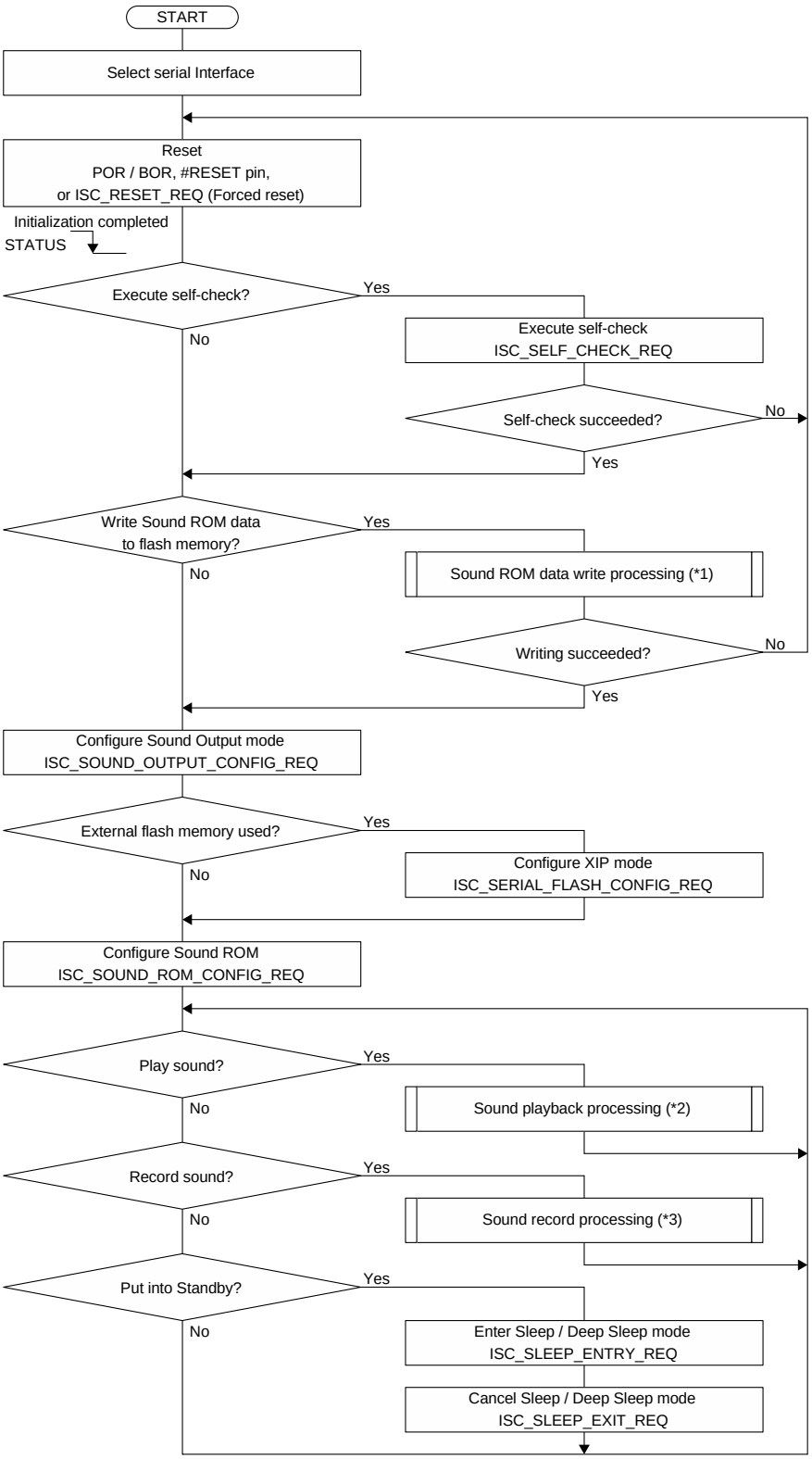
Figure 8.29 IND Message Transmission / Reception (UART)

1. The host transmits an IND message to the RXD pin of this IC.
   This IC receives each IND message byte and calculates CRC. When this IC receives the CRC byte in the message, it compares the calculated CRC with the received CRC (when the CRC check is enabled).

   When a parity error or a flaming error occurs, this IC outputs a High level from the ERROR pin.
2. After the lapse of t_{RESP} (receive status response wait time), this IC transmits the receive status (REQ message reception completed) to the host from the TXD pin. The receive status is 0x0F when the REQ message is successfully received. Otherwise, it indicates a reception failure.
3. This IC returns the read status data or flash memory data to the host following the receive status byte.

8.3 Entire Sound Control Flow

Figure 8.30 shows an entire flow for controlling this IC.



*1: See Figure 8.32 in "*8.4 Writing Sound ROM Data*."
*2: See Figure 8.33 in "*8.5.3 Sound Playback Control Procedure*."
*3: See Figure 8.37 in "*8.7 Sound Recording Function*."

Figure 8.30 Entire Sound Control Flow

8.4 Writing Sound ROM Data

Note: Data to be stored in the flash memory must be written from the host by setting this IC into Host Interface mode even if this IC is assumed to be used in Standalone mode. Therefore, the descriptions in this section are applied to a standalone product development.

When Sound ROM data has not been written in the embedded or external flash memory, it should be written using messages for flash programming.

The ISC_FLASH_PROGRAM_MODE_ACTIVATE_REQ, ISC_FLASH_PROGRAM_REQ, and ISC_FLASH_PROGRAM_STATUS_IND messages are used for programming the flash memory.

After a message is received, this IC informs the operating status (this IC is busy) to the host by setting the STATUS pin to High from starting the flash memory operation until it is completed. The host can determine that the operation has completed by checking if the STATUS signal returns from High to Low. While the STATUS pin outputs High, this IC cannot receive any massages.

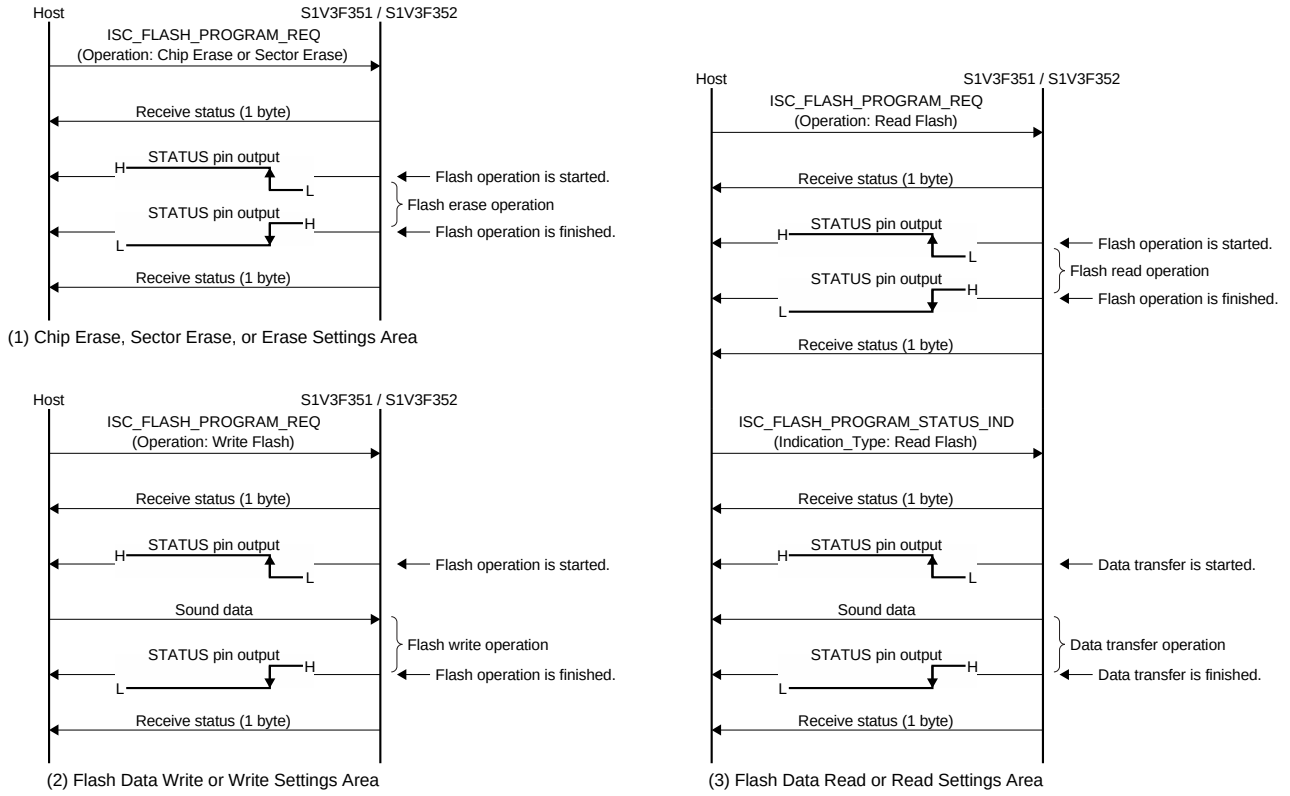


Figure 8.31 Message Flow in Flash Programming Mode

8.4.1 Procedure to Write Sound ROM Data to Embedded / External Flash Memory

The figure below shows a procedure to write Sound ROM data to the flash memory.

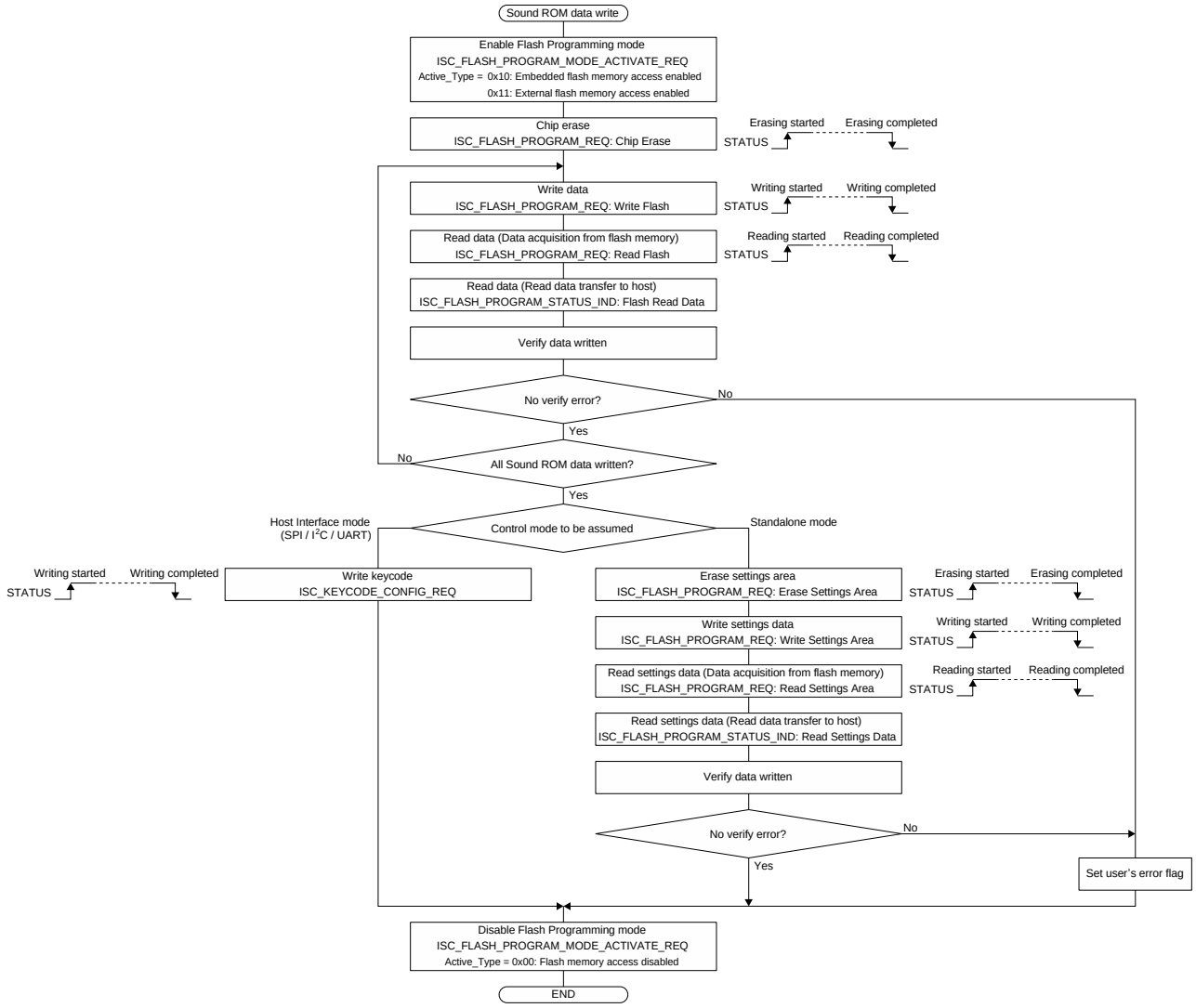


Figure 8.32 Sound ROM Data Writing Flow

Notes: • The name described under a REQ message, e.g., **_Addr[31:0], is a field name in the message that specifies a parameter.

• The operation procedures shown hereafter do not describe the operations to check the receive status that is returned from this IC after the host sends a message. After a message has been sent, the host should check if the receive status is returned before sending a subsequent message.

Enabling Flash Programming Mode

1. Send the ISC_FLASH_PROGRAM_MODE_ACTIVATE_REQ message.
   Activate_Type: 0x10 = Embedded Flash Programming mode
   0x11 = External Flash Programming mode

   This message puts this IC into Embedded Flash Programming mode or External Flash Programming mode.

Writing Sound ROM Data

2. Send the ISC_FLASH_PROGRAM_REQ: Chip Erase message.

   This message erases the Sound ROM area in the embedded flash memory or the entire external flash memory area.
   The STATUS pin goes High during erasing and reverts to Low after the erasing is completed. Further a receive status (erase completion notice) is sent back to the host after the erasing has completed.

3. Send the ISC_FLASH_PROGRAM_REQ: Write Flash message.
   WR_Addr[31:0]: Write area start address (1K-byte boundary address)
   Num_Bytes[15:0]: Write data size (in byte, Max. 1K bytes)

4. After waiting for the return of the receive status responded to the message sent in Step 3, send data to be written to the flash memory (number of bytes specified with Num_Bytes[15:0]).

   This message writes data to the area of the specified size beginning with the specified address.
   The STATUS pin goes High during writing data and reverts to Low when the writing is completed. After the writing has completed, a receive status (writing completion notice) is sent back to the host.

* When the SPI interface is used, the host can perform high-speed data transfer by switching the synchronous clock to a high-speed clock before starting data transmission. However, when the data transmission has completed, the host must restore to the normal clock before transmitting a subsequent message.

Steps 5 to 7 below are a procedure to verify if data was written correctly and it is optional whether these steps are executed or not.

5. Send the ISC_FLASH_PROGRAM_REQ message: Read Flash message.
   RD_Addr[31:0]: Read area start address (1K-byte boundary address)
   Num_Bytes[15:0]: Read data size (in byte, Max. 1K bytes)

   This message reads data of the specified size from the flash memory beginning with the specified address and temporarily stores it in the IC.
   The STATUS pin goes High during reading data and reverts to Low when the reading is completed. After the reading has completed, a receive status (reading completion notice) is sent back to the host.

6. Send the ISC_FLASH_PROGRAM_STATUS_IND: Flash Read Data message.
   Num_Bytes[15:0]: Read data size (in byte, Max. 1K bytes)

   This IC sends the data that has been read in Step 5 from the beginning for the number of bytes specified in this message back to the host.

7. Verify the data written in Step 4 with the data read in Step 6.

   If there is a mismatch in the verification, record it, for example, by setting an error flag, and then disable the Flash Programming mode (Step 15). After that check the host interface connection path and then execute the data writing again by enabling the Flash Programming mode.

8. Repeat Steps 2 to 7 (or Steps 2 to 4) until the sound ROM data is all written.

The subsequent processing is different between Host Interface mode and Standalone mode.

Writing Keycode (for Host Interface mode use)

9. Send the ISC_KEYCODE_CONFIG_REQ message.
   Keycode[31:0]: Keycode

Write the keycode, which has been provided by Seiko Epson, to the flash memory using this message.
The STATUS pin goes High during writing the keycode and reverts to Low when the writing is completed. After the writing has completed, a receive status (keycode writing completion notice) is sent back to the host.

After the keycode has been written, disable Flash Programming mode (Step 15) to restore this IC to Normal mode.

Writing Settings Information (for Standalone mode use)

Note: Writing setting information can be executed only in Embedded Flash Programming mode. An error occurs when executed in External Flash Programming mode.

9. Send the ISC_FLASH_PROGRAM_REQ: Erase Settings Area message.

   This message erases the settings information area in the embedded flash memory.
   The STATUS pin goes High during erasing and reverts to Low after the erasing is completed. Further a receive status (erase completion notice) is sent back to the host after the erasing has completed.

10. Send the ISC_FLASH_PROGRAM_REQ: Write Settings Area message.

11. After waiting for the return of the receive status respondeding to the message sent in Step 10, send data to be written to the settings information area (256 bytes).

    This message writes data to the settings information area in the embedded flash memory.
    The STATUS pin goes High during writing data and reverts to Low when the writing is completed. After the writing has completed, a receive status (writing completion notice) is sent back to the host.

    * When the SPI interface is used, the host can perform high-speed data transfer by switching the synchronous clock to a high-speed clock before starting data transmission. However, when the data transmission has completed, the host must restore to the normal clock before transmitting a subsequent message.

Steps 12 to 14 below are a procedure to verify if data was written correctly and it is optional whether these steps are executed or not.

12. Send the ISC_FLASH_PROGRAM_REQ message: Read Settings Area message.

    This message reads data of 256 bytes from the settings information area in the embedded flash memory and temporarily stores it in the IC.
    The STATUS pin goes High during reading data and reverts to Low when the reading is completed. After the reading has completed, a receive status (reading completion notice) is sent back to the host.

    * This message cannot read the keycode.

13. Send the ISC_FLASH_PROGRAM_STATUS_IND: Read Settings Data message.

    This IC sends the data that has been read in Step 12 back to the host.

14. Verify the data written in Step 11 with the data read in Step 13.

    If there is a mismatch in the verification, record it, for example, by setting an error flag, and then disable the Flash Programming mode (Step 15). After that check the host interface connection path and then execute the data writing again.

Disabling Flash Programming Mode

15. Send the ISC_FLASH_PROGRAM_MODE_ACTIVATE_REQ message.
    Activate_Type: 0x00 = Exit Flash Programming mode

    To terminate the data writing, send this message to restore this IC to Normal Operating mode.

8.5 Sound Playback Function

This section describes a sound playback procedure in Host Interface mode.

8.5.1 Checking Operating State

In Host Interface mode, the functions of this IC are controlled by sending REQ messages from the host. However, depending on the operating state, this IC cannot receive REQ messages. Before a REQ message can be sent to this IC, send an IND message to check the operating state of the channel (Ch.0 / Ch.1) to be controlled.

1. Send the ISC_STATUS_IND: Sound Operation State message.
2. Check the state (CHx_State[15:0]) returned.

Table 8.6 Operating States

CHx_State[15:0]	Operating state
0x0004	Mute state
0x0002	Sound Playback state
0x0001	Idle state
0x0000	Initialization state

8.5.2 Preparation Prior to Sound Playback

The following configurations should be performed before starting a sound playback. Once the configurations are completed, re-configuration is not necessary until it must be changed or this IC is reset.

Configuring Sound Output Destination and Sampling Rate

Configure the sound output destination and sampling rate by sending the ISC_SOUND_OUTPUT_CONFIG_REQ message.

1. Check if this IC is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_OUTPUT_CONFIG_REQ message.
   Sound_Out_Sel: Sound output destination
   Sampling_Rate: Sound sampling rate

Table 8.7 Sound Output Destination Configuration

Sound_Out_Sel	Output destination	
	S1V3F351	S1V3F352
0x07	Speaker output (mode 3)	Speaker output (mode 3)
0x06	4-pin buzzer output (mode 3)	Reserved
0x05	2-pin buzzer output (mode 3)	Reserved
0x04	4-pin buzzer output (mode 1)	Reserved
0x03	2-pin buzzer output (mode 1)	Reserved
0x02	4-pin buzzer output (mode 2)	Reserved
0x01	2-pin buzzer output (mode 2)	2-pin buzzer output (mode 1)
0x00	Speaker output (mode 0)	Speaker output (mode 0)

Table 8.8 Sound Sampling Rate Configuration

Sampling_Rate	Sampling rate
0x01	8 kHz
0x00	16 kHz

Note: When the ISC_SOUND_OUTPUT_CONFIG_REQ message is sent, the parameters that have been previously configured by the following messages are all cleared, therefore, they must be reconfigured.
- ISC_SOUND_ROM_CONFIG_REQ
- ISC_VOLUME_CONFIG_REQ
- ISC_SPEED_CONFIG_REQ
- ISC_PITCH_CONFIG_REQ

Configuring XIP Mode Parameters for External Flash Memory

When using an external flash memory, configure the mode bytes and dummy cycle length for accessing the flash memory in XIP mode by sending the ISC_SERIAL_FLASH_CONFIG_REQ message.

1. Check if this IC is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_SERIAL_FLASH_CONFIG_REQ message.
   XIP_Activate_Byte: Mode byte for activating an XIP session
   XIP_Terminate_Byte: Mode byte for terminating the XIP session
   XIP_Dummy_Cycles: Dummy cycle length (in number of clocks)

The QSPI interface in this IC always outputs the mode bytes from the LSB first. When using a flash memory that expects the mode bytes to be output from the MSB first, specify the mode bytes to XIP_Activate_Byte and XIP_Terminate_Byte in reverse bit order.

Table 8.9 Dummy Cycle Length Configuration

XIP_Dummy_Cycles	Dummy cycle length
0x10	16 clocks
0x0F	15 clocks
...	(Specified value) clocks
0x03	3 clocks
0x02	2 clocks
Other	Setting prohibited

Configuring Sound ROM Information

Select the flash memory to be used for sound playback and configure the Sound ROM data area start address and size by sending the ISC_SOUND_ROM_CONFIG_REQ message.

1. Check if this IC is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_ROM_CONFIG_REQ message.
   Flash_Select: Embedded flash memory / external flash memory selection
   ROM_Addr[31:0]: Sound ROM start address *
   ROM_Size[31:0]: Sound ROM size

Table 8.10 Internal / External Flash Memory Selection

FlashSelect	Flash memory
0x01	External flash memory
0x00	Embedded flash memory

* Sound ROM start address range that can be specified
  S1V3F351 embedded flash memory: 0x0 0000, 0x0 0100 ... 0x0 FF00 (256-byte boundary address)
  S1V3F352 embedded flash memory: 0x0 0000, 0x0 0100 ... 0x2 7F00 (256-byte boundary address)
  External flash memory: 0x00 0000, 0x10 0000 ... 0xF0 0000 (1M-byte boundary address)

8.5.3 Sound Playback Control Procedure

The following describes a sound playback control procedure.

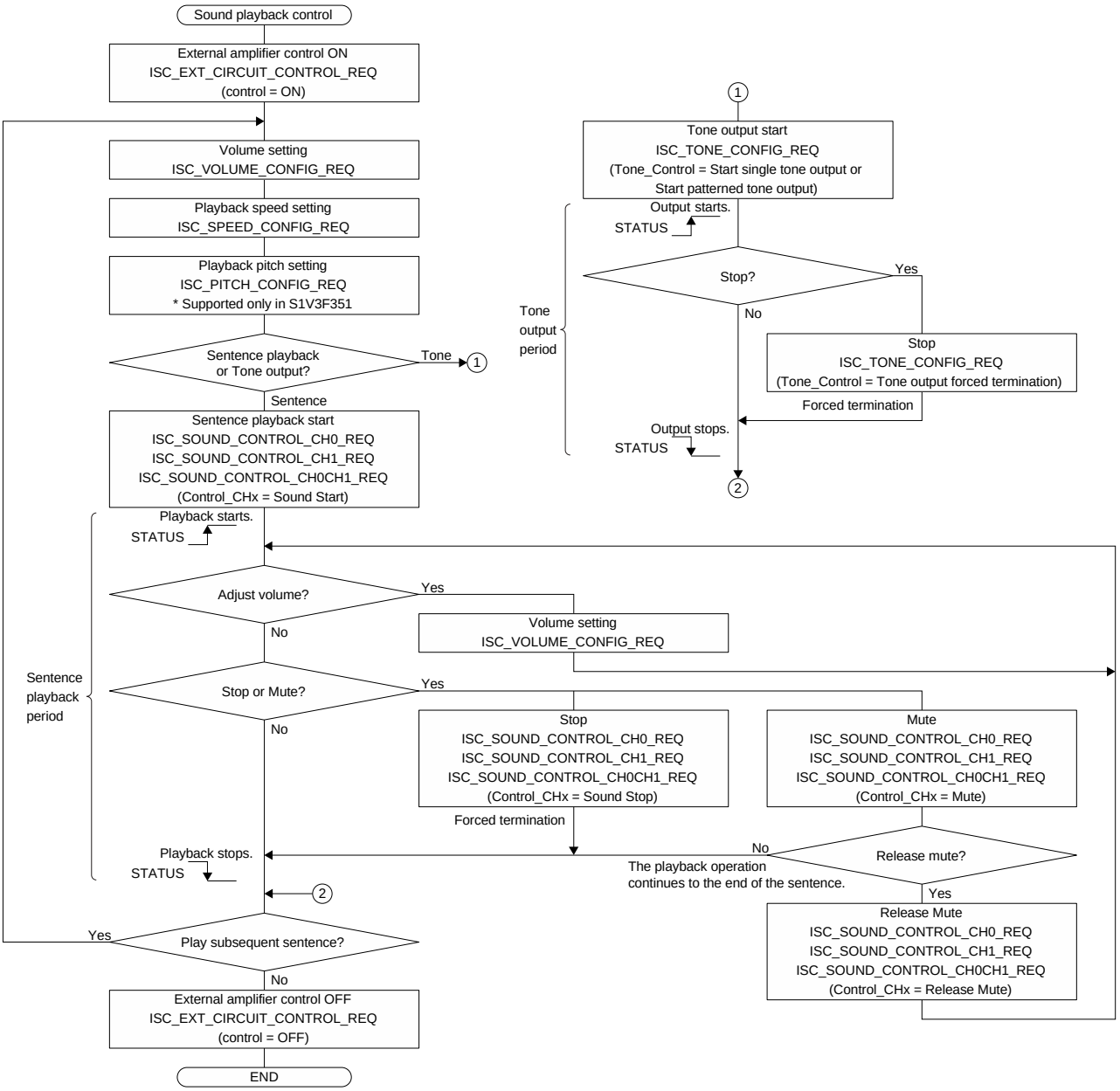


Figure 8.33 Sound Playback Control Flow

Setting Volume

The volume can be changed in each channel individually, regardless of whether in Idle state or Sound Playback state.

1. Send the ISC_VOLUME_CONFIG_REQ message.
   Volume_CH0: Ch.0 volume level
   Volume_CH1: Ch.1 volume level

Table 8.11 Volume Setting

Volume_CHx	Volume
0xFF–0x80	Setting prohibited (error)
0x7F	0 dB
0x7E	-0.5 dB
0x7D	-1.0 dB
:	(Can be specified in 0.5 dB steps.)
0x02	-62.5 dB
0x01	-63.0 dB
0x00	Silent

Setting Sound Playback Speed / Pitch

Set the playback speed and pitch as necessary before starting playback. These setting cannot be changed during playback.

(1) Setting Playback Speed (Effective only in Ch. 0)

Set the playback speed by sending the ISC_SPEED_CONFIG_REQ message.

1. Check if this IC is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_SPEED_CONFIG_REQ message.
   Speed_CH0: Playback speed

Set Speed_CH0 to 0x00 when the playback speed conversion function is not used.

Table 8.12 Playback Speed Settings (when the playback pitch conversion function is disabled*) [S1V3F351, S1V3F352]

Speed_CH0[7:0]	Playback speed	
0x7D	125%	Fast
0x78	120%	↑
0x73	115%	
0x6E	110%	
0x69	105%	
0x64	100%	← Standard speed
0x5F	95%	
0x5A	90%	
0x55	85%	
0x50	80%	↓
0x4B	75%	Slow
0x00	Playback speed conversion disabled	
Other	Setting prohibited	

* Pitch_CH0 of the ISC_PITCH_CONFIG_REQ message = 0x00 (S1V3F351)

When using this function with the playback pitch conversion function, the setting range is limited as shown in the table below.

Table 8.13 Playback Speed Settings (when the playback pitch conversion function is enabled*) [S1V3F351 only]

Speed_CH0[7:0]	Playback speed	
0x73	115%	Fast
0x6E	110%	↑
0x69	105%	
0x64	100%	← Standard speed
0x5F	95%	
0x5A	90%	↓
0x55	85%	Slow
0x00	Playback speed conversion disabled	
Other	Setting prohibited	

* 0x5A ≦ Pitch_CH0 of the ISC_PITCH_CONFIG_REQ message ≦ 0x6E

(2) Setting Playback Pitch (Effective only in S1V3F351 Ch.0)

Set the playback pitch by sending the ISC_PITCH_CONFIG_REQ message.

1. Check if this IC is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_PITCH_CONFIG_REQ message.
   Pitch_CH0: Playback pitch

Set Pitch_CH0 to 0x00 when the playback pitch conversion function is not used.

Table 8.14 Playback Pitch Settings (when the playback speed conversion function is disabled*)

Pitch_CH0[7:0]	Pitch	
0x7D	125%	High
0x78	120%	↑
0x73	115%	
0x6E	110%	
0x69	105%	
0x64	100%	← Standard pitch
0x5F	95%	
0x5A	90%	
0x55	85%	
0x50	80%	↓
0x4B	75%	Low
0x00	Playback pitch conversion disabled	
Other	Setting prohibited	

* Speed_CH0 of the ISC_SPEED_CONFIG_REQ message = 0x00

When using this function with the playback speed conversion function, the setting range is limited as shown in the table below.

Table 8.15 Playback Pitch Settings (when the playback speed conversion function is enabled*)

Pitch_CH0[7:0]	Pitch	
0x6E	110%	High
0x69	105%	↑
0x64	100%	← Standard pitch
0x5F	95%	↓
0x5A	90%	Low
0x00	Playback pitch conversion disabled	
Other	Setting prohibited	

* 0x55 ≦ Speed_CH0 of the ISC_SPEED_CONFIG_REQ message ≦ 0x73

Table 8.16 Setting Allowable Range when Converting Speed and Pitch Simultaneously [S1V3F351 only]

			Pitch_CH0											
			0x7D	0x78	0x73	0x6E	0x69	0x64	0x5F	0x5A	0x55	0x50	0x4B	0x00
			125%	120%	115%	110%	105%	100%	95%	90%	85%	80%	75%	–
Speed_CH0	0x7D	125%	–	–	–	–	–	–	–	–	–	–	–	OK
	0x78	120%	–	–	–	–	–	–	–	–	–	–	–	OK
	0x73	115%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x6E	110%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x69	105%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x64	100%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x5F	95%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x5A	90%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x55	85%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x50	80%	–	–	–	–	–	–	–	–	–	–	–	OK
	0x4B	75%	–	–	–	–	–	–	–	–	–	–	–	OK
	0x00	–	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK

Controlling External Amplifier Circuit

This IC provides the EXT_CIRCUIT_CTRL pin of which the output can be used as the control signal to turn the external amplifier circuit for the speaker or buzzer On and Off. Send the ISC_EXT_CIRCUIT_CONTROL_REQ message to turn the amplifier circuit On before starting a sound playback or to turn Off after the sound playback ends.

1. Check if this IC is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_EXT_CIRCUIT_CONTROL_REQ message.
   Control: 0x01 = On, 0x00 = Off

Take an appropriate wait time according to the external circuit specifications until a sound playback starts after turning the external amplifier circuit On using this message, and until turning the external amplifier circuit Off after the sound playback has ended.

Controlling Sound Playback

The sound playback is controlled with the playback control commands (Control_CHx) that can be specified using the ISC_SOUND_CONTROL_CHx_REQ message provided for each channel. Also the ISC_SOUND_CONTROL_CH0CH1_REQ message is provided to control Ch.0 and Ch.1 simultaneously. Table 8.17 lists the playback control commands.

Table 8.17 List of Playback Control Commands (Control_CHx)

Control_CHx / Control_CH0CH1	Playback control command
Other	Setting prohibited (error)
0x09	Release Mute
0x08	Mute after Current Phrase
0x07	Mute Immediately
0x03	Sound Stop after Current Phrase
0x02	Sound Stop Immediately
0x01	Sound Start

(1) Starting / Stopping Sound Playback

This IC can play sounds of each channel individually or two channels mixed (e.g., Ch.0 outputs a voice and Ch.1 outputs a BGM). The sound to be played is specified by a sentence number.

Individual Control of Ch.x (Ch.0 / Ch.1)

The following shows a playback starting procedure:

1. Check if Ch.x is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_CONTROL_CHx_REQ message.
   Control_CHx: Sound Start
   Sentence_CHx[15:0]: Sentence number to be played
   Repeat_CHx: Playback repeat count for the selected sentence

   This message plays the sound data specified with the sentence number for the specified repeat count. The playback stops automatically at the end of repeated sound data, and Ch.x enters Idle state.
   CHx_Sentence[15:0] should be set to the sentence number displayed on "ESPER2."

(CHx = CH0 or CH1)

Table 8.18 Repeat Count Specification

Repeat_CHx	Playback repeat count
0xFF	Repeat until Sound Stop command execution
0xFE	254 times
0x7E	253 times
:	:
0x03	3 times
0x02	2 times
0x01, 0x00	1 time (no repetition)

When the Sound Start command is sent again during a playback, the current playback is terminated and it restarts from the beginning of the specified sentence.

The following shows a forced playback termination procedure:

1. Check if Ch.x is in Sound Playback state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_CONTROL_CHx_REQ message.
   Control_CHx: Sound Stop Immediately or Sound Stop after Current Phrase

   An arbitrary value can be specified for Sentence_CHx[15:0] and Repeat_CHx.

   The Sound Stop Immediately command terminates the current playback immediately after this message is sent. At this time, a fade-out process is carried out to suppress the occurrence of noise.
   The Sound Stop after Current Phrase command terminates the current playback at the end of the phrase being output when this message is sent.
   Ch.x enters Idle state after the sound playback operation is completed.

Simultaneous Control of Ch.0 and Ch.1 (Channel Mixing Output)

The following shows a playback starting procedure:

1. Check if Ch.0 and Ch.1 are in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_CONTROL_CH0CH1_REQ message.
   Control_CH0CH1: Sound Start
   Sentence_CH0[15:0]: Sentence number to be played in Ch.0
   Sentence_CH1[15:0]: Sentence number to be played in Ch.1
   Repeat_CH0: Playback repeat count for the selected sentence of Ch.0
   Repeat_CH1: Playback repeat count for the selected sentence of Ch.1

   This message plays the Ch.0 and Ch.1 sound data specified with the respective sentence numbers for the specified repeat count. The playback stops automatically at the end of repeated sound data, and this IC enters Idle state.
   Sentence_CHx[15:0] should be set to the sentence number displayed on "ESPER2."

When a Sound Start command is sent again during a playback, the current playback is terminated and it restarts from the beginning of the specified sentences of Ch.0 and Ch.1.

The following shows a forced playback termination procedure:

1. Check if Ch.0 and Ch.1 are in Sound Playback state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_CONTROL_CH0CH1_REQ message.
   Control_CH0CH1: Sound Stop Immediately or Sound Stop after Current Phrase

   An arbitrary value can be specified for Sentence_CHx[15:0] and Repeat_CHx.

   The Sound Stop Immediately command terminates the current playback of both channels immediately after this message is sent. At this time, a fade-out process is carried out to suppress the occurrence of noise.
   The Sound Stop after Current Phrase command terminates the current playback of each channel at the end of the phrase being output when this message is sent.
   Ch.0 and Ch.1 enter Idle state after the sound playback operation is completed.

STATUS Pin (Status Signal) Output

The STATUS pin goes High when a playback starts; it reverts to Low when the playback stops.
For detail of the STATUS output timing, refer to "*10.13 STATUS Output Timing*."

(2) Changing Volume

The volume can be changed even if this IC is playing a sound. For more information, refer to "*Setting Volume*" mentioned above.

(3) Mute

Setting Mute State

1. Check if Ch.x is in Sound Playback state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_CONTROL_CHx_REQ message.
   Control_CHx: Mute Immediately or Mute after Current Phrase

   During channel mixing output, send the ISC_SOUND_CONTROL_CH0CH1_REQ message (Control_CH0CH1: Mute Immediately or Mute after Current Phrase).

   The Mute Immediately command mutes the current sound output immediately after this message is sent. At this time, a fade-out process is carried out to suppress the occurrence of noise.
   The Mute after Current Phrase command mutes the current sound output at the end of the phrase being output when this message is sent.

The playback sequence continues even in Mute state.

If the sound data ends in Mute state, this IC returns to Idle state and cancels mute (the subsequent playback sound will not be muted).

Canceling Mute State

1. Check if Ch.x is in Mute state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_CONTROL_CHx_REQ message.
   Control_CHx: Release Mute

   During channel mixing output, send the ISC_SOUND_CONTROL_CH0CH1_REQ message (Control_CH0CH1: Release Mute).

   This message cancels mute. The volume returns to the original level with the sound playback operation continued. At this time, a fade-in process is carried out to suppress the occurrence of noise.

8.6 Tone Output Function

The tone output function outputs square wave(s) with a frequency specified as a tone signal. A patterned tone generated with up to four frequencies can be output as well as a single frequency tone output.

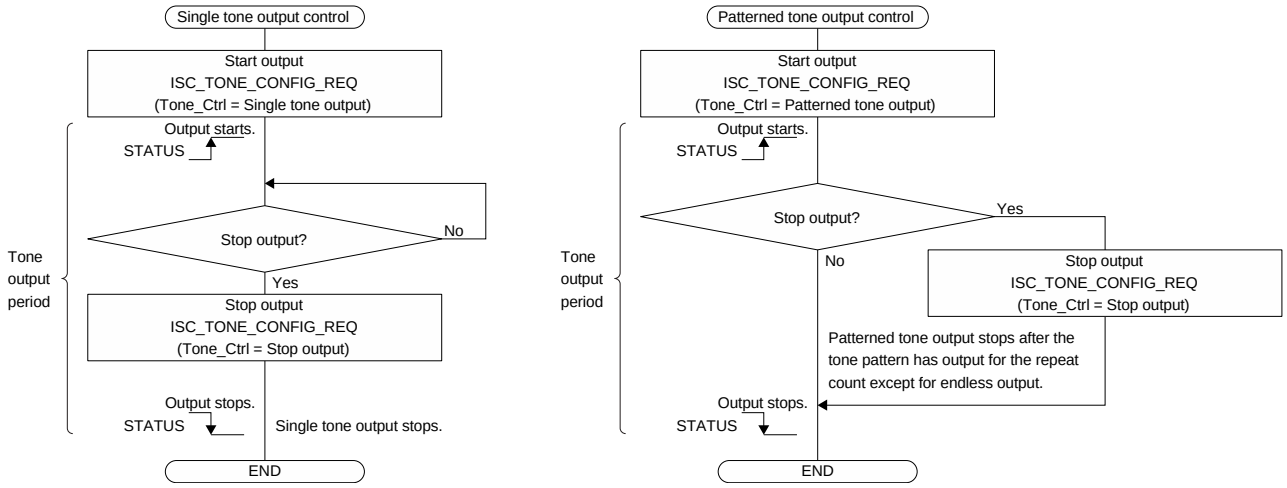


Figure 8.34 Tone Output Control Flow

8.6.1 Single Tone Output

This function generates a tone signal with a single frequency (31 Hz to 16 kHz) and outputs the generated tone. The tone output continues until a REQ message for termination is received.

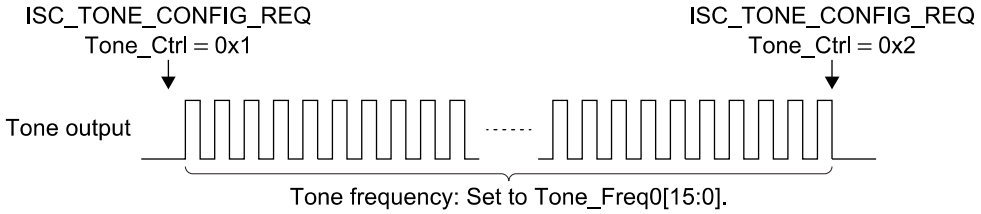


Figure 8.35 Single Tone Output

The following shows a control procedure:

1. Check if Ch.0 and Ch.1 are in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_TONE_CONFIG_REQ message.
   Tone_Freq0[15:0]: Output tone frequency
   Tone_Ctrl: 0x01 (Single tone output)

   This message outputs the configured tone signal. The single tone output does not stop automatically.
3. Send the ISC_TONE_CONFIG_REQ message.
   Tone_Ctrl: 0x2 (Tone output forced termination)

   This message terminates the tone output.

Table 8.19 Tone Frequency Setting

Tone_FreqX[15:0]	Tone frequency
Other	Setting prohibited
0x3E80	16000 Hz
0x3E7F	15999 Hz
:	:
0x0021	33 Hz
0x0020	32 Hz
0x001F	31 Hz

8.6.2 Patterned Tone Output

A patterned tone can be generated by specifying up to four frequencies within the range from 31 Hz to 16 kHz and their output durations and it can be output. The generated patterned tone can be output repeatedly for the specified number of times (up to 254 times) or until it is forcibly terminated by sending a REQ message.

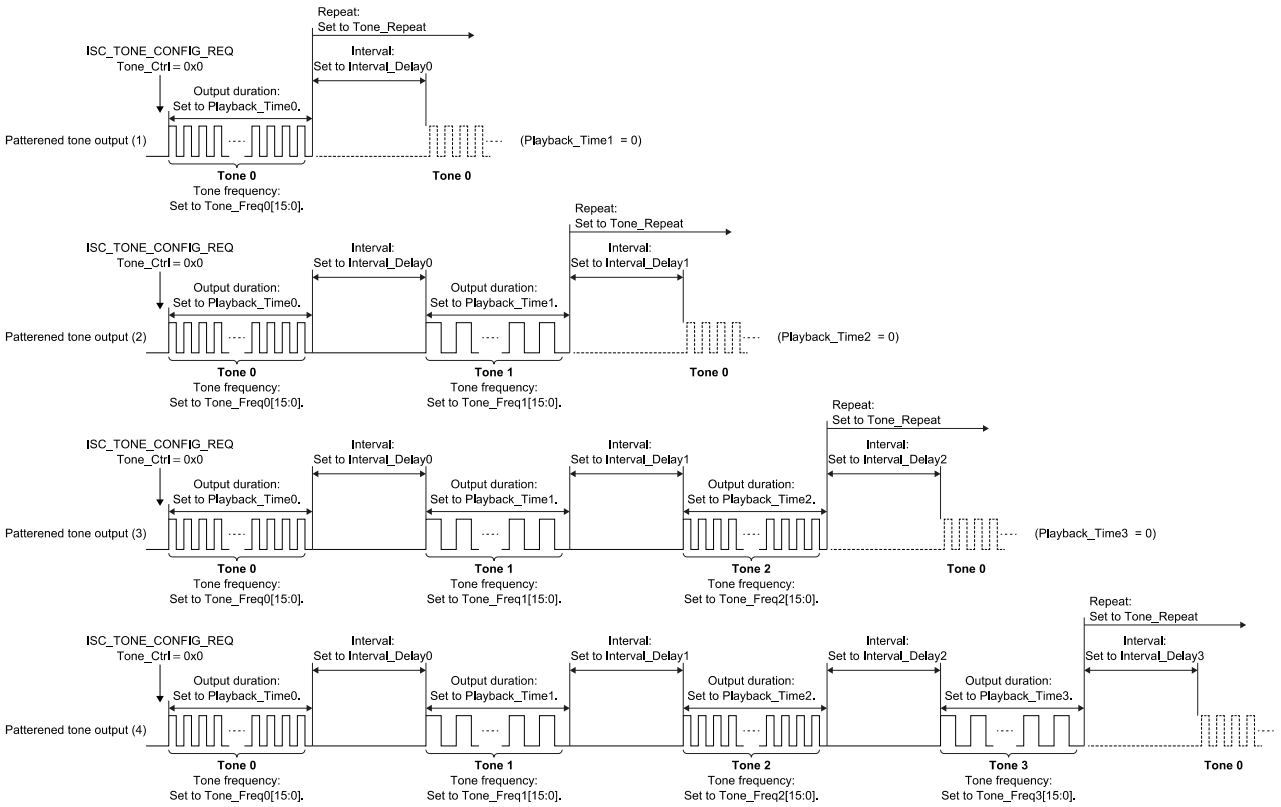


Figure 8.36 Patterned Tone Output

The following shows a control procedure:

1. Check if Ch.0 and Ch.1 are in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_TONE_CONFIG_REQ message.
   Tone_Ctrl: 0x0 (Patterned tone output)
   Tone_Freq0[15:0]: Tone 0 frequency
   Playback_Time0: Tone 0 output duration
   Interval_Delay0: Interval between Tones 0 and 1 (silent time)
   Tone_Freq1[15:0]: Tone 1 frequency
   Playback_Time1: Tone 1 output duration
   Interval_Delay1: Interval between Tones 1 and 2 (silent time)
   Tone_Freq2[15:0]: Tone 2 frequency
   Playback_Time2: Tone 2 output duration
   Interval_Delay2: Interval between Tones 2 and 3 (silent time)
   Tone_Freq3[15:0]: Tone 3 frequency
   Playback_Time3: Tone 3 output duration
   Interval_Delay3: Interval between Tones 3 and 0 (silent time)
   Tone_Repeat: Tone output repeat count

This message starts the configured patterned tone output sequence. The output automatically stops after the sequence is repeated for the specified number of times.

If Playback_TimeX is set to 0, the subsequent settings are ignored.

The following shows a forced termination method when endless output is specified as the repeat count or before the repeat count reaches the specified number of times:

1. Send the ISC_TONE_CONFIG_REQ message.
   Tone_Ctrl: 0x2 (Tone output forced termination)

For the tone frequency selections, see Table 8.19.

Table 8.20 Tone Output Duration Setting

Playback_TimeX	Tone output duration
0xFF	2550 ms
0xFE	2540 ms
:	(Can be specified in 10 ms units)
0x02	20 ms
0x01	10 ms
0x00	0 ms

Table 8.21 Tone Output Interval Setting

Interval_DelayX	Tone output interval
0xFF	2550 ms
0xFE	2540 ms
:	(Can be specified in 10 ms units)
0x02	20 ms
0x01	10 ms
0x00	0 ms

Table 8.22 Patterned Tone Output Repeat Count Specification

Tone_Repeat	Output repeat count
0xFF	Endless output
0xFE	254 times
0x7E	253 times
:	:
0x03	3 times
0x02	2 times
0x01	1 time (No repetition)
0x00	

8.7 Sound Recording Function

This section describes a sound recording procedure in Host Interface mode.

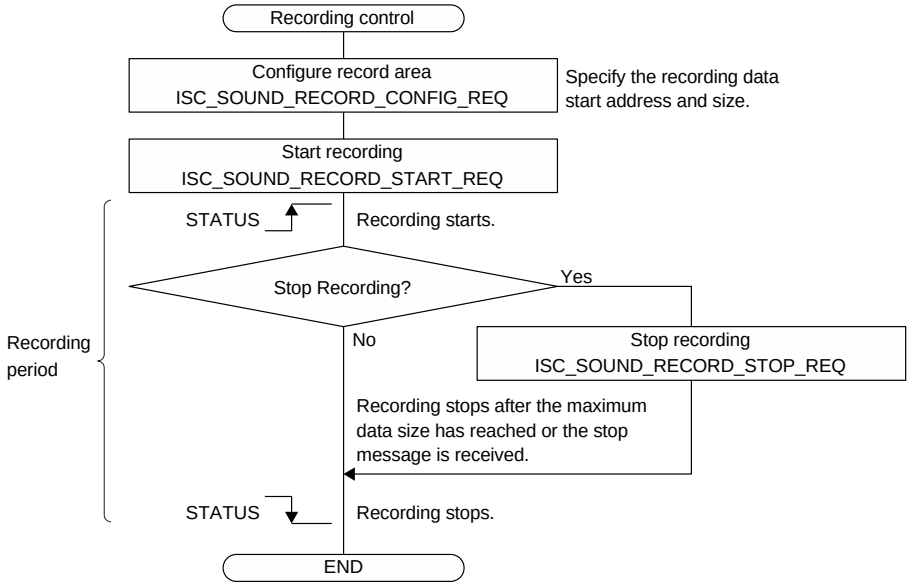


Figure 8.37 Sound Recording Control Flow

Configuring Recording Data Area

Before a recording can be started, configure the recording data area by sending the ISC_SOUND_RECORD_CONFIG_REQ message.

1. Check if this IC is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_RECORD_CONFIG_REQ message.
   Rec_Start_Addr[31:0]: Recording data area start address in the external flash memory
   Max_Rec_Size[15:0]: Maximum recording data size (block = 64K-byte units, e.g., specify 16 for 1M bytes)

Starting Sound Recording

A sound recording starts by sending the ISC_SOUND_RECORD_START_REQ message.

1. Check if this IC is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_RECORD_START_REQ message.

This IC operates as follows:

1. Erases the recording data storage area in the external flash memory.
2. After the recording data area has been erased, the STATUS pin goes High to inform the host that a recording has started.
3. Samples the input from the external microphone module cyclically and converts it into digital data using the internal AD converter. The converted data is stored in the recording data area.
4. Repeats Step 3 until the terminating condition is established.

During recording processing from Steps 1 to 4, this IC cannot accept any messages except for the recording termination message.

Terminating Sound Recording

The sound recording that has started is terminated when data for maximum recording size is stored or when the ISC_SOUND_RECORD_STOP_REQ message is received. When the sound recording is terminated, the STATUS pin goes Low to inform the host that the recording processing has completed. After that, the messages sent from the host can be accepted.

Playing Recorded Sound Data

The recorded sound data can be played as in the following procedure:

1. Check if this IC is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_SOUND_OUTPUT_CONFIG_REQ message.
   Sound_Out_Sel: Sound output destination
   Sampling_Rate: Sound sampling rate

   * This step is not necessary if the configuration has been completed using this message.
3. Send the ISC_SOUND_ROM_CONFIG_REQ message.
   Flash_Select: 0x01 (External flash memory)
   ROM_Addr[31:0]: Sound ROM start address
   ROM_Size[31:0]: Sound ROM size
4. Send the ISC_SOUND_RECORD_CONFIG_REQ message.
   ROM_Addr[31:0]: Recording data area start address in the external flash memory
   ROM_Size[31:0]: Maximum recording data size (block = 64K-byte units, e.g., specify 16 for 1M bytes)
5. Send the ISC_VOLUME_CONFIG_REQ message as necessary.
   Volume_CH0: Ch.0 volume
6. Send the ISC_SPEED_CONFIG_REQ message as necessary.
   Speed_CH0: Playback speed

   When not using the playback speed conversion function, set Speed_CH0 to 0x00.
7. Send the ISC_PITCH_CONFIG_REQ message as necessary. (S1V3F351 only)
   Pitch_CH0: Playback pitch

   When not using the pitch conversion function, set Pitch_CH0 to 0x00.
8. Send the ISC_SOUND_CONTROL_CH0_REQ message.
   Control_CH0: Sound Start
   Sentence_CH0[15:0]: 0x0000 (Sentence number to be played = 0)
   Repeat_CH0[7:0]: Playback repeat count for the selected sentence

   This message plays the sound data of Sentence No. 0 (recorded data) for the specified repeat count. The playback stops automatically at the end of repeated sound data, and Ch.0 of this IC enters Idle state.

For other sound playback functions (forced termination, mute, mixed output with Ch.1), refer to "*8.5.3 Sound Playback Control Procedure*."

8.8 Sound Data CRC Check Function

This IC is equipped with a CRC check function that performs a CRC check for the sound data stored in the embedded flash memory or the external flash memory.

Execution Procedure

1. Check if this IC is in Idle state (refer to *Section 8.5.1*).
2. Send the ISC_FLASH_PROGRAM_MODE_ACTIVATE_REQ message.
   Activate_Type: 0x10 = Embedded Flash Programming mode
   0x11 = External Flash Programming mode

   This message selects the flash memory to be checked.
3. Send the ISC_FLASH_PROGRAM_REQ: CRC Check message.
   Addr[31:0]: CRC check area start address
   Num_Bytes[31:0]: CRC check area size
   Flash_CRC: Original CRC value (CRC value obtained when the Sound ROM data was generated)

This IC reads data from the specified area and calculates the CRC value, and then compares it with the original CRC value sent by the message above.

The STATUS pin outputs a High level from the start to end of the CRC check. This IC does not accept any message during this period.

CRC Check Result Confirmation Procedure

1. Check if the STATUS pin goes Low (CRC check has completed).
2. Send the ISC_STATUS_IND: Error/Warning Status message.

No CRC error has occurred when the returned ERROR1[15:0] status Bit 11 = 0.
If Bit 11 = 1, a CRC error has occurred. In this case, write the sound data again.

8.9 Standby Function

This section describes how to enter to and return from a standby mode (Sleep mode or Deep Sleep mode) by sending a message.

Entering Standby Mode

1. Send the ISC_SLEEP_ENTRY_REQ message.
   Mode: Sleep mode / Deep Sleep mode specification

   This message puts this IC into the standby mode specified with Mode.

Table 8.23 Entering Standby Mode

Mode	Standby mode
Other than 0x00	Deep Sleep mode
0x00	Sleep mode

Sleep mode stops clock supply to the internal circuits while the system clock (16 MHz) is being continuously operated.

Deep Sleep mode stops all clocks including the system clock (16 MHz).

When a standby (Sleep or Deep Sleep) mode is entered, the EXT_CIRCUIT_CTRL pin goes Off. Therefore, the external speaker amplifier or buzzer amplifier controlled with this signal also stops operating.

Returning from Standby Mode

SPI / I^2C (Return from Sleep / Deep Sleep mode), UART (Return from Sleep mode)

1. Send the message ID (0xXX) of the ISC_SLEEP_EXIT_REQ message.

   When this message is received, this IC exits from the standby mode and enters Idle mode.

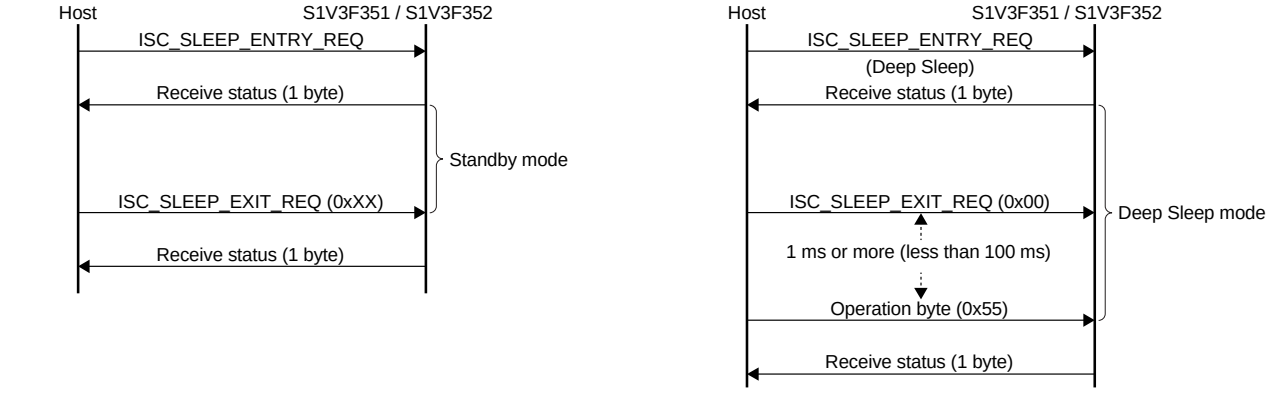
UART (Return from Deep Sleep mode)

1. Send the message ID (0x00) of the ISC_SLEEP_EXIT_REQ message.
2. Wait for at least 1 ms (less than 100 ms) and then send the Operation byte (0x55) for exiting from Deep Sleep mode in UART.
3. Receive the receive status (0x0F) sent from this IC.

   When this message is received, this IC exits from Deep Sleep mode and enters Idle mode. However, if the wait time in Step 2 exceeds 100 ms, this message becomes ineffective and this IC continues Deep Sleep mode. In this case, this IC does not exit from Deep Sleep mode and does not return a receive status (0x0F) even if the Operation byte (0x55) is sent from the host after 100 ms has elapsed.

After this IC receives this message, it takes a restoration time until it enters Idle mode (ready-to-playback status). For the restoration time, refer to "*10.14 Standby Mode AC Characteristics*."

The EXT_CIRCUIT_CTRL pin does not revert to On even if the operation mode is returned from a standby mode. Set it to output On again by sending the ISC_EXT_CIRCUIT_CONTROL_REQ message before starting a subsequent sound playback.



(1) SPI / I²C (Return from Sleep / Deep Sleep mode)
UART (Return from Sleep mode)

(2) UART (Return from Deep Sleep mode)

Figure 8.38 Standby Control

8.10 Error Handling

When an error occurs while this IC is receiving a message or is in Flash Programming mode, the ERROR pin (normal Low) goes High to inform the host that an error has occurred.

For more information on the ERROR signal assert / negate timings, refer to "*10.12 ERROR Output Timing*."

8.10.1 Kind of Error and Confirmation Method

After the ERROR signal = High is detected, the host can confirm the kind of error that has occurred by sending an IND message.

This IC sends back an ERROR0[15:0] or ERROR 1[15:0] status when an ISC_STATUS_IND: Error / Warning Status message is sent from the host.

ERROR0

ERROR 0 indicates an error that has occurred while the command is being processed after a REQ message is received.

Table 8.24 ERROR0[15:0] Bits

Value	Error	Description
0000 0000 0000 0000	error0_no_error	No error has occurred.
Non-fatal error		
xxxx xxxx xxxx xxx1 (bit 0)	error0_ch0_command	A command that is undefined or is ineffective in the current state has been specified in Ch.0.
xxxx xxxx xxxx xx1x (bit 1)	error0_ch1_command	A command that is undefined or is ineffective in the current state has been specified in Ch.1.
xxxx xxxx xxxx x1xx (bit 2)	error0_ch0_sentence_no	An invalid sentence number has been specified in Ch.0.
xxxx xxxx xxxx 1xxx (bit 3)	error0_ch1_sentence_no	An invalid sentence number has been specified in Ch.1.
xxxx xxxx 1xxx xxxx (bit 7)	error0_sdac_overflow	An overflow has occurred in the DAC output signal.
Fatal error		
xxxx xxx1 xxxx xxxx (bit 8)	error0_ch0_decode	Invalid sound data has been read in Ch.0.
xxxx xx1x xxxx xxxx (bit 9)	error0_ch1_decode	Invalid sound data has been read in Ch.1.
xxx1 xxxx xxxx xxxx (bit 12)	error0_rom_data_mount	The sound ROM cannot be accessed.
1xxx xxxx xxxx xxxx (bit 15)	error0_others	Another error has occurred.

ERROR1

ERROR1 indicates a serial communication error that has occurred while a REQ message is being received or an error that has occurred while the flash memory is being accessed.

Table 8.25 ERROR1[15:0] Bits

Value	Error	Description
0000 0000 0000 0000	error1_no_error	No error has occurred.
Non-fatal error		
xxxx xxxx xxxx xxx1 (bit 0)	error1_message_timeout	A time out has occurred during communication.
xxxx xxxx xxxx xx1x (bit 1)	error1_extflash_not_connected	No external flash memory is connected.
xxxx xxxx xxxx x1xx (bit 2)	error1_message_invalid_id	An invalid ID has been specified in the message.
xxxx xxxx xxxx 1xxx (bit 3)	error1_message_invalid_data	An invalid data has been sent in the message.
xxxx xxxx xxx1 xxxx (bit 4)	error1_message_crc_error	A CRC error has occurred in the message.
xxxx xxxx xx1x xxxx (bit 5)	error1_message_com_error	A communication error has occurred.
xxxx xxxx x1xx xxxx (bit 6)	error1_message_buffer_overflow	A buffer overflow has occurred during communication.
xxxx xxxx 1xxx xxxx (bit 7)	error1_message_other_errors	Another error has occurred.
Fatal error		
xxxx xxx1 xxxx xxxx (bit 8)	error1_flash_erase	Erasing of the external / embedded flash memory has failed.
xxxx xx1x xxxx xxxx (bit 9)	error1_flash_write	Writing to the external / embedded flash memory has failed.
xxxx x1xx xxxx xxxx (bit 10)	error1_flash_read	Reading from the external / embedded flash memory has failed.
xxxx 1xxx xxxx xxxx (bit 11)	error1_flash_crc_error	An error has occurred in the CRC check of the external / embedded flash memory.
1xxx xxxx xxxx xxxx (bit 15)	error1_self_check_error	An abnormality has been detected in the self-check.

8.10.2 Error Clearing Method

The error that has occurred can be cleared as follows:

Non-fatal error: Issue a Non-fatal error clear by sending the ISC_RESET_REQ message.
The ERROR signal reverts to Low after receiving this message. It also clears the ERROR0 and ERROR1 bit statuses that are acquired using the ISC_STATUS_IND message.

Fatal error: Issue a Forced reset by sending the ISC_RESET_REQ message (or execute a hardware reset).
After that, redo the processing from initialization.

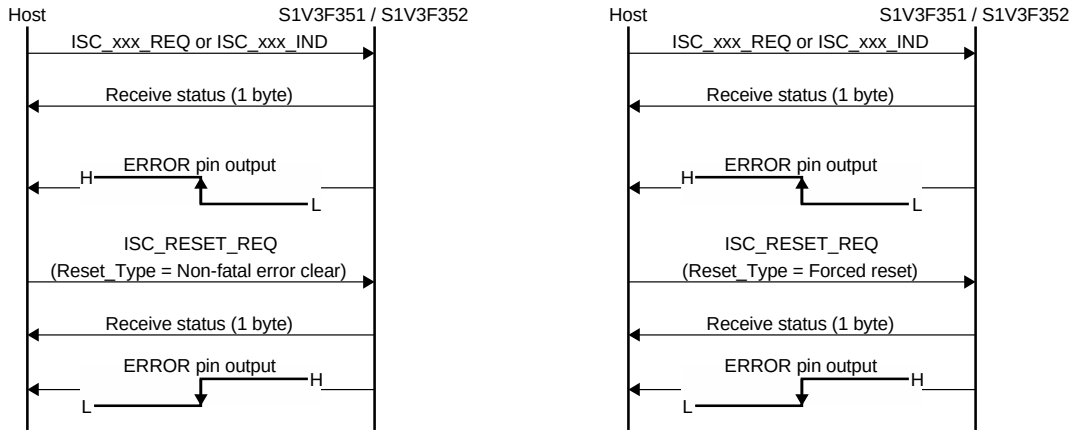


Figure 8.39 Clearing Error

8.10.3 Messages Valid When Error Occurred

After an error has occurred, this IC does not accept messages except for those shown below until the error state is canceled. When another message is received, this IC returns 0x80 (Other error) to the host as the receive status and the message will not be executed.

Messages Accepted in Error State

- All the ISC_STATUS_IND messages
- ISC_RESET_REQ message

8.11 Messages

8.11.1 List of Messages

Table 8.26 List of Messages

Message Name	Msg _ID	Operation (REQ) / Indication_Type (IND)		Description
System Control Messages				
ISC_CRC_CONFIG_REQ	0x01	–		Enables / disables CRC check.
ISC_SOUND_ROM_CONFIG_REQ	0x0B	–		Selects sound ROM and configures its address and size.
ISC_SOUND_OUTPUT_CONFIG_REQ	0x0E	–		Selects sound output destination and sampling rate.
ISC_KEYCODE_CONFIG_REQ	0x13	–		Sets keycode.
ISC_SERIAL_FLASH_CONFIG_REQ	0x15			Sets XIP parameters for external flash memory.
ISC_EXT_CIRCUIT_CONTROL_REQ	0x16			Controls external amplifier circuit.
ISC_RESET_REQ	0x99	–		Issues Non-fatal error clear / forced reset.
UART Configuration Message				
ISC_UART_CONFIG_REQ	0x02	–		Configures UART communication conditions.
Sound Playback Control Messages				
ISC_SOUND_CONTROL_CH0_REQ	0x03	–		Controls Ch.0 sound playback.
ISC_SOUND_CONTROL_CH1_REQ	0x04	–		Controls Ch.1 sound playback.
ISC_SOUND_CONTROL_CH0CH1_REQ	0x05	–		Controls Ch.0 & Ch.1 sound playback.
Sound Effect Control Messages				
ISC_VOLUME_CONFIG_REQ	0x06	–		Sets volume.
ISC_SPEED_CONFIG_REQ	0x07	–		Sets playback speed.
ISC_PITCH_CONFIG_REQ	0x08	–		Sets playback pitch.
ISC_TONE_CONFIG_REQ	0x09	–		Controls tone output.
Sound Recording Control Messages				
ISC_SOUND_RECORD_START_REQ	0x12	–		Starts recording.
ISC_SOUND_RECORD_STOP_REQ	0x00	–		Terminates recording.
ISC_SOUND_RECORD_CONFIG_REQ	0x14	–		Configures recording data area.
Sleep Control Messages				
ISC_SLEEP_ENTRY_REQ	0x0A	–		Enters Sleep / Deep Sleep mode.
ISC_SLEEP_EXIT_REQ	0xXX	–		[SPI / I²C] Returns from Sleep / Deep Sleep mode. [UART] Returns from Sleep mode.
	0x00	0x55	UART Deep Sleep Exit	[UART] Returns from Deep Sleep mode.
Self-Check Messages				
ISC_SELF_CHECK_REQ	0xF0	–		Executes self-check.
Flash Memory Control Messages				
ISC_FLASH_PROGRAM_MODE_ACTIVATE_REQ	0x0F	_		Switches between Flash Programming and Normal Operating mode.
ISC_SERIAL_FLASH_OPERATION_REQ	0x0C	0x00	Read Serial Flash ID	Reads external flash memory ID.
		0x01	Read Serial Flash Register	Reads from external flash memory registers.
		0x02	Write Serial Flash Register	Writes to external flash memory registers.
ISC_FLASH_PROGRAM_REQ	0x10	0x01	Chip Erase	Erases entire external / embedded flash memory.
		0x02	Sector Erase	Erases external / embedded flash memory sectors.
		0x03	Write Flash	Writes data to external / embedded flash memory.
		0x04	Read Flash	Reads data from external / embedded flash memory.
		0x05	CRC Check	Checks external / embedded flash memory.
		0x06	Erase Settings Area	Erases embedded flash memory setting information area.
		0x07	Write Settings Area	Writes setting information to embedded flash memory.
		0x08	Read Settings Area	Read setting information from embedded flash memory.
Status / Data Acquisition Messages				
ISC_STATUS_IND	0x0D	0x00	Error / Warning Status	Obtains error information.
		0x01	Sound Operation State	Obtains playback operation information.
		0x02	CRC Setting	Obtains CRC check setting status.
		0x03	Sound Effect Settings	Obtains sound / tone output information
		0x04	Sound ROM Settings	Obtains Sound ROM information.
		0x06	Read Serial Flash ID	Obtains external flash memory ID.
		0x07	Read Serial Flash Register	Obtains external flash memory register values.
		0x08	Sound Output State	Obtains sound playback state
ISC_FLASH_PROGRAM_STATUS_IND	0x11	0x01	Flash Read Data	Obtains flash memory read data.
		0x02	Read Settings Data	Obtains setting information in embedded flash memory.

8.11.2 REQ Messages

ISC_CRC_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x01**	**ISC_CRC_CONFIG_REQ** Enables / disables the CRC check function. For more information, refer to "*8.1.3 CRC*."
	1	CRC8_En	<0x00 or 0x01>	Bit0) CRC check enable / disable 1: Enable CRC check 0: Disable CRC check
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

ISC_UART_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x02**	**ISC_UART_CONFIG_REQ** Configures the UART data format. For more information, refer to Section "*8.2.3 UART Interface*."
	1	UART_Config[7:0]	<0x00–0x05>	UART_Config[10:0]) UART data format Bits 7–0) Baud rate 0x05: 230400 bps (*1) 0x04: 115200 bps 0x03: 57600 bps 0x02: 38400 bps 0x01: 19200 bps 0x00: 9600 bps (default) Bit 8) Stop bit length 1 = 2 bits 0 = 1 bit (default) Bit 9) Parity enable 1 = Enable parity 0 = Disable parity (default) Bit 10) Even / odd parity 1: Odd parity 0: Even parity (default)
	2	UART_Config[15:8]	<0x00–0x07>	
	3	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: Depending on the operating temperature range, the S1V3F352 cannot select this baud rate (refer to "*10.8 UART Interface Characteristics*").

ISC_SOUND_CONTROL_CH0_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x03**	**ISC_SOUND_CONTROL_CH0_REQ** Controls the sound playback of Ch.0. For more information, refer to "*Controlling Sound Playback*" in Section 8.5.3.
	1	Control_CH0	<0x00–0x09>	CH0 Playback control command 0x09: Release Mute 0x08: Mute after Current Phrase 0x07: Mute Immediately 0x03: Sound Stop after Current Phrase 0x02: Sound Stop Immediately 0x01: Sound Start Other: Setting prohibited
	2	Sentence_CH0[7:0]	<sentence[7:0]>	CH0 Sentence number to be played (*1)
	3	Sentence_CH0[15:8]	<sentence[15:8]>	
	4	Repeat_CH0	<0x00–0xFF>	CH0 Repeat count (*1) 0xFF: Repeat until Sound Stop command is executed. 0xFE: 254 times 0x7E: 253 times ... 0x02: 2 times 0x01, 0x00: 1 time (no repetition)
	5	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: The Sentence_CH0[15:0] and Repeat_CH0 values should be specified when sending the Sound Start command. Send dummy values for other playback control commands.

ISC_SOUND_CONTROL_CH1_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x03**	**ISC_SOUND_CONTROL_CH1_REQ** Controls the sound playback of Ch.1. For more information, refer to "*Controlling Sound Playback*" in Section 8.5.3.
	1	Control_CH1	<0x00–0x09>	CH1 Playback control command 0x09: Release Mute 0x08: Mute after Current Phrase 0x07: Mute Immediately 0x03: Sound Stop after Current Phrase 0x02: Sound Stop Immediately 0x01: Sound Start Other: Setting prohibited
	2	Sentence_CH1[7:0]	<sentence[7:0]>	CH1 Sentence number to be played (*1)
	3	Sentence_CH1[15:8]	<sentence[15:8]>	
	4	Repeat_CH1	<0x00–0xFF>	CH1 Repeat count (*1) 0xFF: Repeat until Sound Stop command is executed. 0xFE: 254 times 0x7E: 253 times ... 0x02: 2 times 0x01, 0x00: 1 time (no repetition)
	5	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: The Sentence_CH1[15:0] and Repeat_CH1 values should be specified when sending the Sound Start command. Send dummy values for other playback control commands.

ISC_SOUND_CONTROL_CH0CH1_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x05**	**ISC_SOUND_CONTROL_CH0CH1_REQ** Controls the simultaneous sound playback of Ch.0 and Ch.1. For more information, refer to "*Controlling Sound Playback*" in Section 8.5.3.
	1	Control_CH0CH1	<0x00–0x09>	CH0 & CH1 Playback control command 0x09: Release Mute 0x08: Mute after Current Phrase 0x07: Mute Immediately 0x03: Sound Stop after Current Phrase 0x02: Sound Stop Immediately 0x01: Sound Start Other: Setting prohibited
	2	Sentence_CH0[7:0]	<sentence[7:0]>	CH0 Sentence number to be played (*1)
	3	Sentence_CH0[15:8]	<sentence[15:8]>	
	4	Repeat_CH0	<0x00–0xFF>	CH0 Repeat count (*1) 0xFF: Repeat until Sound Stop command is executed. 0xFE: 254 times 0x7E: 253 times ... 0x02: 2 times 0x01, 0x00: 1 time (no repetition)
	5	reserved	–	–
	6	Sentence_CH1[7:0]	<sentence[7:0]>	CH1 Sentence number to be played (*1)
	7	Sentence_CH1[15:8]	<sentence[15:8]>	
	8	Repeat_CH1	<0x00–0xFF >	CH1 Repeat count (*1) (The setting values are the same as Repeat_CH0.)
	9	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: The Sentence_CHx[15:0] and Repeat_CHx values should be specified when sending the Sound Start command. Send dummy values for other playback control commands.

ISC_VOLUME_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x06**	**ISC_VOLUME_CONFIG_REQ** Specifies the sound volumes of Ch.0 and Ch.1 individually. This message can be sent regardless of whether the IC is in Idle state or Playback state.
	1	Volume_CH0	<0x00–0x7F>	CH0 / CH1 Volume 0x7F: 0 dB 0x7E: -0.5 dB 0x7D: -1.0 dB ... Can be specified in 0.5 dB steps. 0x02: -62.5 dB 0x01: -63.0 dB 0x00: Silent Other: Setting prohibited
	2	Volume_CH1	<0x00–0x7F>	
	3	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

ISC_SPEED_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x07**	**ISC_SPEED_CONFIG_REQ** Specifies the playback speed of Ch.0. (*1)
	1	Speed_CH0	<speed>	CH0 Playback speed 0x7D: 125% (*2) 0x78: 120% (*2) 0x73: 115% 0x6E: 110% 0x69: 105% 0x64: 100% 0x5F: 95% 0x5A: 90% 0x55: 85% 0x50: 80% (*2) 0x4B: 75% (*2) 0x00: Playback speed conversion disabled Other: Setting prohibited
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: The playback speed can be changed only in Ch.0 and when playback is stopped.

*2: [S1V3F351] These settings can be specified only when Pitch_Ch0 is set to 0x00 using the ISC_PITCH_CONFIG_ REQ message. (See Table 8.16.)

ISC_PITCH_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x08**	**ISC_PITCH_CONFIG_REQ** Specifies the playback pitch of Ch.0. (*1)
	1	Pitch_CH0	<pitch>	CH0 Playback pitch 0x7D 125% (*2) 0x78: 120% (*2) 0x73: 115% (*2) 0x6E: 110% 0x69: 105% 0x64: 100% 0x5F: 95% 0x5A: 90% 0x55: 85% (*2) 0x50: 80% (*2) 0x4B: 75% (*2) 0x00: Playback pitch conversion disabled Other: Setting prohibited
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: The playback pitch can be changed only in the S1V3F351 Ch.0 and when playback is stopped. This message cannot be used in the S1V3F352.

*2: These settings can be specified only when Speed_Ch0 is set to 0x00 using the ISC_SPEED_CONFIG_ REQ message. (See Table 8.16.)

ISC_TONE_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x09**	**ISC_TONE_CONFIG_REQ** Controls the tone output. For more information, refer to "*8.6 Tone Output Function*."
	1	Tone_Ctrl	<0x00–0x02>	Tone output control 0x02: Tone output forced termination 0x01: Start single tone (Tone 0) output 0x00: Start patterned tone (Tones 0–3) output
	2	Tone_Freq0[7:0]	<frequency[7:0]>	Tone 0 frequency 0x3E80: 16000 Hz 0x3E7F: 15999 Hz ... Can be specified in 1 Hz steps. 0x0020: 32 Hz 0x001F: 31 Hz Other: Invalid
	3	Tone_Freq0[15:8]	<frequency[15:8]>	
	4	Playback_Time0	<0x00–0xFF>	Tone 0 output duration (*1) 0xFF: 2550 ms 0xFE: 2540 ms ... Can be specified in 10 ms steps. 0x01: 10 ms 0x00: 0 ms
	5	Interval_Delay0	<0x00–0xFF>	Interval between Tone 0 and Tone 1 (or Tone 0) 0xFF: 2550 ms 0xFE: 2540 ms ... Can be specified in 10 ms steps. 0x01: 10 ms 0x00: 0 ms
	6	Tone_Freq1[7:0]	<frequency[7:0]>	Tone 1 frequency
	7	Tone_Freq1[15:8]	<frequency[15:8]>	(The setting values are the same as Tone_Freq0[15:0].)
	8	Playback_Time1	<0x00–0xFF>	Tone 1 output duration (*1) (The setting values are the same as Playback_Time 0.)
	9	Interval_Delay1	<0x00–0xFF>	Interval between Tone 1 and Tone 2 (or Tone 0) (The setting values are the same as Interval_Delay0.)
	10	Tone_Freq2[7:0]	<frequency[7:0]>	Tone 2frequency
	11	Tone_Freq2[15:8]	<frequency[15:8]>	(The setting values are the same as Tone_Freq0[15:0].)
	12	Playback_Time2	<0x00–0xFF>	Tone 2 output duration (*1) (The setting values are the same as Playback_Time 0.)
	13	Interval_Delay2	<0x00–0xFF>	Interval between Tone 2 and Tone 3 (or Tone 0) (The setting values are the same as Interval_Delay0.)
	14	Tone_Freq3[7:0]	<frequency[7:0]>	Tone 3 frequency
	15	Tone_Freq3[15:8]	<frequency[15:8]>	(The setting values are the same as Tone_Freq0[15:0].)
	16	Playback_Time3	<0x00–0xFF>	Tone 3 output duration (*1) (The setting values are the same as Playback_Time 0.)
	17	Interval_Delay3	<0x00–0xFF>	Interval between Tone 3 and Tone 0 (The setting values are the same as Interval_Delay0.)
	18	Tone_Repeat	<0x00–0xFF>	Tone output repeat count 0xFF: Endless output 0xFE: 254 times 0x7E: 253 times ... 0x02: 2 times 0x01, 0x00: 1 time (No repetition)
	19	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: If the specified tone output duration is 0, the settings from that tone are ignored.

ISC_SLEEP_ENTRY_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0A**	**ISC_SLEEP_ENTRY_REQ** Puts this IC into a standby mode.
	1	Mode	<0x00 or 0x01–0xFF>	Bit 0) Standby mode specification Other than 0: Deep Sleep mode 0: Sleep mode
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

ISC_SLEEP_EXIT_REQ

SPI / I^2C (Return from Sleep / Deep Sleep mode), UART (Return from Sleep mode)

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0xXX** (*1)	**ISC_SLEEP_EXIT_REQ** Returns from the standby mode.
S1V → Host	0	Receive_Status	0x0F	Response byte

*1: Any values can be used as the message ID. However, this message is effective only in a standby mode.

UART (Return from Deep Sleep mode)

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x00**	**ISC_SLEEP_EXIT_REQ**
Wait for at least 1 ms (less than 100 ms) (*1)				
Host → S1V	0	Operation	0x55	**UART Deep Sleep Exit** Returns from Deep Sleep mode when the UART interface is used.
S1V → Host	0	Receive_Status	0x0F	Response byte

*1: If the wait time exceeds 100 ms, this message becomes ineffective and this IC continues Deep Sleep mode. In this case, this IC does not return a receive status (0x0F) even if the Operation byte (0x55) is sent from the host.

ISC_SOUND_ROM_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0B**	**ISC_SOUND_ROM_CONFIG_REQ** Configures the Sound ROM.
	1	ROM_Addr[7:0]	<address[7:0]>	Sound ROM start address (*1) Embedded flash memory 0xX XX00 256-byte boundary address (0x0 0100, 0x0 0200, ...) External flash memory: 0xX0 0000 1M-byte boundary address (0x00 0000, 0x10 0000, ... 0xF0 0000)
	2	ROM_Addr[15:8]	<address[15:8]>	
	3	ROM_Addr[23:16]	<address[23:16]>	
	4	ROM_Addr[31:24]	<address[31:24]>	
	5	ROM_Size[7:0]	<size[7:0]>	Sound ROM size (in byte)
	6	ROM_Size[15:8]	<size[15:8]>	
	7	ROM_Size[23:16]	<size[23:16]>	
	8	ROM_Size[31:24]	<size[31:24]>	
	9	Flash_Select	<0x00 or 0x01>	Bit 0) Flash memory selection 1: External flash memory 0: Embedded flash memory
	10	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: An error occurs if a non-boundary address is specified.

*2: When using an external flash memory, the ISC_SERIAL_FLASH_CONFIG_REQ message must be issued before sending this message.

ISC_SOUND_OUTPUT_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0E**	**ISC_SOUND_OUTPUT_CONFIG_REQ** Configures the sound output destination and sampling rate. (*1)
	1	Sound_Out_Sel	<0x00–0x06>	Sound output selection • S1V3F351 0x07: Speaker output (mode 3) (*3) 0x06: 4-pin buzzer output (mode 3) (*2) 0x05: 2-pin buzzer output (mode 3) (*3) 0x04: 4-pin buzzer output (mode 1) (*2) 0x03: 2-pin buzzer output (mode 1) (*3) 0x02: 4-pin buzzer output (mode 2) (*2) 0x01: 2-pin buzzer output (mode 2) (*3) 0x00: Speaker output (mode 0) (*2) • S1V3F352 0x07: Speaker output (mode 3) (*3, *4) 0x01: 2-pin buzzer output (mode 1) (*3) 0x00: Speaker output (mode 0) (*2, *4)
	2	Sampling_Rate	<0x00 or 0x01>	Bit 0) Sampling rate 1: 8 kHz 0: 16 kHz
	3	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: When this message is sent, the parameters that have been previously configured by the following messages are all cleared, therefore, they must be reconfigured.
ISC_SOUND_ROM_CONFIG_REQ
ISC_VOLUME_CONFIG_REQ
ISC_SPEED_CONFIG_REQ
ISC_PITCH_CONFIG_REQ

*2: The EXT_CIRCUIT_CTRL signal goes High when turned ON; it goes Low when turned OFF.

*3: The EXT_CIRCUIT_CTRL signal goes Low when turned ON; it goes High when turned OFF.

*4: The speaker output pins (SPEAKER_OUT_P / N) are used to output the signals for sound playback, while the 2-pin buzzer output pins (BUZZER_OUT_P / N) are used to output the signals for tone output.

ISC_SOUND_RECORD_START_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x12**	**ISC_SOUND_RECORD_START_REQ** Starts a sound recording. For more information, refer to "*8.7 Sound Recording Function*."
	1	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

ISC_SOUND_RECORD_STOP_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x00**	**ISC_SOUND_RECORD_STOP_REQ** Terminates the sound recording. For more information, refer to "*8.7 Sound Recording Function*."
S1V → Host	0	Receive_Status	0x0F	Response byte

*1: This message is effective only while a sound recording is being executed.

ISC_KEYCODE_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x13**	**ISC_KEYCODE_CONFIG_REQ** Sets the keycode.
	1	Keycode[7:0]	<keycode[7:0]>	Keycode (*1)
	2	Keycode[15:8]	<keycode[15:8]>	
	3	Keycode[23:16]	<keycode[23:16]>	
	4	Keycode[31:24]	<keycode[31:24]>	
	5	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
Keycode write processing (STATUS = H)				
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return keycode writing completion notice

*1: A keycode is provided by Seiko Epson.

*2: When using this IC in Standalone mode, keycode should be set using the ISC_FLASH_PROGRAM_REQ message, not this message.

ISC_SOUND_RECORD_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x14**	**ISC_SOUND_RECORD_CONFIG_REQ** Configures the recording data area.
	1	Rec_Start_Addr[7:0]	<address[7:0]>	Recording data area start address 64K-byte boundary address in the external flash memory
	2	Rec_Start_Addr[15:8]	<address[15:8]>	
	3	Rec_Start_Addr[23:16]	<address[23:16]>	
	4	Rec_Start_Addr[31:24]	<address[31:24]>	
	5	Max_Rec_Size[7:0]	<size[7:0]>	Maximum recording data size (64K-byte units)
	6	Max_Rec_Size[15:8]	<size[15:8]>	
	7	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

ISC_SERIAL_FLASH_CONFIG_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x15**	**ISC_SERIAL_FLASH_CONFIG_REQ** Configures the mode bytes and dummy cycle length for accessing the external flash memory in XIP mode.
	1	XIP_Activate_Byte	<0x00–0xFF>	Mode byte for activating an XIP session
	2	XIP_Terminate_Byte	<0x00–0xFF>	Mode byte for terminating the XIP session
	3	XIP_Dummy_Cycles	<0x02–0x10>	Dummy cycle length (in number of clocks) 0x10: 16 clocks 0x0F: 15 clocks ... 0x03: 3 clocks 0x02: 2 clocks Other: Setting prohibited
	4	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

ISC_EXT_CIRCUIT_CONTROL_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x16**	**ISC_EXT_CIRCUIT_CONTROL_REQ** Controls the EXT_CIRCUIT_CTRL pin output to turn the external amplifier circuit for the speaker or buzzer On and Off.
	1	Control	<0x00 or 0x01>	Bit 0) External amplifier circuit control 1: On 0: Off
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

ISC_RESET_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x99**	**ISC_RESET_REQ** Issues a reset to this IC.
	1	Reset_Type	<0x00 or 0x01>	Bit 0) Reset type 1: Forced reset (same operation as hardware reset) (*1) 0: Non-fatal error clear (*2)
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: When Forced reset is executed, this IC restarts as the same as the hardware reset, therefore, all the sound processing configurations and internal circuits are initialized.

*2: When Non-fatal error clear is executed, it clears the Non-fatal error of ERROR0 or ERROR1 that has been occurred.

ISC_SELF_CHECK_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0xF0**	**ISC_SELF_CHECK_REQ** Executes the self-check. For more information, refer to "*7.5 Self-Check Function*."
	1	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
Self-check processing (STATUS = H)				
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return self-check completion notice

8.11.3 IND Messages

ISC_STATUS_IND: Error / Warning Status

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0D**	**ISC_STATUS_IND**
	1	Indication_Type	**0x00**	**Error / Warning Status** Obtains the cause of the error that has occurred. This message is used to check the cause of the error immediately after the ERROR signal goes High. For more information on error handling, refer to "*8.10 Error Handling*."
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
	1	Error0[7:0]	<error0[7:0]>	ERROR0 status (See Table 8.24.) Bit 0–Bit 7: Non-fatal error Bit 8–Bit 15: Fatal error 0x0000: No error
	2	Error0[15:8]	<error0[15:8]>	
	3	Error1[7:0]	<error1[7:0]>	ERROR1 status (See Table 8.25.) Bit 0–Bit 7: Non-fatal error Bit 8–Bit 15: Fatal error 0x0000: No error
	4	Error1[15:8]	<error1[15:8]>	

ISC_STATUS_IND: Sound Operation State

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0D**	**ISC_STATUS_IND**
	1	Indication_Type	**0x01**	**Sound Operation State** Obtains the current Ch.0 and Ch.1 operation states.
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
	1	CH0_State[7:0]	<0x0000–0x0002, 0x0004>	Ch.0 / Ch.1 operation state 0x0004: Mute state 0x0002: Playback state 0x0001: Idle state 0x0000: Initialization state
	2	CH0_State[15:8]		
	3	CH1_State[7:0]	<0x0000–0x0002, 0x0004>	
	4	CH1_State[15:8]		

ISC_STATUS_IND: CRC Setting

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0D**	**ISC_STATUS_IND**
	1	Indication_Type	**0x02**	**CRC Setting** Obtains the currently set CRC check enable / disable status.
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
	1	CRC_Setting	<CRC>	Bit 0) CRC check function setting status (Refer to "*ISC_CRC_CONFIG_REQ.*") 1: CRC check enabled 0: CRC check disabled

ISC_STATUS_IND: Sound Effect Settings

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0D**	**ISC_STATUS_IND**
	1	Indication_Type	**0x03**	**Sound Effect Settings** Obtains the current playback effect setting statuses.
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
	1	Volume_CH0	<volume>	Ch.0 Volume setting status (Refer to "*ISC_VOLUME_CONFIG_REQ.*")
	2	Volume_CH1	<volume>	Ch.1 Volume setting status (Refer to "*ISC_VOLUME_CONFIG_REQ.*")
	3	Speed_CH0	<speed>	Ch.0 Playback speed setting status (Refer to "*ISC_SPEED_CONFIG_REQ.*")
	4	Pitch_CH0	<pitch>	S1V3F351: Ch.0 Playback pitch setting status (Refer to "*ISC_PITCH_CONFIG_REQ.*") S1V3F352: Fix at 0x00.
	5	Tone_Freq[7:0]	<frequency[7:0]>	Currently / previously output tone frequency (Refer to "*ISC_TONE_CONFIG_REQ.*")
	6	Tone_Freq[15:8]	<frequency[15:8]>	
	7	Tone_On	<0x00–0x02>	Tone output status 0x01: During output 0x00: Output stopped
	8	Sound_Out_Sel	<0x00–0x06>	Sound output selection status (Refer to "*ISC_SOUND_OUTPUT_CONFIG_REQ.*") • S1V3F351 0x07: Speaker output (mode 3) 0x06: 4-pin buzzer output (mode 3) 0x05: 2-pin buzzer output (mode 3) 0x04: 4-pin buzzer output (mode 1) 0x03: 2-pin buzzer output (mode 1) 0x02: 4-pin buzzer output (mode 2) 0x01: 2-pin buzzer output (mode 2) 0x00: Speaker output (mode 0) • S1V3F352 0x07: Speaker output (mode 3) 0x01: 2-pin buzzer output (mode 1) 0x00: Speaker output (mode 0)

ISC_STATUS_IND: Sound ROM Settings

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0D**	**ISC_STATUS_IND**
	1	Indication_Type	**0x04**	**Sound ROM Settings** Obtains the sound ROM information.
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
	1	ROM_Addr[7:0]	<address[7:0]>	Sound ROM start address (Refer to "*ISC_SOUND_ROM_CONFIG_REQ*.") Embedded flash memory: 0xX XX00 256-byte boundary address External flash memory: 0xX0 0000 1M-byte boundary address
	2	ROM_Addr[15:8]	<address[15:8]>	
	3	ROM_Addr[23:16]	<address[23:16]>	
	4	ROM_Addr[31:24]	<address[31:24]>	
	5	ROM_Size[7:0]	<size[7:0]>	Sound ROM size (Refer to "*ISC_SOUND_ROM_CONFIG_REQ*.")
	6	ROM_Size[15:8]	<size[15:8]>	
	7	ROM_Size[23:16]	<size[23:16]>	
	8	ROM_Size[31:24]	<size[31:24]>	
	9	Flash_Select	<0x00 or 0x01>	Bit 0) Selected flash memory (Refer to "*ISC_SOUND_ROM_CONFIG_REQ*.") 1: External flash memory 0: Embedded flash memory

ISC_STATUS_IND: Read Serial Flash ID

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0D**	**ISC_STATUS_IND**
	1	Indication_Type	**0x06**	**Read Serial Flash ID** Obtains the external flash manufacturer ID and the device ID. (*1)
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
	1	Mmanufacturer_ID	<mfg_id> (*1)	Manufacturer ID
	2	Device_ID[7:0]	<dev_id0> (*1)	Device ID
	3	Device_ID[15:8]	<dev_id1> (*1)	

*1: This IND message transfers the information read by the ISC_SERIAL_FLASH_OPERATION_REQ: Read Flash ID message to the host.

ISC_STATUS_IND: Read Serial Flash Register

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0D**	**ISC_STATUS_IND**
	1	Indication_Type	**0x07**	**Read Serial Flash Register** Obtains the current external flash memory control register values. (*1)
	2	Num_Bytes	<N>	Number of bytes to send to the host
	3	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
	1	Reg_Velue1	<val> (*1)	Register values
	...	...	<val> (*1)	
	N	Reg_ValueM	<val> (*1)	

*1: This IND message transfers the information read by the ISC_SERIAL_FLASH_OPERATION_REQ: Read Flash Register message to the host.

ISC_STATUS_IND: Sound Output State

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0D**	**ISC_STATUS_IND**
	1	Indication_Type	**0x08**	**Sound Output State** Obtains the current sound playback operation states.
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
	1	CH0_State[7:0]	<0x0000–0x0002, 0x0004>	Ch.0 / Ch.1 operation state 0x0004: Mute state 0x0002: Playback state 0x0001: Idle state 0x0000: Initialization state
	2	CH0_State[15:8]		
	3	CH1_State[7:0]	<0x0000–0x0002, 0x0004>	
	4	CH1_State[15:8]		
	5	Tone_On	<0x00–0x01>	Tone output status 0x01: During output 0x00: Output stopped
	6	Status	<0x00–0x01>	STATUS signal status 0x01: STATUS = H 0x00: STATUS = L

8.11.4 Flash Memory Messages

External Flash Memory Dedicated Messages

ISC_SERIAL_FLASH_OPERATION_REQ: Read Serial Flash ID

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0C**	**ISC_SERIAL_FLASH_OPERATION_REQ**
	1	Operation	**0x00**	**Read Serial Flash ID** Reads the external flash manufacturer ID and the device ID. (*1)
	2	reserved	0x00	-
	3	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: To transfer the data read by this REQ message to the host, the host must send an ISC_STATUS_IND: Read Serial Flash ID message.

ISC_SERIAL_FLASH_OPERATION_REQ: Read Serial Flash Register

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0C**	**ISC_SERIAL_FLASH_OPERATION_REQ**
	1	Operation	**0x01**	**Read Serial Flash Register** Reads the external flash memory control register values. (*1)
	2	Command	<command> (*2)	Command byte for the Read Flash Register
	3	Num_Bytes	<N>	Number of bytes to read
	4	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: To transfer the data read by this REQ message to the host, the host must send an ISC_STATUS_IND: Read Serial Flash Register message.

*2: This value should be set according to the command specification of the external serial flash memory to be used.

ISC_SERIAL_FLASH_OPERATION_REQ: Write Serial Flash Register

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0C**	**ISC_SERIAL_FLASH_OPERATION_REQ**
	1	Operation	**0x02**	**Write Serial Flash Register** Writes data for the specified number of bytes to the external flash memory control registers.
	2	Command	<command> (*1)	Command byte for the Write Flash Register
	3	Num_Bytes	<N>	Number of bytes to write
	4	Reg_Value1	<write value>	Register write data byte 1
	...	...	<write value>	...
	4 + N - 1	Reg_ValueN	<write value>	Register write data byte N
	4 + N	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

*1: This value should be set according to the command specification of the external serial flash memory to be used.

Embedded / External Flash Memory Common Messages

ISC_FLASH_PROGRAM_MODE_ACTIVATE_REQ

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x0F**	**ISC_FLASH_PROGRAM_MODE_ACTIVATE_REQ** Switches between Flash Programming mode and Normal Operating mode.
	1	Active_Type	<0x00, 0x10, 0x11>	Switches Flash Programming mode. 0x11: Placing the external flash memory into programming mode 0x10: Placing the embedded flash memory into programming mode 0x00: Switching to Normal Operating mode from Flash programming mode
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status

ISC_FLASH_PROGRAM_REQ: Chip Erase

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x10**	**ISC_FLASH_PROGRAM_REQ**
	1	Operation	**0x01**	**Chip Erase** Executes a chip erase of the flash memory. Embedded flash memory The Sound ROM data area is erased. External flash memory The entire memory is erased.
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
Erase processing (STATUS = H)				
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return erasing completion notice

ISC_FLASH_PROGRAM_REQ: Sector Erase

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x10**	**ISC_FLASH_PROGRAM_REQ**
	1	Operation	**0x02**	**Sector Erase** Executes a sector erase of the flash memory. Embedded flash memory A 1K-byte area beginning with the specified sector address is erased. External flash memory A 4K-byte area beginning with the specified sector address is erased.
	2	Sector_Addr[7:0]	<address[7:0]>	Sector address Embedded flash memory 1K-byte boundary address (low-order 10 bits (address[9:0]) are ignored.) Embedded flash memory 4K-byte boundary address (low-order 12 bits (address[11:0]) are ignored.)
	3	Sector_Addr[15:8]	<address[15:8]>	
	4	Sector_Addr[23:16]	<address[23:16]>	
	5	Sector_Addr[31:24]	<address[31:24]>	
	6	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
Erase processing (STATUS = H)				
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return erasing completion notice

ISC_FLASH_PROGRAM_REQ: Write Flash

Direction	Byte No.	Field	Value	Description	
Host → S1V	0	Msg_ID	**0x10**	**ISC_FLASH_PROGRAM_REQ**	
	1	Operation	**0x03**	**Write Flash** Writes data for the specified number of bytes to the flash memory.	
	2	WR_Addr[7:0]	<address[7:0]>	Data write address 1K-byte boundary address (low-order 10 bits (address[9:0]) are ignored.)	
	3	WR_Addr[15:8]	<address[15:8]>		
	4	WR_Addr[23:16]	<address[23:16]>		
	5	WR_Addr[31:24]	<address[31:24]>		
	6	Num_Bytes[7:0]	<N[7:0]>	Number of bytes to write (Max. 1024 bytes)	
	7	Num_Bytes[15:8]	<N[15:8]>		
	8	CRC	<CRC>	CRC value	
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status	
Host → S1V	0	Data1	<write data byte>	Data byte 1	Data write processing (STATUS = H)
	...	...	<write data byte>	...	
	N - 1	DataN	<write data byte>	Data byte N	
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return data writing completion notice	

ISC_FLASH_PROGRAM_REQ: Read Flash

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x10**	**ISC_FLASH_PROGRAM_REQ**
	1	Operation	**0x04**	**Read Flash** Reads data for the specified number of bytes from the flash memory. (*1)
	2	RD_Addr[7:0]	<address[7:0]>	Data read address 1K-byte boundary address (low-order 10 bits (address[9:0]) are ignored.)
	3	RD_Addr[15:8]	<address[15:8]>	
	4	RD_Addr[23:16]	<address[23:16]>	
	5	RD_Addr[31:24]	<address[31:24]>	
	6	Num_Bytes[7:0]	<N[7:0]>	Number of bytes to read (Max. 1024 bytes)
	7	Num_Bytes[15:8]	<N[15:8]>	
	8	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
Data read processing (STATUS = H)				
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return data read completion notice

*1: To transfer the data read by this REQ message to the host, the host must send an ISC_FLASH_PROGRAM_ STATUS_IND: Flash Read Data message.

ISC_FLASH_PROGRAM_REQ: CRC Check

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x10**	**ISC_FLASH_PROGRAM_REQ**
	1	Operation	**0x05**	**CRC Check** Executes a CRC check of the flash memory. For more information, refer to "*8.8 Sound Data CRC Check Function*."
	2	Addr[7:0]	<address[7:0]>	CRC check area start address
	3	Addr[15:8]	<address[15:8]>	
	4	Addr[23:16]	<address[23:16]>	
	5	Addr[31:24]	<address[31:24]>	
	6	Num_Bytes[7:0]	<N[7:0]>	CRC check area size
	7	Num_Bytes[15:8]	<N[15:8]>	
	8	Num_Bytes[23:16]	<N[23:16]>	
	9	Num_Bytes[31:24]	<N[31:24]>	
	10	Flash_CRC	<Original CRC>	Original CRC value (CRC value obtained when the Sound ROM data was generated)
	11	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
Memory check processing (STATUS = H)				
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return memory check completion notice

ISC_FLASH_PROGRAM_REQ: Erase Settings Area

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x10**	**ISC_FLASH_PROGRAM_REQ**
	1	Operation	**0x06**	**Erase Settings Area** Erases the setting information area in the embedded flash memory. (*1)
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
Erase processing (STATUS = H)				
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return erasing completion notice

*1: This REQ message can be executed only in Embedded Flash Programming mode. An error occurs when executed in External Flash Programming mode.

ISC_FLASH_PROGRAM_REQ: Write Settings Area

Direction	Byte No.	Field	Value	Description	
Host → S1V	0	Msg_ID	**0x10**	**ISC_FLASH_PROGRAM_REQ**	
	1	Operation	**0x07**	**Write Settings Area** Writes data to the setting information area in the embedded flash memory. (*1)	
	2	CRC	<CRC>	CRC value	
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status	
Host → S1V	0	Setting_Data0	<write data byte>	Setting information byte 0	Data write processing (STATUS = H)
	...	...	<write data byte>	...	
	255	Setting_Data255	<write data byte>	Setting information byte 255	
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return data writing completion notice	

*1: This REQ message can be executed only in Embedded Flash Programming mode. An error occurs when executed in External Flash Programming mode.

ISC_FLASH_PROGRAM_REQ: Read Settings Area

Direction	Byte No.	Field	Value	Description
Host → S1V	0	Msg_ID	**0x10**	**ISC_FLASH_PROGRAM_REQ**
	1	Operation	**0x08**	**Read Settings Area** Reads data from the setting information area in the embedded flash memory. (*1, *2, *3)
	2	CRC	<CRC>	CRC value
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status
Data read processing (STATUS = H)				
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return data read completion notice

*1: To transfer the data read by this REQ message to the host, the host must send an ISC_FLASH_PROGRAM_ STATUS_ IND: Read Settings Data message.

*2: This REQ message can be executed only in Embedded Flash Programming mode. An error occurs when executed in External Flash Programming mode.

*3: The keycode cannot be read.

ISC_FLASH_PROGRAM_STATUS_IND: Flash Read Data

Direction	Byte No.	Field	Value	Description	
Host → S1V	0	Msg_ID	**0x11**	**ISC_FLASH_PROGRAM_STATUS_IND**	
	1	Indication_Type	**0x01**	**Flash Read Data** Obtains the data read from the flash memory. (*1)	
	2	Num_Bytes[7:0]	<N[7:0]>	Number of bytes to read	
	3	Num_Bytes[15:8]	<N[15:8]>		
	4	CRC	<CRC>	CRC value	
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status	
S1V → Host	0	Data1	<read data byte>	Data byte 1	Data transfer processing (STATUS = H)
	...	...	<read data byte>	...	
	N - 1	DataN	<read data byte>	Data byte N	
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return data transfer completion notice	

*1: This IND message transfers the data read by the ISC_FLASH_PROGRAM_REQ: Read Flash message to the host.

ISC_FLASH_PROGRAM_STATUS_IND: Read Settings Data

Direction	Byte No.	Field	Value	Description	
Host → S1V	0	Msg_ID	**0x11**	**ISC_FLASH_PROGRAM_STATUS_IND**	
	1	Indication_Type	**0x02**	**Read Settings Data** Obtains the data read from the setting information area in the embedded flash memory. (*1, *2, *3)	
	2	CRC	<CRC>	CRC value	
S1V → Host	0	Receive_Status	<status>	Response byte to indicate receiving status	
S1V → Host	0	Setting_Data0	<read data byte> (*2)	Setting information byte 0	Data transfer processing (STATUS = H)
	...	...	<read data byte> (*2)	...	
	255	Setting_Data255	<read data byte> (*2)	Setting information byte 255	
S1V → Host	0	2nd_Receive_Status	<status>	Response byte to return data transfer completion notice	

*1: This IND message transfers the data read by the ISC_FLASH_PROGRAM_REQ: Read Settings Area message to the host.

*2: This REQ message can be executed only in Embedded Flash Programming mode. An error occurs when executed in External Flash Programming mode.

*3: The keycode cannot be read.

9. Standalone Mode

This chapter describes the operations and control procedure in Standalone mode.

9.1 Flash Memory Selection Rule

Standalone mode determines the flash memory to be used according to the following rules:

- When an external QSPI flash memory is not connected
  - The embedded flash memory is used.
- When an external QSPI flash memory is connected
  - The external flash memory is used if the ExtSoundDataSize parameter is not 0.
  - The embedded flash memory is used if the ExtSoundDataSize parameter is 0.

9.2 Parameter Information

In Standalone mode, this IC operates according to the parameter information that has been stored in the embedded flash memory. When no parameter information exists, this IC does not operate in Standalone mode.

For creation of parameter information, refer to the "ESPER2 Simple Manual."

To write Sound ROM data to the flash memory, this IC must be placed into Host Interface mode (refer to "*8.4 Writing Sound ROM Data*").

9.2.1 List of Parameters

Table 9.1 lists the parameters.

Table 9.1 List of Parameters

Byte location	Parameter name	Byte length	Description	Configurable value / range	Remarks
0	Keycode (*1)	4	Keycode value	0–0xFFFFFFFF	–
4	ManufacturerId	4	Manufacturer ID used for checking if the parameter information exists	0x30525345	A tag to identify the presence of the parameter information
8	Reserved	8	–	-	–
16	GpioDetectionTime	1	GPIO input sampling interval	1–255	[ms]
17	Reserved	1	–	–	–
18	ExtCircuitCtrlOnTime	1	Time until a sound output starts after the EXT_CIRCUIT_CTRL signal goes ON	1–255 (N)	t = N x 10 [ms]
19	Reserved	1	–	–	–
20	ExtCircuitCtrlOffTime	2	Time until the EXT_CIRCUIT_CTRL signal goes OFF after a sound output stops	1–65535 (N)	t = N x 10 [ms]
22	StndaInSleepTimerCount	2	Timeout time of the sleep timer	1–65535	[s]
24	StndaInSoundVolumeSteps	1	Number of selectable volume levels	1–11	[level]
25	StndaInSoundSpeedSteps	1	Number of selectable playback speed levels	1–7	[level]
26	StndaInSoundPitchSteps	1	Number of selectable playback pitch levels	1–5	[level]
27	StndaInSoundVolumeDiff	1	Volume difference between Ch.0 and Ch.1 during mixing output (Ch.1 = Ch.0 - diff)	0–0x7F (N)	diff = N x 0.5 [dB]
28	StndaInDefaultVolumeLevel	1	Initial volume level after the IC starts up	0–10	[level]
29	StndaInDefaultSpeedLevel	1	Initial playback speed level after the IC starts up	0–6	[level]
30	StndaInDefaultPitchLevel	1	Initial playback pitch level after the IC starts up	0–4	[level]
31	Reserved	1	–	–	–
32	StndaInSentenceNoCh0	15	Sentence or tone pattern number assignment to each Ch.0 sentence number	0, 128: Stop playback 1–127: Sentence No. 129–131: Tone No.	x15 params
47	Reserved	1	–	–	–
48	StndaInSentenceNoCh1	15	Sentence or tone pattern number assignment to each Ch.1 sentence number	0, 128: Stop playback 1–127: Sentence No. 129–131: Tone No.	x15 params
63	Reserved	1	–	–	–
64	StndaInRepeatCountCh0	15	Playback repeat count for each Ch.0 sentence number	0x00, 0x01: 1 time 0x02–0xFE: 2–254 times 0xFF: Endless	x15 params
79	Reserved	1	–	–	–
80	StndaInRepeatCountCh1	15	Playback repeat count for each Ch.1 sentence number	0x00, 0x01: 1 time 0x02–0xFE: 2–254 times 0xFF: Endless	x15 params
95	Reserved	1	–	–	–
96	SerFlsCmdXipActivateByte	1	QSPI flash memory unique command	0–0xFF	–
97	SerFlsCmdXipTerminateByte	1	QSPI flash memory unique command	0–0xFF	–
98	SerFlsDummyCycles	1	QSPI flash memory unique command	0x02–0x10	–
99	DefaultSoundOutType	1	Sound output destination	• S1V3F351 0x00: Speaker (m0) 0x01: 2-pin buzzer (m2) 0x02: 4-pin buzzer (m2) 0x03: 2-pin buzzer (m1) 0x04: 4-pin buzzer (m1) 0x05: 2-pin buzzer (m3) 0x06: 4-pin buzzer (m3) 0x07: Speaker (m3) • S1V3F352 0x00: Speaker (m0) 0x01: 2-pin buzzer (m1) 0x07: Speaker (m3)	mX = mode X
100	DefaultSamplingRate	1	Sound sampling frequency	0: 16 kHz 1: 8 kHz	–
101	StndaInSoundVolumeLevelList	11	Volume setting value for each volume level	0–0x7F	x11 params
112	StndaInSoundSpeedLevelList	7	Speed setting value for each playback speed level	0x4B–0x7D 0x55–0x73 when using with playback pitch conversion	x7 params

Byte location	Parameter name	Byte length	Description	Configurable value / range	Remarks
119	StndaInSoundPitchLevelList	5	Pitch setting value for each playback pitch level	0x4B–0x7D 0x5A–0x6E when using with playback speed conversion	x5 params
124	IntSoundDataSize	4	Sound ROM data size in the embedded flash memory	S1V3F351: 0–0x10000 S1V3F352: 0–0x28000	[byte]
128	ExtSoundDataStartAddr	4	Sound ROM data start address in the external flash memory	0–0xF00000	[byte], 0x100000 (1 MB) steps
132	ExtSoundDataSize	4	Sound ROM data size in the external flash memory	0–0x1000000	[byte]
136	ExtFlsRecordDataStartAddr	4	Recording data area start address in the external flash memory	0–0xF00000	[byte], 0x100000 (1 MB) steps
140	ExtFlsRecordDataMaxSize	2	Maximum recording data size to store in the external flash memory	0–0xFF	x64K [byte]
142	IntSoundDataCRC	1	CRC value of the sound ROM data in the embedded flash memory	0–0xFF	–
143	ExtSoundDataCRC	1	CRC value of the sound ROM data in the external flash memory	0–0xFF	–
144	PATTERN1_TONE_FREQ0	2	Pattern 1, Tone 0 frequency	31–16000	[Hz]
146	PATTERN1_PlaybackTime0	1	Pattern 1, Tone 0 output duration	1–255 (N)	t = N x 10 [ms]
147	PATTERN1_IntervalDelay0	1	Pattern 1, Tone 0–1 (0) interval time	1–255 (N)	t = N x 10 [ms]
148	PATTERN1_TONE_FREQ1	2	Pattern 1, Tone 1 frequency	31–16000	[Hz]
150	PATTERN1_PlaybackTime1	1	Pattern 1, Tone 1 output duration	1–255 (N)	t = N x 10 [ms]
151	PATTERN1_IntervalDelay1	1	Pattern 1, Tone 1–2 (0) interval time	1–255 (N)	t = N x 10 [ms]
152	PATTERN1_TONE_FREQ2	2	Pattern 1, Tone 2 frequency	31–16000	[Hz]
154	PATTERN1_PlaybackTime2	1	Pattern 1, Tone 2 output duration	1–255 (N)	t = N x 10 [ms]
155	PATTERN1_IntervalDelay2	1	Pattern 1, Tone 2–3 (0) interval time	1–255 (N)	t = N x 10 [ms]
156	PATTERN1_TONE_FREQ3	2	Pattern 1, Tone 3 frequency	31–16000	[Hz]
158	PATTERN1_PlaybackTime3	1	Pattern 1, Tone 3 output duration	1–255 (N)	t = N x 10 [ms]
159	PATTERN1_IntervalDelay3	1	Pattern 1, Tone 3–0 interval time	1–255 (N)	t = N x 10 [ms]
160	PATTERN2_TONE_FREQ0	2	Pattern 2, Tone 0 frequency	31–16000	[Hz]
162	PATTERN2_PlaybackTime0	1	Pattern 2, Tone 0 output duration	1–255 (N)	t = N x 10 [ms]
163	PATTERN2_IntervalDelay0	1	Pattern 2, Tone 0–1 (0) interval time	1–255 (N)	t = N x 10 [ms]
164	PATTERN2_TONE_FREQ1	2	Pattern 2, Tone 1 frequency	31–16000	[Hz]
166	PATTERN2_PlaybackTime1	1	Pattern 2, Tone 1 output duration	1–255 (N)	t = N x 10 [ms]
167	PATTERN2_IntervalDelay1	1	Pattern 2, Tone 1–2 (0) interval time	1–255 (N)	t = N x 10 [ms]
168	PATTERN2_TONE_FREQ2	2	Pattern 2, Tone 2 frequency	31–16000	[Hz]
170	PATTERN2_PlaybackTime2	1	Pattern 2, Tone 2 output duration	1–255 (N)	t = N x 10 [ms]
171	PATTERN2_IntervalDelay2	1	Pattern 2, Tone 2–3 (0) interval time	1–255 (N)	t = N x 10 [ms]
172	PATTERN2_TONE_FREQ3	2	Pattern 2, Tone 3 frequency	31–16000	[Hz]
174	PATTERN2_PlaybackTime3	1	Pattern 2, Tone 3 output duration	1–255 (N)	t = N x 10 [ms]
175	PATTERN2_IntervalDelay3	1	Pattern 2, Tone 3–0 interval time	1–255 (N)	t = N x 10 [ms]
176	PATTERN3_TONE_FREQ0	2	Pattern 3, Tone 0 frequency	31–16000	[Hz]
178	PATTERN3_PlaybackTime0	1	Pattern 3, Tone 0 output duration	1–255 (N)	t = N x 10 [ms]
179	PATTERN3_IntervalDelay0	1	Pattern 3, Tone 0–1 (0) interval time	1–255 (N)	t = N x 10 [ms]
180	PATTERN3_TONE_FREQ1	2	Pattern 3, Tone 1 frequency	31–16000	[Hz]
182	PATTERN3_PlaybackTime1	1	Pattern 3, Tone 1 output duration	1–255 (N)	t = N x 10 [ms]
183	PATTERN3_IntervalDelay1	1	Pattern 3, Tone 1–2 (0) interval time	1–255 (N)	t = N x 10 [ms]
184	PATTERN3_TONE_FREQ2	2	Pattern 3, Tone 2 frequency	31–16000	[Hz]
186	PATTERN3_PlaybackTime2	1	Pattern 3, Tone 2 output duration	1–255 (N)	t = N x 10 [ms]
187	PATTERN3_IntervalDelay2	1	Pattern 3, Tone 2–3 (0) interval time	1–255 (N)	t = N x 10 [ms]
188	PATTERN3_TONE_FREQ3	2	Pattern 3, Tone 3 frequency	31–16000	[Hz]
190	PATTERN3_PlaybackTime3	1	Pattern 3, Tone 3 output duration	1–255 (N)	t = N x 10 [ms]
191	PATTERN3_IntervalDelay3	1	Pattern 3, Tone 3–0 interval time	1–255 (N)	t = N x 10 [ms]
192	Reserved[64]	64	–	–	–

*1: This parameter is used in both Host Interface mode and Standalone mode.

9.2.2 Input Pin Configuration Parameters

The following shows the parameters related to the input pins used to control Standalone mode.

GPIO Input Sampling Interval Configuration

Table 9.2 GPIO Input Sampling Interval Configuration Parameter

Parameter name	Description	Byte length	Settable value	Unit
GpioDetectionTime	GPIO input sampling interval	1	1–255	ms

This parameter is used to set the time to detect a valid input to the input pins (sampling cycle time).
For more information, refer to "*9.4 Input Signal Detection Methods*."

Sentence / Tone Pattern Number Assignment to #CHx_PLAY[3:0] Input Pins

Table 9.3 Parameters to Assign Sentence / Tone Pattern Number to #CHx_PLAY[3:0] Input Pins

Parameter name	Description	Byte length	Settable value	Unit
StndalnSentenceNoCh0[0]	Sentence or tone pattern number assignment to each Ch.0 sentence number	1	0x00–0x83	–
StndalnSentenceNoCh0[1]		1		
StndalnSentenceNoCh0[2]		1		
...		...		
StndalnSentenceNoCh0[14]		1		
StndalnSentenceNoCh1[0]	Sentence or tone pattern number assignment to each Ch.1 sentence number	1	0x00–0x83	–
StndalnSentenceNoCh1[1]		1		
StndalnSentenceNoCh1[2]		1		
...		1		
StndalnSentenceNoCh1[14]		1		

This parameter is used to configure the sentence or tone pattern that will be selected by each combination of the inputs to the #CHx_PLAY[3:0] pins (except for 0b1111).
Specify a sentence number in the Sound ROM by a number within 1 to 127, or a tone pattern 1 to 3 by a number within 129 to 131.
Sentence No. 0 (0x00) and tone pattern No. 0 (0x80) are used to stop sound playback and tone output.

Table 9.4 Sentence Number / Tone Pattern Number Specification

StndalnSentenceNoCh0/1[X]	Sentence No. / tone pattern No.
0xFF–0x84	Setting prohibited
131 (0x83)	Tone pattern 3
130 (0x82)	Tone pattern 2
129 (0x81)	Tone pattern 1
128 (0x80)	Stop playback (Tone pattern 0)
127 (0x7F)	Sentence 127
...	...
2 (0x02)	Sentence 2
1 (0x01)	Sentence 1
0 (0x00)	Stop playback (Sentence 0)

Configuration example

StndalnSentenceNoCh0[0] = 0x00:
Sound playback / tone output stops when the #CH0_PLAY[3:0] input = 0b0000.

StndalnSentenceNoCh0[1] = 0x01:
Sentence 1 in the Sound ROM is played when the #CH0_PLAY[3:0] input = 0b0001.

StndalnSentenceNoCh0[14] = 0x83:
Tone pattern 3 is output when the #CH0_PLAY[3:0] input = 0b1110.

9.2.3 Sound Playback Configuration Parameters

The following shows the parameters required for sound playback.

Sound Output Configuration

Table 9.5 Sound Output Configuration Parameter

Parameter name	Description	Byte length	Settable value	Unit
DefaultSoundOutType	Sound output destination	1	0x00–0x07	–
DefaultSamplingRate	Sound sampling frequency	1	0x00 or 0x01	–

This parameter is used to select the sound output destination and sampling frequency.

Table 9.6 Sound Output Destination Settings

DefaultSoundOutType	Sound output destination	
	S1V3F351	S1V3F352
0x07	Speaker output (mode 3) (*2)	Speaker output (mode 3) (*2, *3)
0x06	4-pin buzzer output (mode 3) (*1)	Reserved
0x05	2-pin buzzer output (mode 3) (*2)	Reserved
0x04	4-pin buzzer output (mode 1) (*1)	Reserved
0x03	2-pin buzzer output (mode 1) (*2)	Reserved
0x02	4-pin buzzer output (mode 2) (*1)	Reserved
0x01	2-pin buzzer output (mode 2) (*2)	2-pin buzzer output (mode 1) (*2)
0x00	Speaker output (mode 0) (*1)	Speaker output (mode 0) (*1, *3)

*1: The EXT_CIRCUIT_CTRL signal goes High when turned ON; it goes Low when turned OFF.

*2: The EXT_CIRCUIT_CTRL signal goes Low when turned ON; it goes High when turned OFF.

*3: The speaker output pins (SPEAKER_OUT_P / N) are used to output the signals for sound playback, while the 2-pin buzzer output pins (BUZZER_OUT_P / N) are used to output the signals for tone output.

Table 9.7 Sound Sampling Frequency Settings

DefaultSamplingRate	Sound sampling frequency
0x01	8 kHz
0x00	16 kHz

Sound Data Configuration

Table 9.8 Sound Data Configuration Parameters

Parameter name	Description	Byte length	Settable value	Unit
Keycode	Keycode	4	0–0xFFFFFFFF	–
IntSoundDataSize	Sound ROM data size in the embedded flash memory	4	S1V3F351: 0–0x10000 S1V3F352: 0–0x28000	byte
ExtSoundDataStartAddr	Sound ROM data start address in the external flash memory	4	0–0xF00000	byte
ExtSoundDataSize	Sound ROM data size in the external flash memory	4	0–0x1000000	byte
IntSoundDataCRC	CRC value of the sound ROM data in the embedded flash memory	1	0–0xFF	–
ExtSoundDataCRC	CRC value of the sound ROM data in the external flash memory	1	0–0xFF	–

These parameters are used to configure related with sound data.

Keycode is the parameter to set the customer unique code issued when the ESPER2 license was granted. For more information, please contact our sales office.

IntSoundDataSize is the parameter to set the Sound ROM data size stored in the embedded flash memory.

ExtSoundDataStartAddr and ExtSoundDataSize are the parameters to set the start address (1M-byte boundary address) and size of the Sound ROM data stored in the external flash memory. When ExtSoundDataSize is 0, the external flash memory is not used as the Sound ROM.

IntSoundDataCRC or ExtSoundDataCRC is used for the CRC check of the Sound ROM data. Set the CRC value that has been calculated from the Sound ROM data in advance.

Volume Configuration

Table 9.9 Volume Configuration Parameters

Parameter name	Description	Byte length	Settable value	Unit
StndalnSoundVolumeSteps	Number of selectable volume levels	1	1–11	level
StndalnSoundVolumeLevelList[0]	Volume setting value for each level	1	0–0x7F	dB
StndalnSoundVolumeLevelList[1]		1	0–0x7F	dB
StndalnSoundVolumeLevelList[2]		1	0–0x7F	dB
…		…	…	…
StndalnSoundVolumeLevelList[10]		1	0x00–0x7F	dB
StndalnDefaultVolumeLevel	Initial volume level after the IC starts up	1	0–10	level
StndalnSoundVolumeDiff	Volume difference (diff) between Ch.0 and Ch.1 during mixing output (Ch.1 = Ch.0 – diff x 0.5 [dB])	1	0–0x7F	dB

This IC allows setting of volume to 128 levels. In Standalone mode, up to 11 volume levels, which are configured using these parameters, can be switched using the input pins.

The StndalnSoundVolumeSteps parameter configures the number of volume levels to be used and the StndalnSound VolumeLevelList parameter assigns a volume setting value to each level.
The StndalnSoundVolumeLevelList parameter is effective from Element 0 to the element of which number is (StndalnSoundVolumeSteps - 1) and the settings exceeding this range are ignored.
The StndalnDefaultVolumeLevel parameter determines the default volume level that is initially set when this IC starts up. It should be specified by the element number of StndalnSoundVolumeLevelList.
The StndalnSoundVolumeDiff parameter sets the sound volume difference between Ch.0 and Ch.1 for mixing playback. During mixing playback, the Ch.1 playback volume is lowered by this setting value x 0.5 [dB] than the Ch.0 volume.

Table 9.10 Volume Setting Value

StndalnSoundVolumeLevelList	Volume
0xFF–0x80	Setting prohibited
0x7F	0 dB
0x7E	-0.5 dB
0x7D	-1.0 dB
…	(Can be specified in 0.5 dB steps.)
0x02	-62.5 dB
0x01	-63.0 dB
0x00	Silent

Configuration example

Number of levels: StndalnSoundVolumeSteps = 3

Volume value for each level: StndalnSoundVolumeLevelList[0] = 0x01 (Level 0 = -63.0 dB (small))
StndalnSoundVolumeLevelList[1] = 0x40 (Level 1 = -31.5 dB (medium))
StndalnSoundVolumeLevelList[2] = 0x7F (Level 2 = 0 dB (large))

Initial volume at start-up: StndalnDefaultVolumeLevel = 1 (Level 1 = -31.5 dB (medium))

Mixing output volume difference: StndalnSoundVolumeDiff = 0x14 (Ch.1 = Ch.0 - 10 dB)

Playback Speed Configuration

Table 9.11 Playback Speed Configuration Parameters

Parameter name	Description	Byte length	Settable value	Unit
StndalnSoundSpeedSteps	Number of selectable speed levels	1	1–7	level
StndalnSoundSpeedLevelList[0]	Speed setting value for each level	1	0x4B–0x7D *1	%
StndalnSoundSpeedLevelList[1]		1	0x4B–0x7D *1	%
StndalnSoundSpeedLevelList[2]		1	0x4B–0x7D *1	%
…		…	…	…
StndalnSoundSpeedLevelList[6]		1	0x4B–0x7D *1	%
StndalnDefaultSpeedLevel	Initial speed level after the IC starts up	1	0–6	level

*1: 0x55–0x73 when the playback pitch conversion function is simultaneously used (S1V3F351)

Ch.0 of this IC allows setting of playback speed to 11 levels (or 7 levels when the playback pitch conversion function is simultaneously used). In Standalone mode, up to 7 speed levels, which are configured using these parameters, can be switched using the input pins.

The StndalnSoundSpeedSteps parameter configures the number of speed levels to be used and the StndalnSound SpeedLevelList parameter assigns a speed setting value to each level.
The StndalnSoundSpeedLevelList parameter is effective from Element 0 to the element of which number is (StndalnSoundSpeedSteps - 1) and the settings exceeding this range are ignored.
The StndalnDefaultSpeedLevel parameter determines the default speed level that is initially set when this IC starts up. It should be specified by the element number of StndalnSoundSpeedLevelList.

Table 9.12 Playback Speed Settings (when the pitch conversion function is disable*) [S1V3F351, S1V3F352]

StndalnSoundSpeedLevelList	Playback speed	
0x7D	125%	Fast
0x78	120%	↑
0x73	115%	
0x6E	110%	
0x69	105%	
0x64	100%	← Standard speed
0x5F	95%	
0x5A	90%	
0x55	85%	
0x50	80%	↓
0x4B	75%	Slow
0x00	Playback speed conversion disabled	
Other	Setting prohibited	

* When the StndalnSoundPitchLevelList bytes are all 0x00 (S1V3F351)

Table 9.13 Playback Speed Settings (when the pitch conversion function is enabled*) [S1V3F351 only]

StndalnSoundSpeedLevelList	Playback speed	
0x73	115%	Fast
0x6E	110%	↑
0x69	105%	
0x64	100%	← Standard speed
0x5F	95%	
0x5A	90%	↓
0x55	85%	Slow
0x00	Playback speed conversion disabled	
Other	Setting prohibited	

* 0x5A ≦ StndalnSoundPitchLevelList ≦ 0x6E

Table 9.14 Setting Allowable Range when Converting Speed and Pitch Simultaneously [S1V3F351 only]

			StndaInSoundPitchLevelList											
			0x7D	0x78	0x73	0x6E	0x69	0x64	0x5F	0x5A	0x55	0x50	0x4B	0x00
			125%	120%	115%	110%	105%	100%	95%	90%	85%	80%	75%	–
StndaInSoundSpeedLevelList	0x7D	125%	–	–	–	–	–	–	–	–	–	–	–	OK
	0x78	120%	–	–	–	–	–	–	–	–	–	–	–	OK
	0x73	115%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x6E	110%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x69	105%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x64	100%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x5F	95%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x5A	90%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x55	85%	–	–	–	OK	OK	OK	OK	OK	–	–	–	OK
	0x50	80%	–	–	–	–	–	–	–	–	–	–	–	OK
	0x4B	75%	–	–	–	–	–	–	–	–	–	–	–	OK
	0x00	–	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK

Configuration example

- When converting the playback speed only

  Number of levels: StndaInSoundSpeedSteps = 7

  Speed value for each level: StndaInSoundSpeedLevelList[0] = 0x4B (75%)
  StndaInSoundSpeedLevelList[1] = 0x55 (85%)
  StndaInSoundSpeedLevelList[2] = 0x5F (95%)
  StndaInSoundSpeedLevelList[3] = 0x64 (100%)
  StndaInSoundSpeedLevelList[4] = 0x69 (105%)
  StndaInSoundSpeedLevelList[5] = 0x73 (115%)
  StndaInSoundSpeedLevelList[6] = 0x7D (125%)

  Initial speed at start-up: StndaInDefaultVolumeLevel = 3 (100%)

- When conversing the playback speed and pitch simultaneously (S1V3F351)

  Number of levels: StndaInSoundSpeedSteps = 7

  Speed value for each level: StndaInSoundSpeedLevelList[0] = 0x55 (85%)
  StndaInSoundSpeedLevelList[1] = 0x5A (90%)
  StndaInSoundSpeedLevelList[2] = 0x5F (95%)
  StndaInSoundSpeedLevelList[3] = 0x64 (100%)
  StndaInSoundSpeedLevelList[4] = 0x69 (105%)
  StndaInSoundSpeedLevelList[5] = 0x6E (110%)
  StndaInSoundSpeedLevelList[6] = 0x73 (115%)

  Initial speed at start-up: StndaInDefaultVolumeLevel = 3 (100%)

Playback Pitch Configuration (S1V3F351 only)

Table 9.15 Playback Pitch Configuration Parameters

Parameter name	Description	Byte length	Settable value	Unit
StndalnSoundPitchSteps	Number of selectable pitch levels	1	1–5	level
StndalnSoundPitchLevelList[0]	Pitch setting value for each level	1	0x4B–0x7D *1	%
StndalnSoundPitchLevelList[1]		1	0x4B–0x7D *1	%
StndalnSoundPitchLevelList[2]		1	0x4B–0x7D *1	%
…		…	…	…
StndalnSoundPitchLevelList[4]		1	0x4B–0x7D *1	%
StndalnDefaultPitchLevel	Initial pitch level after the IC starts up	1	0–4	level

*1: 0x5A–0x6E when the playback speed conversion function is simultaneously used

The S1V3F351 Ch.0 allows setting of playback pitch to 11 levels (or 5 levels when the playback speed conversion function is simultaneously used). In Standalone mode, up to 5 pitch levels, which are configured using these parameters, can be switched using the input pins.

The StndalnSoundPitchSteps parameter configures the number of pitch levels to be used and the StndalnSoundPitch LevelList parameter assigns a pitch setting value to each level.
The StndalnSoundPitchLevelList parameter is effective from Element 0 to the element of which number is (StndalnSoundPitchSteps - 1) and the settings exceeding this range are ignored.
The StndalnDefaultPitchLevel parameter determines the default pitch level that is initially set when this IC starts up. It should be specified by the element number of StndalnSoundPitchLevelList.

Table 9.16 Playback Pitch Settings (when the speech speed conversion function is disabled*)

StndalnSoundPitchLevelList	Pitch	
0x7D	125%	High
0x78	120%	↑
0x73	115%	
0x6E	110%	
0x69	105%	
0x64	100%	← Standard pitch
0x5F	95%	
0x5A	90%	
0x55	85%	
0x50	80%	↓
0x4B	75%	Low
0x00	Playback pitch conversion disabled	
Other	Setting prohibited	

* When the StndalnSoundSpeedLevelList bytes are all 0x00

Table 9.17 Playback Pitch Settings (when the speech speed conversion function is enabled*)

StndalnSoundPitchLevelList	Pitch	
0x6E	110%	High
0x69	105%	↑
0x64	100%	← Standard pitch
0x5F	95%	↓
0x5A	90%	Low
0x00	Playback pitch conversion disabled	
Other	Setting prohibited	

* 0x55 ≦ StndalnSoundSpeedLevelList ≦ 0x73

Configuration example

- When converting the playback pitch only

  Number of levels: StndalnSoundPitchSteps = 5

  Pitch value for each level: StndalnSoundPitchLevelList[0] = 0x55 (85%)
  StndalnSoundPitchLevelList[1] = 0x5F (95%)
  StndalnSoundPitchLevelList[2] = 0x64 (100%)
  StndalnSoundPitchLevelList[3] = 0x73 (115%)
  StndalnSoundPitchLevelList[4] = 0x7D (125%)

  Initial pitch at start-up: StndalnDefaultVolumeLevel = 2 (100%)

- When conversing the playback speed and pitch simultaneously

  Number of levels: StndalnSoundPitchSteps = 5

  Pitch value for each level: StndalnSoundPitchLevelList[0] = 0x5A (90%)
  StndalnSoundPitchLevelList[1] = 0x5F (95%)
  StndalnSoundPitchLevelList[2] = 0x64 (100%)
  StndalnSoundPitchLevelList[3] = 0x69 (105%)
  StndalnSoundPitchLevelList[4] = 0x6E (110%)

  Initial pitch at start-up: StndalnDefaultVolumeLevel = 2 (100%)

Playback Count Settings

Table 9.18 Playback Count Setting Parameters

Parameter name	Description	Byte length	Settable value	Unit
StndalnCh0RepeatCount[0]	Playback count for each sentence number / tone pattern number assigned to the #CH0_PLAY[3:0] input pins	1	0x00–0xFF	times
StndalnCh0RepeatCount[1]		1	0x00–0xFF	times
StndalnCh0RepeatCount[2]		1	0x00–0xFF	times
…		…	…	…
StndalnCh0RepeatCount[14]		1	0x00–0xFF	times
StndalnCh1RepeatCount[0]	Playback count for each sentence number / tone pattern number assigned to the #CH1_PLAY[3:0] input pins	1	0x00–0xFF	times
StndalnCh1RepeatCount[1]		1	0x00–0xFF	times
StndalnCh1RepeatCount[2]		1	0x00–0xFF	times
…		…	…	…
StndalnCh1RepeatCount[14]		1	0x00–0xFF	times

These parameters are used to set the playback count for each sentence number / tone pattern number assigned to the #CHx_PLAY[3:0] input pins.

Table 9.19 Playback Count Specification

StndalnChxRepeatCount	Playback count
0xFF	Endless playback
0xFE	254 times
0x7E	253 times
…	…
0x03	3 times
0x02	2 times
0x01, 0x00	1 time (No repetition)

External Amplifier Circuit Control Signal Configuration

Table 9.20 External Amplifier Circuit Control Signal Configuration Parameters

Parameter name	Description	Byte length	Settable value	Unit
ExtCircuitCtrlOnTime	Time until a sound output starts after the EXT_CIRCUIT_CTRL signal goes On	1	1–255 (= 10–2550 ms, 10 ms steps)	ms
ExtCircuitCtrlOffTime	Time until the EXT_CIRCUIT_CTRL signal goes Off after a sound output stops	2	1–65535 (= 10–655350 ms, 10 ms steps)	ms

These parameters are used to configure the EXT_CIRCUIT_CTRL output timing.

The ExtCircuitCtrlOnTime parameter configures the time until a sound signal output starts after the EXT_CIRCUIT_CTRL signal goes On.
The ExtCircuitCtrlOffTime parameter configures the time until the EXT_CIRCUIT_CTRL signal goes Off after the sound signal output stops.
For more information, refer to "*10.15 EXT_CIRCUIT_CTRL Output Timing*."

Specify an appropriate wait time according to the external circuit specifications.

Note: Any port inputs cannot be accepted in the period configured by ExtCircuitCtrlOnTime. Port inputs will be accepted after starting a playback.

9.2.4 Tone Generation Parameters

The following shows the parameters required for generating tone signals.

Table 9.21 Tone Generation Parameters

Parameter name	Description	Byte length	Settable value	Unit
PATTERN1_TONE_FREQ0	Pattern 1, Tone 0 frequency	2	31–16000	Hz
PATTERN1_PlaybackTime0	Pattern 1, Tone 0 output duration	1	0–255 (= 0–2550 ms, 10 ms steps)	ms
PATTERN1_IntervalDelay0	Pattern 1, Tone 0–1 interval time	1	0–255 (= 0–2550 ms, 10 ms steps)	ms
PATTERN1_TONE_FREQ1	Pattern 1, Tone 1 frequency	2	31–16000	Hz
PATTERN1_PlaybackTme1	Pattern 1, Tone 1 output duration	1	0–255 (= 0–2550 ms, 10 ms steps)	ms
PATTERN1_IntervalDelay1	Pattern 1, Tone 1–2 interval time	1	0–255 (= 0–2550 ms, 10 ms steps)	ms
PATTERN1_TONE_FREQ2	Pattern 1, Tone 2 frequency	2	31–16000	Hz
PATTERN1_PlaybackTime2	Pattern 1, Tone 2 output duration	1	0–255 (= 0–2550 ms, 10 ms steps)	ms
PATTERN1_IntervalDelay2	Pattern 1, Tone 2–3 interval time	1	0–255 (= 0–2550 ms, 10 ms steps)	ms
PATTERN1_TONE_FREQ3	Pattern 1, Tone 3 frequency	2	31–16000	Hz
PATTERN1_PlaybackTme3	Pattern 1, Tone 3 output duration	1	0–255 (= 0–2550 ms, 10 ms steps)	ms
PATTERN1_IntervalDelay3	Pattern 1, Tone 3–0 interval time	1	0–255 (= 0–2550 ms, 10 ms steps)	ms
PATTERN2_…	Pattern 2 settings (same as Pattern 1)	…	…	…
PATTERN3_...	Pattern 3 settings (same as Pattern 1)	…	…	…

These parameters are used to define tone waveforms as shown in Figure 9.1. Up to 3 patterns can be defined and they can be configured using the StndalnSentenceNoChx parameter so that they will be output by selecting with the #CHx_PLAY[3:0] pins.

Each pattern can be configured with up to 4 tones.
The PATTERNx_TONE_FREQ y parameter specifies the frequency (31 Hz to 16000 Hz) of Tone y in Pattern x. If a value out of the settable range is specified, the ERROR pin goes High.
The PATTERNx_PlaybackTime y and PATTERNx_IntervalDelay y parameters specify the Tone y output duration (0 to 2550 ms) and the interval between Tones y and z (0 to 2550 ms), respectively, in 10 ms units. If the PATTERNx_ PlaybackTime y parameter is set to 0, the settings from that tone are ignored. This makes it possible to generate a single to 3-tone waveform.

The defined tone pattern can be repeatedly output for the repeat count (1 to 254 times or endless) specified using the StndalnRepeatCountChx parameter.

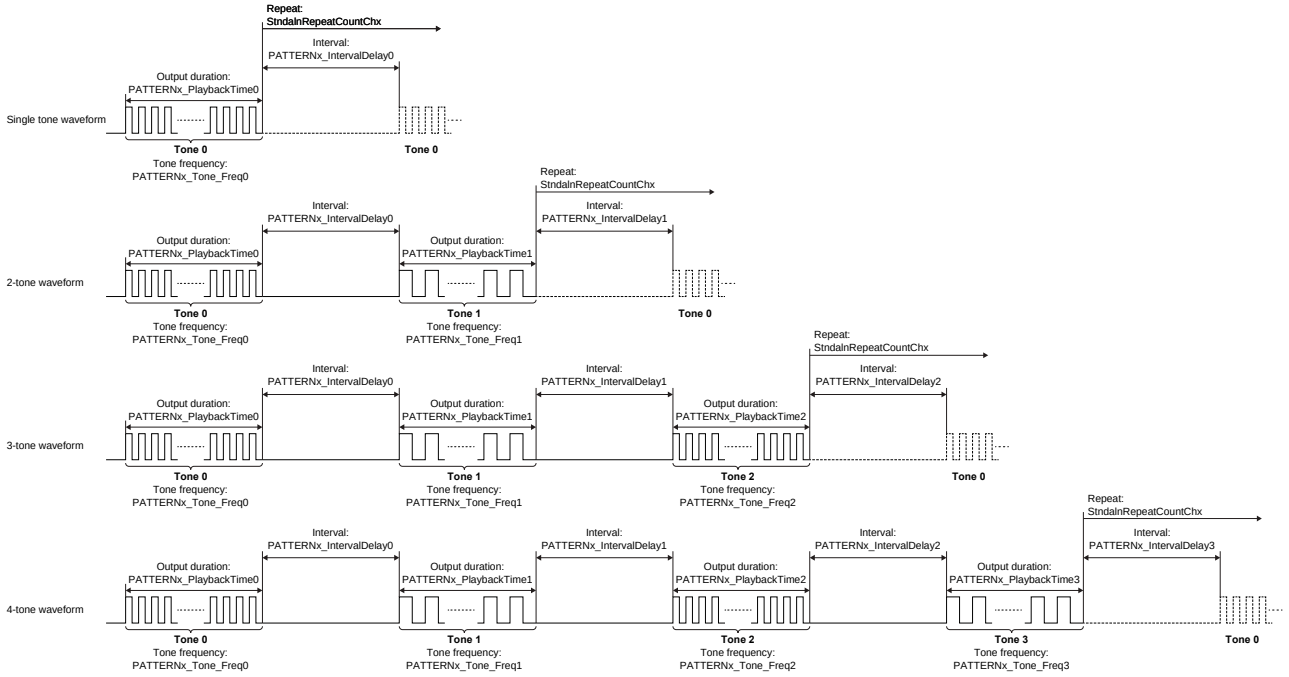


Figure 9.1 Generated Tone Waveforms

Table 9.22 Tone Frequency Setting

PATTERNx_TONE_FREQy	Tone frequency
Other	Setting prohibited
0x3E80	16000 Hz
0x3E7F	15999 Hz
…	(Can be specified in 1 Hz units)
0x0021	33 Hz
0x0020	32 Hz
0x001F	31 Hz

Table 9.23 Tone Output Duration Setting

PATTERNx_PlaybackTime y	Tone output duration
0xFF	2550 ms
0xFE	2540 ms
…	(Can be specified in 10 ms units)
0x02	20 ms
0x01	10 ms
0x00	0 ms

Table 9.24 Tone Output Interval Setting

PATTERNx_IntervalDelay y	Tone output interval
0xFF	2550 ms
0xFE	2540 ms
…	(Can be specified in 10 ms units)
0x02	20 ms
0x01	10 ms
0x00	0 ms

9.2.5 Sound Recording Configuration Parameters

The following shows the parameters required for sound recording.

Table 9.25 Sound Recording Configuration Parameters

Parameter name	Description	Byte length	Settable value	Unit
ExtFlsRecordDataStartAddr	Recording data area start address	4	0x000000–0xF00000 (0x100000 steps)	–
ExtFlsRecordDataMaxSize	Maximum recording data size	2	0x00–0xFF	x64K bytes

These parameters are used to configure the recording data area in the external flash memory. Recording data can be stored only in the external flash memory.

The ExtFlsRecordDataStartAddr parameter specifies the recording data area start address. Specify a 1M-byte boundary address (0x100000, 0x200000, ... 0xF00000).
The ExtFlsRecordDataMaxSize parameter specifies the recording area size in 64K-byte units. Specify it so that it will not exceed the external flash memory size.

9.2.6 External QSPI Flash Memory Configuration Parameters

The following shows the parameters required for accessing the external QSPI flash memory.

Table 9.26 External QSPI Flash Memory Configuration Parameters

Parameter name	Description	Byte length	Settable value	Unit
SerFlsCmdXipActivateByte	Mode byte for activating an XIP session	1	0–0xFF	–
SerFlsCmdXipTerminateByte	Mode byte for terminating the XIP session	1	0–0xFF	–
SerFlsDummyCycles	Dummy cycle length (in number of clocks)	1	0x02–0x10	–

These parameters are used to configure the QSPI interface so that it will access the external QSPI flash memory in XIP (eXecute-In-Place) mode.

Table 9.27 Dummy Cycle Length

SerFlsDummyCycles	Dummy cycle length
0x10	16 clocks
0x0F	15 clocks
...	(Specified value + 1) clocks
0x03	3 clocks
0x02	2 clocks
Other	Setting prohibited

9.2.7 Standby Mode Parameter

The following shows the parameter required for entering standby mode.

Table 9.28 Standby Mode Parameter

Parameter name	Description	Byte length	Settable value	Unit
StndalnSleepTimerCount	Timeout time of the sleep timer	2	1–65535	s

In Standalone mode, this IC automatically enters Deep Sleep mode if a control input nonexistence state continues for the time set using the StndalnSleepTimerCount parameter after this IC enters Idle mode.

9.3 Input Pins and Functions

Standalone mode detects the input pin states in the methods shown in the table below and executes the function according to the detection results.

Table 9.29 Input Pins and Functions

Function	Input pin	Input signal detection method
Ch.0 sentence selection and playback control	#CH0_PLAY[3:0]	Code detection
Ch.1 sentence selection and playback control	#CH1_PLAY[3:0]	Code detection
Playback speed control (speed up)	#SPEED_UP	Push detection
Playback speed control (speed down)	#SPEED_DOWN	Push detection
Playback pitch control (pitch up) *1	#PITCH_UP	Push detection
Playback pitch control (pitch down) *1	#PITCH_DOWN	Push detection
Volume control (volume up)	#VOLUME_UP	Push detection
Volume control (volume down)	#VOLUME_DOWN	Push detection
Sound recording control	#SOUND_REC	Long-press detection
Recorded sound playback control	#REC_SOUND_PLAY	Push detection
Standby mode control	#SLEEP_CTRL	Push detection
Self-check control	#CH1_PLAY[3:0]	Push detection

*1: S1V3F351 only

Simultaneous Port Inputs

This IC monitors the input states of all input ports listed above and performs input signal detection in parallel. Therefore, there is a possibility of detecting two or more control inputs simultaneously. Therefore, the functions have a priority to be executed. If a simultaneous input is detected, this IC executes the function having the highest priority only. However, the control input of the low-priority function is recorded and will be executed in the input order.

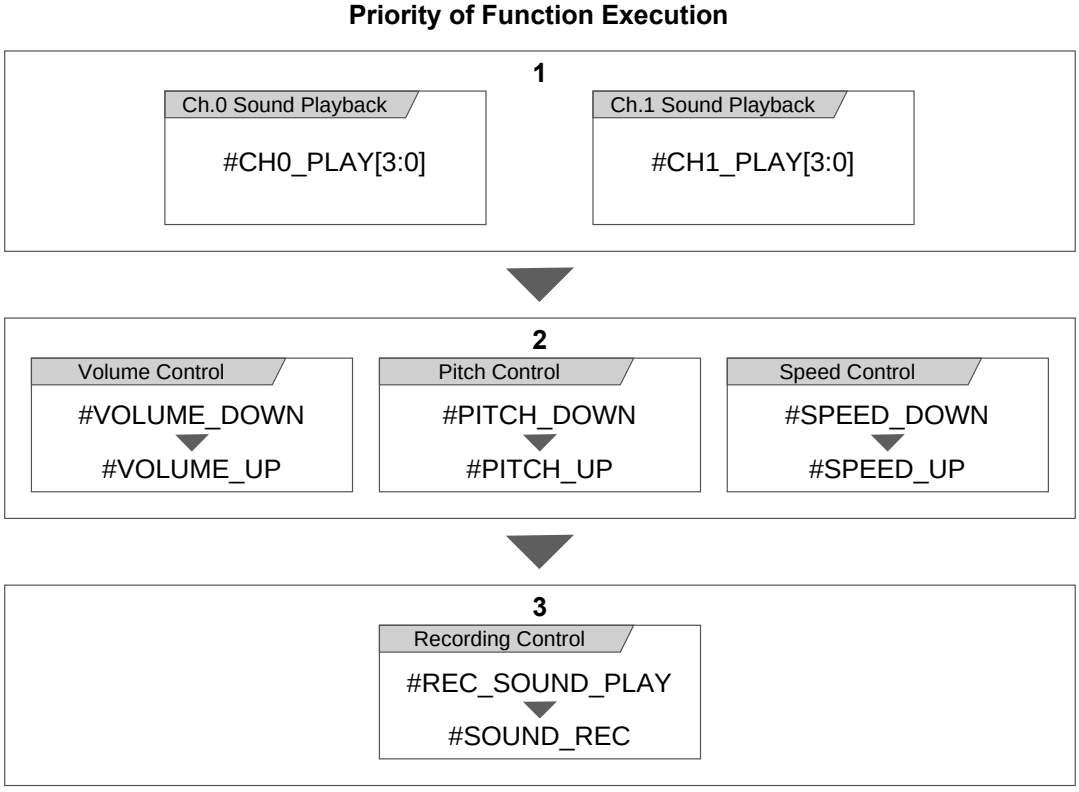


Figure 9.2 Order of Priority when Simultaneous Port Input Occurs

9.4 Input Signal Detection Methods

9.4.1 Code Detection

The #CH0_PLAY[3:0] and #CH1_PLAY[3:0] pins specify a sentence number and start playback respectively for Ch.0 and Ch.1. These inputs are sampled in the Code Detection method.

(1) Start of scan
When one or more signals input to the #CHx_PLAY[3:0] pins change from High to Low, this IC starts scanning of the #CHx_PLAY[3:0] input pins.

(2) Low input determination
When the Low level input continues for the period defined as GpioDetectionTime during scanning, this IC determines it as a valid Low input.

(2)'Input cancellation
If the input changes to a High level before the lapse of GpioDetectionTime, the input of the pin is cancelled. However, the input that has already been determined as a valid Low input is retained as valid.

(3) End of scan
When one of the inputs that has been determined as a valid Low input changes to a High level and the High input state continues for the GpioDetectionTime period, this IC terminates scanning of the #CHx_PLAY[3:0] input pins.

(3)'Input cancellation
If the input changes to a Low level before the lapse of GpioDetectionTime, this IC continues scanning until the scan end condition is established.

(4) Sampling code generation
A 4-bit code is generated from the #CHx_PLAY[3:0] input state during the scan period by assuming that a valid Low input is 0 and others are 1.

(5) Code execution
Using the generated code as the #CHx_PLAY[3:0] sentence number, this IC executes a playback of the sentence or tone that has been assigned to the sentence number in the parameter information.

GpioDetectionTime: GPIO input sampling interval defined as parameter information by the user (1 ms to 255 ms)

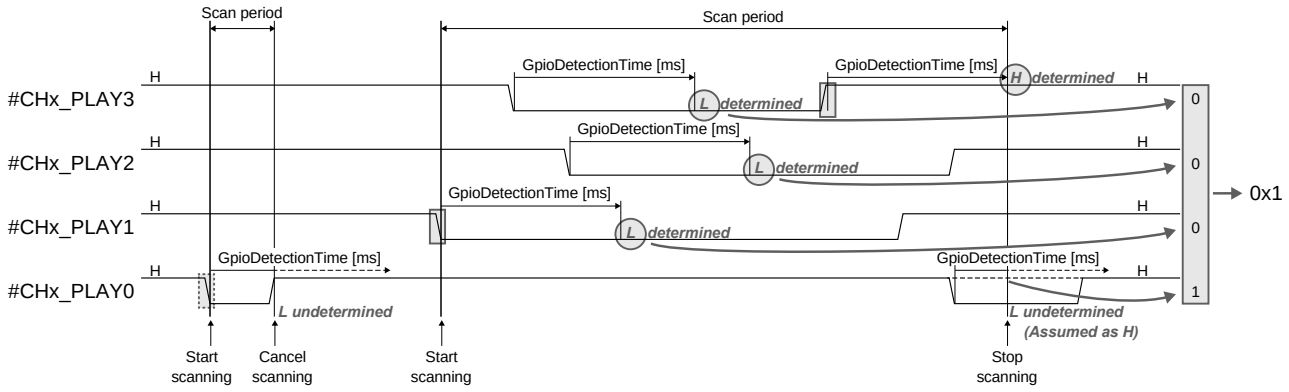


Figure 9.3 Code Detection Sequence

9.4.2 Push Detection

The #SPEED_UP / DOWN, #PITCH_UP / DOWN, #VOLUME_UP / DOWN, #REC_SOUND_PLAY, and #SLEEP_CTRL pin inputs are sampled individually in the Push Detection method.

(1) Start of scan
When one or more signals input to the pins listed above change from High to Low, this IC starts scanning of the input pins.

(2) Low input determination
When the Low level input continues for the period defined as GpioDetectionTime during scanning, this IC determines it as a valid Low input.

(2)'Input cancellation
If the input changes to a High level before the lapse of GpioDetectionTime, the input of the pin is cancelled.

(3) End of scan
When the input that has been determined as a valid Low input changes to a High level and the High input state continues for the GpioDetectionTime period, this IC terminates scanning of the input pin.

(3)'Input cancellation
If the input changes to a Low level before the lapse of GpioDetectionTime, this IC continues scanning until the scan end condition is established.

(4) Function execution
This IC executes the function according to the pin input that has been determined as a valid Low input.

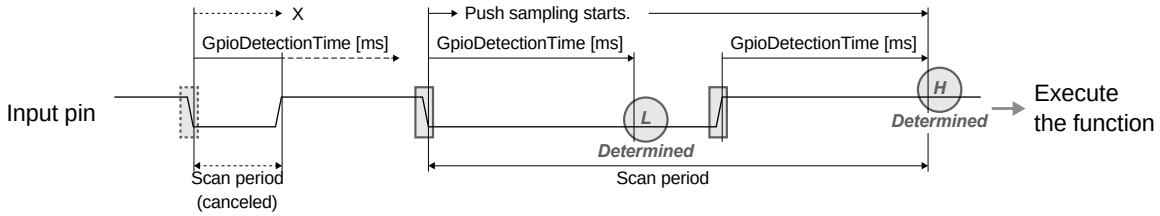


Figure 9.4 Push Detection Sequence

9.4.3 Long-Press Detection

The #SOUND_REC pin input is sampled in the Long-Press Detection method, as it is used to record voice / sound while it maintains at Low.

(1) Start of scan
When the pin input changes from High to Low, this IC starts scanning of the input pin.

(2) Low input determination (start of recording)
When the Low level input continues for the period defined as GpioDetectionTime during scanning, this IC determines it as a valid Low input and starts recording.

(2)'Input cancellation
If the input changes to a High level before the lapse of GpioDetectionTime, the pin input is cancelled.

(3) End of scan (recording termination)
When the pin input changes to a High level after the recording has started, this IC terminates scanning and recording.

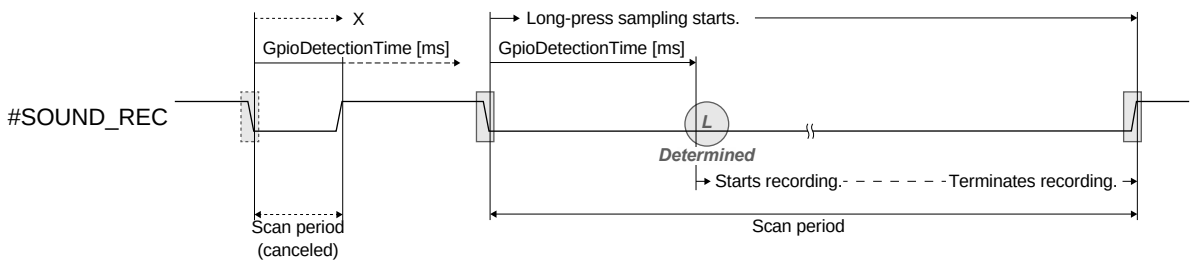


Figure 9.5 Long-Press Detection Sequence

9.5 Sound Playback Control Procedure

This section describes a sound playback procedure in Standalone mode. For the parameters required for the control, refer to "*9.2 Parameter Information*."

Starting and Terminating Sound Playback

Ch.0 starts playing when the #CH0_PLAY[3:0] pin inputs are sampled as a valid code in the Code Detection method; Ch.1 starts playing when the #CH1_PLAY[3:0] pin inputs are sampled. The sentence to be played is specified by a combination of the pin inputs at this time. This IC plays the sentence of which the sentence number has been assigned in the parameter information.

The specified sentence is played repeatedly for the repeat count defined in the parameter information and the playback stops at the end of repeated sound data.

To stop an endless playback or before reaching the repeat count, select the sentence of which the sentence number has been set to 0x00, by the #CH0_PLAY[3:0] or #CH1_PLAY[3:0] pins of the channel being currently played.

By manipulating the #CH0_PLAY[3:0] and #CH1_PLAY[3:0] pins simultaneously, sounds of Ch.0 and Ch.1 can be output by mixing.

If a new input occurs to the #CHx_PLAY[3:0] pins of the channel being currently played, the playback is switched to the top of the newly specified sentence at that point.

Changing Volume

The volume can be changed by the #VOLUME_DOWN and #VOLUME_UP pin inputs sampled in the Push Detection method regardless of whether this IC is in Idle state or Playback state.

The volume is switched one level at a time as shown below every time an active pulse is input to the #VOLUME_DOWN or #VOLUME_UP pin.

Example: When the parameters are set as follows
StndalnSoundVolumeSteps: 5 levels
StndalnDefaultVolumeLevel: Level 2

#VOLUME_DOWN: Level 2 → Level 1 → Level 0 → Level 0 ...

#VOLUME_UP: Level 2 → Level 3 → Level 4 → Level 4 ...

Changing Playback Speed (Effective only in Ch.0)

The playback speed can be changed by the #SPEED_DOWN and #SPEED_UP pin inputs sampled in the Push Detection method. However, an input during sound playback will take effect after the playback ends.

The playback speed is switched one level at a time as shown below every time an active pulse is input to the #SPEED_DOWN or #SPEED_UP pin.

Example: When the parameters are set as follows
StndalnSoundSpeedSteps: 7 levels
StndalnDefaultSpeedLevel: Level 3

#SPEED_DOWN: Level 3 → Level 2 → Level 1 → Level 0 → Level 0 ...

#SPEED_UP: Level 3 → Level 4 → Level 5 → Level 6 → Level 6 ...

Changing Playback Pitch (Effective only in S1V3F351 Ch.0)

The playback pitch can be changed by the #PITCH_DOWN and #PITCH_UP pin inputs sampled in the Push Detection method. However, an input during sound playback will take effect after the playback ends.

The playback pitch is switched one level at a time as shown below every time an active pulse is input to the #PITCH_DOWN or #PITCH_UP pin.

Example: When the parameters are set as follows
StndalnSoundPitchSteps: 5 lebels
StndalnDefaultPitchLevel: Level 2

#PITCH_DOWN: Level 2 → Level 1 → Level 0 → Level 0 ...

#PITCH_UP: Level 2 → Level 3 → Level 4 → Level 4 ...

9.6 Sound Recording Control Procedure

This section describes a sound recording procedure in Standalone mode. For the parameters required for the control, refer to "*9.2 Parameter Information*."

Starting and Terminating Sound Recording

The sound recording starts by the #SOUND_REC pin input sampled in the Long-Press method and continues while a Low level is input to the #SOUND_REC pin. The recording operation is terminated when a High level is input to the #SOUND_REC pin or the recorded data reaches the maximum recording size defined by ExtFlsRecordData MaxSize.

The recording operation status can be checked by monitoring the STATUS pin. The STATUS pin goes High when a recording starts and reverts to Low after the recording is terminated.

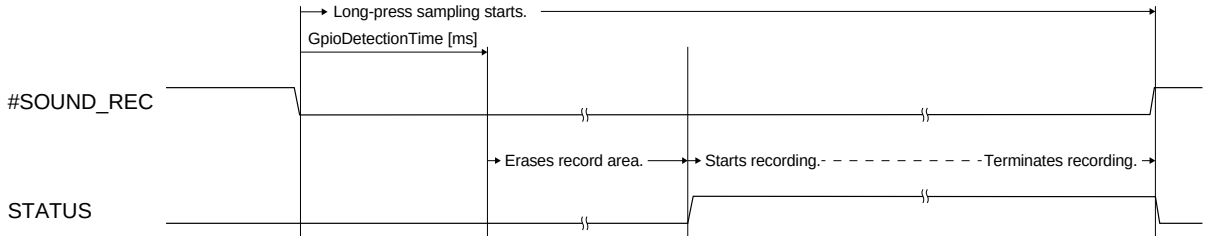


Figure 9.6 STATUS Output During Recording

Playing Recorded Sound Data

The recorded data can be played by the #REC_SOUND_PLAY pin input sampled in the Push Detection method. The playback stops when the recorded data ends.

The playback speed, pitch, and volume can be changed as described in the previous section.

When a new input to the #REC_SOUND_PLAY pin occurs during playing, the recorded data is replayed from the beginning immediately after that.

9.7 Standby Control Procedure

This section describes how to place and return the IC into/from standby mode in Standalone mode. Standalone mode supports Deep Sleep mode only.

Entering Standby Mode

There are two conditions shown below for this IC to enter Deep Sleep mode in Standalone mode.

1. When the Idle state continues for the StndalnSleepTimerCount seconds after the IC has entered the state StndalnSleepTimerCount is parameter information that can be set from 1 to 65535 seconds.
2. When the #SLEEP_CTRL pin input is changed as High → Low → High

Deep Sleep mode stops all clocks including the system clock.

When Deep Sleep mode is entered, the EXT_CIRCUIT_CTRL pin goes Off. Therefore, the external speaker amplifier or buzzer amplifier controlled with this signal also stops operating.

Returning from Standby Mode

The following shows the condition to exit Deep Sleep mode.

1. When any control input pin for Standalone mode changes High → Low

After this operation, a wait time is required until the IC enters Idle mode (input standby state). For the wait time, refer to "*10.14 Standby Mode AC Characteristics*."

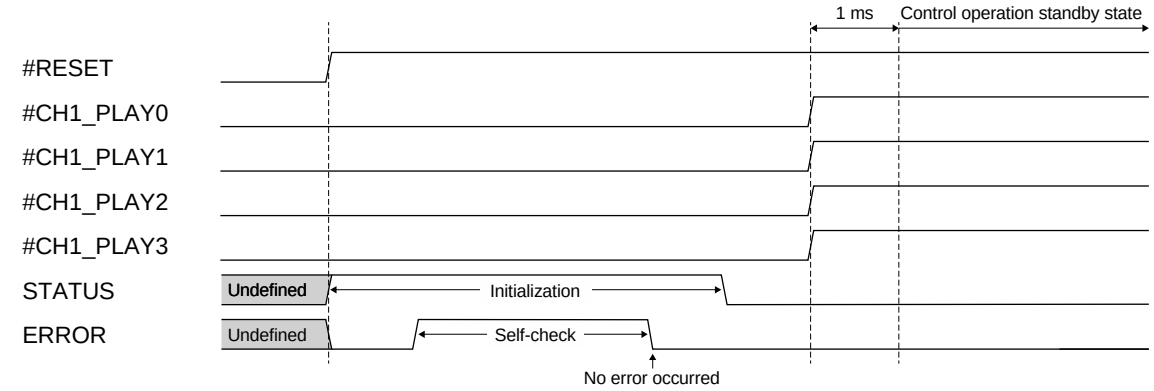
The EXT_CIRCUIT_CTRL pin does not revert to On even if the IC returns from the standby mode. It will revert On when starting a subsequent sound playback.

9.8 Self-Check Starting Procedure

This IC is equipped with a self-check function (self-check, CRC check of the embedded / external flash memory, etc.). To execute the self-check in Standalone mode, set all the four #CH1_PLAY[3:0] input pins to a Low level and turn the power On or reset this IC using the #RESET pin. To perform the CRC check of the embedded / external flash memory, the CRC value that has been calculated from the Sound ROM data must be set in the parameter information in advance.

The STATUS pin goes High during executing the self-check and reverts to Low when the self-check is finished. If an error occurs in the self-check, the ERROR pin goes High.

When no error occurred in the self-check



When an error occurred in the self-check

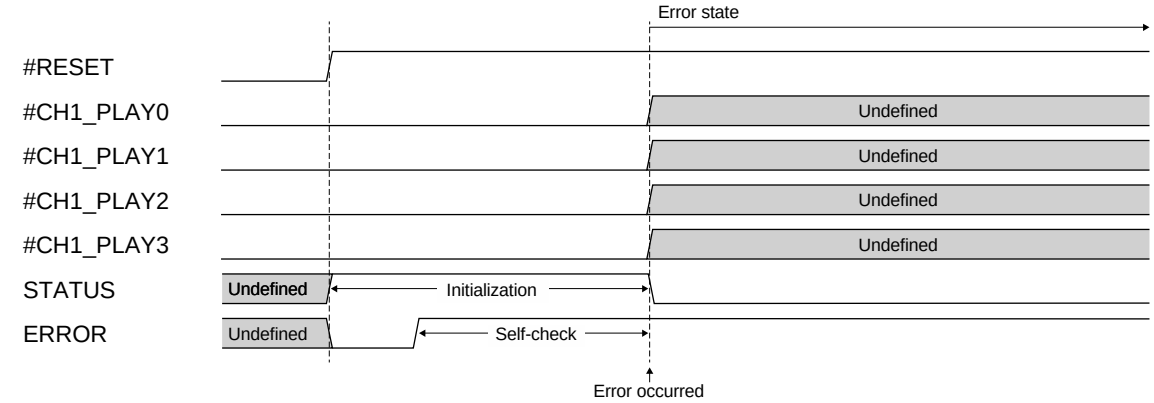


Figure 9.7 STATUS / ERROR Output During Self-Check

9.9 Error Handling

The ERROR pin goes High when an error shown below has occurred even in Standalone mode.

- Invalid sound data is read.
- Sound ROM data cannot be accessed.
- An error has occurred in the self-check.

In this case, this IC must be reset by turning the power On again after once being turned Off or setting the #RESET pin to Low.

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Table 10.1 Absolute Maximum Ratings (S1V3F351 / S1V3F352)

(V_{SS} = 0 V)

Item	Symbol	Condition	Rated value	Unit
Power supply voltage	V_{DD}		-0.3 to 7.0	V
QSPI-Flash interface power supply voltage	V_{DDQSPI}		-0.3 to 7.0	V
Flash programming voltage regulator output	V_{FLASH}		-0.3 to 8.0	V
Input voltage	V_I	#RESET, TEST, SIS / RXD / SDA / #CH0_PLAY3, SCKS / – / SCL / #CH0_PLAY2, SOS / TXD / – / #CH0_PLAY1, NSCSS / – / – / #CH0_PLAY0, V_{REF}, ADIN	-0.3 to V_{DD} + 0.5	V
		SHISEL1, SHISEL0, #CH1_PLAY3, #CH1_PLAY2, #CH1_PLAY1, #CH1_PLAY0, #SPEED_UP, #SPEED_DOWN, #PITCH_UP, # PITCH_DOWN, #VOLUME_UP, #VOLUME_DOWN, #SOUND_REC, #REC_SOUND_PLAY, OSCEN, #SLEEP_CTRL	-0.3 to 7.0	V
Output voltage	V_O		-0.3 to V_{DD} + 0.5	V
Output current	I_{OUT}	1 pin	±10	mA
Operating temperature	Ta		-40 to 85	°C
Storage temperature	Tstg		-65 to 125	°C

10.2 Recommended Operating Conditions

Table 10.2 Recommended Operating Conditions (S1V3F351)

(V_{SS} = 0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}		1.8	–	5.5	V
QSPI-Flash interface power supply voltage	V_{DDQSPI}		3	–	3.6	V
OSC oscillation frequency	fosc	Crystal / ceramic oscillator	–	16	–	MHz
Bypass capacitor between V_{SS} and V_{DD}	C_{VDD}		–	3.3	–	µF
Bypass capacitor between V_{SS} and V_{REG}	C_{VREG}		–	1	1.2	µF
Bypass capacitor between V_{SS} and V_{DDQSPI}	$C_{VDDQSPI}$		–	3.3	–	µF
Gate capacitor for OSCI oscillator input	C_G	When the crystal / ceramic oscillator is used	0	–	100	pF
Drain capacitor for OSCO oscillator output	C_D	When the crystal / ceramic oscillator is used	0	–	100	pF
Capacitor between V_{SS} and V_{FLASH}	C_{VFLASH}		–	0.1	–	µF
Capacitor between V_{SS} and V_{REF}	C_{VREF}		–	0.1	–	µF

Table 10.3 Recommended Operating Conditions (S1V3F352)

(V_{SS} = 0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}		1.8	–	5.5	V
QSPI-Flash interface power supply voltage	V_{DDQSPI}		3	–	3.6	V
OSC oscillation frequency	fosc	Crystal / ceramic oscillator	–	16	–	MHz
Bypass capacitor between V_{SS} and V_{DD}	C_{VDD}		–	3.3	–	µF
Bypass capacitor between V_{SS} and V_{REG}	C_{VREG}		–	1	1.2	µF
Bypass capacitor between V_{SS} and V_{DDQSPI}	$C_{VDDQSPI}$		–	3.3	–	µF
Gate capacitor for OSC oscillator	C_G	When the crystal / ceramic oscillator is used	0	–	100	pF
Drain capacitor for OSC oscillator	C_D	When the crystal / ceramic oscillator is used	0	–	100	pF
Capacitor between V_{SS} and V_{FLASH}	C_{VFLASH}		–	0.1	–	µF
Capacitor between V_{SS} and V_{REF}	C_{VREF}		–	0.1	–	µF

10.3 Current Consumption

Table 10.4 Current Consumption (S1V3F351)

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
In Idle state	I_{IDLE1}	Internal oscillation	–	4.6	6.9	mA
	I_{IDLE2}	Ceramic oscillation	–	3.9	5.9	mA
In Playback state *1	I_{PLAY1}	Internal oscillation	–	7.4	11.0	mA
	I_{PLAY2}	Ceramic oscillation	–	6.8	10.2	mA
In Sleep mode	I_{SLEEP}		–	410	620	µA
In Deep Sleep mode	I_{DSLEEP}		–	0.34	4.0	µA

*1: Measured by outputting full-scale white noise

Table 10.5 Current Consumption (S1V3F352)

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
In Idle state	I_{IDLE1}	Internal oscillation	–	5.8	8.7	mA
	I_{IDLE2}	Ceramic oscillation	–	5.8	8.7	mA
In Playback state *1	I_{PLAY1}	Internal oscillation	–	7.2	10.8	mA
	I_{PLAY2}	Ceramic oscillation	–	7.0	10.5	mA
In Sleep mode	I_{SLEEP}		–	490	760	µA
In Deep Sleep mode	I_{DSLEEP}		–	0.46	4.0	µA

*1: Measured by outputting full-scale white noise

10.4 Oscillator Characteristics

Table 10.6 Oscillator Characteristics (S1V3F351)

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal / ceramic oscillator oscillation start time	t_{STAC}	Crystal resonator	–	–	20	ms
		Ceramic resonator	–	–	1	ms
Internal oscillator oscillation frequency	f_{OSCII}	0°C to 85°C	15.84	16	16.16	MHz
		-40°C to 0°C	15.76	16	16.24	MHz

Table 10.7 Oscillator Characteristics (S1V3F352)

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal / ceramic oscillator oscillation start time	t_{STAC}	Crystal resonator	–	–	20	ms
		Ceramic resonator	–	–	1	ms
Internal oscillator oscillation frequency	f_{OSCII}	0°C to 50°C	15.84	16	16.32	MHz
		-20°C to 60°C	15.6	16	16.4	MHz
		-40°C to 85°C	15.44	16	16.56	MHz

10.5 Reset Characteristics

Power-On Reset Characteristics

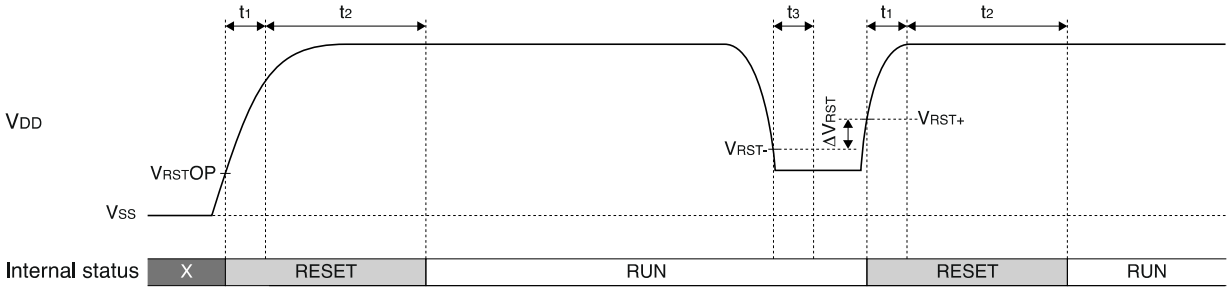


Figure 10.1 Power-On Reset Characteristics

Table 10.8 Power-On Reset Characteristics (S1V3F351)

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
t_1	Reset request hold time (time from V_{DD} rise to immediately before canceling reset request)	0.01	–	4	ms
t_2	Reset hold time	0.5	–	1.8	ms
t_3	Reset detection response time	–	–	500	µs
V_{RST+}	POR / BOR canceling voltage	–	–	1.75	V
V_{RST-}	POR / BOR detection voltage	1.05	–	1.6	V
ΔV_{RST}	POR / BOR hysteresis voltage	40	60	–	mV
V_{RSTOP}	POR / BOR operating limit voltage	–	0.5	0.95	V

POR: Power-On Reset BOR: Brown-Out Reset

Table 10.9 Power-On Reset Characteristics (S1V3F352)

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
t_1	Reset request hold time (time from V_{DD} rise to immediately before canceling reset request)	0.01	–	4	ms
t_2	Reset hold time	0.1	–	0.2	ms
t_3	Reset detection response time	–	–	20	µs
V_{RST+}	POR / BOR canceling voltage	1.41	–	1.75	V
V_{RST-}	POR / BOR detection voltage	1.25	–	1.55	V
ΔV_{RST}	POR / BOR hysteresis voltage	40	60	–	mV
V_{RSTOP}	POR / BOR operating limit voltage	–	0.5	0.95	V

POR: Power-On Reset BOR: Brown-Out Reset

#RESET Pin Characteristics

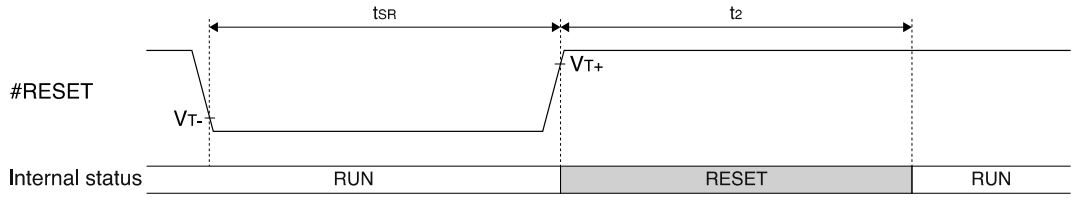


Figure 10.2 #RESET Pin Characteristics

Table 10.10 #RESET Pin Characteristics (S1V3F351)

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
V_{T+}	High level Schmitt input threshold voltage	0.5 × V_{DD}	–	0.8 × V_{DD}	V
V_{T-}	Low level Schmitt input threshold voltage	0.2 × V_{DD}	–	0.5 × V_{DD}	V
ΔV_T	Schmitt input hysteresis voltage	180	–	–	mV
R_{IN}	Input pull-up resistance	100	200	500	kΩ
C_{IN}	Pin capacitance	–	–	15	pF
t_{SR}	Reset Low pulse width	25	–	–	µs

Table 10.11 #RESET Pin Characteristics (S1V3F352)

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
V_{T+}	High level Schmitt input threshold voltage	0.5 × V_{DD}	–	0.8 × V_{DD}	V
V_{T-}	Low level Schmitt input threshold voltage	0.2 × V_{DD}	–	0.5 × V_{DD}	V
ΔV_T	Schmitt input hysteresis voltage	180	–	–	mV
R_{IN}	Input pull-up resistance	100	270	500	kΩ
C_{IN}	Pin capacitance	–	–	15	pF
t_{SR}	Reset Low pulse width	5	–	–	µs

10.6 SPI Interface AC Characteristics

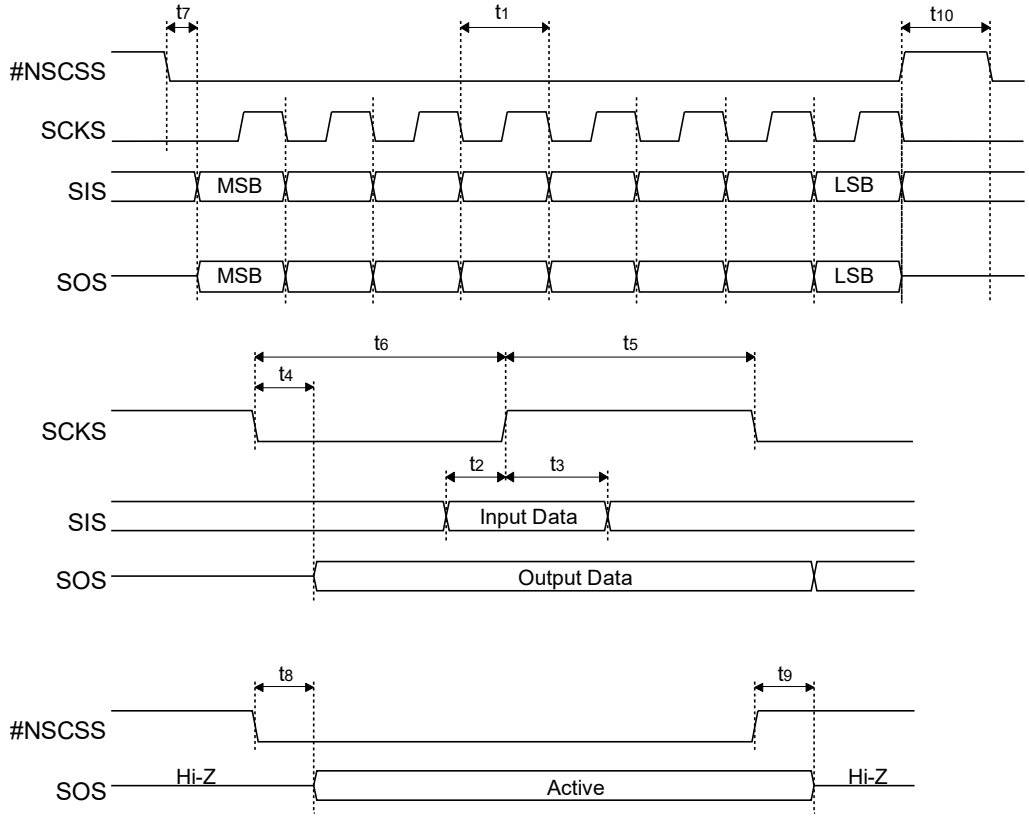


Figure 10.3 SPI Interface AC Characteristics

Table 10.12 SPI Interface AC Characteristics

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
t_1	SCKS period	250	–	–	ns
t_2	SIS setup time	20	–	–	ns
t_3	SIS hold time	25	–	–	ns
t_4	SOS output delay time (time from SCKS fall to SOS enabled)	–	–	100	ns
t_5	SCKS clock High pulse width	100	–	–	ns
t_6	SCKS clock Low pulse width	100	–	–	ns
t_7	#NSCSS setup time (time from #NSCSS fall to clock fall)	20	–	–	ns
t_8	SOS output start time	–	–	100	ns
t_9	SOS output stop time	–	–	100	ns
t_{10}	#NSCSS High pulse width	100	–	–	ns

10.7 I²C Interface AC Characteristics

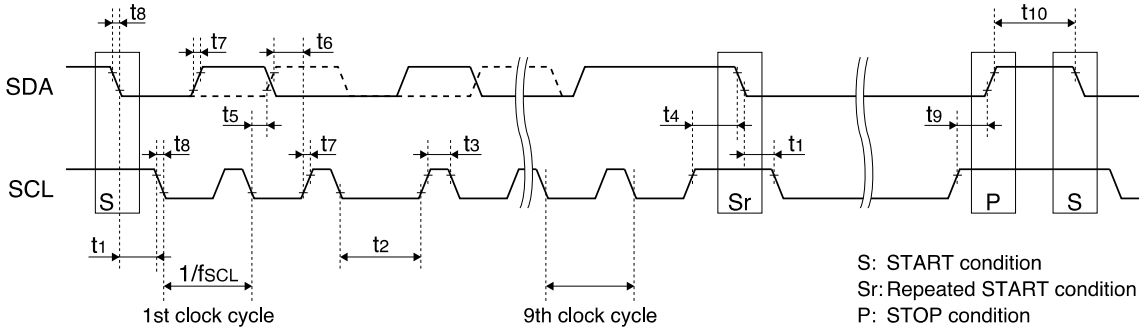


Figure 10.4 I²C Interface AC Characteristics

Table 10.13 I²C Interface AC Characteristics

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	SCL frequency	0	–	100	0	–	300	kHz
t_1	Hold time (repeated) START condition *1	4.0	–	–	0.6	–	–	µs
t_2	SCL Low pulse width	4.7	–	–	1.3	–	–	µs
t_3	SCL High pulse width	4.0	–	–	0.6	–	–	µs
t_4	Repeated START condition setup time	4.7	–	–	0.6	–	–	µs
t_5	Data hold time	0	–	–	0	–	–	µs
t_6	Data setup time	250	–	–	100	–	–	ns
t_7	SDA, SCL rise time	-	–	1000	–	–	300	ns
t_8	SDA, SCL fall time	-	–	300	–	–	300	ns
t_9	STOP condition setup time	4.0	–	–	0.6	–	–	µs
t_{10}	Bus free time	4.7	–	–	1.3	–	–	µs

*1: After this period, the first clock pulse is generated.

10.8 UART Interface Characteristics

Table 10.14 UART Interface Characteristics (S1V3F351)

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT}	Ta = -40°C to 85°C	9600	–	230400	bps

Table 10.15 UART Interface Characteristics (S1V3F352)

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT}	Ta = -40°C to 85°C	9600	–	230400	bps

10.9 QSPI Interface AC Characteristics

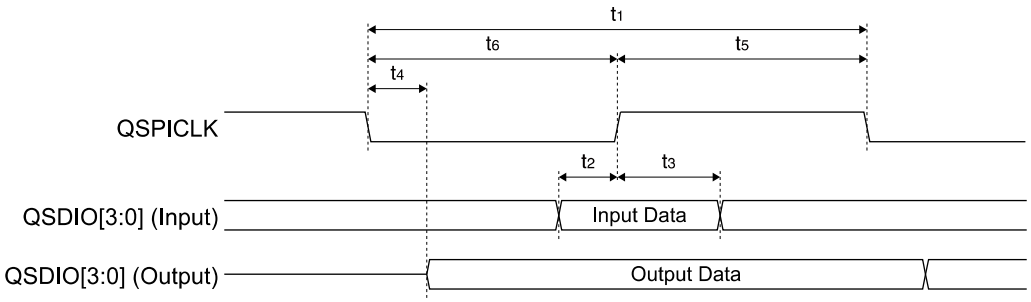


Figure 10.5 QSPI Interface AC Characteristics

Table 10.16 QSPI Interface AC Characteristics

Unless otherwise specified: V_{DDQSPI} = 3.0 V to 3.6 V , V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
t_1	QSPICLK period	125	–	–	ns
t_5	QSPICLK High pulse width	50	–	–	ns
t_6	QSPICLK Low pulse width	50	–	–	ns
t_2	QSDIOn[3:0] setup time	35	–	–	ns
t_3	QSDIOn[3:0] hold time	10	–	–	ns
t_4	QSDIOn[3:0] output delay time (time from QSPICLK fall to QSDIOn[3:0] enabled)	–	–	35	ns

10.10 Standalone Mode AC Characteristics

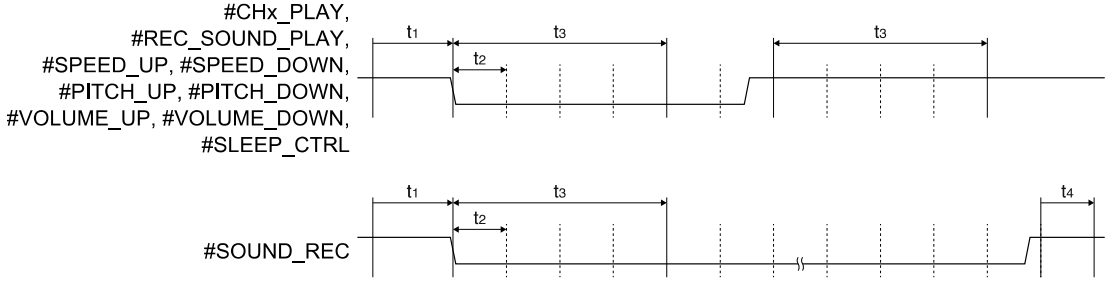


Figure 10.6 Standalone Mode AC Characteristics

Table 10.17 Standalone Mode AC Characteristics

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
t_1	Time from reset cancellation to GPIO inputs enabled (*1)	–	–	50	ms
t_2	GPIO input detection interval(*2)	–	1	–	ms
t_3	Time from GPIO input stabilized to determined as valid GPIO input value (*3)	t_2 x 1	–	t_2 x 255	ms
t_4	Time from valid GPIO input value determined to sound recording terminated or to subsequent operation enabled	1	–	3	ms

*1: When the self-check is not executed

*2: Since t2 is generated by the system clock, it includes the same error as the system clock oscillation frequency.

*3: t_3 can freely be configured (in 1 ms steps) as a user parameter.

10.11 Command Receive Timing

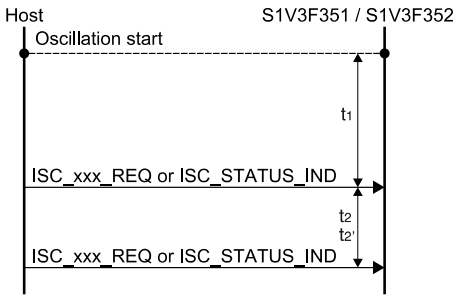


Figure 10.7 Command Receive Timing

Table 10.18 Command Receive Timing

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
t_1	Time from oscillation initiated after canceling reset to message reception enabled (*1)	–	–	50	ms
t_2	Time from message received to subsequent message reception enabled	–	–	1	ms
$t_{2'}$	Time from overwrite playback message received to subsequent message reception enabled	–	–	120	ms

*1: The t_1 and t_2 ($t_{2'}$) periods allow sending padding bytes.

10.12 ERROR Output Timing

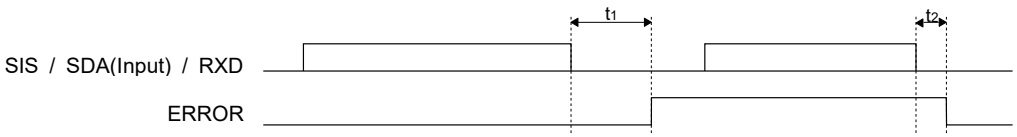


Figure 10.8 Serial Communication Error Output Timing

Table 10.19 Serial Communication Error Output Timing

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
t_1	Time from serial communication completed to ERROR output rise (*1)	–	–	100	µs
t_2	Time from error clear message received to ERROR output fall from High to Low (*2)	–	–	50	µs

*1: The ERROR signal is output when an error occurs in this IC.

*2: When an error clear message is received while the ERROR pin is outputting High, it goes Low if the error that has occurred is not a Fatal Error.

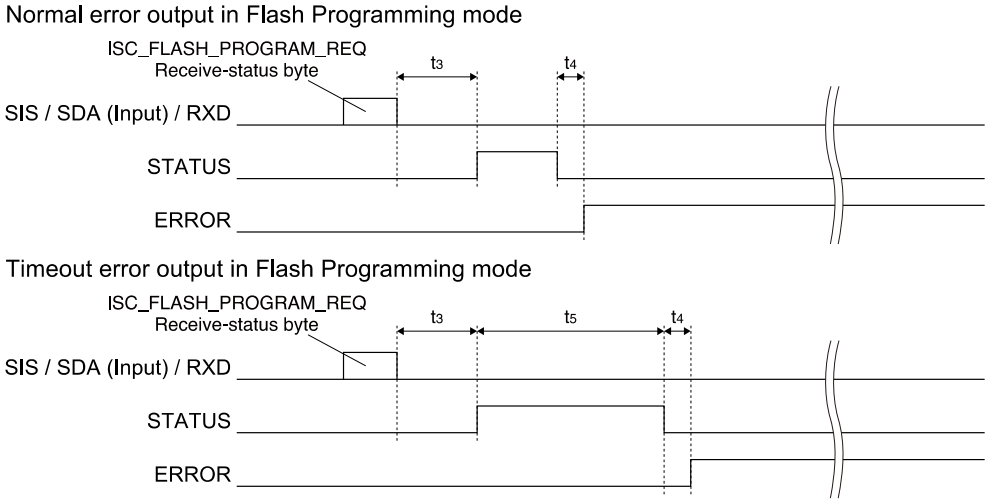


Figure 10.9 Error Output Timing in Flash Programming Mode

Table 10.20 Error Output Timing in Flash Programming Mode

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
t_3	Time from message received to STATUS rise	–	–	70	µs
t_4	Time from STATUS fall to ERROR rise	–	–	40	µs
t_5	Flash accessing timeout time	–	–	20	s

10.13 STATUS Output Timing

The STATUS output goes High in the cases below, otherwise it goes Low.

- Period after reset status has canceled until a message can be received
- During sound playback
- During recording
- During tone output
- While the internal / external flash memory is operating
- During memory check
- During self-check

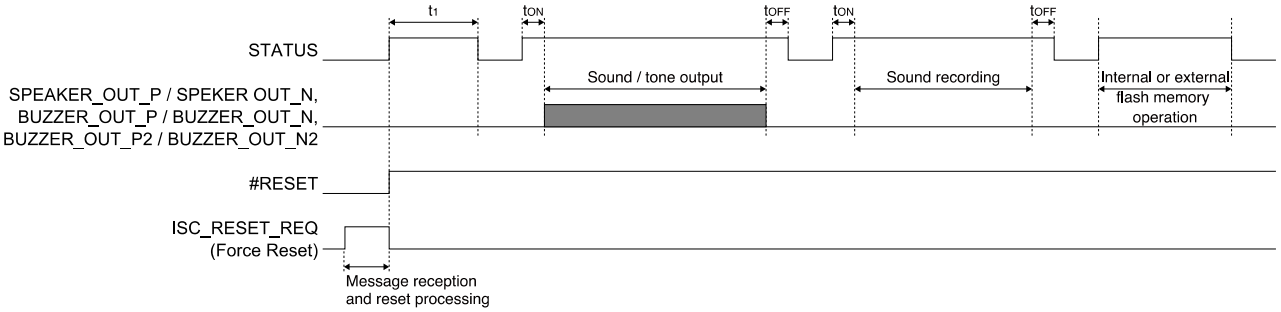


Figure 10.10 STATUS Output Timing

Table 10.21 STATUS Output Timing

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
t_1	Time from reset canceled to message reception enabled	–	–	50	ms
t_{ON}	Time from STATUS rise to sound playback started	–	–	60	ms
t_{OFF}	Time from sound playback terminated to STATUS rise	–	–	6	ms

10.14 Standby Mode AC Characteristics

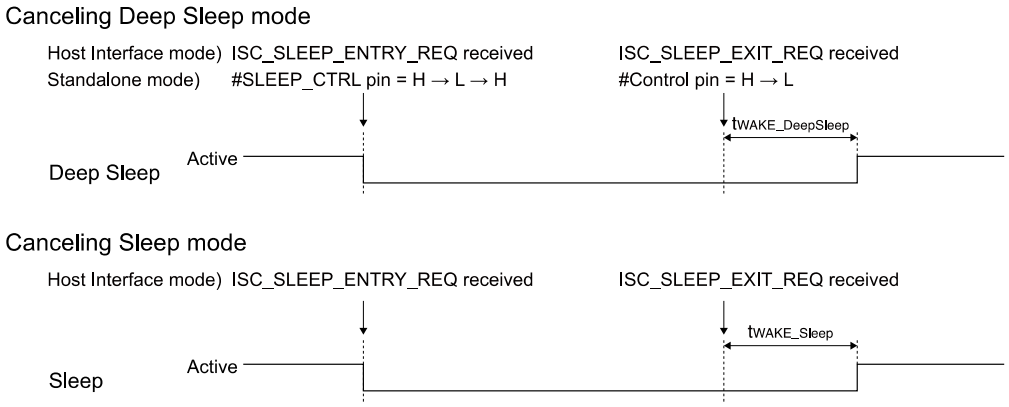


Figure 10.11 Standby Mode AC Characteristics

Table 10.22 Standby Mode AC Characteristics

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
$t_{WAKE\_DeepSleep}$	In Host Interface mode Time from ISC_SLEEP_EXIT_REQ received in Deep Sleep mode to system activated	–	–	550(*1) 200(*2)	µs
	In Standalone mode Time from a #Control pin input fall in Deep Sleep mode to system activated	–	–	510(*1) 170(*2)	µs
t_{WAKE_Sleep}	In Host Interface mode Time from ISC_SLEEP_EXIT_REQ received in Sleep mode to system activated	–	–	50(*1) 40(*2)	µs

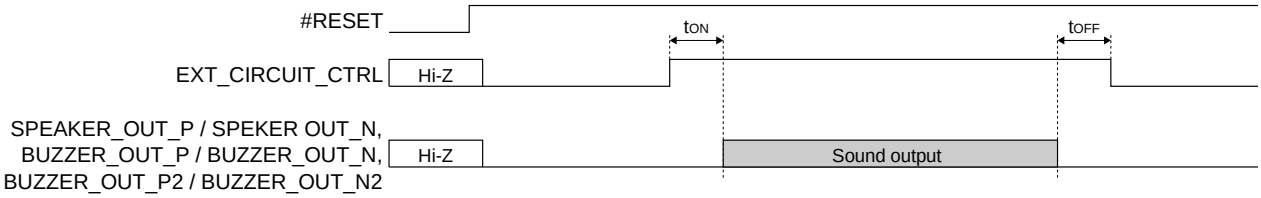
*1: For S1V3F351

*2: For S1V3F352

10.15 EXT_CIRCUIT_CTRL Output Timing

The descriptions in this section are applied to Standalone mode.

When a speaker, piezoelectric buzzer, or 4-pin electromagnetic buzzer is driven



When a 2-pin electromagnetic buzzer is driven

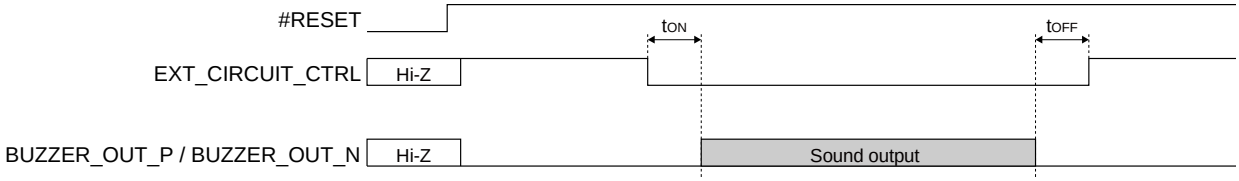


Figure 10.12 EXT_CIRCUIT_CNTL Output Timing

Table 10.23 EXT_CIRCUIT_CNTL Output Timing

Unless otherwise specified: V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, Ta = -40°C to 85°C

Symbol	Description	Min.	Typ.	Max.	Unit
t_{ON}	Time from EXT_CIRCUIT_CNTL turned On to sound output started (*1)	10	–	2550	ms
t_{OFF}	Time from sound output terminated to EXT_CIRCUIT_CNTL turned Off (*1)	10	–	655350	ms

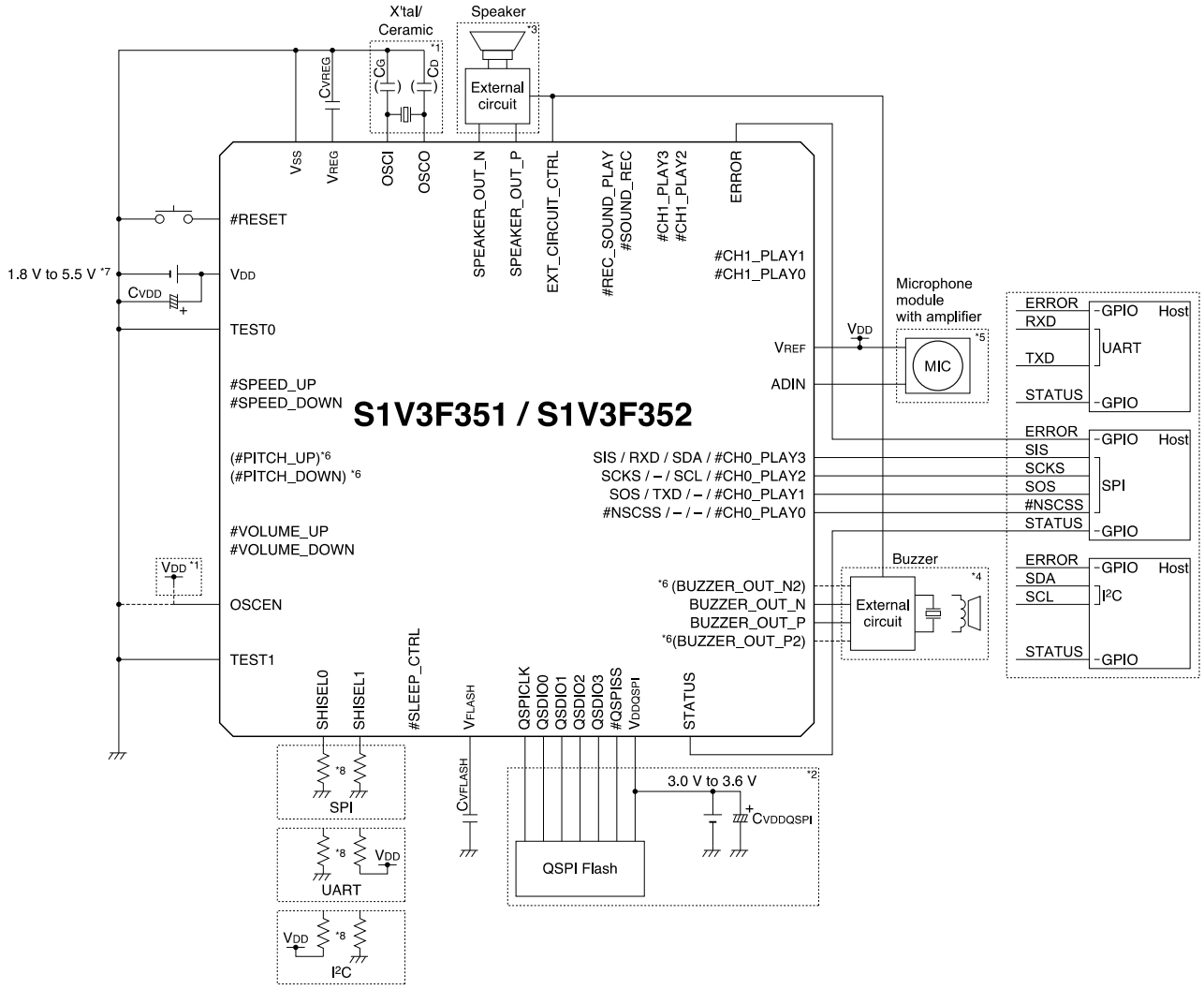
*1: t_{ON} and t_{OFF} can be specified as parameter information in 10 ms units.

*2: The EXT_CIRCUIT_CTRL output can be used to enable / disable the external speaker amplifier or to enable / disable the power supply for the external electromagnetic buzzer amplifier.

*3: When a sound playback is re-executed during the t_{OFF} period, the new sound playback starts after resetting the t_{OFF} period. If the EXT_CIRCUIT_CTRL has been already set to active, the t_{ON} count is omitted.

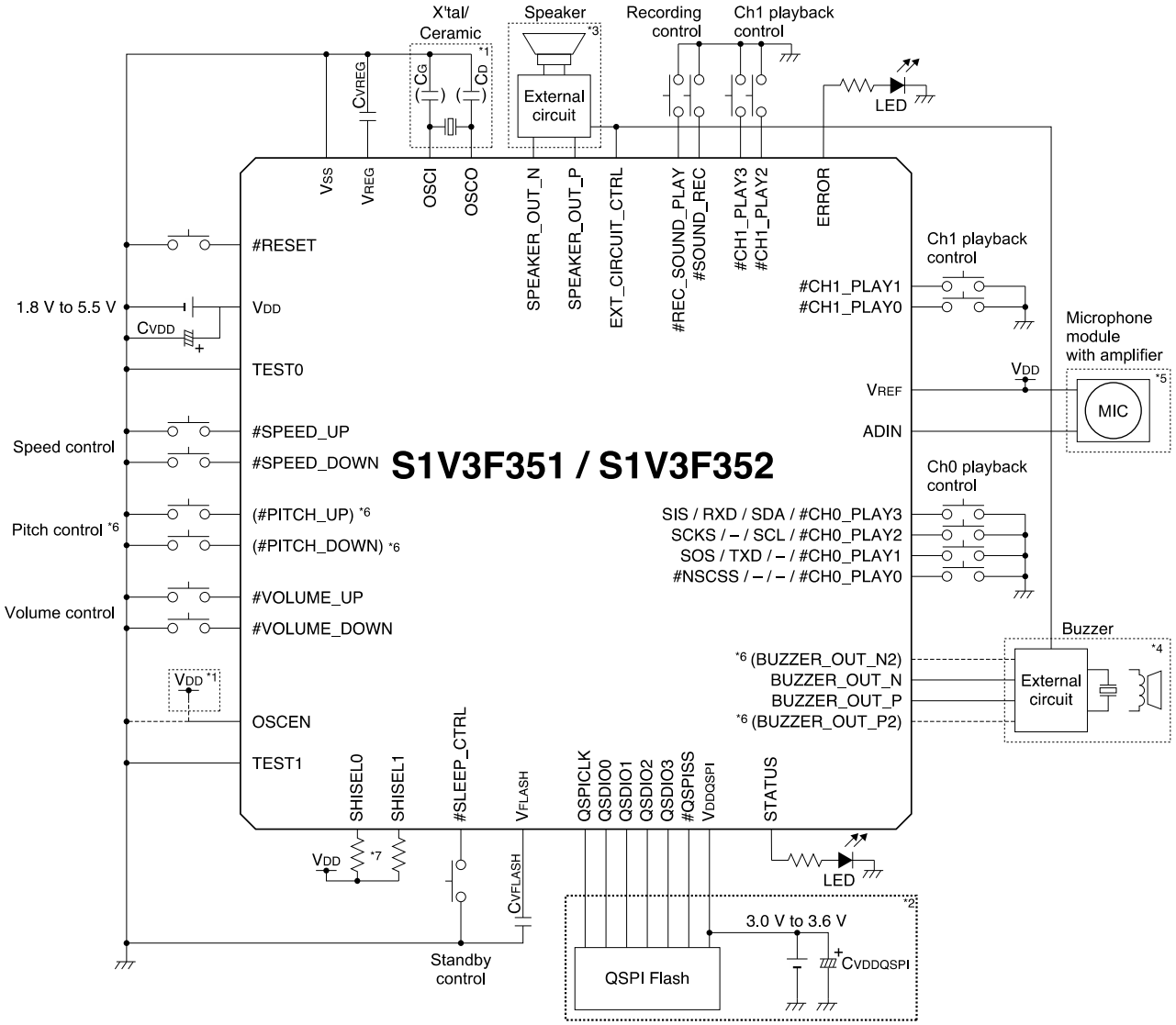
*4: Any port inputs cannot be accepted in the t_{ON} period. It will be accepted after starting a playback.

11. Basic External Connection Diagram



*1: When an external oscillation is used
*2: When an external QSPI flash memory is used (When not used, connect V_{DDQSPI} to V_{DD} and leave the other pins open.)
*3: When the speaker output is used
*4: When the buzzer output is used
*5: When a microphone input is used
*6: Available only in the S1V3F351
*7: 2.2 V to 5.5 V (S1V3F351) or 2.4 V to 5.5 V (S1V3F352) for programming the embedded flash memory
*8: It is recommended to connect Pull-up / pull-down resistors if it is necessary to switch the interface when rewriting Sound ROM data in the embedded flash memory or external QSPI flash memory.

Figure 11.1 Basic External Connection Diagram (Host Interface Mode)



*1: When an external oscillation is used
*2: When an external QSPI flash memory is used (When not used, connect V_{DDQSPI} to V_{DD} and leave the other pins open.)
*3: When the speaker output is used
*4: When the buzzer output is used
*5: When a microphone input is used
*6: Available only in the S1V3F351
*7: It is recommended to connect Pull-up / pull-down resistors (see also Figure 11.1) if it is necessary to switch the interface when rewriting Sound ROM data in the embedded flash memory or external QSPI flash memory.

Figure 11.2 Basic External Connection Diagram (Standalone Mode)

Sample External Components

Symbol	Name	Recommended components
X'tal	Crystal resonator	FA-238V (16 MHz) manufactured by Seiko Epson Corporation
Ceramic	Ceramic resonator	(16 MHz) manufactured by Murata Manufacturing Co., Ltd.
CG	OSC gate capacitor	Ceramic capacitor
CD	OSC drain capacitor	Ceramic capacitor
C_{VDD}	Bypass capacitor between V_{SS} and V_{DD}	Ceramic capacitor or electrolytic capacitor
C_{VREG}	Capacitor between V_{SS} and V_{REG}	Ceramic capacitor
$C_{VDDQSPI}$	Capacitor between V_{SS} and V_{DDQSPI}	Ceramic capacitor or electrolytic capacitor
C_{VFLASH}	Capacitor between V_{SS} and V_{FLASH}	Ceramic capacitor

* For recommended component values, refer to "*10.2 Recommended Operating Conditions*." However, the final values should be determined after evaluating operations using an actual mounting board.

12. Package Dimensions

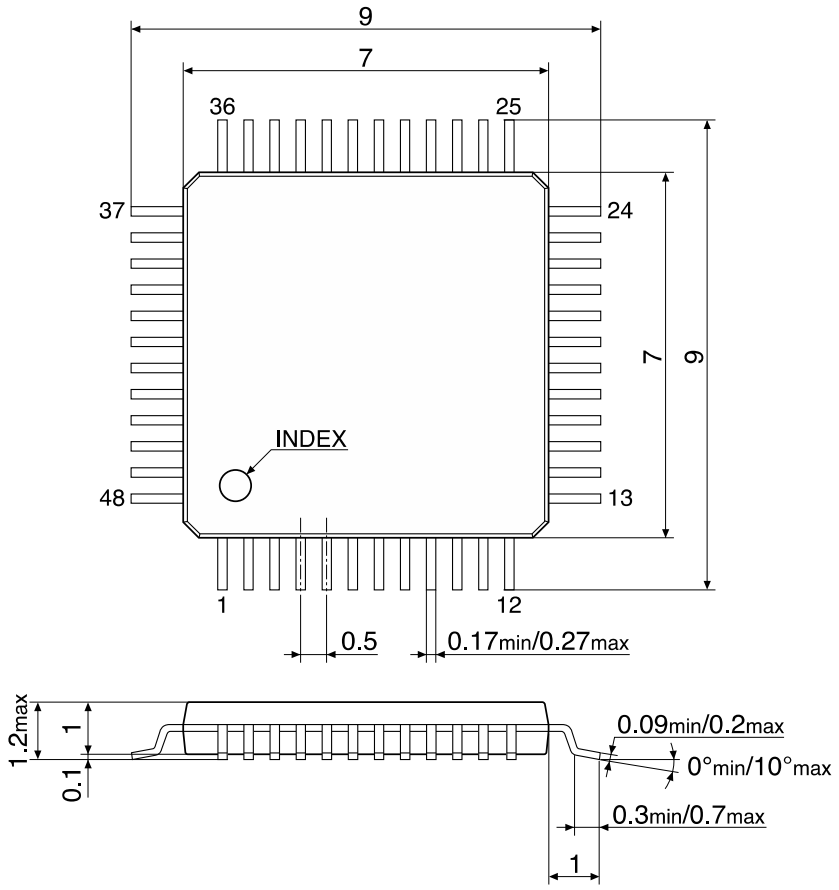


Figure 12.1 TQFP12-48PIN (P-TQFP048-0707-0.50) Package Dimensions

Appendix A. Mounting Precautions

This section describes various precautions for circuit board design and IC mounting.

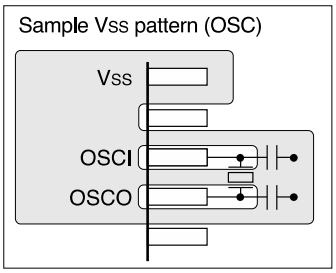
External Oscillator Circuit

- Oscillation characteristics depend on factors such as components used (resonator, C_G, C_D) and circuit board patterns. In particular, with crystal resonators, select the appropriate capacitors (C_G, C_D) only after fully evaluating components actually mounted on the circuit board.
- Oscillator clock disturbances caused by noise may cause malfunctions. To prevent such disturbances, consider the following points.

  (1) Components such as a resonator, resistors, and capacitors connected to the OSCI and OSCO pins should have the shortest connections possible.

  (2) Wherever possible, avoid locating digital signal lines within 3 mm of the OSCI and OSCO pins or related circuit components and wiring. Rapidly-switching signals, in particular, should be kept at a distance from these components. Since the spacing between layers of multi-layer printed circuit boards is a mere 0.1 mm to 0.2 mm, the above precautions also apply when positioning digital signal lines on other layers.
  Never place digital signal lines alongside such components or wiring, even if more than 3 mm distance or located on other layers. Avoid crossing wires.

  (3) Use V_{SS} to shield the OSCI and OSCO pins and related wiring (including wiring for adjacent circuit board layers). Layers wired should be adequately shielded as shown to the right. Fully ground adjacent layers, where possible. At minimum, shield the area at least 5 mm around the above pins and wiring. Even after implementing these precautions, avoid configuring digital signal lines in parallel, as described in (2) above. Avoid crossing even on discrete layers, except for lines carrying signals with low switching frequencies.



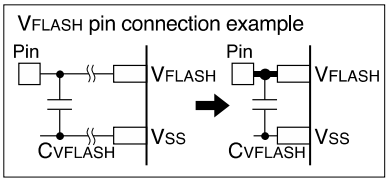
  Failure to observe precautions (1) to (3) adequately may lead to jitter in the clock output. Jitter in the clock output will reduce operating frequencies.

#RESET Pin

Components such as a switch and resistor connected to the #RESET pin should have the shortest connections possible to prevent noise-induced resets.

V_{FLASH} Pin

Connect a capacitor C_{VFLASH} between the V_{SS} and V_{FLASH} pins to suppress fluctuations within $V_{FLASH} \pm 1$ V. The C_{VFLASH} should be placed as close to the V_{FLASH} pin as possible and use a sufficiently thick wiring pattern that allows current of several tens of mA to flow.

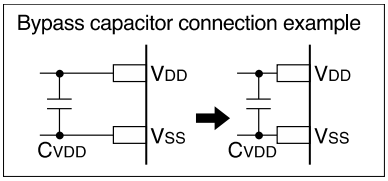


Power Supply Circuit

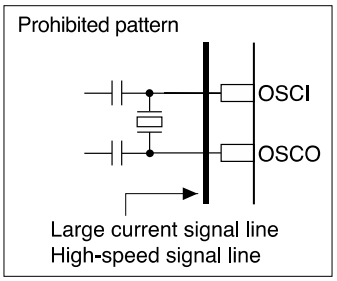
Sudden power supply fluctuations due to noise will cause malfunctions. Consider the following issues.

(1) Connections from the power supply to the V_{DD} and V_{SS} pins should be implemented via the shortest, thickest patterns possible.

(2) If a bypass capacitor is connected between V_{DD} and V_{SS}, connections between the V_{DD} and V_{SS} pins should be as short as possible.



Signal Line Location



- To prevent electromagnetically-induced noise arising from mutual induction, large-current signal lines should not be positioned close to pins susceptible to noise, such as oscillator and analog measurement pins.
- Locating signal lines in parallel over significant distances or crossing signal lines operating at high speed will cause malfunctions due to noise generated by mutual interference.

Unused Pins

(1) Input / Output Port Pins
Unused pins should be left open.

(2) OSCI and OSCO pins
If the crystal / ceramic oscillator circuit is not used, the OSCI and OSCO pins should be left open.

Miscellaneous

Minor variations over time may result in electrical damage arising from disturbances in the form of voltages exceeding the absolute maximum rating when mounting the product in addition to physical damage. The following factors can give rise to these variations:

(1) Electromagnetically-induced noise from industrial power supplies used in mounting reflow, reworking after mounting, and individual characteristic evaluation (testing) processes

(2) Electromagnetically-induced noise from a solder iron when soldering

In particular, during soldering, take care to ensure that the soldering iron GND (tip potential) has the same potential as the IC GND.

Appendix B. Measures Against Noise

To improve noise immunity, take measures against noise as follows:

Noise Measures for V_{DD}, V_{DDQSPI}, and V_{SS} Power Supply Pins

When noise falling below the rated voltage is input, an IC malfunction may occur. If desired operations cannot be achieved, take measures against noise on the circuit board, such as designing close patterns for circuit board power supply circuits, adding noise-filtering decoupling capacitors, and adding surge/noise prevention components on the power supply line.
For the recommended patterns on the circuit board, refer to *Appendix A*, "*Mounting Precautions*."

Noise Measures for #RESET Pin

If noise is input to the #RESET pin, the IC may be reset. Therefore, the circuit board must be designed properly taking noise measures into consideration.
For the recommended patterns on the circuit board, refer to *Appendix A*, "*Mounting Precautions*."

Noise Measures for Oscillator Pins

The oscillator input pins must pass a signal of small amplitude, so they are hypersensitive to noise. Therefore, the circuit board must be designed properly taking noise measures into consideration.
For the recommended patterns on the circuit board, refer to *Appendix A*, "*Mounting Precautions*."

Noise Measures for UART Pins

This product includes a UART for asynchronous communications. The UART starts receive operation when it detects a low level input from the RXD pin. Therefore, a receive operation may be started if the RXD pin is set to low due to extraneous noise. In this case, a receive error may occur or invalid data may be received.
To prevent the UART from malfunction caused by extraneous noise, take the following measure:

- Execute the resending process via software after executing the receive error handler with a parity check.

Noise Measures for Input Pins Connected to Signal with High Driving Capability Such As Power Supply

There is a possibility of a large current flow into the pins that are directly connected to a power supply or an output of a device with high driving capability if noise is input to those pins. To prevent this, connect a 30 Ω or more pin protection resistor to the pins in series. The resistance value should be determined by evaluating it on the mounting board.
When connecting a power supply directly to the V_{REFA} pin, insert a 100 Ω resistor in series. This resistance does not affect the A/D converter characteristics.

Revision History

Attachment-1

Rev. No.	Date	Page	Category	Contents
Rev 1.00	2023/12/20	All	New	

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