

Epson ASIC proposal

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MD Sales Division

The product features in this presentation is as of
Jan. 2025 and may change without notification.

1. About Epson ASIC

- Key features
- Major usage
- Application examples

2. Product features

- Features
- Lineups
- Target of replacement

3. Use cases

- Reproduction of discontinued ASIC
- Replacement from PLD to ASIC
- Replacement projects and NRE images

4. New product idea

- S1L80000(0.15um gate array)
- Features of LVDS-Tx
- PLD examples for package compatible

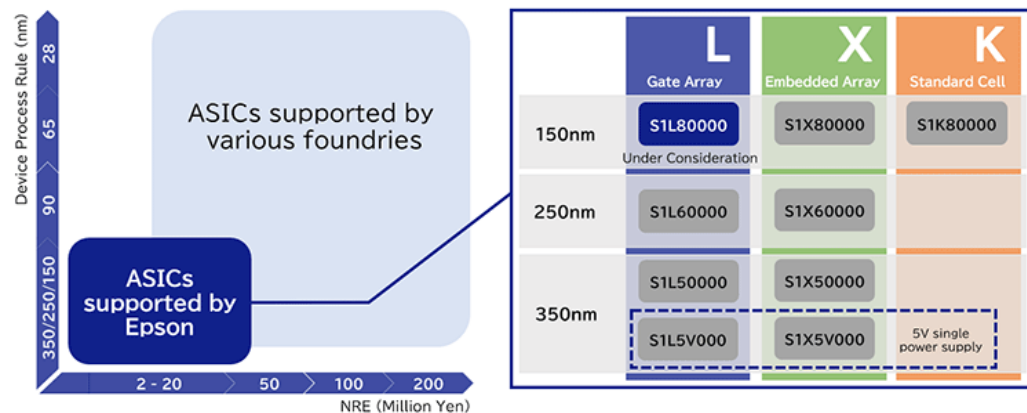
5. Others

- Design interface
- ASIC website
- Fab location

1. About Epson ASIC

■Key features of Epson ASIC

- Started ASIC business on 1982, have many design experiences and shipment records.
- Various lineup of Gate array/Embedded array/Standard cell
- Have own fabs and provide IDM solution from design to production and testing.



■Major usage of Epson ASIC

- Reproduction of discontinued ASIC or PLD(FPGA, CPLD)
- Redevelopment to respond to market supply constraints or price increase
- Custom IC development which cannot realize by standard MCU or PLD
(ex. Constraints of Supply voltage, size, power consumption...)

■Application examples

- Product which required long product lifecycle
- Industrial applications
(PLC, Industrial displays, Servo, Inverter, CNC, etc.)
- Measurement instruments

2. Product features

Free pin assignment

Realize pin-to-pin compatible when you replace from discontinued IC

5V single power operation

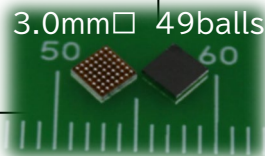
Suitable for legacy system or products which require noise immunity.

Power consumption measurement

Can measure actual developed ASIC power consumption with LSI tester to compare with original IC.(Optional)

Small package support

4mm□~ VFBGA/SQFN
2.4mm□~ WL-CSP
Suitable for small products



Power supply separation

- I/O:Can interface between different voltage devices
- Core:Realize low power operation or battery backup

Wide range voltage operation

Can operate at different voltage level with single products. (i.e. 3.3V and 5V, or 2.0V and 3.3V)

Customization of I/O characteristics

Customize DC, AC characteristics of I/O to support original IC's interface standard.(Optional)

LVDS IO

Tx and Rx can be installed in pairs.
Wide amplitude low-voltage differential signaling (WA-LVDS) is available.

※Contents of this slide differ for each ASIC series.

2. Series lineups

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Macro cells

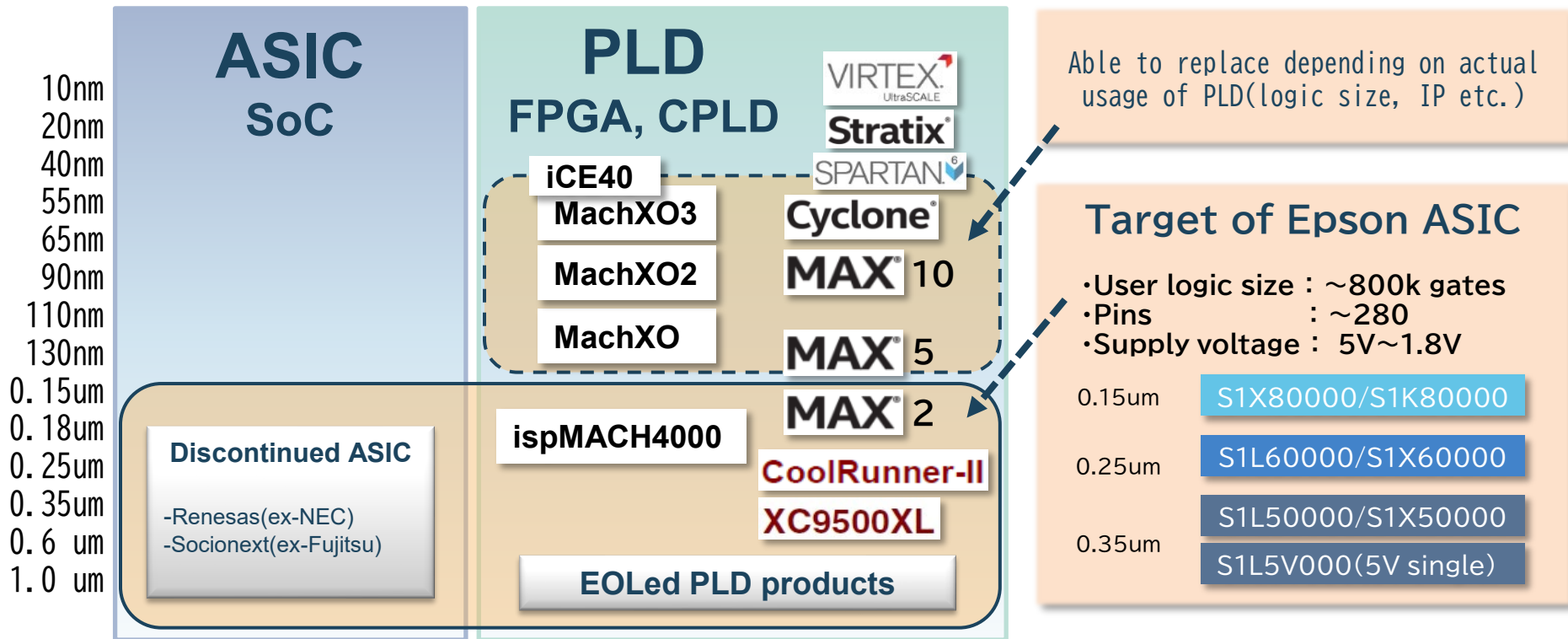
PLL
32kHz -> 200MHz
5MHz -> 200MHz

SRAM
1-port
2-port (1R+1W)
Dual port (2R+2W)

ROM
1k to 256k-bit
1k to 512k-bit/0.15um

LVDS
FPD-Link
LVDS-IO(WA-LVDS)

2. Target of replacement

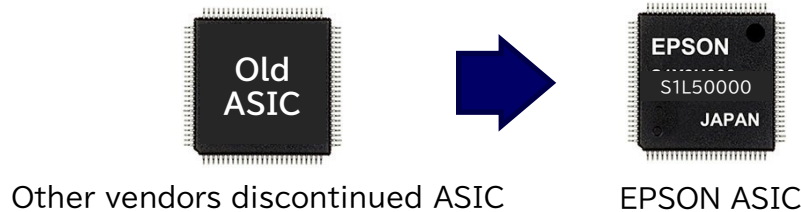


3. Use case examples: Reproduction of discontinued ASIC

EPSON

Realize short development time with low cost NRE

• Reproduction of discontinued IC

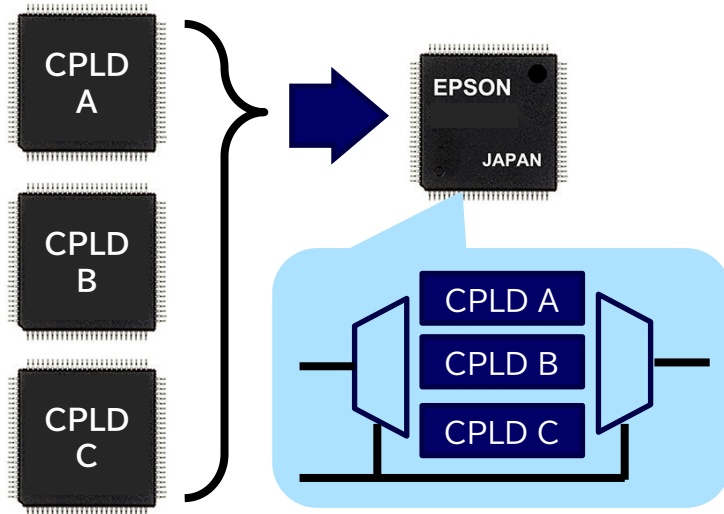


- Power supply voltage, pin assignment, function compatible
- Can adjust I/O characteristics to be the same as original IC
- Design support for low power consumption, and verify by the measurement of actual sample.
- Can support legacy system which require 5V power supply
- Not only just copy original, re-development with additional function

3. Use case examples: Replacement from PLD to ASIC

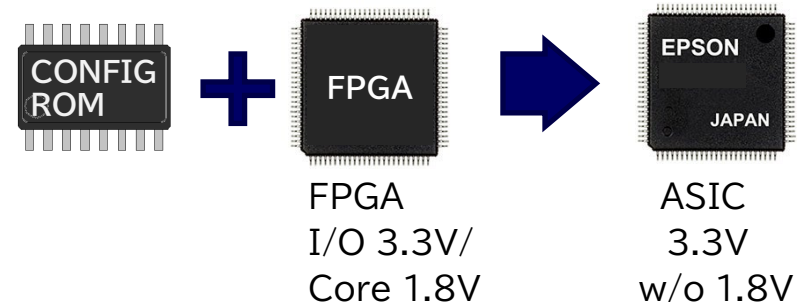
- Reproduction for EOled PLD
 - Replacement due to supply issues
- ➔ Solution for the stable supply and improving profitability

Multiple CPLDs into one ASIC



CPLD A/B/C selection is realized by PKG bonding option or dedicated external signal

FPGA to ASIC



footprint compatible
without config ROM
without 1.8V Power supply

3. Use case examples: Actual replacement projects

Replacement target		ASICs	Packages
Low-cost FPGA	Spartan	S1L5V042 S1L51253 S1L60284 S1X50000	P-LQFP100-1414-0.50 P-LQFP100-1414-0.50 P-TQFP080-1212-0.50 P-TQFP128-1414-0.40
Low-cost FPGA	Cyclone	S1L50553 S1X50000	P-LQFP144-2020-0.50 P-LQFP100-1414-0.50
Small-size FPGA	MAX10	S1L5V254	P-LQFP080-1212-0.50
CPLD	MAX2 MAX5	S1L50552 S1L50282	P-LQFP144-2020-0.50 P-TQFP100-1414-0.50
CPLD	MACH	S1L5V012 S1L50122 S1L50282 S1L50552	P-LQFP048-0707-0.50 P-TFBGA-096-0606-0.50 P-LQFP100-1414-0.50 P-LQFP144-2020-0.50
Low-cost FPGA Small-size FPGA		S1L80000	<i>Planning new product: 0.15um Gate array S1L80000 series</i>

3. Use case examples: NRE images

Replacement target		Product	Package	Process/Metal layer NRE
Small-size FPGA	MAX5	S1L50282	P-TQFP100-1414-0.50	0.35um/2LM Gate Array 2Myen
Low-cost FPGA	Spartan6	S1L60284	P-LQFP080-1212-0.50	0.25um/4LM Gate Array 5Myen
Low-cost FPGA	Cyclone4	S1L61584	P-LQFP256-2828-0.40	0.25um/4LM Gate Array 7Myen
Low-cost FPGA	Spartan6	S1X50000	P-TQFP128-1414-0.40	0.35um/4LM Embedded Array 10Myen
EOL ASIC	0.18um	S1X80000	P-LQFP100-1414-0.50	0.15um/5LM Embedded Array 17Myen

4. New product idea: S1L80000 series (0.15um Gate Array) EPSON

- New Gate Array product idea to replace existing PLD, now under planning
- Can realize 0.15um ASIC with cheaper NRE, and able to support reasonable MOQ

<i>tentative</i>	<i>S1L8010</i>	<i>S1L8015</i>	<i>S1L8020</i>	<i>S1L8030</i>
Usable gates 4LM	120K	230K	315K	650K
Usable gates 5LM	135K	255K	350K	720K
Usable pads	100	180	256	280
Available PKG examples Line up	QFP48, 64, 100 VFBGA5H-81 VFBGA6H-121	QFP48, 64, 100, 144 PFBGA10U-144 PFBGA12U-180	QFP64, 100, 144, 208, 256 PFBGA14U-256 PBGA1UE-256	QFP64, 100, 144, 208, 256 PFBGA14U-256 PFBGA16U-280
Power supply voltage	Dual: Core 1.8V, I/O 3.3V Single: 3.3V	Dual: Core 1.8V, I/O 3.3V	Dual: Core 1.8V, I/O 3.3V	Dual: Core 1.8V, I/O 3.3V
Target operating frequency	Dual: 120MHz Single: 40MHz	Dual: 120MHz	Dual: 120MHz	Dual: 120MHz
LDO w/external capacitor	Core 1.8V up to 30mA	-	-	-
PLL 5M->200MHz	1pc	2pcs	2pcs	2pcs
Embedded SRAM	-	-	DP-RAM: 16b x 256w x 4pcs	DP-RAM: 16b x 256w x 4pcs
LVDS IO	-	Tx 4pairs/Rx 4pairs	Tx 8pairs/Rx 8pairs	Tx 8pairs/Rx 8pairs
Device characteristics S1X80000	Internal gate delay: 34.5ps/1.8V 2-input NAND Typ. Power consumption: 0.063uW/MHz/gate 2-input NAND typ. Drivability of output buffer: IOL=2, 4, 8, 12mA at 3.3V			
Others	Gate array configurable SRAM 1port/2port, OSC buffers for external x' tal			

4. New product: Features of LVDS-Tx

The optimum output for LVDS-Rx can be set

WA-LVDS Wide Amplitude LVDS

[News Release](#)

[Technical Note](#)

The graph showing characteristics(not guaranteed values)

The amplitude, output current,
and phase jitter of differential outputs

✗ LVDS, LV-PECL, HCSL

● WA-LVDS

<Figure 1>

Output current LVDS < LV-PECL, HCSL

Noise tolerance LVDS < LV-PECL, HCSL

<Figure 2>

As WA-LVDS amplitude increases,
phase jitter decreases,
resulting in differential output with
low noise.

Item	Specification
Power supply	3.3V±0.3V
Amplitude voltage	350~800mV 16 step setting
Offset voltage	0.9, 1.25, 1.5, 1.65V 4 step setting

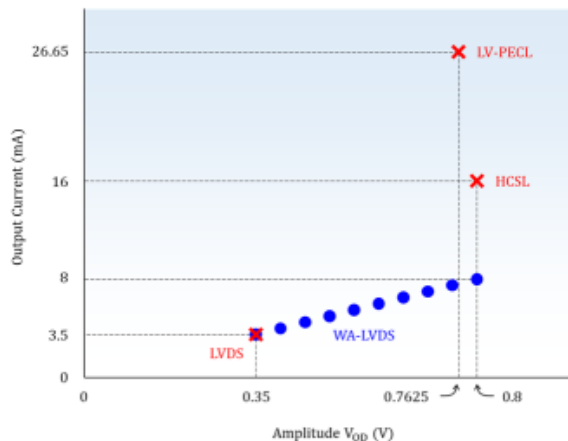


Figure 1: Amplitude vs. output current for differential

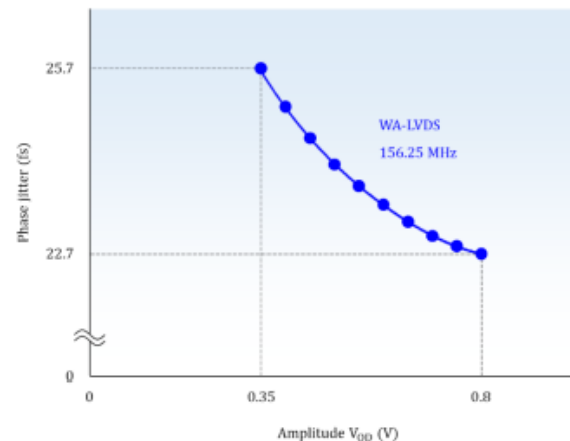
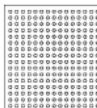


Figure 2: WA-LVDS phase jitter

4. PLD examples for package compatible

QFP15-100PIN P-LQFP100-1414-0.50	Lattice TQFP	LCMXO	LCMXO256	LCMXO640	LCMXO1200	LCMXO2280
		LCMXO2	XO2-256	XO2-640	XO2-1200	XO2-2000
	Intel TQFP	MAX II	EPM240	EPM570		
		MAX V	5M80Z	5M160Z	5M240Z	5M570Z
QFP20-144PIN P-LQFP144-2020-0.50	Lattice TQFP	LCMXO	LCMXO640	LCMXO1200	LCMXO2280	
		LCMXO2	XO2-640U	XO2-1200	XO2-2000	XO2-4000 XO2-7000
		ECP5	LFE5U-12	LFE5U-25	LFE5U-45	
	Intel TQFP	MAX II	EPM570	EPM1270		
		MAX V	5M240Z	5M570Z	5M1270Z	
		MAX 10	10M02SC	10M04SC	10M08SC	10M16SC 10M25SC 10M40SA 10M50SA
		Cyclone10	10CL006	10CL010	10CL016	10CL025
		Cyclone4	EP4CE6	EP4CE10	EP4CE15	EP4CE22
		AMD TQG	Spartan-6	XC6SLX4	XC6SLX9	
VFPGA6H-121 P-VFPGA-121-0606-0.50	Lattice csfBGA	LCMXO3	XO3L-640	XO3L-1300	XO3L-2100	XO3L-4300
		iCE40 LP	LP1K			
PFPGA14U-256 P-TFPGA-256-1414-0.80	Lattice caBGA	LCMXO	LCMXO640	LCMXO1200	LCMXO2280	
		LCMXO2	XO2-2000	XO2-4000	XO2-7000	
		LCMXO3	XO3L-1300	XO3L-2100	XO3L-4300	XO3L-6900 XO3L-9400
		ECP5	LFE5U-12	LFE5U-25	LFE5U-45	
		iCE40 HX	HX8K			
	Intel UBGA	Cyclone10	10CL006	10CL010	10CL016	10CL025
		Cyclone4	EP4CE6	EP4CE10	EP4CE15	EP4CE22
PBGA1UC256 P-LBGA-0256-1717-1.00	Lattice ftBGA	LCMXO	LCMXO640	LCMXO1200	LCMXO2280	
		LCMXO2	XO2-1200U	XO2-2000	XO2-4000	XO2-7000
	Intel FBGA	MAX II	EPM1270	EPM2210		
		MAX V	5M570Z	5M2210Z	5M1270Z	
		MAX 10	10M04DA	10M08DA	10M16DA	10M25DA 10M40DA 10M50DA
		Cyclone V	5CEBA2	5CEBA4		
		Cyclone4	EP4CE6	EP4CE10	EP4CE15	EP4CE22
		AMD FTG	Spartan-6	XC6SLX9	XC6SLX16	XC6SLX25

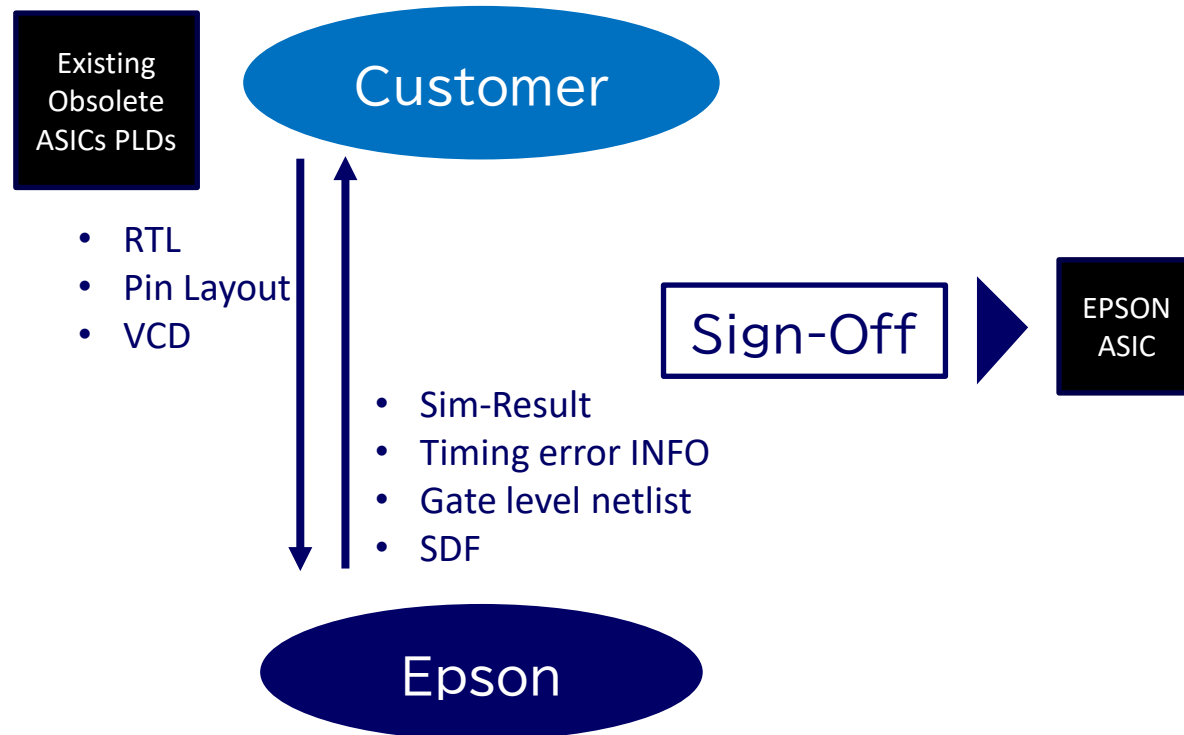
PKG Type		Body Size (mm)	Lead Pitch (mm)
QFP15-100PIN		14 x 14 x 1.7	0.5
QFP20-144PIN		20 x 20 x 1.7	0.5

PKG Type		Body Size (mm)	Ball Pitch (mm)
VFPGA6H-121		6 x 6 x 1.0	0.5
PFPGA14U-256		14 x 14 x 1.2	0.8
PBGA1UE256		17 x 17 x 1.7	1.0

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5. Others: ASIC Design interface

Users only need to send us RTL and VCD files of simulation results obtained with their test bench.



ASIC top page

<https://global.epson.com/products and drivers /semicon/products/asic/>

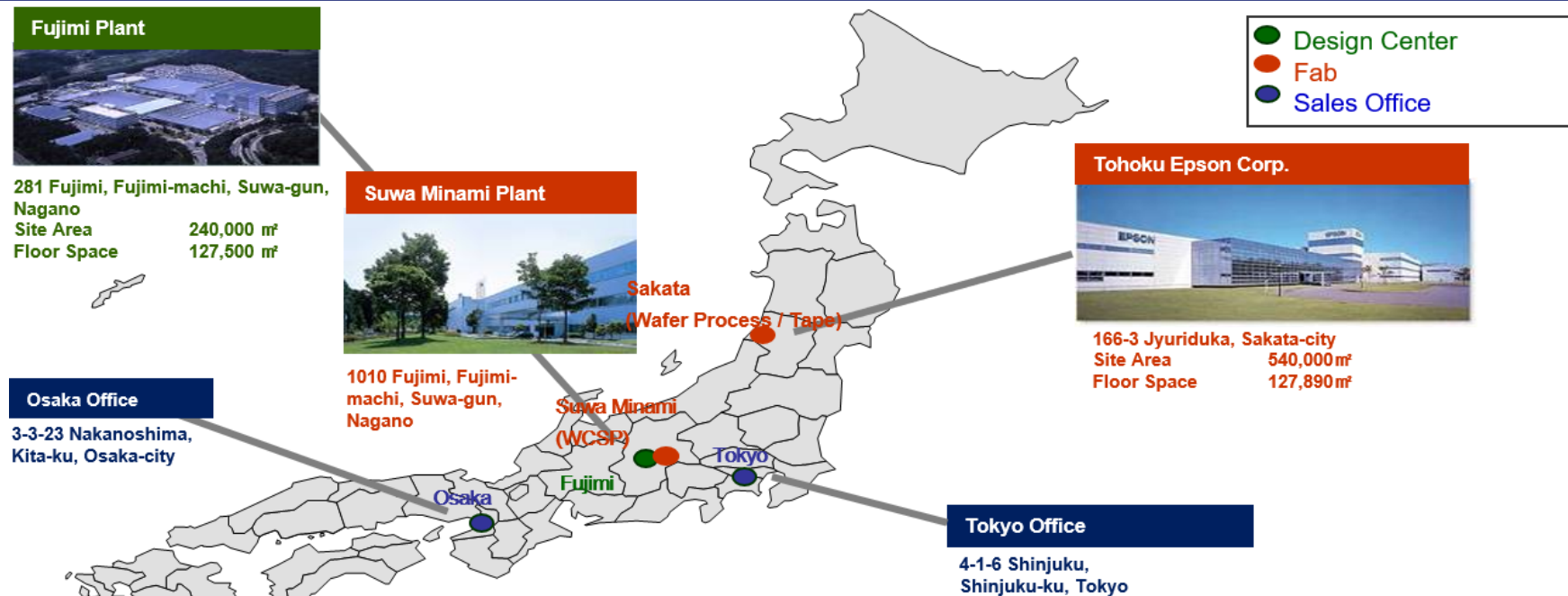
ASIC Development Interface

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Pamphlet PDF 32MB

<https://global.epson.com/products and drivers /semicon/pdf/id000456.pdf>

5. Others: Fab location



Wafer Process

Wafer Size	Technology	Capacity (wf/month)	Location	Operation Start
8 inch (T wing)	0.15 - 0.35 μ m	25K	Tohoku Epson	1997
6 inch (S wing)	0.35 - 1.2 μ m	20K	Tohoku Epson	1991

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