Errata No. X42A-P-001-01

Device: S1D13700F00A100

The following problems exist for the S1D13700F00A100. This document outlines the problems and provides possible work-arounds.

Problem Description: External Connection Change for MC68K Interface

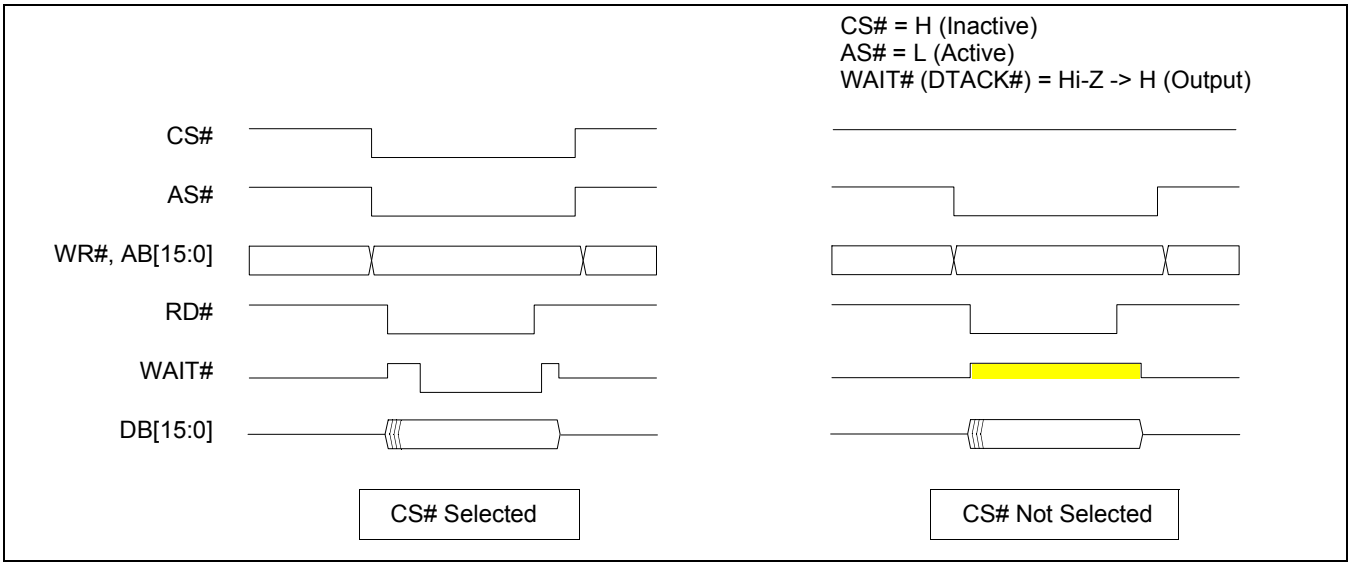
The problem occurs when the MC68K family MPU is selected (CNF[3:2] = 11b) and the WAIT# (DTACK#) output signal is used. In this case, a gate circuit must be added on the system board.

Note

The Generic Bus Interface (including the Z80 Family Bus) and the M6800 Family Bus Interface have different architectures and are not affected by this problem.

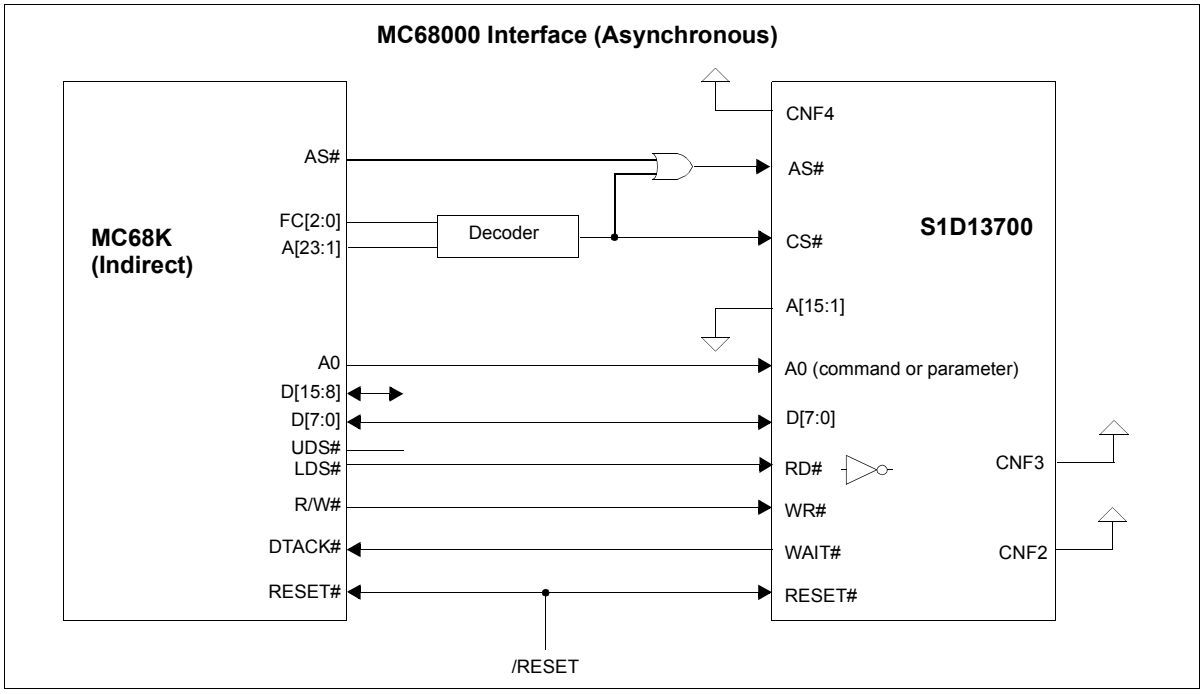
Problem

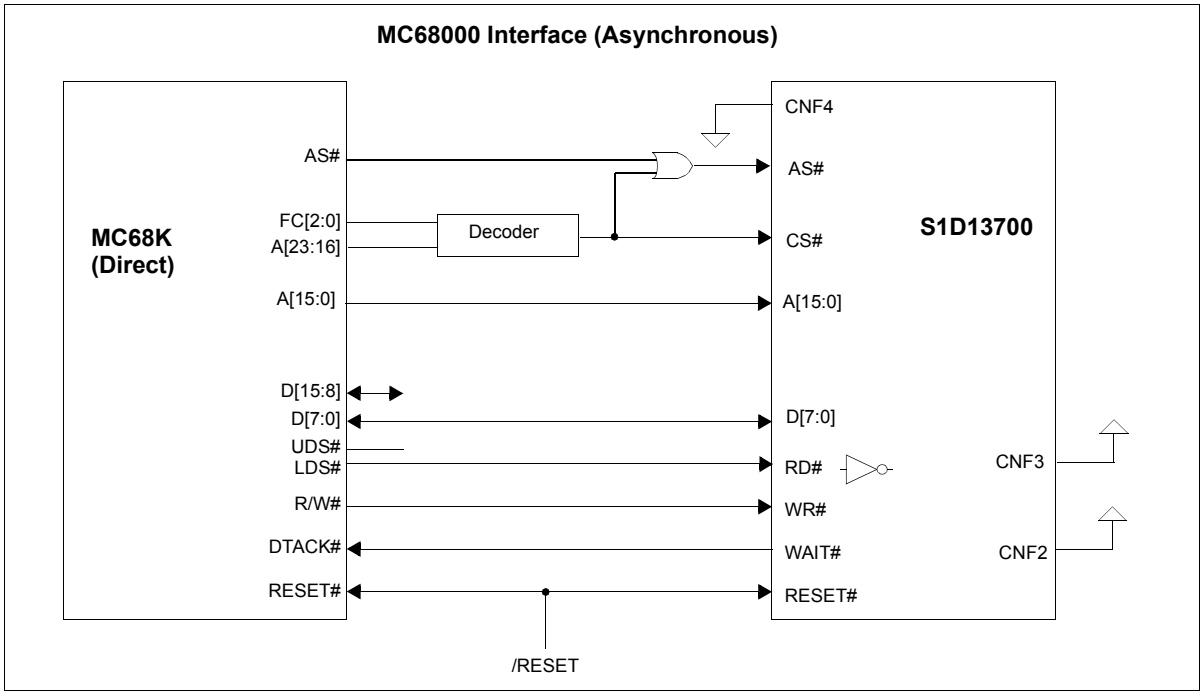
WAIT# (DTACK#) is a tri-state output pin. When CS# is not selected, the S1D13700 should place the WAIT# pin in a Hi-Z state. However, the S1D13700F00100 drives the WAIT# pin to the H level as shown by the yellow colored pulse in the following chart.



Work-around

A possible work-around for the problem is to make an additional circuit on the system board. Add an OR gate circuit to system board as shown in the following diagrams. When this OR gate is added to the S1D13700 AS# input, the S1D13700 remains in a high impedance state for WAIT# (DTACK#) output even when CS# is not selected.





Problem Description: Display Noise Caused by Display Memory Access While Overlaying Three Layers

When display memory is accessed by the MPU while overlaying three graphics layers, line noise may occur on the display during the display memory access period. This problem occurs when all of the following conditions are met.

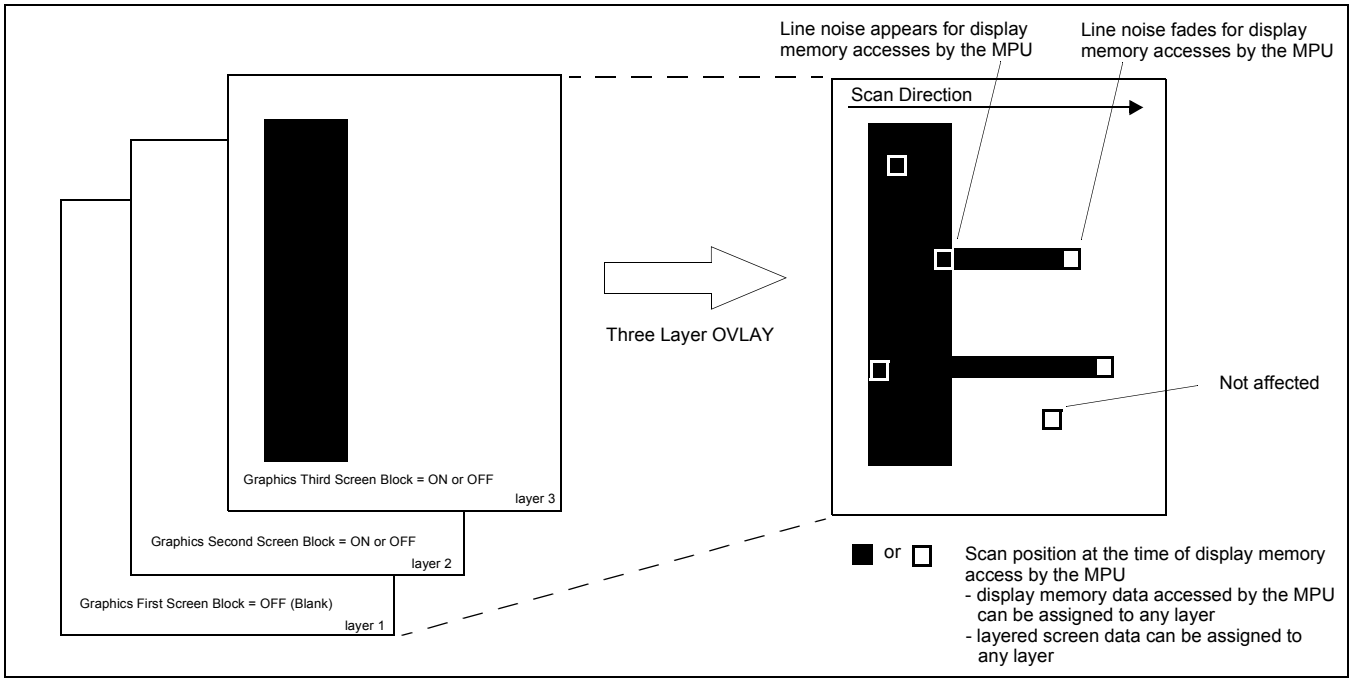
- When displaying all three layers overlaid (all layers are graphics). (W/S=0, OV=1, DM[2:1] = 11b)
- When display of 1st layer is set to "off" (blank). (FP[1:0] = 00b)
- When a read or write access to the display memory is made by the MPU while displaying the screen.

Note
This problem is not dependent on which display layer memory area is accessed by the MPU.

Problem

When overlaying three layers, the S1D13700 scans display memory data line by line and then displays it. If the display memory is accessed by the MPU while the S1D13700 is scanning, data shown on the display is fixed to the data scanned. If access to the display memory does not continue, the display state returns to normal from the next frame onward.

The following diagram shown how the problem appears on the display. Random line noise appears to the right of the black and white border, only while the MPU is accessing the display memory.

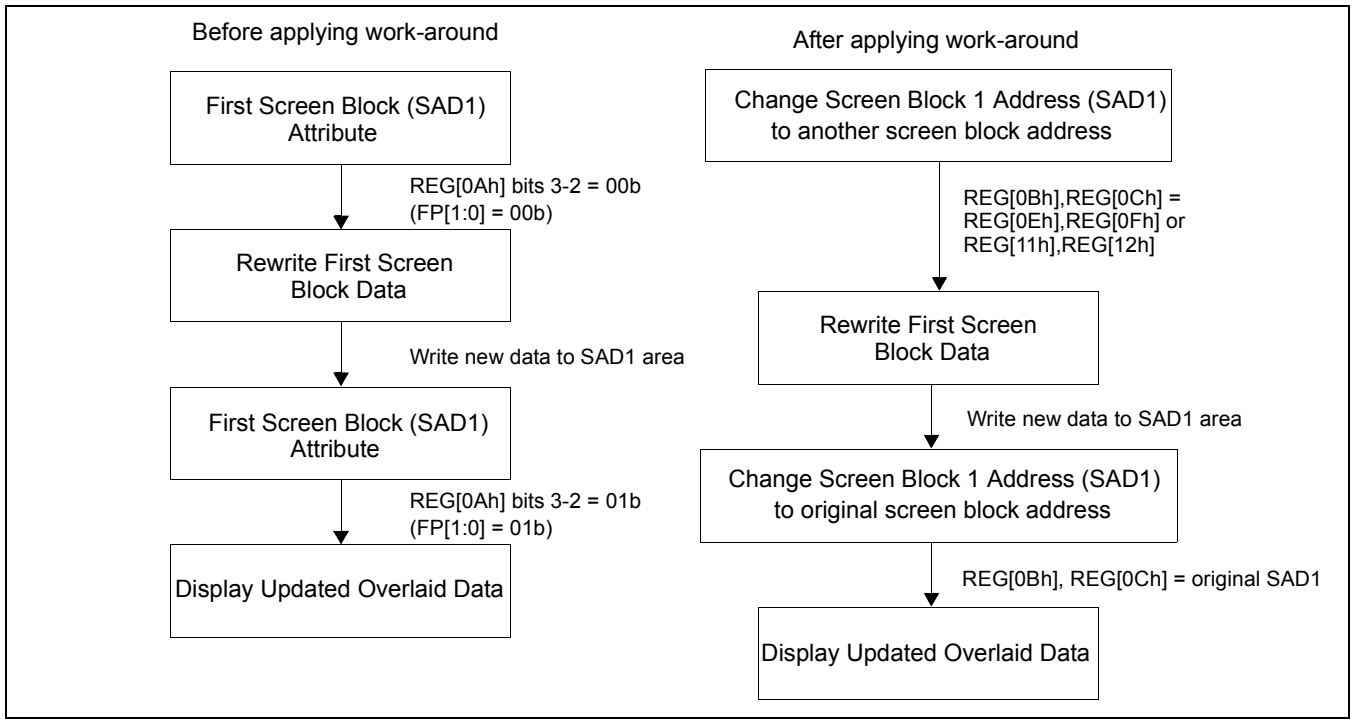


Work-around

There is a software work-around for this problem. The following flowchart shows two example flows. The flow on the left does not use the work-around and will cause the problem to occur. The flow on the right demonstrates the work-around and will avoid the line noise problem.

The flow on the left sets first screen block attribute to "off", accesses the display memory, and then returns the attribute to "on". This flow will allow the problem to occur.

The flow on the right changes the first screen block address to the same value as another screen block address instead of setting the attribute to "off". This causes the first layer not to be displayed while the display memory is being updated by the MPU. Once the display memory update is complete, the screen block address can be returned to the original address. This flow avoids the line noise problem.



Note

If all layers (first, second, and third) are set to "off", all display data becomes 0 and the problem does not occur. In this case, the work-around is not required.