Apr/17/2017

errata_c1762x/60x_10

S1C17 Family Technical Manual Errata

ITEM **A part of shipping form is discontinued**			
Object manual	Document code	Object item	Page
S1C17624/604/602/621 Technical Manual	411914903	Shipping form	1-2

1.1 Features

(Error)

Shipping form				
1	TQFP15-128pin	TQFP14-100pin	TQFP15-128pin	TQFP14-100pin
2	Die form	Die form	Die form	Die form
3				VFBGA7H-144
Size/pitch	TQFP15-128pin (body size: 14 mm × 14 mm, lead pitch: 0.4 mm) TQFP14-100pin (body size: 12 mm × 12 mm, lead pitch: 0.4 mm) VFBGA7H-144 (body size: 7 mm × 7 mm, ball pitch: 0.5 mm) Die form (pad pitch: 100 µm)			

(Correct)

Shipping form				
1	TQFP15-128pin	TQFP14-100pin	TQFP15-128pin	TQFP14-100pin
2	Die form	Die form	Die form	Die form
3				VFBGA7H-144 #1
Size/pitch	TQFP15-128pin (body size: 14 mm × 14 mm, lead pitch: 0.4 mm) TQFP14-100pin (body size: 12 mm × 12 mm, lead pitch: 0.4 mm) VFBGA7H-144 (body size: 7 mm × 7 mm, ball pitch: 0.5 mm) #1 Die form (pad pitch: 100 µm)			

#1 : VFBGA7H-144 for S1C17602 & S1C17621 is discontinued.

Mar/29/2013

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S1C17 Family Technical Manual Errata

ITEM Features of OSC1 oscillator circuit

Object manual	Document code	Object item	Page
S1C17624/604/622/602/621 Technical Manual	411914902	1.1 Features	1-1

(Error)

Clock generator	
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator circuit Supports an external clock input.

(Correct)

Clock generator	
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator circuit ~~Supports an external clock input.~~

S1C17 Family Technical Manual Errata

ITEM About the Fine mode setting of T16E.			
Object manual	Document code	Object item	Page
S1C17001 Technical Manual	411412303	13.6 Clock Output Control	150
S1C17003 Technical Manual	411635102	13.6 Clock Output Control	13-8
S1C17624/604/622/621 Technical Manual	411914902	12.7 Clock Output Control	12-6
S1C17701 Technical Manual	411089905	13.6 Controlling Clock Output	13-8
S1C17702 Technical Manual	411581702	13.6 Clock Output Control	13-8
S1C17704 Technical Manual	411511903	13.6 Controlling Clock Output	13-8

Page 150 S1C17001 Technical Manual

Page 13-8 S1C17003 Technical Manual

Page 13-8 S1C17701 Technical Manual

Page 13-8 S1C17702 Technical Manual

Page 13-8 S1C17704 Technical Manual

Add following comment at Precautions of “Setting fine mode for clock output”.

(3) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).

Page 12-6 S1C17623/604/622/621 Technical Manual

Add following comment at Precautions of “Setting fine mode for clock output”.

(4) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).

Oct/5/2012

errata_c1762x/60x_7

S1C17 Family Technical Manual Errata

ITEM About Internal RAM size select.			
Object manual	Document code	Object item	Page
S1C17624/604/622/621 Technical Manual	411914902	3.3.1 Embedded RAM	3-6

Page 3-6 S1C17623/604/622/621 Technical Manual

(Error)

The S1C17624/604 enables the RAM size used to apply restrictions to 8KB, 4KB, or 2KB. The S1C17602 enables the RAM size used to apply restrictions to 4KB or 2KB. For example, when using the S1C17624/604/602 to develop an application for a built-in ROM model, you can set the RAM size to match that of the target model, preventing creating programs that seek to access areas outside the RAM areas of the target product. The RAM size is selected using IRAMSZ[2:0]/MISC_IRAMSZ register.

(Correct)

The S1C17624/604 enables the RAM size used to apply restrictions to 8KB, 4KB, or 2KB. The S1C17622 enables the RAM size used to apply restrictions to 4KB or 2KB. For example, when using the S1C17624/604/622 to develop an application for a built-in ROM model, you can set the RAM size to match that of the target model, preventing creating programs that seek to access areas outside the RAM areas of the target product. The RAM size is selected using IRAMSZ[2:0]/MISC_IRAMSZ register.

S1C17 Family Technical Manual Errata

ITEM About Flash Protect Bits			
Object manual	Document code	Object item	Page
S1C17624/604/622/621 Technical Manual	411914902	3. Memory Map 3.2.3 Protect Bits	3-2, 3-5

Page 3-2 S1C17623/604/622/621 Technical Manual

(Error-1)

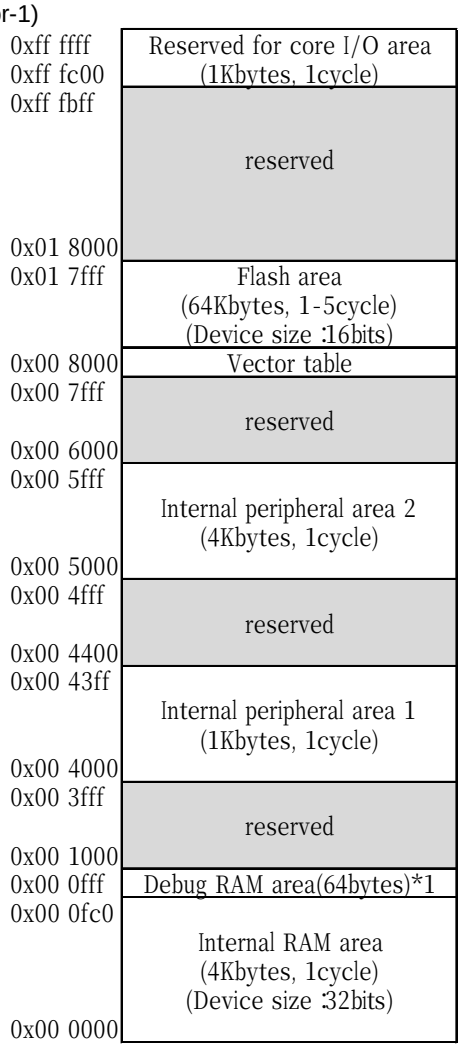

Figure3.2 S1C17622/602 Memory Map

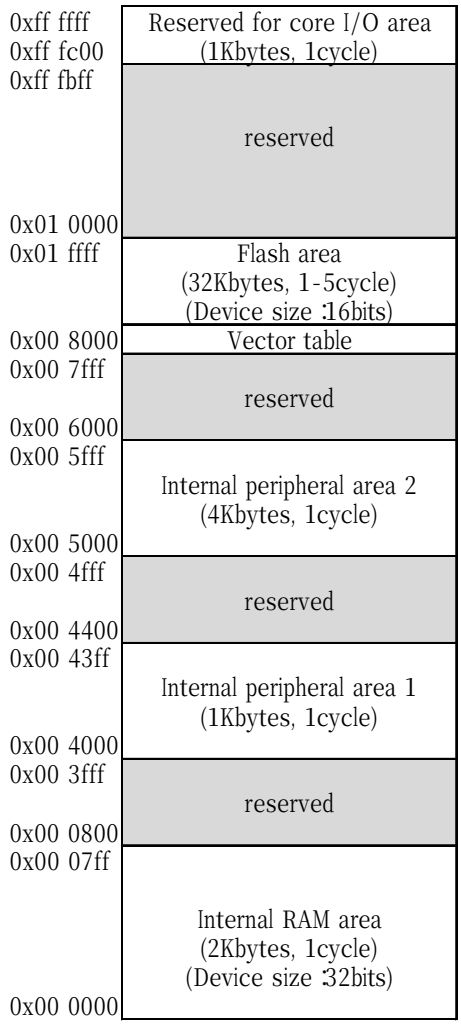

Figure3.3 S1C17621 Memory Map

(Correct-1)

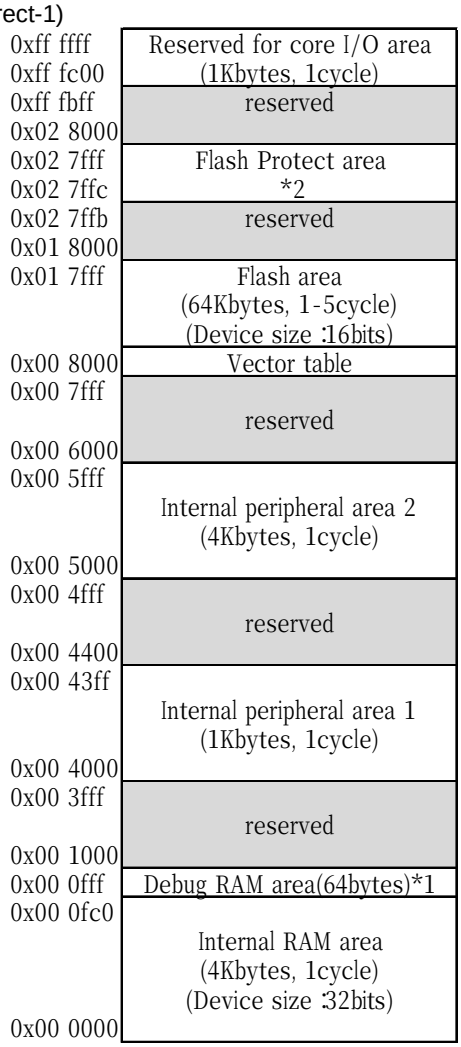

Figure3.2 S1C17622/602 Memory Map

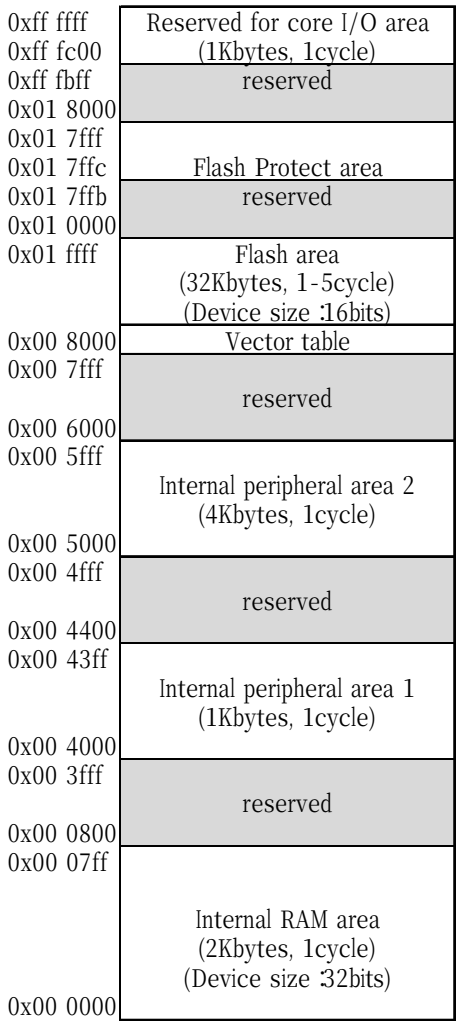

Figure3.3 S1C17621 Memory Map

*2 The address range from 0x27ffc to 0x27fffof the S1C17602 is a reserved area.

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(Error-2)

Flash Protect Bits (S1C17622/602)

Address	Bit	Function	Setting	Init.	R/W	Remarks
0x17ffc (16 bits)	D15-4	Reserved	-	-	-	
	D3	Flash write-protect bit for 0x14000-0x17fff	1 Writeable 0 Protected	1	R/W	
	D2	Flash write-protect bit for 0x10000-0x13fff	1 Writeable 0 Protected	1	R/W	
	D1	Flash write-protect bit for 0xc000-0xffff	1 Writeable 0 Protected	1	R/W	
	D0	Flash write-protect bit for 0x8000-0xbfff	1 Writeable 0 Protected	1	R/W	

Address	Bit	Function	Setting	Init.	R/W	Remarks
0x17ffe (16 bits)	D15-4	Reserved	-			
	D3	Flash data-read-protect bit for 0x14000-0x17fff	1 Readable 0 Protected	1	R/W	
	D2	Flash data-read-protect bit for 0x10000-0x13fff	1 Readable 0 Protected	1	R/W	
	D1	Flash data-read-protect bit for 0xc000-0xffff	1 Readable 0 Protected	1	R/W	
	D0	reserved	1	1	R/W	Always set to 1.

Flash Protect Bits (S1C17621)

Address	Bit	Function	Setting	Init.	R/W	Remarks
0xfffc (16 bits)	D15-2	Reserved	-	-	-	
	D1	Flash write-protect bit for 0xc000-0xffff	1 Writeable 0 Protected	1	R/W	
	D0	Flash write-protect bit for 0x8000-0xbfff	1 Writeable 0 Protected	1	R/W	

Address	Bit	Function	Setting	Init.	R/W	Remarks
0xfffe (16 bits)	D15-2	Reserved	-	-	-	
	D1	Flash data-read-protect bit for 0xc000-0xffff	1 Writeable 0 Protected	1	R/W	
	D0	reserved	1	1	R/W	Always set to 1.

Notes:
- Be sure not to locate the area with data-read protection into the .data and .rodata sections.
- Be sure to set D0 of address 0x27ffe (S1C17624/604), 0x17ffe (S1C17622/602), or 0xfffe (S1C17621) to 1. If it is set to 0, the program cannot be booted.

(Correct-2)

Flash Protect Bits (S1C17622)

Address	Bit	Function	Setting				Init.	R/W	Remarks
0x27ffc (16 bits)	D15-4	Reserved	-				-	-	
	D3	Flash write-protect bit for 0x14000-0x17fff	1	Writeable	0	Protected	1	R/W	
	D2	Flash write-protect bit for 0x10000-0x13fff	1	Writeable	0	Protected	1	R/W	
	D1	Flash write-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W	
	D0	Flash write-protect bit for 0x8000-0xbfff	1	Writeable	0	Protected	1	R/W	

Address	Bit	Function	Setting				Init.	R/W	Remarks
0x27ffe (16 bits)	D15-4	Reserved	-						
	D3	Flash data-read-protect bit for 0x14000-0x17fff	1	Readable	0	Protected	1	R/W	
	D2	Flash data-read-protect bit for 0x10000-0x13fff	1	Readable	0	Protected	1	R/W	
	D1	Flash data-read-protect bit for 0xc000-0xffff	1	Readable	0	Protected	1	R/W	
	D0	reserved	1				1	R/W	Always set to 1.

Flash Protect Bits (S1C17602)

Address	Bit	Function	Setting				Init.	R/W	Remarks
0x17ffc (16 bits)	D15-4	Reserved	-				-	-	
	D3	Flash write-protect bit for 0x14000-0x17fff	1	Writeable	0	Protected	1	R/W	
	D2	Flash write-protect bit for 0x10000-0x13fff	1	Writeable	0	Protected	1	R/W	
	D1	Flash write-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W	
	D0	Flash write-protect bit for 0x8000-0xbfff	1	Writeable	0	Protected	1	R/W	

Address	Bit	Function	Setting				Init.	R/W	Remarks
0x17ffe (16 bits)	D15-4	Reserved	-						
	D3	Flash data-read-protect bit for 0x14000-0x17fff	1	Readable	0	Protected	1	R/W	
	D2	Flash data-read-protect bit for 0x10000-0x13fff	1	Readable	0	Protected	1	R/W	
	D1	Flash data-read-protect bit for 0xc000-0xffff	1	Readable	0	Protected	1	R/W	
	D0	reserved	1				1	R/W	Always set to 1.

Flash Protect Bits (S1C17621)

Address	Bit	Function	Setting				Init.	R/W	Remarks
0x17ffc (16 bits)	D15-2	Reserved	-				-	-	
	D1	Flash write-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W	
	D0	Flash write-protect bit for 0x8000-0xbfff	1	Writeable	0	Protected	1	R/W	

Address	Bit	Function	Setting				Init.	R/W	Remarks
0x17ffe (16 bits)	D15-2	Reserved	-				-	-	
	D1	Flash data-read-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W	
	D0	reserved	1				1	R/W	Always set to 1.

Notes: • Be sure not to locate the area with data-read protection into the .data and .rodata sections.
• Be sure to set D0 of address 0x27ffe (S1C17624/604/622) or 0x17ffe (S1C17602/621) to 1.
If it is set to 0, the program cannot be booted.

Dec/27/2011

errata_c1762x/60x_5

S1C17 Series Technical Manual Errata

ITEM About the CBUFEN register of T16A/T16A2

Object manual	Document code	Object Item	Page
S1C17624/604/622/602/621 Technical Manual	411914902	13.8 Control Register Details	13-14 13-15
S1C17705/703 Technical Manual	411706602	10.8 Control Register Details	10-19
S1C17706 Technical Manual	412026401	10.8 Control Register Details	10-17
S1C17711 Technical Manual	411905602	10.8 Control Register Details	10-14
S1C17554/564 Technical Manual	411914402	11.8 Control Register Details	11-14
S1C17651 Technical Manual	412120600	12.8 Control Register Details	12-13

Page 13-14 13-15 S1C624/604/622/602/621 Technical Manual

Page 10-17 S1C17706 Technical Manual

Page 12-13 S1C17651 Technical Manual

(Error)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.

(Correct)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare

A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (CLKEN = 0) before setting CBUFEN.

Page 13-14 13-15 S1C17705/703 Technical Manual

Page 10-14 S1C17711 Technical Manual

Page 11-14 S1C17554/564 Technical Manual

(Error)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.

(Correct)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (CLKEN = 0) before setting CBUFEN.