S1C17 Family Technical Manual Errata

ITEM	LCD drive voltage		
Object manual	Document code	Object item	Page
S1C17701Technical Manual	411089905	26.4 Analog Circuit Characteristics	26-3
S1C17702Technical Manual	411581702	27.4 Analog Circuit Characteristics	27-3
S1C17704Technical Manual	411511903	26.4 Analog Circuit Characteristics	26-3
S1C17705/703Technical Manual	411706602	25.9 LCD Driver Characteristics	25-10
S1C17706Technical Manual	412026401	27.9 LCD Driver Characteristics	27-7

(Error)

Unless otherwise specified: V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta = 25°C, C_1–C_{11} = 0.1μF, Checker pattern displayed, No panel load

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1}		$0.18V_{C5}$		$0.22V_{C5}$	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2}		$0.39V_{C5}$		$0.43V_{C5}$	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3}		$0.59V_{C5}$		$0.63V_{C5}$	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4}		$0.79V_{C5}$		$0.83V_{C5}$	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5}	LC[3:0] = 0x0		4.20		V
			LC[3:0] = 0x1		4.30		V
			LC[3:0] = 0x2		4.40		V

(Correct)

Unless otherwise specified: V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta = 25°C, C_1–C_{11} = 0.1μF, Checker pattern displayed, No panel load

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between ~~V_{SS} and V_{C1}~~ V_{C5} and V_{C1}		$0.18V_{C5}$		$0.22V_{C5}$	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2}		$0.39V_{C5}$		$0.43V_{C5}$	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3}		$0.59V_{C5}$		$0.63V_{C5}$	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4}		$0.79V_{C5}$		$0.83V_{C5}$	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5}	LC[3:0] = 0x0		4.20		V
			LC[3:0] = 0x1		4.30		V
			LC[3:0] = 0x2		4.40		V

S1C17 Family Technical Manual Errata

ITEM About the Fine mode setting of T16E.			
Object manual	Document code	Object item	Page
S1C17001 Technical Manual	411412303	13.6 Clock Output Control	150
S1C17003 Technical Manual	411635102	13.6 Clock Output Control	13-8
S1C17624/604/622/621 Technical Manual	411914902	12.7 Clock Output Control	12-6
S1C17701 Technical Manual	411089905	13.6 Controlling Clock Output	13-8
S1C17702 Technical Manual	411581702	13.6 Clock Output Control	13-8
S1C17704 Technical Manual	411511903	13.6 Controlling Clock Output	13-8

Page 150 S1C17001 Technical Manual
Page 13-8 S1C17003 Technical Manual
Page 13-8 S1C17701 Technical Manual
Page 13-8 S1C17702 Technical Manual
Page 13-8 S1C17704 Technical Manual

Add following comment at Precautions of "Setting fine mode for clock output".

(3) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).

Page 12-6 S1C17623/604/622/621 Technical Manual

Add following comment at Precautions of "Setting fine mode for clock output".

(4) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).

S1C17 Manual errata

ITEM: SPI Clock		
Object manuals	Document code	Object number
S1C17121	411723700	P19-3
S1C17702	411581700	P19-3
S1C17003	411635100	P19-3
S1C17601	411805700	P19-3
S1C17611	411882300	P19-3
S1C17705	411706600	P15-2
S1C17621/S1C17602/S1C17622/ S1C17604/S1C17624	411914900	P19-3

P19-3(S1C17602,S1C17121,S1C17702,S1C17003,S1C17601,S1C17611)

(Error)

The Master mode SPI uses the internal clock output by the 16-bit timer Ch.1 as SPI clock. This clock is output from the SPICLK pin to slave device while also driving the shift register. Use the MCLK(D9/SPI_CTL register) to select to use the 16-bit timer ch.1 output clock or PCLK-1/4 clock. Setting MCLK to 1 selects the 16-bit timer Ch.1 output clock; setting to 0 selects to 0 selects the PCLK-1/4 clock.

 *MCLK: SPI Clock Source Select Bit in the SPI Control(SPI_CTL)Register(D9/0x4326)

Using the 16-bit timer Ch.1 output clock enables programmable transfer rates. For more information on 16-bit timer control, see "11 16-bit Timer(T16)."

(Correct)

The Master mode SPI uses the internal clock output by the 16-bit timer Ch.1 as SPI clock. This clock is output from the SPICLK pin to slave device while also driving the shift register. Use the MCLK(D9/SPI_CTL register) to select to use the 16-bit timer ch.1 output clock or PCLK-1/4 clock is used. Setting MCLK to 1 selects the 16-bit timer Ch.1 output clock; setting to 0 selects to 0 selects the PCLK-1/4 clock.

*MCLK: SPI Clock Source Select Bit in the SPI Control(SPI_CTL)Register(D9/0x4326)

Using the 16-bit timer Ch.1 output clock enables programmable transfer rates. For more information on 16-bit timer control, see "11 16-bit Timer(T16)."
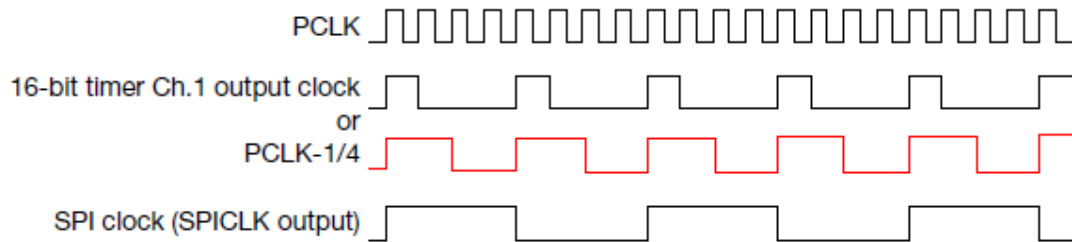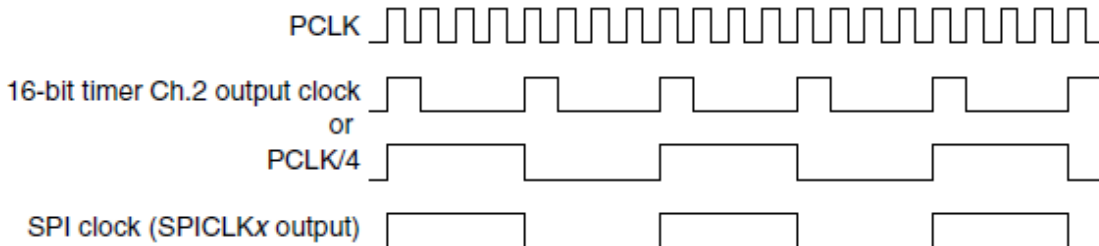

P15-2(S1C17705)

(Error)

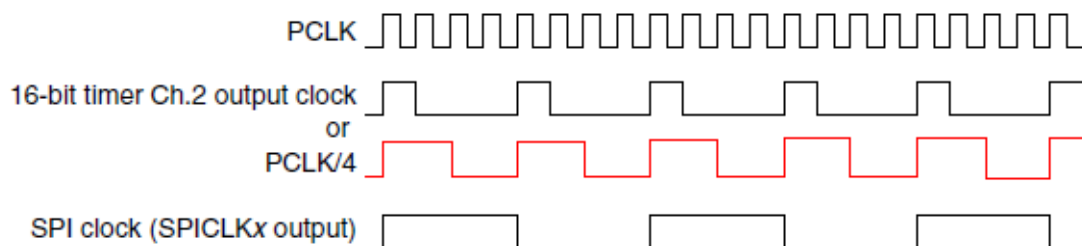Figure 15.3.1 Master Mode SPI Clock

(Correct)

Figure 15.3.1 Master Mode SPI Clock

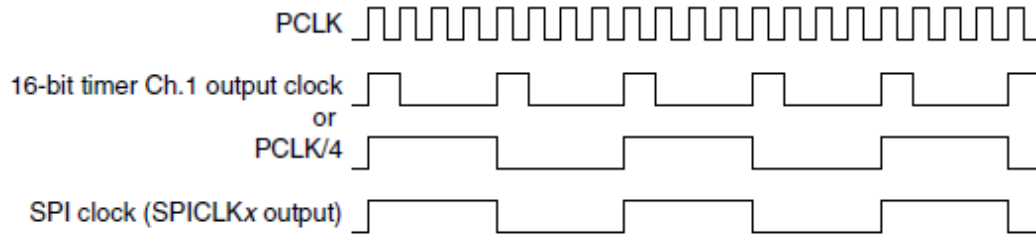**P19-3(S1C17621/S1C17602/S1C17622/S1C17604/S1C17624)**

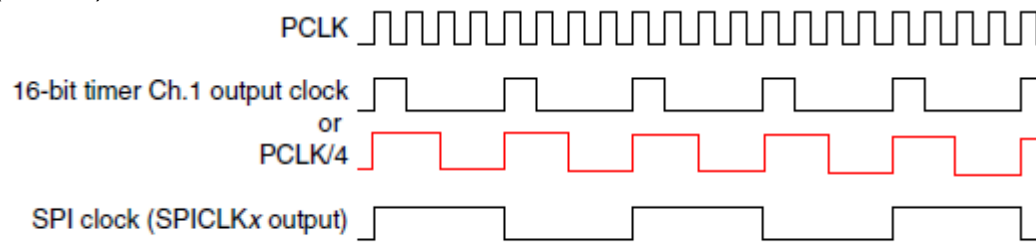(Error)

Figure 19.3.1 Master Mode SPI Clock

(Correct)

Figure 19.3.1 Master Mode SPI Clock

S1C17 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C17704 technical manual	411511902	**18.10 Precautions**	18-21
S1C17702 technical manual	411581701	**18.10 Precautions**	18-21
S1C17705 technical manual	411706600	**14.9 Control Register Details**	14-10
S1C17601 technical manual	411805700	**18.10 Precautions**	18-21
S1C17602 technical manual	411620100	**18.10 Precautions**	18-21
S1C17611 technical manual	411882300	**18.10 Precautions**	18-21
S1C17121 technical manual	411723701	**18.10 Precautions**	18-21
S1C17003 technical manual	411635101	**18.10 Precautions**	18-21

(Error)
For S1C17705
    The following UART bits should be set with transfers disabled (RXEN = 0).
    ......
    All UART_CTLx register bits other than RXEN (RBFI, TIEN, RIEN, REIEN, TEIEN)
    ......
For S1C17704
    • Before setting the bits listed below, make sure the transmit and receive operations are
     disabled (RXEN = 0).
    ......
    - All bits (RBFI, TIEN, RIEN, and REIEN except RXEN) of the UART_CTL register
    ......
For Others
    • The following UART bits should be set with transfers blocked (RXEN = 0).
    ......
    - All UART_CTL register (0x4104) bits other than RXEN (RBFI, TIEN, RIEN, REIEN)
    ......

(Correct)
• The following UART bits should be set with transfers disabled (RXEN = 0).

....

- RBFI bit in the UART_CTL*x* register

....

S1C17 Manual errata

ITEM: I2CM Interrupts			
Object manuals	Document codes	Items	Pages
S1C17701 technical manual	411089903	20.6 I2C Interrupt	20-11
S1C17704 technical manual	411511902	20.6 I2C Interrupt	20-11
S1C17702 technical manual	411581701	20.6 I2C Interrupt	20-10
S1C17705 technical manual	411706600	16.6 I2CM Interrupts	16-6
S1C17601 technical manual	411805700	20.6 I2C Master Interrupts	20-10
S1C17602 technical manual	411620100	20.6 I2C Master Interrupts	20-10
S1C17611 technical manual	411882300	20.6 I2C Master Interrupts	20-10
S1C17121 technical manual	411723701	20.6 I2C Master Interrupts	20-10
S1C17001 technical manual	411412301	20.6 I2C Interrupt	250
S1C17003 technical manual	411635101	20.6 I2C Master Interrupts	20-10

(Error)

Transmit buffer empty interrupt

To use this interrupt, set TINTE/I2CM_ICTL register to 1. If TINTE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.

If transmit buffer empty interrupts are enabled (TINTE = 1), an interrupt request is output to the ITC as soon as the transmit data set in RTDT[7:0]/I2CM_DAT register is transferred to the shift register.

An interrupt occurs if other interrupt conditions are satisfied.

Receive buffer full interrupt

To use this interrupt, set RINTE/I2CM_ICTL register to 1. If RINTE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.

If receive buffer full interrupts are enabled (RINTE = 1), an interrupt request is output to the ITC as soon as the data received in the shift register is loaded to RTDT[7:0].

An interrupt occurs if other interrupt conditions are met.

For more information on interrupt processing, see the "Interrupt Controller (ITC)" chapter.

(Correct)

Transmit buffer empty interrupt

To use this interrupt, set TINTE/I2CM_ICTL register to 1. If TINTE is set to 0 (default),

interrupt requests for this cause will not be sent to the ITC.

If transmit buffer empty interrupts are enabled (TINTE = 1), an interrupt request is output to the ITC as soon as the transmit data set in RTDT[7:0]/I2CM_DAT register is transferred to the shift register.

An interrupt occurs if other interrupt conditions are satisfied.

Transmit buffer empty interrupt occurs when the data was only sent.

- The clear method of transmit buffer empty flag

  Write the data to RTDT/I2CM_DAT.

  When TXE/I2CM_DAT is 0, the data doesn't send and the flag is only cleared.

Receive buffer full interrupt

To use this interrupt, set RINTE/I2CM_ICTL register to 1. If RINTE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.

If receive buffer full interrupts are enabled (RINTE = 1), an interrupt request is output to the ITC as soon as the data received in the shift register is loaded to RTDT[7:0].

An interrupt occurs if other interrupt conditions are met.

Receive buffer full interrupt occurs when the data was only received.

- The clear method of receive buffer full flag

  Read the data from RTDT/I2CM_DAT.

NOTE: When I2CM interrupt occurs, decide the transmit buffer empty interrupt or the receive buffer full interrupt by the program sequence of the I2C master. There're not registers to decide which interrupt occurred.

For more information on interrupt processing, see the "Interrupt Controller (ITC)" chapter.

S1C17 Manual errata

ITEM: Turning Display On and Off			
Object manuals	Document codes	Items	Pages
S1C17701 technical manual	411089903	22.6.1 Turning Display On and Off	22-9
S1C17704 technical manual	411511902	22.6.1 Turning Display On and Off	22-9
S1C17702 technical manual	411581701	22.6.1 Display On and Off	22-9
S1C17705 technical manual	411706600	19.7.1 Display On and Off	19-16

(Error)

Set DSPC[1:0] to 0x1 to display normally. However, the clock must be supplied in advance (see Section 22.3).

(Correct)

Set DSPC[1:0] to 0x1 to display normally. However, the clock must be supplied in advance (see Section 22.3). When DSPC[1:0] set to anything except 0x0 before the clock is sourced, the LCD voltage can't be generated right. In this case, set back DSPC[1:0] to 0x0 . After the clock be supplied, set again DSPC[1:0] to anything except 0x0.

Note: "The clock supplied state" is the state that the clock is supplied to LCD driver circuit after oscillation circuit is enable, oscillation start time and stable time through, and LCD clock set to enable.

S1C17 Manual errata

ITEM: Heavy Load Protection Function			
Object manuals	Document codes	Items	Pages
S1C17702 technical manual	411581701	4.4 Heavy Load Protection Function	4-5
S1C17705 technical manual	411706600	4.5 Heavy Load Protection Function	4-4
S1C17601 technical manual	411805700	4.4 Heavy Load Protection Function	4-4
S1C17602 technical manual	411620100	4.4 Heavy Load Protection Function	4-4
S1C17611 technical manual	411882300	4.4 Heavy Load Protection Function	4-4

(Error)

The internal logic voltage regulator enters heavy load protection mode by writing 1 to the HVLD/VD1_CTL register and it ensures stable VD1 output. Use the heavy load protection function when a heavy load such as a lamp or buzzer is driven with a port output.

(Correct)

The internal logic voltage regulator enters heavy load protection mode by writing 1 to the HVLD/VD1_CTL register and it ensures stable VD1 output. ~~Use the heavy load protection function when a heavy load such as a lamp or buzzer is driven with a port output~~. If the unstable operation occurs by programming operations as the below, Use the heavy load protection function.

● The case of driving the high current consumption such as diode, buzzer and so on by the port outputs; set the heavy load protection function to enable during driving the diode or buzzer.

● The case of having the high current consumption difference between high clock and low clock using by system clock; set the heavy load protection function to enable during several ten micro seconds from in front of the change to end of the change.

● The case of having the high current consumption difference between HALT/SLEEP mode and those releases, and of changing frequently them; set the heavy load protection function to enable during repeating their process.

NOTE: Release the heavy load protection function after the unstable operations finished. In addition, If the unstable operations occur frequently, set the heavy load protection function to enable during these operations.

S1C17 Manual errata

ITEM: Mistakes of a method to clear receive data buffer.			
Object manuals	Document codes	Items	Pages
S17C17702 Technical Manual	411581700	18 UART	18-7, 18-19, 18-21

P18-7(S1C17702)

(Error)

Setting the RXEN bit to 0 empties the transmission and receive data buffers, clearing any remaining data. The data being transferred cannot be guaranteed if RXEN is set to 0 while data is being sent or received.

(Correct)

Setting the RXEN bit to 0 empties the transmission ~~and receive~~ data buffers, clearing any remaining data. The data being transferred cannot be guaranteed if RXEN is set to 0 while data is being sent or received.

P18-19(S1C17702)

(Error) **D0 RXEN: UART Enable Bit**

Enables the UART to transmit/receive data.

1 (R/W): Enable

0 (R/W): Disable (default)

Before the UART can transmit/receive data, RXEN must be set to 1. When RXEN is set to 0, data transmission/reception is disabled.

Always make sure RXEN = 0 before setting the transfer conditions.

Writing 0 to RXEN also clears the transmit/receive data buffers.

(Correct) **D0 RXEN: UART Enable Bit**

Enables the UART to transmit/receive data.

1 (R/W): Enable

0 (R/W): Disable (default)

Before the UART can transmit/receive data, RXEN must be set to 1. When RXEN is set to 0, data transmission/reception is disabled.

Always make sure RXEN = 0 before setting the transfer conditions.

Writing 0 to RXEN also clears the transmit~~/receive~~ data buffer~~s~~.

P18-21(S1C17702)

(Error)

Preventing transfer by setting RXEN to 0 clears (initializes) transfer data buffers. Before writing 0 to RXEN, confirm the absence of data in the buffers awaiting transmission or

reading.
(Correct) Preventing transfer by setting RXEN to 0 clears (initializes) transfer data buffers. Before writing 0 to RXEN, confirm the absence of data in the buffers awaiting transmission ~~or reading~~.

S1C17 Manual errata

ITEM: Mistakes of a method to reset of receive err flags.			
Object manuals	Document codes	Items	Pages
S17C17702 Technical Manual	411581700	18 UART	18-14

P18-14(S1C17702)

(Error) **D6 FER: Framing Error Flag Bit**

Indicates whether a framing error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

FER is set to 1 when a framing error occurs. Framing errors occur when data is received with the stop bit set to 0. FER is reset by writing 1 or by setting RXEN/UART_CTL*x* register to 0.

D5 PER: Parity Error Flag Bit

Indicates whether a parity error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

PER is set to 1 when a parity error occurs. Parity checking is enabled only when PREN/ UART_MOD*x* register is set to 1 and is performed when received data is transferred from the shift register to the receive data buffer. PER is reset by writing 1 or by setting RXEN/UART_CTL*x* register to 0.

D4 OER: Overrun Error Flag Bit

Indicates whether an overrun error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

OER is set to 1 when an overrun error occurs. Overrun errors occur when data is received in the shift register when the receive data buffer is already full and additional data is sent. The receive data buffer is not overwritten even if this error occurs. The shift register is overwritten as soon as the error occurs.

OER is reset by writing 1 or by setting RXEN/UART_CTL*x* register to 0.

(Correct) **D6 FER: Framing Error Flag Bit**

Indicates whether a framing error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

FER is set to 1 when a framing error occurs. Framing errors occur when data is received with the stop bit set to 0. FER is reset by writing 1 ~~or by setting RXEN/UART_CTLx register to 0~~.

D5 PER: Parity Error Flag Bit

Indicates whether a parity error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

PER is set to 1 when a parity error occurs. Parity checking is enabled only when PREN/ UART_MOD*x* register is set to 1 and is performed when received data is transferred from the shift register to the receive data buffer. PER is reset by writing 1 ~~or by setting RXEN/UART_CTLx register to 0~~.

D4 OER: Overrun Error Flag Bit

Indicates whether an overrun error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

OER is set to 1 when an overrun error occurs. Overrun errors occur when data is received in the shift register when the receive data buffer is already full and additional data is sent. The receive data buffer is not overwritten even if this error occurs. The shift register is overwritten as soon as the error occurs.

OER is reset by writing 1 ~~or by setting RXEN/UART_CTLx register to 0~~.

S1C17 series Manual errata

ITEM: Addition of the attention point at the time of HSCLK switching		
Object manuals	Document code	Object number
S1C17702 Technical Manual	411581700	7-5
S1C17602 Technical Manual	411620100	7-5
S1C17121 Technical Manual	411723700	7-5

7-5 S1C17702 Technical Manual

(Error)

Note: Both the IOSC and OSC3 oscillator circuits must be turned on when selecting HSCLK. Otherwise, the system will fail to switch to HSCLK even when HSCLKSEL is written to, and the HSCLKSEL value will remain unchanged.

(Correct)

Note: Both the IOSC and OSC3 oscillator circuits must be turned on when selecting HSCLK. Otherwise, the system will fail to switch to HSCLK even when HSCLKSEL is written to, and the HSCLKSEL value will remain unchanged. Additionally, please make the PCLKEN (D[1:0]/0x5080 :0x3) enabled if you want switch HSCLK.

7-5   S1C17602/ S1C17121 Technical Manual

(Error)

Note: To select HSCLK, both of the IOSC and OSC3 must be turned on. Writing to HSCLKSEL while both of them are not turned on does not switch HSCLK, and does not change the HSCLKSEL value.

(Correct)

Note: To select HSCLK, both of the IOSC and OSC3 must be turned on. Writing to HSCLKSEL while both of them are not turned on does not switch HSCLK, and does not change the HSCLKSEL value. Additionally, please make the PCLKEN (D[1:0]/0x5080 :0x3) enabled if you want switch HSCLK.

S1C17 Series Manual errata

ITEM: Error in list of instructions		
Object manuals	Document code	Object number
S1C17701 Technical Manual	411089902	2-5
S1C17704 Technical Manual	411511901	2-5
S1C17702 Technical Manual	411581700	2-5
S1C17602 Technical Manual	411620100	2-5
S1C17001 Technical Manual	411412300	2-5
S1C17003 Technical Manual	411635100	2-5
S1C17002 Technical Manual	411554401	I-5-5
S1C17501 Technical Manual	411525601	I-5-5
S1C17801 Technical Manual	411390801	I-5-5

2-5 (S1C17701, S1C17704, S1C17702, S1C17602, S1C17001, S1C17003) /

I-5-5 (S1C17501, S1C17801, S1C17002)

(Error)

Branch	jpa	imm7	Absolute jump
	ipa.d	%rb	Delayed branching possible

(Correct)

Branch	jpa	imm7	Absolute jump
	jpa.d	%rb	Delayed branching possible

S1C17 Series Manual errata

ITEM: Correct operating temperatures		
Object manuals	Document code	Object number
S1C17702 Technical Manual	411581700	1-2
S1C17602 Technical Manual	411620100	1-2

1-2
(Error) ●Operating temperatures　　　・-20°C to 70°C
(Correct) ●Operating temperatures　　　・-25°C to 70°C

S1C17 Series Manual errata

ITEM: Delete ITC from peripheral modules that use PCLK		
Object manuals	Document code	Object number
S1C17702 Technical Manual	411581700	7-1, 8-1, AP-35, 8-3, 8-5, 8-7, AP-36
S1C17602 Technical Manual	411620100	7-1, 8-1, AP-38, 8-3, 8-5, 8-7, AP-39
S1C17003 Technical Manual	411635100	7-1, 8-1, AP-31, 8-3, 8-5, 8-7, AP-32

7-1, 8-1, AP-35 (S1C17702) / 7-1, 8-1, AP-38 (S1C17602) / 7-1, 8-1, AP-31 (S1C17003)

(Error)
    (In figure, ITC is included in the block that connect to PCLK)

(Correct)
    (Delete ITC from the block that connect to PCLK)

8-3, 8-5, 8-7, AP-36 (S1C17702) / 8-3, 8-5, 8-7, AP-39 (S1C17602) / 8-3, 8-5, 8-7, AP-32 (S1C17003)

(Error)
- 8-bit timer Ch.0 & Ch.1
- 16-bit timer Ch.0 to 2
- Interrupt controller
- SPI
- I2C

(Correct)
- 8-bit timer Ch.0 & Ch.1
- 16-bit timer Ch.0 to 2
- ~~Interrupt controller~~
- SPI
- I2C

S1C17702 Manual errata

ITEM: Description about OSC3 external clock input		
Object manuals	Document code	Object number
S1C17702	411581700	7-3, 27-7

7-3

(Error)

  (There is no description about OSC3 external clock input)

(Correct)

External clock input of OSC3

  The clock can be input to the OSC3 pin from external. To stop the external clock, stop it at the VSS level. Forinformation about input clock waveforms, refer to "27 Electrical Characteristics."

27-7

(Error)

Input rising edge time	tCR			80	ns
Input drop-off time	tCF			80	ns

(Correct)

Input rising edge time	tCR			80	ns
Input drop-off time	tCF			80	ns
OSC3 clock cycle time	tOSC3	125			ns
OSC3 clock input duty	tOSC3D	46		54	%

S1C17 Series Manual errata

ITEM: SPICLK frequency limitation in SPI slave mode		
Object manuals	Document code	Object number
S1C17001 Technical Manual	411412300	235
S1C17701 Technical Manual	411089902	19-3
S1C17602 Technical Manual	411620100	19-3
S1C17702 Technical Manual	411581700	19-3
S1C17002 Technical Manual	411554401	V-4-3, V-5-3
S1C17501 Technical Manual	411525601	VI-3-3, VI-4-3
S1C17801 Technical Manual	411390801	VI-3-3, VI-4-3

1-2

(Error)

Note: The frequency of the clock input via the SPICLK pin must be less than 1/3 of the PCLK and have a clock duty ratio of 50%.

```
(Timing Chart)
```

Figure 19.3.2   Slave mode SPI clock

(Correct)

Note: The duty ratio of the clock input via the SPICLK pin must be less than 1/3 of the PCLK and have a clock duty ratio of 50%.
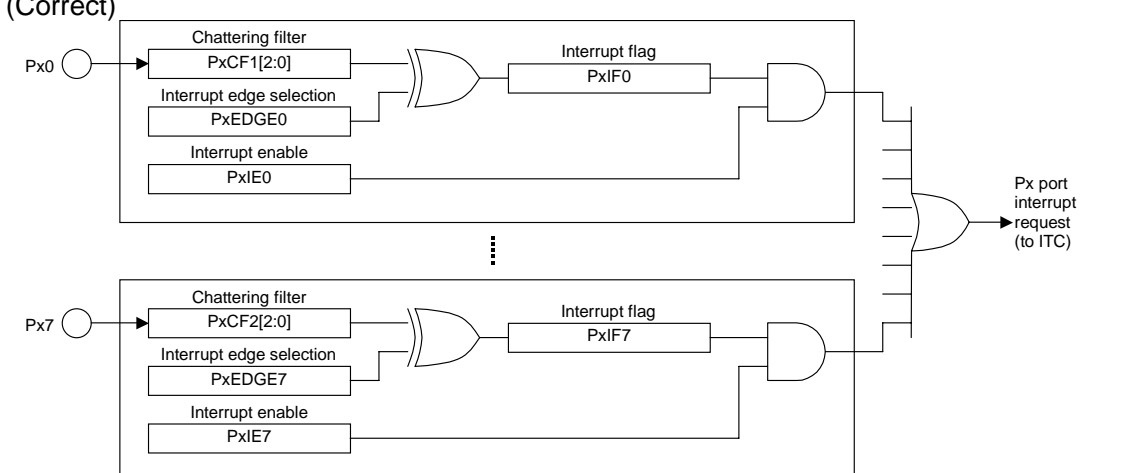
```
(Timing Chart)
```

Figure 19.3.2   Slave mode SPI clock

S1C17702 Manual errata

ITEM: SVD comparison voltage settings		
Object manuals	Document code	Object number
S1C17702	411581700	1-2, 23-2, 23-7, AP-22

1-2

(Error)

Power supply voltage detection (SVD) circuit • 16-value programmable (1.7 V to 3.2 V)

(Correct)

Power supply voltage detection (SVD) circuit • 15-value programmable (1.8 V to 3.2 V)

23-2

(Error)

0x0	1.7V

(Correct)

0x0	reserved

23-7

(Error)

				0x0	1.7V			

(Correct)

				0x0	reserved			

(Error)

0x0	1.7V

(Correct)

0x0	reserved

AP-22

| (Error) | | | | | | 0x0 | 1.7V | | | |

| (Correct) | | | | | | 0x0 | reserved | | | |

S1C17702 Manual errata

ITEM: Reset condition of DSPC[1:0] register		
Object manuals	Document code	Object number
S1C17702	411581700	P22-9, P22-14

(Error)

DSPC[1:0] is reset to 0x0 (Display off) at initial reset or when the slp instruction is executed.

(Correct)

DSPC[1:0] is reset to 0x0 (Display off) at initial reset.

DSPC[1:0] is not reset to 0x0 (Display off) when the slp instruction is executed.

Please execute slp instruction after DSPC [1:0] is reset to 0x0 (indication Off) with software, because there is the fear that causes LCD depleted, in the case that the slp command is run at the time of the liquid crystal indication.

S1C17702 Manual errata

ITEM: Configulation and description of P Port input interrupt.		
Object manuals	Document code	Object number
S1C17702 technical manual	411581700	P10-8, P10-9, P10-18

(Error)

  (Figure 10.7.1 is different)

(Correct)

Figure 10.7.1   Port input interrupt circuit configulation

(Error)

Interrupt flags

The ITC is able to accept interrupt requests for both P0 and P1 port interrupts, and the P port module contains interrupt flags P*x*IF[7:0] corresponding to the individual 16 ports to enable individual control of the 16 P0[7:0] and P1[7:0] port interrupts. Setting the corresponding P*x*IE[7:0] to 1 sets P*x*IF[7:0] to 1 at the specified edge(rising or falling edge) of the input signal. A P0 or P1 port interrupt request signal is also output to the ITC at the same time. Meeting the ITC and S1C17 core interrupt conditions generates an interrupt.

(Correct)

Interrupt flags

The ITC is able to accept interrupt requests for both P0 and P1 port interrupts, and the P port module contains interrupt flags P*x*IF[7:0] corresponding to the individual 16 ports to enable individual control of the 16 P0[7:0] and P1[7:0] port interrupts. ~~Setting the corresponding P*x*IE[7:0] to 1 sets~~ P*x*IF[7:0] will be set to 1 at the specified edge(rising or falling edge) of the input signal. A P0 or P1 port interrupt request signal is also output to the ITC at the same time if the corresponding PxIE[7:0] is set to 1. Meeting the ITC and S1C17 core interrupt conditions generates an interrupt.

(Error)

PxIF[7:0] are interrupt flags corresponding to the individual 16 ports of P0[7:0] and P1[7:0]. Setting the corresponding PxIE[7:0] (Px_IMSK register) to 1 sets PxIF[7:0] to 1 at the specified edge (rising or falling edge) of the input signal. A P0 or P1 port interrupt request signal is also output to the ITC at the same time. This interrupt request signal causes the P0/P1 port interrupt flag inside the ITC to be set to 1. Meeting the ITC and S1C17 core interrupt conditions generates an interrupt.

(Correct)

PxIF[7:0] are interrupt flags corresponding to the individual 16 ports of P0[7:0] and P1[7:0]. ~~Setting the corresponding PxIE[7:0] (Px_IMSK register) to 1 sets~~ PxIF[7:0] will be set to 1 at the specified edge (rising or falling edge) of the input signal. A P0 or P1 port interrupt request signal is also output to the ITC at the same time if the corresponding PxIE[7:0] is set to 1. This interrupt request signal causes the P0/P1 port interrupt flag inside the ITC to be set to 1. Meeting the ITC and S1C17 core interrupt conditions generates an interrupt.