

## S1C17 Technical Manual Errata

ITEM: USI/USIL AC Characteristics					
Object manual	Document code	Object ITEM	Page		
S1C17803 Technical Manual	411820401	30.7.3 USI AC Characteristics	30-10		
30-10					
(Error)					
<b>SPI master mode (8 or 9 bits, normal mode)</b>					
Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 4.5 to 5.5V, VSS = 0V					
Item	Symbol	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	85 + tPCLK	-	-	ns
spi_sdi setup time	tSDS	85 + tPCLK	-	-	ns
Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 2.7 to 3.6V, VSS = 0V					
Item	Symbol	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	85 + tPCLK	-	-	ns
spi_sdi setup time	tSDS	85 + tPCLK	-	-	ns
<b>SPI master mode (8 or 9 bits, fast mode)</b>					
Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 4.5 to 5.5V, VSS = 0V					
Item	記号	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	85	-	-	ns
spi_sdi setup time	tSDS	85	-	-	ns
Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 2.7 to 3.6V, VSS = 0V					
Item	記号	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	85	-	-	ns
spi_sdi setup time	tSDS	85	-	-	ns
(Correct)					
<b>SPI master mode (8 or 9 bits, normal mode)</b>					
Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 4.5 to 5.5V, VSS = 0V					
Item	Symbol	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	<b>(85 + tPCLK) x 2</b>	-	-	ns
spi_sdi setup time	tSDS	85 + tPCLK	-	-	ns
Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 2.7 to 3.6V, VSS = 0V					
Item	Symbol	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	<b>(85 + tPCLK) x 2</b>	-	-	ns
spi_sdi setup time	tSDS	85 + tPCLK	-	-	ns

**SPI master mode (8 or 9 bits, fast mode)**

Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1\_VDD/IO2\_VDD= 4.5 to 5.5V, VSS = 0V

Item	記号	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	<b>85 x 2</b>	-	-	ns
spi_sdi setup time	tSDS	85	-	-	ns

Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1\_VDD/IO2\_VDD= 2.7 to 3.6V, VSS = 0V

Item	記号	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	<b>85 x 2</b>	-	-	ns
spi_sdi setup time	tSDS	85	-	-	ns

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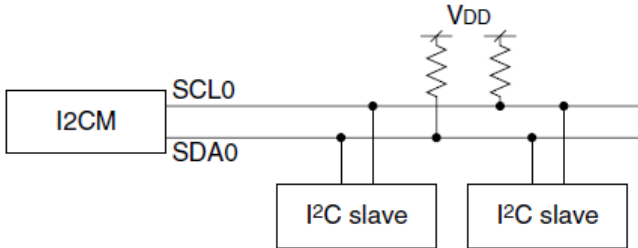
ITEM I2C Slave Input/Output Pins			
Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	21.2 I2C Slave Input/Output Pins	21-2
S1C17611 Technical Manual	411882301	21.2 I2C Slave Input/Output Pins	21-2
S1C17706 Technical Manual	412026401	18.2 I2CS Input/Output Pins	18-1
S1C17002 Technical Manual	411554402	V.3.2 I2C Slave I/O Pins	V-3-2
S1C17003 Technical Manual	411635102	21.2 I2C Slave Input/Output Pins	21-2
S1C17803 Technical Manual	411820401	21.2 I2CS Input/Output Pins	21-2

(Addition)

Note: The pins go to high impedance status when the port function is switched. The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDD with an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.

The diagram illustrates the I2C bus configuration. An I2C master is connected to the SDA1 and SCL1 pins of an I2CS (I2C Slave) and an I2C slave. The SDA1 and SCL1 lines are pulled up to VDD with resistors to ensure they are in a high state when not driven by the master.

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ITEM I2C Master Input/Output Pins			
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S1C17601 Technical Manual	411805701	20.2 I2C Master Input/Output Pins	20-2
S1C17611 Technical Manual	411882301	20.2 I2C Master Input/Output Pins	20-2
S1C17701 Technical Manual	411089904	20.2 I2C I/O Pins	20-2
S1C17704 Technical Manual	411511903	20.2 I2C I/O Pins	20-2
S1C17706 Technical Manual	412026401	17.2 I2CM Input/Output Pins	17-1
S1C17001 Technical Manual	411412301	20.2 I2C Input/Output Pins	252
S1C17002 Technical Manual	411554402	V.2.2 I2C Master I/O Pins	V-2-2
S1C17003 Technical Manual	411635102	20.2 I2C Master Input/Output Pins	20-2
S1C17501 Technical Manual	411525602	VI.2.2 I2C I/O Pins	VI-2-2
S1C17801 Technical Manual	411390802	VI.2.2 I2C I/O Pins	VI-2-2
S1C17803 Technical Manual	411820401	20.2 I2CM Input/Output Pins	20-2
<p>(Addition)</p> <p>Note: The pins go to high impedance status when the port function is switched.</p> <p>The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDD with an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.</p> 			

## S1C17 Family Technical Manual Errata

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(Error)

### **4.7 Precautions on Power Supply**

#### **Power-on sequence**

In order to operate the device normally, supply power in accordance with the following timing.

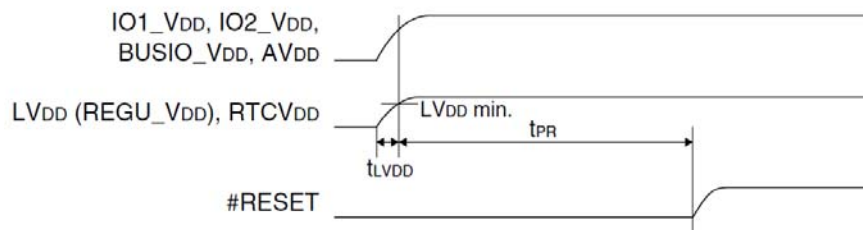


Figure 4.7.1 Power-On Sequence

(1) tLVDD: Elapsed time until the power supply stabilizes after power-on

Supply power in the following sequence.

Power-on: 1. LVDD (and RTCVDD) or REGU\_VDD

2. BUSIO\_VDD, IO1\_VDD, IO2\_VDD, AVDD (May be applied with 1 above at the same time.)

3. Apply the input signal

\* The RTCVDD can be always supplied to the chip to operate the RTC and BBRAM.

(2) tPR: Power-on-reset time

Keep the #RESET signal low for this period. See “Electrical Characteristics” for the power-on-reset time.

(Correct)

## 4.7 Precautions on Power Supply

### Power-on sequence

In order to operate the device normally, supply power in accordance with the following timing.

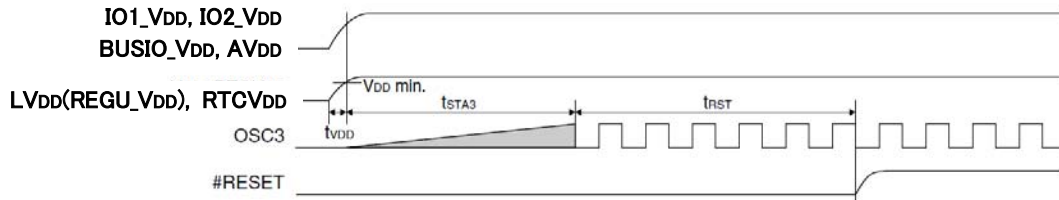


Figure 4.7.1 Power-On Sequence

(1) t<sub>VDD</sub>: Elapsed time until the power supply stabilizes after power-on

Supply power in the following sequence.

Power-on: 1. LV<sub>DD</sub> (and RTCV<sub>DD</sub>) or REGU\_V<sub>DD</sub>

2. BUSIO\_V<sub>DD</sub>, IO1\_V<sub>DD</sub>, IO2\_V<sub>DD</sub>, AV<sub>DD</sub> (May be applied with 1 above at the same time.)

3. Apply the input signal

\* The RTCV<sub>DD</sub> can be always supplied to the chip to operate the RTC and BBRAM.

(2) t<sub>STA3</sub>: Time at which OSC3 oscillation starts

(3) t<sub>RST</sub>: Minimum reset pulse width

Time at which the clock supplied to the chip stabilizes plus at least six clocks; Keep the #RESET signal low.