

S1C31 Manual errata

ITEM: Real-Time Clock (RTCA) Theoretical Regulation Function			
Object manuals	Document codes	Items	Pages
S1C31W74 Technical Manual	413374500	10.3.2 Theoretical Regulation Function	10-2
S1C31D01 Technical Manual	413520400	10.3.2 Theoretical Regulation Function	10-2
<p>(Error)</p> <p>10.3.2 Theoretical Regulation Function</p> <p>The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.</p> <ol style="list-style-type: none"> 1. Measure the frequency tolerance “m [ppm]” of f_{OSC1}. 2. Determine the theoretical regulation execution cycle time “n seconds.” 3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2. 4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt. 5. Monitor the RTC1S signal to check that every n-second cycle has no error included. <p>The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two’s-complement number. Use Eq. 9.1 to calculate the correction value.</p> <p>n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.RTCTRM[6:0] bits periodically via software) m: OSC1 frequency tolerance [ppm]</p>			
<p>(Correct)</p> <p>10.3.2 Theoretical Regulation Function</p> <p>The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.</p> <ol style="list-style-type: none"> 1. Determine the correction value of frequency tolerance “m [ppm] = - $\{(f_{OSC1}-32768[Hz]) / 32768[Hz]\} \times 10^6$” by measuring the f_{OSC1}. 2. Determine the theoretical regulation execution cycle time “n seconds.” 3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2. 4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt. 5. Monitor the RTC1S signal to check that every n-second cycle has no error included. 			

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two's-complement number. Use Eq. 9.1 to calculate the correction value.

n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.RTCTRM[6:0] bits periodically via software)

m: OSC1's correction value of frequency tolerance [ppm]

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ITEM: LCD Driver Operations			
Object manuals	Document codes	Items	Pages
S1C31W74 Technical Manual	413374500	20.5.2 Display On/Off	20-8
<p>(Error)</p> <p>When “Display off” is selected, the drive voltage supply stops and the LCD driver pin outputs are all set to VSS level. Since “All on” and “All off” directly control the driving waveform output by the LCD driver, data in the display data RAM is not altered. The common pins are set to dynamic drive for “All on” and to static drive for “All off.” This function can be used to make the display flash on and off without altering the display memory.</p>			
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ITEM: Flash Memory Pin																							
Object manuals	Document codes	Items	Pages																				
S1C31W74 Technical Manual	413374500	1.3.3 Pin Descriptions 4.3.1 Flash Memory Pin 24 Basic External Connection Diagram	1-8 4-2 24-1																				
<p>(Error)</p> <p>1.3.3 Pin Descriptions</p> <p style="text-align: center;">Table 1.3.3.1 Pin Description</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <thead> <tr> <th style="width: 10%;">P26</th> <th style="width: 15%;">P26</th> <th style="width: 10%;">I/O</th> <th style="width: 10%;">Hi-Z</th> <th style="width: 10%;">-</th> <th style="width: 45%;">I/O port</th> </tr> </thead> <tbody> <tr> <td></td> <td>EXOSC</td> <td>I</td> <td></td> <td></td> <td>Clock generator external clock input</td> </tr> </tbody> </table> <p>4.3.1 Flash Memory Pin</p> <p style="text-align: center;">Table 4.3.1.1 Flash Memory Pin</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <thead> <tr> <th style="width: 20%;">Pin name</th> <th style="width: 15%;">I/O</th> <th style="width: 15%;">Initial status</th> <th style="width: 50%;">Function</th> </tr> </thead> <tbody> <tr> <td>V_{PP}</td> <td>P</td> <td>-</td> <td>Flash programming power supply</td> </tr> </tbody> </table> <p>For the V_{PP} voltage, refer to “Recommended Operating Conditions, Flash programming voltage V_{PP}” in the “Electrical Characteristics” chapter.</p> <p>Note: Always leave the V_{PP} pin open except when programming the Flash memory.</p> <p>24 Basic External Connection Diagram</p> <div style="text-align: center; margin: 10px 0;"> </div>				P26	P26	I/O	Hi-Z	-	I/O port		EXOSC	I			Clock generator external clock input	Pin name	I/O	Initial status	Function	V _{PP}	P	-	Flash programming power supply
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4.3.1 Flash Memory Pin

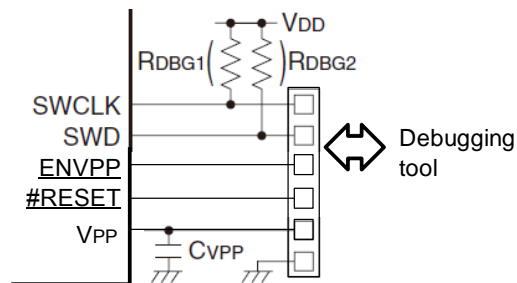
Table 4.3.1.1 Flash Memory Pin

Pin name	I/O	Initial status	Function
V _{PP}	P	-	Flash programming power supply
(ENV _{PP})	O or Hi-Z	Hi-Z	Flash programming control signal output

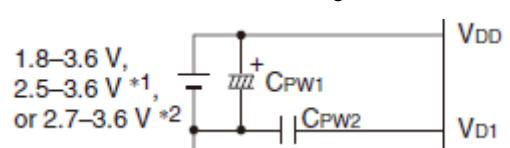
For the V_{PP} voltage, refer to “Recommended Operating Conditions, Flash programming voltage V_{PP}” in the “Electrical Characteristics” chapter.

Note: Always leave the V_{PP} pin open except when programming the Flash memory.

24 Basic External Connection Diagram



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ITEM Flash Programming																																		
Object manual	Document code	item	Page																															
S1C31W74 Technical Manual	413374500	1.1 Features	1-2																															
		4.3.3 Flash Programming	4-2																															
		23.2 Recommended Operating Conditions	23-1																															
		24 Basic External Connection Diagram	24-1																															
		Appendix C Mounting Precautions	AP-C-1																															
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<p>The Flash memory supports on-board programming, so it can be programmed using a flash loader.</p> <p>The VPP voltage can be supplied from either an external power supply or the internal voltage booster.</p> <p>Choose the flash loader according to the VPP power supply to be used.</p> <p>Notes: When the internal voltage booster is used, 2.7 V or more V_{DD} voltage is required.</p>																																		
23.2 Recommended Operating Conditions																																		
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Item</th> <th style="width: 10%;">Symbol</th> <th style="width: 25%;">Condition</th> <th style="width: 5%;">Min.</th> <th style="width: 5%;">Typ.</th> <th style="width: 5%;">Max.</th> <th style="width: 5%;">Unit</th> </tr> </thead> <tbody> <tr> <td rowspan="3">Power supply voltage</td> <td rowspan="3">VDD</td> <td>For normal operation</td> <td>1.8</td> <td>-</td> <td>3.6</td> <td>V</td> </tr> <tr> <td>For Flash programming</td> <td>2.7</td> <td>-</td> <td>3.6</td> <td>V</td> </tr> <tr> <td>For LCD driver operation</td> <td>2.5</td> <td>-</td> <td>3.6</td> <td>V</td> </tr> <tr> <td>Capacitor between V_{SS} and V_{PP}</td> <td>CVPP</td> <td>*5</td> <td>-</td> <td>0.1</td> <td>-</td> <td>μF</td> </tr> </tbody> </table>				Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Power supply voltage	VDD	For normal operation	1.8	-	3.6	V	For Flash programming	2.7	-	3.6	V	For LCD driver operation	2.5	-	3.6	V	Capacitor between V _{SS} and V _{PP}	CVPP	*5	-	0.1	-	μF
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24 Basic External Connection Diagram																																		
 <p style="margin-left: 20px;">1.8-3.6 V, 2.5-3.6 V *1, or 2.7-3.6 V *2</p>																																		
*1: When the LCD driver is used																																		
*2: For Flash programming (when VPP is generated internally)																																		

Appendix C Mounting Precautions

VPP pin

If fluctuations in the Flash programming voltage VPP is large, connect a capacitor CVPP between the VSS and VPP pins to suppress fluctuations within VPP ± 1 V. The CVPP should be placed as close to the VPP pin as possible and use a sufficiently thick wiring pattern that allows current of several tens of mA to flow.

(Correct)

1.1 Features

Power supply voltage	
VDD operating voltage	1.8 to 3.6 V
VDD operating voltage for Flash programming	2.4 to 3.6 V (when VPP is supplied externally) 2.7 to 3.6 V (when VPP is generated internally)
VDD operating voltage when LCD driver is used	2.5 to 3.6 V

4.3.3 Flash Programming

The Flash memory supports on-board programming, so it can be programmed using a flash loader. The VPP voltage can be supplied from either an external power supply or the internal voltage booster. The VPP voltage can also be generated by the internal power supply for generating the Flash programming voltage. Be sure to connect a capacitor CVPP between the VSS and VPP pins for stabilizing the voltage when the VPP voltage is supplied externally or for generating the voltage when the internal power supply is used. The VPP pin must be left open except when programming the Flash memory. However, it is not necessary to disconnect the wire when using "Bridge Board (S5U1C31001L)" to supply the VPP voltage, as Bridge Board controls the power supply so that it will be supplied during Flash programming only.

- Notes:
- When the VPP voltage is supplied externally, 2.4 V or more VDD voltage is required.
 - When the VPP voltage is generated internally, 2.7 V or more VDD voltage is required
 - Be sure to avoid using the VPP pin output for driving external circuits when the VPP voltage is generated internally.

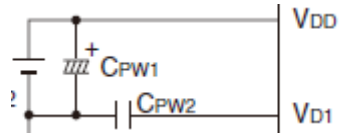
23.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max	Unit	
Power supply voltage	VDD	For normal operation	1.8	-	3.6	V	
		For Flash programming	When VPP is supplied externally	2.4	-	3.6	V
			When VPP is generated internally	2.7	-	3.6	V
		For LCD driver operation	2.5	-	3.6	V	
Capacitor between VSS and VPP	CVPP	*5	-	0.1	-	µF	

~~*5 CVPP should be connected only when the VPP voltage is not stable.~~

24 Basic External Connection Diagram

1.8-3.6V,
2.5-3.6V*1,
2.4-3.6V*2,
or 2.7-3.6V*3



*1: When the LCD driver is used

*2: For Flash programming (when VPP is supplied externally)

*3: For Flash programming (when VPP is generated internally)

Appendix C Mounting Precautions

VPP pin

~~If fluctuations in the Flash programming voltage VPP is large,~~ Connect a capacitor CVPP between the VSS and VPP pins to suppress fluctuations within $VPP \pm 1$ V. The CVPP should be placed as close to the VPP pin as possible and use a sufficiently thick wiring pattern that allows current of several tens of mA to flow.